Intel StrataFlash® Wireless Memory (L18 SCSP)

*768-Mbit L18 Family with Synchronous PSRAM*

Datasheet

Product Features

- Device Architecture
  — Flash Die Density: 128 or 256-Mbit
  — PSRAM Die Density: 32 or 64-Mbit
  — x16 Non-Mux or ADMux I/O Interface Option
  — Bottom or Top Flash Parameter Configuration
- Device Voltage
  — Core: V_{CC} = 1.8 V
  — I/O: V_{CCQ} = 1.8 V
- Device Packaging
  — Ballout: QUAD+ (88 Balls)
  — Area: 8x10 mm to 11x13 mm
  — Height: 1.2 mm to 1.4 mm
- PSRAM Performance
  — 70 ns Initial Read Access; 20 ns Asynchronous Page-Mode Read
  — Up to 54 MHz with 9 ns Clock-to-Data Synchronous Burst-Mode Reads and Writes
  — Configurable 4-, 8-, 16- and Continuous-Word Burst-Length Reads and Writes
  — Partial-Array Self and Temperature-Compensated Refresh
  — Programmable Output Impedance

- Flash Performance
  — 85 ns Initial Read Access; 25 ns Asynchronous Page-Mode Read
  — Up to 54 MHz with 14 ns Clock-to-Data Output Synchronous Burst-Mode Read
  — Buffered Enhanced Factory Programming (BEFP): 5 μs/byte (typ.)
  — Write-buffer program: 7 μs/Byte (typ.)
- Flash Architecture
  — Read-While-Write/Erase
  — Asymmetrical blocking structure
  — 8-Mbit or 16-Mbit partition sizes
  — 16-Kword parameter blocks (Top or Bottom); 64-Kword main blocks
  — 2-Kbit One-Time Programmable Protection Register
  — Zero-latency block locking
  — Absolute write protection with block lock using F-VPP and F-WP#
- Flash Software
  — Intel® FDI, Intel® PSM, and Intel® VFM
  — Common Flash Interface
  — Basic and Extended Flash Command Set
- Quality and Reliability
  — Extended Temperature –25 °C to +85 °C
  — Minimum 100K Flash Block Erase cycles
  — 130 nm ETOX™ VIII Flash Technology

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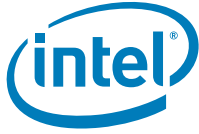
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Contents

Figures

Tables

Revision History

Date	Revision	Description
August 2006	-001	Initial release to public web.

1.0   Introduction

This document contains information pertaining to the *768-Mbit LQ Family with Synchronous PSRAM* stacked device family. The L18 is available as a Non-Multiplex or Address-Data Muxltiplex (ADMux) I/O interface option, while the synchronous PSRAM is available only as a Non-Multiplex I/O interface. The intent of this document is to provide information where this product differs from the *Intel StrataFlash® Wireless Memory (L18 SCSP)* device.

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory (L18 SCSP)* Discrete Datasheet (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for specific flash product details not included in this document.

The 768-Mbit Intel StrataFlash® Wireless memory with synchronous PSRAM stacked device family offers multiple high-performance solutions. The L18 (Non-Mux or ADMux I/O interface option) highlighted features like asymmetrical block array, configurable burst lengths, security using OTP and zero-latency block lock. The L18 delivers up to 54 MHz synchronous burst and page-mode read rates with multi-partitioning Read-While-Write and Read-While-Erase operations. The synchronous PSRAM (Non-Mux I/O interface) is a high-performance volatile memory operating at speeds up to 54 MHz with configurable burst lengths. The PSRAM lower sixteen addresses can be routed to the data pins on the PCB board to enable a flexible flash and PSRAM A/D-Mux I/O interface device design. The L18 stacked device features 1.8 volt low-voltage operation in an Intel® QUAD+ standard footprint and signal ballouts.

1.1   Nomenclature

1.8 Volt Core	VCC (memory subsystem die core) voltage range of 1.7 V – 1.95 V.
1.8 Volt I/O	VCCQ (memory subsystem I/O) voltage range of 1.7 V – 1.95 V.
ADMux I/O	Address-Data Multiplex I/O interface, where the lower sixteen (16) addresses are multiplexed on the data pins (DQ[15:0]) during any address cycle.
Asserted	Signal with logical voltage level V_{IL}, or enabled.
Block	Group of cells, bits, bytes, or words within the flash memory array that get erased with one erase instruction.
Deasserted	Signal with logical voltage level VIH or disabled.
Device	A specific memory type or stacked flash and xRAM memory density configuration combination within a memory subsystem product family.
Die	Individual flash or xRAM die used in a stacked package memory device.
High-Z	High Impedance.
Low-Z	Signal is Driven on the bus.
Non-Array Reads	Flash reads which return flash Device Identifier, CFI Query, Protection Register, and Status Register information.
Non-Mux I/O	Traditional parallel flash interface where address are not multiplex onto the data pins. All address and data pins are unique.
Partition	A group of flash blocks that shares common status register read state.
Program	An operation to Write data to the flash array or xRAM.
Write	Bus cycle operation at the inputs of the flash or xRAM die, in which a command or data are sent to the flash array or xRAM.

1.2 Acronyms

APS	Automatic Power Savings
EFA	Extended Flash Array
BCR	(PSRAM) Bus Control Register
Buffered EFP	Buffered Enhanced Factory Programming
CR	(Flash) Configuration Register
CSP	Chip Scale Package
MLC	Multi-Level Cell
OTP	One-Time Programmable
PLR	Protection Lock Register
PR	Protection Register
RCR	(PSRAM) Refresh Control Register
RFU	Reserved for Future Use
RWW / RWE	Read-While-Write / Read-While-Erase
SR	Status Register
WSM	Write State Machine

1.3 Conventions

A5	Denotes one element of a signal group, in this case address bit 5.
Clear	Logical zero (0).
DQ[15:0]	Denotes a group of similarly named signals, such as data bus.
F-CE#	Denotes Chip Enable of the flash die, where "F" to denote the specific signal suffix and "CE#" is the root signal name of the NOR flash die.
P-CE# or P-CS#	Denotes Chip Enable of the PSRAM die, where "P" to denote the specific signal suffix and "CE# or CS#" are the root signal name of the PSRAM die. PSRAM CE# and CS# is used interchangably throughout the document.
S-CS1#	Denotes Chip Enable of the SRAM die, where "S" to denote the specific signal suffix and "CS1#" is the root signal name of the SRAM die.
Set	Logical one (1).
SR4	A flash status register bit, in this case status register bit 4 of SR[15:0].
VCC	Signal or voltage connection.
V_{CC}	Signal or voltage level.
VSS	Denotes a global power signal of the stacked device. VSS is common to all memory dies within a stacked memory device.

2.0 Functional Overview

2.1 Product Description

The L18 family with synchronous PSRAM stacked product family encompasses multiple L18 flash memory plus synchronous PSRAM die combinations.

Figure 1 shows the maximum configuration options for L18 non-multiplex I/O (standard) product and Figure 2 shows the maximum configuration options for L18 AD-Multiplex I/O product family with synchronous PSRAM internal package connections.

Table 1 on page 13 lists the available L18 flash with synchronous PSRAM stacked combinations within the L18 stacked device product family.

Figure 1. L18 Product Family with Sync PSRAM Block Diagram
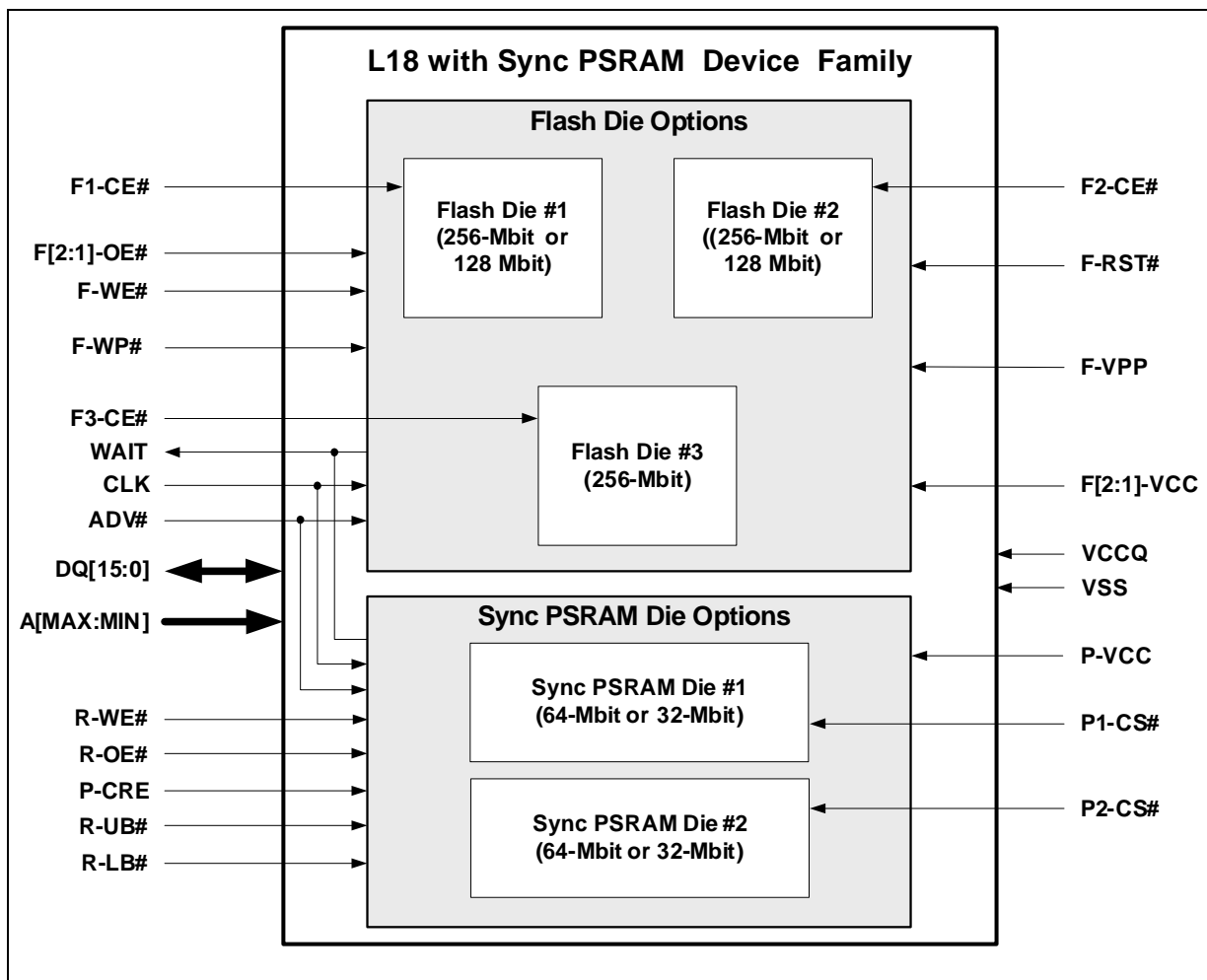
Notes:
1. F2-OE# must be treated as an RFU. However, for compatiblity to future products, F2-OE# can be tied to F1-OE# or left floated.
2. F2-VCC must be treated as an RFU. However, for compatibility to future products, F2-VCC can be tied to F1-VCC or left floated.
3. See Table 8 on page 26 for signal description details.

Figure 2.   L18 ADMux I/O Interface Product Family with Sync PSRAM Block Diagram
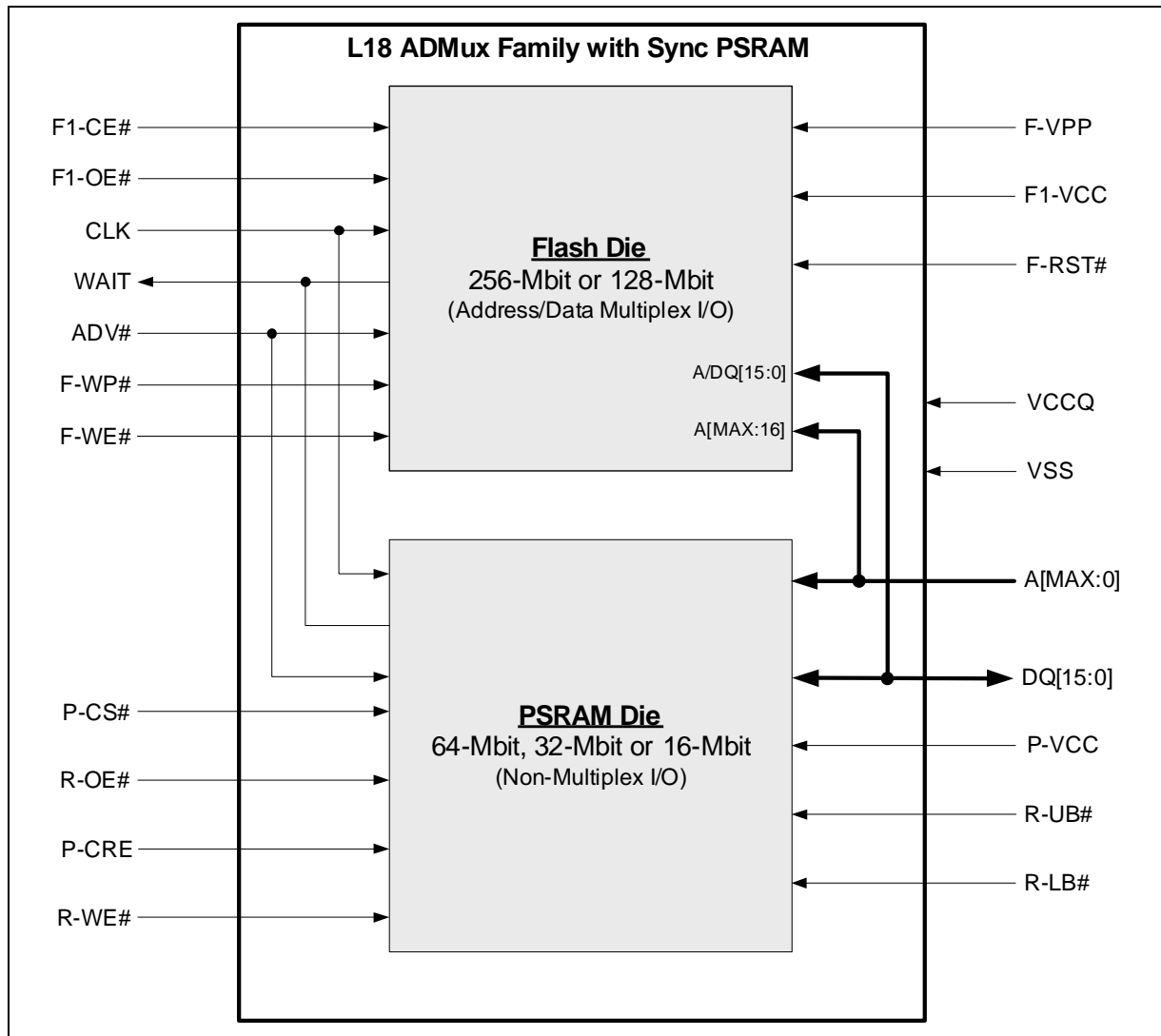
Notes:
1.   F2-OE# must be treated as an RFU. However, for compatiblity to future products, F2-OE# can be tied to F1-OE# or left floated.
2.   F2-VCC must be treated as an RFU. However, for compatibility to future products, F2-VCC can be tied to F1-VCC or left floated.
3.   See Table 8 on page 26 for signal description details.

2.2 Available Device Combinations

Table 1. Available L18 with Synchronous PSRAM Device Combinations

I/O Voltage	Flash Type (Mbit)	xRAM Type (Mbit)	Package Size (mm)	Package Ballout
1.8 V	128 L18	32 Sync PSRAM	8x10x1.2	QUAD+
	128 L18	64 Sync PSRAM	8x10x1.2	QUAD+
	256 L18	64 Sync PSRAM	8x11x1.2	QUAD+
	256 L18	64 + 64 Sync PSRAM	8x11x1.4	QUAD+
	256 +128 L18	64 Sync PSRAM	8x11x1.4	QUAD+
	256 + 256 L18	64 Sync PSRAM	8x11x1.4	QUAD+
	256 + 256 L18	64 + 64 Sync PSRAM	11x13x1.4	QUAD+
	128 L18 (ADMux I/O)	32 Sync PSRAM	8x10x1.2	QUAD+
	128 L18 (ADMux I/O)	64 Sync PSRAM	8x10x1.2	QUAD+
	256 L18 (ADMux I/O)	32 Sync PSRAM	8x11x1.2	QUAD+

Note: For combination not listed in Table 1, contact your local Intel Sales Representative for details. For ordering information, see Table 28, "Available Product Ordering Information" on page 70 for details.

2.3　Device Operation Overview

The following sections describes the bus operations and device state between the flash and synchronous PSRAM. Bus operations for the L18 stacked device involve the control of flash and PRAM inputs. The bus operations are shown in Table 2.

Note:　See the *Intel StrataFlash® Wireless Memory (L18 SCSP)* Discrete Datasheet (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for complete descriptions of the flash modes and commands, command bus-cycle definitions, and flowcharts that illustrate operational routines not documented in this Datasheet.

Table 2.　Flash and PSRAM Device Bus Operations

Device	Mode	F-RST#	F-CE#	F-OE#	F-WE#	ADV#[8]	F-VPP	P-CRE#	P-CS#	R-OE#	R-WE#	R-UB#, R-LB#	DQ[15:0]	WAIT[7]	Notes
Flash (#1, #2, or #3)	Synchronous Array and Non-Array Read	H	L	L	H	L	X	X	H	X	X	X	Flash D_{OUT}	Active	1,2,4
	Asynchronous Read	H	L	L	H	X	X	X	H	X	X	X	Flash D_{OUT}	Deasserted	1,2,4
	Write	H	L	H	L	L	V_{PPL} or V_{PPH}	X	H	X	X	X	Flash D_{IN}	Deasserted	1,2,3
	Output Disable	H	L	H	H	X	X	Any PSRAM mode allowed					Flash High-Z	Flash High-Z	1,2
	Standby	H	H	X	X	X	X						Flash High-Z	Flash High-Z	1,2
	Reset	L	X	X	X	X	X						Flash High-Z	Flash High-Z	1,2
PSRAM (#1 or #2)	Read	X	H	X	X	X	X	L	L	L	H	L	PSRAM D_{OUT}	Active	1,2,5,7
	Write	X	H	X	X	X	X	L	L	H	L	L	PSRAM D_{IN}	Active	1,2,5,7
	Output Disable	Any Flash mode allowed						L	L	H	H	X	PSRAM High-Z	PSRAM High-Z	1,2
	Standby							L	H	X	X	X	PSRAM High-Z	PSRAM High-Z	1,2
	Low Power Mode							X	X	X	X	X	PSRAM High-Z	PSRAM High-Z	1,2

Notes:
1.　For flash, do not simultaneously assert F-OE# and F-WE#. For PSRAM, do not simultaneously assert R-OE# and R-WE#.
2.　X can be V_{IL} or V_{IH} for flash or xRAM inputs; V_{PPLK}, V_{PPL}, or V_{PPH} for F-VPP.
3.　Refer to the latest revision of the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: *Non-Mux I/O doc #251902* and *ADMux I/O doc #313295)* for valid D_{IN} during Flash writes.
4.　Flash CFI query and Status Register accesses, use DQ[7:0] only. All other reads use DQ[15:0].
5.　P-CRE# is *low* if PSRAM is in standby. P-CRE# is *X* if PSRAM is in Low-Power mode. See Section 12.0, "PSRAM Device Operation" on page 54 for more details about Standby and Low Power mode.
6.　WAIT indicates data validity only when in Synchronous mode. Ignore this setting in Asynchronous and Page-mode.
7.　The Flash and Synchronous PSRAM dies share the WAIT signal.
8.　During AD-Mux I/O operation, ADV# must remain deasserted during the data phase.

Table 3. PSRAM Bus Operation

State	Operation Modes	Power Mode	CLK	P-CS#	ADV#	R-WE#	R-OE#	R-UB# R-LB#	P-CRE	A19/A18	Addr.	DQ	Notes
Read	Asynchronous	Active	L	L	L	H	L	L	L	V	V	DOUT	
Write	Asynchronous NOR-Flash	Active	L	L	L	L	X	L	L	V	V	DIN	1,2
Set Control Register	Asynchronous NOR-Flash	Active	L	L	L	L	H	X	H	LL HL	RCR BCR	X	
Fetch Control Register	Asynchronous	Active	L	L	L	H	L	L	H	LL HL LH	X	RCR BCR	
No Operation	Asynchronous Synchronous NOR-Flash	Standby /Active	L	L	H	H	H	X	L	X	X	High-Z	3
Deselect	Asynchronous Synchronous NOR-Flash	Standby	L	H	X	X	X	X	X	X	X	High-Z	
Deep Power Down	Asynchronous Synchronous NOR-Flash	Deep Power Down	L	H	X	X	X	X	X	X	X	High-Z	
Burst Init Read	Synchronous NOR-Flash	Active	L->H	L	L	H	X	L	L	V	V	X	4
Burst Read	Synchronous NOR-Flash	Active	L->H	L	H	X	L	L	X	X	X	DOUT	4,5
Burst Init Write	Synchronous	Active	L->H	L	L	L	H	X	L	V	V	X	4
Burst Write	Synchronous	Active	L->H	L	H	X	X	L	X	X	X	DIN	4
Set Control Register	Synchronous	Active	L->H	L	L	L	H	X	H	LL HL	RCR BCR	X	4
Fetch Control Register	Synchronous	Active	L->H	L	L	H	L	L	H	LL HL LH	X	RCR BCR	4,6

Notes:
1. The table reflects behavior if R-UB# and R-LB# are asserted low. If only either of the signals, R-UB# or R-LB# is asserted low only the corresponding data byte will be written (UB# enables DQ15-DQ8, LB# enables DQ7-DQ0).
2. During a write access invoked by R-WE# set to low the R-OE# signal is ignored.
3. Power mode of Standby or Active will depend on the internal operation of device at the time.
4. Clock configuration is rising edge.
5. Output drivers are controlled by the asynchronous R-OE# control signal.
6. During the initial command cycle R-OE# is don't care (X) and subsequent cycles it must be low (L)

2.4 Flash Memory Map and Partitioning

The *768-Mbit LQ Family with Synchronous PSRAM* is available in several density and parameter configurations. The memory map is based on stacking individual 128-Mbit and 256-Mbit flash die density options, and shows individual flash die configurations and block/partition allocations. See the following figures and tables:

- Figure 3, "LQ Family Flash Die Configurations: Top Parameter" on page 16
- Figure 4, "LQ Family Flash Die Configurations: Bottom Parameter" on page 17
- Table 4, "Flash-CE# Assignment and Device Parameter Configuration" on page 17
- Table 5, "One or Two Flash Dies SCSP Memory Map" on page 18
- Table 6, "3-Flash Dies (Top Parameter) SCSP Memory Map" on page 19
- Table 7, "3-Flash Dies (Bottom Parameter) SCSP Memory Map" on page 20

Figure 3.   LQ Family Flash Die Configurations: Top Parameter
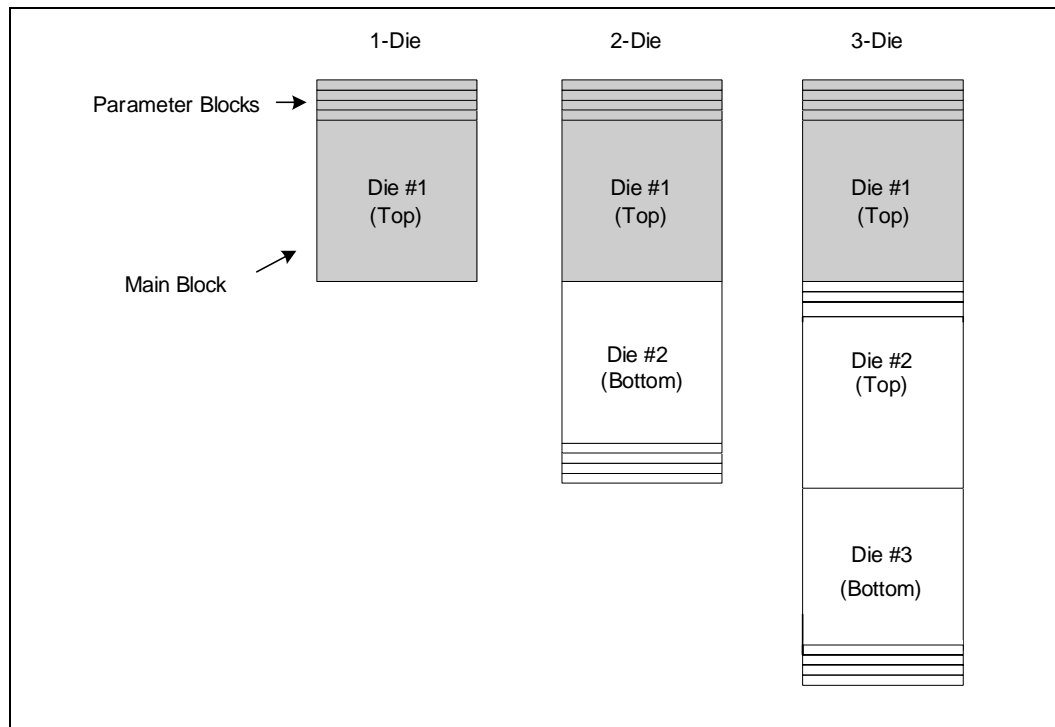
Figure 4.   LQ Family Flash Die Configurations: Bottom Parameter
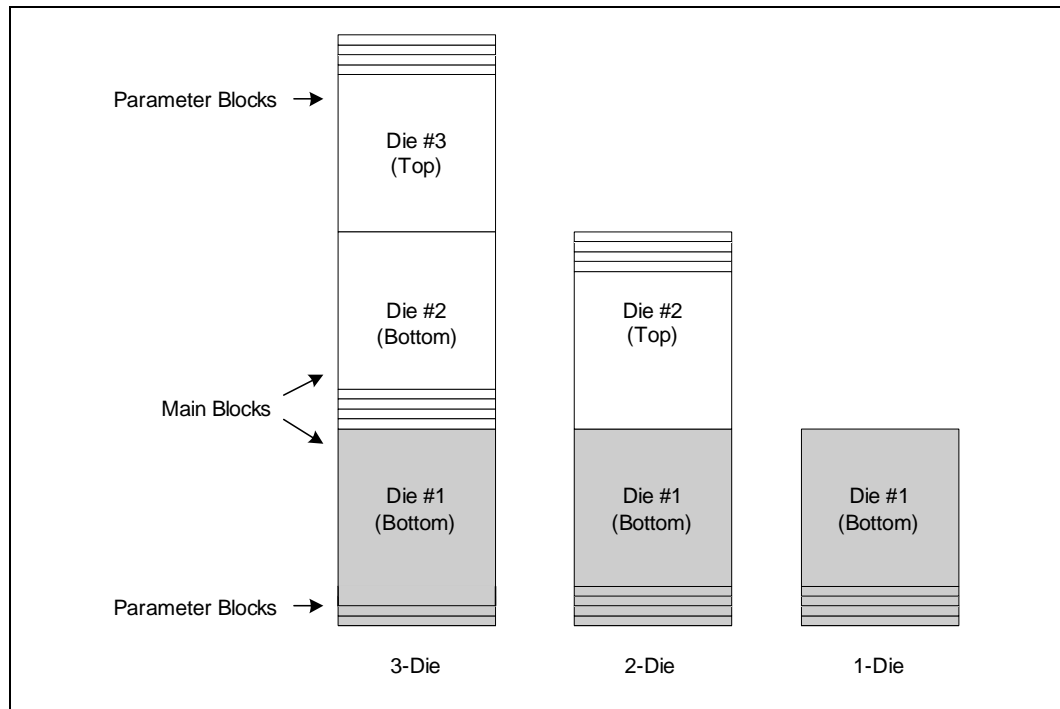
Table 4 shows the flash chip enable assignment within a stacked device, while Table 5 to Table 7 shows an example of the memory map and partitioning information for combinations with up to three flash dies in the L18 SCSP LQ family with Synchronous PSRAM.

Table 4.   Flash-CE# Assignment and Device Parameter Configuration

Device Parameter	Stacked Combinations	Flash Die #1	Flash Die #2	Flash Die #3
Top Parameter	One Flash Die	F1-CE# (Top)	—	—
	Two Flash Dies	F1-CE# (Top)	F2-CE# (Bottom)	—
	Three Flash Dies	F1-CE# (Top)	F2-CE# (Top)	F3-CE# (Bottom)
Bottom Parameter	One Flash Die	F1-CE# (Bottom)	—	—
	Two Flash Dies	F1-CE# (Bottom)	F2-CE# (Top)	—
	Three Flash Dies	F1-CE# (Bottom)	F2-CE# (Bottom)	F3-CE# (Top)

Table 5. One or Two Flash Dies SCSP Memory Map

Flash Die Type	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
				Blk#	Address Range		Blk#	Address Range
Flash die (Top Parameter) 128-Mbit or 256-Mbit	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
		⋮		⋮	⋮		⋮	⋮
		16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
		64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
		⋮		⋮	⋮		⋮	⋮
		64		120	780000-78FFFF		240	F00000-FFFFFF
	Main Partitions (Partition 1-7)	64	8	119	770000-77FFFF	16	239	EF0000-EFFFFF
		⋮		⋮	⋮		⋮	⋮
		64		64	400000-4FFFFF		128	800000-80FFFF
	Main Partitions (Partition 8-15)	64	8	63	3F0000-3FFFFF	16	127	F70000-F7FFFF
		⋮		⋮	⋮		⋮	⋮
		64		0	000000-00FFFF		0	000000-00FFFF
Flash die (Bottom Parameter) 128-Mbit or 256-Mbit	Main Partitions (Partition 8-15)	64	8	130	7F0000-7FFFFF	16	258	FF0000-FFFFFF
		⋮		⋮	⋮		⋮	⋮
		64		67	400000-40FFFF		131	100000-10FFFF
	Main Partitions (Partition 1-7)	64	8	66	3F0000-3FFFFF	16	130	7F0000-7FFFFF
		⋮		⋮	⋮		⋮	⋮
		64		11	080000-08FFFF		19	100000-10FFFF
	Parameter Partition (Partition 0)	64	8	10	070000-07FFFF	16	18	0F0000-0FFFFF
		⋮		⋮	⋮		⋮	⋮
		64		4	010000-01FFFF		4	010000-01FFFF
		16		3	00C000-00FFFF		3	00C000-00FFFF
		⋮		⋮	⋮		⋮	⋮
		16		0	000000-003FFF		0	000000-003FFF

Table 6. 3-Flash Dies (Top Parameter) SCSP Memory Map

Flash Die Type	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
				Blk	Address Range		Blk	Address Range
Flash die #1 (Top Parameter) 128-Mbit or 256-Mbit	Parameter Partition (Partition 0)	16	8	13	7FC000-7FFFFF	16	258	FFC000-FFFFFF
		⋮		⋮	⋮		⋮	⋮
		16		12	7F0000-7F3FFF		255	FF0000-FF3FFF
		64		12	7E0000-7EFFFF		254	FE0000-FEFFFF
		⋮		⋮	⋮		⋮	⋮
		64		12	780000-78FFFF		240	F00000-FFFFFF
	Main Partitions (Partition 1-7)	64	8	11	770000-77FFFF	16	239	EF0000-EFFFFF
		⋮		⋮	⋮		⋮	⋮
		64		64	400000-4FFFFF		128	800000-80FFFF
	Main Partitions (Partition 8-15)	64	8	63	3F0000-3FFFFF	16	127	F70000-F7FFFF
		⋮		⋮	⋮		⋮	⋮
		64		0	000000-00FFFF		0	000000-00FFFF
Flash die #2 (Top Parameter) 128-Mbit or 256-Mbit	Parameter Partition (Partition 0)	16	8	13	7FC000-7FFFFF	16	258	FFC000-FFFFFF
		⋮		⋮	⋮		⋮	⋮
		16		12	7F0000-7F3FFF		255	FF0000-FF3FFF
		64		12	7E0000-7EFFFF		254	FE0000-FEFFFF
		⋮		⋮	⋮		⋮	⋮
		64		12	780000-78FFFF		240	F00000-FFFFFF
	Main Partitions (Partition 1 to 7)	64	8	11	770000-77FFFF	16	239	EF0000-EFFFFF
		⋮		⋮	⋮		⋮	⋮
		64		64	400000-4FFFFF		128	800000-80FFFF
	Main Partitions (Partition 8 to 15)	64	8	63	3F0000-3FFFFF	16	127	F70000-F7FFFF
		⋮		⋮	⋮		⋮	⋮
		64		0	000000-00FFFF		0	000000-00FFFF
Flash die #3 (Bottom Parameter) 128-Mbit or 256-Mbit	Main Partitions (Partition 8 to 15)	64	8	13	7F0000-7FFFFF	16	258	FF0000-FFFFFF
		⋮		⋮	⋮		⋮	⋮
		64		67	400000-40FFFF		131	100000-10FFFF
	Main Partitions (Partition 1 to 7)	64	8	66	3F0000-3FFFFF	16	130	7F0000-7FFFFF
		⋮		⋮	⋮		⋮	⋮
		64		11	080000-08FFFF		19	100000-10FFFF
	Parameter Partition (Partition 0)	64	8	10	070000-07FFFF	16	18	0F0000-0FFFFF
		⋮		⋮	⋮		⋮	⋮
		64		4	010000-01FFFF		4	010000-01FFFF
		16		3	00C000-00FFFF		3	00C000-00FFFF
		⋮		⋮	⋮		⋮	⋮
		16		0	000000-003FFF		0	000000-003FFF

Table 7. 3-Flash Dies (Bottom Parameter) SCSP Memory Map

Flash Die Type	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
				Blk	Address Range		Blk	Address Range
Flash die #3 (Top Parameter) 128-Mbit or 256-Mbit	Parameter Partition (Partition 0)	16		130	7FC000-7FFFFF		25	FFC000-FFFFFF
		⋮	8	⋮	⋮	16	⋮	⋮
		16		127	7F0000-7F3FFF		25	FF0000-FF3FFF
		64		126	7E0000-7EFFFF		25	FE0000-FEFFFF
		⋮		⋮	⋮		⋮	⋮
		64		120	780000-78FFFF		24	F00000-FFFFFF
	Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		23	EF0000-EFFFFF
		⋮	8	⋮	⋮	16	⋮	⋮
		64		64	400000-4FFFFF		12	800000-80FFFF
	Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		12	F70000-F7FFFF
		⋮	8	⋮	⋮	16	⋮	⋮
		64		0	000000-00FFFF		0	000000-00FFFF
Flash die #2 (Bottom Parameter) 128-Mbit or 256-Mbit	Main Partitions (Partition 8 to 15)	64		130	7F0000-7FFFFF		25	FF0000-FFFFFF
		⋮	8	⋮	⋮	16	⋮	⋮
		64		67	400000-40FFFF		13	100000-10FFFF
	Main Partitions (Partition 1 to 7)	64		66	3F0000-3FFFFF		13	7F0000-7FFFFF
		⋮	8	⋮	⋮	16	⋮	⋮
		64		11	080000-08FFFF		11	080000-08FFFF
	Parameter Partition (Partition 0)	64		10	070000-07FFFF		10	070000-07FFFF
		⋮		⋮	⋮		⋮	⋮
		64		4	010000-01FFFF		4	010000-01FFFF
		16	8	3	00C000-00FFFF	16	3	00C000-00FFFF
		⋮		⋮	⋮		⋮	⋮
		16		0	000000-003FFF		0	000000-003FFF
Flash die #1 (Bottom Parameter) 128-Mbit or 256-Mbit	Main Partitions (Partition 8 to 15)	64		130	7F0000-7FFFFF		25	FF0000-FFFFFF
		⋮	8	⋮	⋮	16	⋮	⋮
		64		67	400000-40FFFF		13	100000-10FFFF
	Main Partitions (Partition 1 to 7)	64		66	3F0000-3FFFFF		13	7F0000-7FFFFF
		⋮	8	⋮	⋮	16	⋮	⋮
		64		11	080000-08FFFF		19	100000-10FFFF
	Parameter Partition (Partition 0)	64		10	070000-07FFFF		18	0F0000-0FFFFF
		⋮		⋮	⋮		⋮	⋮
		64		4	010000-01FFFF		4	010000-01FFFF
		16	8	3	00C000-00FFFF	16	3	00C000-00FFFF
		⋮		⋮	⋮		⋮	⋮
		16		0	000000-003FFF		0	000000-003FFF

3.0   Device Package Information

Figure 5 shows the QUAD+ package ballout mechanical dimensions for available devices within the 768-Mbit L18 family with synchronous PSRAM.

Figure 5.   Mechanical Specifications for QUAD+ Ballout Package (8x10x1.2 mm)

			Millimeters				Inches	
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

Figure 6. Mechanical Specifications for QUAD+ Ballout Package (8x11x1.2 mm)

Drawing not to scale.

Dimensions	Symbol	Millimeters			Notes	Inches		
		Min	Nom	Max		Min	Nom	Max
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.900	11.000	11.100		0.4291	0.4331	0.4370
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 7. Mechanical Specifications for QUAD+ Ballout Package (8x11x1.4 mm)

Drawing not to scale.

Dimensions	Symbol	Millimeters			Notes	Inches		
		Min	Nom	Max		Min	Nom	Max
Package Height	A			1.400				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.900	11.000	11.100		0.4291	0.4331	0.4370
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 8. Mechanical Specifications for QUAD+ Ballout Package (11x13x1.4 mm)

Top View - Ball Down

Bottom View - Ball Up

Drawing not to scale.

Dimensions	Symbol	Millimeters			Notes	Inches		
		Min	Nom	Max		Min	Nom	Max
Package Height	A			1.400				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	12.900	13.000	13.100		0.5079	0.5118	0.5157
Package Body Width	E	10.900	11.000	11.100		0.4291	0.4331	0.4370
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	2.600	2.700	2.800		0.1024	0.1063	0.1102
Corner to Ball A1 Distance Along D	S2	2.000	2.100	2.200		0.0787	0.0827	0.0866

Note: For other mechanical drawings not shown in this document, contact your local Intel Sales representative for additional details.

4.0 Ballout and Signal Descriptions

4.1 Device Signal Ballout

Figure 9 shows the L18 family with synchronous PSRAM in the QUAD+ package ballout.

Figure 9. QUAD+ Ballout

Pin 1

	1	2	3	4	5	6	7	8	
A	DU	DU					DU	DU	A
B	A4	A18	A19	VSS	F1-VCC	F2-VCC	A21	A11	B
C	A5	R-LB#	A23	VSS	S-CS2	CLK	A22	A12	C
D	A3	A17	A24	F-VPP	R-WE#	P1-CS#	A9	A13	D
E	A2	A7	A25	F-WP#	ADV#	A20	A10	A15	E
F	A1	A6	R-UB#	F-RST#	F-WE#	A8	A14	A16	F
G	A0	DQ8	DQ2	DQ10	DQ5	DQ13	WAIT	F2-CE#	G
H	R-OE#	DQ0	DQ1	DQ3	DQ12	DQ14	DQ7	F2-OE#	H
J	S-CS1#	F1-OE#	DQ9	DQ11	DQ4	DQ6	DQ15	VCCQ	J
K	F1-CE#	P2-CS#	F3-CE#	S-VCC	P-VCC	F2-VCC	VCCQ	P-Mode# / P-CRE	K
L	VSS	VSS	VCCQ	F1-VCC	VSS	VSS	VSS	VSS	L
M	DU	DU					DU	DU	M
	1	2	3	4	5	6	7	8	

Top View - Ball Side Down

Legend:		
		Active Signals
		De-Populated Balls
		Do Not Use

Note: See Figure 1, "L18 Product Family with Sync PSRAM Block Diagram" on page 11 for electrical connections details.

4.2 Signal Descriptions

Table 8 describes the ballout signals for the L18 device family.

Table 8.   Signal Descriptions (Sheet 1 of 3)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
A[MAX:0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 • 64-Mbit: AMAX = A21 • 32-Mbit: AMAX = A20 • A0 is the lowest-order word address. • Unused address inputs should be treated as RFU. *Note:* During AD-Mux I/O operation, L18 A[MAX:16] can be treated as a NC pins, but C_L will exist on the pins.	1
DQ[15:0]	Input / Output	**DATA INPUT/OUTPUTS:** Global device signals. Inputs data and commands during Write cycles, outputs data during Read cycles. Data signals are High-Z when the device is deselected or its output is disabled.	
Address and Data Signals, A/D-Mux			
DQ[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** AD-Mux I/O flash signals. During AD-Mux Read cycles, DQ[15:0] are used to input the lower address followed by read-data output. During AD-Mux Write cycles, DQ[15:0] are used to input the lower address followed by commands or data. • DQ[15:0] are High-Z when the device is deselected or its output is disabled. • DQ[15:0] is only used with AD-Mux I/O flash device.	1
Control Signals			
ADV#	Input	**ADDRESS VALID:** Flash- and Synchronous PSRAM-specific signal; low-true input. During a synchronous read operation, the address is latched on the rising edge of ADV# or on the next valid CLK edge with ADV# low, whichever occurs first. • In an asynchronous flash read operation, the address is latched on the rising edge of ADV#, or continuously flows through while ADV# is low. • During a synchronous flash Read operation, the address is latched on the rising edge of ADV# or the first active CLK edge whichever occurs first. . • During synchronous PSRAM read and synchronous write modes, the address is either latched on the first rising clock edge after ADV# assertion or on the rising edge of ADV# whichever edge occurs first. In asynchronous read and asynchronous write modes, ADV# can be used to latch the address, but can be held low for the entire operation as well. *Note:* During AD-Mux I/O operation, ADV# must remain deasserted during the data phase.	
F[3:1]-CE#	Input	**FLASH CHIP ENABLE:** Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[3:2]-CE# are dedicated to flash die #3 through #2, respectively, if present. Otherwise, any unused flash chip enable should be treated as RFU.	
CLK	Input	**CLOCK:** Flash- and Synchronous PSRAM-specific input signal. CLK synchronizes the flash and/or synchronous PSRAM with the system clock during synchronous operations.	
F[2:1]-OE#	Input	**FLASH OUTPUT ENABLE:** Flash-specific signal; low-true input. When low, F-OE# enables the output drivers of the selected flash die. When high, F-OE# disables the output drivers of the selected flash die and places the output drivers in High-Z. • F2-OE# common to all other flash dies, if present. Otherwise it is an RFU, however, it is highly recommended to always common F1-OE# and F2-OE# on the PCB.	

Table 8.   Signal Descriptions (Sheet 2 of 3)

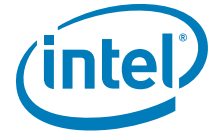| Symbol	Type	Signal Descriptions	Notes
R-OE#	Input	**RAM OUTPUT ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-OE# enables the output drivers of the selected memory die. When high, R-OE# disables the output drivers of the selected memory die and places the output drivers in High-Z if present. Otherwise it is an RFU.	3
F-RST#	Input	**FLASH RESET:** Flash-specific signal; low-true input. When low, F-RST# resets internal operations and inhibits writes. When high, F-RST# enables normal operation.	
WAIT	Output	**WAIT:** Flash- and Synchronous PSRAM-specific signal; configurable true-level output. When asserted, WAIT indicates invalid output data. When deasserted, WAIT indicates valid output data. • WAIT is driven whenever the flash or the synchronous PSRAM is selected and its output enable is low. • WAIT is High-Z whenever flash or the synchronous PSRAM is deselected, or its output enable is high. • Flash and PSRAM must configure the WAIT RCR bit to be the same true-level state.	
F-WE#	Input	**FLASH WRITE ENABLE:** Flash-specific signal; low-true input. When low, F-WE# enables Write operations for the enabled flash die. Address and data are latched on the rising edge of F-WE#.	
R-WE#	Input	**RAM WRITE ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-WE# enables Write operations for the selected memory die. Data is latched on the rising edge of R-WE# if present. Otherwise it is an RFU.	3
F-WP#	Input	**FLASH WRITE PROTECT:** Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command.	
P-CRE	Input	**PSRAM CONTROL REGISTER ENABLE:** Synchronous PSRAM-specific signal; high-true input. When high, P-CRE enables access to the PSRAM Refresh Control Register (P-RCR) or Bus Control Register (P-BCR). When low, P-CRE enables normal Read or Write operations if present. Otherwise it is an RFU.	2
P-MODE#	Input	**PSRAM MODE#:** Asynchronous only PSRAM-specific signal; low-true input. When low, P-MODE# enables access to the PSRAM configuration register, and to enter or exit Low-Power mode. When high, P-MODE# enables normal Read or Write operations if present. Otherwise it is an RFU.	2
P[2:1]-CS#	Input	**PSRAM CHIP SELECT:** PSRAM-specific signal; low-true input. When low, P-CS# selects the associated PSRAM memory die. When high, P-CS# deselects the associated PSRAM die. PSRAM die power is reduced to standby levels, and its data and WAIT outputs are placed in a High-Z state. • P1-CS# is dedicated to PSRAM die #1 if present. Otherwise it is an RFU. • P2-CS# is dedicated to PSRAM die #2 if present. Otherwise it is an RFU.	3
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM-specific signals; S-CS1# low-true input, S-CS2 high-true input. When both S-CS1# and S-CS2 are asserted, the SRAM die is selected. When either S-CS1# or S-CS2 is deasserted, the SRAM die is deselected. • S-CS1# and S-CS2 are dedicated to SRAM if present. Otherwise it is an RFU.	3
R-UB# R-LB#	Input	**RAM UPPER/LOWER BYTE ENABLES:** PSRAM- and SRAM-specific signals; low-true inputs. When low, R-UB# enables DQ[15:8] and R-LB# enables DQ[7:0] during PSRAM or SRAM Read and Write cycles. When high, R-UB# masks DQ[15:8] and R-LB# masks DQ[7:0] if present. Otherwise it is an RFU.	3
Power Signals			
F-VPP	Power	**FLASH PROGRAM/ERASE VOLTAGE:** Flash specific. F-VPP supplies program or erase power to the flash die.	
F[2:1]-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. • F[2:1]-VCC supplies the core power to the flash dies. • F2-VCC is recommended to be tied to F1-VCC, else it is an RFU.	
VCCQ	Power	**I/O POWER SUPPLY:** Global device I/O power. VCCQ supplies the device input/output driver voltage.	

Table 8. Signal Descriptions (Sheet 3 of 3)

Symbol	Type	Signal Descriptions	Notes
P-VCC	Power	**PSRAM CORE POWER SUPPLY:** PSRAM specific. P-VCC supplies the core power to the PSRAM die if present. Otherwise it is an RFU.	3
S-VCC	Power	**SRAM POWER SUPPLY:** SRAM specific. S-VCC supplies the core power to the SRAM die if present. Otherwise it is an RFU.	3
VSS	Ground	**DEVICE GROUND:** Global ground reference for all signals and power supplies. Connect all VSS balls to system ground. Do not float any VSS connections.	
DU	—	**DO NOT USE:** This ball should not be connected to any power supplies, signals, or other balls. This ball can be left floating.	
RFU	—	RESERVED for FUTURE USE: Reserved by Intel for future device functionality and enhancement. This ball must be left floating.	

Notes:
1. Only used when AD-Mux I/O flash is present
2. P-CRE and P-Mode share the same package ball location. Only one signal function is available, depending on the stacked device combination.
3. Only available on stacked device combinations with PSRAM, and/or SRAM die. Otherwise, it should be treated as RFU.

5.0 Maximum Ratings and Operating Conditions

5.1 Device Absolute Maximum Ratings

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only.

Table 9. Device Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Device Case Temperature Under Bias	−25	+85	°C	
Storage Temperature	−55	+125	°C	
Voltage On Any Signal (Except for F-V_{CC}, F-V_{PP}, P-V_{CC}, V_{CCQ}, and S-V_{CC})	−0.2	2.25	V	1,3
F-V_{CC} Voltage	−0.2	+2.45	V	1,2
V_{CCQ}, P-V_{CC}, and Optional S-V_{CC} Voltage	−0.2	+2.45	V	1,3
F-V_{PP} Voltage	−0.2	+10.0	V	1,4
I_{SH} (Output Short Circuit Current)	—	+50	mA	5

Notes:
1. Voltage is referenced to V_{SS}.
2. During power transitions, minimum DC voltage may undershoot to −2.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CC} (operating max) + 2.0 V for periods < 20 ns.
3. During power transitions, minimum DC voltage may undershoot to −1.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CCQ} (operating max) + 1.0 V for periods < 20 ns.
4. During power transitions, minimum DC voltage may undershoot to −2.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{PPH} (operating max) + 2.0 V for periods < 20 ns.
5. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Device Operating Conditions

Warning: Operation beyond the Operating Conditions is not recommended and extended exposure may affect device reliability.

Table 10. Device Operating Conditions

Symbol	Parameter	Test Condition	Flash + xRAM Min	Flash + xRAM Max	Unit
T_C	Device Case Operating Temperature	—	−25	+85	°C
F-V_{CC}	Flash Supply Voltage	—	+1.7	+2.0	V
V_{CCQ}, P-V_{CC}, S-V_{CC}	Flash and PSRAM I/O Voltage PSRAM and SRAM Supply Voltage	—	+1.7	+1.95	V
V_{PPL}	F-V_{PP} (Flash Programming Voltage Supply, Logic Level)	—	−0.9	+2.0	V
V_{PPH}	F-V_{PP} (Flash Factory Word Programming Voltage Supply)	—	+8.5	+9.5	V
Block Erase Cycles	Flash Main Array and EFA Blocks	$V_{PP} = V_{CC}$	100,000	—	Cycles
		$V_{PP} = V_{PPH}$	—	1000	Cycles

Note: In typical operation, the F-VPP program voltage is V_{PPL}. F-VPP can be connected to 8.5 V - 9.5 V for a maximum of 80 cumulative hours or 1000 cycles on the main array blocks.

5.3 Device Power-Up/Down
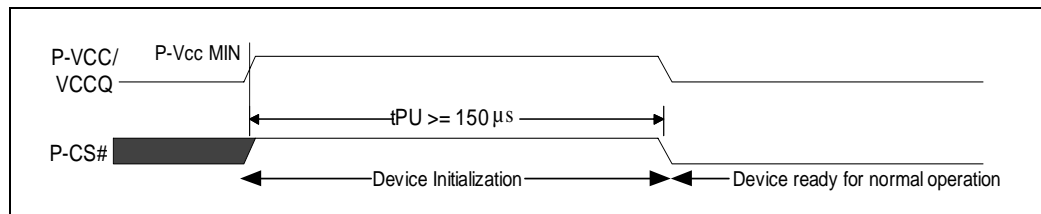
5.3.1 Flash Power and Reset Specifications

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for detailed information.

5.3.2 PSRAM Power-Up Sequence and Initialization

The power-on and initialization sequence ensures that the device is properly preconditioned to operate as expected. Like conventional DRAMs, the PSRAM must be powered up and initialized in a predefined manner. VCC and VCCQ must be applied at the same time to the specified voltage while the input signals are held in a deselected state (CS# = High).

After power on, an initial pause of 150 μs is required prior to the control register access or normal operation. Failure to follow these steps may lead to unpredictable behavior. The default operation mode after power up is the asynchronous (SRAM) mode.

Figure 10. PSRAM Timing Waveform for Power-Up Sequence

6.0 Device Electrical Specifications

The DC current and voltage characteristics referenced in this document are for individual memory die type within the SCSP device. The total current for each parameter is determined by sum of the current for each memory die type specification within the SCSP device.

> NOTICE: Individual DC Characteristics of all dies in a SCSP device must be considered accordingly, depending on the SCSP device stacked combinations and operations.

6.1 Flash DC Operating Characteristics

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for flash DC characteristics.

6.2 Synchronous PSRAM DC Operating Characteristics

Synchronous PSRAM DC operating characteristics are shown in Table 11 and Table 12.

Table 11. PSRAM DC Characteristics

Parameter	Description	Test Conditions	Density	Min	Typ	Max	Unit	Notes
V_{CC}	Supply Voltage range	—		1.7	1.8	1.95	V	
V_{CCQ}	I/O Supply Voltage range	—		1.7	1.8	1.95	V	1
V_{IH}	Input High Voltage	—		$V_{CCQ} - 0.4$	—	$V_{CCQ} + 0.2$	V	
V_{IL}	Input Low Voltage	—		-0.2	—	0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -0.2$ mA		$0.8 \times V_{CCQ}$	—	—	V	
V_{OL}	Output Low Voltage	$I_{OL} = 0.2$ mA		—	—	$0.2 \times V_{CCQ}$	V	
I_{IL}	Input Leakage Current	—		—	—	1	µA	
I_{OL}	Output Leakage Current	—		—	—	1	µA	
I_{CC1}	Async Random Read/Write @ T_{RC}Min	$V_{IN} = V_{CC}$ or V_{SS}; $I_{OUT} = 0$	32Mb	—	—	20	mA	
			64Mb	—	—	25		
I_{CC1P}	Async Page Read	$V_{IN} = V_{CC}$ or V_{SS}; $I_{OUT} = 0$	32Mb	—	—	15	mA	
			64Mb	—	—	15		
I_{CC4R}	Synchronous Burst Read (continuous)	$V_{IN} = V_{CC}$ or V_{SS}; $I_{OUT} = 0$	32Mb	—	—	25	mA	
			64Mb	—	—	35		
I_{CC4W}	Synchronous Burst Write (continuous)	$V_{IN} = V_{CC}$ or V_{SS}; $I_{OUT} = 0$	32Mb	—	—	35	mA	
			64Mb	—	—	15		
I_{CC5}	Burst Initial Access	$V_{IN} = V_{CC}$ or V_{SS}; $I_{OUT} = 0$	32Mb	—	—	35	mA	
			64Mb	—	—	15		
I_{CC2}	Standby Current (Full Array Refresh)	$V_{IN} = V_{CC}$ or V_{SS}; P-CS# = Deselected	32Mb	—	—	110	µA	
			64Mb	—	—	120		
I_{CC3}	Deep Power-Down	$V_{IN} = V_{CC}$ or V_{SS}; P-CS# = Deselected	32Mb	—	—	70	µA	
			64Mb	—	—	70		

Note: VCCQ is not allowed to be outside of P-$V_{CC} \pm 0.2$ V except during power-up situation to avoid

unnecessary current flow.

Table 12. PSRAM Partial-Array Self-Refresh (Typical) Current

Density	Active Array	Typical Standby Current (μA)			
		85 °C	70 °C	45 °C	15 °C
32-Mbit	Full	70	65	50	45
	1/2	60	55	45	40
	1/4	55	50	40	35
	1/8	50	45	40	35
	0	40	35	30	25
64-Mbit	Full	120	105	85	70
	1/2	115	TBD	TBD	70
	1/4	110	TBD	TBD	70
	1/8	105	TBD	TBD	70
	0	70	70	70	70

Note: On-chip temperature sensor is used for temperature-compensated self-refresh, therefore the standby current values at 70, 45 and 15 °C are for reference only.

6.3 Device AC Test Conditions

Figure 11. Device Transient Equivalent Testing Load Circuit
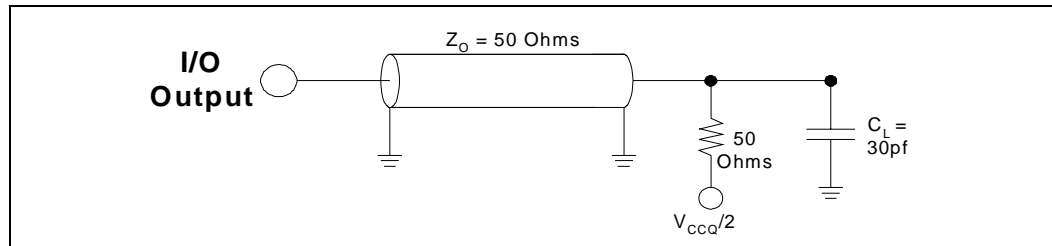
Notes:
1. Test configuration component value for worst case speed conditions.
2. C_L includes jig capacitance.

6.3.1 Flash Die Capacitance

Table 13. L18 Individual Die Capacitance

Symbol	Parameter	Min	Max	Unit	Condition
C_{IN}	Input Capacitance (Address, CLK, F-CE#, F-OE#, ADV#, WE#, F-WP#)	6	8	pF	V_{IN} = 0.0 V to 1.8 V
C_{OUT}	Output Capacitance (Data and WAIT)	8	10	pF	V_{OUT} = 0.0 V to 1.8 V

Note: Sampled, not 100% tested. T_C = 25 °C, f = 1 MHz.

6.3.2 Synchronous PSRAM Die Capacitance

Table 14. Synchronous PSRAM Individual Die Capacitance

Symbol	Parameter	Min	Max	Unit	Condition
C_{IN}	Input Capacitance (Address, CLK, P-CS#, R-OE#, ADV#, WE#, R-UB#, R-LB#)	—	6.5	pF	$V_{IN} = 0.0$ V
C_{OUT}	Output Capacitance (WAIT)	—	6.5	pF	$V_{OUT} = 0.0$ V
$C_{I/O}$	Input/Output Capacitance (DQ)	—	6.5	pF	$V_{OUT} = 0.0$ V

Note: Sampled, not 100% tested. $T_C = 25$ °C, f = 1 MHz.

7.0 Flash AC Characteristics

The following sections reference the *Intel StrataFlash® Wireless Memory (L18 SCSP)* die AC characteristics.

7.1 Flash AC Read Specifications

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for detailed information.

7.2 Flash AC Write Specifications

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for detailed information.

7.3 Flash Program and Erase Characteristics

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for detailed information.

8.0 Synchronous PSRAM AC Characteristics

The figures and tables below shows the PSRAM AC characteristics. All timing parameters are measured with the default output drive strength (half drive strength).

8.1 PSRAM Asynchronous Read

Table 15.   PSRAM AC Characteristics—Asynchronous Read

Symbol	Parameter	85 ns PSRAM		70 ns PSRAM		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	85	—	70	—	ns	1
t_{AA}	Address Access Time	—	85	—	70	ns	1
t_{AADV}	ADV# Access Time	—	85	—	70	ns	1
t_{PC}	Page Address Cycle Time	25	—	20	—	ns	1,5
t_{PAA}	Page Address Access Time	—	25	—	20	ns	1,5
t_{AVH}	Address Hold from ADV# High	—	—	5	—	ns	1,3
t_{AVS}	Address Setup to ADV# High	—	—	10	—	ns	1,3
t_{CVS}	CE# Low to ADV# High	—	—	10	—	ns	1,3
t_{OH}	Output Hold from Address Change	6	—	5	—	ns	1
t_{CO}	CE# Access Time	—	85	—	70	ns	1
t_{BA}	UB#, LB# Access Time	—	85	—	70	ns	1
t_{OE}	OE# to Valid Output Data	—	20	—	20	ns	1
t_{CSL}	CE# Pulse Width Low Time	—	10	—	4	µs	1,2
t_{LZ}	CE# Low to Output Low-Z	10	—	6	—	ns	1
t_{HZ}	CE# High to Output High-Z	0	8	0	8	ns	1
t_{BLZ}	UB#, LB# Low to Output Low-Z	10	—	6	—	ns	1
t_{BHZ}	UB#, LB# High to Output High-Z	—	8	0	8	ns	1
t_{OLZ}	OE# Low to Output Low-Z	5	—	3	—	ns	1
t_{OHZ}	OE# High to Output HIgh-Z	0	—	0	8	ns	1
t_{VP}	ADV# Pulse Width Low	—	—	10	—	ns	1,3
t_{VPH}	ADV# Pulse Width High	10	—	10	—	ns	1,3
t_{CPH}	UB#, LB# and CE# Pulse Width High	15	—	10	—	ns	1
t_{CRES}	CRE Setup to CE# Low	—	—	0	—	ns	1
t_{ASKEW}	Address Skew (Non-Page Access)	—	—	—	10	ns	1,4
t_{ASKEWP}	Page Mode Access Address Skew [A3:A0]	—	—	—	2	ns	1,5

Notes:
1. Timing parameters are at the default output drive strength (half drive strength).
2. t_{CSL} max limit applies during asynchronous reads when page mode is enabled.
3. Applies to ADV# controlled Asynchronous Read operations.
4. Applies when control signals (ADV#, CS#, UB#/LB#) are active.
5. When operating the PSRAM as an ADMux I/O interface, Page-Mode operation is not available.

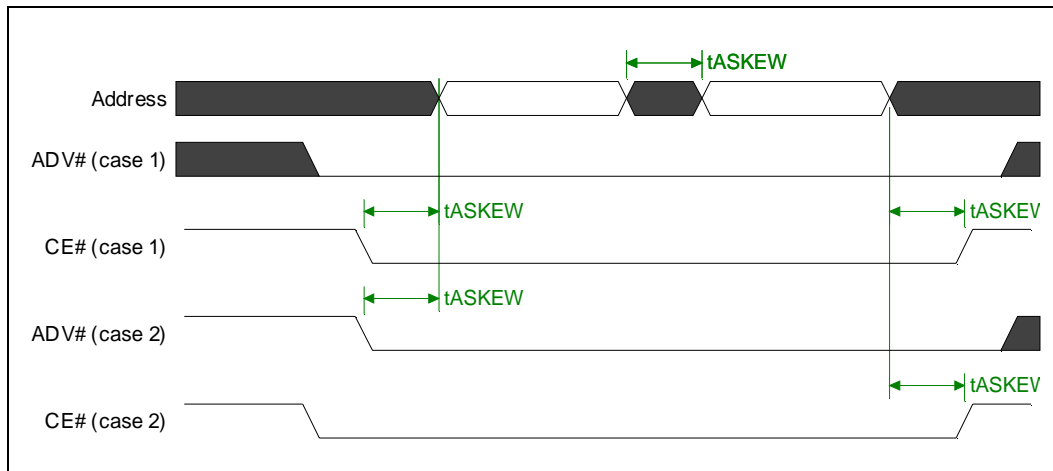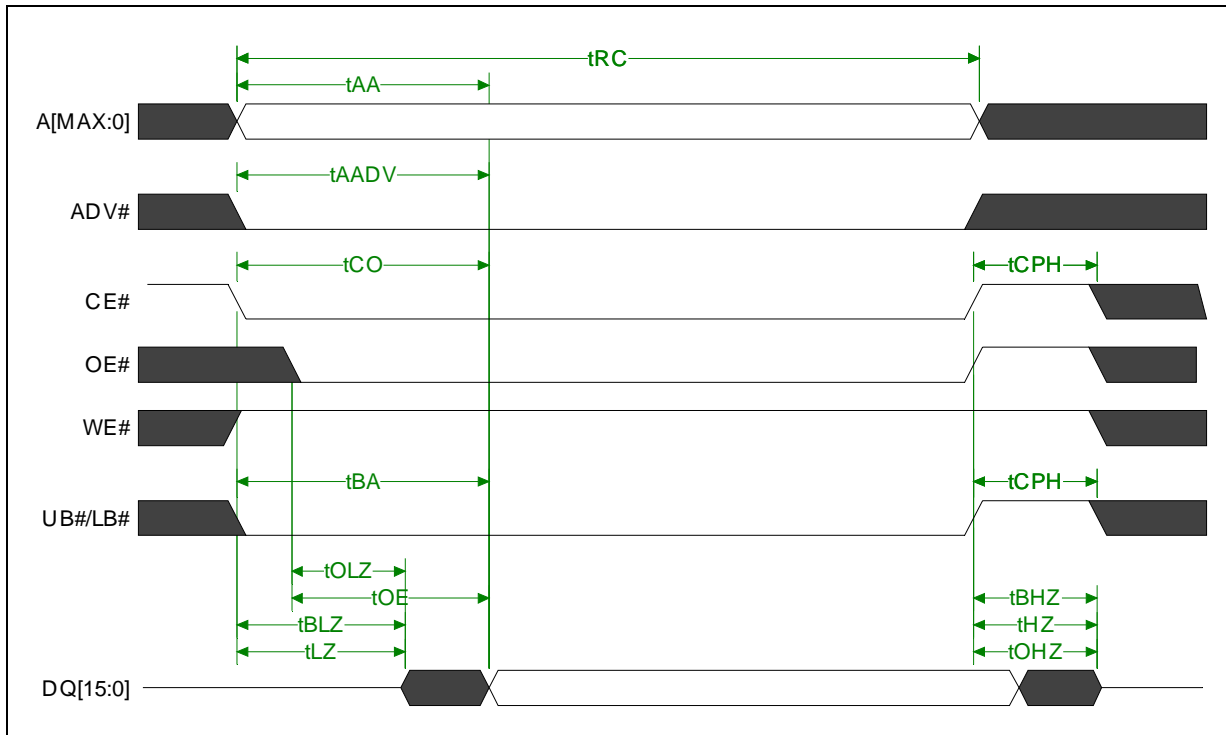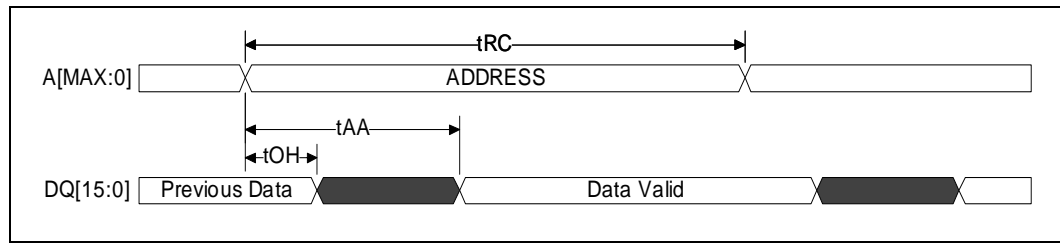**Figure 12. Address Skew for Asynchronous Operations**

Figure 13. PSRAM Asynchronous Single-Word Read

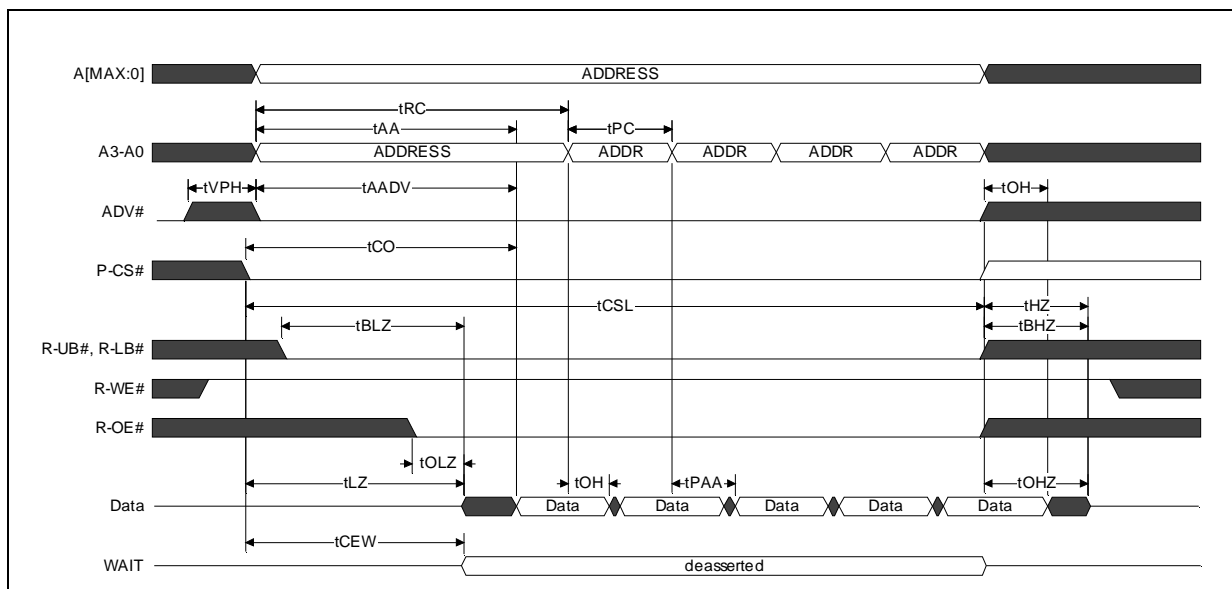*Note:* WAIT is configured for active-low polarity.

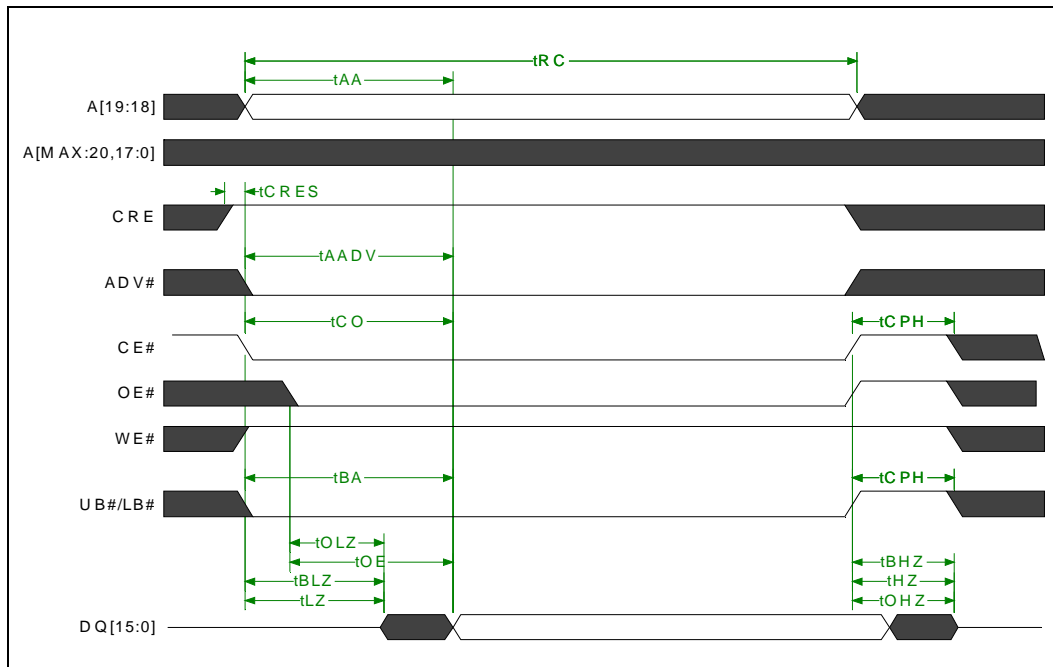**Figure 14.   Asynchronous Address-controlled Read**

Note: CE# = OE# = UB# =LB# = CRE = Low; WE# = High

Figure 15.   PSRAM Asynchronous Page-Mode Read

Note: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, Page-Mode operation cannot be used.

Figure 16. PSRAM Asynchronous Control Register Read

8.2   PSRAM Asynchronous Write

The figures and tables below shows the PSRAM AC characteristics. All timing parameters are measured with the default output drive strength (half drive strength).

Table 16.   PSRAM AC Characteristics—Asynchronous Write (Sheet 1 of 2)

Symbol	Parameter	85 ns PSRAM		70 ns PSRAM		Units	Notes
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	85	—	70	—	ns	
t_{AS}	Address Setup Time	0	—	0	—	ns	
t_{AW}	Address Valid to End of Write	85	—	70	—	ns	
t_{WR}	Write Recovery	0	—	0	—	ns	
t_{CSL}	CE# Pulse Width Low Time	—	10	—	4	µs	
t_{CW}	CE# to End of Write	85	—	70	—	ns	
t_{VPH}	ADV# Pulse Width High	7	—	10	—	ns	2
t_{VP}	ADV# Pulse Width Low	6	—	10	—	ns	2
t_{AVH}	Address Hold from ADV# High	5	—	5	—	ns	2
t_{AVS}	Address Setup to ADV# High	10	—	10	—	ns	2
t_{CVS}	CE# Low to ADV# High	—	—	10	—	ns	2
t_{VS}	ADV# Setup to End of Write	85	—	70	—	ns	
t_{BW}	UB#, LB# Setup to End of Write	85	—	70	—	ns	
t_{WP}	WE# Pulse Width Low	45	—	46	—	ns	1

Table 16.   PSRAM AC Characteristics—Asynchronous Write (Sheet 2 of 2)

Symbol	Parameter	85 ns PSRAM		70 ns PSRAM		Units	Notes
		Min	Max	Min	Max		
t_{WPH}	WE# Pulse Width High	15	—	10	—	ns	
t_{CPH}	UB#, LB# and CE# Pulse Width High	15	—	10	—	ns	
t_{WHZ}	Write Enable Low to Output High-Z	0	10	—	8	ns	
t_{OW}	End of Write to Output Low-Z	5	—	5	—	ns	
t_{DW}	Write Data Setup Time	20	—	23	—	ns	
t_{DH}	Write Data Hold Time	0	—	0	—	ns	
t_{CRES}	CRE SetupTime to CE# and WE# Low	5	—	0	—	ns	4
t_{CREH}	CRE Hold Time From WE# High	0	—	0	—	ns	4
t_{ASKEW}	Address Skew (Non-Page Access)	—	—	—	10	ns	3

Notes:
1.   WE# Low time must be limited to t_{CSL} Max.
2.   For ADV# controlled Async Write operation.
3.   Applies when control signals (ADV#, CE#, UB#, LB#) are Active.
4.   For ADV# controlled write t_{AVS} and t_{AVH} apply to CRE signal instead of t_{CRES} and t_{CREH}.

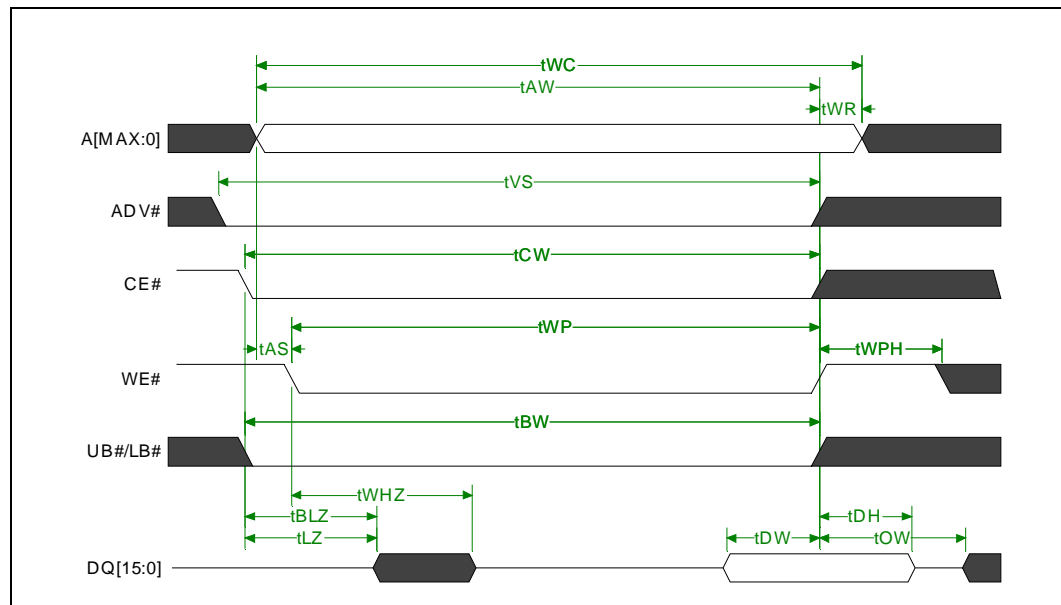**Figure 17.   PSRAM Asynchronous WE# controlled Write**

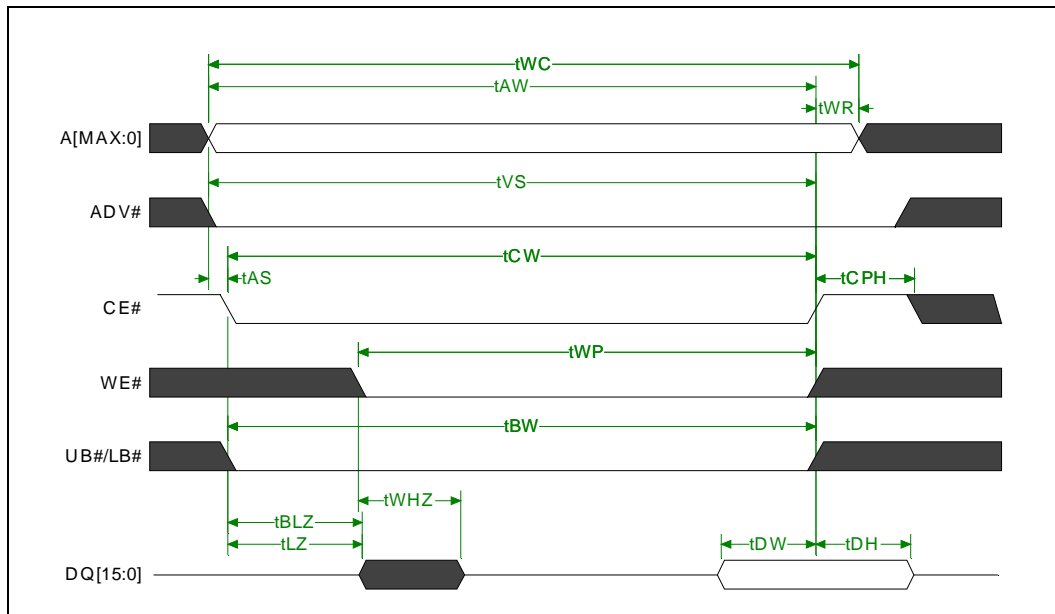**Figure 18.** **PSRAM Asynchronous CE# controlled Write**

Figure 19. **PSRAM Asynchronous UB#/LB# controlled Write**
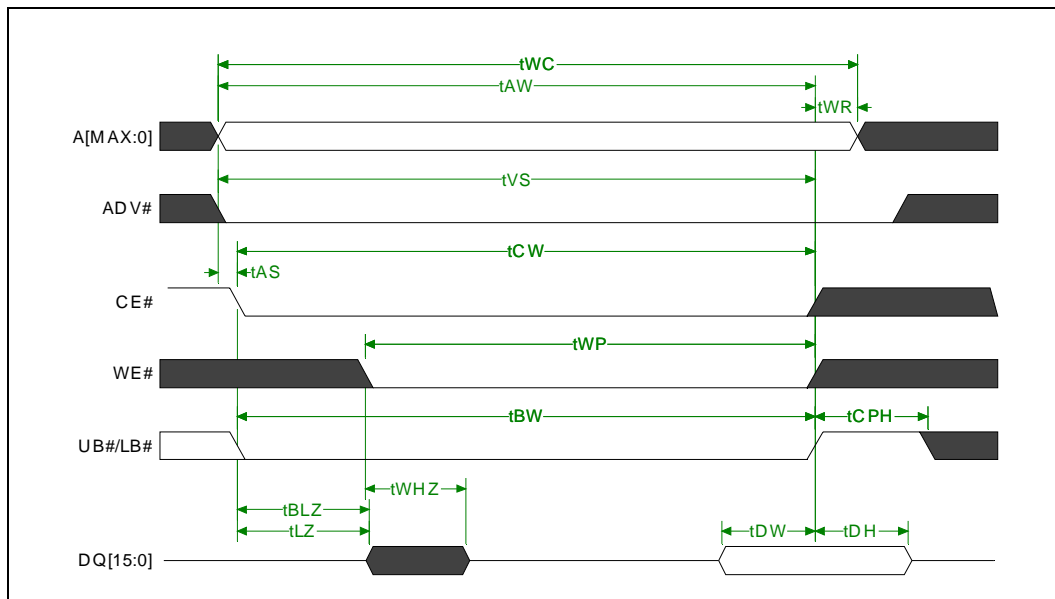
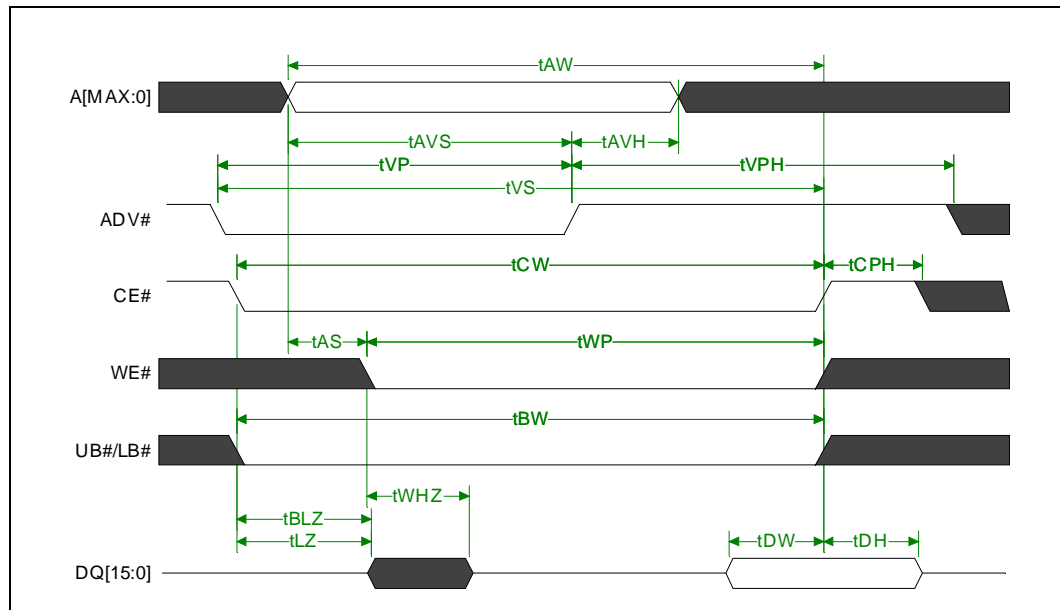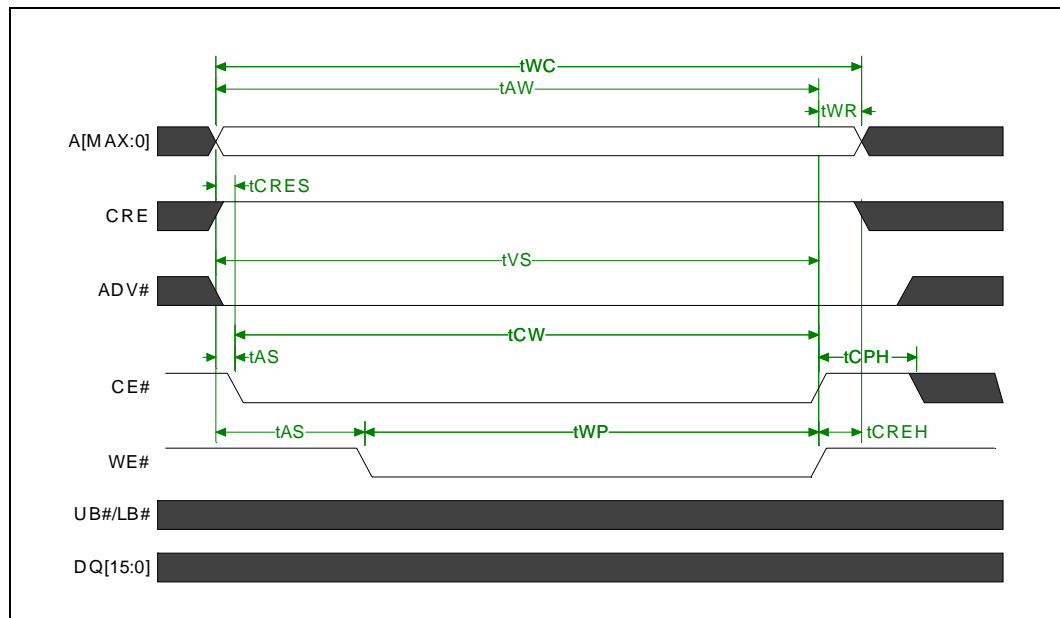**Figure 20.   PSRAM Asynchronous ADV# controlled Write**

Figure 21.   PSRAM Asynchronous Control Register Write

8.3   PSRAM Synchronous Read and Write

The figures and tables below shows the PSRAM AC characteristics. All timing parameters are measured with the default output drive strength (half drive strength).

Table 17.   PSRAM AC Characteristics—Synchronous Read and Write

Symbol	Parameter	Min	Max	Units	Notes
f_{CLK2}	CLK Frequency (Variable Latency = 2)	—	54	MHz	
f_{CLK6}	CLK Frequency (Fixed Latency = 6)	—	54	MHz	
t_{CLK2}	CLK Period (Variable Latency = 2)	18.5	—	ns	
t_{CLK6}	CLK Period (Fixed Latency = 6)	18.5	—	ns	
t_{CKH}	CLK High Time	4	—	ns	
t_{CKL}	CLK Low Time	4	—	ns	
t_T	CLK Rise/Fall Time	—	1.8	ns	
t_{ABA}	Burst Read First Access Delay (Variable Latency = 2)	—	47.5	ns	1
t_{AA}	Address Access Time (Fixed Latency)	—	70	ns	
t_{AADV}	ADV# Access Time (Fixed Latency)	—	70	ns	
t_{CO}	CE# Access Time (Fixed Latency)	—	70	ns	
t_{AVH}	Address Hold from ADV# High (Fixed Latency)	5	—	ns	
t_{SP}	Input Setup to CLK High (except CE#)	3	20	ns	2
t_{HD}	Input Hold from CLK High	2	—	ns	
t_{CSS}	CE# Low Setup to CLK High	4.5	20	ns	3
t_{CSL}	CE# Pulse Width Low Time	—	4	µs	4
t_{CBPH}	CE# Pulse Width High Time Between Operations	6	—	ns	5
t_{OL}	OE# or UB#/LB# Low to Output Low-Z	3	—	ns	
t_{OD}	CE#, OE#, or UB#/LB# High to Output in High-Z	0	8	ns	
t_{AOE}	OE# Low to Output Delay	—	20	ns	
t_{CWT}	CE# Low to WAIT Valid	1	7.5	ns	
t_{WZ}	CE# High to WAIT High-Z	—	8	ns	
t_{WK}	CLK to WAIT Valid	—	9	ns	
t_{ACLK}	CLK to Output Delay	—	9	ns	
t_{KOH}	Output Hold from CLK	2	—	ns	
t_{ASKEW}	Address Skew	—	10	—	5

Notes:
1. In case of refresh collisions with the first access, more WAIT cycles will be added.
2. t_{SP} Max values only applies to ADV#.
3. The purpose of the Max limit is to prevent the PSRAM from starting Async access cycle.
4. To allow for proper refresh operation, the CE# must be high during a clock low to high transition or keep CE# high for min 15 ns.
5. Address Skew maximum must not be exceeded during synchronous operations to avoid inadvertent asynchronous operation
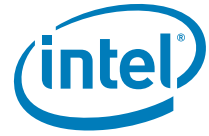
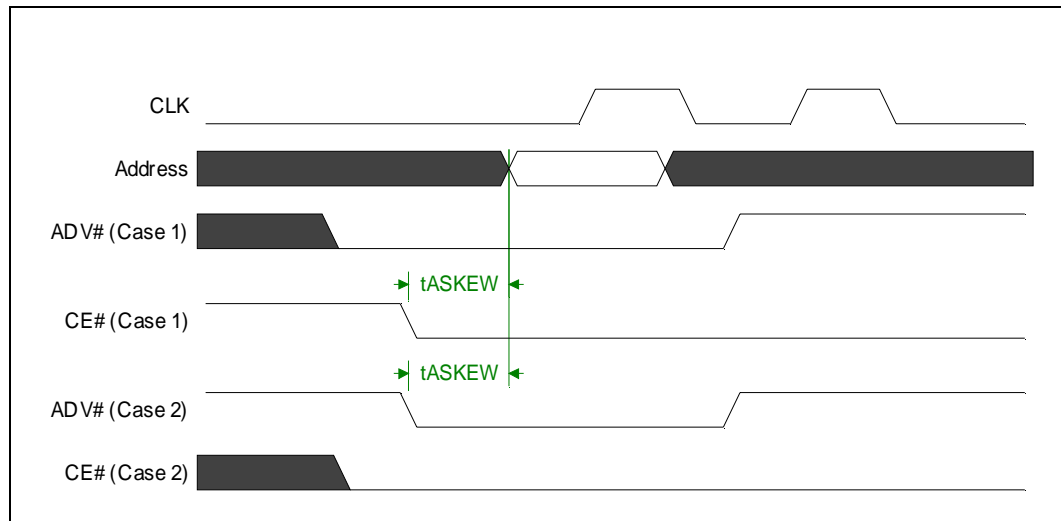**Figure 22.   Address Skew for Synchronous Operations**

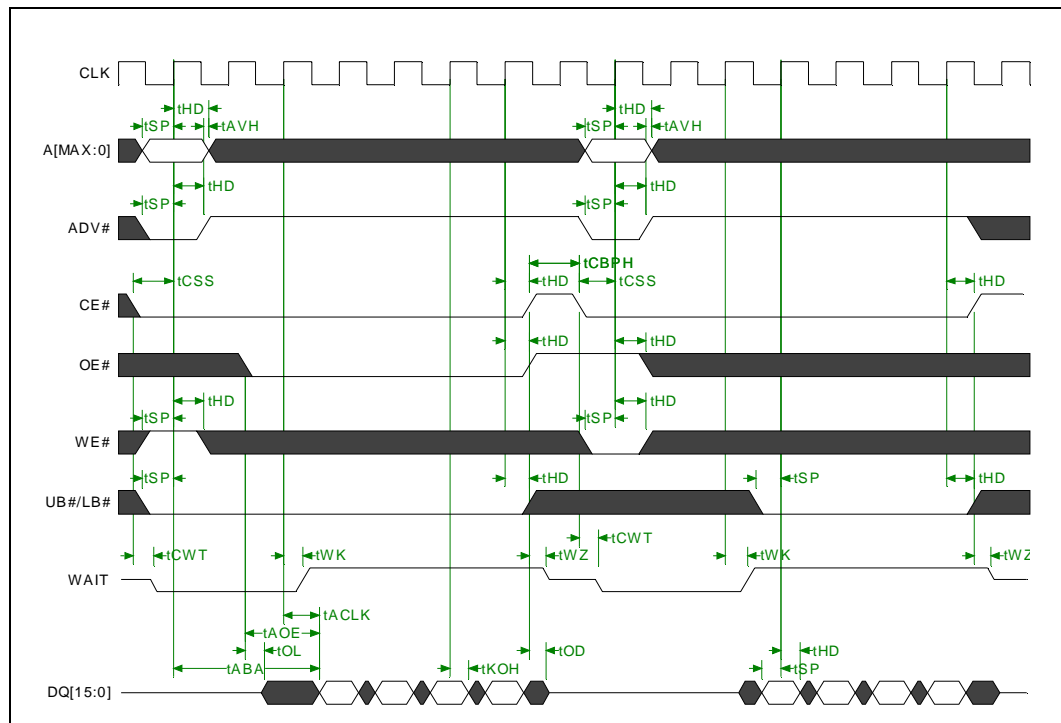**Figure 23.   PSRAM Synchronous Read followed by Synchronous Write**

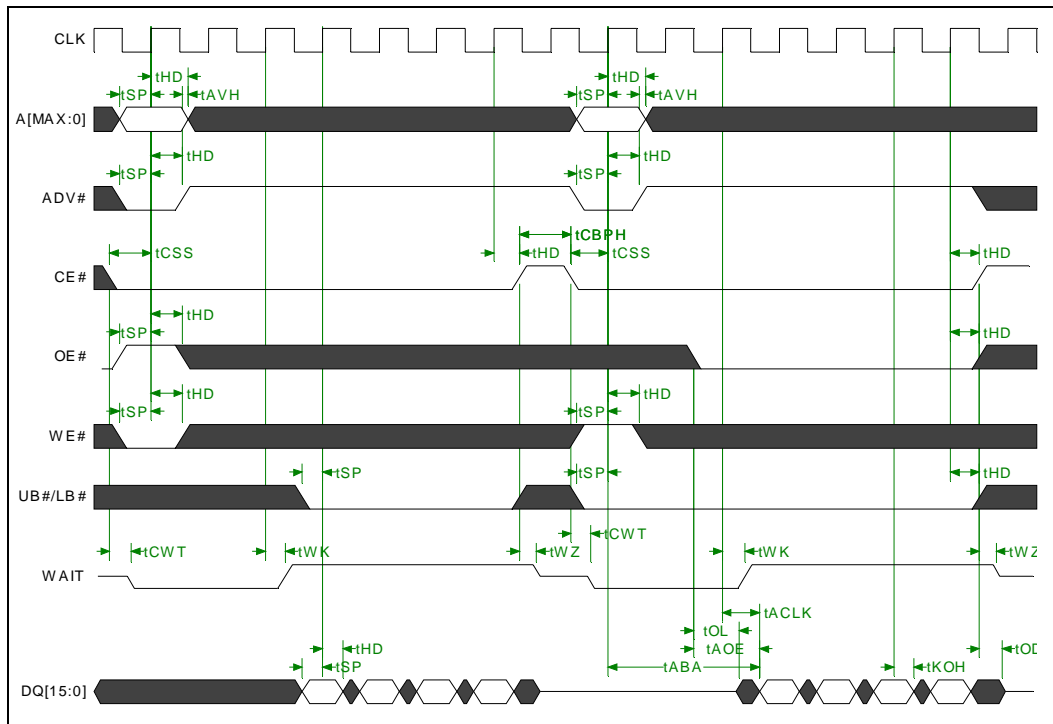**Figure 24.   PSRAM Synchronous Write followed by Synchronous Read**

Figure 25.   PSRAM Synchronous Read followed by Asynchronous Write
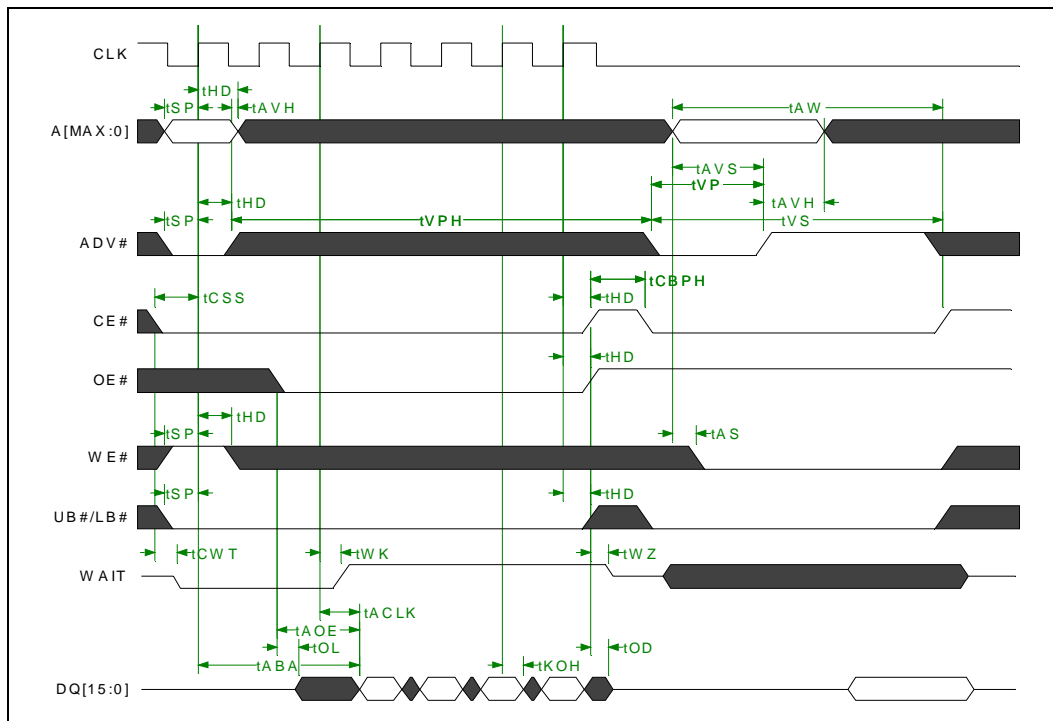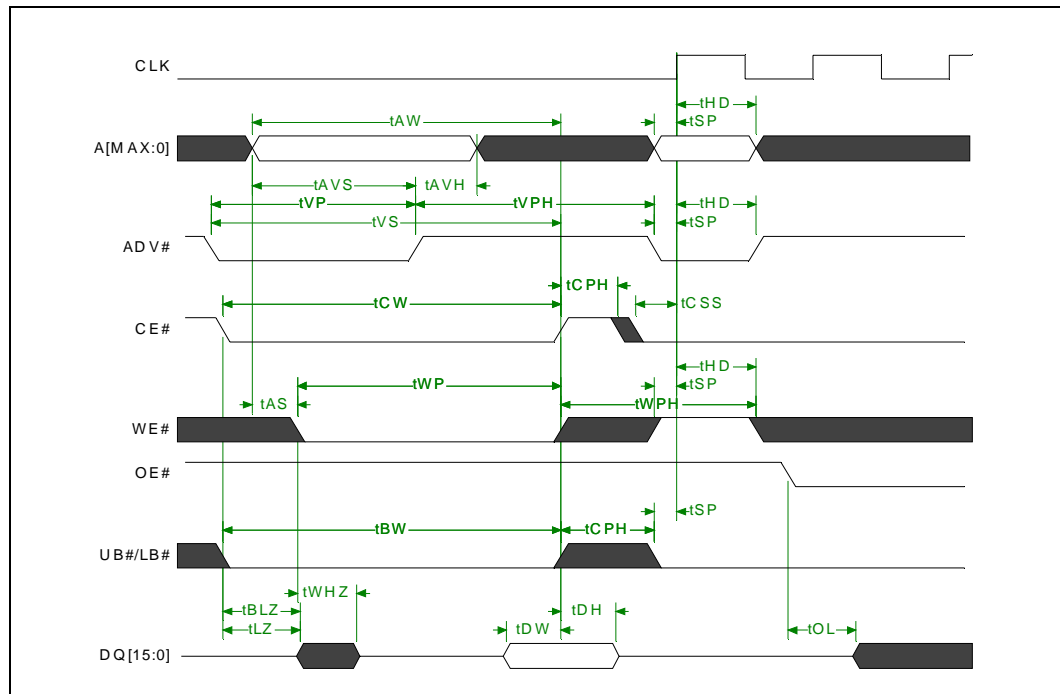
Figure 26. PSRAM Asynchronous Write followed by Synchronous Read

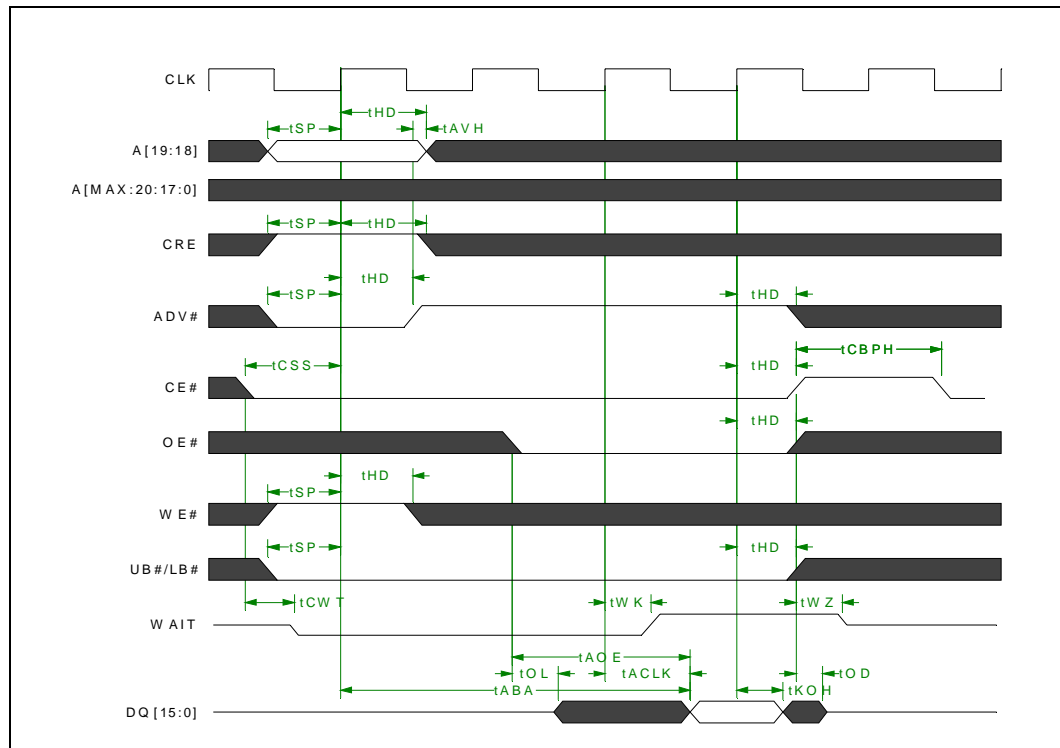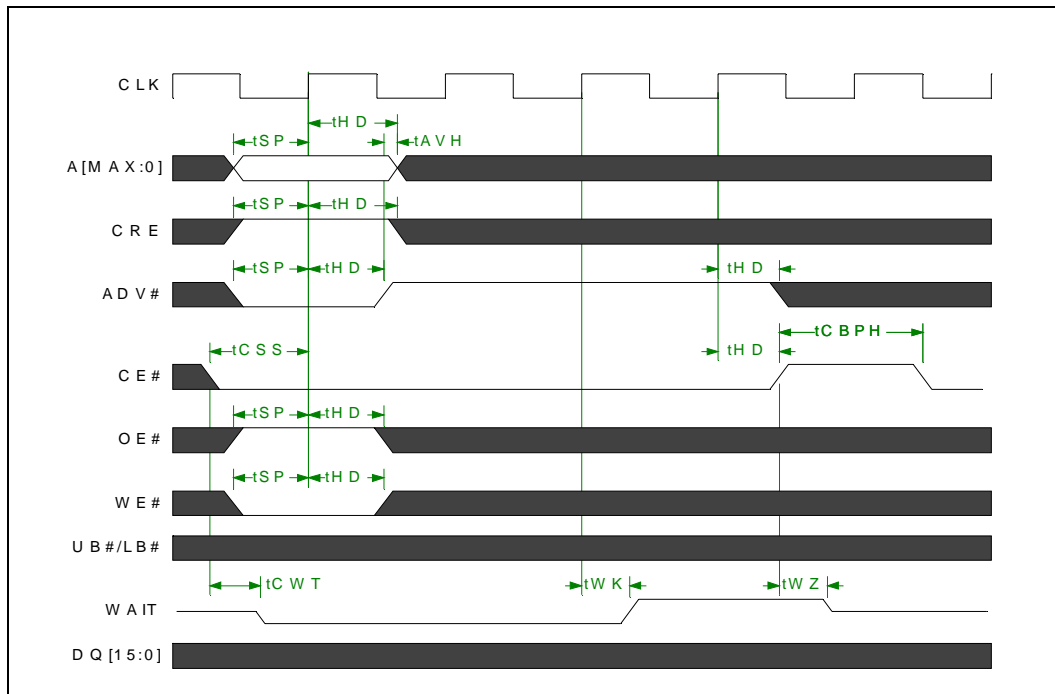**Figure 27. PSRAM Synchronous Control Register Read**

Figure 28.   PSRAM Synchronous Control Register Write

9.0 Flash Bus Interface

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for detailed information regarding the Flash Bus Interface as referenced by the sections below.

9.1 Flash Configuration Register

9.2 Flash Enhanced Configuration Register

9.3 Flash Asynchronous Page-Mode Read

9.4 Flash Synchronous Burst-Mode Read

9.5 Flash Status Register

9.6 Flash Device Identifier

9.7 Common Flash Interface

9.8 Extended Flash Array

10.0 Flash Operations

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for detailed information regarding the Flash Operations as referenced by the sections below.

10.1 Flash Read Operation

10.2 Flash Program Operation

10.3 Flash Erase Operation

10.4 Flash Suspend and Resume Operations

10.5 Flash Block Locking and Unlocking Operations

10.6 Flash Protection Register Operation

10.7 Flash Configuration Operation

11.0 PSRAM Bus Interface

The PSRAM bus interface supports asynchronous and synchronous read and write transfers. By default the PSRAM device is reset to the asynchronous SRAM-type mode after power-up. To put the device in a different operation mode the Bus Configuration Register must be programmed first accordingly.

11.1 PSRAM Reads

The PSRAM bus interface supports asynchronous single-word, asynchronous page-mode, and synchronous burst-mode reads. PSRAM Refresh Control Register bit 7 (RCR7) defines whether page-mode reads are enabled. Page-mode reads are enabled when RCR7 is set to a one, and disabled when RCR7 is set to zero.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, Page-Mode operation cannot be used. RCR7 must be set to Zero.

11.1.1 PSRAM Asynchronous Read

To initiate an asynchronous read operation:

- CE#, OE#, and UB#/LB# must be asserted.
- WE# and CRE must be deasserted.
- ADV# can be toggled to latch the address or held low for the entire read operation.
- CLK must be held in a static state.

Valid data is available on the data bus after the specified access time has elapsed. WAIT output is driven, but should be ignored for asynchronous-mode read operations.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.1.2 PSRAM Asynchronous Page-Mode Read

Page mode allows toggling of the four lower address bits (A3 to A0) to perform subsequent random read accesses (max. 16-words by A3-A0) at much faster speed than the 1st read access. Only page mode Read operations are supported by the PSRAM. Once page mode is enabled by appropriately setting the BCR, tCSL restrictions will apply to asynchronous Read accesses. Therefore CE# will have to be pulled high at least every tCSL period during asynchronous Read operations. ADV# has to be held low for the entire page operation.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, Page-Mode operation cannot be used. RCR7 must be set to Zero.

11.1.3 PSRAM Synchronous Burst-Mode Reads

In the Full Synchronous mode and NOR-Flash mode, PSRAM read operations are synchronous. A *BURST INIT READ* command is used to initiate a synchronous read operation and latch the burst start address. To initiate a synchronous read operation:

- CE#, ADV#, and both UB# and LB# must be asserted;
- WE# and CRE must be deasserted; and

- Burst start address is latched on the rising edge of the clock;

To continue the synchronous read operation:

- CE#, OE#, and both UB# and LB# must be asserted; and
- ADV# must be deasserted;

The first data word is output after the number of clock cycles defined by the programmed latency mode and latency count in the BCR. Subsequent data words are output at successive clock cycles after the first data word.

- WAIT output will be driven and should be monitored in Variable Latency mode.
- WAIT may be ignored in fixed latency mode.
- Both UB# and LB# must be held static low for the entire read access. The size of the burst is also specified in the BCR.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.1.4   PSRAM Asynchronous Fetch Control Register Read

In the Asynchronous (SRAM-type) mode the contents of the BCR and RCR can be read asynchronously. To initiate an asynchronous Fetch Control Register (FCR):

- CE#, OE#, CRE, and both UB# and LB# must be asserted;
- WE# must be deasserted;
- ADV# can be toggled to latch the address or held low for the entire read operation;
- CLK must be held in a static low state.

Except for A19 and A18, all other address and data bits are don't care. A19 and A18 specify the target register (RCR = 00b, BCR = 10b) The contents of the selected register are available on the data bus after the specified access time has elapsed. WAIT output will be driven but should be ignored for asynchronous operations.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.2   PSRAM Writes

The PSRAM bus interface supports asynchronous single-word and synchronous burst-mode writes. BCR15 defines whether asynchronous or synchronous mode is enabled.

11.2.1   PSRAM Asynchronous Write

In the Asynchronous (SRAM-type) mode and NOR-Flash mode, PSRAM write commands are asynchronous. To initiate an asynchronous write operation:

- CE# and WE# must be asserted;
- UB# and LB# must be asserted appropriately depending on the data byte(s) that are being written. UB# enables DQ[15:8] and LB# enables DQ[7:0].
- CRE must be deasserted;
- ADV# can be toggled to latch the address or held low for the entire read operation;
- CLK must be held in a static state.

The data to be written will be latched on the rising edge of CE#, WE# or UB#/LB# whichever occurs first. WAIT output will be driven but should be ignored for asynchronous-mode operations.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.2.2   PSRAM Synchronous Write

In the Full Synchronous mode, PSRAM write operations are synchronous. A BURST INIT WRITE command is used to initiate a synchronous write operation and latch the burst start address. To initiate a synchronous write operation:

- CE#, ADV#, and WE# must be asserted;
- OE# and CRE must be deasserted; and
- Burst start address is latched on the rising edge of the clock;

To continue the synchronous write operation:

- CE#, and UB#/LB# must be asserted; and
- ADV# must be deasserted;

The first data word is input after the number of clock cycles defined by the programmed latency mode and latency count in the BCR. Subsequent data words are input at successive clock cycles after the first data word. The size of the burst is also specified in the BCR. WAIT output will be driven and may be monitored. But since synchronous write is always at fixed latency regardless of the Latency Mode setting, WAIT may be ignored. UB# or LB# may be deasserted to mask the associated data byte.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.2.3   PSRAM Asynchronous Set Control Register Write

In the Asynchronous (SRAM-type) mode and NOR-Flash mode the contents of the BCR and RCR can be set asynchronously. To initiate an asynchronous Set Control Register:

- CE#, WE#, and CRE must be asserted;
- OE# must be deasserted;
- ADV# can be toggled to latch the address or held low for the entire read operation;
- CLK must be held in a static low state.

The DQ signals are ignored by the PSRAM. Address bits A19 and A18 specify the target register (RCR = 00b, BCR = 10b.) The values of the remaining address bits are loaded into the selected register. The Set Control Register command should only be issued when the PSRAM is in the idle state (deselected).

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.2.4 PSRAM Synchronous Set Control Register Write

In the full Synchronous mode the contents of the BCR and RCR can be set synchronously. To initiate a synchronous Set Control Register:

- CE#, WE#, ADV#, and CRE must be asserted; and
- OE# must be deasserted;
- Address is latched on the rising edge of the clock

The DQ signals are ignored by the PSRAM and therefore the WAIT signal should be ignored. Address bits A19 and A18 specify the target register (RCR = 00b, BCR = 10b.) The values of the remaining address bits are loaded into the selected register. The Set Control Register command should only be issued when the PSRAM is in the idle state (deselected).

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.3 PSRAM No Operation Command

The No Operation (NOP) command is used to perform a no operation to a selected PSRAM (CE# = Low) Operations in progress are not affected. A NOP may be issued in Asynchronous, Synchronous, or NOR-Flash mode. To initiate a NOP:

- CE#, must be asserted;
- WE#, ADV#, OE#, and CRE must be deasserted; and
- CLK must be held in a static low state while in Asynchronous mode. CLK may toggle during a NOP in Synchronous mode.
- In Synchronous mode, ADV# deasserted hold time (tHD) must be observed.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

11.4 PSRAM Deselect

The Deselect function prevents new commands from being executed by the PSRAM. A deselected PSRAM places its I/O signals in a high impedance state. To place the device in a deselected state:

- CE# must be deasserted.
- CLK must be held in a static low state while in Asynchronous mode. CLK may toggle during a NOP in Synchronous mode.

11.5 PSRAM Deep Power Down

Deep Power Down (DPD) stops all refresh-related activities and the current consumption of the device drops to a very low level. The contents of the Memory are not preserved. After setting RCR4 = 1b, to place the device in the DPD state

- CE# must be deasserted.
- CLK must be held in a static low state to achieve minimum current consumption levels.

11.6 PSRAM WAIT Signal

The WAIT signal is used in synchronous mode to indicate to the host system periods of invalid data. Periods of invalid data are caused by:

1. First access delays, or

2. End of Row condition for continuous or wrap-off burst settings.

For fixed length bursts with wrap on, WAIT remains deasserted when the End of Row is reached and the burst will wrap around and continue without any delay. Therefore for fixed length bursts with wrap on, WAIT is only asserted during First access delays.

For continuous or wrap-off burst length configuration, End of Row condition, WAIT will transition from being de-asserted to being asserted within the time window defined by tKOH and tWK. Depending on the implementation for a burst write, WAIT may be asserted at the same time as the delay (condition A of Figure 29) or one clock cycle later (condition B of Figure 29.) This inconsistency does not occur during burst read.

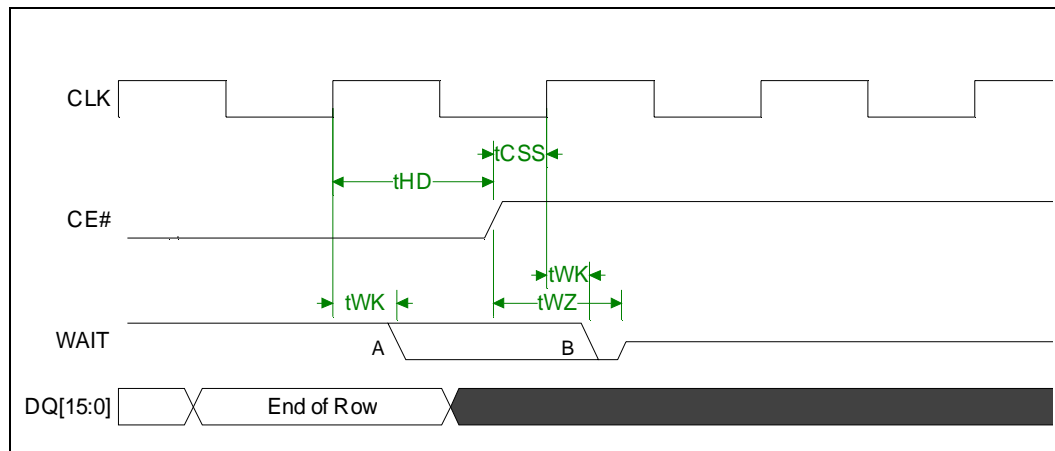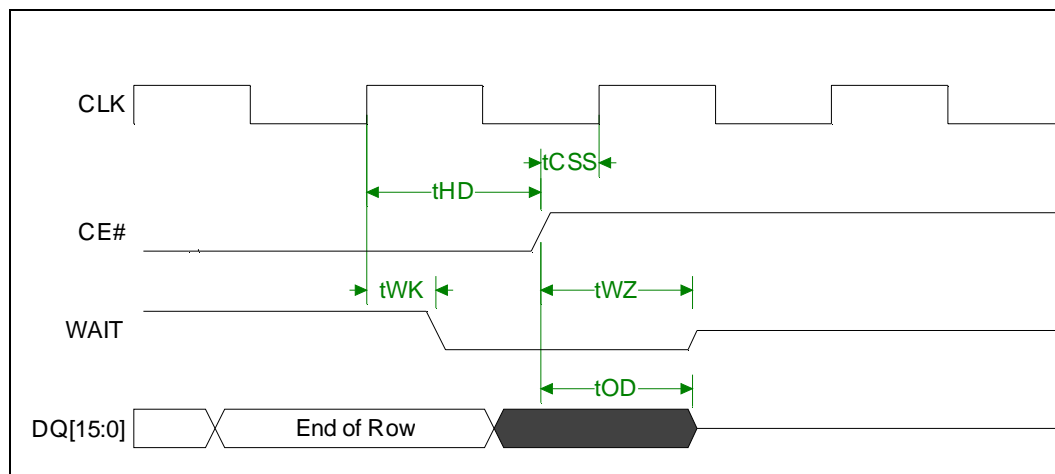**Figure 29. PSRAM WAIT Behavior during Burst Write End-of-Row with Wrap Off**

Figure 30. PSRAM WAIT Behavior during Burst Read End-of-Row with Wrap Off

During variable latency burst write operations and fixed latency burst write and read operations the initial latency is fixed so the system is not required to monitor the WAIT signal although the WAIT signal is fully functional and may be monitored by the system. The system should terminate or interrupt the burst access to avoid row boundary crossings in both fixed and variable latency mode.

To match with the Flash interfaces of different microprocessor types the polarity and the timing of the WAIT signal can be configured. The polarity can be programmed to be either active low or active high. The timing of the WAIT signal can be adjusted as well. Depending on the BCR setting the WAIT signal will be either asserted at the same time the data becomes invalid or it will be set active one clock period in advance.

In asynchronous mode including page mode, the WAIT signal is not used but stays asserted as BCR10 is specified. In this case, the system should ignore the WAIT signal. When the PSRAM is deselected or in deep power down, the WAIT output will be in a high impedance state.
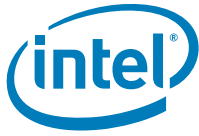
12.0 PSRAM Device Operation

12.1 PSRAM Operating Modes

The PSRAM can be used in three different modes:

- SRAM (full asynchronous) mode: In this mode the PSRAM applies the standard asynchronous SRAM protocol to perform read and write accesses. In additions, reads may be performed in page mode if the page mode is properly enabled by programming the RCR. In this mode the clock must always remain static low.
- Fully Synchronous mode: In this mode, both read and write accesses are performed synchronously with respect to the clock. Synchronous operations are defined by the states of the control signals CE#, ADV#, OE#, WE# and UB#, LB# at the positive (default) edge of the clock.
- NOR-Flash mode: In this mode, reads are performed synchronously with respect to the clock and writes are performed asynchronously. The asynchronous write operation requires that the clock remain static low during the entire write. Synchronous read operations are defined by the states of the control signals CE#, ADV#, OE#, WE# and UB#, LB# at the positive (default) edge of the clock.

12.2 PSRAM Control Registers

The two control registers define the PSRAM device operation. The Bus Control Register (BCR) defines how the PSRAM interacts with the system memory busy, and the Refresh Control Register (RCR) defines low-power refresh modes. Both these registers are loaded with default values on power-up and can be updated at any time using hardware or software access method.

12.2.1 PSRAM Bus Control Register

The Bus Control Register (BCR) specifies the interface configurations. The Bus Control Register is programmed via the Set Control Register command (with CRE = 1 and A[19:18] = 10b) and retains the stored information until it is reprogrammed or the device loses power.

Reserved bit fields of the BCR should be ignored during a Fetch Control Register command as they may have undefined values even when set to 0b with a Set Control Register command. The BCR contents can only be set or changed when the PSRAM is in idle state.

Table 18. PSRAM Bus Control Register Map

	Reserved	Register Select	Reserved	Operating Mode	Initial Latency	Latency Counter			WAIT Polarity	Reserved	WAIT Configuration	Reserved		Drive Strength		Burst Wrap	Burst Length		
DQ [15:0]				DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
A [MAX:0]	A22-A20	A19	A18	A17-A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
BCR Bit	22-20	19	18	17-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 19.   Bus Control Register Description

BCR Bit	NAME	Description
22:20	Reserved	Reserved bits should be set to '0' during set control register commands
19:18	Register Select	10 = Select BCR
17:16	Reserved	Reserved bits should be set to '0' during set control register commands
15	Operating Mode	0 = Synchronous Burst Mode 1 = Asynchronous Mode (Default)
14	Initial Latency	0 = Variable (Default) 1 = Fixed
13:11	Latency Counter	000 = Code 0 - Reserved 001 = Code 1 - Reserved 010 = Code 2 011 = Code 3 (Default) 100 = Code 4 101 = Code 5 110 = Code 6 111 = Code 7 - Reserved
10	WAIT Polarity	0 = Active Low 1 = Active High (Default)
9	Reserved	Reserved bits should be set to '0' during set control register commands
8	WAIT Configuration	0 = WAIT asserted during delay 1 = WAIT asserted one data cycle before delay (Default)
7:6	Reserved	Reserved bits should be set to '0' during set control register commands
5:4	Drive Strength	00 = Full 01 = 1/2 (Default) 10 = 1/4 11 = Reserved
3	Burst Wrap	0 = Burst wraps within the burst length 1 = Burst does not wrap (Default)
2:0	Burst Length	000 = Reserved 001 = 4 words 010 = 8 words 011 = 16 words 100 = 32 words 101 = Reserved 110 = Reserved 111 = Continuous Burst (Default)
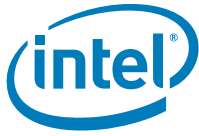
12.2.1.1 PSRAM BCR Operating Mode

The PSRAM supports three different interface access protocols:

- SRAM-type protocol with asynchronous read and write accesses
- NOR-Flash-type protocol with synchronous read and asynchronous write accesses
- FULL SYNCHRONOUS mode with synchronous read and synchronous write accesses

Operating the PSRAM in synchronous mode maximizes bandwidth. The NOR-Flash type mode is the recommended mode for legacy systems which are not able to run the synchronous write protocol. The Operating Mode bit BCR15 defines whether the device is operating in synchronous (fully or partially) mode or asynchronous mode.

When BCR15 is set low, the mode of write operation, NOR-flash or Full synchronous, is adaptively detected by detecting a rising clock edge during ADV# valid. If a rising clock edge occurs within ADV# valid, Full synchronous write is detected. If there is no rising clock edge then NOR-Flash write is detected and CE# must go high when transitioning from asynchronous to synchronous operation or when transitioning from synchronous to asynchronous operation..

When BCR15 is set high, the SRAM-type mode of operation is selected.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, ADV# must be de-asserted during any data phase cycle.

12.2.1.2 PSRAM Initial Latency BCR Bit

The PSRAM latency is related to the number of clock cycles from the burst-init command to be either 1st valid data output (read burst) or 1st valid data input (burst write.) In Fixed Latency mode, the number of clock cycles from bust-init command to valid data is always fixed as defined by the Latency Counter setting in the BCR. In Variable Latency mode, the number of clock cycles from bust-init command to valid data output (read burst) is variable depending on internal device operation. The minimum latency in Variable Latency mode is defined by the Latency Counter setting in the BCR. Additional WAIT cycles may be added in Variable Latency mode if the burst-init Read command collides with an on-going internal refresh. Additional WAIT cycles are not added for burst-init Write commands in Variable Latency mode.

12.2.1.3 PSRAM Latency Counter BCR Bit

The latency counter defines the number of clock cycles that pass before the first output data is valid (read burst) or before the first input data is valid (read burst.) Each Latency Code setting has an associate maximum PSRAM clock frequency. In the case of Variable Latency the first access delay might be extended by additional wait cycles in case the burst read access collides with an ongoing self-refresh operation. The allowed values of the Latency Counter also depend on the Initial Latency setting in BCR.

Table 20. Optional PSRAM BCR Latency Counter Settings in Variable Latency

Latency Counter	PSRAM
010	Code 2; Max 54 MHz
011	Code 3; Max 80 MHz
Others	Reserved

Table 21.   Optional PSRAM BCR Latency Counter Settings in Fixed Latency

Latency Counter	PSRAM
010	Code 2; Max 33 MHz
011	Code 3; Max 52 MHz
100	Code 4; Max 66 MHz
101	Code 5; Max 75 Mhz
110	Code 6; Max 104 MHz
Others	Reserved

Figure 31.   Example of the Latency of First Valid Data in Synchronous Mode
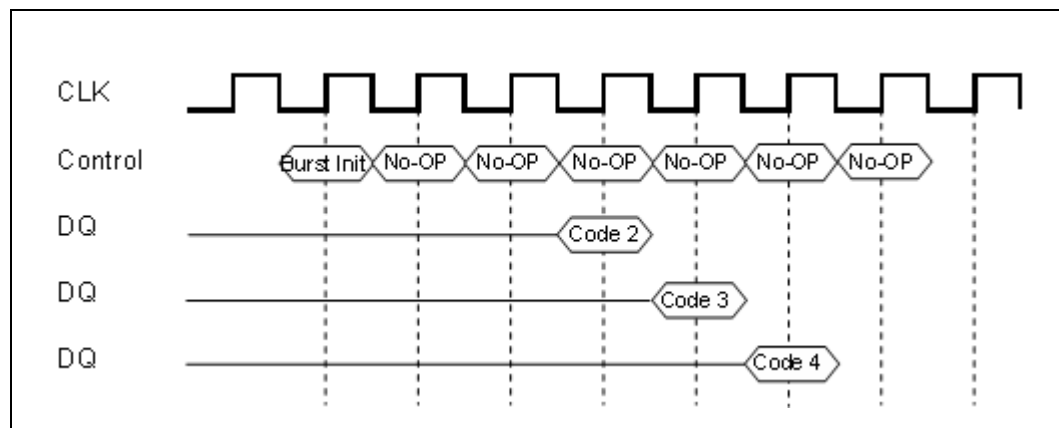
12.2.1.4   PSRAM WAIT Polarity BCR Bit

The WAIT polarity control bit allows the user to define the polarity of the WAIT output signal. The WAIT output line is used during a variable latency synchronous read burst to signal when the output data is invalid. Active low WAIT polarity means that when WAIT is asserted low, output data is invalid. Similarly active high WAIT polarity means that when WAIT is asserted high, output data is invalid.

12.2.1.5   PSRAM WAIT Configuration BCR Bit

The WAIT signal configuration control bit specifies whether the WAIT signal is asserted at the time of the delay or whether it is asserted one clock cycle in advance of the delay.

12.2.1.6   PSRAM Drive Strength BCR Bit

For adaptation to different system characteristics the output impedance can be configured. Full drive strength is targeted for 25-30 Ohm systems, half drive strength is targeted for 50 Ohm systems, and quarter drive strength is targeted for 100 Ohm systems.

12.2.1.7 PSRAM Burst Wrap BCR Bit

The burst wrap control bit defines whether there is a wrap around within a burst access or not. In case of fixed 8-word burst length, this means that after word #7, word #0 is going to be output in wrap mode.

In case of continuous burst mode the internal address counter will increment continuously until terminated by the system. For continuous burst mode or non-wrap mode, the burst access must be terminated prior to a row boundary crossing.

The burst wrap setting is used for both Write and Read operations.

12.2.1.8 PSRAM Burst Length BCR Bit

The burst length setting defines the Wrap boundary whenever Burst Wrap is enabled by setting BCR3 = 0b. When Burst Wrap is disabled by setting BCR3 = 1b, all burst behave as Continuous Bursts regardless of the Burst Length setting. Furthermore all fixed length bursts (4-, 8-, 16-, and 32-word bursts) will continue until terminated by bringing CE# high or interrupted by initiating a new burst access. Continuous Burst and Fixed Length Burst with Wrap Off will increment the address until a row boundary crossing is reached. Fixed Length Bursts will continue to wrap around and cycle through their limited address space until terminated or interrupted. The burst length setting is used for both Write and Read operations.

Table 22. PSRAM Burst Length Sequences

Burst Length	Starting Address [A4:A0]	Burst Address Sequence (decimal)	
		Wrap Off	**Wrap On**
4	00000b 00001b ... 11110b 11111b	0-1-2-3-4-5-6-7-...-EOR 1-2-3-4-5-6-7-8-...-EOR ... 30-31-32-33-34-...-EOR 31-32-33-34-35-...-EOR	0-1-2-3-0-1-2-3-... 1-2-3-0-1-2-3-1-... ... 30-31-28-29-30-31-28-29-... 31-28-29-30-31-28-29-30-...
8	00000b 00001b ... 11110b 11111b	0-1-2-3-4-5-6-7-...-EOR 1-2-3-4-5-6-7-8-...-EOR ... 30-31-32-33-34-...-EOR 31-32-33-34-35-...-EOR	0-1-2-3-4-5-6-7-0-1-2-3-... 1-2-3-4-5-6-7-0-1-2-3-4-... ... 30-31-24-25-26-27-28-29-30-... 31-24-25-26-27-28-29-30-31...
16	00000b 00001b ... 11110b 11111b	0-1-2-3-4-5-6-7-...-EOR 1-2-3-4-5-6-7-8-...-EOR ... 30-31-32-33-34-...-EOR 31-32-33-34-35-...-EOR	0-1-2-...-13-14-15-0-1-2-... 1-2-3-...-14-15-0-1-2-3-... ... 30-31-16-17-...-29-30-31-16-17-... 31-16-17-...-29-30-31-16-17-...
32	00000b 00001b ... 11110b 11111b	0-1-2-3-4-5-6-7-...-EOR 1-2-3-4-5-6-7-8-...-EOR ... 30-31-32-33-34-...-EOR 31-32-33-34-35-...-EOR	0-1-2-...-29-30-31-0-1-2-... 1-2-3-...-29-30-31-0-1-2-... ... 30-31-0-...-29-30-31-0-1-... 31-0-1-...-29-30-31-0-1-...
Continuous	00000b 00001b ... 11110b 11111b	0-1-2-3-4-5-6-7-...-EOR 1-2-3-4-5-6-7-8-...-EOR ... 30-31-32-33-34-...-EOR 31-32-33-34-35-...-EOR	0-1-2-3-4-5-6-7-...-EOR 1-2-3-4-5-6-7-8-...-EOR ... 30-31-32-33-34-...-EOR 31-32-33-34-35-...-EOR

Note: EOR = End of Row

12.2.2 PSRAM Refresh Control Register

The Refresh Control Register (RCR) allows for additional stand-by power savings by making use of the Partial-Array Self Refresh (PASR) and Deep Power Down (DPD) features. The RCR is programmed via the Control Register Set command (with CRE = 1 and A[18:19] = 00b) and retains the stored information until it is reprogrammed or the device loses power.

Reserved bit fields of the RCR should be ignored during a Fetch Control Register command as they may have undefined values even when set to 0b with a Set Control Register command. The RCR contents can only be set or changed when the PSRAM is in idle state.

Table 23.   PSRAM Refresh Control Register Map

	Reserved	Register Select		Reserved	Page Mode	Reserved		Deep Power Down (DPD)	Reserved	PASR		
DQ[15:0]				DQ16-DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
A[MAX:0]	A22 - A20	A19	A18	A17 - A8	A7	A6	A5	A4	A3	A2	A1	A0
RCR Bit	22 - 20	19	18	17 - 8	7	6	5	4	3	2	1	0

Table 24.   PSRAM Refresh Control Register Description

RCR Bit	NAME	Description
22:20	Reserved	Reserved bits should be set to '0' during set control register commands
19:18	Register Select	00 = Select RCR
17:8	Reserved	Reserved bits should be set to '0' during set control register commands
7	Page Mode	0 = Page Mode disabled (Default) 1 = Page Mode enabled
6:5	Reserved	Reserved bits should be set to '0' during set control register commands
4	Deep Power Down (DPD)	0 = DPD enabled 1 = DPD disabled (Default)
3	Reserved	Reserved bits should be set to '0' during set control register commands
2:0	Partial Array Self Refresh	000 = Full array refreshed (Default) 001 = Bottom 1/2 of array refreshed 010 = Bottom 1/4 of array refreshed 011 = Bottom 1/8 of array refreshed 100 = None of array refreshed 101 = Top1/2 of array refreshed 110 = Top1/4 of array refreshed 111 = Top1/8 of array refreshed

12.2.2.1 PSRAM Page Mode RCR Bit

In asynchronous (SRAM) mode, the user has the option to enable page mode. Page mode applies only to asynchronous read operations and has no impact on asynchronous write operations. In synchronous and NOR-Flash modes, the page mode setting has no impact on PSRAM operation. The maximum page length is 16 words, so A[3:0] is regarded as the page address.

Warning: When operating the PSRAM as an ADMux I/O interface by connecting the lower sixteen (16) addresses, A[15:0], to the data pins, Page-Mode operation cannot be used.

12.2.2.2 PSRAM Deep-Power Down RCR Bit

To put the device in deep power down mode the DPD control bit must be set low (RCR4 =0.) All internal voltage generators inside the PSRAM are switched off and the internal self-refresh is stopped. This means that all stored memory information will be lost by entering DPD. Only the register values of BCR, and RCR remain valid during DPD.

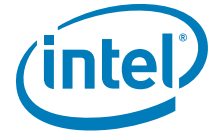#### 12.2.2.2.1 PSRAM Deep-Power Down Entry

To enter deep power down, RCR4 is set low, CE# is then pulled high and is maintained high for the entire time duration that Deep Power Down mode is desired. To insure proper operation, once CE# is pulled high, it should be maintained high for minimum of 150 µs before beginning the Deep Power Down Exit sequence.

12.2.2.2.2 PSRAM Deep-Power Down Exit

To exit the deep power down mode the CE# must go low for minimum 10 µs, followed by a guard time of at least 150 µs where CE# must be maintained high. Once deep power down is exited, the DPD control bit RCR4 is automatically reset to 1. All other Control Register contents are unchanged.

Figure 32. Deep Power Down Exit Timing
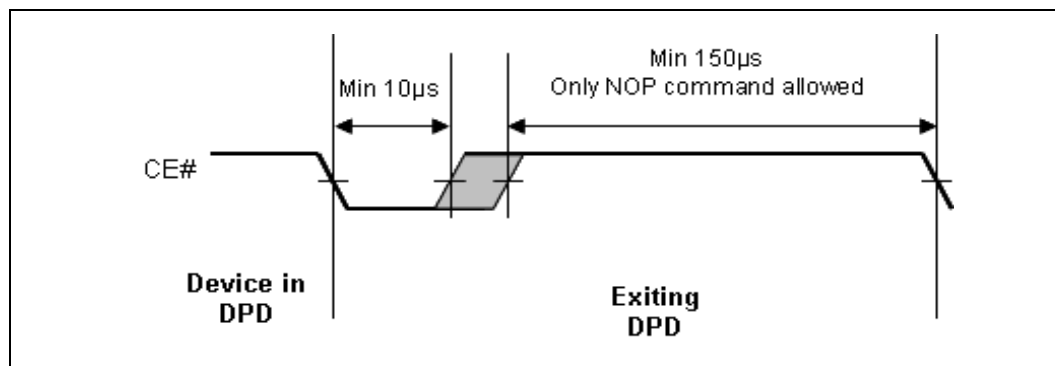
12.2.2.3 Description of PSRAM Partial-Array Self-Refresh RCR Bit

By applying PASR the user can dynamically customize the memory capacity to the system's actual need in normal operation mode and standby mode. RCR[2:0] specifies the active memory array and its location (starting from bottom or top). The memory parts not used are powered down immediately after the mode register has been programmed. Advice for the proper register setting including the address ranges is given in the figure below. PASR is effective in normal operation and standby mode as soon as it has been configured by register programming.

Table 25.   PSRAM PASR Address Pattern

Device	A2	A1	A0	Density (Mb)	Active Section	Address
64 Mbit	0	0	0	64	Full Array	000000h - 3FFFFFh
	0	0	1	32	Lower 1/2 of the array	000000h - 1FFFFFh
	0	1	0	16	Lower 1/4 of the array	000000h - 0FFFFFh
	0	1	1	8	Lower 1/8 of the array	000000h - 07FFFFh
	1	0	0	0	None	None
	1	0	1	32	Upper 1/2 of the array	200000h - 3FFFFFh
	1	1	0	16	Upper 1/4 of the array	300000h - 3FFFFFh
	1	1	1	8	Upper 1/8 of the array	380000h - 3FFFFFh
32 Mbit	0	0	0	32	Full Array	000000h – 1FFFFFh
	0	0	1	16	Lower 1/2 of the array	000000h – 0FFFFFh
	0	1	0	8	Lower 1/4 of the array	000000h – 07FFFFh
	0	1	1	4	Lower 1/8 of the array	000000h – 03FFFFh
	1	0	0	0	None	0
	1	0	1	16	Upper 1/2 of the array	100000h – 1FFFFFh
	1	1	0	8	Upper 1/4 of the array	180000h – 1FFFFFh
	1	1	1	4	Upper 1/8 of the array	1C0000h – 1FFFFFh

12.3   PSRAM Access to Control Register

The PSRAM control registers (BCR and RCR) can be updated at any time to select desired operating modes.

The control registers can be accessed by the hardware access method using the CRE pin or software access method consisting of a series of reads and writes.

The two methods are described in the sections below.

12.3.1   PSRAM Hardware Control Register Access

Hardware write or read access to the PSRAM registers occurs by applying the SCR and FCR commands with the CRE signal asserted high. During the SCR and FCR commands, A[19:18] designates target register. A[19:18] = 00b accesses the Refresh Control Register (RCR), A[19:18] = 10b accesses the Bus Control Register (BCR). The SCR and FCR commands can be applied in either synchronous or asynchronous mode.

After applying the SCR command in asynchronous mode, CE# must be pulled high for minimum of tCPH prior to initiating any subsequent command. After applying the SCR command in synchronous mode, CE# must be pulled high for minimum of tCPBH prior to initiating a subsequent synchronous command. Additionally, when applying the synchronous SCR command CE# must remain low to complete a burst of one write even though the DQ values are ignored by the PSRAM. To insure predictable device behavior, an SCR command should not be terminated or interrupted prematurely and ADV# should not go low more than one time prior to CE# being pulled high.

12.3.2 PSRAM Software Register Access

Software access of the registers uses a sequence of asynchronous read and asynchronous write operations. First, two asynchronous reads to the maximum address are performed followed by an asynchronous write to the maximum address. The data values during this asynchronous write select the appropriate register.

During the fourth operation, DQ[15:0] transfer data in to or out of the bits [15:0] of the registers.

During the software access sequence, it is necessary to:

- Toggle CE# between every read or write command (so the Device can distinguish 4 separate cycles).
- Maintain the address input until it is latched by ADV# or until CE# goes high. After setting the control registers using the software access method, CE# must be pulled high for minimum of tCPH prior to initiating any subsequent command.
- To insure predictable device behavior, the fourth access cycle of the software access should not be terminated or interrupted prematurely and ADV# should not go low more than one time during each access where CE# is low

Furthermore, during the 3rd cycle of the software access, the asynchronous write operation should be CE# controlled, that is on the 3rd cycle CE# must go high prior to WE# and UB#/LB#.

Figure 33. PSRAM Loading Configurations Registers Using Software Access
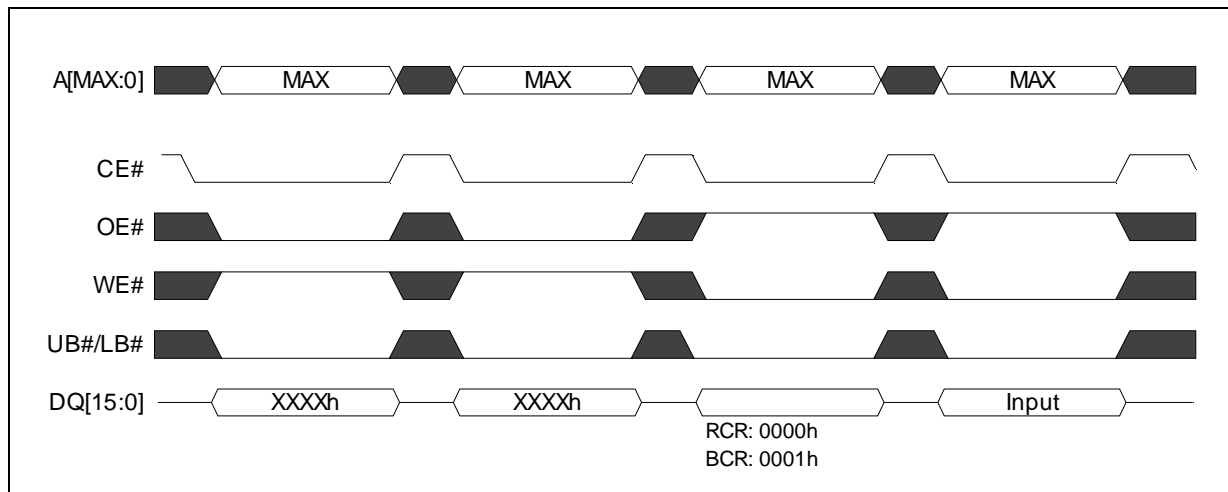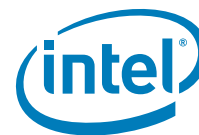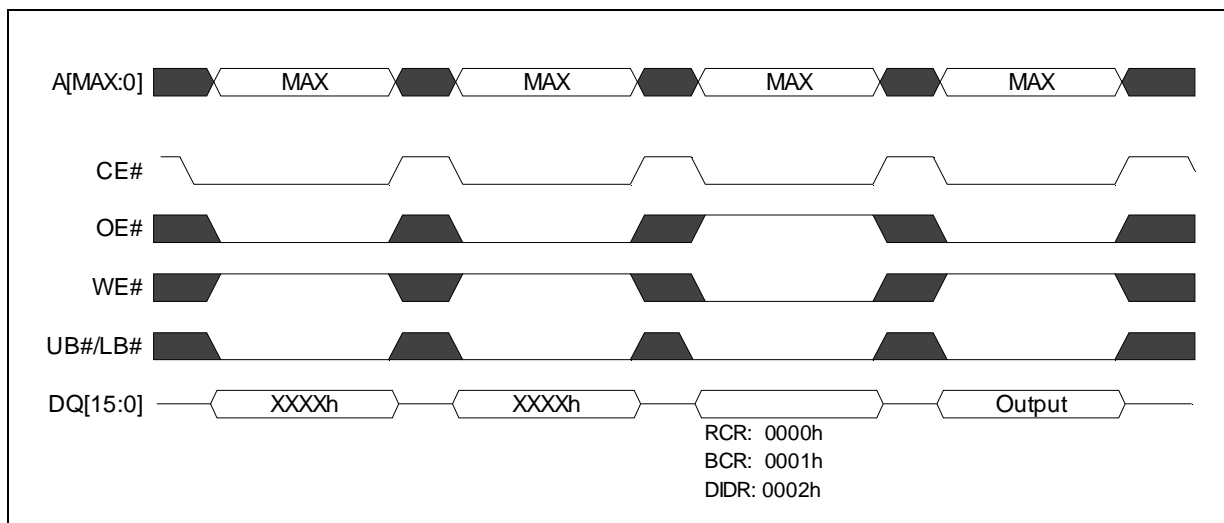
Figure 34. PSRAM Reading Registers Using Software Access

12.3.3 Cautionary Note About Software Register Access

To insure inadvertent access to the PSRAM registers during asynchronous operation, the system must avoid the below two command sequences when accessing the main memory array. On the 3rd cycle of the below command sequences the write to the main memory may be blocked and the software register access mode may be entered. To avoid such possibility, the system should avoid the below command sequences unless it is intending to access the registers through the software method.

Table 26. Cautionary Command Sequences

Cautionary Command Sequence #1

Address	Max	Max	Max
Command	Async Read	Async Read	Async Write

Cautionary Command Sequence #2

Address	Max	Max	Max
Command	Async Write (WE# controlled)	Async Read	Async Write

12.4   PSRAM Self-Refresh Operation

Unlike DRAMs, The PSRAM relieves the host system from issuing refresh commands. Self-refresh operations are autonomously scheduled and performed by the PSRAM device. In synchronous mode of operations (variable latency Read), the additional WAIT cycles are used to indicate when the data output is delayed in case a burst initiated access collides with an ongoing refresh cycle.

12.4.1   PSRAM Self-Refresh Operations at Low Frequency

At low frequencies (< 100 KHz), the PSRAM can support only asynchronous read (non-page and non-burst modes) operations. All other operations (asynchronous writes, page-mode reads, and synchronous burst-mode accesses) are subject to refresh restrictions.
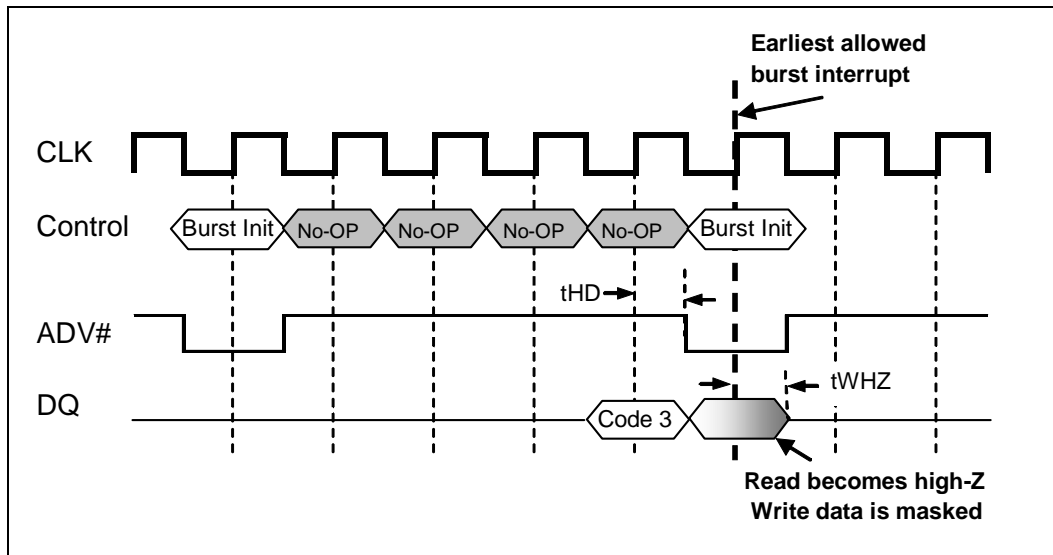
12.5   PSRAM Burst Suspend, Interrupt, or Termination

12.5.1   PSRAM Burst Suspend

While in synchronous burst operation, the bus interface may need to be assigned to other memory transaction sharing the same bus. Burst suspend is used to fulfill this purpose. Keeping CE# low (WAIT stays active although the DQ are tri-stated), burst suspend is initiated by halting CLK. CLK can stay at either high or low state. Burst suspend may also by initiated while WAIT is asserted during the initial latency period or at the end of a row.

As specified, duration of keeping CE# low can not exceed tCSL maximum so that internal refresh operation is able to run properly. In the event that tCSL maximum may be exceeded, termination of burst by bringing CE# high is strongly recommended instead of using burst suspend mode.

Figure 35. Example of PSRAM Burst Suspend with Read Burst with Latency Code 2

Note: WAIT is configured as Active Low and asserted during delay.

12.5.2 PSRAM Burst Interrupt

In burst interrupt an on-going burst is ended and new burst command issued while keeping CE# low (subject to tCSL restrictions.) To insure proper device operation, a burst interrupt is prohibited until the previous burst-init command completes its first valid data transaction. If a burst read is interrupted by a new burst command, the DQ are put into a high-Z state (within tWHZ time period.) If a burst write is interrupted by a new burst command, the write data is automatically masked regardless of UB#/LB# setting. Also note, that prior to initiating a burst interrupt by taking ADV# low, the ADV# high hold time of tHD must be met with respect to the previous clock cycle

Figure 36. **Example of PSRAM Burst Interrupt**

12.5.3 PSRAM Burst Termination

A burst access is terminated by bringing CE# high and maintaining high for minimum of tCBPH.

In burst mode a refresh opportunity must be provided every tCSL period by maintaining CE# high for minimum of 15ns or maintaining CE# high during a clock low to high transition.

12.6 PSRAM Row Boundary Crossing

Row boundary crossings are not allowed in burst mode (regardless of using variable or fixed latency mode.) An on-going burst must be terminated by the system prior to a row boundary crossing. A row boundary crossing would never occur if the PSRAM is operating in fixed burst length and wrap mode. Therefore the only time the system should be concerned with row boundary crossing is if the PSRAM is operating with "no wrap" (BCR3 = 0b) or "continuous burst length" (BCR[2:0] = 111b) settings.

In terminating bursts prior to row boundary crossing, the system may read the row size (128 or 256 words) to determine at which addresses the row boundary crossing occurs. If the system cannot do this, then it should be assumed that the row size is 128 words. In the case of 128-word row size the boundary between adjacent rows occurs at every address ending in 7Fh (111 1111 b.) In the case of 256-word row size the boundary between adjacent rows occurs at every address ending in FFh (1111 1111 b.)

At a Row boundary crossing, a burst interrupt or termination must occur no later than 2-clock cycle past the transaction representing the last word of a row.
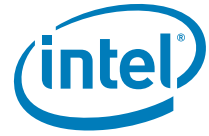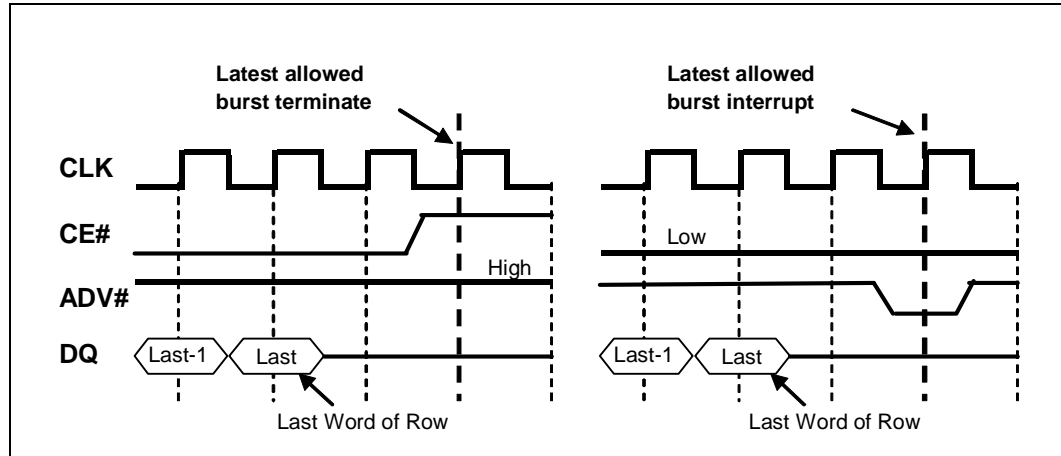
Figure 37. Terminating or Interrupting Burst Prior to Row Boundary Crossing

Appendix A Flash Write State Machine

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for the Write State Machine details.

Appendix B Flash Common Flash Interface

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for the Common Flash Interface (CFI) details.
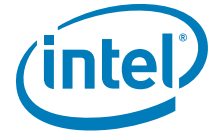
Appendix C Flash Flowcharts

Refer to the *Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet* (order number: Non-Mux I/O doc #251902 and ADMux I/O doc #313295) for the flash flowchart details.

Appendix D Additional Information

Order Number	Document
251902	Intel StrataFlash® Wireless Memory (L18 SCSP) Datasheet
251904	Intel StrataFlash® Wireless Memory (L18 SCSP) ADMux I/O Datasheet

Notes:
1. Call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel Sales Representative.
2. For current information on Intel® Flash memory products, software and tools, visit http://www.intel.com/design/flash/datashts/.

![intel logo]

Appendix E Ordering Information

Table 28 shows available L18 with synchronous PSRAM device combinations, and Table 29 provide additional device details.

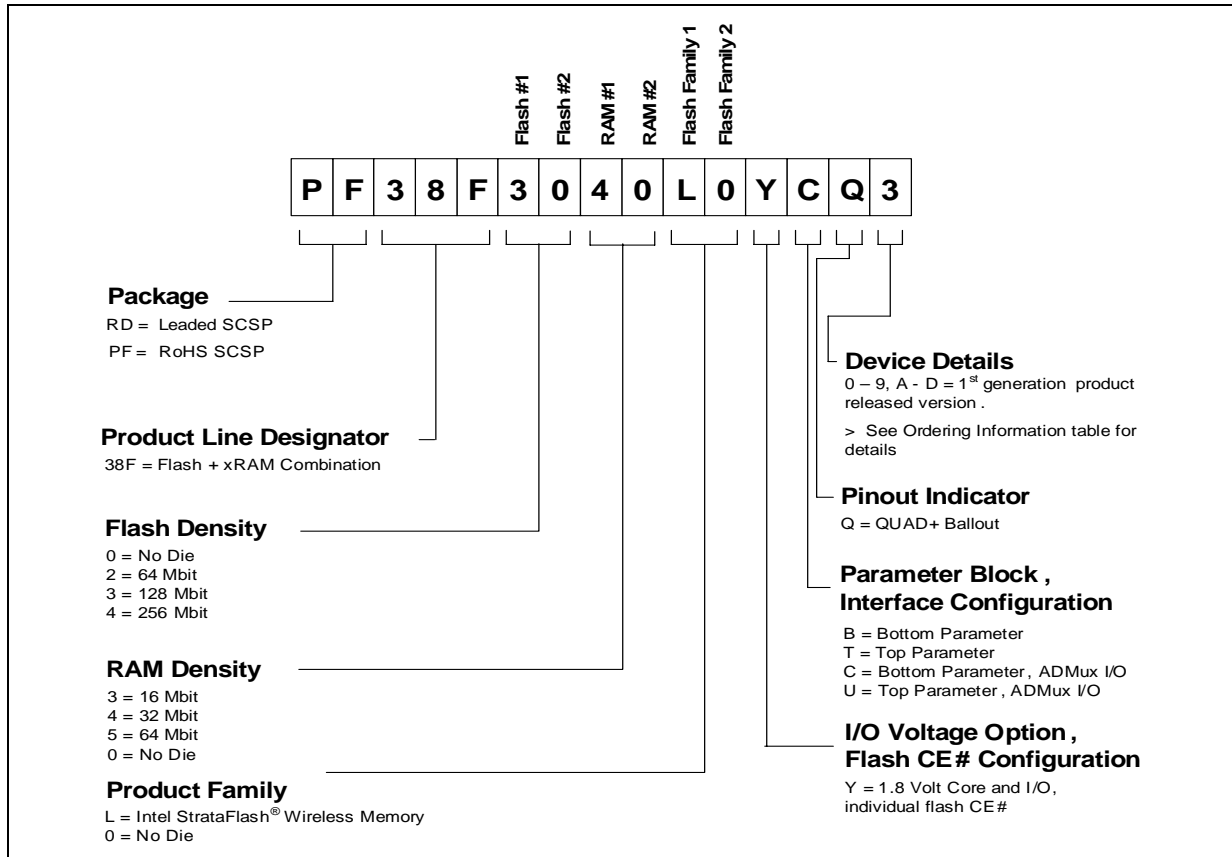**Figure 38. Ordering Information Decoder for L18 Family with Synchronous PSRAM**

Table 27. 38F and 48F Product Density Decoder

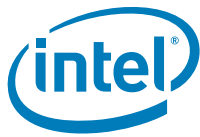| Code	Flash Die Density	RAM Die Density
0	No Die	No Die
1	32 Mbits	4 Mbits
2	64 Mbits	8 Mbits
3	128 Mbits	16 Mbits
4	256 Mbits	32 Mbits
5	512 Mbits	64 Mbits
6	1 Gbits	128 Mbits
7	2 Gbits	256 Mbits
8	4 Gbits	512 Mbits
9	8 Gbits	1 Gbits
A	16 Gbits	2 Gbits

Table 28.   Available Product Ordering Information

I/O Voltage (V)	Flash Family (Mbit)	xRAM Type (Mbit)	Package			Part Number	Add'l Detail Notes
			Size (mm)	Ballout Name	Ball Type		
1.8	128 L18 (ADMux I/O)	32 Sync PSRAM	8x10x1.2	QUAD+	RoHS	PF38F3040L0YCQ3 PF38F3040L0YUQ3	2,4,6
	128 L18 (ADMux I/O)	64 Sync PSRAM	8x10x1.2	QUAD+	RoHS	PF38F3050L0YCQ3 PF38F3050L0YUQ3	2,4,6
	256 L18 (ADMux I/O)	32 Sync PSRAM	8x10x1.2	QUAD+	RoHS	PF38F4040L0YCQ0 PF38F4040L0YUQ0	2,4,6
	256 L18 (ADMux I/O)	64 Sync PSRAM	8x11x1.2	QUAD+	RoHS	PF38F4050L0YCQ3 PF38F4050L0YUQ3	2,4,6

Table 29.   Ordering Information Additional Device Details

Add'l Detail Notes Reference	Additional Description Details
1	For devices not listed in this table, contact your local Intel representative for additional details.
2	Device request for -30 °C to +85 °C operation support, contact your local Intel representative for details.
3	Device is limited to a maximum operating frequency of 54 MHz with PSRAM tAC = 85 ns. Support only Fix Latency synchronous operations.
4	Device is limited to a maximum operating frequency of 54 MHz with PSRAM tAC = 70 ns. Support Fix or Variable Latency synchronous operations.
5	Custom device. Contact your local Intel representative for details.
6	L18 die is configured as an ADMux I/O interface device, while the PSRAM is configured as a Non-Multiplex I/O interface device. For an ADMux I/O interface device operation the PSRAM A[15:0] must be connected to the DQ[15:0] on the targeted PCB design. In addition, Page-Mode operation is not available. Contact your local Intel representative for details or design validation support.