S71GL064A based MCPs

Stacked Multi-Chip Product (MCP) Flash Memory and RAM 64 Megabit (4 M x 16-bit) CMOS 3.0 Volt-only Page Mode Flash Memory and 16/8 Megabit (1M/512K x 16-bit) Pseudo Static RAM / Static RAM

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71GL064A_00 **Revision** A **Amendment** 4 **Issue Date** September 6, 2007

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Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

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When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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Data Sheet

Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - 100 ns access time (100 ns Flash, 70 ns pSRAM/SRAM)
  - 25 ns page read times
- **Packages**
  - 7 x 9 x 1.2 mm 56 ball FBGA (TLC056)
- **Operating Temperature**
  - –25°C to +85°C

General Description

The S71GL064A product series consists of S29GL064 Flash memory with pSRAM and SRAM combinations defined as:

		Flash Memory Density
		64Mb
pSRAM / SRAM Density	8 Mb	S71GL064A80 (1) / S71GL064A08 (1)
	16 Mb	S71GL064AA0 / S71GL064A0A (1)
	32 Mb	S71GL064AB0

Note

1. *These MCPs are no longer offered, and customers are encouraged to migrate to the S71GL-N MCP product line. Please contact your local Spansion sales representative for more details.*

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29GL-A	S29GL-A_00
8 Mb pSRAM Type 1	pSRAM_12 (2)
16 Mb pSRAM Type 7	pSRAM_13
32 Mb pSRAM Type 8	pSRAM_31

Notes

1. *These MCPs are no longer offered, and customers are encouraged to migrate to the S71GL-N MCP product line. Please contact your local Spansion sales representative for more details.*
2. *This pSRAM is no longer valid as the base MCP is not being offered as per Note 1.*

1. Product Selector Guide

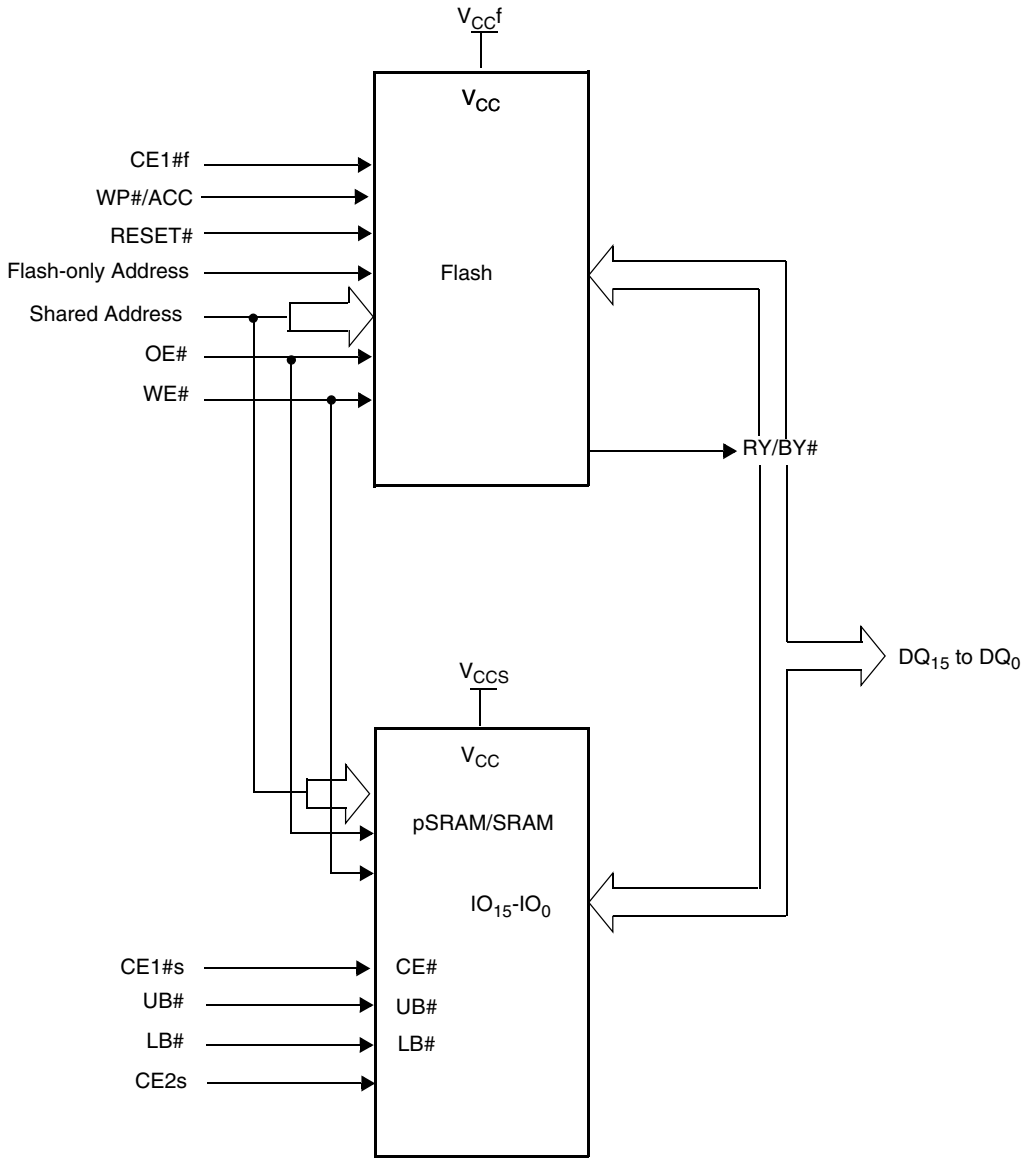
1.1 64 Mb Flash Memory

Device-Model# (Note)	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	(p)SRAM type	Package
S71GL064A80-0K	100	8 M pSRAM	70	pSRAM1	TLC056
S71GL064A80-0P					
S71GL064A08-0B		8 M SRAM		SRAM1	
S71GL064A08-0F					
S71GL064AA0-0K		16 M pSRAM		pSRAM1	
S71GL064AA0-0P					
S71GL064AA0-0U				pSRAM7	
S71GL064AA0-0Z					
S71GL064A0A-0B		16 M SRAM		SRAM1	
S71GL064A0A-0F					
S71GL064AB0-0U		32 M pSRAM		pSRAM 8	
S71GL064AB0-0Z					

Notes

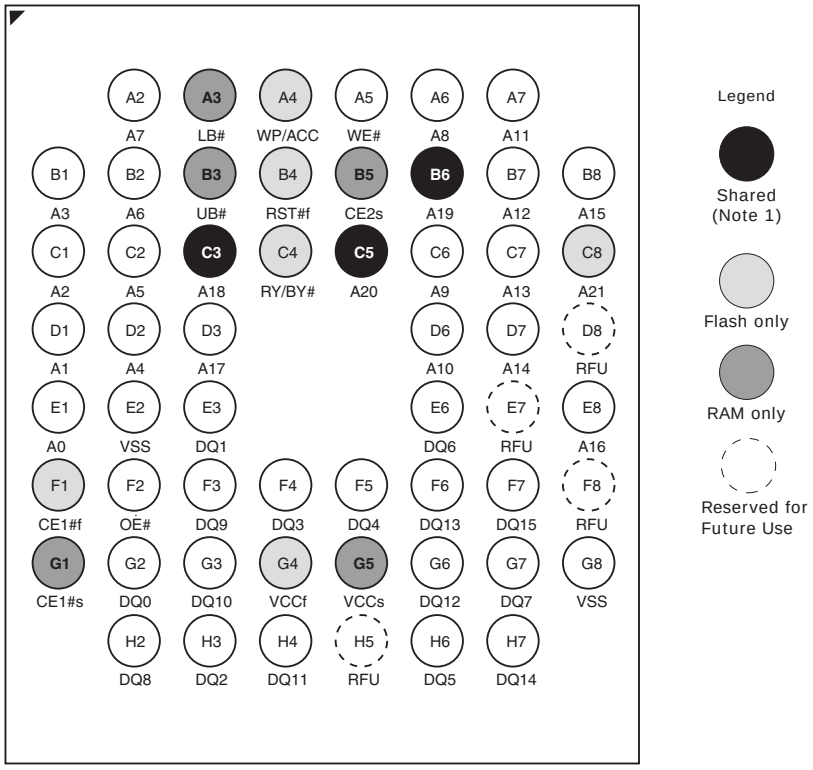
1. *Please see the valid combinations table for the model# description.*
2. *Shaded products indicate MCPs that are no longer offered.*

2. MCP Block Diagram



3. Connection Diagram (S71GL064A)

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Note

1. *May be shared depending on density.*
   - A19 is shared for the 16M pSRAM and above configurations.
   - A18 is shared for the 8M (p)SRAM and above configurations.

MCP	Flash-only Addresses	Shared Addresses
S71GL064AB0	A21	A20-A0
S71GL064AA0	A21-A20	A19-A0
S71GL064A0A	A21-A20	A19-A0
S71GL064A80	A21-A19	A18-A0
S71GL064A08	A21-A19	A18-A0

3.1 Special Handling Instructions For FBGA Package

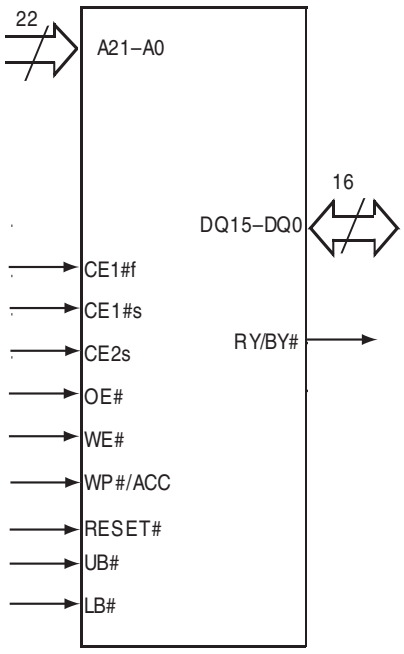
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4. Pin Description

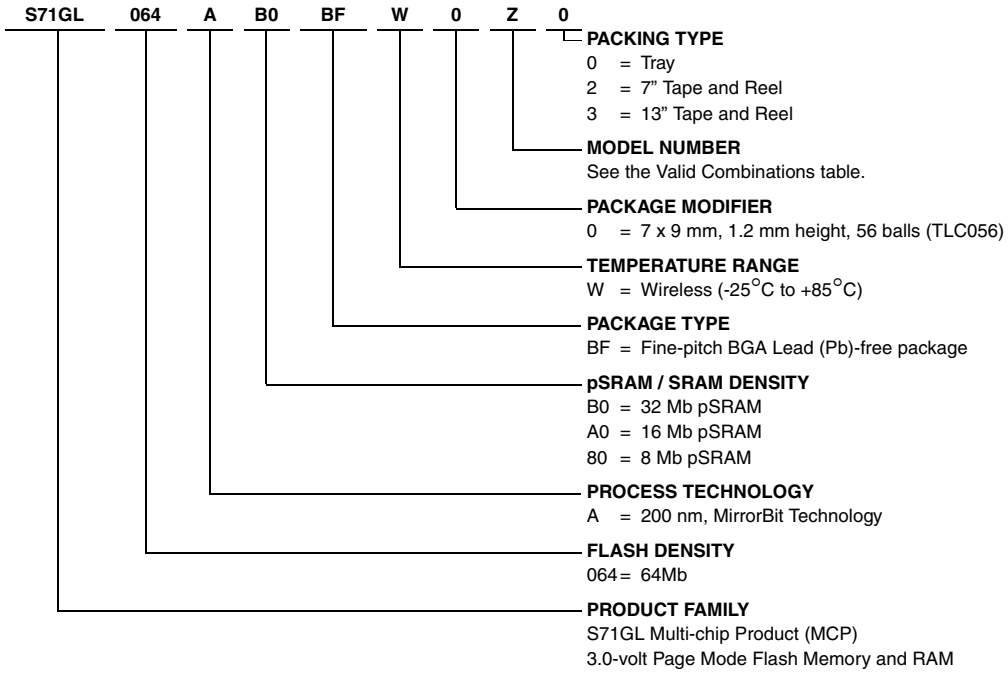
Pin	Description
A21–A0	22 Address Inputs (Common and Flash only)
DQ15–DQ0	16 Data Inputs/Outputs (Common)
CE1#f	Chip Enable (Flash)
CE1#s	Chip Enable 1 (pSRAM/SRAM)
CE2s	Chip Enable 2 (pSRAM/SRAM)
OE#	Output Enable (Common)
WE#	Write Enable (Common)
RY/BY#	Ready/Busy Output (Flash 1)
UB#	Upper Byte Control (pSRAM/SRAM)
LB#	Lower Byte Control (pSRAM/SRAM)
RESET#	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{CCS}	pSRAM/SRAM Power Supply
V_{SS}	Device Ground (Common)
NC	Pin Not Connected Internally

5. Logic Symbol



6. Ordering Information

The order number is formed by a valid combinations of the following:



S71GL064A Valid Combinations				Speed Options (ns)/Boot Sector Option	(p)SRAM Type/ Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/Model Number	Packing Type			
S71GL064A80	BFW	0K	0, 2, 3 (Note 1)	100 / Bottom Boot Sector	pSRAM1/ 70	TLC056
S71GL064A80		0P		100 / Top Boot Sector		
S71GL064A08		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A08		0F		100 / Top Boot Sector		
S71GL064AA0		0K		100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064AA0		0P		100 / Top Boot Sector		
S71GL064AA0		0U		100 / Bottom Boot Sector	pSRAM7 / 70	
S71GL064AA0		0Z		100 / Top Boot Sector		
S71GL064A0A		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A0A		0F		100 / Top Boot Sector		
S71GL064AB0		0U		100 / Bottom Boot Sector	pSRAM8 / 70	
S71GL064AB0		0Z		100 / Top Boot Sector		

Note

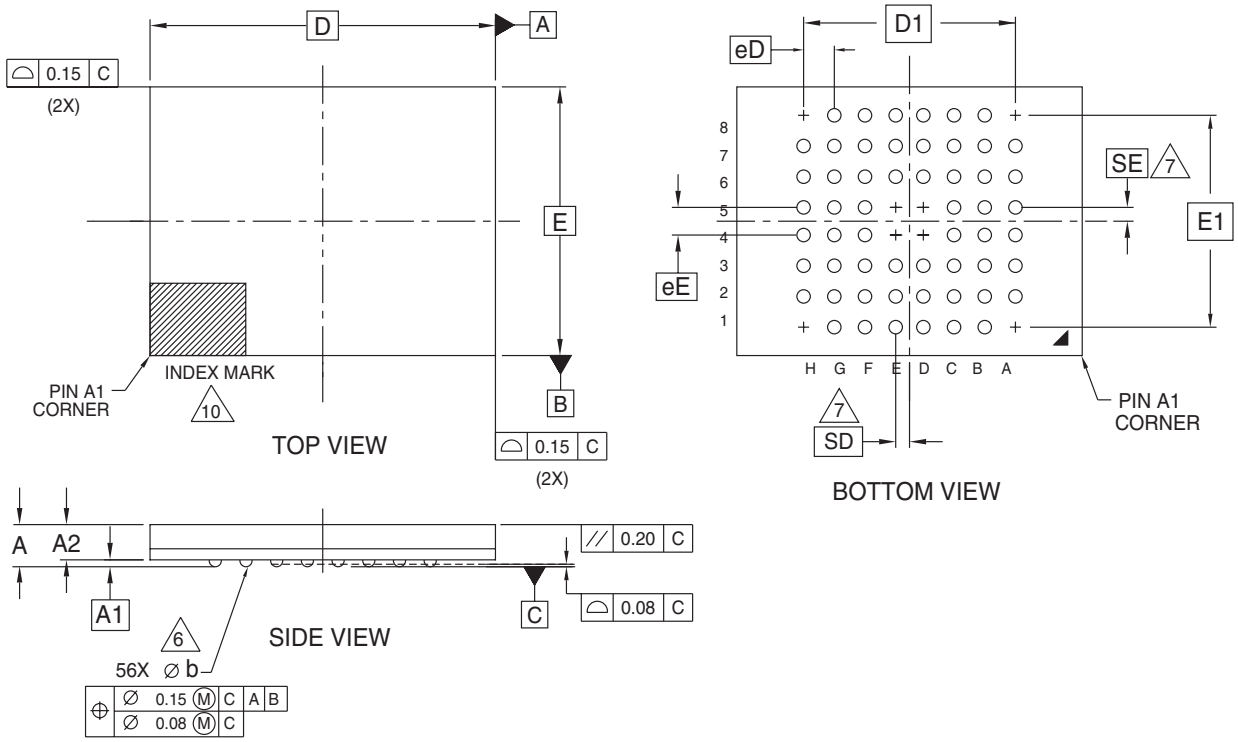
1. Type 0 is standard. Specify other options as required.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

7. Physical Dimensions

7.1 TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	7.00 BSC.			BODY SIZE
D1	5.60 BSC.			MATRIX FOOTPRINT
E1	5.60 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A1,A8,D4,D5,E4,E5,H1,H8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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8. Revision History

Section	Description
Revision A (October 28, 2004)	
	Initial release.
Revision A1 (December 7, 2004)	
Global	Access speed updated.
MCP Block Diagram	Control signals updated.
Pin Description	Descriptions updated.
Ordering Information	Package Modifiers and pSRAM densities updated.
Valid Combinations table	Speed options updated.
Revision A2 (February 8, 2005)	
pSRAM Type 7	Entire section updated.
Revision A3 (February 2, 2007)	
Global	Modularized format
Global	Added the 32Mb pSRAM Type 8
Revision A4 (September 6, 2007)	
Global	Removed Industrial temperature ordering option Noted obsolescence for all listed products in this document except the S71GL064AA0 and S71GL064AB0

Colophon

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