S71VS/XS-R Memory Subsystem Solutions

MirrorBit® 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode pSRAM

256/128/64 Mb (16/8/4 Mb x 16-bit) Flash,
128/64/32 Mb (8/4/2 Mb x 16-bit) pSRAM

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71VS_XS-R_00 **Revision** 08 **Issue Date** April 9, 2010

Downloaded from Elcodis.com electronic components distributor

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

Downloaded from Elcodis.com electronic components distributor

S71VS/XS-R Memory Subsystem Solutions

MirrorBit® 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode pSRAM

256/128/64 Mb (16/8/4 Mb x 16-bit) Flash, 128/64/32 Mb (8/4/2 Mb x 16-bit) pSRAM

Data Sheet

Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Flash / pSRAM Burst Speed: 108 MHz, 104 MHz, 83 MHz**
- **MCP BGA Packages**
  - 52 ball, 7.5 x 5.0 mm, 0.5 mm ball pitch
  - 56 ball, 7.7 x 6.2 mm, 0.5 mm ball pitch
  - 56 ball, 9.2 x 8.0 mm, 0.5 mm ball pitch
- **Operating Temperature**
  - Wireless, –25°C to +85°C

General Description

The S71VS-R Series is a product line of stacked Multi-Chip Package (MCP) memory solutions and consists of the following items:

- One or more S29VS-R or S29XS-R Flash memory die
- One or more pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual data sheet for further details.

Flash Density	pSRAM Density	Product
64 Mb	32 Mb	S71VS064RB0
128 Mb	32 Mb	S71VS128RB0
128 Mb	64 Mb	S71VS128RC0
256 Mb	64 Mb	S71VS256RC0
256 Mb	128 Mb	S71VS256RD0
256 Mb	128 Mb	S71XS256RD0

Publication Number S71VS_XS-R_00 **Revision** 08 **Issue Date** April 9, 2010

Downloaded from Elcodis.com electronic components distributor

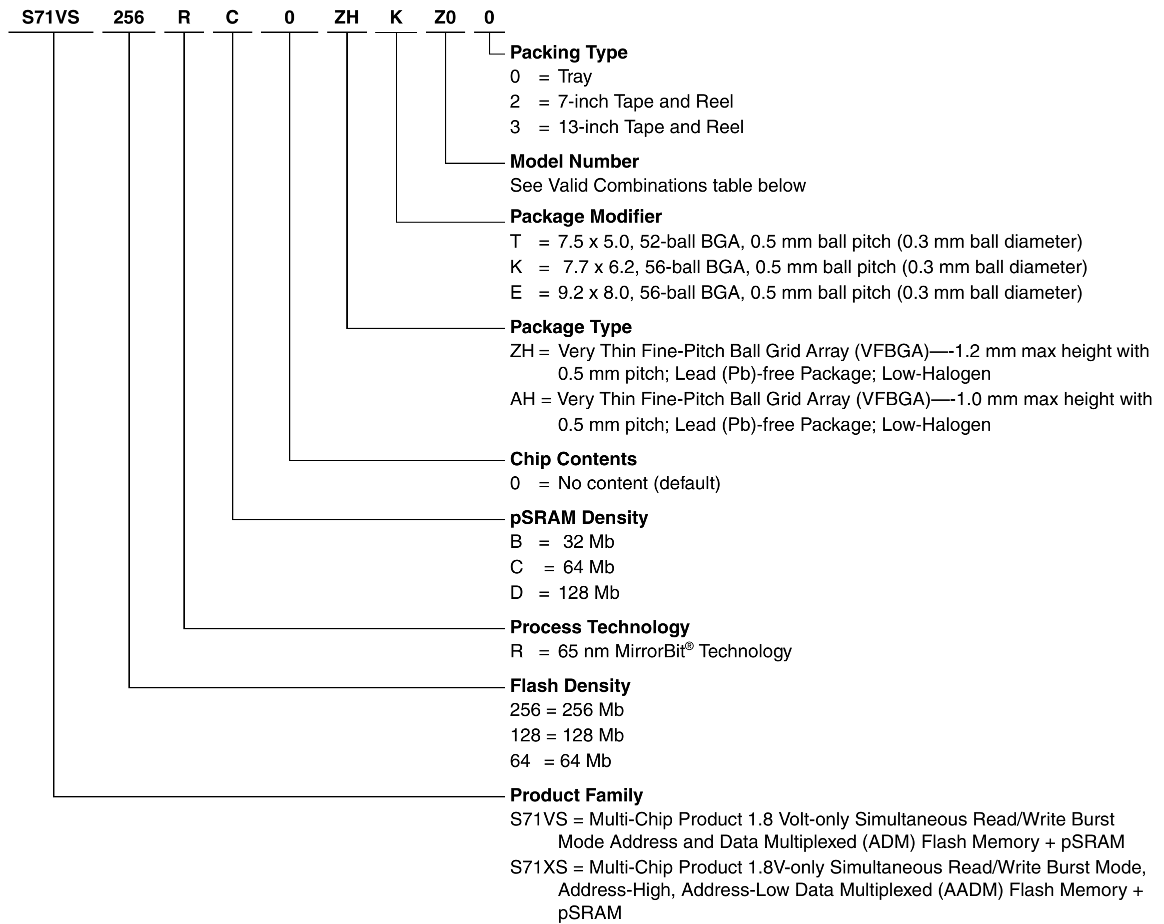
For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number
S29VS-R	S29VS_XS-R_00
S29XS-R	S29VS_XS-R_00
128 Mb MUX pSRAM Type 5	pSRAM_39
64 Mb MUX pSRAM Type 3	muxpsram_15
32 Mb MUX pSRAM Type 3	muxpsram_10
32 Mb MUX pSRAM	CustComspec_01
32 Mb CellularRAM Address/Data multiplexed	SWM032D108M1R_03
32 Mb CellularRAM Address/Data multiplexed	SWM032D108M1N_01
64 Mb CellularRAM Address/Data multiplexed	SWM064D108M1N_01
64 Mb CellularRAM Address/Data multiplexed	SWM064D108M1R_01

Downloaded from Elcodis.com electronic components distributor

1. Ordering Information

The order number is formed by a valid combinations of the following:



Downloaded from Elcodis.com electronic components distributor

1.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

<table>
<tr><th>Base Ordering Part Number</th><th>Package</th><th>Model Number</th><th>Packing Type</th><th>pSRAM Type</th><th>Flash Boot</th><th>Flash / pSRAM Speed</th><th>Pinout and Package Notes</th></tr>
<tr><td rowspan="2">S71VS064RB0</td><td rowspan="2">AHT</td><td>00</td><td rowspan="17">0, 2, 3</td><td rowspan="2">MUX pSRAM</td><td rowspan="17">Top Boot</td><td>104 MHz</td><td rowspan="2">Pinout: S71VS-R 52-ball
Package: RSB052</td></tr>
<tr><td>04</td><td>83 MHz</td></tr>
<tr><td rowspan="2">S71VS128RB0</td><td rowspan="4">AHK</td><td>2L</td><td>SWM032D108M1N</td><td rowspan="2">108 MHz</td><td rowspan="4">Pinout: S71VS-R 56-ball
Package: RSD056</td></tr>
<tr><td>0L</td><td>SWM032D108M1R</td></tr>
<tr><td rowspan="2">S71VS128RC0</td><td>20</td><td>MUX pSRAM Type 3</td><td>104 MHz</td></tr>
<tr><td>4L</td><td>SWM064D108M1R</td><td>108 MHz</td></tr>
<tr><td rowspan="3">S71VS128RC0</td><td rowspan="6">ZHK</td><td>2L</td><td>SWM064D108M1N</td><td>108 MHz</td><td rowspan="6">Pinout: S71VS-R 56-ball
Package: NSD056</td></tr>
<tr><td>20</td><td rowspan="2">MUX pSRAM Type 3</td><td>104 MHz</td></tr>
<tr><td>24</td><td>83 MHz</td></tr>
<tr><td rowspan="4">S71VS256RC0</td><td>2L</td><td>SWM064D108M1N</td><td>108 MHz</td></tr>
<tr><td>20</td><td rowspan="2">MUX pSRAM Type 3</td><td>104 MHz</td></tr>
<tr><td>24</td><td>83 MHz</td></tr>
<tr><td>AHK</td><td>4L</td><td>SWM064D108M1R</td><td>108 MHz</td><td>Pinout: S71VS-R 56-ball
Package: RSD056</td></tr>
<tr><td rowspan="2">S71VS256RD0</td><td rowspan="4">ZHE</td><td>40</td><td rowspan="4">MUX pSRAM Type 5</td><td>104 MHz</td><td rowspan="2">Pinout: S71VS-R 56-ball
Package: NLB056—56-ball</td></tr>
<tr><td>44</td><td>83 MHz</td></tr>
<tr><td rowspan="2">S71XS256RD0</td><td>40</td><td>104 MHz</td><td rowspan="2">Pinout: S71XS-R 56-ball
Package: NLB056</td></tr>
<tr><td>44</td><td>83 MHz</td></tr>
</table>

Downloaded from Elcodis.com electronic components distributor

2. Input/Output Descriptions

Table 2.1 identifies the input and output package connections provided on the device.

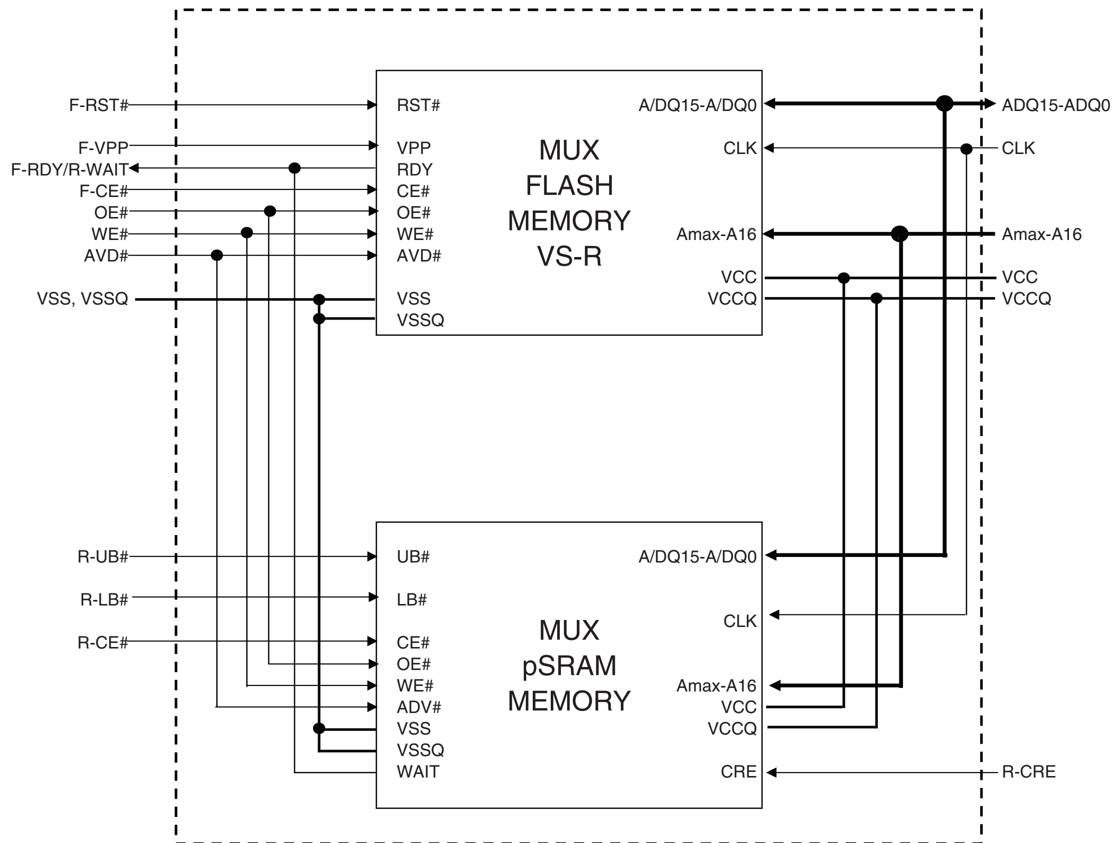
Table 2.1 Input/Output Descriptions

Symbol	Description	Flash	RAM
AMAX – A16	Address inputs	X	X
A/DQ15-A/DQ0	Multiplexed Address/Data	X	X
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.	X	X
WE#	Write Enable input.	X	X
V_{SS}	Ground	X	X
V_{SSQ}	Input/Output Ground	X	X
NC	No Connect; not connected internally	X	X
F-RDY/R-WAIT	Ready output; indicates the status of the Burst read. Flash Memory RDY (using default “Active HIGH” configuration) V_{OL} = data invalid V_{OH} = data valid Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal. pSRAM WAIT (using default “Active HIGH” configuration) V_{OL} = data valid V_{OH} = data invalid To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY)	X	X
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode	X	X
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs	X	X
F-RST#	Hardware reset input. Low = device resets and returns to reading array data	X	
F-V_{PP}	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	
R-CE#	Chip-enable input for pSRAM.		X
F-CE#	Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode.	X	
R-CRE	Control Register Enable (pSRAM).		X
V_{CC}	Flash and pSRAM 1.8 Volt-only single power supply.	X	X
V_{CCQ}	Flash and pSRAM Input/Output Power Supply	X	X
R-UB#	Upper Byte Control (pSRAM).		X
R-LB#	Lower Byte Control (pSRAM)		X
RFU	Reserved For Future Use		

Downloaded from Elcodis.com electronic components distributor

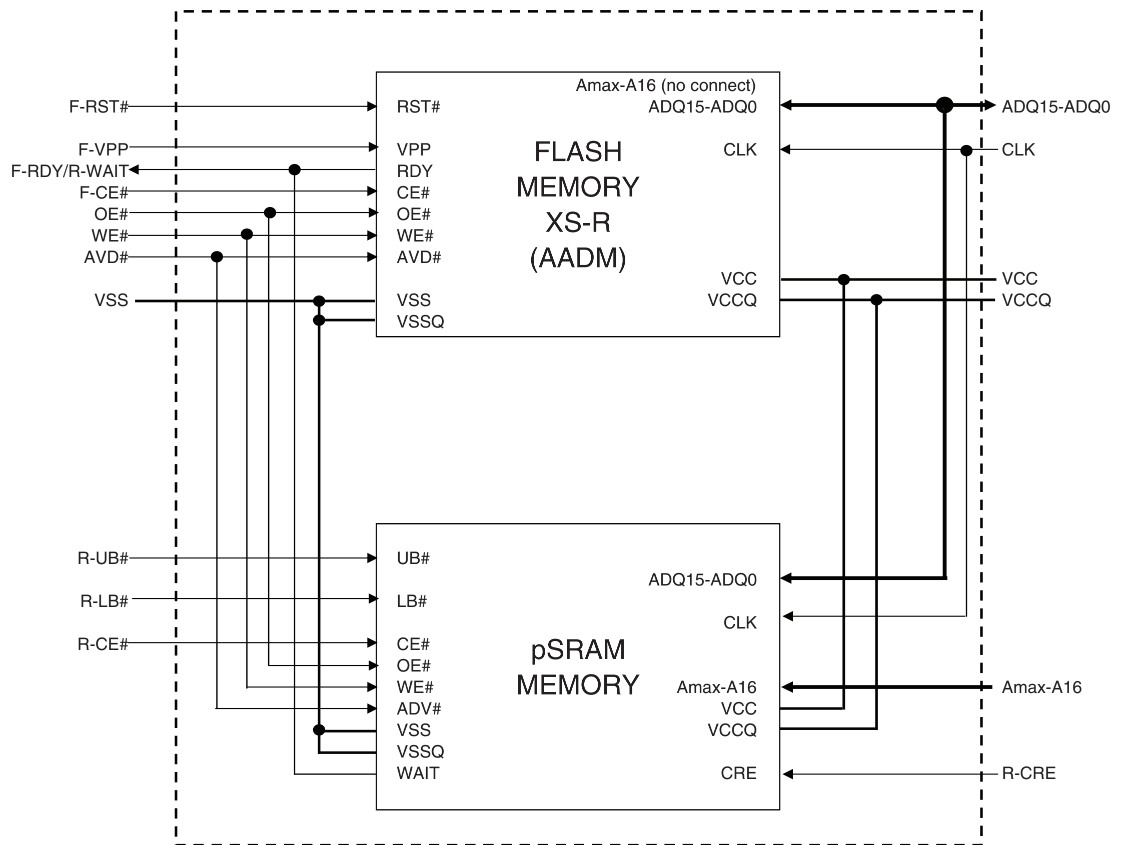
3. MCP Block Diagram

Figure 3.1 S71VS-R MCP Block Diagram



Downloaded from Elcodis.com electronic components distributor

Figure 3.2 S71XS-R MCP Block Diagram



Downloaded from Elcodis.com electronic components distributor

4. Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71VS-R.

4.1 Special Handling Instructions for FBGA Packages

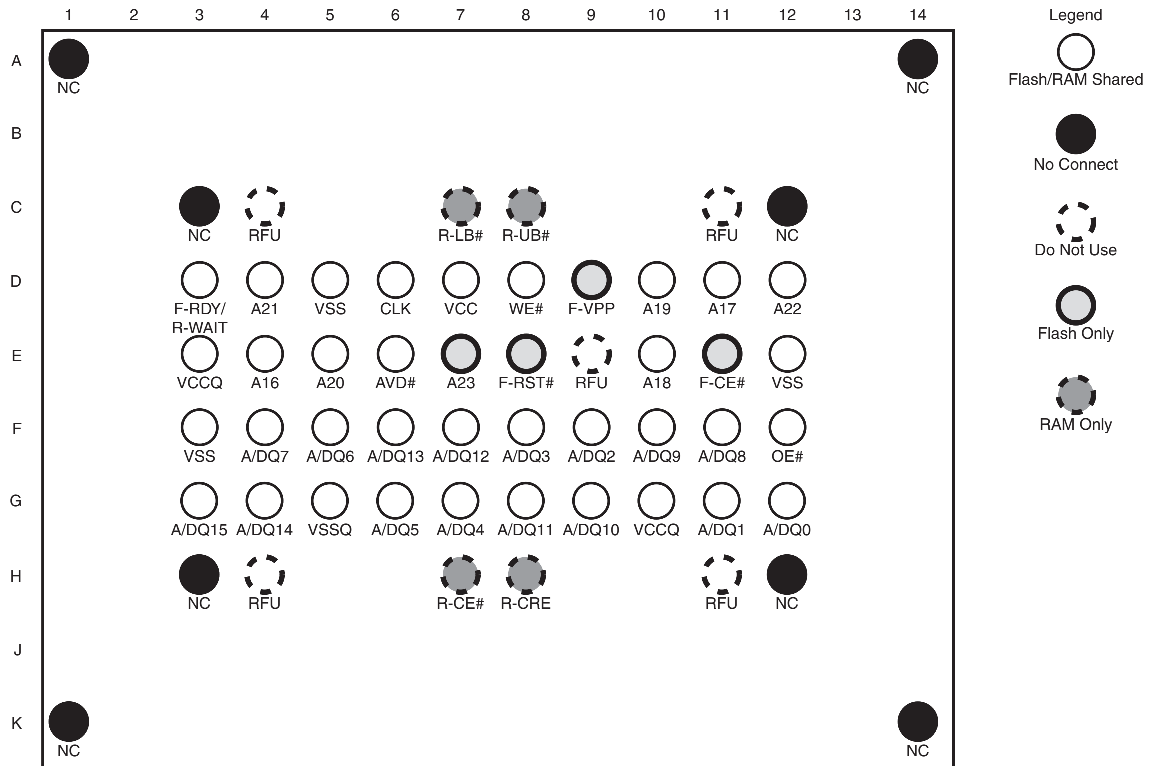
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4.2 Connection Diagrams

Figure 4.1 S71VS-R 56-ball Fine-Pitch Ball Grid Array

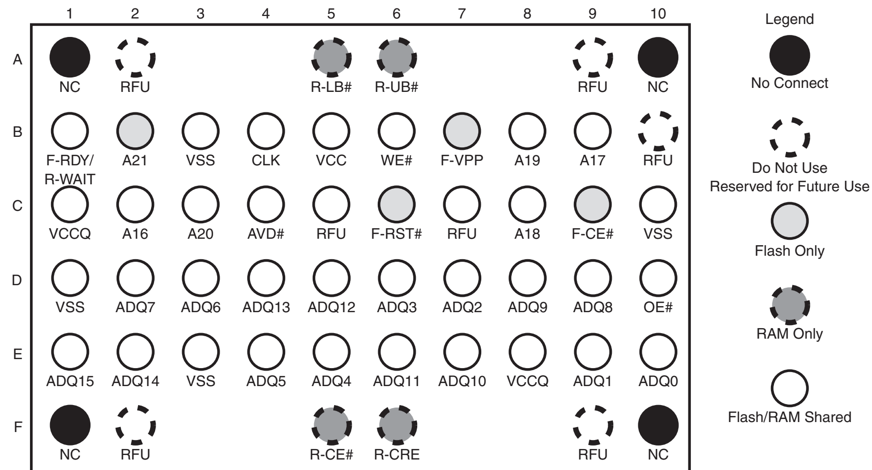
(Top View, Balls Facing Down)



Downloaded from Elcodis.com electronic components distributor

Figure 4.2 S71VS-R 52-ball Fine-Pitch Ball Grid Array

(Top View, Balls Facing Down)



Notes

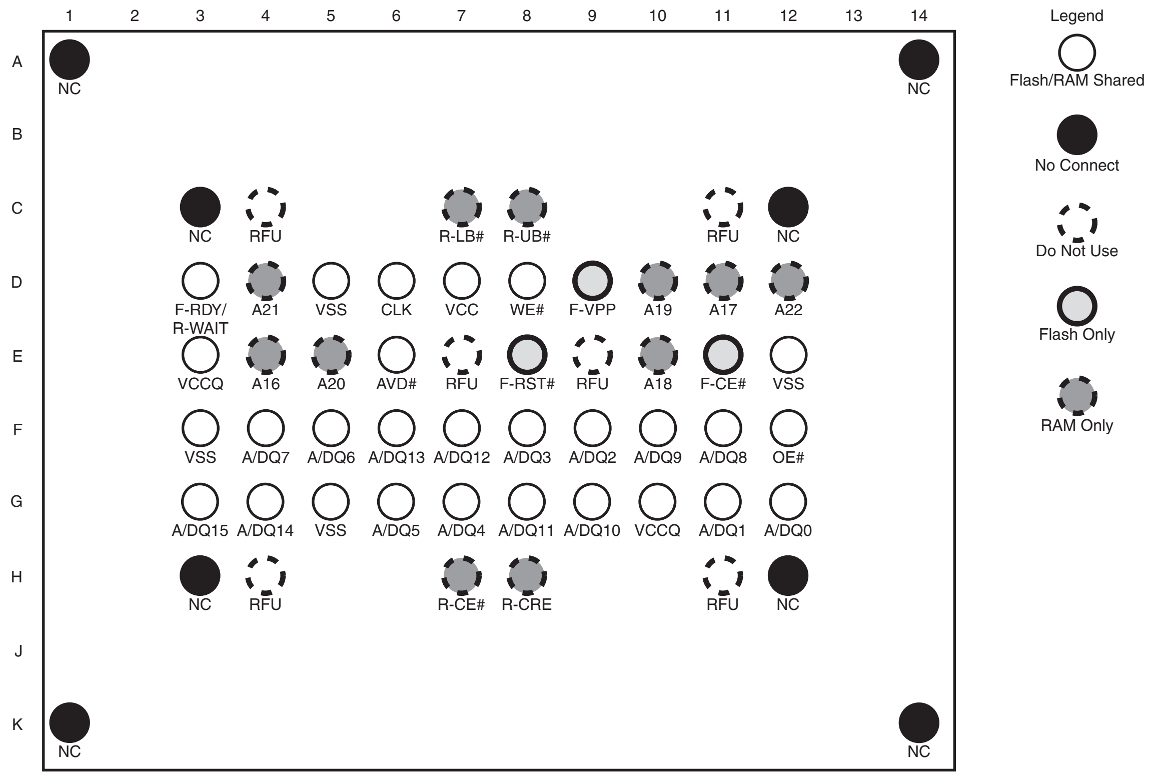
1. *Addresses are shared between Flash and RAM depending on the density of the pSRAM.*
2. *V_{SS} and V_{SSQ} must be connected together.*

MCP	Flash-Only Addresses	Shared Addresses	Shared ADQ Pins
S71VS064RB0	A21	A20-A16	A/DQ15-A/DQ0
S71VS128RC0	A22	A21-A16	
S71VS256RC0	A23-A22	A21-A16	
S71VS256RD0	A23	A22-A16	

Downloaded from Elcodis.com electronic components distributor

Figure 4.3 S71XS-R 56-ball Fine-Pitch Ball Grid Array

(Top View, Balls Facing Down)



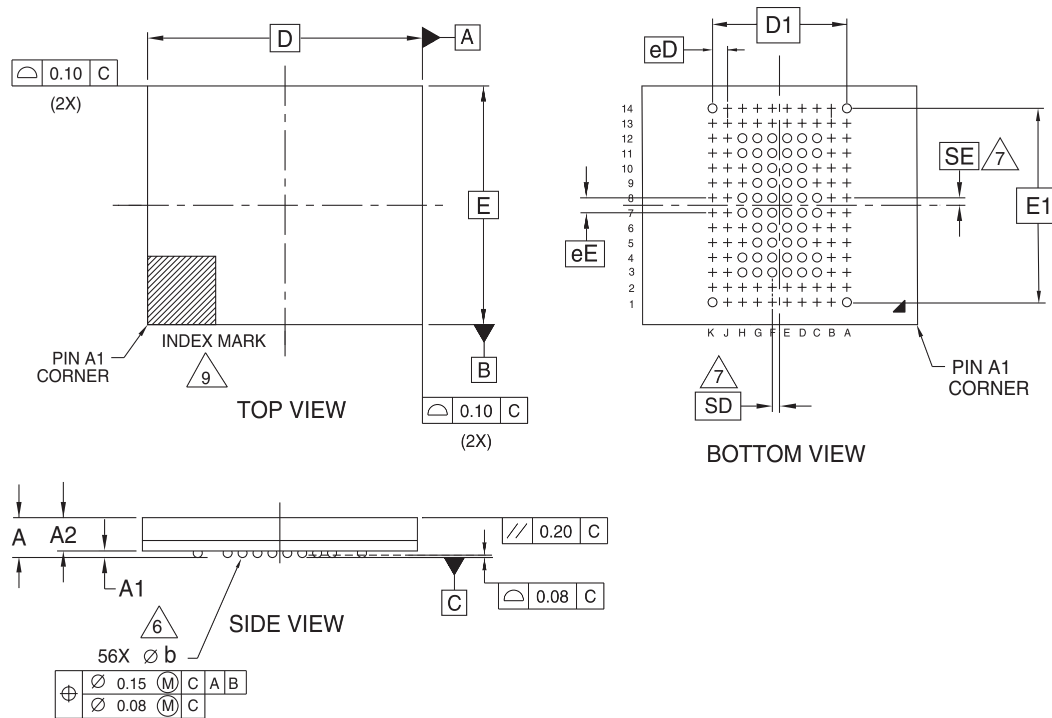
MCP	pSRAM-Only Addresses	Shared Addresses	Shared ADQ Pins
S71XS256RD0	A22-A16	N/A	A/DQ15-A/DQ0

Downloaded from Elcodis.com electronic components distributor

SPANSION®

4.3 Physical Dimensions

Figure 4.4 NLB056—56-ball VFBGA 9.2 x 8.0 mm



PACKAGE	NLB 056			
JEDEC	N/A			
D x E	9.20 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D	9.20 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	4.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2 ~ A13,B1 ~ B14 C1,C2,C5,C6,C9,C10,C13,C14 D1,D2,D13,D14,E1,E2,E13,E14,F1,F2,F13,F14 G1,G2,G13,G14,H1,H2,H5,H6,H9,H10,H13,H14 J1 ~ J14, K2 ~ K13			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

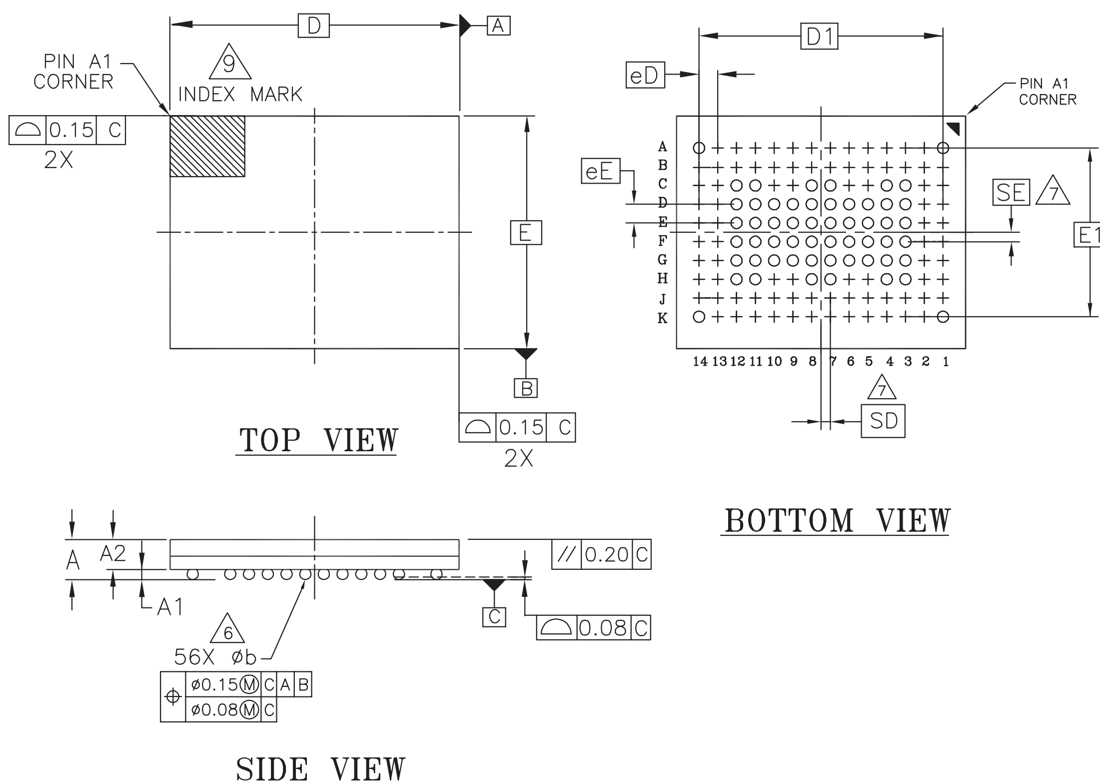
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3507\ 16-038.22 \ 7.14.5

Downloaded from Elcodis.com electronic components distributor

Figure 4.5 NSD056—56-ball VFBGA 7.7 x 6.2 mm



PACKAGE	NSD 056			
JEDEC	N/A			
D x E	7.70 mm x 6.20 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D	7.70 BSC.			BODY SIZE
E	6.20 BSC.			BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	4.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2~A9, B1~B10, C1,C2,C9,10,D1,D2,D9,D10 E1,E2,E3,E8,E9,E10,F1,F2,F3,F8,F9,F10,G1,G2,G9,G10 H1,H2,H9,H10,J1,J2,J3,J8,J9,J10,K1,K2,K3,K8,K9,K10 L1,L2,L9,L10,M1,M2,M9,M10, N1~N10, P2~P9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

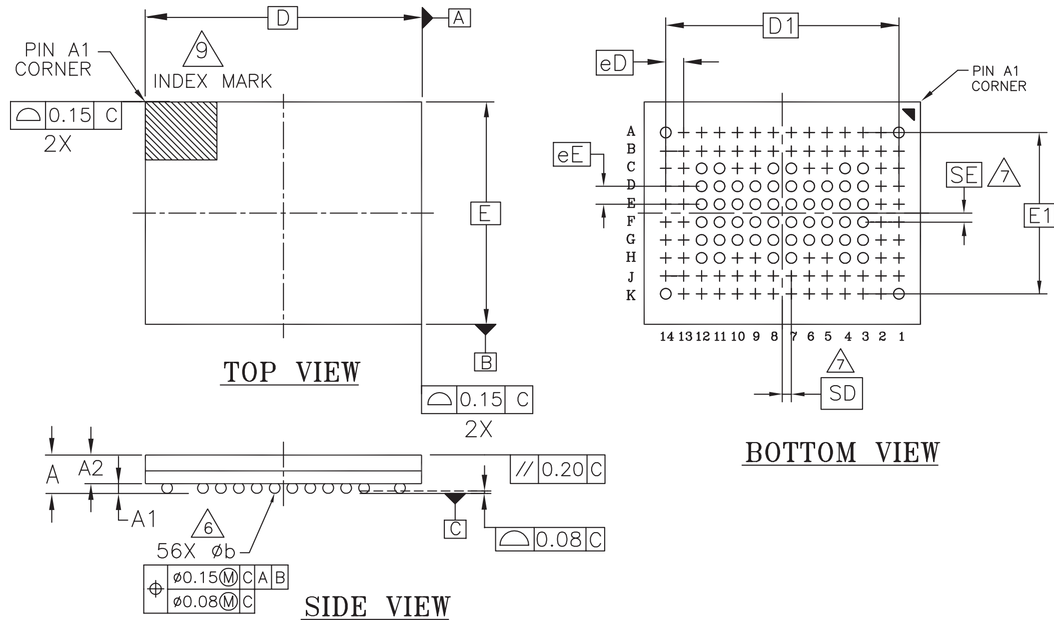
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3628 \ 16-038.22 \ 2.21.07

Downloaded from Elcodis.com electronic components distributor

Figure 4.6 RSD056—56-ball VFBGA 7.7 x 6.2 mm



PACKAGE	RSD 056			NOTE
JEDEC	N/A			
D x E	7.70 mm x 6.20 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	0.80	0.90	1.00	PROFILE
A1	0.18	---	---	BALL HEIGHT
A2	0.62	---	0.74	BODY THICKNESS
D	7.70 BSC			BODY SIZE
E	6.20 BSC			BODY SIZE
D1	6.50 BSC			MATRIX FOOTPRINT
E1	4.50 BSC			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC			BALL PITCH
eD	0.50 BSC			BALL PITCH
SE SD	0.25 BSC			SOLDER BALL PLACEMENT
	A2~A9, B1~B10, C1,C2,C9,10,D1,D2,D9,D10 E1,E2,E3,E8,E9,E10,F1,F2,F3,F8,F9,F10,G1,G2,G9,G10 H1,H2,H9,H10,J1,J2,J3,J8,J9,J10,K1,K2,K3,K8,K9,K10 L1,L2,L9,L10,M1,M2,M9,M10, N1~N10, P2~P9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

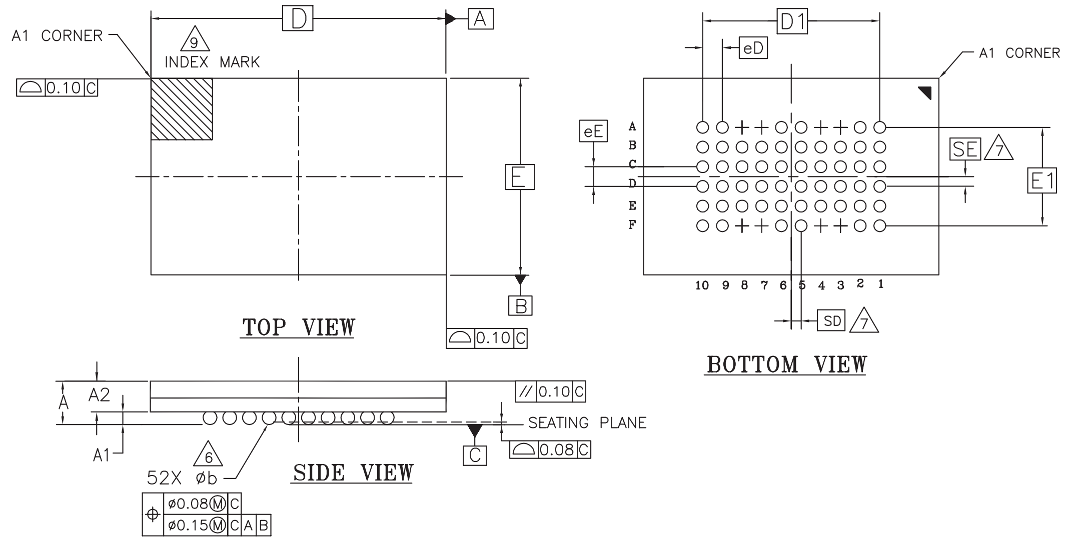
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3719 \ f16-038.63 \ 1.26.9

Downloaded from Elcodis.com electronic components distributor

Figure 4.7 RSB052—52-ball VFBGA 5.0 x 7.5 mm



PACKAGE	RSB 052			
JEDEC	N/A			
D x E	7.50 mm x 5.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	---	1.00	PROFILE
A1	0.18	---	---	BALL HEIGHT
A2	0.62	---	0.77	BODY THICKNESS
D		7.50 BSC		BODY SIZE
E		5.00 BSC		BODY SIZE
D1		4.50 BSC		MATRIX FOOTPRINT
E1		2.50 BSC		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		6		MATRIX SIZE E DIRECTION
n		52		BALL COUNT
Ø b	0.25	0.30	0.35	BALL DIAMETER
e		0.50 BSC		BALL PITCH
SE/SD		0.25 BSC		BALL PITCH
		3A,3F,4A,4F,7A,7F,8A,8F		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3711 \ 16-038.63 \ 10.24.8

Downloaded from Elcodis.com electronic components distributor

5. Revision History

Section	Description
Revision 01 (August 25, 2008)	
	Initial release
Revision 02 (November 4, 2008)	
Global	Added OPNs S71VS064RB0AHT00/04/80/84
Connection Diagrams	Added S71VS-R 52-ball connection diagram
Physical Dimensions	Added RSB052
General Description	Changed 128 Mb Mux pSRAM PID from TBD to pSRAM_39
Revision 03 (November 10, 2008)	
General Description	Changed 64 Mb MUX pSRAM Type 3 PID from muxpsram_14 to muxpsram_15
Revision 04 (January 13, 2009)	
Physical Dimensions	Replaced NLD056 with NSD056
Revision 05 (January 23, 2009)	
Valid Combinations	Added OPN S71VS128RC0AHK20
Physical Dimensions	Added RSD056
Revision 06 (March 11, 2009)	
Valid Combinations	Added 108 MHz speed grade to S71VS128RC0 and S71VS256RC0
Revision 07 (September 29, 2009)	
General Description	Added S71VS128RB0; added muxpsram_10
Valid Combinations	Added OPN S71VS128RB0
Revision 08 (April 9, 2010)	
General Description	Added SWM064D108M1R Updated pSRAM documentation names
Valid Combinations	Added OPNs: S71VS128RC0AHK4L S71VS256RC0AHK4L Removed Bottom Boot options
Connection Diagrams	Updated V_{SSQ} ball to V_{SS}

Downloaded from Elcodis.com electronic components distributor

Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

Trademarks and Notice

The contents of this document are subject to change without notice. This document may contain information on a Spansion product under development by Spansion. Spansion reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Spansion assumes no liability for any damages of any kind arising out of the use of the information in this document.

Copyright © 2008-2010 Spansion Inc. All rights reserved. Spansion®, the Spansion Logo, MirrorBit®, MirrorBit® Eclipse™, ORNAND™, EcoRAM™ and combinations thereof, are trademarks and registered trademarks of Spansion LLC in the United States and other countries. Other names used are for informational purposes only and may be trademarks of their respective owners.

Downloaded from Elcodis.com electronic components distributor