Intel® Wireless Flash Memory (W18 SCSP)

32-Mbit W18 + 8-Mbit SRAM (38F1020W0YTQ1, 38F1020W0YBQ1)

Datasheet

Product Features

- **Flash Architecture**
  - Flexible, Multi-Partition, Dual-Operation: Read-While-Write / Read-While-Erase
  - 8 Partitions, 4 Mbits each
  - 7 Main Partitions, 8 Main Blocks each
  - 1 Parameter Partition, 8 Parameter + 7 Main Blocks
  - 32-KWord Main Blocks, 4-KWord Parameter Blocks
  - Top and Bottom Parameter Configuration
- **Flash Performance**
  - 65 ns Initial Access Speed
  - 25 ns Page-Mode Read Speed; 4-Word Page
  - 14 ns Burst-Mode Read Speed
  - 4-, 8-, 16- or Continuous-Word Burst Modes
  - Burst- and Page-Mode Reads in Parameter and Main Partitions
  - Burst Suspend
  - Burst-Mode Reads can Traverse Partition Boundaries
  - Programmable WAIT Polarity
  - Enhanced Factory Programming: 3.1 µs/Word (typ)
- **Flash Data Protection**
  - Absolute Protection with VPP and WP#
  - Individual Dynamic Zero-Latency Block Locking
  - Individual Block Lock-Down
  - Erase/Program Lockout during Power Transitions
- **Flash Protection Register**
  - 64 Unique Device Identifier Bits
  - 64 User-Programmable OTP Bits
- **Flash Automation Suspend Operations**
  - Erase Suspend to Program or Read
  - Program Suspend to Read
  - 5 µs (typ) Program/Erase Suspend Latency
- **Flash Software**
  - Intel® Flash Data Integrator (Intel® FDI) Optimized
  - Common Flash Interface (CFI)
- **SCSP Architecture**
  - 32-Mbit Flash die + 8-Mbit SRAM die
  - Reduces Board Space Requirement
  - Simplifies PCB Design Complexity
  - Easy Migration to Future SCSP Devices
- **SCSP Voltage**
  - 1.7 V to 1.95 V V_{CC}/V_{CCQ} and S-V_{CC}
- **SCSP Packaging**
  - 0.8 mm Ball-Pitch Intel® SCSP
  - Area: 8x10 mm, Height: 1.2 mm max
  - 88-Ball (8 x 10 Matrix): 80 Active Balls with 2 Support Balls at Each Corner
- **SRAM Architecture and Performance**
  - 70 ns Access Time
  - Low-Voltage Data Retention Mode
- **Flash Quality and Reliability**
  - Extended Temperature: –25 °C to +85 °C
  - Minimum 100,000 Block Erase Cycles
  - Intel® 0.13 µm ETOX™ VIII Process Technology

This datasheet describes the key features of the Intel® Wireless Flash Memory (W18 SCSP) device. This device stacks a wireless flash memory device (W18) in combination with a low-power 8-Mbit SRAM device, into a versatile and compact Stacked Chip Scale Package (SCSP). The 32-Mbit W18 + 8-Mbit SRAM combination device described in this document provides a solution for high-performance, low-power, board-constrained memory applications. . Refer to the latest revision of the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) for flash device details not provided in this document.

Order Number: 252635, Revision: 003
28 Jun 2005

Contents

Revision History

Date of Revision	Version	Description
2/12/03	-001	Original SCSP release.
9/03	-002	Added number column to flash and RAM AC tables and updated title.
5/04	-002	Reformatted the datasheet according to the new layout.
28 Jun 2005	-003	Updated product number and ordering information

1.0 Introduction

This document contains information about the Intel® Wireless Flash Memory (W18 SCSP) 32-Mbit W18 + 8-Mbit SRAM SCSP device (38F1020W0YQ1).

This datasheet provides information about the 38F1020W0YQ1 SCSP device where it differs from the discrete Intel® Wireless Flash Memory (W18) device. Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) for information not provided in this document.

1.1 Nomenclature

0x	Hexadecimal prefix
Byte	8 bits
k	1000
Kword	1024 words
M	1,000,000
Mbits	1,048,576 bits
NC	No Connect
RFU	Reserved for Future Use
SCSP	Stacked Chip Scale Package
Word	16 bits

1.2 Conventions

Device	Term used interchangeably throughout this document to denote either a particular die or both die in the package.
R-OE#, R-LB#, R-UB#, R-WE#	Identifies OE#, LB#, UB#, and WE# RAM signals.
Using VCC and VPP or V_{CC} and V_{PP}	• When the reference is to a signal or package connection name, the notation is VCC or VPP. • When the reference is to a timing or level, the notation is subscripted (for example, V_{CC} or V_{PP}).

2.0 Functional Overview

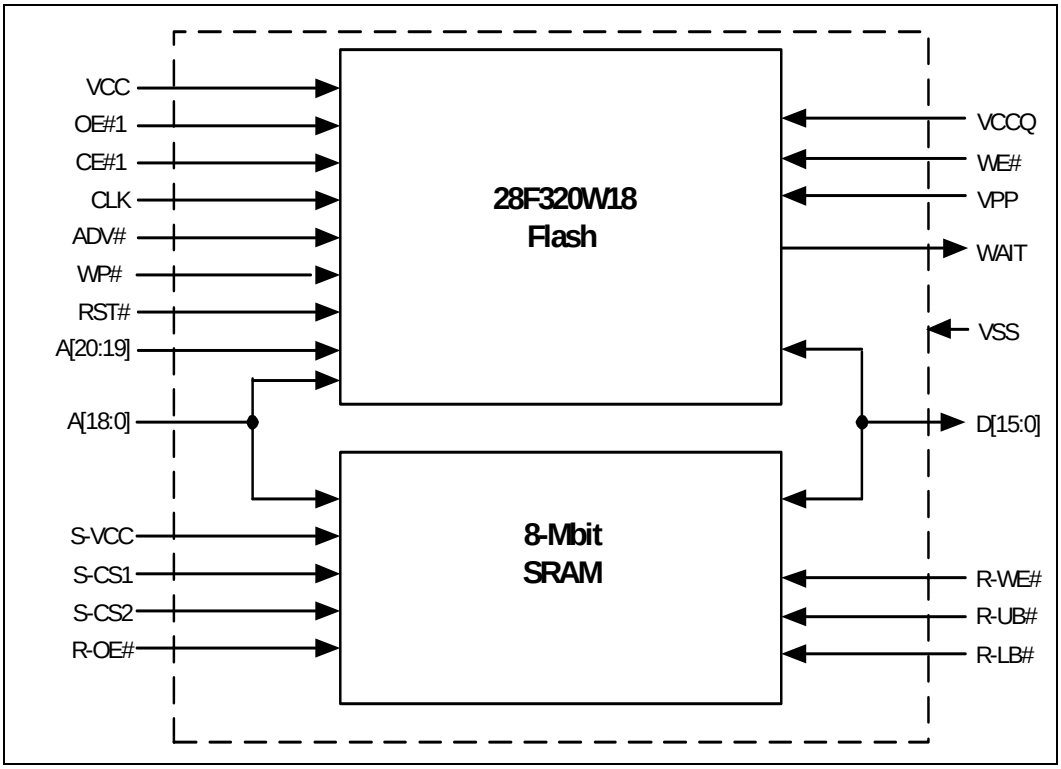
This section provides an overview of 38F1020W0YQ1 device features.

The 38F1020W0YQ1 devices combine one flash and one SRAM die into a single package. Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* for an overview of the flash product features.

2.1 Block Diagram

Figure 1 is the block diagram for the 38F1020W0YQ1 devices. Refer to Table 1 “Signal Descriptions” on page 9 for a description of each signal shown.

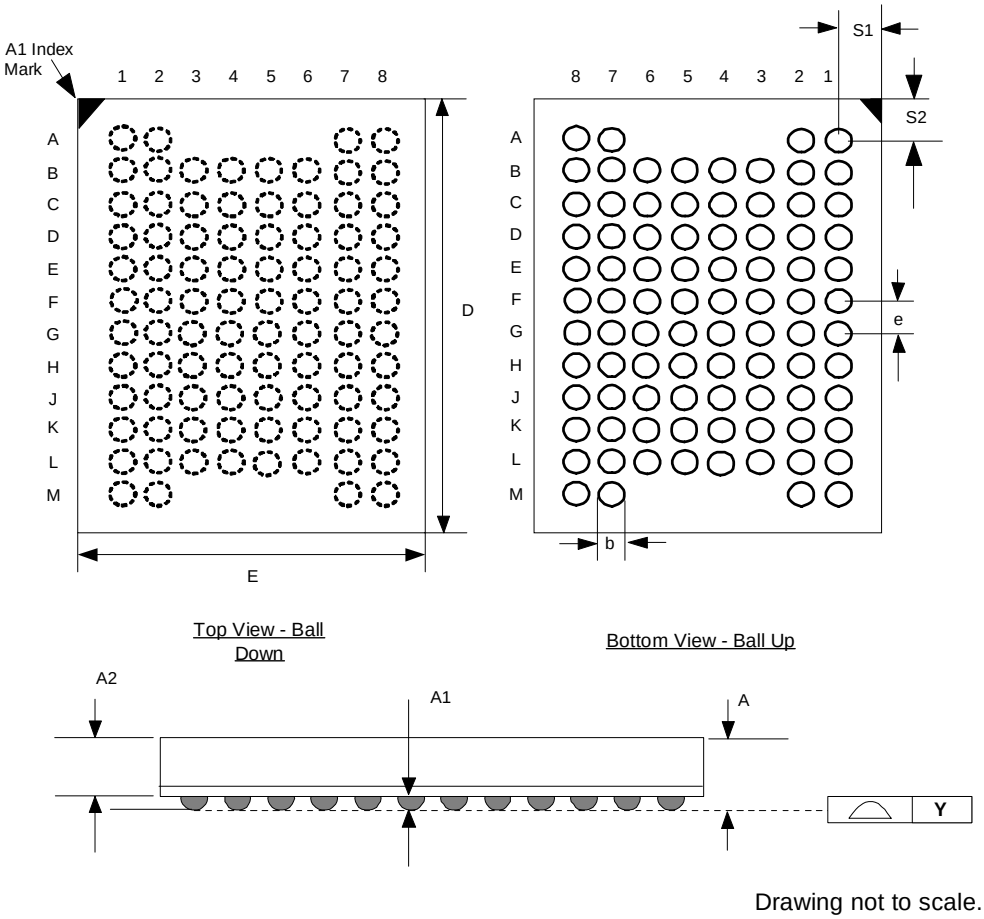
Figure 1. Block Diagram



3.0 Package Information

3.1 88-Ball Mechanical Specification

Figure 2. 88-Ball Mechanical Specification



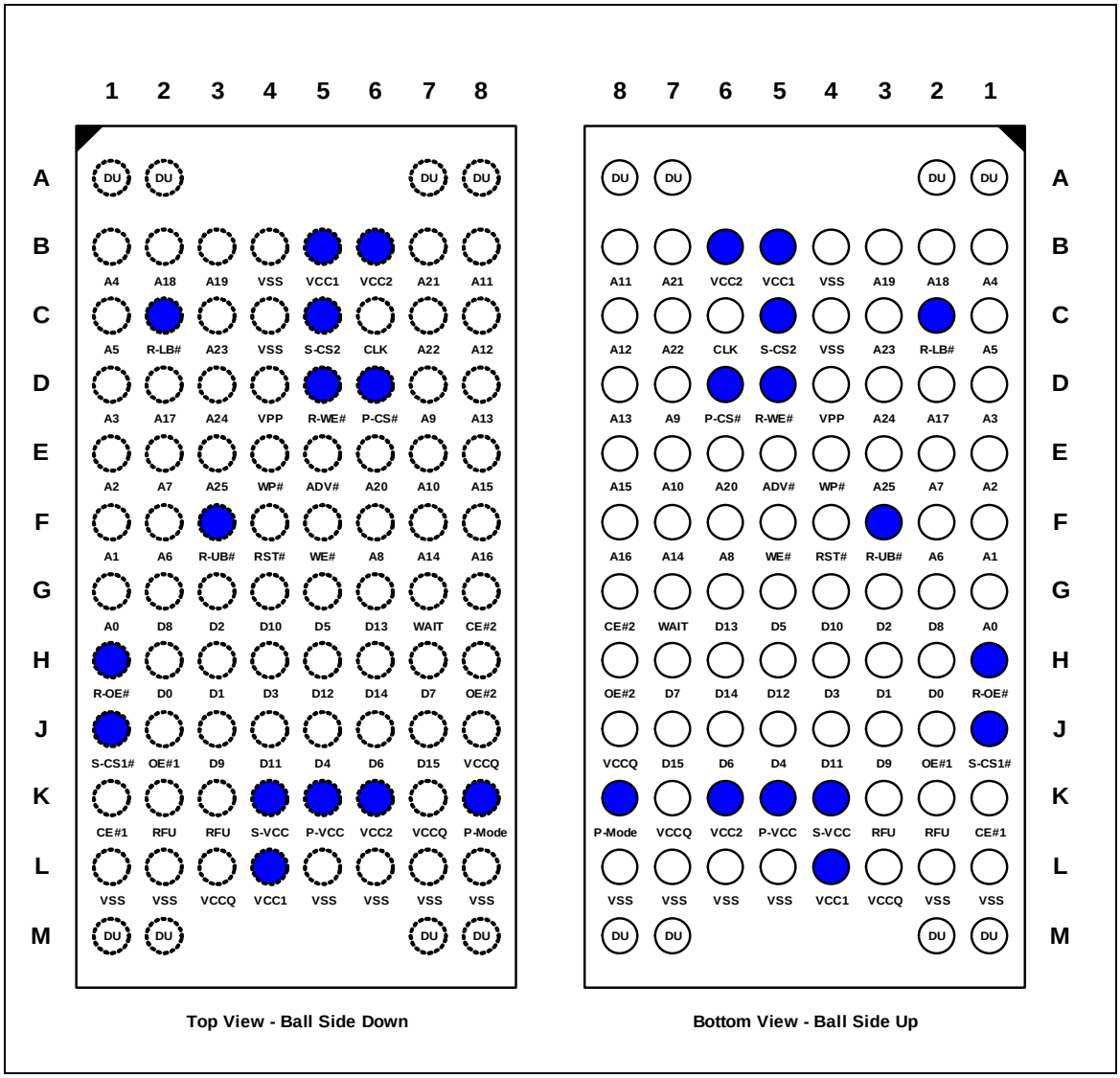
Drawing not to scale.

		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

4.0 Ballout and Signal Description

The 38F1020W0YQ1 devices are available in an 88-ball SCSP with ball pitch of 0.8 mm. Figure 3 shows the ballout.

Figure 3. 88-Ball SCSP Package Diagram



4.1 Signal Descriptions

Table 1 describes the active signals used on the 38F1020W0YQ1 devices.

Table 1. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Name and Function
A[25:0]	Input	**ADDRESS INPUTS:** Decodes a specific location for reads or writes, or targets a flash device block for erase. Flash memory addresses are latched during writes, and for reads when ADV# (or CLK with ADV# low) is issued. • A[20:0] decodes a specific location within the 28F320W18 die. • A[18:0] decodes a specific location within the 8-Mbit SRAM. • A[25:21] is not used in this SCSP device and is Reserved for Future Use (RFU).
D[15:0]	Input/ Output	**DATA INPUTS/OUTPUTS:** Inputs data for SRAM writes or flash device programming. Flash memory commands issued during CUI writes are input on D[7:0] only. • D[15:0] outputs the device memory contents or flash device ID codes. D[15:0] are floated when the device is deselected or the outputs are disabled. • Flash memory SRD is read on D[7:0] only. • Flash device I/Os D[15:8, 6:0] are floated when the flash device WSM is busy.
CE#1, CE#2	Input	**FLASH CHIP ENABLE:** • CE#1-low selects the flash device. – When asserted, the flash device internal control logic, input buffers, decoders, and sense amplifiers are activated. – When deasserted, the flash die is deselected, power levels reduce to standby, and data and WAIT outputs are placed in high-Z state. • CE#2 is not used in this SCSP device and is RFU.
S-CS1#, S-CS2	Input	**SRAM CHIP SELECTS:** Activates the SRAM internal control logic, input buffers, decoders, and sense amplifiers. When either are deasserted (S-CS1# = V_{IH} or S-CS2 = V_{IL}), the SRAM is deselected and its power reduces to standby levels.
RST#	Input	**FLASH RESET:** RST#-low resets the flash device internal circuitry and inhibits write operations. Use this function to protect data during power transitions. After exiting the reset state (RST# returned to logic-high), the selected flash die resumes operation in asynchronous read-array mode.
OE#1, OE#2	Input	**FLASH OUTPUT ENABLE:** OE#1-low activates device output through the flash memory device data buffers during a flash memory read cycle. When deasserted, the flash device outputs tristate to high-Z. OE#2 is not used in this SCSP device and is RFU.
R-OE#	Input	**SRAM OUTPUT ENABLE:** R-OE#-low activates device output through the SRAM data buffers during a SRAM read cycle. When deasserted, the SRAM outputs tristate to high-Z.
WE#	Input	**FLASH WRITE ENABLE:** WE# controls writes to the selected flash memory die. WE#-low allows input to the flash device CUI, array, PR/PLR, RCR, or block lock bits. Addresses and data latch on the signal rising edge.
R-WE#	Input	**SRAM WRITE ENABLE:** R-WE#-low allows writes to the SRAM array.
R-UB#, R-LB#	Input	**SRAM UPPER / LOWER BYTE ENABLES:** R-UB#-low enables the SRAM high-order bytes (D[15:8]). R-LB#-low enables the SRAM low-order bytes (D[7:0]).

Table 1. Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Name and Function
ADV#	Input	**FLASH ADDRESS VALID:** • During synchronous reads, flash device addresses latch on the ADV# rising edge or on a CLK transition with ADV# low. • For asynchronous reads, either drive ADV# high to latch an address or hold ADV# low throughout the read cycle.
CLK	Input	**FLASH CLOCK:** CLK synchronizes the flash device to the system bus frequency. Used only for burst reads, CLK increments the internal address generator within the flash device. If ADV# is asserted low, the flash device uses a CLK transition to latch externally-applied addresses .
WAIT	Output	**FLASH WAIT:** Indicates that the flash memory D_{OUT} is not yet valid. Used only for synchronous reads. WAIT is high-Z if CE#1 is deasserted, but is not gated by OE#1.
WP#	Input	**FLASH WRITE PROTECT:** Enables/disables the flash lock-down mechanism. WP#-low secures locked-down blocks from software unlock attempts. WP#-high overrides the lock-down function, thus allowing system software to unlock locked-down blocks.
VPP	Power	**FLASH PROGRAM/ERASE SUPPLY:** Hardware program and erase protection. A valid voltage level allows program or erase; memory contents cannot be altered when V_{PP} is at or below the V_{PP} lockout voltage (V_{PPLK}). Do not attempt program or erase at invalid V_{PP} voltages. Set $V_{PP} = V_{CC}$ for in-system read, program and erase operations. V_{PP} must remain above V_{PP1MIN} for in-system program or erase operations. V_{PP2} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. V_{PP} can be V_{PP2} for cumulative total, not to exceed 80 hours maximum. Extended use of V_{PP} at V_{PP2} might reduce block cycling capability.
VCC	Power	**FLASH POWER SUPPLY:** Supplies power to the flash core.
S-VCC	Power	**SRAM POWER SUPPLY:** Supplies power for SRAM operations.
VSS	Power	**GROUND:** Do not float any VSS connection.
RFU	—	**RESERVED for FUTURE USE:** RFU locations are NC (no connect) on this SCSP product. Contact Intel regarding their future use.
DU	—	**DO NOT USE:** Do not drive, leave disconnected.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Absolute maximum ratings for the 38F1020W0YQ1 devices are shown in Table 2.

Warning: Stressing the device beyond the Absolute Maximum Ratings in Table 2 might cause permanent damage. These are stress ratings only. Extended operation beyond the Operating Conditions in Table 3 might affect device reliability.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Table 2. Absolute Maximum Ratings

Parameter	Maximum Ratings		Unit	Notes
	Min	Max		
Temperature under Bias Expanded	–25	+85	°C	
Storage Temperature	–65	+125	°C	
Voltage On Any Signal (except V_{CC}, V_{CCQ}, V_{PP} and S-V_{CC})	–0.5	+2.45	V	1
V_{CC} Voltage	–0.2	+2.45	V	1
V_{CCQ} and S-V_{CC} Voltage	–0.2	+2.45	V	1
V_{PP} Voltage	–0.2	+14	V	1,2
Output Short Circuit Current	–	100	mA	3

Notes:

1. Specified voltages are with respect to V_{SS}. Minimum DC voltage is –0.5 V on inputs and I/Os, and –0.2 V on V_{CC}, V_{CCQ}, V_{PP} and S-V_{CC} supplies. During transitions, this level might undershoot to –2.0 V for periods < 20 ns. During transitions, the maximum DC voltage level might overshoot to V_{CC} + 2.0 V for periods < 20 ns.
2. V_{PP} program voltage is typically V_{PP1}. Maximum DC voltage on V_{PP} might overshoot to +14 V for periods < 20 ns. V_{PP} can be V_{PP2} for 1000 erase cycles on main blocks, 2500 cycles on parameter blocks.
3. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Table 3. Temperature and Voltage Operating Conditions (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Test Condition
T_A	Operating Temperature	–25	+85	°C	Ambient Temperature
V_{CC}	Flash Memory Supply Voltage	1.7	1.95	V	
V_{CCQ}	Flash Memory I/O Voltage	1.7	1.95	V	

Table 3. Temperature and Voltage Operating Conditions (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{PP1}	Flash Memory Program Logic Level	0.9	1.95	V	
V_{PP2}	Flash Memory Factory Program Voltage	11.4	12.6	V	
S-V_{CC}	SRAM Supply Voltage	1.7	1.95	V	

5.3 Capacitance

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance, Flash Memory Device (CE#1, OE#1, WE#, RST#, WP#, ADV#, CLK, A[20:19])	6	8	pF	V_{IN} = 0.0 V
C_{IN}	Input Capacitance, SRAM (S-CS#1, S-CS2, R-OE#, R-WE#, R-UB#, R-LB#)	10	10	pF	V_{IN} = 0.0 V
C_{IN}	Input Capacitance, Flash Memory and SRAM (A[18:0])	16	18	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance, Flash Memory and SRAM (D[15:0])	18	22	pF	V_{OUT} = 0.0 V
C_{OUT}	Output Capacitance, Flash Memory Device (WAIT)	8	12	pF	V_{OUT} = 0.0 V

Note: Sampled, not 100% tested. T_A = +25 °C, f = 1 MHz.

6.0 Electrical Specifications

6.1 DC Characteristics

Refer to the discrete *W18 Datasheet* for flash DC current parameters and DC voltage information.

Table 4. SRAM DC Characteristics

Parameter	Description	Test Conditions	1.8 V SRAM		Unit
			Min	Max	
V_{CC}	Voltage Range		1.7	1.95	V
V_{DR}	V_{CC} for Data Retention		1.0	–	V
I_{CC}	Operating Current at min cycle time	I_{IO}= 0 mA	–	35	mA
I_{CC2}	Operating Current at max cycle time (1us)	I_{IO}= 0 mA	–	6	mA
I_{SB}	Standby Current	S-CS1#>= S-V_{CC}-0.2V or S-CS2<= V_{ss}+0.2V Address/Data toggling at minimum cycle time	–	20	µA
I_{DR}	Current in Data Retention mode	1.8 V SRAM: S-V_{CC} = 1.0 V	–	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = -100uA	S-V_{CC}- 0.15	–	V
V_{OL}	Output LOW Voltage	I_{OL} = 100uA, V_{CCMIN}	-0.1	0.2	V
V_{IH}	Input HIGH Voltage		S-V_{CC}- 0.4	S-V_{CC}+ 0.2	V
V_{IL}	Input LOW Voltage		-0.2	0.4	V
I_{OH}	Output HIGH Current		–	–	mA
I_{OL}	Output LOW Current		–	–	mA
*I_{IL}	Input Leakage Current	-0.2<Vin<S-V_{CC}+0.2 V	-1	+1	µA
*I_{LDR}	Input Leakage Current in Data Retention Mode	-0.2<Vin<S-V_{CC}+0.2 V S-V_{CC}=V_{DR}	-1	+1	µA

* Input leakage currents include Hi-Z output leakage for bidirectional buffers with tristate outputs.

7.0 AC Characteristics

7.1 Flash Memory Device AC Characteristics

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) for flash memory device AC characteristics details not included in Table 5.

Table 5. Flash Memory Device AC Read Characteristics

Number	Sym	Parameter	W18		Unit
			Min	Max	
	Asynchronous Specifications				
R1	t_{AVAV}	Read Cycle Time	65		ns
R2	t_{AVQV}	Address to Output Delay		65	ns
R3	t_{ELQV}	CE# Low to Output Delay		65	ns
	Latching Specifications				
R108	t_{APA}	Page Address Access Time		25	ns

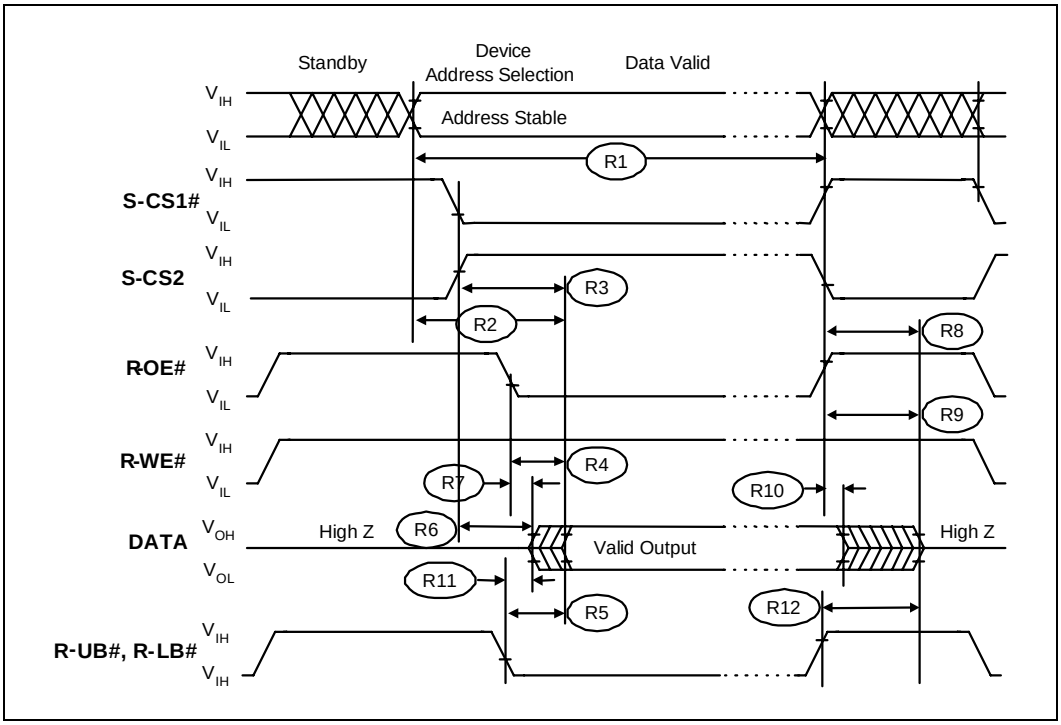
7.2 SRAM AC Characteristics

Number	Symbol	Parameter	Min	Max	Unit	Notes
R1	t_{RC}	Read Cycle Time	70	–	ns	
R2	t_{AA}	Address to Output Delay	–	70	ns	
R3	t_{CO1}	S-CS_1# to Output Delay	–	70	ns	
R3	t_{CO2}	S-CS_2 to Output Delay	–	70	ns	
R4	t_{OE}	R-OE# to Output Delay	–	35	ns	
R5	t_{BA}	R-UB#, R-LB# to Output Delay	–	70	ns	
R6	t_{LZ}	S-CS_1# or S-CS_2 to Output in Low-Z	5	–	ns	1,2
R7	t_{OLZ}	R-OE# to Output in Low-Z	0	–	ns	1
R8	t_{HZ}	S-CS_1# or S-CS_2 to Output in High-Z	0	25	ns	1,2,3
R9	t_{OHZ}	R-OE# to Output in High-Z	0	25	ns	1,3
R10	t_{OH}	Output Hold (from Address, S-CS_1#, S-CS_2, or R-OE# Change, whichever Occurs First)	0	–	ns	

Number	Symbol	Parameter	Min	Max	Unit	Notes
R11	t_{BLZ}	R-UB#, R-LB# to Output in Low-Z	0	–	ns	1
R12	t_{BHZ}	R-UB#, R-LB# to Output in High-Z	0	25	ns	1

Notes:
1. Sampled, not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Max) for a given device and from device-to-device interconnection.
3. Timings of t_{HZ} and t_{OHZ} are when the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 4. SRAM Read Waveform



Number	Symbol	Parameter	Min	Max	Unit	Notes
W1	t_{WC}	Write Cycle Time	70	–	ns	1
W2	t_{AS}	Address Setup to R-WE# (S-CS_1#) and R-UB#,R-LB# Going Low	0	–	ns	3
W3	t_{WP}	R-WE# (S-CS_1#) Pulse Width	55	–	ns	1
W4	t_{DW}	Data to Write Time Overlap	30	–	ns	
W5	t_{AW}	Address Setup to R-WE# (S-CS_1#) Going High	60	–	ns	
W6	t_{CW}	S-CS1# (R-WE#) Setup to R-WE# (S-CS_1#) Going High	60	–	ns	2
W7	t_{DH}	Data Hold from R-WE# (S-CS_1#) High	0	–	ns	

Number	Symbol	Parameter	Min	Max	Unit	Notes
W8	t_{WR}	Write Recovery	0	–	ns	4
W9	t_{BW}	R-UB#, R-LB# Setup to R-WE# (S-CS_1#) Going High	60	–	ns	

Notes:

1. A write occurs during the S-CS_1# and R-WE# asserted overlap (t_{WP}).
   – The write begins with the latest transition of S-CS_1# and R-WE# going low (R-UB# and/or R-LB# already asserted).
   – The write ends at the earliest transition of S-CS_1# or R-WE# goes high.
2. t_{CW} is measured from S-CS_1# going low to the end of a write.
3. t_{AS} is measured from address valid to the beginning of a write.
4. t_{WR} is measured from the end of a write to the address change; t_{WR} applied if a write ends as S-CS_1# or R-WE# goes high.

Figure 5. SRAM Write Waveform

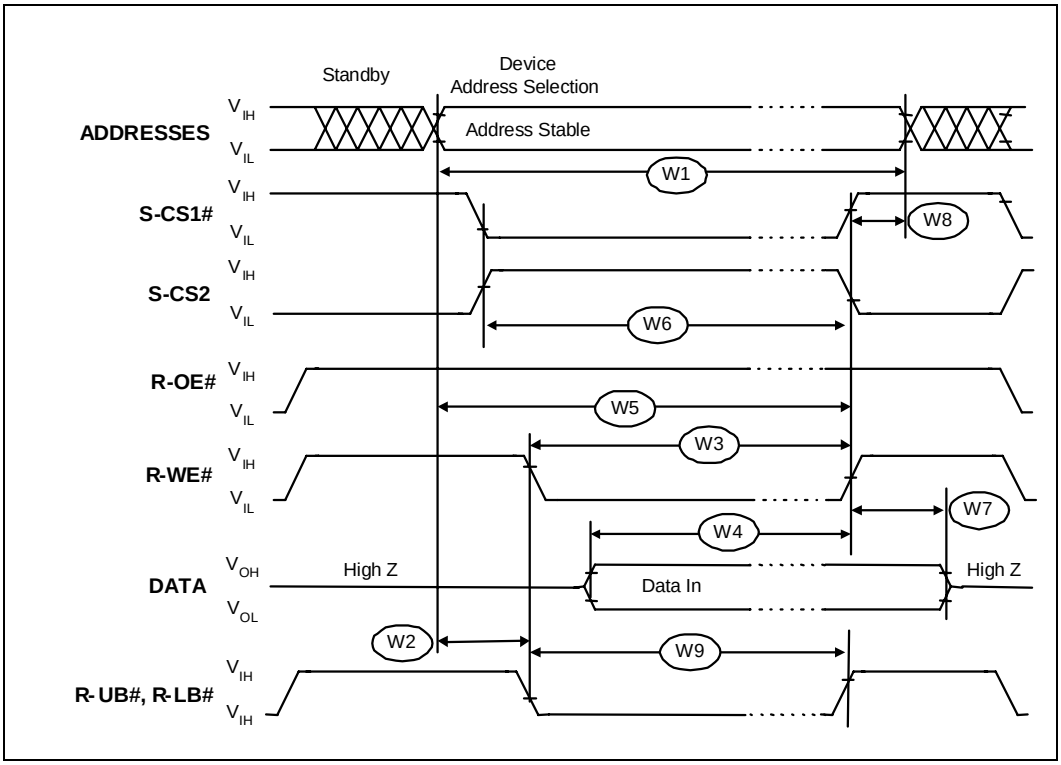


Figure 6. SRAM Data Retention Waveform (S-CS1# Controlled)

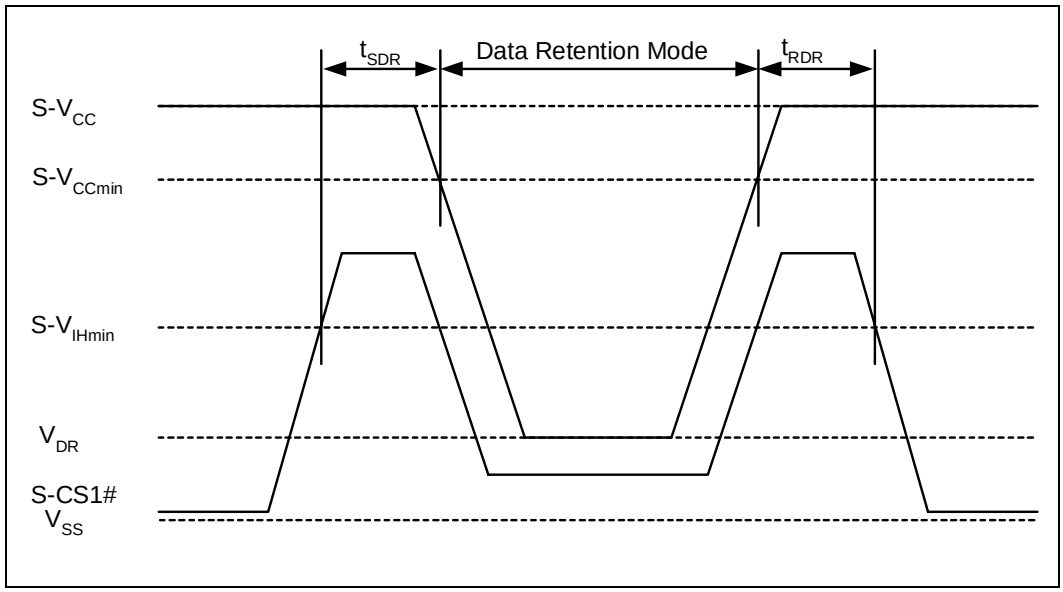
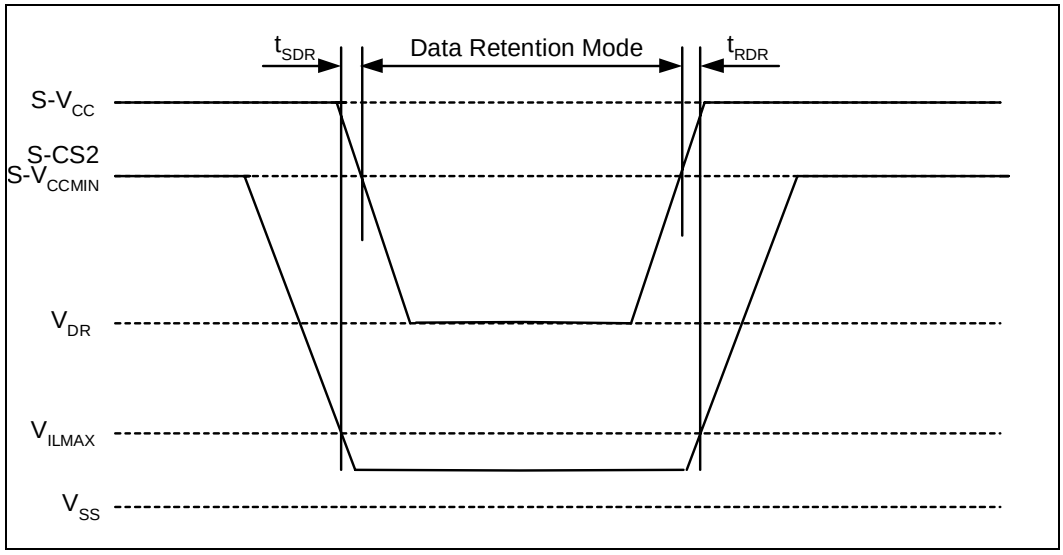


Figure 7. SRAM Data Retention Waveform (S-CS2 Controlled)



8.0 Power and Reset Specifications

For detailed information about power and reset, refer to the *Intel® Wireless Flash Memory (W18) Datasheet*.

9.0 Device Operation

Bus operations for the 38F1020W0YQ1 devices involve the control of the flash and SRAM inputs. The chip enable (CE#1) and output enable (OE#1) control the flash memory device.

Table 6 shows the flash memory and SRAM bus operations.

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* for complete descriptions of flash memory modes and commands, and for command bus-cycle definitions and flowcharts for operational routines.

Table 6. Bus Operations

Device	Mode	RST#	CE#1	OE#1	WE#	VPP	WAIT	S-CS1#	S-CS2	R-OE#	R-WE#	R-UB#, R-LB#	D[15:0]	Notes
Flash Memory	Read	H	L	L	H	X	Valid/ Driven	SRAM must be in High-Z					Flash Memory D_{OUT}	1,2,3,5,6
	Write	H	L	H	L	V_{PP1} or V_{PP2}	Driven						Flash Memory D_{IN}	3,4,7
	Output Disable	H	L	H	H	X	Driven	Any SRAM mode allowed					Flash Memory High-Z	5
	Standby	H	H	X	X	X	High-Z						Flash Memory High-Z	5
	Reset	L	X	X	X	X	High-Z						Flash Memory High-Z	5
SRAM	Read	Flash device must be in High-Z					Note 2	L	H	L	H	L	SRAM D_{OUT}	1,4
	Write						Note 2	L	H	H	L	L	SRAM D_{IN}	4
	Output Disable	Any flash device mode allowed					Note 2	L	H	H	H	X	SRAM High-Z	5
	Standby						Note 2	H / X	X / L	X	X	X	SRAM High-Z	5,8
	Data Retention						Note 2	Same as SRAM standby					SRAM High-Z	9

Notes:

1. For asynchronous read operation, both die can be simultaneously selected, but both die cannot simultaneously drive the memory bus. For synchronous burst-mode reads, both die can be simultaneously selected.
2. WAIT is valid during synchronous flash memory reads. WAIT is driven if CE#1 is asserted.
3. Do not simultaneously assert OE#1 and WE#.
4. For SRAM, do not simultaneously assert R-OE#1 and R-WE#.
5. X can be V_{IL} or V_{IH} for inputs, V_{PP1}, V_{PP2} or V_{PPLK} for V_{PP}.
6. Flash CFI query and status register accesses use D[7:0] only; all other reads use D[15:0].
7. Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* for valid D_{IN} during flash memory writes.
8. The SRAM is enabled or disabled using the following logical function: S-CS1# OR S-CS2.
9. To place the SRAM into data retention mode, lower S-VCC to the V_{DR} limit when in standby mode.

10.0 Flash Memory Read Operations

For detailed information about reads from the flash memory device, refer to the *Intel® Wireless Flash Memory (W18) Datasheet*.

11.0 Flash Memory Program Operations

For detailed information about programming flash memory, refer to the *Intel® Wireless Flash Memory (W18) Datasheet*.

12.0 Flash Memory Program and Erase Operations

For detailed information about erasing flash memory, refer to the *Intel® Wireless Flash Memory (W18) Datasheet.*

13.0 Flash Memory Security Modes

For detailed information about flash memory security modes, refer to the *Intel® Wireless Flash Memory (W18) Datasheet*.

14.0 Flash Memory Set Configuration Register

For detailed information about the set configuration register, refer to the *Intel® Wireless Flash Memory (W18) Datasheet*.

Appendix A Write State Machine

For detailed information about the Write State Machine on flash memory devices, refer to the *Intel® Wireless Flash Memory (W18) Datasheet*.

Appendix B Common Flash Interface

For detailed information about the Common Flash Interface (CFI), refer to the *Intel® Wireless Flash Memory (W18) Datasheet*.

Appendix C Additional Information

Order Number	Document
290701	*Intel® Wireless Flash Memory (W18) Datasheet*
298289	*Intel® Wireless Flash Memory (W18) Specification Update*

Notes:

1. Call the Intel Literature Center at (800) 548-4725 to request Intel documentation. For international customers , contact your local Intel or distribution sales office.
2. For current information about Intel® Flash memory products, software, and tools, visit our website at http://developer.intel.com/design/flash.

Appendix D Ordering Information

Figure 8. Ordering Information