

MNLM613AM-X REV 2B0

 Original Creation Date: 08/02/95
 Last Update Date: 03/12/02
 Last Major Revision Date: 10/23/01

QUAD OPERATIONAL AMPLIFIERS AND ADJUSTABLE REFERENCE
General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps make the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1 ohm typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Industry Part Number

LM613

NS Part Numbers

LM613AMJ/883

Prime Die

LM613

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

CONTROLLING DOCUMENT:

LM613AMJ/883 5962-9300301MEA

(Absolute Maximum Ratings)

(Note 1)

Voltage on Any Pin Except VR (Referred to V ⁻ pin) (Note 2) (Note 3)	36V (Max) -0.3V (Min)
Current through Any input Pin	± 20 mA
Differential Input Voltage	± 36V
Storage Temperature Range	-65C ≤ Ta ≤ +150
Operating Temperature Range	-55C ≤ Ta ≤ + 125
Maximum Junction Temperature	150 C
Thermal Resistance, Junction- (Note 4) J Pkg (Cerdip)	TBD
ESD Tolerance (Note 5)	± 1kV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Input voltage above V⁺ is not allowed. As long as one input pin voltage remain inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V⁻, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{jmax} (maximum junction temperature), Theta_{JA} (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is P_{dmax} = (T_{jmax} - TA) / Theta_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 5: Human body model, 100pF discharged through 1.5K Ohms.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V^- = \text{Gnd} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{cm}} = V_{\text{out}} = V^+ / 2$, $I_{\text{r}} = 100\mu\text{A}$, FEEDBACK PIN TO GND.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I _{cc}	Total Supply Current	R _{load} = Infinity, 4V ≤ V ₊ ≤ 36V				940	μA	1
						1000	μA	2, 3
V _s	Supply Voltage Range				2.8	36	V	1
					3	36	V	2, 3

DC PARAMETERS: Operational Amplifier

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V^- = \text{Gnd} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{cm}} = V_{\text{out}} = V^+ / 2$, $I_{\text{r}} = 100\mu\text{A}$, FEEDBACK PIN TO GND.

V _{io1}	Offset Voltage Over V ₊ Range	4V ≤ V ₊ ≤ 36V			-3.5	3.5	mV	1
						-6.0	6.0	mV
V _{io2}	Offset Voltage Over V _{cm} Range	V _{cm} = 0V through V _{cm} = (V ₊ - 1.4V), V ₊ = 30V			-3.5	3.5	mV	1
		V _{cm} = 0V through V _{cm} = (V ₊ - 1.8V), V ₊ = 30V			-6.0	6.0	mV	2, 3
I _{ib}	Input Bias Current				-25	25	nA	1
						-30	30	nA
I _{io}	Input Offset Current				-4	4	nA	1
						-5	5	nA
CMRR	Common-Mode Rejection Ratio	V ₊ = 30V, CMRR = 20log(ΔV _{cm} /ΔV _{io}), 0V ≤ V _{cm} ≤ (V ₊ - 1.4V)			80		dB	1
		V ₊ = 30V, CMRR = 20log(ΔV _{cm} /ΔV _{io}), 0V ≤ V _{cm} ≤ (V ₊ - 1.8V)				75	dB	2, 3
PSRR	Power Supply Rejection Ratio	PSRR = 20log(ΔV ₊ /ΔV _{io}), 4V ≤ V ₊ ≤ 30V, V _{cm} = V ₊ /2			80		dB	1
						75	dB	2, 3
I _{out}	Output Source Current	V _{out} = V ₊ - 2.5V, V _{in} = 0V, V _{-in} = -0.3V			20		mA	1
						13	mA	2, 3
I _{sink}	Output Sink Current	V _{out} = 1.6V, V _{in} = 0V, V _{-in} = 0.3V			14		mA	1
						8	mA	2, 3
I _{short}	Short Circuit Current	V _{out} = 0V, V _{in} = 3V, V _{-in} = 2V Source				50	mA	1
						60	mA	2, 3
		V _{out} = 5V, V _{in} = 2V, V _{-in} = 3V Sink				60	mA	1
						80	mA	2, 3

Electrical Characteristics

DC PARAMETERS: Voltage Reference

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: $V^- = Gnd = 0V$, $V^+ = 5V$, $V_{cm} = V_{out} = V^+/2$, $I_r = 100\mu A$, FEEDBACK PIN TO GND.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
V_r	Voltage Reference		1		1.2365	1.2515	V	1
Delta $V_r/\Delta I_r$	Vr Change with Current	$V_r(100\mu A) - V_r(17\mu A)$			-1	1	mV	1
					-1.1	1.1	mV	2, 3
		$V_r(10mA) - V_r(100\mu A)$	2		-5	5	mV	1
			2		-5.5	5.5	mV	2, 3
R	Resistance	$\Delta V_r(10mA \text{ to } 100\mu A)/9.9mA$	3			0.51	Ohms	1
			3			0.56	Ohms	2, 3
		$\Delta V_r(100\mu A \text{ to } 17\mu A)/84\mu A$	3			12	Ohms	1
			3			13	Ohms	2, 3
Delta $V_r/\Delta V_{ro}$	Vr Change with High V_{ro}	$V_r(V_{ro}=V_r) - V_r(V_{ro}=5.0V)$, (3.76V between Anode and FEEDBACK)				7	mV	1
						10	mV	2, 3
Delta $V_r/\Delta V^+$	Vr Change with V^+ Change	$V_r(V^+=5V) - V_r(V^+=36V)$			-1.2	1.2	mV	1
					-1.3	1.3	mV	2, 3
		$V_r(V^+=5V) - V_r(V^+=3V)$			-1	1	mV	1
					-1.5	1.5	mV	2, 3
$I_b(fb)$	Feedback Bias Current	$V_{anode} \leq V_{fb} \leq 3.76V$				35	nA	1
						40	nA	2, 3

Electrical Characteristics

DC PARAMETERS: Comparators

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V^- = \text{Gnd} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{cm}} = V_{\text{out}} = V^+/2$, $I_{\text{r}} = 100\mu\text{A}$, FEEDBACK PIN TO GND.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio1	Offset Voltage Over V^+ Range	$4\text{V} \leq V^+ \leq 36\text{V}$, $R_{\text{l}} = 15\text{K Ohms}$			-3.0	3.0	mV	1
					-6.0	6.0	mV	2, 3
Vio2	Offset Voltage Over V_{cm} Range	$0\text{V} \leq V_{\text{cm}} \leq (V^+ - 1.4\text{V})$, $1.0\text{V} \leq V_{\text{cm}} \leq (V^+ - 1.8\text{V})$ over Temp., $V^+ = 30\text{V}$, $R_{\text{l}} = 15\text{K Ohms}$			-3.0	3.0	mV	1
					-6.0	6.0	mV	2, 3
Iib	Input Bias Current				-25	25	nA	1
					-30	30	nA	2, 3
Iio	Input Offset Current				-4	4	nA	1
					-5	5	nA	2, 3
Isink	Output Sink Current	$V^+_{\text{in}} = 0\text{V}$, $V_{\text{out}} = 1.5\text{V}$			10		mA	1
					8		mA	2, 3
		$V^-_{\text{in}} = 1\text{V}$, $V_{\text{out}} = 0.4\text{V}$			1.0		mA	1
					0.5		mA	2, 3
Ileak	Output Leakage Current	$V^+_{\text{in}} = 1\text{V}$, $V^-_{\text{in}} = 0\text{V}$, $V_{\text{out}} = 36\text{V}$				10	μA	1

DC PARAMETERS: Operational Amplifiers

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V^- = \text{Gnd} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{cm}} = V_{\text{out}} = V^+/2$, $I_{\text{r}} = 100\mu\text{A}$, FEEDBACK PIN TO GND.

Vo1	Output Voltage Swing High	$R_{\text{l}} = 10\text{K Ohms to Gnd}$, $V^+ = 36\text{V}$			$V^+ - 1.7$		V	4
					$V^+ - 1.9$		V	5, 6
Vo2	Output Voltage Swing Low	$R_{\text{l}} = 10\text{K Ohms to } V^+$, $V^+ = 36\text{V}$				$V^- + 0.9$	V	4
						$V^- + 1.2$	V	5, 6
Av	Open Loop Voltage Gain	$R_{\text{l}} = 10\text{K Ohms to Gnd}$, $V^+ = 30\text{V}$, $5\text{V} \leq V_{\text{out}} \leq 25\text{V}$			100		V/mV	4
					40		V/mV	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: $V^- = \text{Gnd} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{cm}} = V_{\text{out}} = V^+/2$, $I_{\text{r}} = 100\mu\text{A}$, FEEDBACK PIN TO GND.

Sr	Slew Rate	$V^+ = 30$	4		0.55		V/ μS	7
			4		0.45		V/ μS	8A, 8B

Note 1: V_{ro} is the reference output voltage, which may be set for 1.2V to 5.0V. V_{r} is the V_{ro} to Feedback voltage (nominally 1.244V).

Note 2: Low contact resistance is required for accurate measurement.

Note 3: Guaranteed by V_{r} change with current.

(Continued)

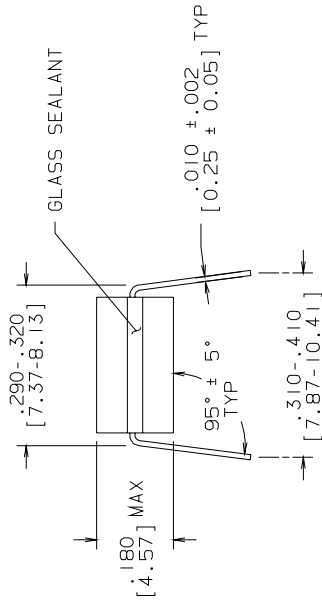
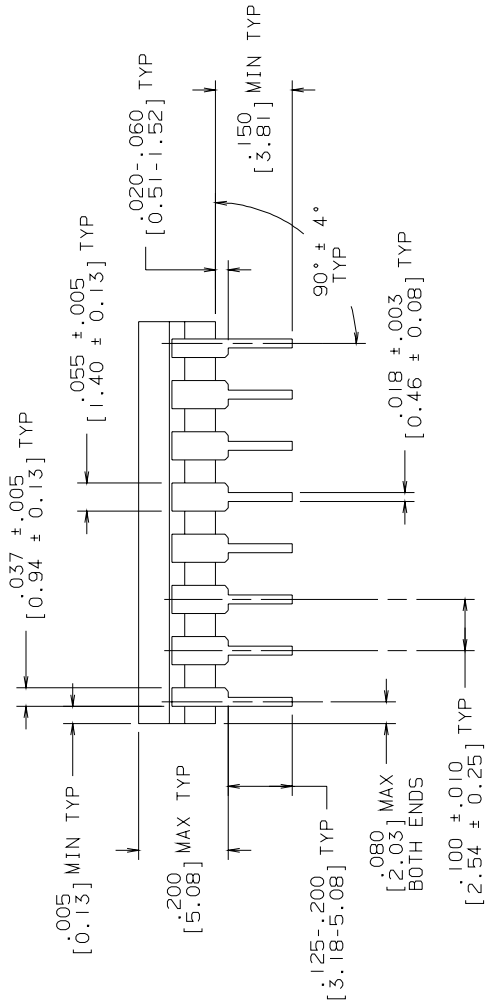
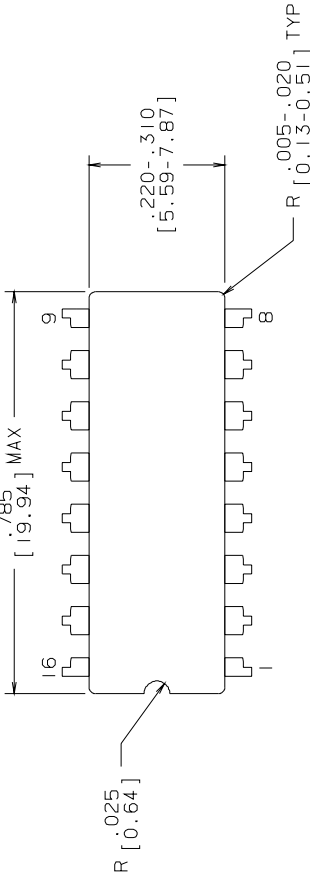
Note 4: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Graphics and Diagrams


GRAPHICS#	DESCRIPTION
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)

See attached graphics following this page.

R E V I S I O N S			
LTR	DESCRIPTION	E. C. N.	DATE
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93
			TL/



MILIAERO CONFIGURATION CONTROL MIL-M-38510
 CONFIGURATION CONTROL CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH	
APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	
PROJECTION 	
	INCH [MM]
SCALE N/A	SIZE B
DRAWING NUMBER MKT-J16A	REV L
DO NOT SCALE DRAWING	SHEET 1 OF 1

NATIONAL SEMICONDUCTOR CORPORATION
 2900 Semiconductor Drive, Santa Clara, CA 95052-8090
 CERDIP (J),
 16 LEAD

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
 - JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0BL	M0001700	08/18/99	Barbara Lopez	Changed: MNL613AM-X Rev. 0AL to MNL613AM-X Rev. 0BL.
1AL	M0003389	11/20/01	Rose Malone	Update MDS: MNL613AM-X, Rev. 0BL to MNL613AM-X, Rev. 1AL. Changed conditions for: Delta Vr/Delta Vro From Vr(Vro=Vr)-Vr(Vro=6.3V), (5.06V between Anode and FEEDBACK) To Vr(Vro=Vr)-Vr(Vro=5.0V), (3.76V between Anode and FEEDBACK), Ib(If) From Ifb; Vanode <= Vfb <= 5.06V To Ifb; Vanode <= Vfb <= 3.76V, and Note 1.
2A0	M0003949	03/12/02	Rose Malone	Update MDS: MNL613AM-X, Rev. 1AL to Fully Released MDS: MNL613AM-X, Rev. 2A0. Updated Main Table, Absolute Maximum Ratings Section, DC Parameters: Operational Amplifiers Electrical Section Parameter Vo2 Subgroup 5, 6 from V- +1.0V to V- +1.2V and Graphics Section.
2B0	M0003976	03/12/02	Rose Malone	Update MDS: MNL613AM-X, Rev. 2A0 to MNL613AM-X, Rev. 2B0. Corrected Typo in Note 5 for Absolute Maximum Ratings Section.