National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC114A-X REV 0A0

Original Creation Date: 08/03/98
Last Update Date: 01/12/99
Last Major Revision Date: 08/03/98

QUAD, LOW-POWER VIDEO BUFFER

General Description

The CLC114 is a high-performance, closed-loop quad buffer intended for power sensitive applications. Requiring only 30mW of quiescent power dissipation per channel (±5V supplies), the CLC114 offers a small signal bandwidth of 200MHz (0.5Vpp) and a slew rate of 450V/uS.

Designed specifically for high density crosspoint switch and analog multiplexer applications, the CLC114 offers excellent linearity and wide channel isolation (62dB @ 10MHz). Driving a typical crosspoint switch load, the CLC114 offers differential gain and phase performance of 0.08% and 0.1%; gain flatness through 30MHz is typically 0.1dB.

With its patented closed-loop topology, the CLC114 has significant performance advantages over conventional open-loop designs. Applications requiring low output impedance and true unity gain stability through very high frequencies (active filters, dynamic load buffering, etc.) will benefit from the CLC114's superior performance.

Industry Part Number

CLC114A

NS Part Numbers

CLC114AE-QML *
CLC114AJ-MLS
CLC114AJ-QML **

Prime Die

UB1417A

Controlling Document

5962-9233901MCA**, M2A*

Processing

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Quality Conformance Inspection

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Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Closed-loop, quad buffer
- 200MHz small-signal bandwidth
- 450V/uS slew rate
- Low power, 30mW per channel (±5V sup.)
- 62dB channel isolation (10MHz)
- Specified for crosspoint switch loads

Applications

- Video crosspoint switch driver
- Video disribution buffers
- Video switching buffers
- Video signaling multiplexing
- Instrumentation amps
- Active filters

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vs)	±7V dc
Output Current (Iout)	35 mA
Power Dissipation (Pd) (Note 2)	1.2W
Lead Temperature (soldering, 10 seconds)	+300 C
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150 C
Thermal Resistance	
Junction-to-ambient (ThetaJA)	
Ceramic DIP (Still Air)	97 C/W
Ceramic DIP (500 LFPM)	59 C/W
LCC (Still Air)	TBD
LCC (500 LFPM)	TBD
Junction-to-case (ThetaJC)	
Ceramic DIP	20 C/W
LCC	TBD
Package Weight (Typical)	
Ceramic DIP	2160 mg
LCC	TBD
ESD Tolerance (Note 3)	2200V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5V dc
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +1, and load resistance (Rl) = 100 Ohms. -55 C ≤ Ta ≤ +125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iin	Input Bias Current				-5	+5	uA	1
					-4	+4	uA	2
					-10	+10	uA	3
Voo	Output Offset Voltage	Rs = 50 Ohms			-5.0	+5.0	mV	1
					-8.0	+8.0	mV	2
					-8.2	+8.2	mV	3
Tc (Iin)	Average Input Bias Current Drift		1		-25	+25	nA/C	2
			1		-62	+62	nA/C	3
Tc (Vio)	Average Offset Voltage Drift		1		-30	+30	uV/C	2
			1		-40	+40	uV/C	3
Is	Total Supply Current	No Load				16.5	mA	1
						16.0	mA	2
						17.0	mA	3
+Rin	Input Resistance		1		1.0		MOhms	1
			1		2.0		MOhms	2
			1		0.3		MOhms	3
Iout	Output Current		1		25		mA	1
			1		20		mA	2
			1		12		mA	3
PSRR	Power Supply Rejection Ratio	+Vs = +4.5V to +5.0V, -Vs = -4.5V to -5.0V			48		dB	1, 3
					46		dB	2
SSBW	Small Signal Bandwidth	-3dB bandwidth, Vout < 0.5Vpp			135		MHz	4
			3		120		MHz	5
			3		135		MHz	6
LSBW	Large Signal Bandwidth	-3dB bandwidth, Vout < 2.0Vpp	1		70		MHz	4, 5, 6
GFPL	Gain Flatness Peaking Low	At 0.1MHz to 30MHz, Vout < 0.5Vpp				0.2	dB	4
			3			0.3	dB	5, 6
GFPH	Gain Flatness Peaking High	30MHz to 200MHz, Vout < 0.5Vpp				0.4	dB	4
			3			0.7	dB	5
			3			1.3	dB	6

Electrical Characteristics

PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +1, and load resistance (Rl) = 100 Ohms. -55 C ≤ Ta ≤ +125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
GFR	Gain Flatness Rolloff	0.1MHz to 60 MHz, Vout < 0.5Vpp				0.8	dB	4
			3			1.0	dB	5
			3			0.8	dB	6
HD2	2nd Harmonic Distortion	2 Vpp at 20 MHz				-38	dBc	4
			3			-38	dBc	5
			3			-36	dBc	6
HD3	3rd Harmonic Distortion	2 Vpp at 20 MHz				-50	dBc	4
			3			-45	dBc	5
			3			-50	dBc	6
SNF	Input Noise Floor	At > 1 MHz	1			-153	dBm 1Hz	4, 5, 6
GA	Small Signal Gain	Rl = 100Ohms	1		0.96		V/V	4, 5
			1		0.95		V/V	6
ILIN	Integral Endpoint Linearity	At ±1V, full scale	1			0.6	%	4
		At ±1V, full scale	1			0.5	%	5
		At ±1V, full scale	1			1.0	%	6
XT	Crosstalk	At 10MHz	1, 2		58		dB	4, 6
			1, 2		60		dB	5
+Vout	Output Voltage Swing	Rl = 100Ohms	1		+1.8		V	4, 5
			1		+1.0		V	6
-Vout	Output Voltage Swing	Rl = 100Ohms	1			-1.8	V	4, 5
			1			-1.0	V	6
Cin	Input Capacitance		1			3.0	pF	4
			1			3.5	pF	5, 6
Ro	Output Impedance	dc	1			3.5	Ohms	1, 2
			1			5.0	Ohms	3
SR	Slew Rate	Measured ±1V with ±4V Step	1		200		V/uS	9
		Measured ±1V with ±4V Step	1		180		V/uS	10, 11
TRS	Rise and Fall Time	0.5V Step	1			2.8	nS	9, 11
			1			3.0	nS	10

Electrical Characteristics

PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +1, and load resistance (Rl) = 100 Ohms. -55 C ≤ Ta ≤ +125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TRL	Rise and Fall Time	2V Step	1			7.0	nS	9, 11
			1			8.0	nS	10
Ts	Settling Time	2V Step at 0.1% of the fixed value	1			15	nS	9, 11
			1			20	nS	10
		2V Step at 0.01% of the fixed value	1			30	nS	9, 11
			1			40	nS	10
OS	Overshoot	0.5V Step	1			10	%	9
			1			15	%	10, 11

DC: PARAMETERS: DRIFT LIMITS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +1. "Deltas not required on B-level product. Deltas required for S-level (-MLS) product as specified on Internal Processing Instructions (IPI)." (Note 4)

Iin	Input Bias Current				-0.5	+0.5	uA	1
Is	Total Supply Current	No Load			-0.5	+0.5	mA	1
Voo	Output Offset Voltage	Rs = 50 Ohms			-0.25	+0.25	mV	1

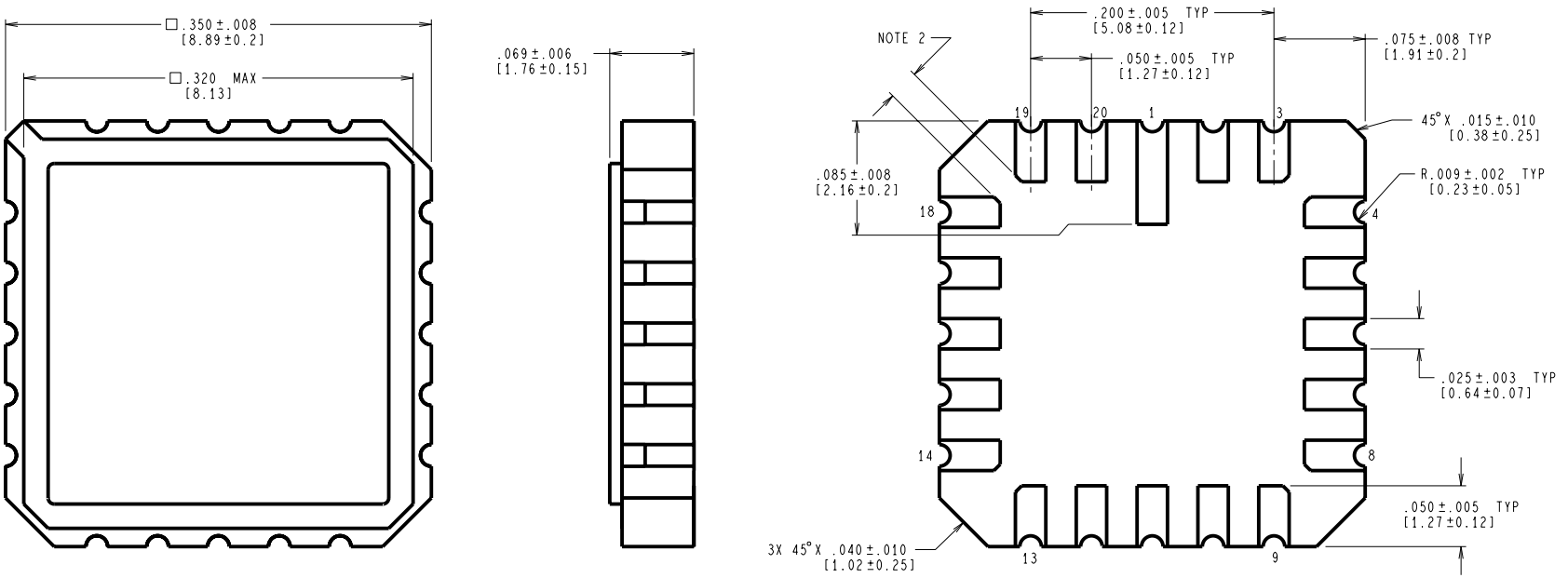
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Three channels are driven simultaneously while observing the output of the undriven fourth channel.
Note 3: Group A sample tested only.
Note 4: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06375HRA1	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
07084HRA2	CERDIP (J), 14 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000402A	CERDIP (J),14 LEAD (PINOUT)
P000447A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

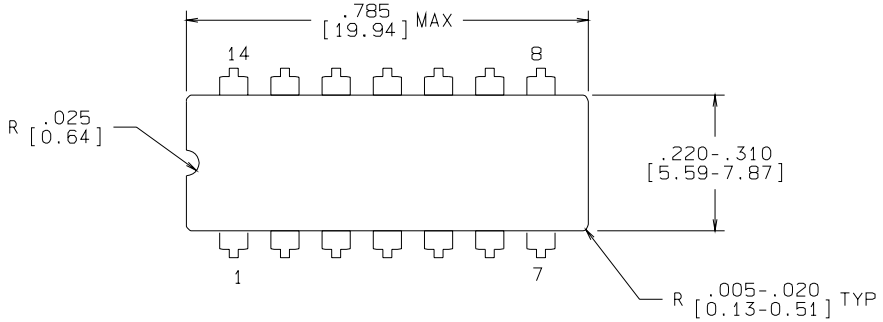
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

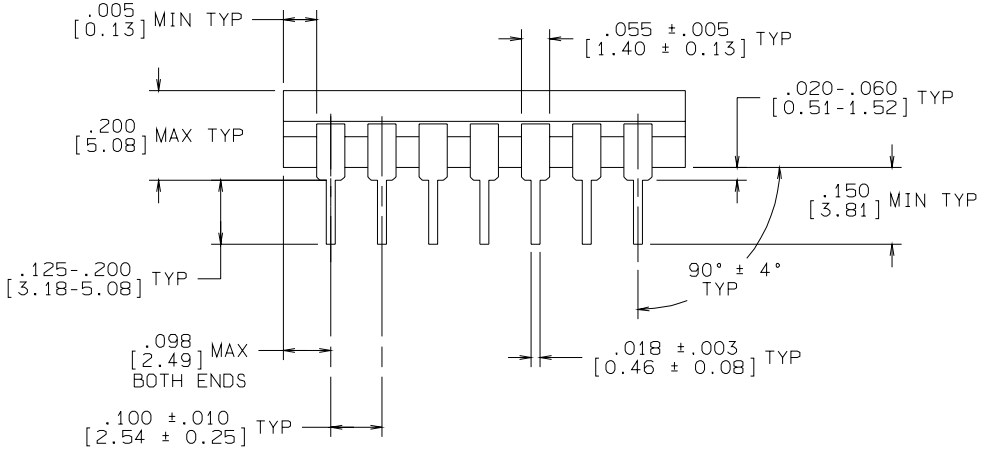
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

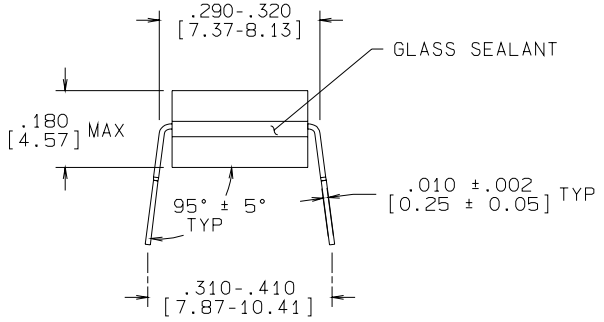
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

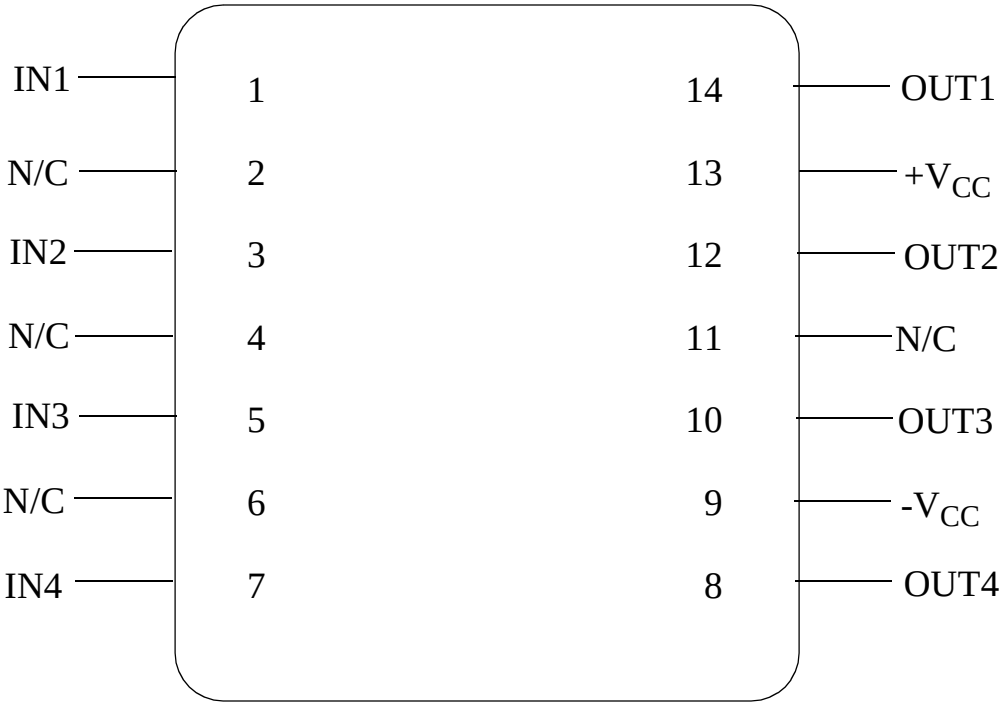
INCH [MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

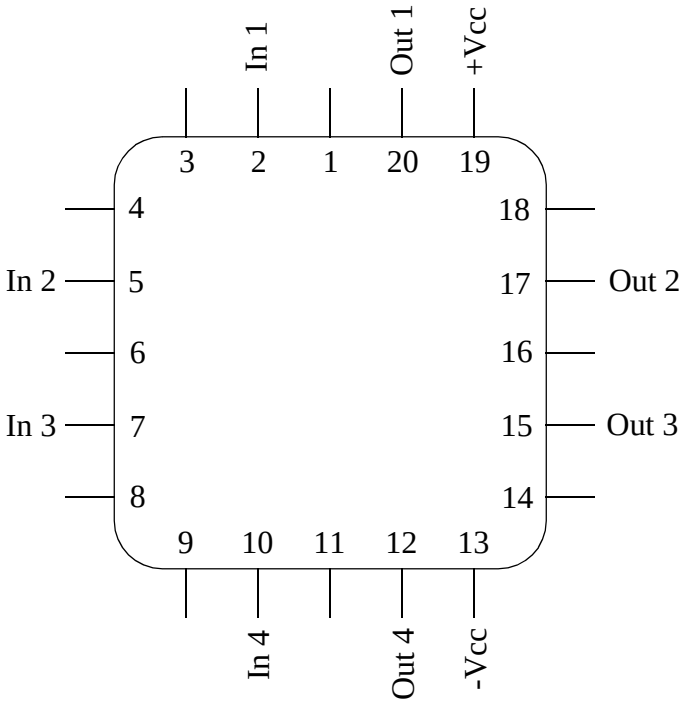
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC114J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000402A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



CLC114E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000447A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003193	01/12/99	Shaw Mead	Initial MDS Release