SC4210A
8-Pin N-FET Linear Regulator Controller

POWER MANAGEMENT

Description

The SC4210A linear regulator controller includes all the features required for an extremely low dropout linear regulator that uses an external N-channel MOSFET as the pass transistor. The device can operate from input voltages as low as 1.75V and can provide high current levels, thus providing an efficient linear solution for custom processor voltages, bus termination voltages, and other logic level voltages down to 0.5V. The onboard charge pump creates a gate drive voltage capable of driving an external N-MOSFET which is optimal for low dropout voltage and high efficiency. The wide versatility of this IC allows the user to optimize the setting of both current limit and output voltage for applications beyond or between standard 3-terminal linear regulator ranges.

The 8-pin controller IC features a duty ratio current limiting technique that provides peak transient loading capability while limiting the average power dissipation of the pass transistor during fault conditions.

The SC4210A is available in an MSOP-8 surface mount package.

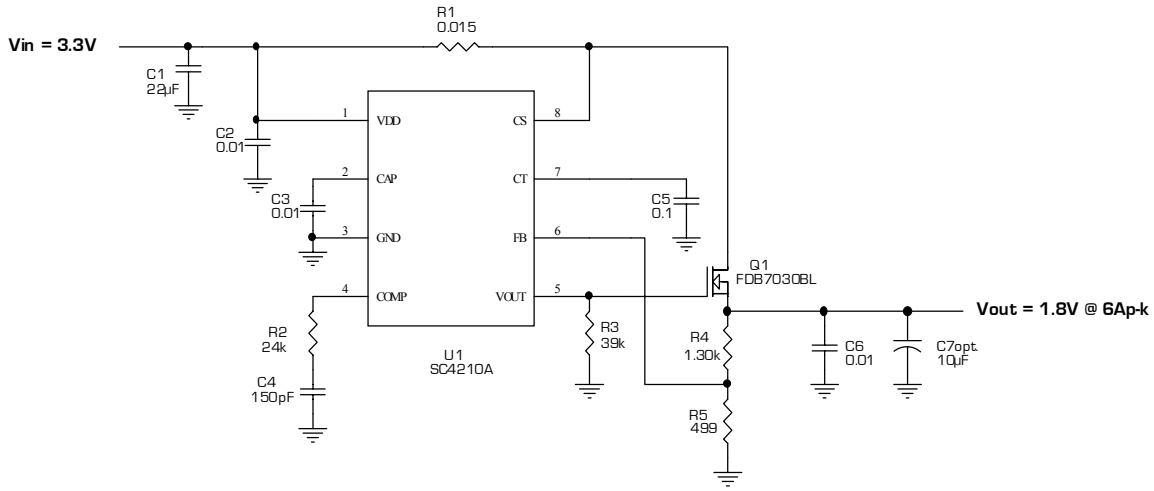
Features

- On-board charge pump to drive external N-MOSFET
- Input voltage as low as 1.75V to 5.5V
- Duty ratio mode over-current protection
- Extremely low dropout voltage
- Low external parts count
- Output voltages as low as 0.5V
- MSOP-8 package

Applications

- Telecom and networking cards
- Industrial applications
- Wireless infrastructure
- Set-top boxes
- Post regulated power supplies

Typical Application Circuit



POWER MANAGEMENT

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Limits	Units
CAP, COMP, VOUT		-0.3 to +12	V
CT, FB, VDD, CS		-0.3 to +6	V
Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C
Thermal Impedance Junction to Ambient	θ_{JA}	207	°C/W

Electrical Characteristics

Unless specified: $T_J = T_A$ = -40 to 125°C, VDD = 1.8V to 5V, C_T = 10nF, C_{CAP} = 100nF.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply						
Supply Current		VDD = 5V		2.0	2.8	mA
Under Voltage Lockout						
Minimum Voltage to Start				1.728	1.764	V
Hysteresis				90		mV
Reference						
V_{REF}		VDD = 3.3V, T_J = 25°C	495	500	505	mV
		VDD = 3.3V, T_J = -40°C to +125°C	488		512	mV
Current Sense						
Comparator Threshold				100		mV
Amplifier Threshold				140		mV
Input Bias Current				0.5	0.8	µA

Electrical Characteristics

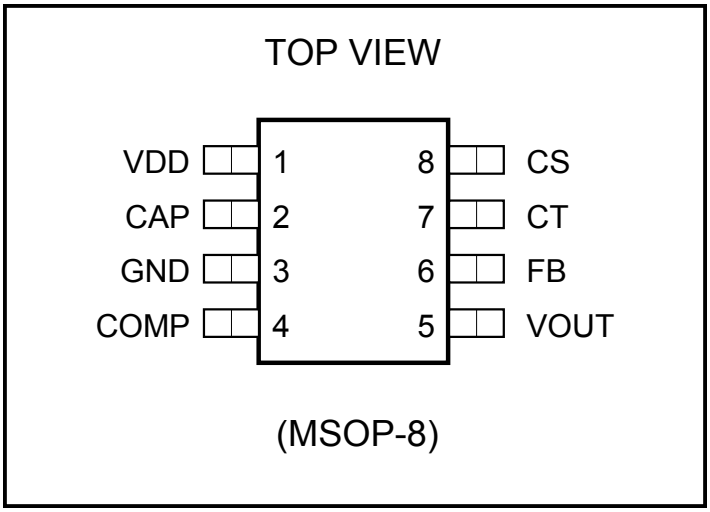
Unless specified: $T_J = T_A$ = -40 to 125°C, VDD = 1.8V to 5V, C_T = 10nF, C_{CAP} = 100nF.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Fault Timer						
CT Charge Current		VCT = 1V, VDD = 5V	20	40	60	µA
CT Discharge Current		VCT = 1V, VDD = 5V	0.8	1.7	3.0	µA
CT Fault Low Threshold				0.3		V
CT Fault High Threshold				1.3		V
Fault Duty Cycle			2.8	4	5.2	%
Error Amplifier						
Input Bias Current				0.2	0.5	µA
Open Loop Gain				66		dB
Transconductance		-10µA to 10µA, VDD = 5V	0.6	0.8		mS
Output Impedance				2.6		MΩ
Unity Gain Crossover	GBW			5		MHz
Source Current		VDD = 5V	30	55		µA
Sink Current		VDD = 5V	20	45		µA
FET Driver						
Peak Output Current		V_{CAP} = 10V, VOUT = 1V	0.7	2		mA
Average Output Current		VOUT = 1V, VDD = 5V	200	330		µA
Max Output Voltage		VDD = 4.5V, I_{CAP} = 10µA	8	8.4		V
Charge Pump						
CAP Voltage		VDD = 4.5V, CS = 0V	8.5	9.4		

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

POWER MANAGEMENT

Pin Configuration



Ordering Information

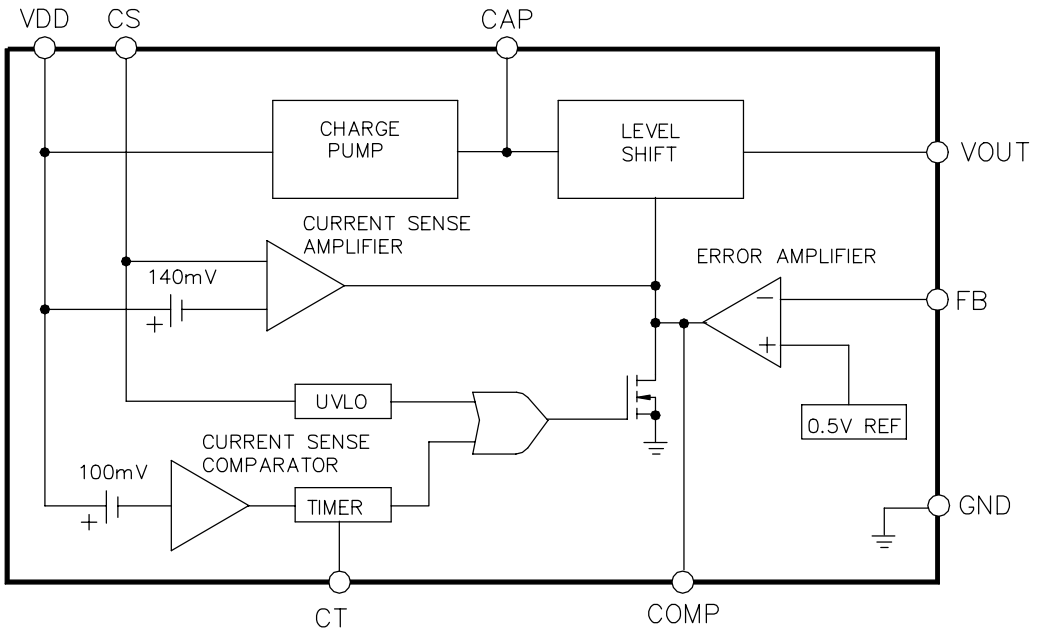
Part Number (1)	Package
SC4210AIMSTRT(2)	MSOP-8
SC4210AEVB	EVALUATION BOARD

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin	Pin Name	Pin Function
1	VDD	The system input voltage is connected to this point. VDD must be above 1.75V. VDD also acts as one side of the current sense amplifier and comparator.
2	CAP	The output of the charge pump circuit. A capacitor is connected between this pin and GND to provide a floating bias voltage for an N-Channel MOSFET gate drive. A minimum of a 0.01µF ceramic capacitor is recommended. CAP can be directly connected to an external regulated source, in which case the external voltage will be the source for driving the N-Channel MOSFET.
3	GND	Ground reference for device.
4	COMP	The common output of the transconductance error amplifier and current sense amplifier. It is used for compensating the small signal characteristics of the voltage and current loop (when the current sense amplifier is active in over-current mode). Also, it can be utilized as an ON/OFF node; if pulled to GND the circuit will shutdown; if left floating, it will enable normal operation.
5	VOUT	This pin directly drives the gate of the external N-MOSFET pass element. The typical output impedance of this pin is 2.5kΩ
6	FB	The inverting terminal of the voltage error amplifier; used to feedback the output voltage for comparison with the internal reference voltage.
7	CT	The input to the duty cycle timer circuit. A capacitor is connected from this pin to GND, setting the maximum ON time of the over-current protection circuits.
8	CS	The negative current sense input signal. This pin should be connected through a low noise path to the low side of the current sense resistor.

Block Diagram



Control Loop Block Diagram

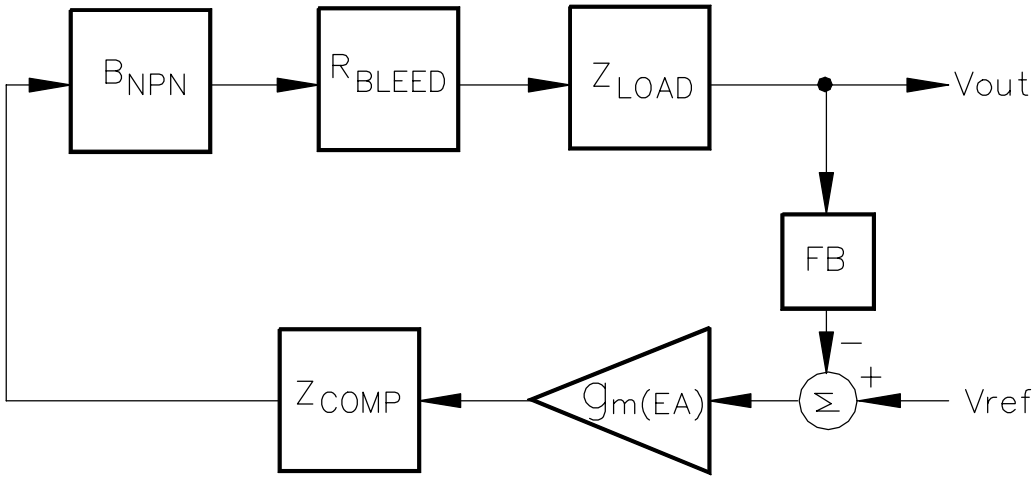


Figure 1.

Applications Information

Basic Operation

Topology

The SC4210A incorporates a charge pump which multiplies the input supply by a factor of approximately three. This charge pump output, or the CAP pin, should be bypassed to GND in order to reduce high frequency ripple – capacitor value isn't critical. The amplified voltage supplies power to both the output stage of the error amplifier and the bipolar buffer transistor which provides the gate potential to the external N-MOSFET.

The error amplifier is a transconductance type with a transconductance of around $0.8mS_{TYP}$. The open loop voltage gain is about 66dB. The output of the E/A is compensated externally through the COMP pin with an RC series network.

The OUT pin is a buffered version of the COMP pin with approximately 2.5kΩ output drive impedance.

Overcurrent protection is accomplished by measuring the voltage potential between the input supply, pin V_{DD}, and the connection of the external sense resistor and drain terminal of the external N-MOSFET at pin CS.

If the potential difference between the CS and V_{DD} exceeds 100mV for a time greater than the value determined by formula (1) below, the device will enter a 4% maximum on-time until the overcurrent condition is removed.

$$T_{delay} = C_T \cdot 0.3V \div 36\mu A \quad (1),$$

where
C_T is the capacitor at the CT pin.

The above applies to the initial overcurrent condition, after which if the overcurrent condition remains in effect, the device will repeatedly cycle on and off according to the following formulas:

$$T_{ON} = C_T \cdot 1V \div 36\mu A \quad (2)$$

$$T_{OFF} = C_T \cdot 1V \div 1.6\mu A \quad (3)$$

During the Gate on-time, the maximum current the pass device may supply is limited to:

$$I_{LIM} = 140mV \div R_{SENSE}$$

The SC4210A incorporates a UVLO rising threshold of $1.73V_{TYP}$ with 90mV hysteresis.

Stability and Transient Performance

The SC4210A topology allows the device to be configured to have both a stable performance across a wide frequency range as well as react quickly to and recover from transients at the output load.

Experimental and simulated results have shown that the device performs well under the following setup conditions:

Rcomp = 24kΩ; Ccomp = 150pF
C_{OUT} = 10uF, tantalum, ESR = 1-2Ω
Rbleed (R3) = 39kΩ
V_{DD} = 3.3V
V_{OUT} = 1.8V
Iout = 100mA to 6A pulses at S_R = 0.3A/µs
External pass device - FDB7030BL, N-MOSFET

The measured ripple voltage is 43mVpk-pk or better than 2.5%; see Figure 2.

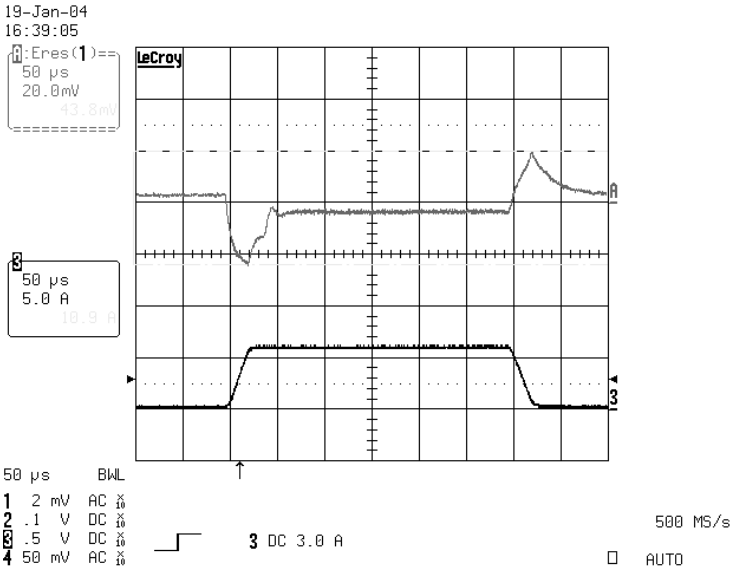


Figure 2.

Applications Information (Cont.)

Using the above values with a constant 3A load gives 80° PM (phase margin) with a unity gain frequency of 2.4MHz; see Figure 3, simulated in P-Spice.

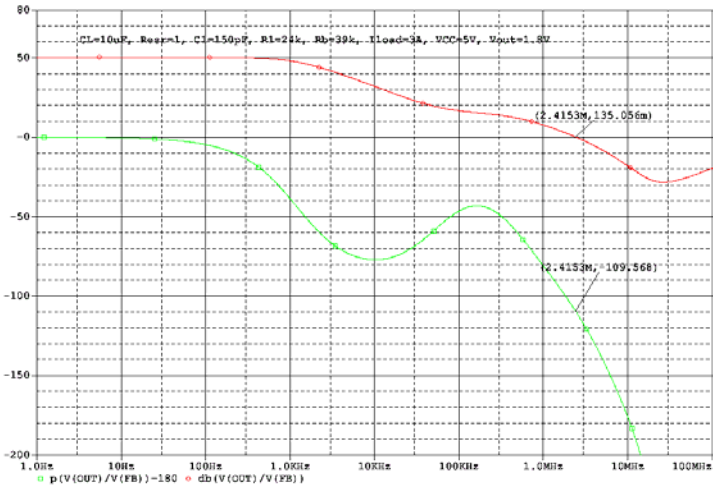


Figure 3.

Compensating the SC4210A can be done by modeling the device in a straight forward fashion using the Control Loop Block Diagram shown in Figure 1.

$$Z_C := \frac{R_C\left(s + \frac{1}{R_C \bullet C_C}\right)}{s}$$

$$R_O := 0.26 \bullet 10^7 \frac{\beta npn \bullet R3}{0.26 \bullet 10^7 + \beta npn \bullet R3}$$

$$F_S := \frac{gm \bullet Ro \bullet Zc}{Ro + Zc}$$

$$gm := 0.8\frac{mA}{V}$$

$$Fs := (0.26 \bullet 10^7) \bullet \frac{(s\,Rc \bullet Cc + 1)R3 \bullet \beta npn \bullet gm}{0.3 \bullet 10^7 \beta npn \bullet R3 \bullet s\,Cc + 0.26 \bullet 10^7 \bullet s\,Rc \bullet Cc + \beta npn \bullet R3 \bullet s\,Rc \bullet Cc + 0.26 \bullet 10^7 + \beta npn \bullet R3}$$

$$FB := \frac{R5}{R4 + R5}$$

$$ZL := \frac{1}{s\,CL} + Resr$$

$$Gs := \frac{RL \bullet ZL}{RL + ZL}$$

$$Gs := \frac{RL\left(\frac{1}{s\,CL} + Resr\right)}{\left(RL + \frac{1}{s\,CL} + Resr\right)}$$

$$Hs := \frac{R5}{(R4 + R5)} \bullet F_S \bullet G_S$$

The basic analysis yields a two pole, two zero system. However, considering a limited bandwidth of the NPN buffer stage and external N-MOSFET, the system eventually rolls off due to the third pole at very high frequencies (10-20MHz). The low ESR ceramic capacitors push the secondary zero to well above the unity gain frequency, requiring accurate placement of the dominant zero for stability.

To adjust the above values, say for an output capacitor of 1µF ceramic (ESR=1mΩ), the Rcomp initially should be decreased by the same multiple as the output capacitor, i.e. Rcomp = 24kΩ ÷ 10 = 2.4kΩ. Simulated results yield over 90° of PM at a unity gain frequency of 386kHz; see Figure 4.

Applications Information (Cont.)

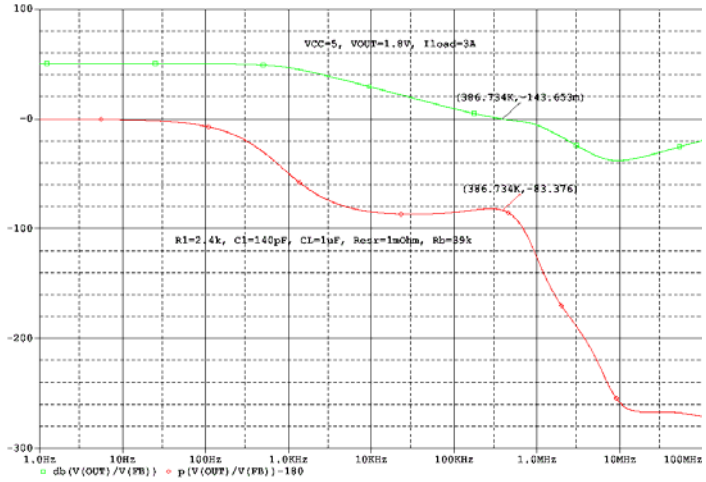


Figure 4.

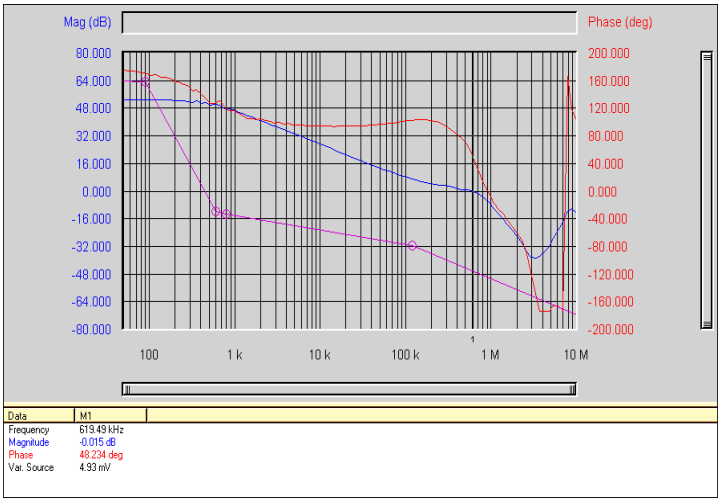


Figure 6.

Figure 5 shows the transient response for the circuit described above – the ripple Vpk-pk is almost 60mVpk-pk, which is a result of the overdamped system.

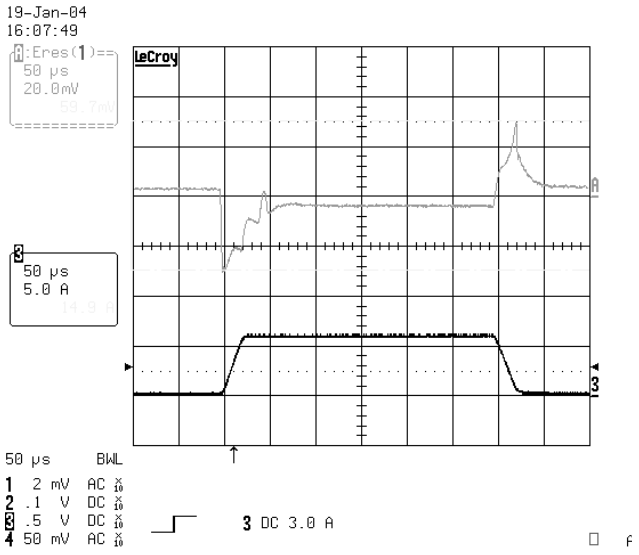


Figure 5.

Figure 7. is an example of how close the actual results can be obtained with the simulation once the correct model has been defined. Below is the P-Spice simulation of the circuit which was built and tested with Ridley instrument; see Figure 6.

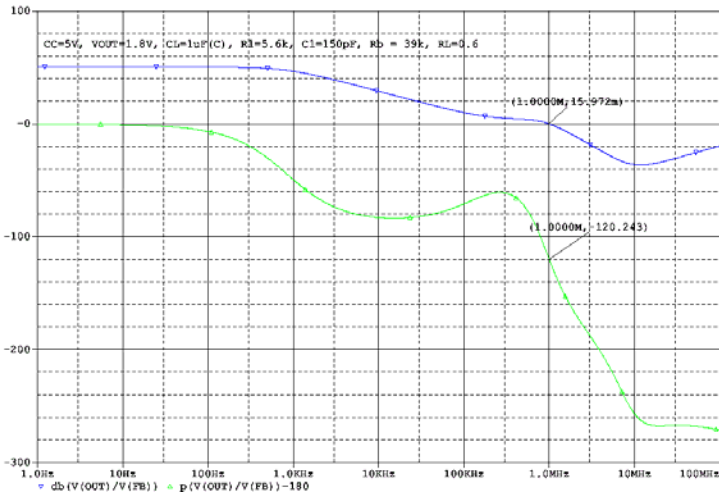


Figure 7.

This circuit can be modified to improve transient performance. This can be achieved by raising Rcomp until the PM decreases to 50-60° at unity gain crossover. This is achieved by raising Rcomp to approximately 5.6kΩ, which gives a PM of 50° at a unity gain of 1MHz; see Figure 6 for the actual circuit Bode plot taken with Ridley Instrument.

Again, we achieved a respectable transient response, V_{OUT_RIPPLE} < 50mVpk-pk, less then 3% of the V_{OUT} = 1.8V; see Figure 8.

Applications Information (Cont.)

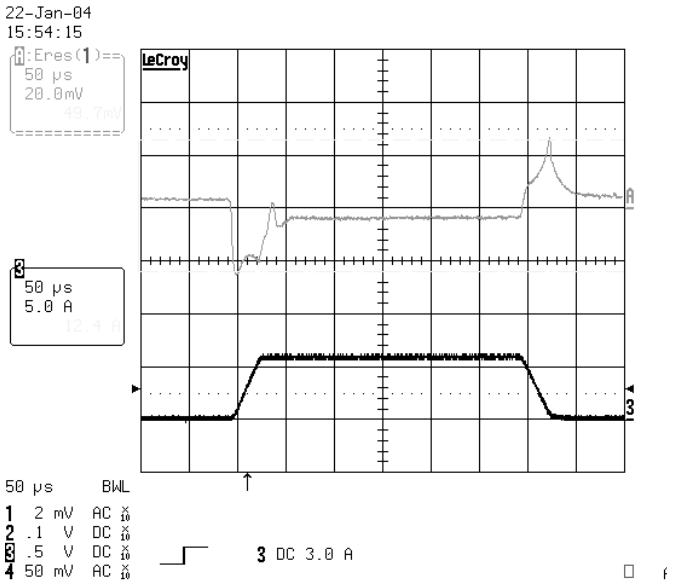


Figure 8.

An output capacitor is not required for stability. If one is used, compensation is required. Assuming there is no output cap present, only Ccomp will be used. Under this condition, the non-dominant pole and both zero's are pushed well above the unity gain frequency. Using only a Ccomp = 100pF without an output capacitor, the system yields a PM of 78.5° with a unity gain frequency of 387kHz; see Figure 9.

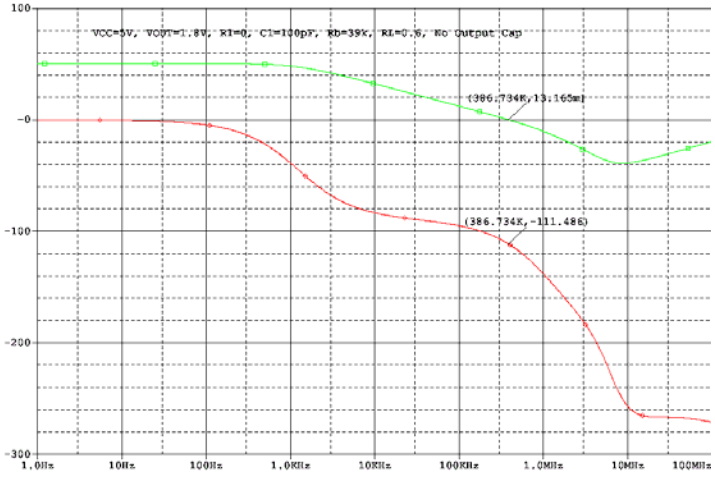


Figure 9.

The pass transistor does add an additional pole to the transfer function. Generally speaking, this parasitic non-dominant pole is at frequencies well above the unity gain frequency but should be considered when various types of N-MOSFETs are available.

The purpose of the R_{BLEED} is to improve the transient response, reduce overshoot, and to remove an unwanted output ripple voltage if no load is applied to the output.

In a practical sense, it is chosen to bleed (drain) about 100µA - 150µA. The optimum value depends on the input/output voltage ratio and the constraints on the output ripple voltage. Simulation analysis and real life circuit testing have shown very close correlation.

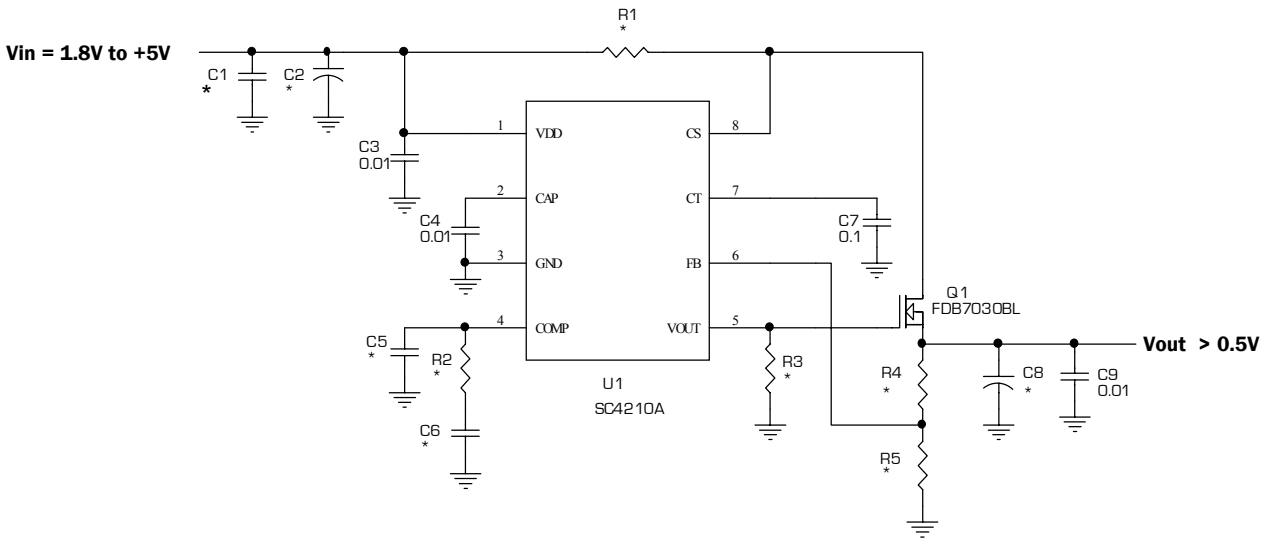
Following the procedure described above yields a stable operation and excellent transient response over a wide range of output capacitors: extra low-ESR "ceramics" and "organics", mid-ESR "polymers" and "tantalums", low-cost aluminum capacitors. Below in Table 1 are the summarized results of choosing R_{COMP} and C_{COMP} values for the typical application circuit shown on Page 1.

V_{OUT_RIPPLE} (mVp-p)	C_{OUT} (µF)	ESR (Ω)	R_{COMP} (K)	C_{COMP} (pF)
32	0.1	0.003 - 0.005	2.7	33
53	1	0.002 - 0.003	2.7	150
50	10	0.001 - 0.002	24	100
45	10	1 - 5	24	100
46	10	10 - 20	24	100
46	22	5 - 10	24	100
41	33	0.001 - 0.002	82	150
55	0	-	24	100
55	0	-	0	100

Table 1

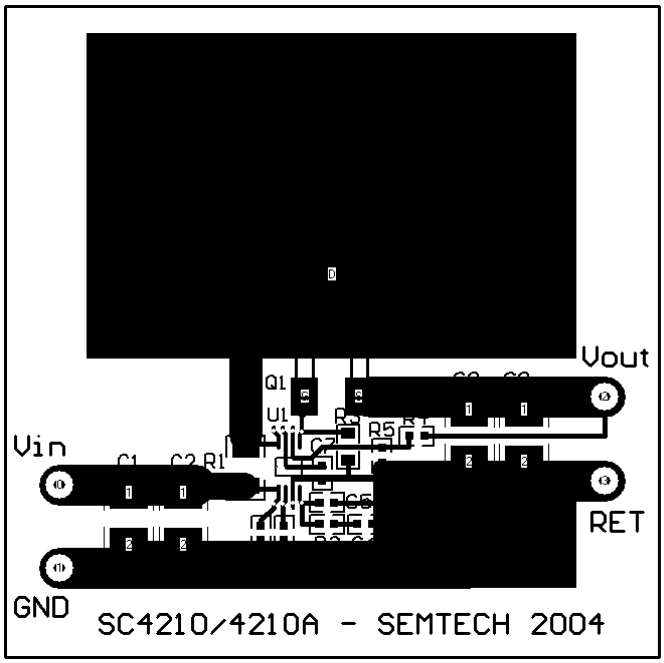
Test Conditions:
V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 6A/0.12A, S_r = 0.3A/µs.

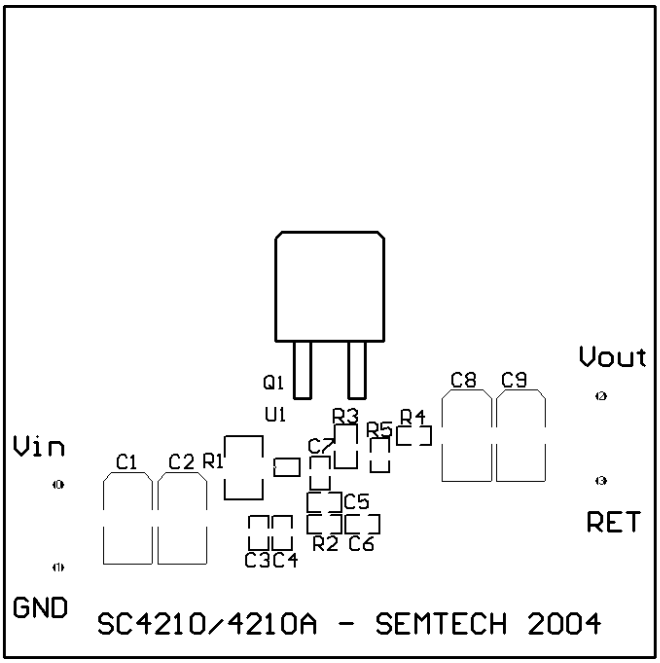
Evaluation Board Circuit



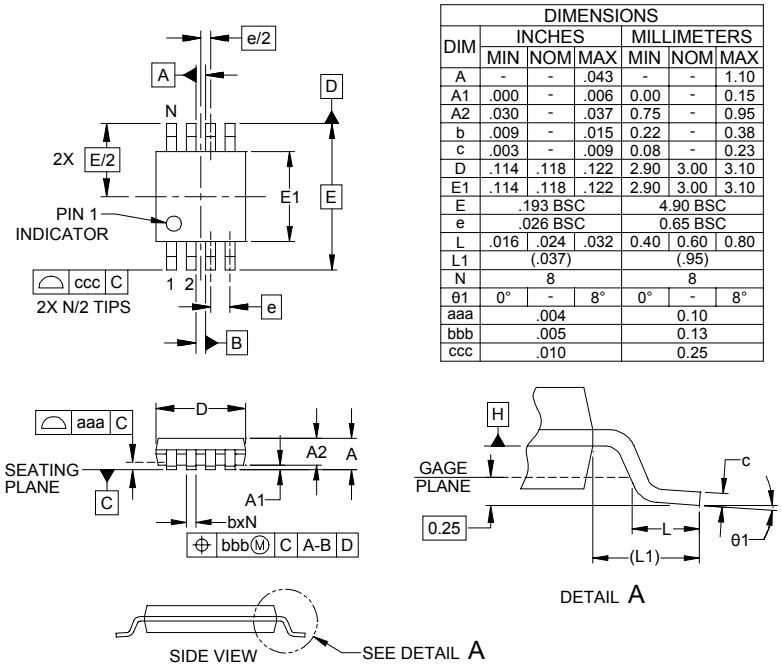
*** Denotes variable components**

Evaluation Board Layout and Components Placement





Outline Drawing - MSOP-8

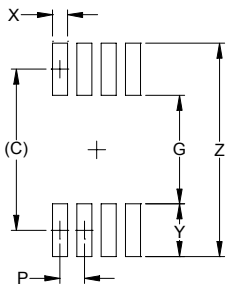


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.009	-	.015	0.22	-	0.38
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.026 BSC			0.65 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.005			0.13		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION AA.

Land Pattern - MSOP-8



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.026	0.65
X	.016	0.40
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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