LINFINITY
A MICROSEMI COMPANY
THE INFINITE POWER OF INNOVATION

UltraMAX™ LX5248 / LX5249

9-LINE LVD SCSI TERMINATOR

PRELIMINARY DATA SHEET

DESCRIPTION

The LX5248/49 IC is a Low Voltage Differential (LVD) Terminator designed to comply with the LVD termination specification in the SPI-2 document. The LX5248/ 49 is designed specifically for LVD applications. Because the LX5248/49 supports only LVD, it has lower output capacitance than multimode terminators such as the LX5240.

The LX5248/49 Utilizes Linfinity's UltraMAX Technology which delivers the ultimate in SCSI bus performance while saving component cost and board area. Elimination of the external capacitors also mitigates the need for a lengthy capacitor selection process. The individual high bandwidth drivers also maximize channel separation and reduces channel-to-channel noise and cross talk. The high-bandwidth UltraMAX architecture insures ULTRA-2 performance, while providing a clear migration path to ULTRA-3 and beyond.

When The LX5248/49 Is Enabled, The Differential Sense (DIFFSENSE) Pin Supplies A Voltage Between 1.2V And 1.4V. In application, the terminator DIFFSENSE output is connected to the system DIFFSENSE line. If there are no single ended or HVD devices attached to the system the LVD output will be enabled. If the DIFFSENSE line is LOW, indicating a single ended device, the LX5248/49 output will be HiZ. If the DIFFSENSE line is HIGH, indicating a high voltage differential device the LX5248/49 output will be HiZ.

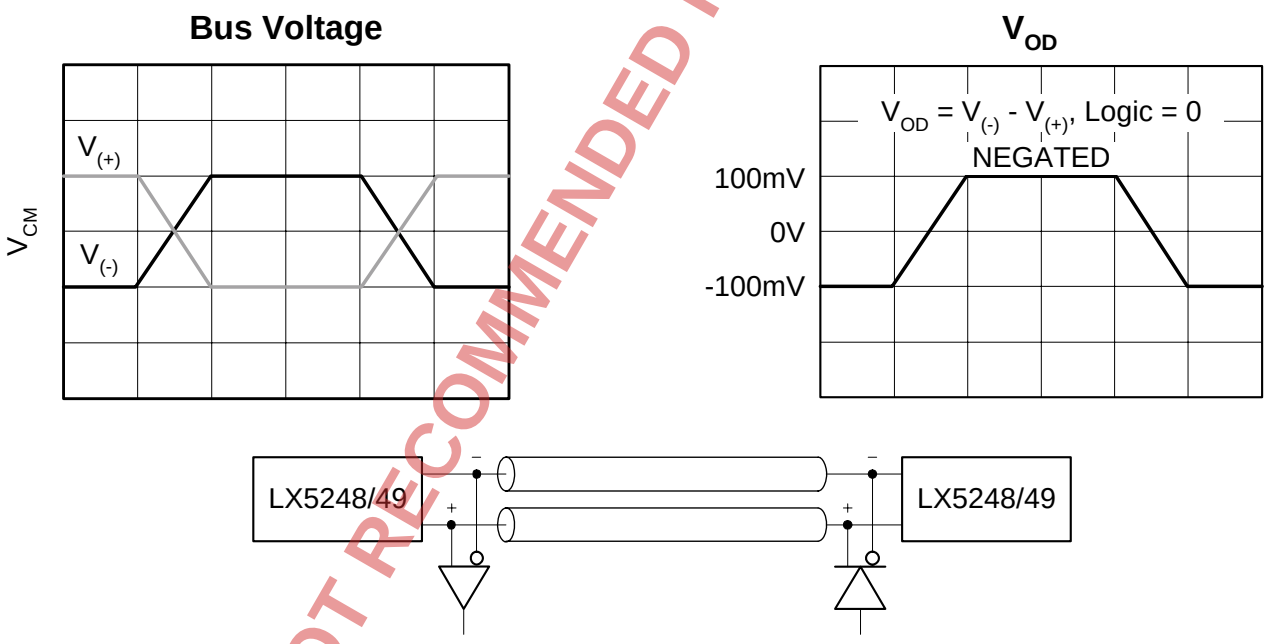
The LX5248/49 IC Has A TTL Compatible DISCONNECT Pin. The LX5248/49 is active LOW. During sleep mode, power dissipation is reduced to a meager 5µA, while also placing all outputs in a HI Z state. Also during sleep mode, the DIFFSENSE function is disabled and is placed in a HI Z state.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- 2.5pF Typical Disabled Output Capacitance
- Fast Response, No External Capacitors Required
- 5µA Supply Current In Disconnect Mode
- 20mA Supply Current During Normal Operation
- Logic Command Disconnects All Termination Lines
- Diffsense Line Driver
- Current Limit And Thermal Protection
- Compliant with SP1-2 (Ultra2) and SP1-3 (Ultra 160)
- Pin Compatible With Industry Standard Multi-Mode Terminators
- For UCC5240 Pin Compatible LVD ONLY Terminator (See LX5245/5246)

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	DB Plastic TSSOP 36-Pin RoHS Compliant / Pb-free Transition DC: 0535	PW Plastic TSSOP 24-Pin RoHS Compliant / Pb-free Transition DC: 0442	PW Plastic TSSOP 28-Pin RoHS Compliant / Pb-free Transition DC: 0518
0 to 70	**LX5249CDBK**	**LX5249CPW**	**LX5248CPW**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX5249CDBK-TR)

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9-LINE LVD SCSI TERMINATOR

PRELIMINARY DATA SHEET

ABSOLUTE MAXIMUM RATINGS (Note 1)

TermPwr Voltage ..... +6.5V
Signal Line Voltage ..... 0V to 6.5V
Differential Voltage ..... 0V to 6.5V
Operating Junction Temperature
Plastic (PW Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C
RoHS / Pb-free Peak Package Solder Reflow Temp.(40 sec. max. exp.)...260°C(+0, -5)

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

DB PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	50°C/W

PW PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

MASTER / $\overline{\text{SLAVE}}$ FUNCTION TABLE

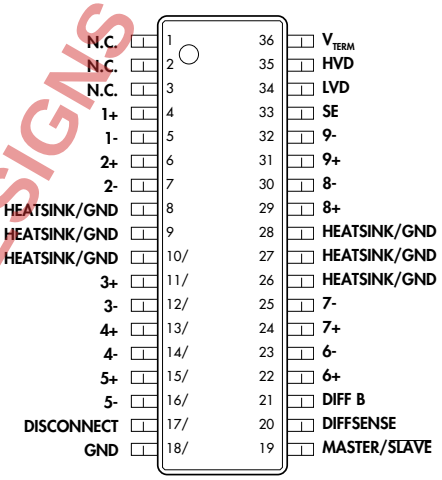
MASTER / $\overline{\text{SLAVE}}$	DIFFSENSE Status	Output Current
L*	HI Z	0mA
H	1.3V	15mA Source
Open (Pull-up)	1.3V	15mA Source

* When in Low state, terminator will detect state of DIFFSENSE line.

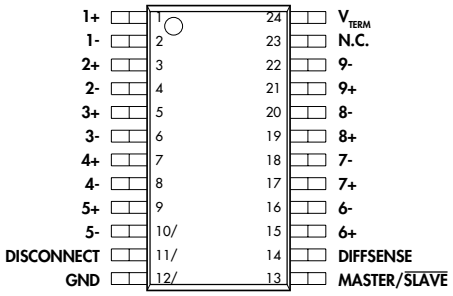
DIFFSENSE / POWER UP / POWER DOWN FUNCTION TABLE

LX5248/LX5249 DISCONNECT	DIFFSENSE	Outputs Status	Outputs Type	Quiescent Current
L	L < 0.5V	Disable	HiZ	2mA
L	0.7V to 1.9V	Enable	LVD	21mA
L	H > 2.4V	Disable	HiZ	2mA
H	X	Disable	HiZ	10µA
Open	X	Disable	HiZ	10µA

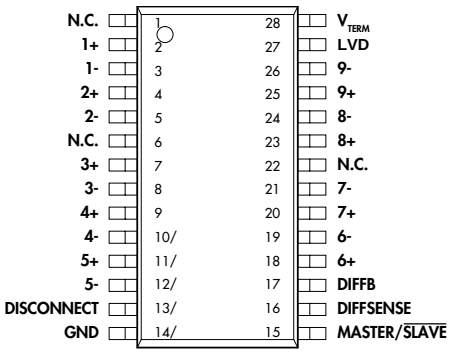
PACKAGE PIN OUTS



LX5249C ("N.C." = No Internal Connection)
DB PACKAGE (Top View)



LX5249CPW ("N.C." = No Internal Connection)
PW PACKAGE (Top View)



LX5248CPW ("N.C." = No Internal Connection)
PW PACKAGE (Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Termpwr Voltage	V_{TERM}	3.0		5.25	V
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		V_{TERM}	V
Operating Junction Temperature Range					
LX5248 / LX5249		0		70	°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperature range of 0°C ≤ T_A ≤ 70°C. TermPwr = 3.3V, DISCONNECT: LX5248/49 = L. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Symbol	Test Conditions	LX5248 / 5249			Units
			Min.	Typ.	Max.	
LVD Terminator Section						
TermPwr Supply Current	LVD I_{CC}	All term lines = Open		21	25	mA
		DISCONNECT: LX5248/49 = H		5	10	µA
Common Mode Voltage	V_{CM}		1.125	1.25	1.375	V
Offset Voltage (Fail Safe Bias Voltage)	V_{FSB}	Open circuit between - and + (see Note 3)	100	112	125	mV
Differential Terminator Impedance	Z_D	V_{OD} = -1V to 1V	100	105	110	Ω
Common Mode Impedance	Z_{CM}	0V to 2.5V	100	200	300	Ω
Output Capacitance	C_O	DISCONNECT: LX5248/49 = H		2.5		pF
Output Leakage	I_{LEAK}	DISCONNECT: LX5248/49 = H, V_{LINE} = 0 to 4V, T_A=25°C		0	2	µA
		DISCONNECT: LX5248/49 = H, V_{TERM} = 0V, V_{LINE} = 2.7V		1		µA
Mode Change Delay	t_{DF}	DIFFSENSE = 1.4V to 0V	100	150		ms
DIFFSENSE Section						
DIFFSENSE Output Voltage	V_{DIFF}		1.2	1.3	1.4	V
DIFFSENSE Output Source Current	I_{DIFF}	DIFFSENSE = 0V	5.0		15.0	mA
DIFFSENSE Sink Current	$I_{SINK (DIFF)}$	V_{IN} = 2.75V			200	µA
DIFFSENSE Output Leakage	$I_{SINK (DIFF)}$	DISCONNECT: LX5248/49 = H, T_A = 25°C			10	µA
DISCONNECT Section						
DISCONNECT Threshold	V_{TH}		0.8		2.0	V
Input Current	I_{IL}	DISCONNECT: LX5248/49 = 0V			10	µA
MASTER / $\overline{\text{SLAVE}}$ Section						
MASTER / $\overline{\text{SLAVE}}$ Threshold	$V_{TH (MS)}$		0.8		2.0	V
Input Current	$I_{IL (MS)}$	MASTER / $\overline{\text{SLAVE}}$: LX5248/49 = 0V			10	µA

Note 3. Open circuit failsafe voltage.

BLOCK DIAGRAM

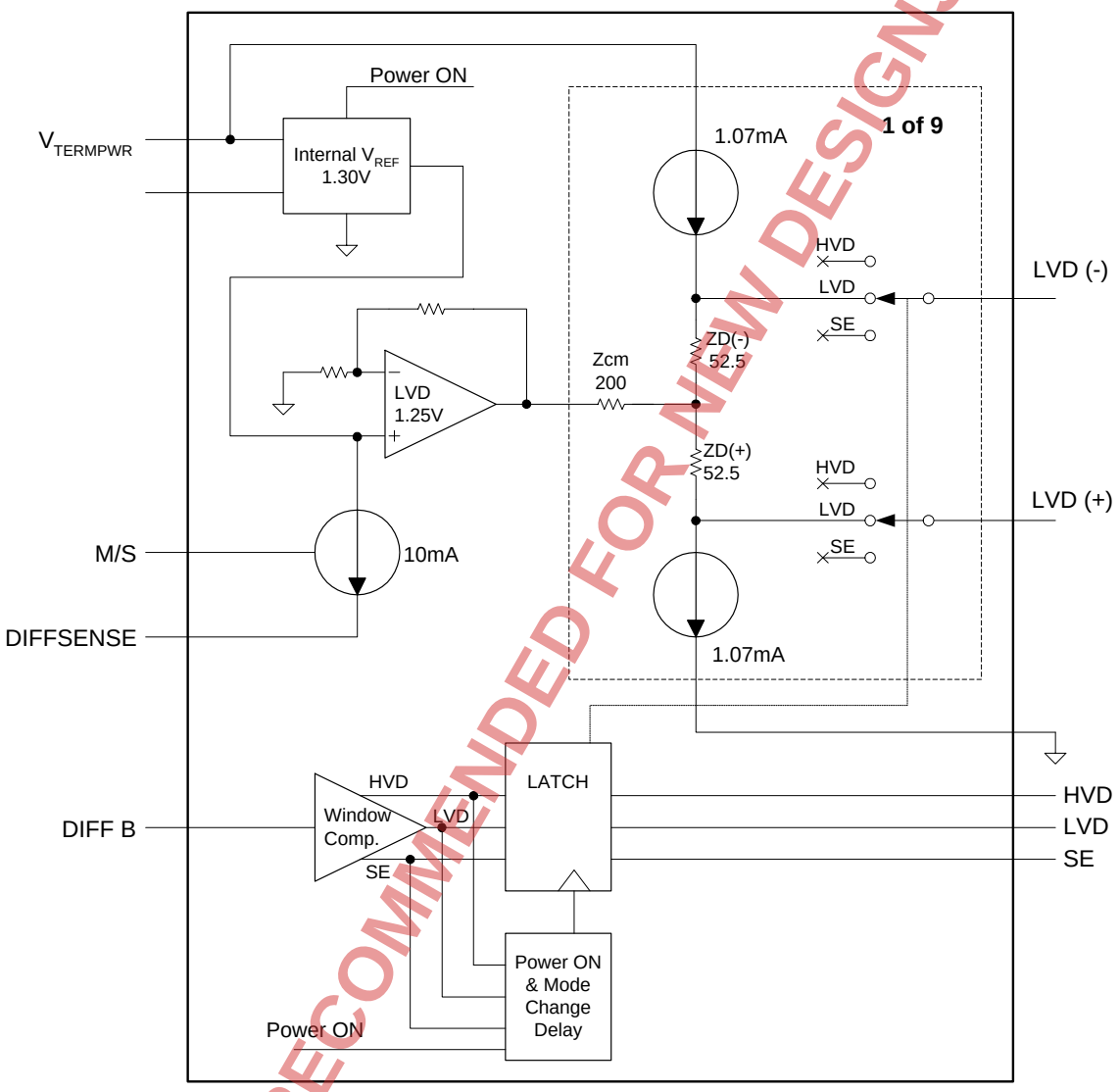
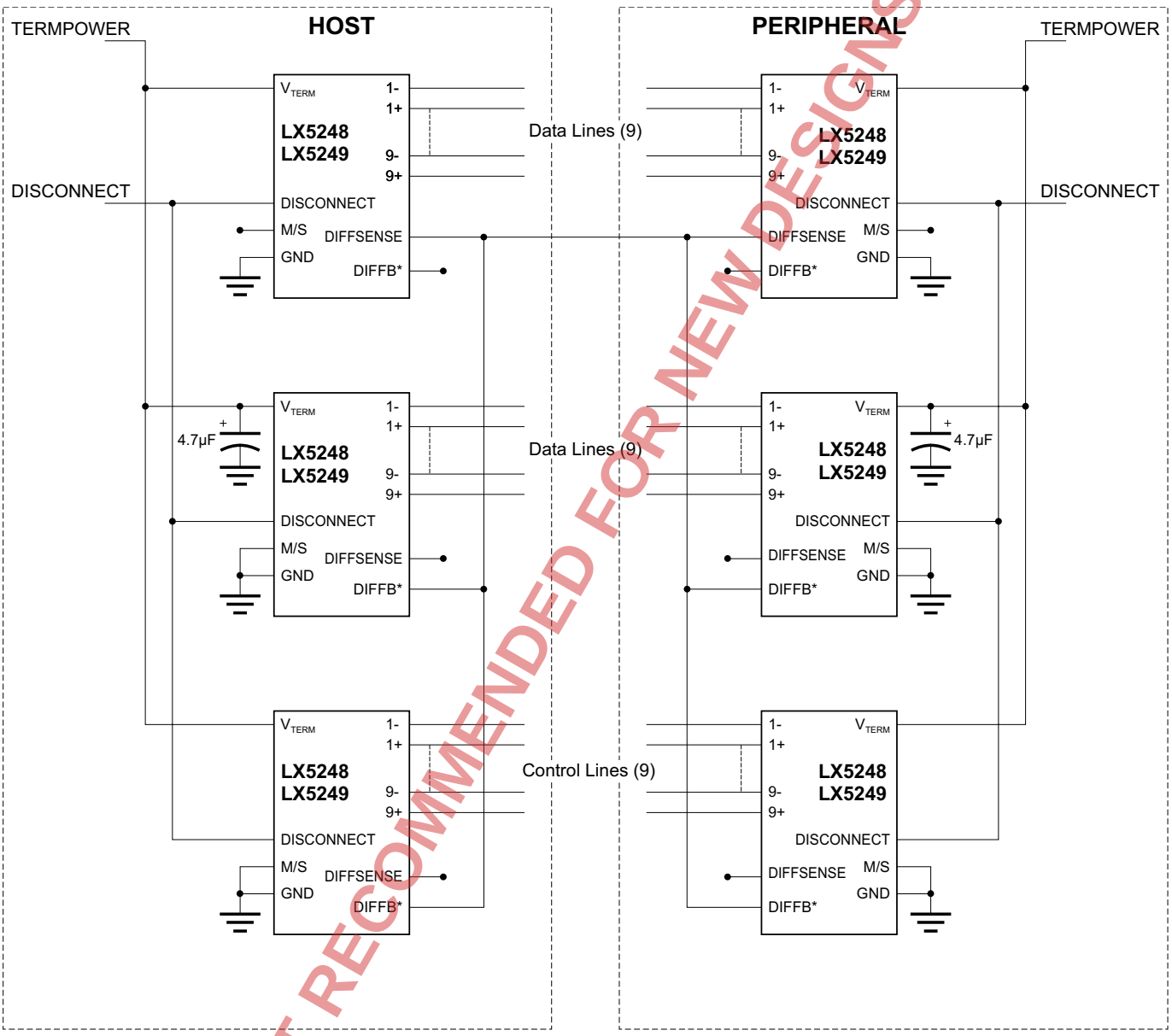


FIGURE 1 — LX5248 / 5249 Block Diagram

FUNCTIONAL PIN DESCRIPTION

Pin Designator	Description
1-, 2-, 3-, 4-, 5-, 6-, 8-, 8-, 9-/	Negative signal termination lines.
1+, 2+, 3+, 4+, 5+, 6+, 7+, 8+, 9+/	Positive signal termination lines.
V_{TERM}	Power supply pin for terminator. Connect to SCSI bus TERMPWR. Must be decoupled by one 4.7µF low-ESR capacitor for every three terminator devices. It is absolutely necessary to connect this pin to the decoupling capacitor through a very low impedence (big traces on PCB). Keeping distances very short from the decoupling capacitors to the V_{TERM} pin is also critical. The value of the decoupling capacitor is somewhat layout dependant and some applications may benefit from high-frequency decoupling with 0.1µF capacitors right at V_{TERM} pin.
DISCONNECT/	Enables / disables terminator. See Power Down Function Table for logic level per device.
GND/	Terminator ground pin. Connect to ground.
MASTER / SLAVE/	Sometimes referred to as M/S pin in this data sheet. Used to select which terminator is the controlling device. MASTER/SLAVE pin High or Open enables the DIFFSENSE output drive. Please see MASTER/SLAVE Function Table.
DIFFSENSE/	This is a dual function pin. It drives the SCSI bus DIFFSENS line. It is also the sense pin to detect the SCSI bus mode (LVD, SE or HVD). DIFFSENSE output drive can be disabled with Low level on the MASTER/SLAVE pin. Please see DIFFSENSE and MASTER/SLAVE Function Tables. Internally connected to DIFFB pin through 20kOhm resistor.
DIFFB/	Internally connected to DIFFSENSE pin through 20kOhm resistor. It can be used as a mode sense pin when the device is a non-controlling terminator (MASTER/SLAVE pin is Low). An RC filter (20kOhm / 0.1µF) is not required on the LX5249, as it has an internal timer.
SE/	Single-ended output: when High, terminator is operating in SE mode.
LVD/	Low Voltage Differential output. When High, terminator is operating in LVD mode.
HVD/	High Voltage Differential output. When High, terminator is operating in HVD mode.
HEATSINK/	Attached to die mounting pad, but not bonded to GND pin. Pins should be considered a heat sink only, and not a true groung connection. It is recommended that these pins be connected to ground, but can be left floating.

APPLICATION SCHEMATIC



* DIFFB Pin not present on LX5248CPW / 5249CPW Packages. Must connect DIFFSENS signal to DIFFSENSE pin on PW package.

FIGURE 2 — LX5248 / 5249 Application Schematic