USB3300

Hi-Speed USB Host, Device or OTG PHY with ULPI Low Pin Interface

PRODUCT FEATURES

Data Brief

- USB-IF Hi-Speed certified to the Universal Serial Bus Specification Rev 2.0
- Interface compliant with the ULPI Specification revision 1.1 in 8-bit mode
- Industry standard UTMI+ Low Pin Interface (ULPI) Converts 54 UTMI+ signals into a standard 12 pin Link controller interface
- 54.7mA Unconfigured Current (typical) - ideal for bus powered applications
- 83uA suspend current (typical) - ideal for battery powered applications
- Latch-Up performance exceeds 150 mA per EIA/JESD 78, Class II
- ESD protection levels of ±8kV HBM without external protection devices
- Integrated protection to withstand IEC61000-4-2 ESD tests (±8kV contact and ±15kV air) per 3rd party test facility
- Supports FS pre-amble for FS hubs with a LS device attached (UTMI+ Level 3)
- Supports HS SOF and LS keep-alive pulse
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 1.0a specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Allows host to turn VBUS off to conserve battery power in OTG applications
- Supports OTG monitoring of VBUS levels with internal comparators. Includes support for an external VBUS or fault monitor.
- Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI wrapper
- Integrated Pull-up resistor on STP for interface protection allows a reliable Link/PHY start-up with slow Links (software configured for low power)
- Internal 1.8 volt regulators allow operation from a single 3.3 volt supply
- Internal short circuit protection of ID, DP and DM lines to VBUS or ground
- Integrated 24MHz Crystal Oscillator supports either crystal operation or 24MHz external clock input
- Internal PLL for 480MHz Hi-Speed USB operation
- Industrial Operating Temperature -40°C to +85°C
- 32 pin, QFN Lead-Free RoHS Compliant package (5 x 5 x 0.90 mm height)

Applications

The USB3300 is the ideal companion to any ASIC, SoC or FPGA solution designed with a ULPI Hi-Speed USB host, peripheral or OTG core.

The USB3300 is well suited for:

- Cell Phones
- PDAs
- MP3 Players
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Printers

ORDER NUMBERS:

USB3300-EZK for 32 pin, QFN Lead-Free RoHS Compliant Package

USB3300-EZK-TR for 32 pin, QFN Lead-Free RoHS Compliant Package (tape and reel)

Reel Size is 4000 pieces.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

General Description

The USB3300 is an industrial temperature Hi-Speed USB Physical Layer Transceiver (PHY). The USB3300 uses a low pin count interface (ULPI) to connect to a ULPI compliant Link layer. The ULPI interface reduces the UTMI+ interface from 54 pins to 12 pins using a method of in-band signaling and status byte transfers between the Link and PHY.

This PHY was designed from the start with the ULPI interface. No UTMI to ULPI wrappers are used in this design which provides a seamless ULPI to Link interface. The result is a PHY with a low latency transmit and receive time. SMSC's low latency high speed and full speed receiver provide the option of re-using existing UTMI Links with a simple wrapper to convert UTMI to ULPI.

The ULPI interface allows the USB3300 PHY to operate as a device, host, or an On-The-Go (OTG) device. Designs using the USB3300 PHY as a device, can add host and OTG capability at a later date with no additional pins.

The ULPI interface, combined with SMSC's proprietary technology, makes the USB3300 the ideal method of adding Hi-Speed USB to new designs. The USB3300 features an industry leading small footprint package (5mm by 5mm) with sub 1mm height. In addition the USB3300 integrates all DP and DM termination resistances and requires a minimal number of external components.

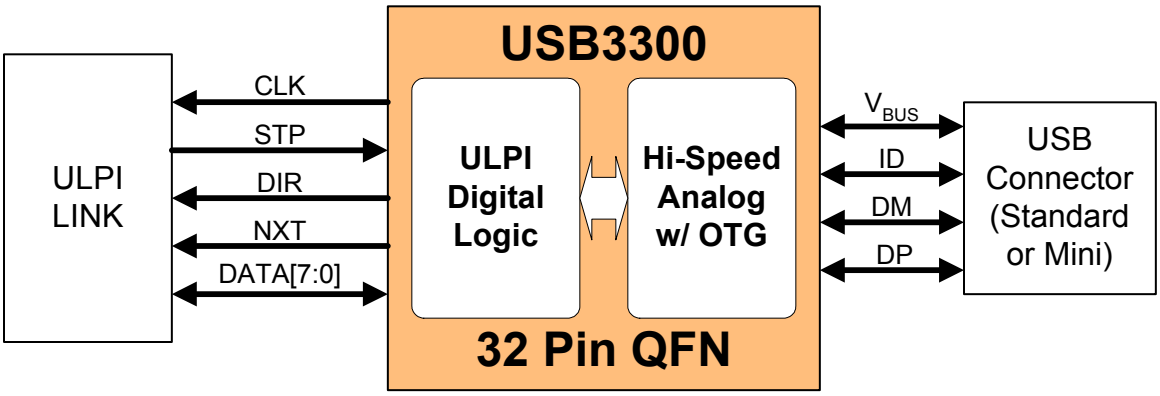

Figure 1 Basic ULPI USB Device Block Diagram

The ULPI interface consists of 12 interface pins; 8 bi-directional data pins, 3 control pins, and a 60 MHz clock. By using the 12 pin ULPI interface the USB3300 is able to provide support for the full range of UTMI+ Level 3 through Level 0, as shown in Figure 2, "ULPI Interface Features as Related to UTMI+". This allows USB3300 to work as a HS and FS peripheral and as a HS, FS, and LS Host.

The USB3300 can also, as an option, fully support the On-the-Go (OTG) protocol defined in the On-The-Go Supplement to the USB 2.0 Specification. On-the-Go allows the USB3300 to function like a host, or peripheral configured dynamically by software. For example, a cell phone may connect to a computer as a peripheral to exchange address information or connect to a printer as a host to print pictures. Finally the OTG enabled device can connect to another OTG enabled device to exchange information. All this is supported using a single low profile Mini-AB USB connector.

Designs not needing OTG can ignore the OTG feature set.

In addition to the advantages of the leading edge ULPI interface, the use of SMSC's advanced analog technology enables the USB3300 to consume a minimum amount of power which results in maximized battery life for portable applications.

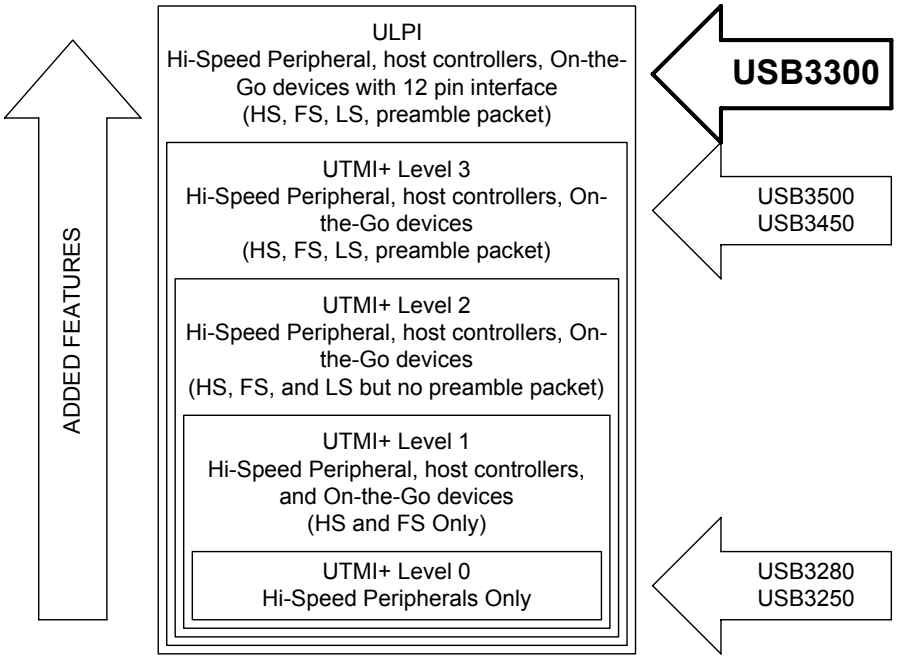

Figure 2 ULPI Interface Features as Related to UTMI+

PRODUCT PREVIEW

Block Diagram

The USB3300 is a highly integrated USB PHY. It contains a complete Hi-Speed USB 2.0 PHY with the ULPI industry standard interface to support fast time to market for a USB product. The USB3300 is composed of the functional blocks shown in Figure 3, "USB3300 Block Diagram" below.

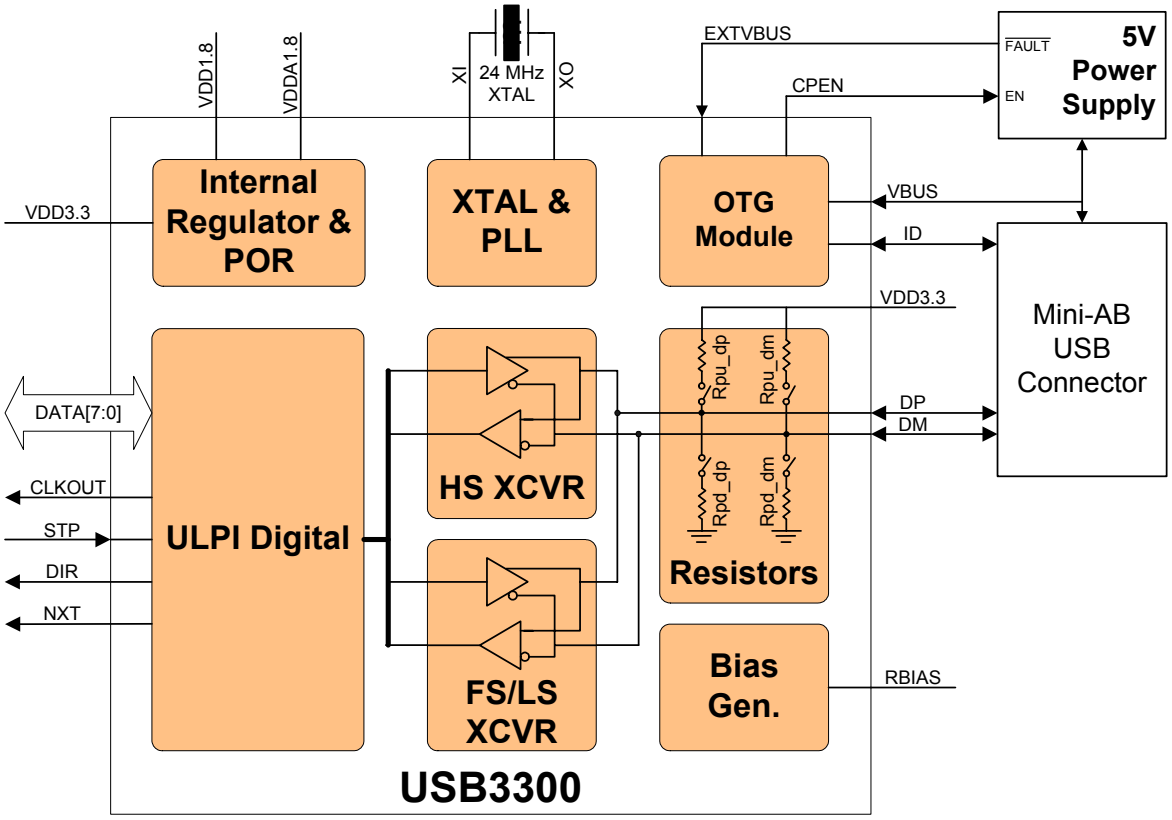

Figure 3 USB3300 Block Diagram

Pin Configuration and Pin Definitions

The USB3300 is offered in a 32 pin QFN package (5 x 5 x 0.9mm). The pin definitions and locations are documented below.

USB3300 Pin Locations

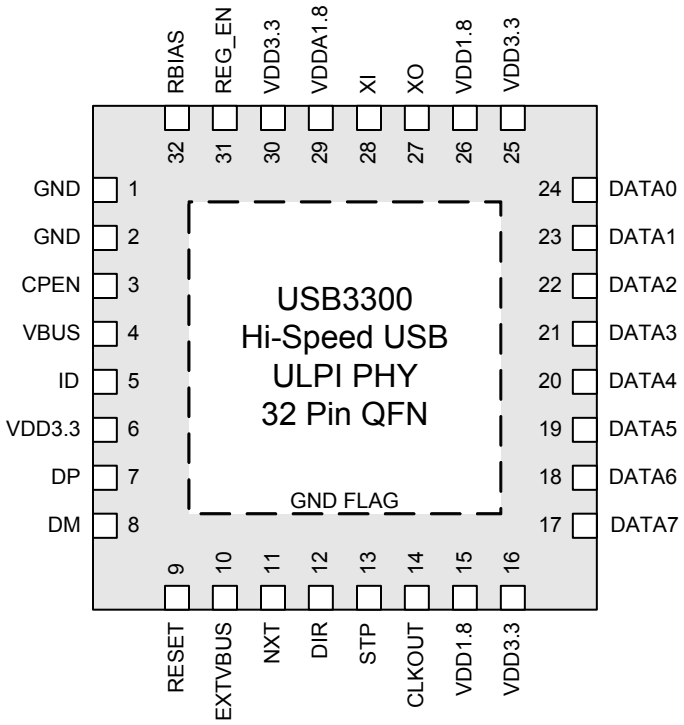

Figure 4 USB3300 Pinout - Top View

The exposed flag of the QFN package must be connected to ground with a via array to the ground plane. This is the main ground connection for the USB3300.

Pin Definitions, 32-Pin QFN Package

Table 1 USB3300 Pin Definitions

PIN	NAME	DIRECTION, TYPE	ACTIVE LEVEL	DESCRIPTION
1	**GND**	Ground	N/A	Ground
2	**GND**	Ground	N/A	Ground
3	**CPEN**	Output, CMOS	High	External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The CPEN pin is low on POR.
4	**VBUS**	I/O, Analog	N/A	VBUS pin of the USB cable. The USB3300 uses this pin for the Vbus comparator inputs and for Vbus pulsing during session request protocol.

Table 1 USB3300 Pin Definitions (continued)

PIN	NAME	DIRECTION, TYPE	ACTIVE LEVEL	DESCRIPTION
5	**ID**	Input, Analog	N/A	ID pin of the USB cable. For non-OTG applications this pin can be floated. For an A-Device ID = 0. For a B-Device ID = 1.
6	**VDD3.3**	Power	N/A	3.3V Supply. A 0.1uF bypass capacitor should be connected between this pin and the ground plane on the PCB.
7	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
8	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
9	**RESET**	Input, CMOS	High	Optional active high transceiver reset. This is the same as a write to the ULPI *Reset*, address 04h, bit 5. This does not reset the ULPI register set. This pin includes an integrated pull-down resistor to ground. If not used, this pin can be floated or connected to ground (recommended).
10	**EXTVBUS**	Input, CMOS	High	External Vbus Detect. Connect to fault output of an external USB power switch or an external Vbus Valid comparator. This pin has a pull down resistor to prevent it from floating when the ULPI bit *UseExternalVbusIndicator* is set to 0.
11	**NXT**	Output, CMOS	High	The PHY asserts NXT to throttle the data. When the Link is sending data to the PHY, NXT indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.
12	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives DIR high to take ownership of the bus. When the PHY has no data to transfer it drives DIR low and monitors the bus for commands from the Link. The PHY will pull DIR high whenever the interface cannot accept data from the Link, such as during PLL start-up.
13	**STP**	Input, CMOS	High	The Link asserts STP for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, STP indicates the last byte of data was on the bus in the previous cycle.
14	**CLKOUT**	Output, CMOS	N/A	60MHz reference clock output. All ULPI signals are driven synchronous to the rising edge of this clock.
15	**VDD1.8**	Power	N/A	1.8V for digital circuitry on chip. Supplied by On-Chip Regulator when REG_EN is active. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 15 to pin 26.
16	**VDD3.3**	Power	N/A	A 0.1uF bypass capacitor should be connected between this pin and the ground plane on the PCB.

Table 1 USB3300 Pin Definitions (continued)

PIN	NAME	DIRECTION, TYPE	ACTIVE LEVEL	DESCRIPTION
17	**DATA[7]**	I/O, CMOS, Pull-low	N/A	8-bit bi-directional data bus. Bus ownership is determined by DIR. The Link and PHY initiate data transfers by driving a non-zero pattern onto the data bus. ULPI defines interface timing for a single-edge data transfers with respect to rising edge of CLKOUT. DATA[7] is the MSB and DATA[0] is the LSB.
18	**DATA[6]**	I/O, CMOS, Pull-low	N/A	
19	**DATA[5]**	I/O, CMOS, Pull-low	N/A	
20	**DATA[4]**	I/O, CMOS, Pull-low	N/A	
21	**DATA[3]**	I/O, CMOS, Pull-low	N/A	
22	**DATA[2]**	I/O, CMOS, Pull-low	N/A	
23	**DATA[1]**	I/O, CMOS, Pull-low	N/A	
24	**DATA[0]**	I/O, CMOS, Pull-low	N/A	
25	**VDD3.3**	Power	N/A	A 0.1uF bypass capacitor should be connected between this pin and the ground plane on the PCB.
26	**VDD1.8**	Power	N/A	1.8V for digital circuitry on chip. Supplied by On-Chip Regulator when REG_EN is active. When using the internal regulators, place a 4.7uF low-ESR capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 26 to pin 15. Do not connect VDD1.8 to VDDA1.8 when using internal regulators. When the regulators are disabled, pin 29 may be connected to pins 26 and 15.
27	**XO**	Output, Analog	N/A	Crystal pin. If using an external clock on XI this pin should be floated.
28	**XI**	Input, Analog	N/A	Crystal pin. A 24MHz crystal is supported. The crystal is placed across XI and XO. An external 24MHz clock source may be driven into XI in place of a crystal.
29	**VDDA1.8**	Power	N/A	1.8V for analog circuitry on chip. Supplied by On-Chip Regulator when REG_EN is active. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. When using the internal regulators, place a 4.7uF low-ESR capacitor near this pin in parallel with the 0.1uF capacitor. Do not connect VDD1.8A to VDD1.8 when using internal regulators. When the regulators are disabled, pin 29 may be connected to pins 26 and 15.
30	**VDD3.3**	Power	N/A	Analog 3.3 volt supply. A 0.1uF low ESR bypass capacitor connected to the ground plane of the PCB is recommended.

Table 1 USB3300 Pin Definitions (continued)

PIN	NAME	DIRECTION, TYPE	ACTIVE LEVEL	DESCRIPTION
31	**REG_EN**	I/O, CMOS, Pull-low	N/A	On-Chip 1.8V regulator enable. Connect to ground to disable both of the on chip (VDDA1.8 and VDD1.8) regulators. When regulators are disabled: ▪ External 1.8V must be supplied to VDDA1.8 and VDD1.8 pins. When the regulators are disabled, VDDA1.8 may be connected to VDD1.8 and a bypass capacitor (0.1uF recommended) should be connected to each pin. ▪ The voltage at VDD3.3 must be at least 2.64V (0.8 * 3.3V) before voltage is applied to VDDA1.8 and VDD1.8.
32	**RBIAS**	Analog, CMOS	N/A	External 12KΩ +/- 1% bias resistor to ground.
	GND FLAG	Ground	N/A	Ground. The flag must be connected to the ground plane with a via array under the exposed flag. This is the main ground for the IC.

Application Diagrams

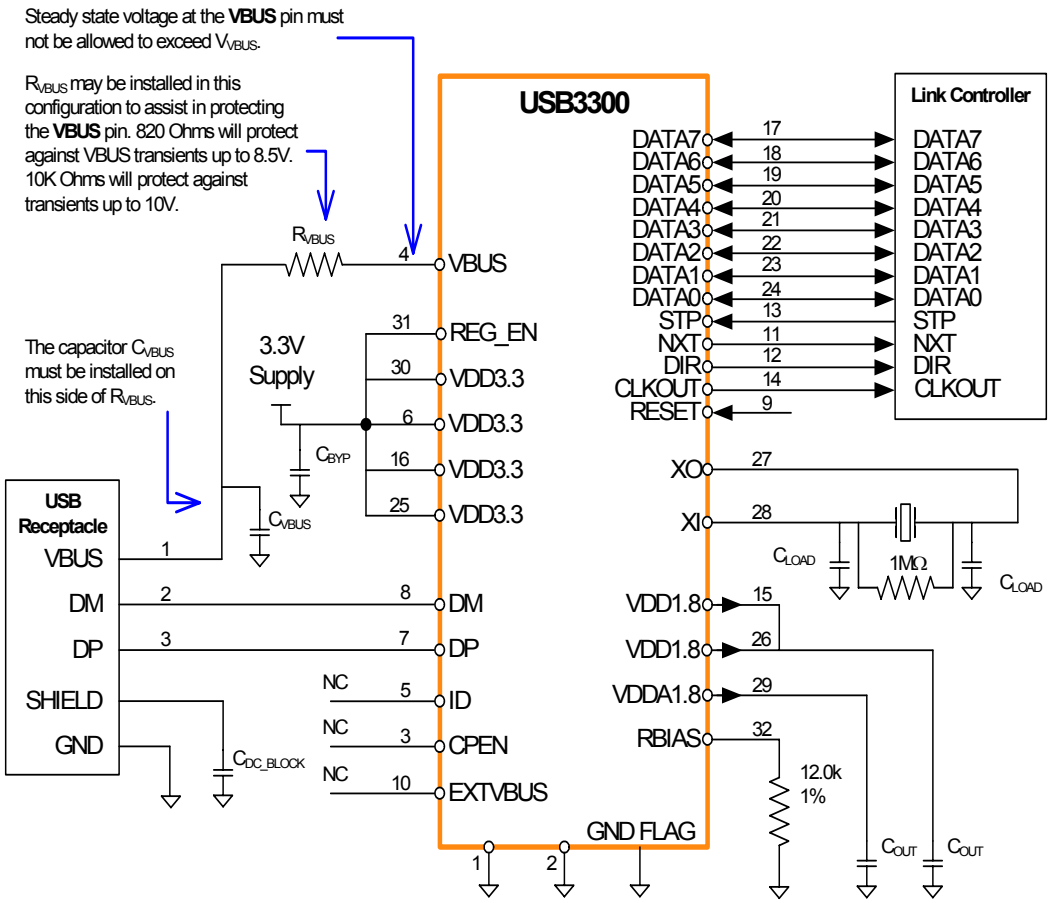

Figure 5 USB3300 Application Diagram (Peripheral)

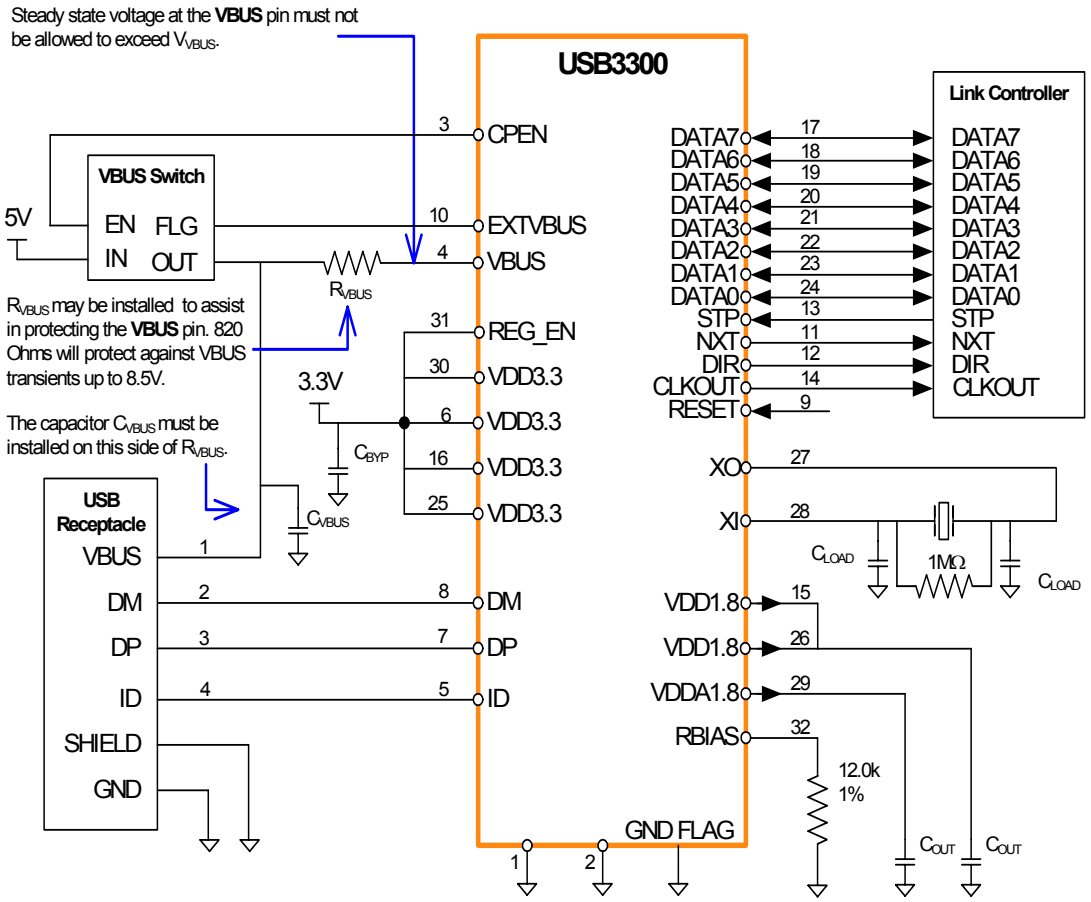

Figure 6 USB3300 Application Diagram (Host or OTG)

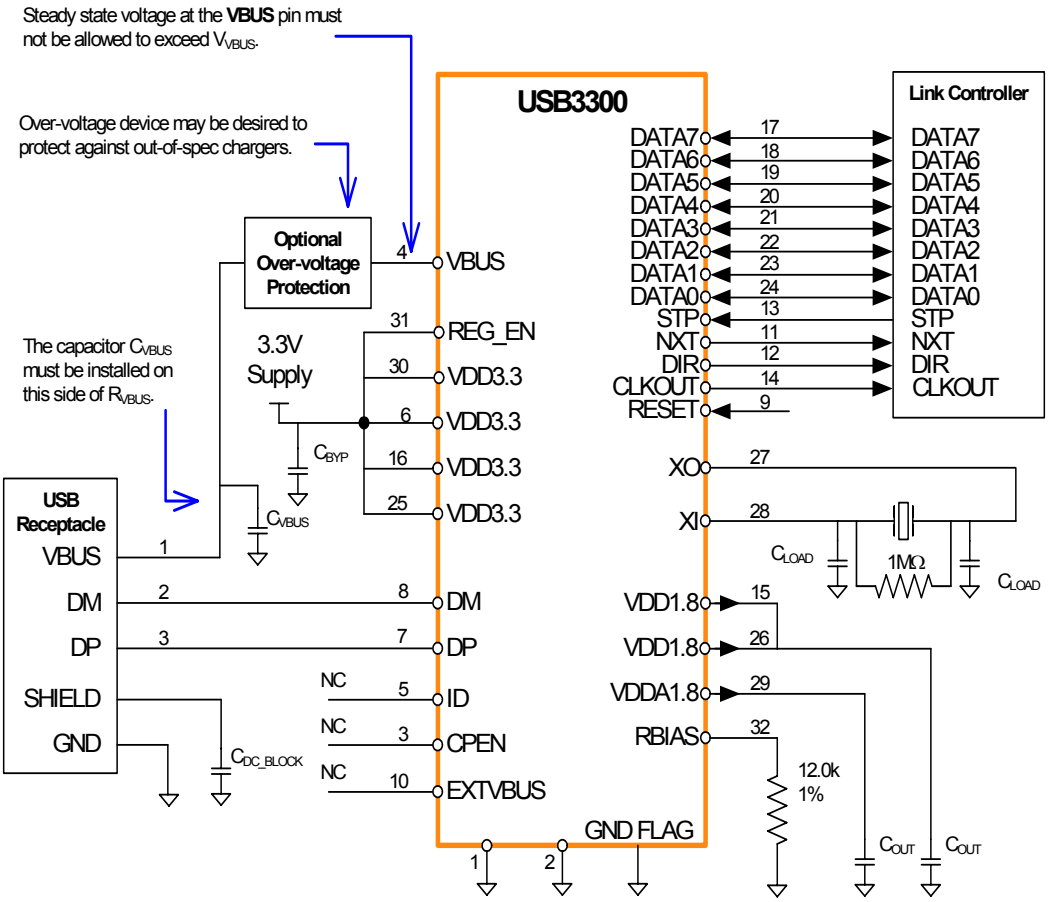

Figure 7 USB3300 Application Diagram (Peripheral with Over Voltage Protection)

Multi-Port Applications

To support multiple ports a single USB3300 host can be combined with one of SMSC's many hub products to expand the number of ports. SMSC has 2-port, 3-port, 4-port, and 7-port hub designs which can be used to expand the number of ports in a design.

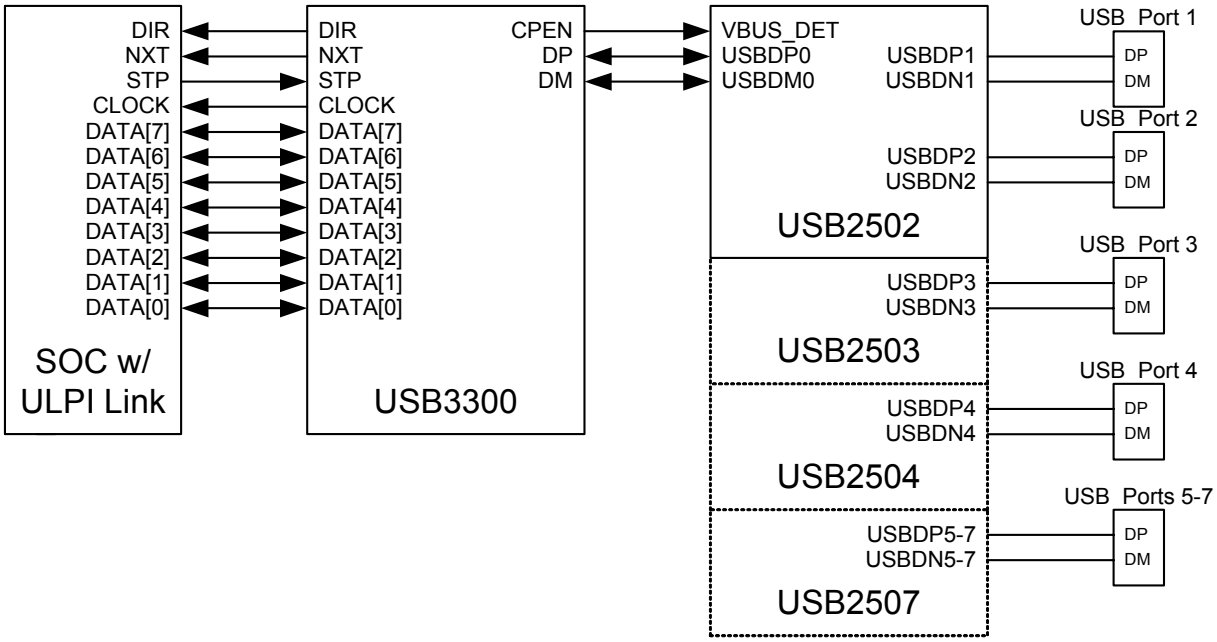

Figure 8 Expanding Downstream Ports for USB3300 Host Applications

Using a SMSC hub to expand the number of ports allows a single Link to run several USB devices without a separate Link to support each USB port. Another advantage of using a SMSC hub is on products where the main board is not located near the USB ports. The USB3300 can be placed on the main board with the Link ASIC and the hub can be placed on a separate board next to the USB ports. The only data connection required between the boards is DP and DM.

The CPEN output of the USB3300 is optional and can be used to turn the Hub on or off to lower current when the USB connection isn't needed.

Evaluation Board

An evaluation board, EVB-USB3300, is available for building a prototype system with the USB3300. The evaluation board provides an industry standard T&MT connector to interface a ULPI Link controller and a Mini-AB connector for the USB cable. A 500mA fault protected 5V Vbus switch that is controlled by the USB3300 is also included.

Supporting Documentation

- Universal Serial Bus Specification, Revision 2.0, April 27, 2000
- On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a, June 24, 2003
- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Version 1.02, May 27, 2000
- UTMI+ Specification, Revision 1.0, February 2, 2004
- UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1

Package Outline

The USB3300 is offered in a compact 32 lead-free QFN package.

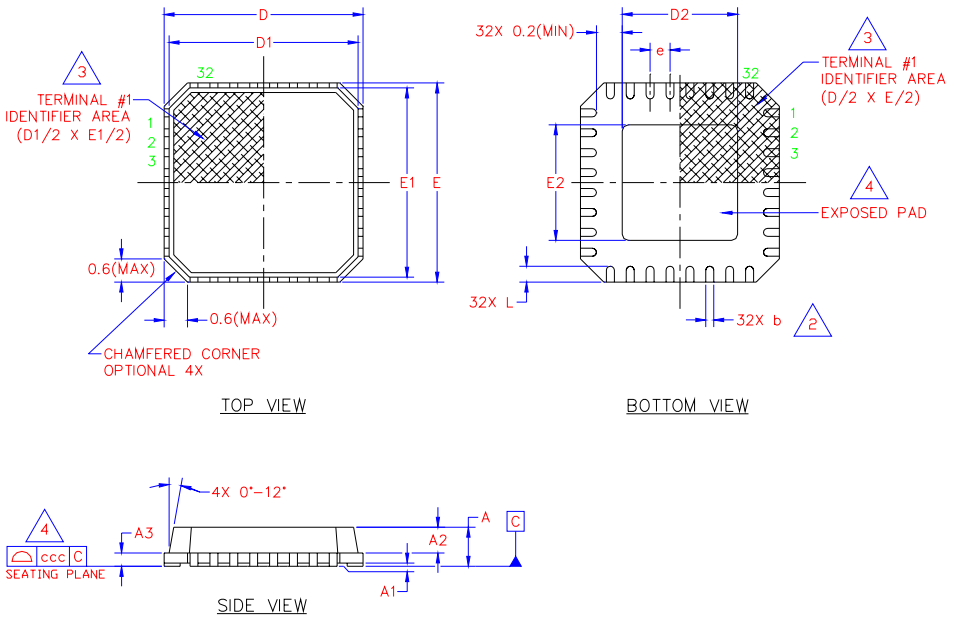

Figure 9 USB3300-EZK 32 Pin QFN Package Outline, 5 x 5 x 0.9 mm Body (Lead-Free)

Table 2 32 Terminal QFN Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	0.70	~	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A2	~	~	0.90	Mold Thickness
A3		0.20 REF		Copper Lead-frame Substrate
D	4.85	5.0	5.15	X Overall Size
D1	4.55	~	4.95	X Mold Cap Size
D2	3.15	3.3	3.45	X exposed Pad Size
E	4.85	5.0	5.15	Y Overall Size
E1	4.55	~	4.95	Y Mold Cap Size
E2	3.15	3.3	3.45	Y exposed Pad Size
L	0.30	~	0.50	Terminal Length
e		0.50 BSC		Terminal Pitch
b	0.18	0.25	0.30	Terminal Width
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Dimension b applies to plated terminals and is measured between 0.15mm and 0.30mm from the terminal tip. Tolerance on the true position of the leads is ± 0.05 mm at maximum material conditions (MMC).
3. Details of terminal #1 identifier are optional but must be located within the zone indicated.
4. Coplanarity zone applies to exposed pad and terminals.