National Semiconductor

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DS90C363B
+3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link -65 MHz

General Description

The DS90C363B transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 170 Mbytes/sec. The DS90C363B transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe Receiver (DS90CF366) without any translation logic.

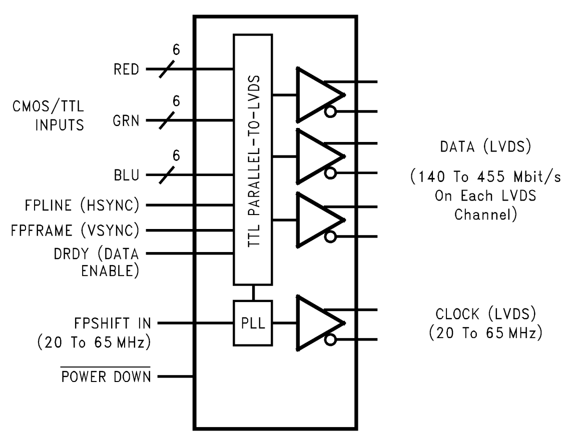
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- No special start-up sequence required between clock/data and /PD pins. Input signal (clock and data) can be applied either before or after the device is powered.
- Support Spread Spectrum Clocking up to 100kHz frequency modulation & deviations of ±2.5% center spread or −5% down spread.
- "Input Clock Detection" feature will pull all LVDS pairs to logic low when input clock is missing and when /PD pin is logic high.
- 18 to 68 MHz shift clock support
- Best–in–Class Set & Hold Times on TxINPUTs
- Tx power consumption < 130 mW (typ) @65MHz Grayscale
- 40% Less Power Dissipation than BiCMOS Alternatives
- Tx Power-down mode < 37μW (typ)
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- Narrow bus reduces cable size and cost
- Up to 1.3 Gbps throughput
- Up to 170 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 48-lead TSSOP package
- Improved replacement for: SN75LVDS84, DS90C363A

Block Diagram

DS90C363B



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Order Number DS90C363BMT
See NS Package Number MTD48

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
MTD48 (TSSOP) Package:	
DS90C363B	1.98 W
Package Derating:	
DS90C363B	16 mW/˚C above +25˚C
ESD Rating	
(HBM, 1.5 kΩ, 100 pF)	7 kV
(EIAJ, 0Ω, 200 pF)	500V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Supply Noise Voltage (V_{CC})			200	mV_{PP}
TxCLKIN frequency	18		68	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	μA
		V_{IN} = GND		−10	0		μA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (Note 4)			1.13	1.25	1.38	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)* " Typ " values are given for V_{CC} = 3.6V and T_A = +25˚C, " Max " values are given for V_{CC} = 3.6V and T_A = −10˚C	f = 25MHz		29	40	mA
			f = 40 MHz		34	45	mA
			f = 65 MHz		42	55	mA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
ICCTG	Transmitter Supply Current 16 Grayscale	$R_L = 100\Omega$, $C_L = 5$ pF, 16 Grayscale Pattern *(Figures 2, 4)* " Typ " values are given for $V_{CC} = 3.6V$ and $T_A = +25^{\circ}C$, " Max " values are given for $V_{CC} = 3.6V$ and $T_A = -10^{\circ}C$	f = 25 MHz		28	40	mA
			f = 40 MHz		32	45	mA
			f = 65 MHz		39	50	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE® under Power Down Mode			11	150	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{CC} = 3.3V$ and $T_A = +25^{\circ}C$ unless specified otherwise.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time *(Figure 5)*			5	ns
TCIP	TxCLK IN Period *(Figure 6)*	14.7	T	50	ns
TCIH	TxCLK IN High Time *(Figure 6)*	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 6)*	0.35T	0.5T	0.65T	ns
TXIT	TxIN, and $\overline{\text{Power Down}}$ pin transition Time	1.5		6.0	ns
TXPD	Minimum pulse width for $\overline{\text{Power Down}}$ pin signal	1			us

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 4)*			0.75	1.4	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 4)*			0.75	1.4	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 11)* (Note 5)	f = 65 MHz	–0.20	0	+0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		2.00	2.20	2.40	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.20	4.40	4.60	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.39	6.59	6.79	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.59	8.79	8.99	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.79	10.99	11.19	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.99	13.19	13.39	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 11)* (Note 5)	f = 40 MHz	–0.25	0	+0.25	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		3.32	3.57	3.82	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.89	7.14	7.39	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		10.46	10.71	10.96	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		14.04	14.29	14.54	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17.61	17.86	18.11	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		21.18	21.43	21.68	ns

Transmitter Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 11)* (Note 5)	f = 25 MHz	−0.45	0	+0.45	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		5.26	5.71	6.16	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		10.98	11.43	11.88	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		16.69	17.14	17.59	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		22.41	22.86	23.31	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		28.12	28.57	29.02	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		33.84	34.29	34.74	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 6)*		2.5			ns
THTC	TxIN Hold to TxCLK IN *(Figure 6)*		0.5			ns
TCCD	TxCLK IN to TxCLK OUT Delay *(Figure 7)* 50% duty cycle input clock is assumed, T_A= −10˚C, and 65MHz for " Min ", T_A= 70˚C, and 25MHz for " Max ", V_{CC}= 3.6V, R_FB = V_{CC}		3.340		7.211	ns
	TxCLK IN to TxCLK OUT Delay *(Figure 7)* 50% duty cycle input clock is assumed, T_A= −10˚C, and 65MHz for " Min ", T_A= 70˚C, and 25MHz for " Max ", V_{CC}= 3.6V, R_FB = GND		3.011		6.062	ns
SSCG	Spread Spectrum Clock support; Modulation frequency with a linear profile (Note 6)	f = 25 MHz		100kHz ± 2.5%/−5%		
		f = 40 MHz		100kHz ± 2.5%/−5%		
		f = 65 MHz		100kHz ± 2.5%/−5%		
TPLLS	Transmitter Phase Lock Loop Set *(Figure 8)*				10	ms
TPDD	Transmitter Power Down Delay *(Figure 10)*				100	ns

Note 5: The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

Note 6: Care must be taken to ensure TSTC and THTC are met so input data are sampling correctly. This SSCG parameter only shows the performance of tracking Spread Spectrum Clock applied to TxCLK IN pin, and reflects the result on TxCLKOUT+ and TxCLK− pins.

AC Timing Diagrams

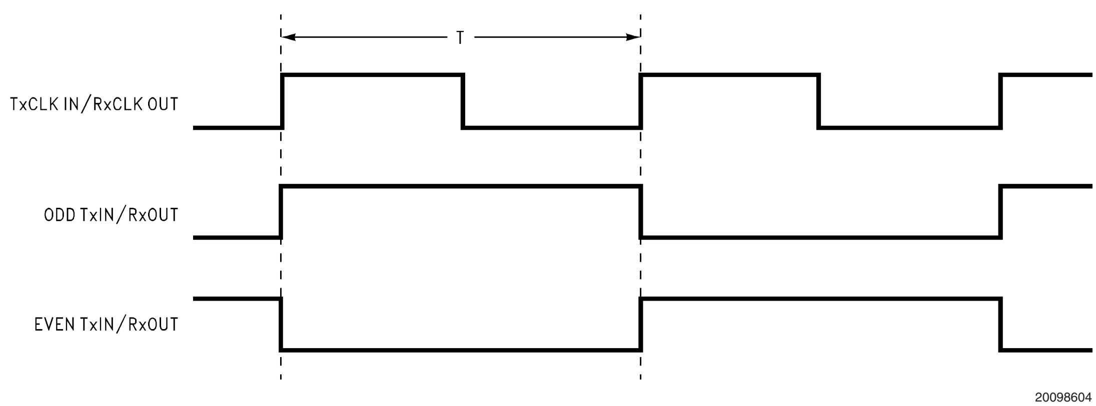


FIGURE 1. "Worst Case" Test Pattern

AC Timing Diagrams (Continued)

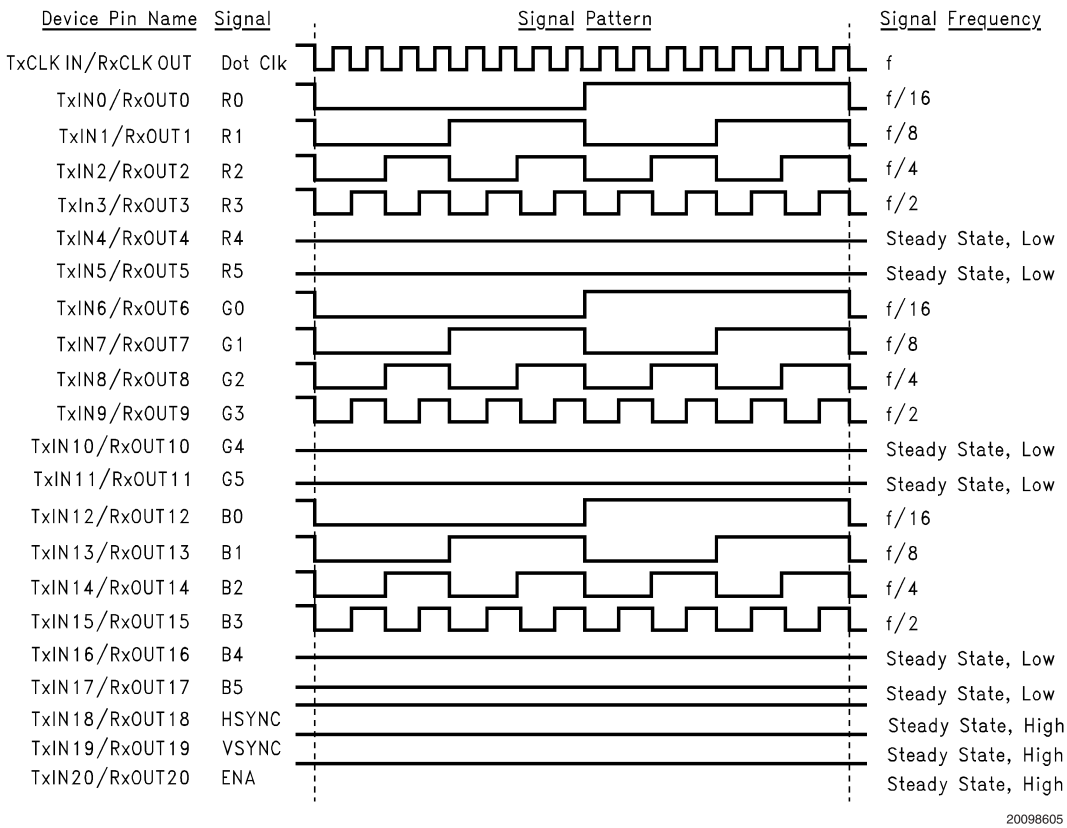


FIGURE 2. "16 Grayscale" Test Pattern (Notes 7, 8, 9, 10)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: *Figures 1, 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 10: Recommended pin to signal mapping. Customer may choose to define differently.

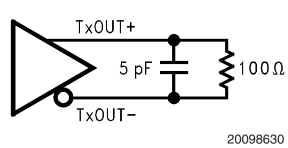


FIGURE 3. DS90C363B (Transmitter) LVDS Output Load

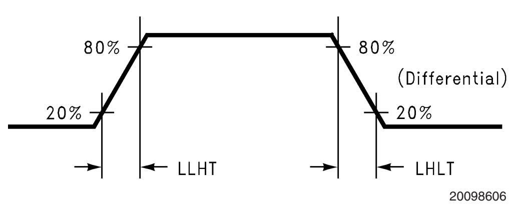


FIGURE 4. DS90C363B (Transmitter) LVDS Transition Times

AC Timing Diagrams (Continued)

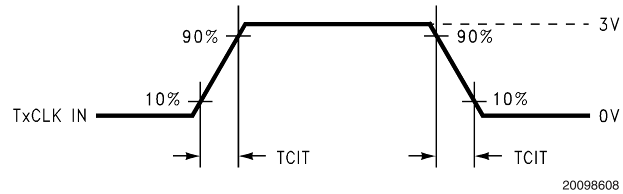


FIGURE 5. DS90C363B (Transmitter) Input Clock Transition Time

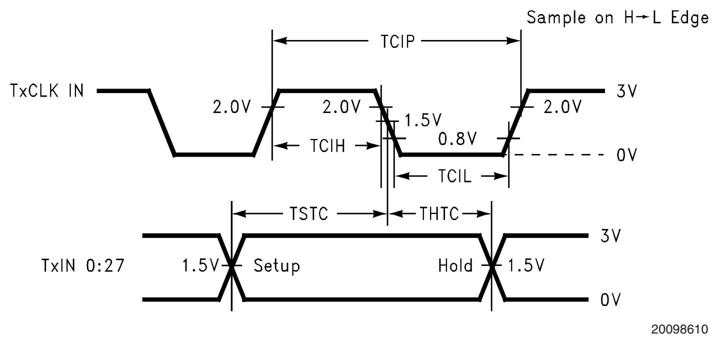


FIGURE 6. DS90C363B (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

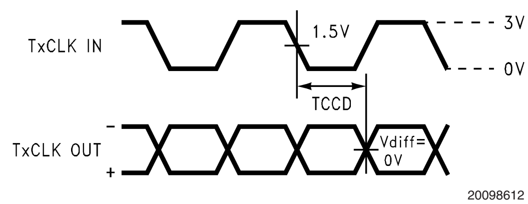


FIGURE 7. DS90C363B (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

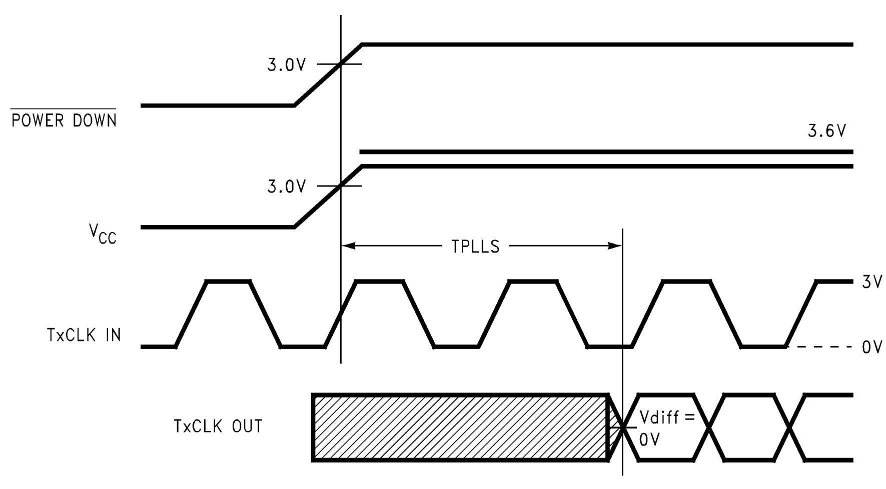


FIGURE 8. DS90C363B (Transmitter) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

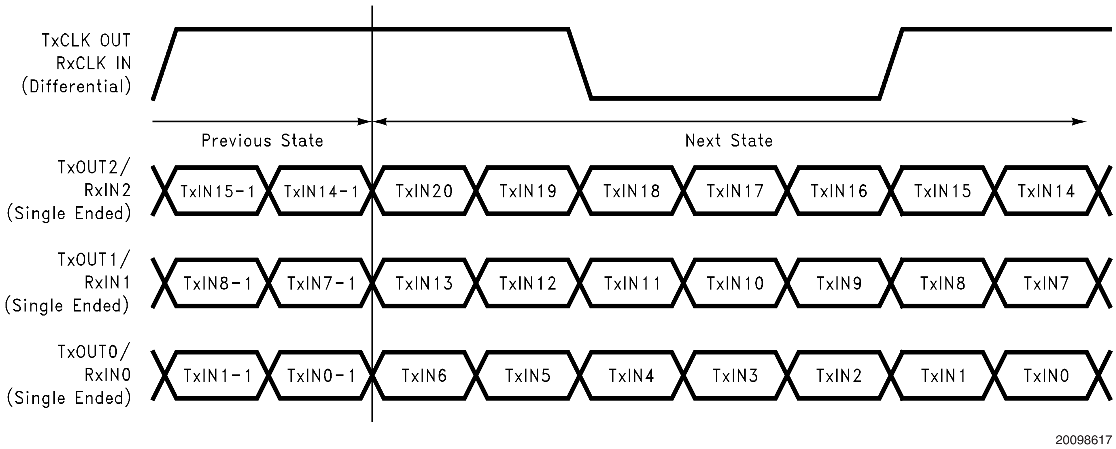


FIGURE 9. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

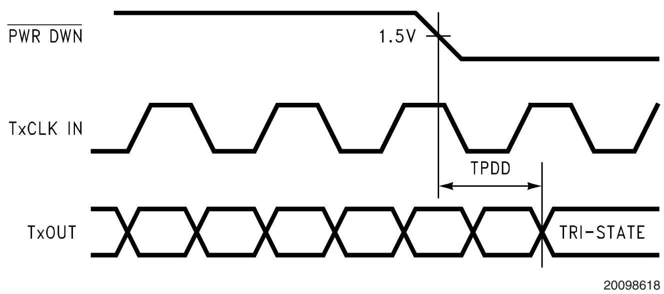


FIGURE 10. Transmitter Power Down Delay

AC Timing Diagrams (Continued)

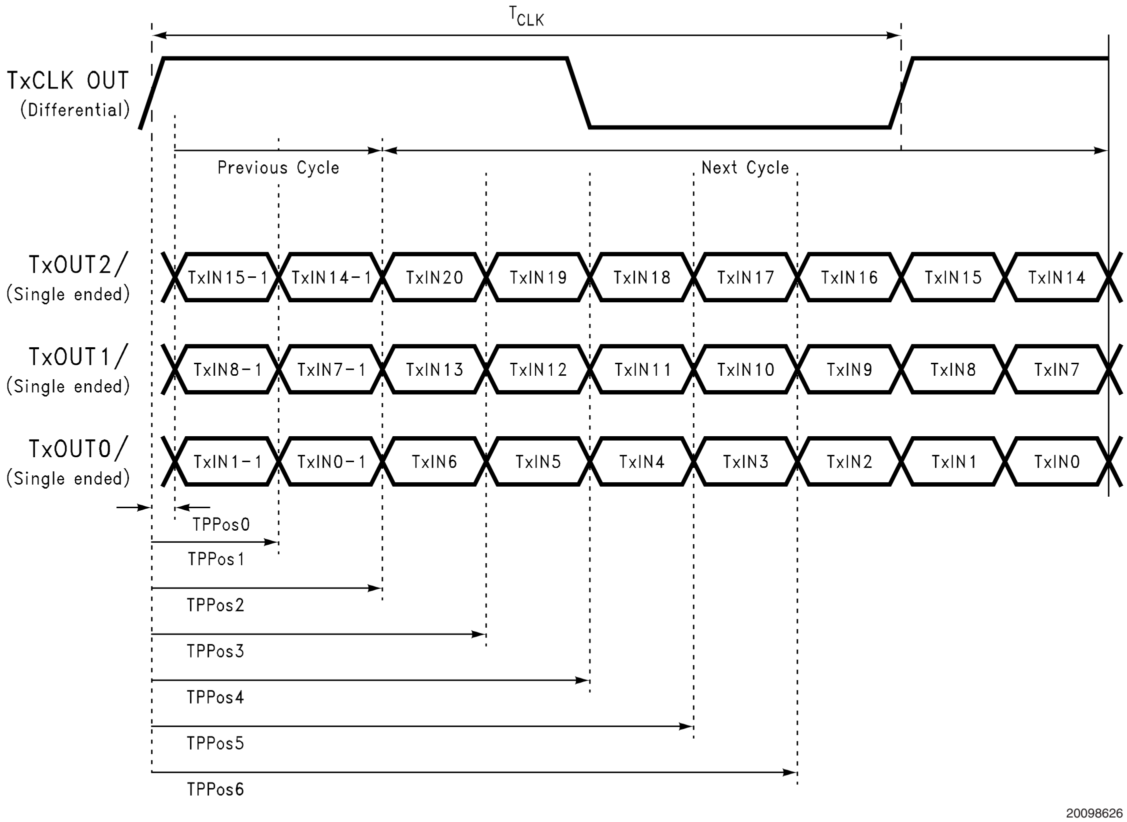


FIGURE 11. Transmitter LVDS Output Pulse Position Measurement

DS90C363B Pin Descriptions — FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	3	Positive LVDS differential data output.
TxOUT−	O	3	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select (See Table 1).
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. See Applications Information section.
V_{CC}	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.
NC		1	No connect

Applications Information

The DS90C363B are backward compatible with the DS90C363/DS90CF363, DS90C363A/DS90CF363A and are a pin-for-pin replacement.

This device may also be used as a replacement for the DS90CF563 (5V, 65MHz) and DS90CF561 (5V, 40MHz) FPD-Link Transmitters with certain considerations/ modifications:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of the transmitter.
2. To implement a falling edge device for the DS90C363B, the R_FB pin (pin 14) may be tied to ground OR left unconnected (an internal pull-down resistor biases this pin low). Biasing this pin to Vcc implements a rising edge device.

TRANSMITTER INPUT PINS

The DS90C363B transmitter input and control inputs accept 3.3V LVTTL/LVCMOS levels. They are not 5V tolerant.

TRANSMITTER INPUT CLOCK/DATA SEQUENCING

The DS90C363B does not require any special requirement for sequencing of the input clock/data and PD (PowerDown) signal. The DS90C363B offers a more robust input sequencing feature where the input clock/data can be inserted after the release of the PD signal. In the case where the clock/ data is stopped and reapplied, such as changing video mode within Graphics Controller, it is not necessary to cycle the PD signal. However, there are in certain cases where the PD may need to be asserted during these mode changes. In cases where the source (Graphics Source) may be supplying an unstable clock or spurious noisy clock output to the LVDS transmitter, the LVDS Transmitter may attempt to lock onto this unstable clock signal but is unable to do so due the instability or quality of the clock source. The PD signal in these cases should then be asserted once a stable clock is applied to the LVDS transmitter. Asserting the PWR DOWN pin will effectively place the device in reset and disable the PLL, enabling the LVDS Transmitter into a power saving standby mode. However, it is still generally a good practice to assert the PWR DOWN pin or reset the LVDS transmitter whenever the clock/data is stopped and reapplied but it is not mandatory for the DS90C363B.

SPREAD SPECTRUM CLOCK SUPPORT

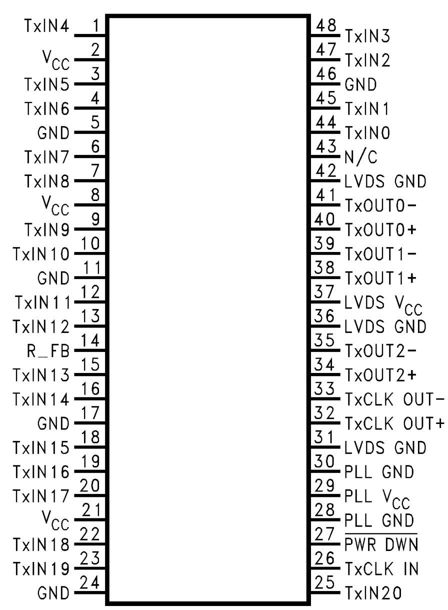
The DS90C363B can support Spread Spectrum Clocking signal type inputs. The DS90C383B outputs will accurately track Spread Spectrum Clock/Data inputs with modulation frequencies of up to 100kHz (max.)with either center spread of ±2.5% or down spread -5% deviations.

POWER SOURCES SEQUENCE

In typical applications, it is recommended to have V_{CC}, LVDS V_{CC} and PLL V_{CC} from the same power source with three separate de-coupling bypass capacitor groups. There is no requirement on which VCC entering the device first.

Pin Diagram

DS90C363B



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Typical Application

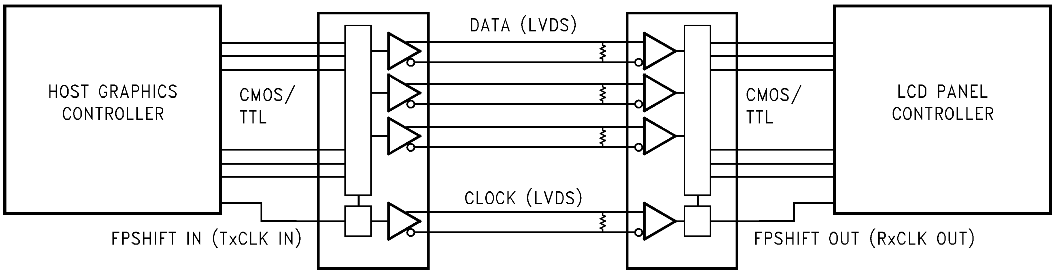

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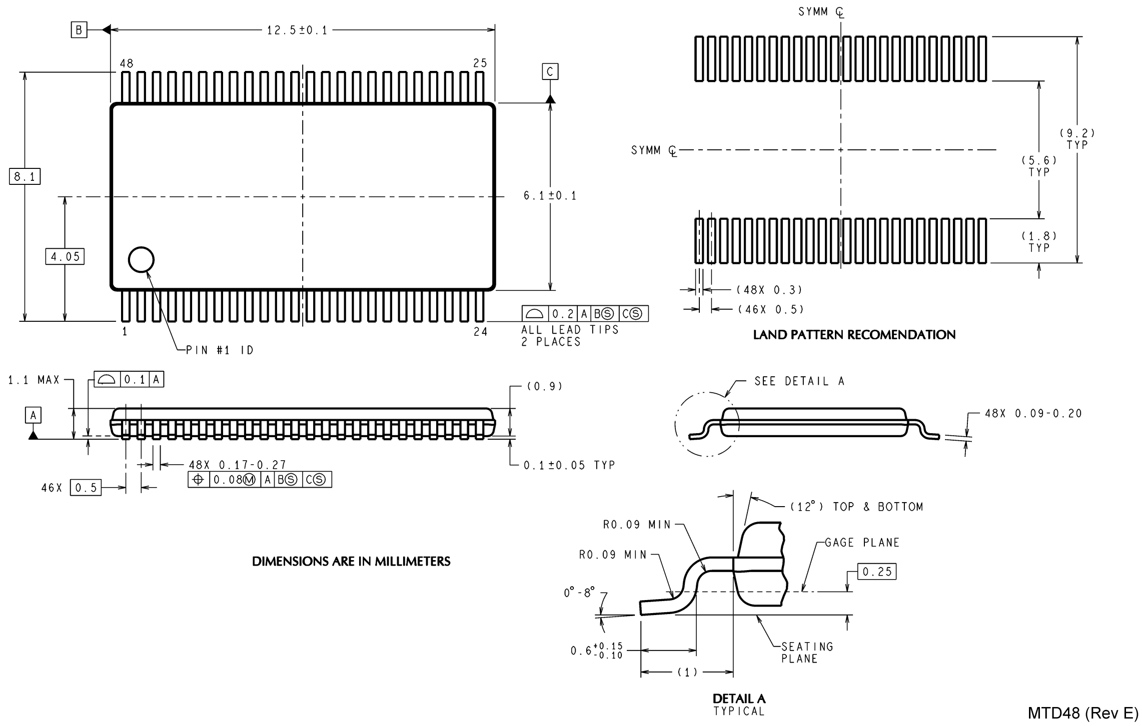
TABLE 1. Programmable Transmitter (DS90C363B)

Pin	Condition	Strobe Status
R_FB	R_FB = V_{CC}	Rising edge strobe
R_FB	R_FB = GND or NC	Falling edge strobe

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90C363BMT
NS Package Number MTD48

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