National Semiconductor

February 2005

LF198QML
Monolithic Sample-and-Hold Circuits

General Description

The LF198 is a monolithic sample-and-hold circuit which utilizes BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Features

- Operates from ±5V to ±18V supplies
- Less than 10 µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 µF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

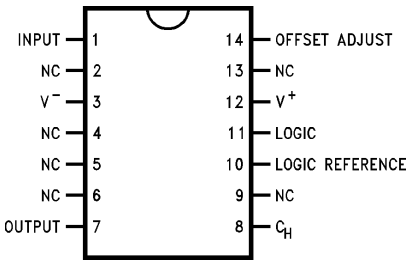
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

Ordering Information

NSC Part Number	JAN Part Number	NSC Package Number	Package Description
LF198H/883	5962–8760801GA	H08C	8LD Metal Can
LF198WG-QMLV	5962–8760801VZA	WG14A	14LD Ceramic SOIC
LF198WG/883	5962–8760801QZA	WG14A	14LD Ceramic SOIC

Connection Diagrams

Small-Outline Package



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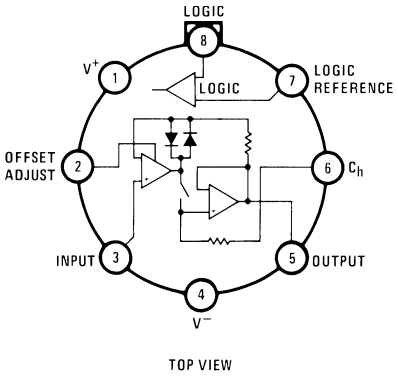
See NS Package Number WG14A

Metal Can Package



TOP VIEW

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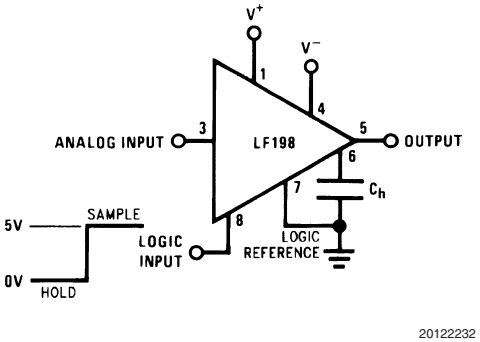
See NS Package Number H08C

Typical Connection and Performance Curve



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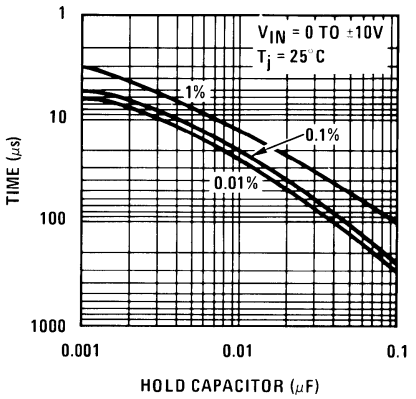
Acquisition Time



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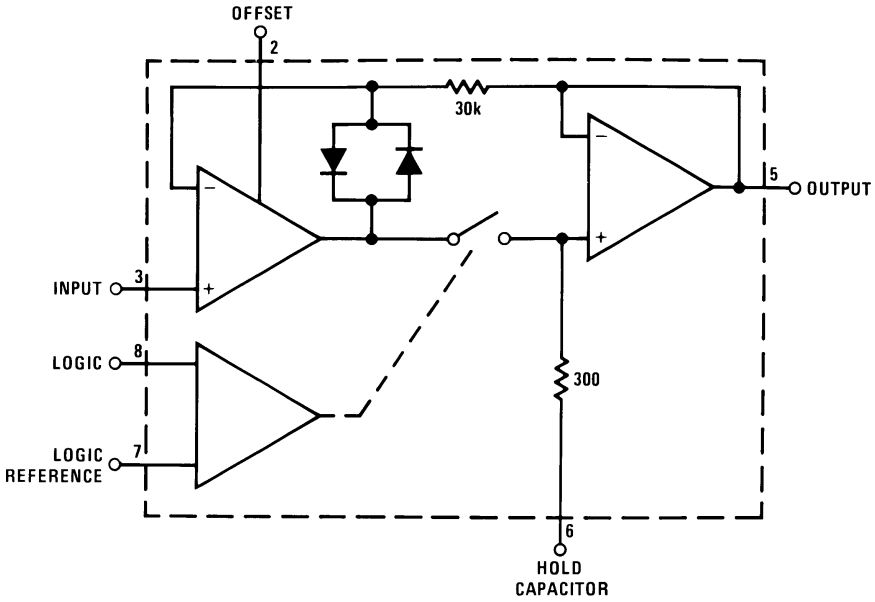
Functional Diagram



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Absolute Maximum Ratings (Note 1)

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 2)	500 mW
Operating Ambient Temperature Range	−55˚C to +125˚C
Maximum Junction Temperature (T_{Jmax})	+150˚C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 3)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 sec.)	260˚C
Thermal Resistance	
θ_{JA}	
Metal Can (Still Air @ 0.5W)	160˚C/W
Metal Can (500 LF/Min Air Flow @ 0.5W)	84˚C/W
Ceramic SOIC (Still Air @ 0.5W)	140˚C/W
Ceramic SOIC (500 LF/Min Air Flow @ 0.5W)	95˚C/W
θ_{JC}	
Metal Can	48˚C/W
Ceramic SOIC	20˚C/W
Package Weight (typical)	
Metal Can	TBD
Ceramic SOIC	415mg
ESD Tolerance (Note 7)	500V

Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temperature (˚C)
1	Static tests at	+25˚C
2	Static tests at	+125˚C
3	Static tests at	−55˚C
4	Dynamic tests at	+25˚C
5	Dynamic tests at	+125˚C
6	Dynamic tests at	−55˚C
7	Functional tests at	+25˚C
8A	Functional tests at	+125˚C
8B	Functional tests at	−55˚C
9	Switching tests at	+25˚C
10	Switching tests at	+125˚C
11	Switching tests at	−55˚C

Electrical Characteristics

The following specifications apply unless otherwise specified. V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{HOLD} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}+	Positive Supply Current	+V_{CC} = 15V, -V_{CC} = -15V			5.5	mA	1, 2
					6.5	mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Sample"			5.5	mA	1, 2
					6.5	mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Hold"			5.5	mA	1, 2
					6.5	mA	3
I_{CC}-	Negative Supply Current	+V_{CC} = 15V, -V_{CC} = -15V		-5.5		mA	1, 2
				-6.5		mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Sample"		-5.5		mA	1, 2
				-6.5		mA	3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Hold"		-5.5		mA	1, 2
				-6.5		mA	3
V_{OS}	Input Offset Voltage	+V_{CC} = 3V, -V_{CC} = -7V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 15V, -V_{CC} = -15V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -26.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 18V, -V_{CC} = -18V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -32.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 26.5V, -V_{CC} = -3.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 32.5V, -V_{CC} = -3.5V, Logic = 2.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		+V_{CC} = 7V, -V_{CC} = -3V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
I_{IB}	Input Bias Current	+V_{CC} = 3V, -V_{CC} = -7V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 15V, -V_{CC} = -15V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -32.5V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 32.5V, -V_{CC} = -3.5V		-25	25	nA	1
				-75	75	nA	2, 3
		+V_{CC} = 7V, -V_{CC} = -3V		-25	25	nA	1
				-75	75	nA	2, 3
$I_{Leak(Cap)}$	Leakage Current into Hold Capacitor	+V_{CC} = 3V, -V_{CC} = -7V	(Note 5)	-100	100	pA	1
		+V_{CC} = 3.5V, -V_{CC} = -32.5V		-100	100	pA	1
		+V_{CC} = 32.5V, -V_{CC} = -3.5V	(Note 5)	-100	100	pA	1
		+V_{CC} = 7V, -V_{CC} = -3V		-100	100	pA	1

Electrical Characteristics (Continued)

The following specifications apply unless otherwise specified. V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{HOLD} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{HS}	Hold Step	+V_{CC} = 15V -V_{CC} = -15V	(Note 4)	-2.0	2.0	mV	1
				-5.6	5.6	mV	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -26.5V	(Note 4)	-2.5	2.5	mV	1
				-5.6	5.6	mV	2, 3
		+V_{CC} = 26.5V, -V_{CC} = -3.5V	(Note 4)	-2.5	2.5	mV	1
				-5.6	5.6	mV	2, 3
A_E	Gain Error	+V_{CC} = 7V, -V_{CC} = -3V			0.02	%	1
					0.06	%	2, 3
		+V_{CC} = 3.5V, -V_{CC} = -26.5V			0.005	%	1
					0.02	%	2, 3
		+V_{CC} = 32.5V, -V_{CC} = -3.5V			0.005	%	1
					0.06	%	2, 3
		+V_{CC} = 26.5V, -V_{CC} = -3.5V			0.005	%	1
					0.02	%	2, 3
Z_I	Input Impedance	+V_{CC} = 8V, -V_{CC} = -28V		10.0		GΩ	1
				0.8		GΩ	2, 3
		+V_{CC} = 28V, -V_{CC} = -8V		10.0		GΩ	1
				0.8		GΩ	2, 3
Z_O	Output Impedance	+V_{CC} = 18V, -V_{CC} = -18V			2.0	Ω	1
					4.0	Ω	2, 3
I_{Charge}	Capacitor Charging Current	+V_{CC} = 8V, -V_{CC} = -28V		-25	-4.5	mA	1
				-25	-3.0	mA	2, 3
		+V_{CC} = 28V, -V_{CC} = -8V		4.5	25	mA	1
				3.0	25	mA	2, 3
Logic	Logic Pin Current	+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Sample", Logic = 7V			10	µA	1, 2, 3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Hold", Logic = -30V			1.0	µA	1
					0.5	µA	2, 3
V_{OS}	Input Offset Voltage	+V_{CC} = 15V, -V_{CC} = -15V, I_{Drive} = +1mA		-3.5	3.5	mV	1
				-6.0	6.0	mV	2, 3
Delta V_{OS}	Input Offset Voltage	+V_{CC} = 15V, -V_{CC} = -15V, I_{Drive} = +1mA to -1mA		-1.1	1.1	mV	1
				-2.0	2.0	mV	2, 3
I_{OS}+	Output Short Circuit Current	+V_{CC} = 18V, -V_{CC} = -18V		7.0	20	mA	1
I_{OS}-	Output Short Circuit Current	+V_{CC} = 18V, -V_{CC} = -18V		-25	-7.0	mA	1
$I_{LogicRef}$	Logic Reference Pin Current	+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Sample", Logic = 7V		-1.0	1.0	µA	1
				-0.5	5.0	µA	2, 3
		+V_{CC} = 18V, -V_{CC} = -18V, Mode = "Hold", Logic = -30V			10	µA	1, 2, 3
PSRR	Power Supply Rejection Ratio	+V_{CC} = 10V, -V_{CC} = -15V		80		dB	1
				74		dB	2, 3
		+V_{CC} = 15V, -V_{CC} = -10V		80		dB	1
				74		dB	2, 3
FTRR	Feed Through Rejection Ratio	+V_{CC} = 3.5V, -V_{CC} = -32.5V		86		dB	1
				74		dB	2, 3
		+V_{CC} = 32.5V, -V_{CC} = -3.5V		86		dB	1
				74		dB	2, 3
V_{TH}	Differential Logic Level		(Note 8)	0.8	2.4	V	1

Electrical Characteristics (Continued)

The following specifications apply unless otherwise specified. V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{HOLD} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OS} (2nd Stg)	2nd Stage V_{OS}	+V_{CC} = 3.5V, -V_{CC} = -32.5V		-35	+35	mV	1
				-50	+50	mV	2, 3
		+V_{CC} = 3V, -V_{CC} = -7V		-35	+35	mV	1
				-50	+50	mV	2, 3
		+V_{CC} = 32.5V, -V_{CC} = -3.5V		-35	+35	mV	1
				-50	+50	mV	2, 3
		+V_{CC} = 7V, -V_{CC} = -3V		-35	+35	mV	1
				-50	+50	mV	2, 3

AC Parameters

The following specifcations apply unless otherwise specified. V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{Hold} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
T_{AQ}	Acquisition Time	Delta V_{OUT} = 10V, C_{Hold} = 1000pF			6.0	µS	4
		Delta V_{OUT} = 10V, C_{Hold} = 0.01µF			25	µS	4

DC Parameters: Drift Values

The following conditions apply to all the following parameters, unless otherwise specified. V_{CC} = ±15V, R_L = 10KΩ, V_{IN} = 0V, C_{Hold} = 0.01 µF, Logic Reference Pin = 0V, Logic Pin = 4V Deltas required for S-Level product ONLY.

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OS}	Input Offset Voltage	+V_{CC} = 15V, -V_{CC} = -15V		-0.5	0.5	mV	1
I_{IB}	Input Bias Current	+V_{CC} = 15V, -V_{CC} = -15V		-2.5	2.5	nA	1

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. .

Note 3: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a junction temperature of 25˚C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25˚C value for each 11˚C increase in chip temperature. Leakage is guaranteed over full input signal range.

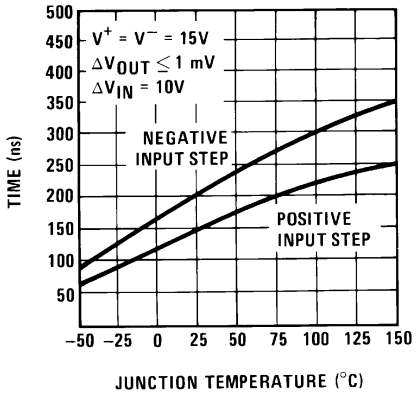
Note 6: See Definition of Terms

Note 7: Human body model, 100pF discharged through 1.5KΩ

Note 8: Parameter tested go no go only for Vth test.

Typical Performance Characteristics

Aperture Time
(Note 6)



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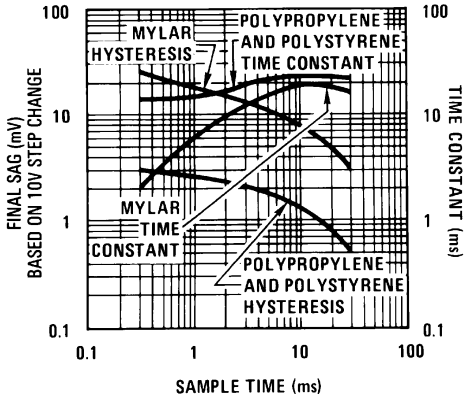
Dielectric Absorption Error in Hold Capacitor



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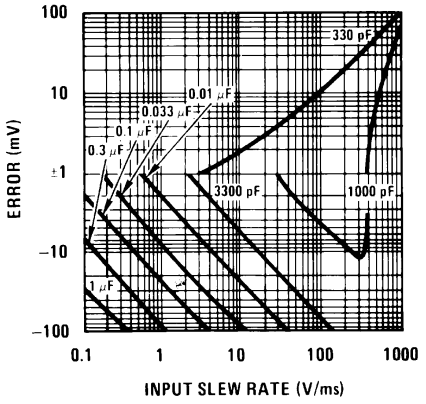
Dynamic Sampling Error



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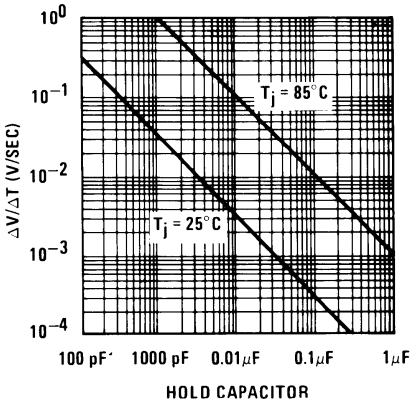
Output Droop Rate



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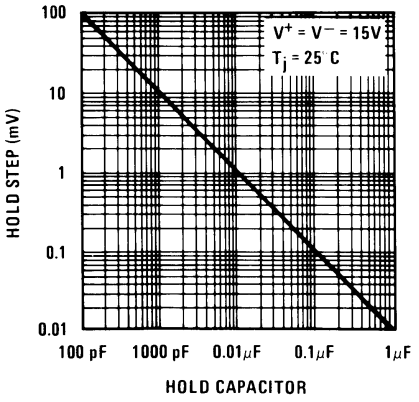
Hold Step



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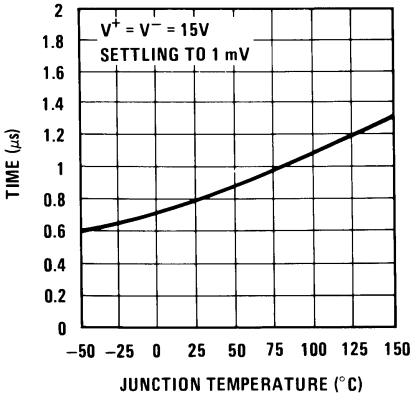
"Hold" Settling Time
(Note 6)



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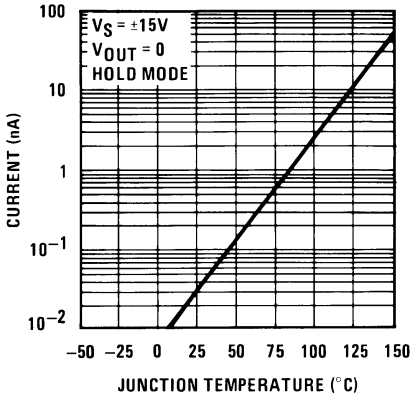
Typical Performance Characteristics (Continued)

Leakage Current into Hold Capacitor



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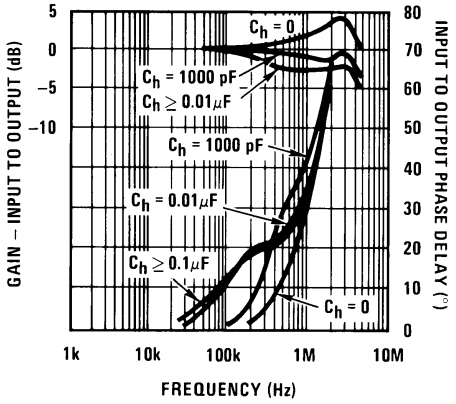
Phase and Gain (Input to Output, Small Signal)



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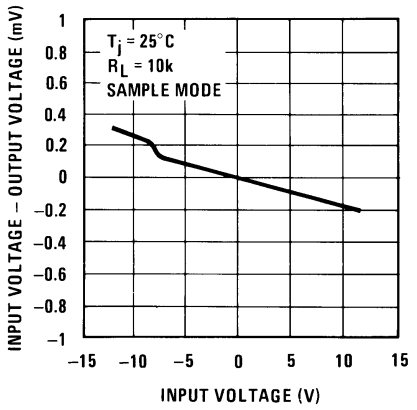
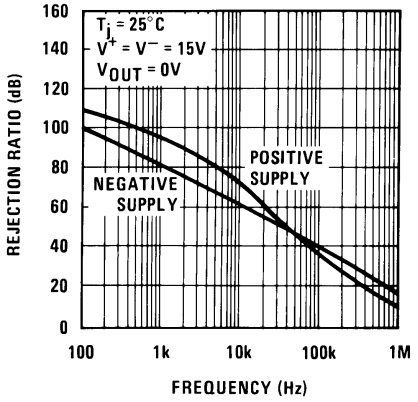
Gain Error



20122225

Power Supply Rejection



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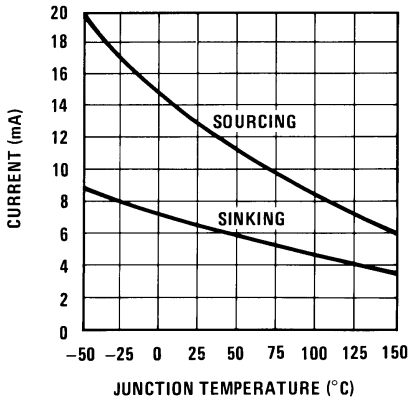
Output Short Circuit Current



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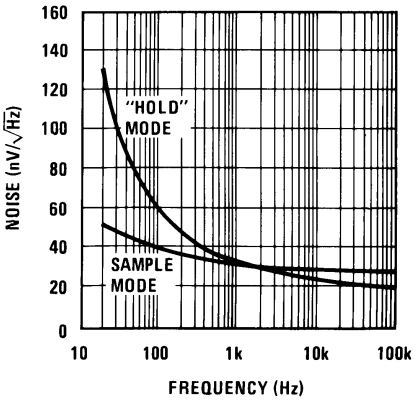
Output Noise



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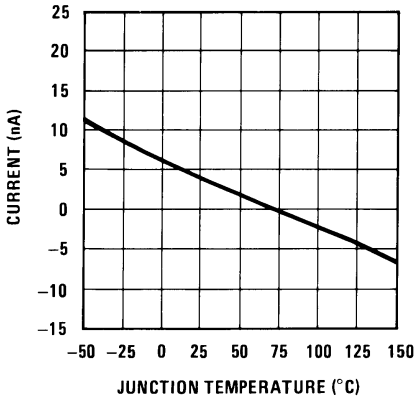
Note 9: See Definition

Typical Performance Characteristics (Continued)

Input Bias Current



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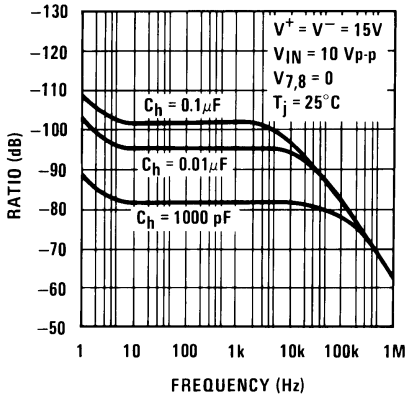
Feedthrough Rejection Ratio (Hold Mode)



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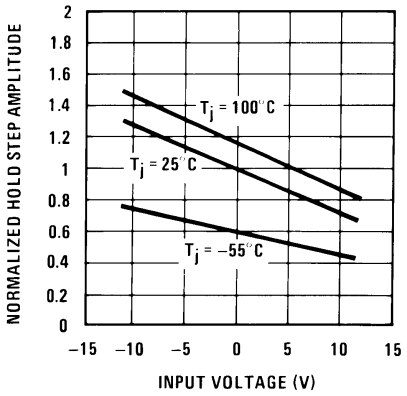
Hold Step vs Input Voltage



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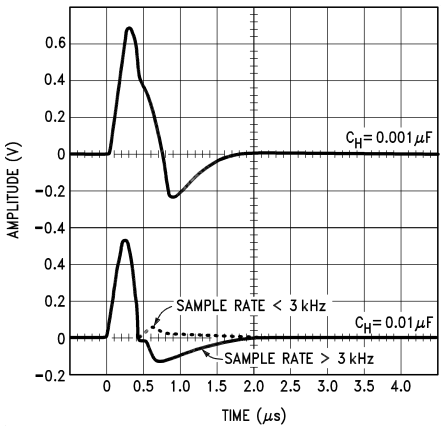
Output Transient at Start of Sample Mode



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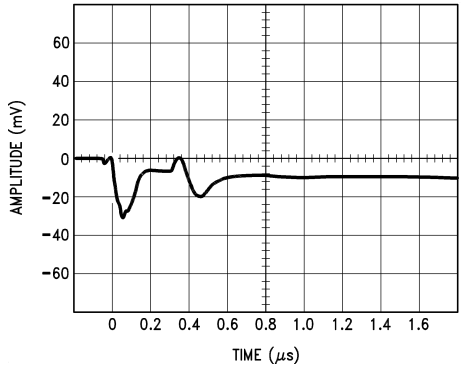
Output Transient at Start of Hold Mode



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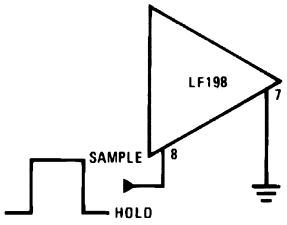
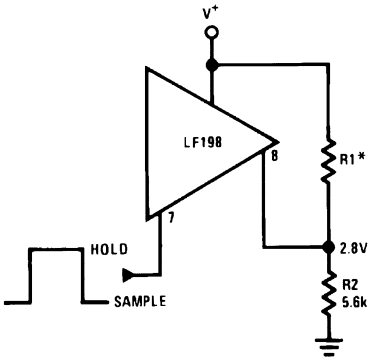
Logic Input Configurations

TTL & CMOS
3V ≤ V_{LOGIC} (Hi State) ≤ 7V



20122233

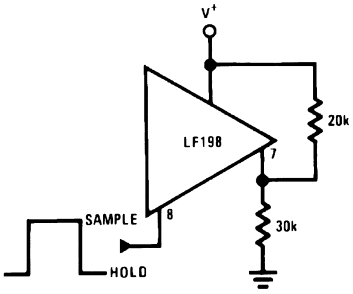
Threshold = 1.4V



20122234

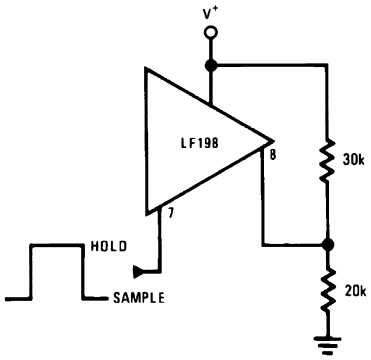
Threshold = 1.4V*Select for 2.8V at pin 8

CMOS
7V ≤ V_{LOGIC} (Hi State) ≤ 15V



20122235

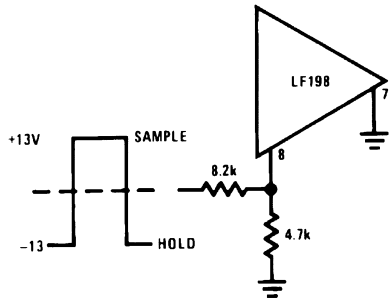
Threshold = 0.6 (V^+) + 1.4V



20122236

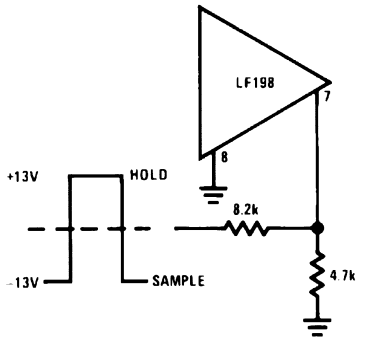
Threshold = 0.6 (V^+) – 1.4V

Op Amp Drive



20122237

Threshold ≈ +4V



20122238

Threshold = –4V

Application Hints

HOLD CAPACITOR

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85˚C to 100˚C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic "NPO" or "COG" capacitors are now available for 125˚C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error.* The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC AND AC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 µF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

LOGIC RISE TIME

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/µs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/µs.

SAMPLING DYNAMIC SIGNALS

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/µs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 µs) (0.6V/µs) = 60 mVerror if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 µs) (0.6 V/µs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

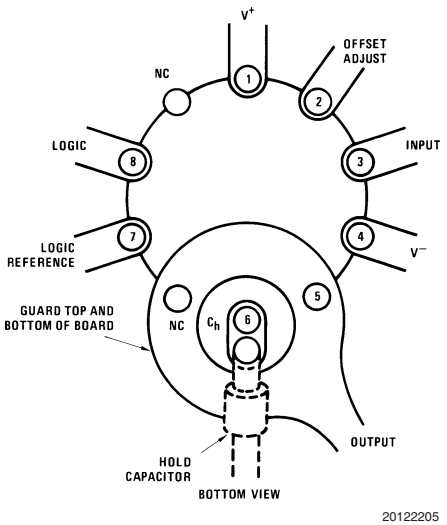
A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the "hold" command.

DIGITAL FEEDTHROUGH

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the C_h pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Guarding Technique

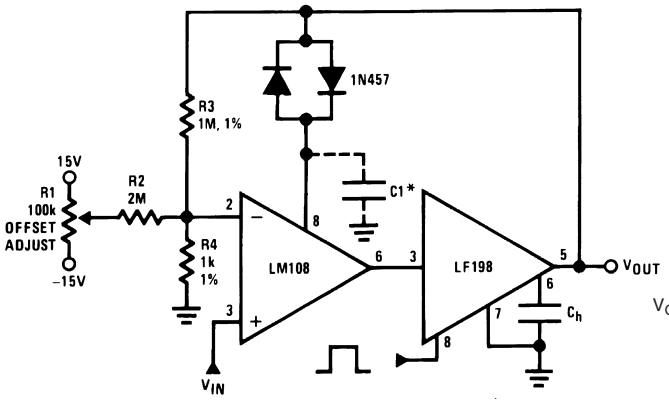


20122205

Use 10-pin layout. Guard around C_h is tied to output.

Typical Applications

X1000 Sample & Hold

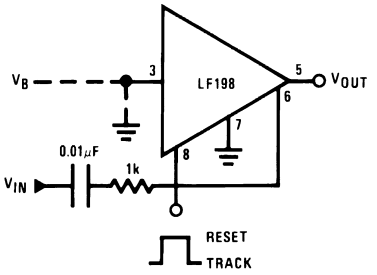


20122239

*For lower gains, the LM108 must be frequency compensated

$$\text{Use} \approx \frac{100}{A_V}\ \text{pF from comp 2 to ground}$$

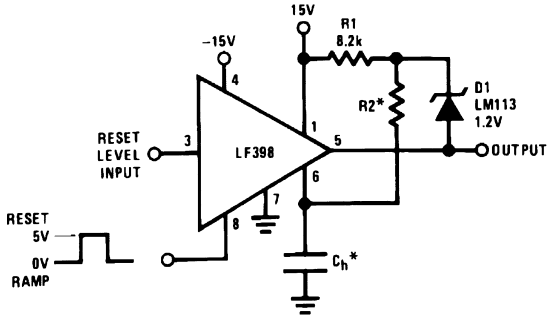
Sample and Difference Circuit (Output Follows Input in *Hold* Mode)



20122240

$$V_{OUT} = V_B + \Delta V_{IN}(\text{HOLD MODE})$$

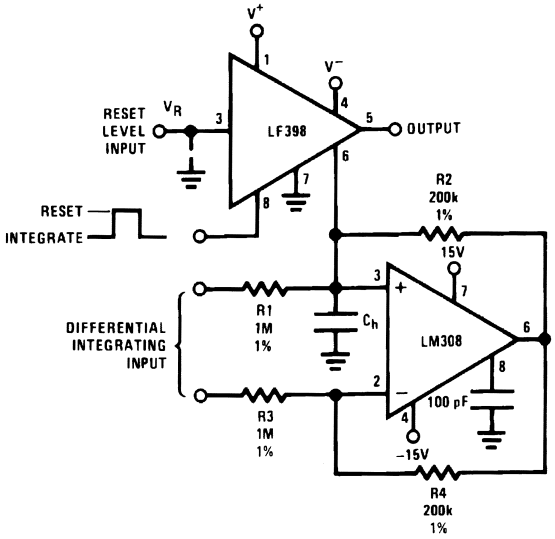
Ramp Generator with Variable Reset Level



20122242

*Select for ramp rate $\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)\ (C_h)}$
R2 ≥ 10k

Integrator with Programmable Reset Level

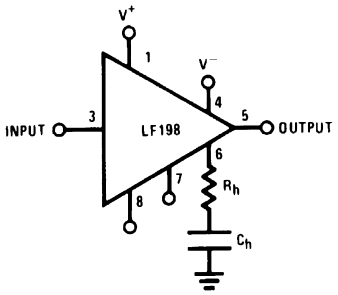


20122243

$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)\ (C_h)} \int_0^t V_{IN}\ dt\right] + \left[V_R\right]$$

Typical Applications (Continued)

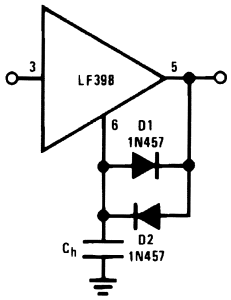
Output Holds at Average of Sampled Input



20122246

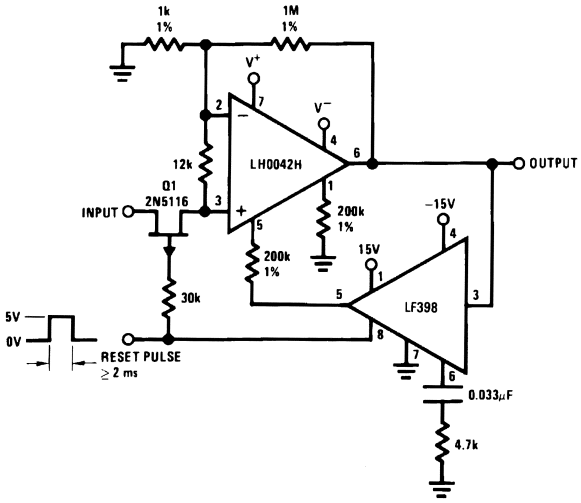
$$\text{Select } (R_h)\,(C_h) \gg \frac{1}{2\pi f_{IN}\,(\text{Min})}$$

Increased Slew Current



20122247

Reset Stabilized Amplifier (Gain of 1000)



20122249

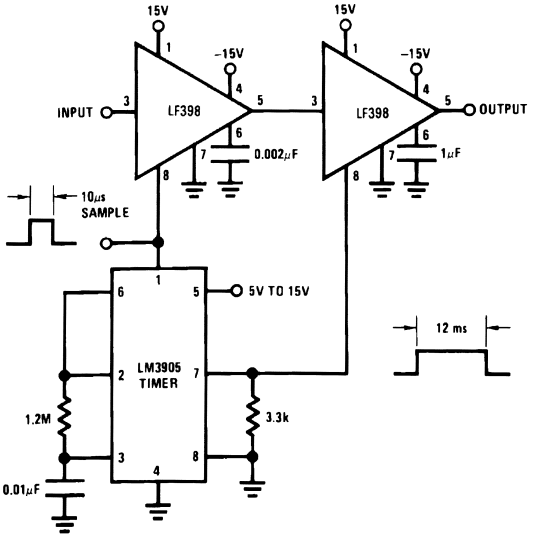
$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/\text{sec}$

$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$

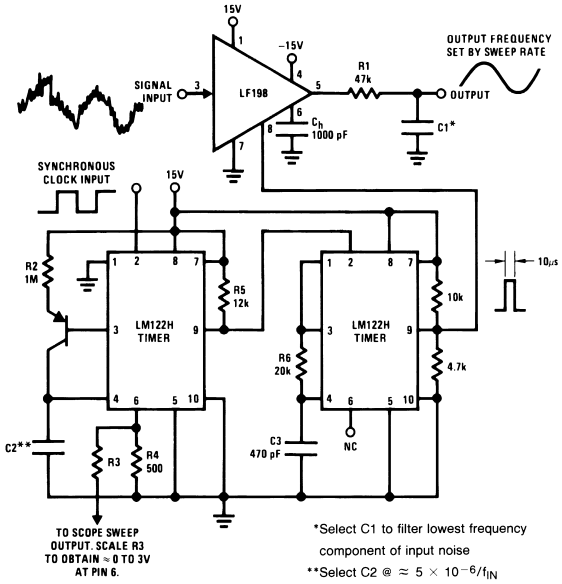
Fast Acquisition, Low Droop Sample & Hold



20122250

Typical Applications (Continued)

Synchronous Correlator for Recovering Signals Below Noise Level

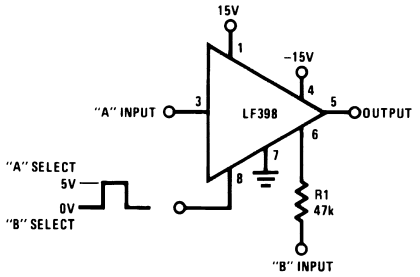


*Select C1 to filter lowest frequency component of input noise

**Select C2 @ ≃ 5 × $10^{-6}/f_{IN}$

20122252

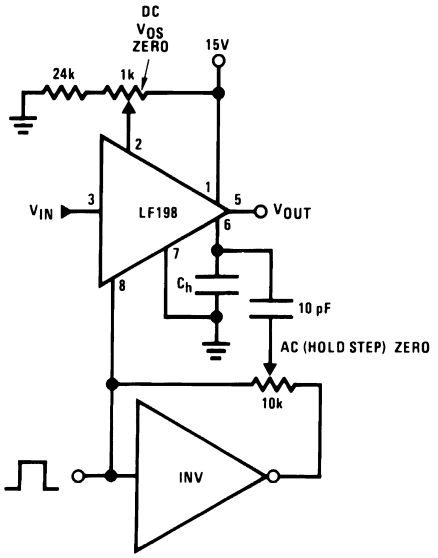
2–Channel Switch



20122253

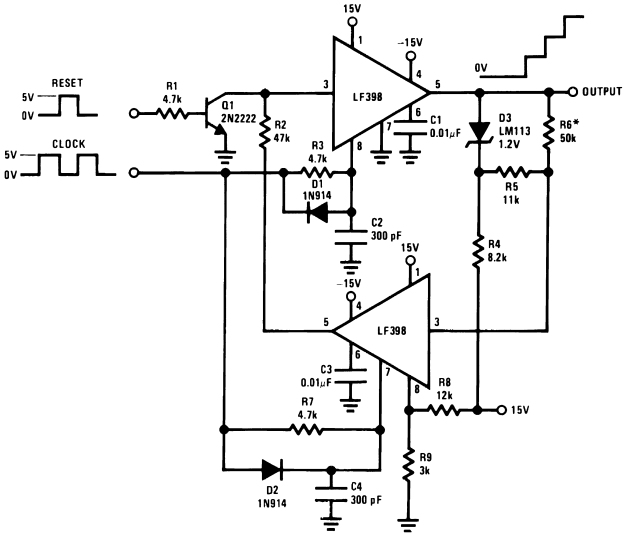
	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≃ 1 MHz	≃ 400 kHz
Crosstalk @ 1 kHz	−90 dB	−90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing



20122259

Staircase Generator



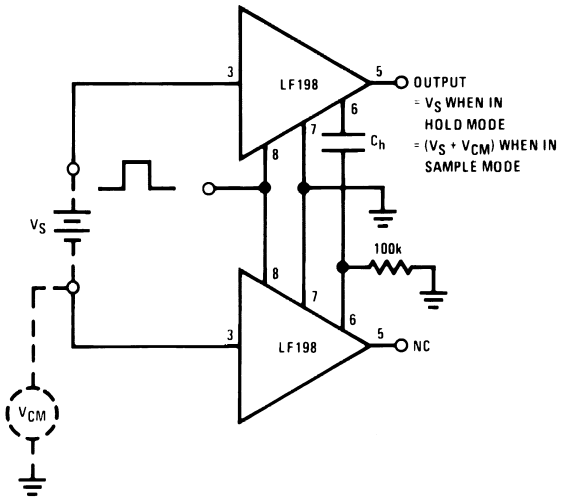
20122255

*Select for step height

50k → ≅ 1V Step

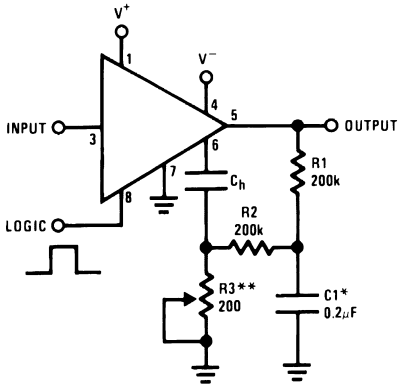
Typical Applications (Continued)

Differential Hold



20122257

Capacitor Hysteresis Compensation



20122256

*Select for time constant C1 = $\frac{\tau}{100k}$

**Adjust for amplitude

Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

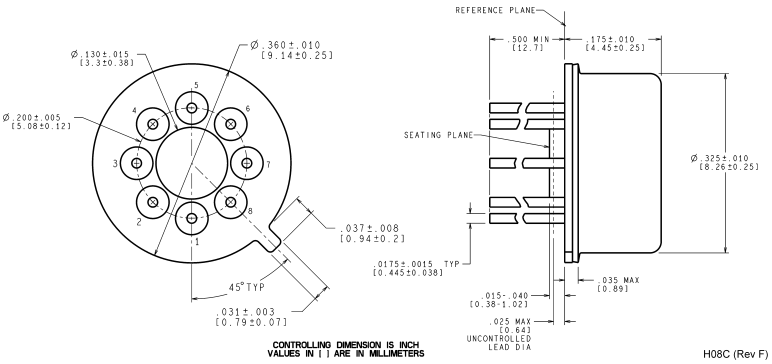
Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

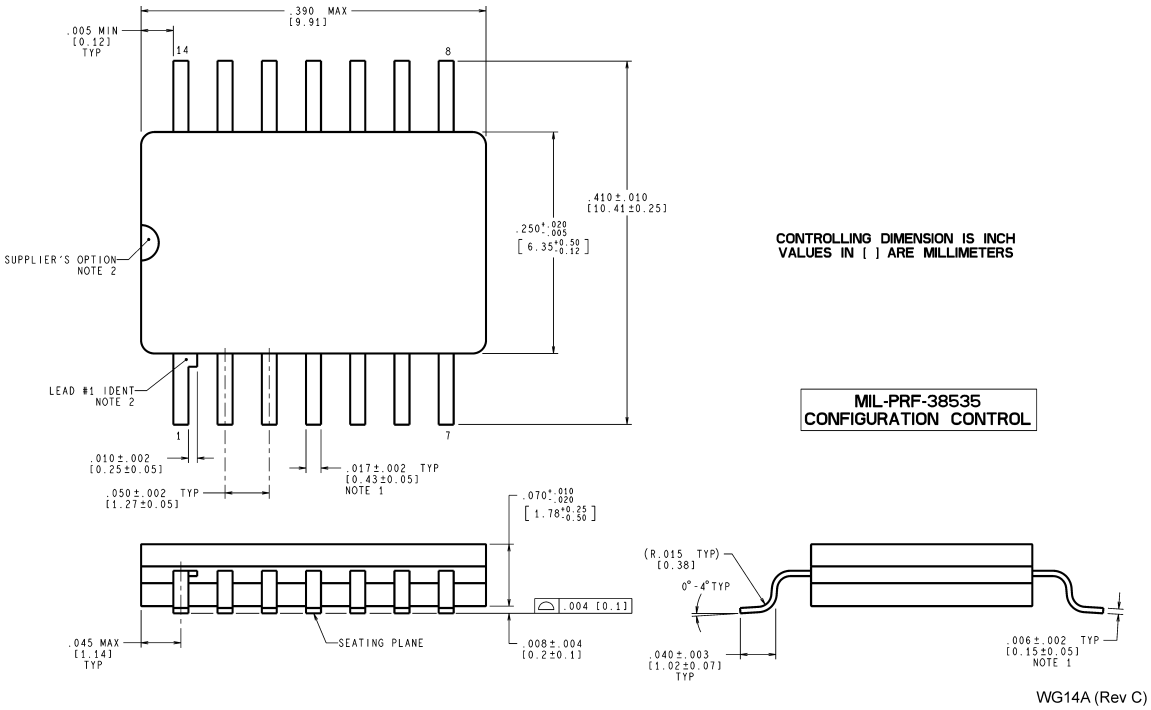
Revision History Section

Date Released	Revision	Section	Originator	Changes
02/25/05	A	New release, Corporate format	L. Lytle	1 MDS converted to corp. datasheet format. MNLF198–X Rev 3B0 MDS to be archived. Change has been made to Electrical Section, Parameter I_{OS}- . Max limit was 7.0 now is –7.0 confirmed with SG. Added note Parameter tested go no go to V_{TH} test.

Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
NS Package Number H08C



14 LD Ceramic SOIC (WG)
NS Package Number WG14A

Notes

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