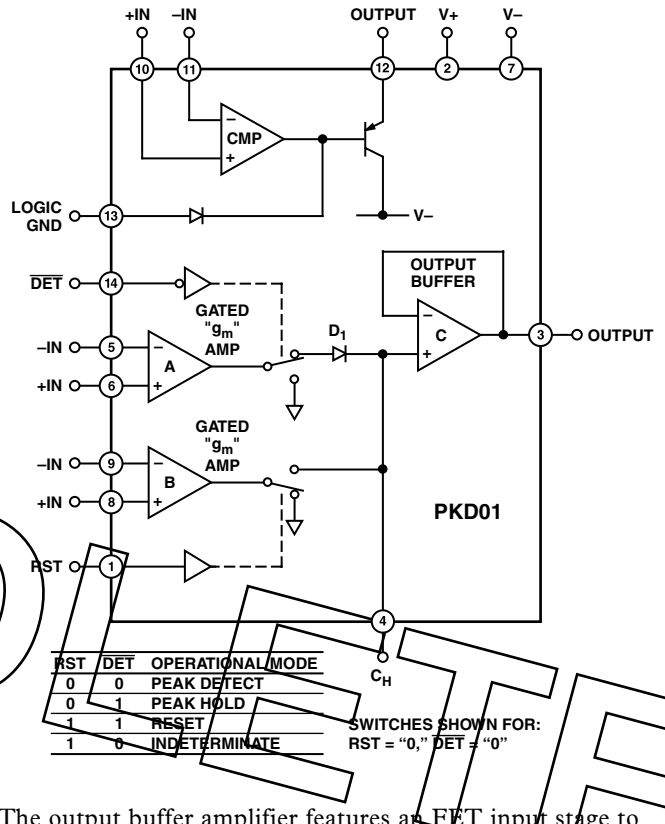
Monolithic Peak Detector with Reset-and-Hold Mode

PKD01

FEATURES

Monolithic Design for Reliability and Low Cost
High Slew Rate: 0.5 V/μs
Low Droop Rate
T_A = 25°C: 0.1 mV/ms
T_A = 125°C: 10 mV/ms
Low Zero-Scale Error: 4 mV
Digitally Selected Hold and Reset Modes
Reset to Positive or Negative Voltage Levels
Logic Signals TTL and CMOS Compatible
Uncommitted Comparator On-Chip
Available in Die Form

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The PKD01 tracks an analog input signal until a maximum amplitude is reached. The maximum value is then retained as a peak voltage on a hold capacitor. Being a monolithic circuit, the PKD01 offers significant performance and package density advantages over hybrid modules and discrete designs without sacrificing system versatility. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals.

Innovative design techniques maximize the advantages of monolithic technology. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The g_m amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. Their outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the hold mode or exiting the reset mode. The inherently low zero-scale error is further reduced by active Zener-Zap trimming to optimize overall accuracy.

The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

Through the $\overline{\text{DET}}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits, since Amplifier A can operate as an inverting or noninverting gain stage.

An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

REV. A

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PKD01–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, C_H = 1000 pF, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	PKD01A/E Min	PKD01A/E Typ	PKD01A/E Max	PKD01F Min	PKD01F Typ	PKD01F Max	Unit
g_m AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}			2	4		3	7	mV
Input Offset Voltage	V_{OS}			2	3		3	6	mV
Input Bias Current	I_B			80	150		80	250	nA
Input Offset Current	I_{OS}			20	40		20	75	nA
Voltage Gain	A_V	R_L = 10 kΩ, V_O = ±10 V	18	25		10	25		V/mV
Open-Loop Bandwidth	BW	A_V = 1		0.4			0.4		MHz
Common-Mode Rejection Ratio	CMRR	–10 V ≤ V_{CM} ≤ +10 V	80	90		74	90		dB
Power Supply Rejection Ratio	PSRR	±9 V ≤ V_S ≤ ±18 V	86	96		76	96		dB
Input Voltage Range[1]	V_{CM}		±10	±11		±10	±11		V
Slew Rate	SR			0.5			0.5		V/µs
Feedthrough Error[1]		ΔV_{IN} = 20 V, DET = 1, RST = 0	66	80		66	80		dB
Acquisition Time to 0.1% Accuracy[1]	t_{AQ}	20 V Step, A_{VCL} = +1		41	70		41	70	µs
Acquisition Time to 0.01% Accuracy[1]	t_{AQ}	20 V Step, A_{VCL} = +1		45			45		µs
COMPARATOR									
Input Offset Voltage	V_{OS}			0.5	1.5		1	3	mV
Input Bias Current	I_B			700	1000		700	1000	nA
Input Offset Current	I_{OS}			75	300		75	300	nA
Voltage Gain	A_V	2 kΩ Pull-Up Resistor to 5 V	5	7.5		3.5	7.5		V/mV
Common-Mode Rejection Ratio	CMRR	–10 V ≤ V_{CM} ≤ +10 V	82	106		82	106		dB
Power Supply Rejection Ratio	PSRR	±9 V ≤ V_S ≤ ±18 V	76	90		76	90		dB
Input Voltage Range[1]	V_{CM}		±11.5	±12.5		±11.5	±12.5		V
Low Output Voltage	V_{OL}	I_{SINK} ≤ 5 mA, Logic GND = 0 V	–0.2	+0.15	+0.4	–0.2	+0.15	+0.4	V
"OFF" Output Leakage Current	I_L	V_{OUT} = 5 V		25	80		25	80	µA
Output Short-Circuit Current	I_{SC}	V_{OUT} = 5 V	7	12	45	7	12	45	mA
Response Time[2]	t_S	5 mV Overdrive, 2 kΩ Pull-Up Resistor to 5 V		150			150		ns
DIGITAL INPUTS – RST, $\overline{DET}$[2]									
Logic "1" Input Voltage	V_H		2			2			V
Logic "0" Input Voltage	V_L				0.8			0.8	V
Logic "1" Input Current	I_{INH}	V_H = 3.5 V		0.02	1		0.02	1	µA
Logic "0" Input Current	I_{INL}	V_L = 0.4 V		1.6	10		1.6	10	µA
MISCELLANEOUS									
Droop Rate[3]	V_{DR}	T_J = 25°C		0.01	0.07		0.01	0.1	mV/ms
		T_A = 25°C		0.02	0.15		0.03	0.20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$\overline{DET}$ = 1, R_L = 2.5 kΩ	±11.5	±12.5		±11	±12		V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{AP}			75			75		ns
Switch Switching Time	ts			50			50		ns
Slew Rate: Amplifier C	SR	R_L = 2.5 kΩ		2.5			2.5		V/µs
Power Supply Current	I_{SY}	No Load		5	7		6	9	mA

NOTES

[1]Guaranteed by design.

[2]$\overline{DET}$ = 1, RST = 0.

[3]Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarified this point. Since most devices (in use) are on for more than 1 second, ADI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. ADI has a droop current cancellation circuit that minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

(@ V_S = ±15 V, C_H = 1000 pF, –55°C ≤ T_A ≤ +125°C for PKD01AY, –25°C ≤ T_A ≤ +85°C for PKD01EY, PKD01FY and 0°C ≤ T_A ≤ +70°C for PKD01EP, PKD01FP, unless otherwise noted.)

Parameter	Symbol	Conditions	PKD01A/E Min	PKD01A/E Typ	PKD01A/E Max	PKD01F Min	PKD01F Typ	PKD01F Max	Unit
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}			4	7		6	12	mV
Input Offset Voltage	V_{OS}			3	6		5	10	mV
Average Input Offset Drift[1]	TCV_{OS}			–9	–24		–9	–24	µV/°C
Input Bias Current	I_B			160	250		160	500	nA
Input Offset Current	I_{OS}			30	100		30	150	nA
Voltage Gain	A_V	R_L = 10 kΩ, V_O = ±10 V	7.5	9		5	9		V/mV
Common-Mode Rejection Ratio	CMRR	–10 V ≤ V_{CM} ≤ +10 V	74	82		72	80		dB
Power Supply Rejection Ratio	PSRR	±9 V ≤ V_S ≤ ±18 V	80	90		70	90		dB
Input Voltage Range[1]	V_{CM}		±10	±11		±10	±11		V
Slew Rate	SR			0.4			0.4		V/µs
Acquisition Time to 0.1% Accuracy[1]	t_{AQ}	20 V Step, A_{VCL} = +1		60			60		µs
COMPARATOR									
Input Offset Voltage	V_{OS}			2	2.5		2	5	mV
Average Input Offset Drift[1]	TCV_{OS}			–4	–6		–4	–6	µV/°C
Input Bias Current	I_B			1000	2000		1100	2000	nA
Input Offset Current	I_{OS}			100	600		100	600	nA
Voltage Gain	A_V	2 kΩ Pull-Up Resistor to 5 V	4	6.5		2.5	6.5		V/mV
Common-Mode Rejection Ratio	CMRR	–10 V ≤ V_{CM} ≤ +10 V	80	100		80	92		dB
Power Supply Rejection Ratio	PSRR	±9 V ≤ V_S ≤ ±18 V	72	82		72	86		dB
Input Voltage Range[1]	V_{CM}		±11			±11			V
Low Output Voltage	V_{OL}	I_{SINK} ≤ 5 mA, Logic GND = 0 V	–0.2	+0.15	+0.4	–0.2	+0.15	+0.4	V
OFF Output Leakage Current	I_L	V_{OUT} = 5 V		25	100		100	180	µA
Output Short-Circuit Current	I_{SC}	V_{OUT} = 5 V	6	10	45	6	10	45	mA
Response Time	t_S	5 mV Overdrive, 2 kΩ Pull-Up Resistor to 5 V		200			200		ns
DIGITAL INPUTS – RST, $\overline{DET}$[2]									
Logic "1" Input Voltage	V_H		2			2			V
Logic "0" Input Voltage	V_L				0.8			0.8	V
Logic "1" Input Current	I_{INH}	V_H = 3.5 V		0.02	1		0.02	1	µA
Logic "0" Input Current	I_{INL}	V_L = 0.4 V		2.5	15		2.5	15	µA
MISCELLANEOUS									
Droop Rate[3]	V_{DR}	T_J = Max Operating Temp.		1.2	10		3	15	mV/ms
		T_A = Max Operating Temp. $\overline{DET}$ = 1		2.4	20		6	20	mV/ms
Output Voltage Swing Amplifier C	V_{OP}	R_L = 2.5 kΩ	±11	±12		±10.5	±12		V
Short-Circuit Current Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{AP}			75			75		ns
Slew Rate: Amplifier C	SR	R_L = 2.5 kΩ		2			2		V/µs
Power Supply Current	I_{SY}	No Load		5.5	8		6.5	10	mA

NOTES

[1]Guaranteed by design.

[2]$\overline{DET}$ = 1, RST = 0.

[3]Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, ADI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. ADI has a droop current cancellation circuit that minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . Equal to Supply Voltage
Logic and Logic Ground
Voltage . . . . . Equal to Supply Voltage
Output Short-Circuit Duration . . . . . Indefinite
Amplifier A or B Differential Input Voltage . . . . . ±24 V
Comparator Differential Input Voltage . . . . . ±24 V
Comparator Output Voltage
. . . . . Equal to Positive Supply Voltage
Hold Capacitor Short-Circuit Duration . . . . . Indefinite
Lead Temperature (Soldering, 60 sec) . . . . . 300°C
Storage Temperature Range
PKD01AY, PKD01EY, PKD01FY . . . . . –65°C to +150°C
PKD01EP, PKD01FP . . . . . –65°C to +125°C
Operating Temperature Range
PKD01AY . . . . . –55°C to +125°C
PKD01EY, PKD01FY . . . . . –25°C to +85°C
PKD01EP, PKD01FP . . . . . 0°C to 70°C
Junction Temperature . . . . . –65°C to +150°C

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JA}*	θ_{JC}	Unit
14-Lead Hermetic DIP (Y)	99	12	°C/W
14-Lead Plastic DIP (P)	76	33	°C/W

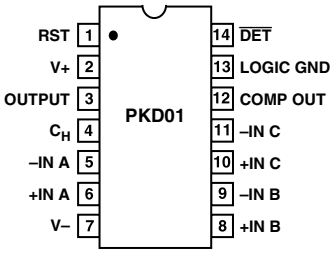
*θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and PDIP packages.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Package Description	Package Option
PKD01AY	–55°C to +85°C	Cerdip	Q-14
PKD01EY	–25°C to +85°C	Cerdip	Q-14
PKD01FY	–25°C to +85°C	Cerdip	Q-14
PKD01EP	0°C to 70°C	Plastic DIP	N-14
PKD01FP	0°C to 70°C	Plastic DIP	N-14

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

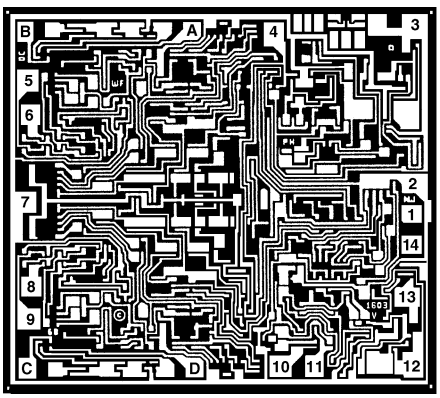
PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the PKD01 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DICE CHARACTERISTICS



1. RST (RESET CONTROL)
2. V+
3. OUTPUT
4. CH (HOLD CAPACITOR)
5. INVERTING INPUT (A)
6. NONINVERTING INPUT (A)
7. V–
8. NONINVERTING INPUT (B)
9. INVERTING INPUT (B)
10. COMPARATOR NONINVERTING INPUT
11. COMPARATOR INVERTING INPUT
12. COMPARATOR OUTPUT
13. LOGIC GROUND
14. $\overline{\text{DET}}$ (PEAK DETECT CONTROL)

A, B (A) NULL
C, D (B) NULL

DIE SIZE 0.090 × 0.100 INCH, 9000 SQ. MILS
(2.286 × 2.54mm, 5.8 SQ. mm)

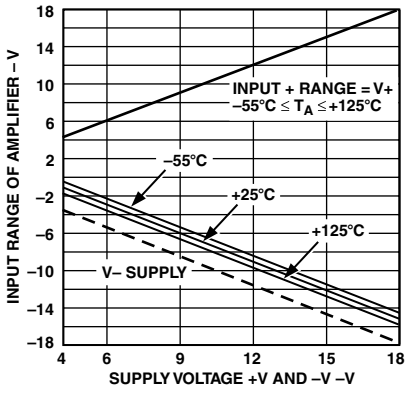
FOR ADDITIONAL DICE INFORMATION REFER TO
1986 DATA BOOK, SECTION 2.

WAFER TEST LIMITS (@ V_S = ±15 V, C_H = 1000 pF, T_A = 25°C, unless otherwise noted.)

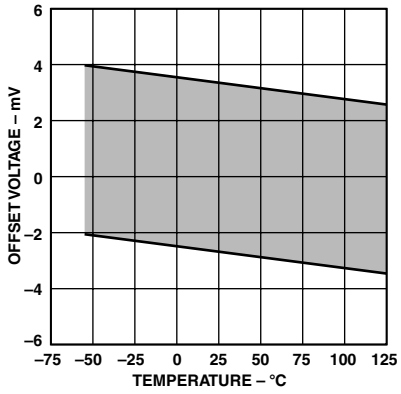
Parameter	Symbol	Conditions	PKD01N Limit	Unit
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV max
Input Offset Voltage	V_{OS}		6	mV max
Input Bias Current	I_B		250	nA max
Input Offset Current	I_{OS}		75	nA max
Voltage Gain	A_V	R_L = 10 kΩ, V_O = ±10 V	10	V/mV min
Common-Mode Rejection Ratio	CMRR	–10 V ≤ V_{CM} ≤ +10 V	74	dB min
Power Supply Rejection Ratio	PSRR	±9 V ≤ V_S ≤ ±18 V	76	dB min
Input Voltage Range[1]	V_{CM}		±11.5	V min
Feedthrough Error		ΔV_{IN} = 20 V, $\overline{DET}$ = 1, RST = 0	66	dB min
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV max
Input Bias Current	I_B		1000	nA max
Input Offset Current	I_{OS}		300	nA max
Voltage Gain[1]	A_V	2 kΩ Pull-Up Resistor to 5 V	3.5	V/mV min
Common-Mode Rejection Ratio	CMRR	–10 V ≤ V_{CM} ≤ +10 V	82	dB min
Power Supply Rejection Ratio	PSRR	±9 V ≤ V_S ≤ ±18 V	76	dB min
Input Voltage Range[1]	V_{CM}		±11.5	V min
Low Output Voltage	V_{OL}	I_{SINK} ≤ 5 mA, Logic GND = 5 V	0.4	V max
			–0.2	V min
"OFF" Output Leakage Current	I_L	V_{OUT} = 5 V	80	µA max
Output Short-Circuit Current	I_{SC}	V_{OUT} = 5 V	45	mA min
			7	mA min
DIGITAL INPUTS–RST, $\overline{DET}$[2]				
Logic "1" Input Voltage	V_H		2	V min
Logic "0" Input Voltage	V_L		0.8	V max
Logic "1" Input Current	I_{INH}	V_H = 3.5 V	1	µA max
Logic "0" Input Current	I_{INL}	V_L = 0.4 V	10	µA max
MISCELLANEOUS				
Droop Rate[3]	V_{DR}	T_J = 25°C,	0.1	mV/ms max
		T_A = 25°C	0.20	mV/ms max
Output Voltage Swing Amplifier C	V_{OP}	R_L = 2.5 kΩ	±11	V min
Short-Circuit Current Amplifier C	I_{SC}		40	mA max
			7	mA min
Power Supply Current	I_{SY}	No Load	9	mA max
g_m AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/µs
Acquisition Time[1]	t_A	0.1% Accuracy, 20 V Step, A_{VCL} = 1	41	µs
	t_A	0.01% Accuracy, 20 V Step, A_{VCL} = 1	45	µs
COMPARATOR				
Response Time		5 mV Overdrive, 2 kΩ Pull-Up Resistor to 5 V	150	ns
MISCELLANEOUS				
Switch Aperture Time	t_{AP}		75	ns
Switching Time	t_S		50	ns
Buffer Slew Rate	SR	R_L = 2.5 kΩ	2.5	V/µs

NOTES
[1]Guaranteed by design.
[2]$\overline{DET}$ = 1, RST = 0.
[3]Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, ADI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. ADI has a droop current cancellation circuit that minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

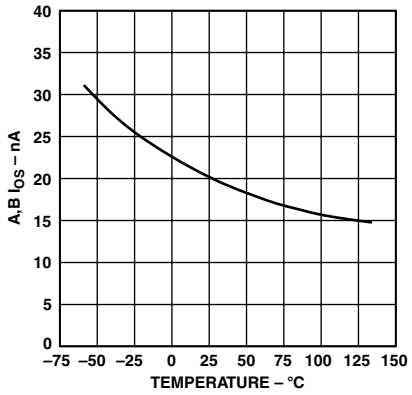
PKD01–Typical Performance Characteristics



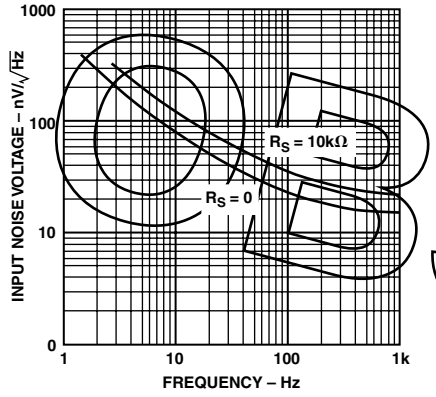
TPC 1. A and B Input Range vs. Supply Voltage



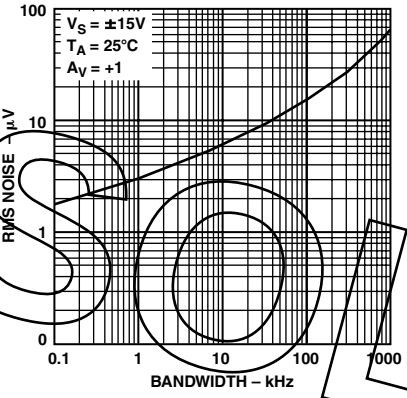
TPC 2. A and B Amplifiers Offset Voltage vs. Temperature



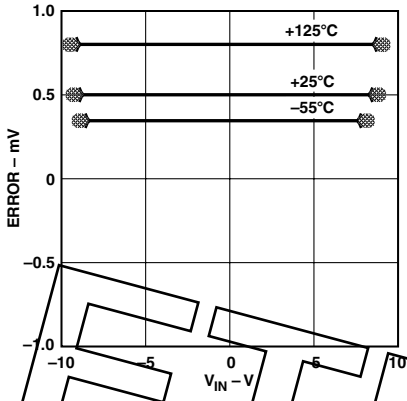
TPC 3. A, B I_{OS} vs. Temperature



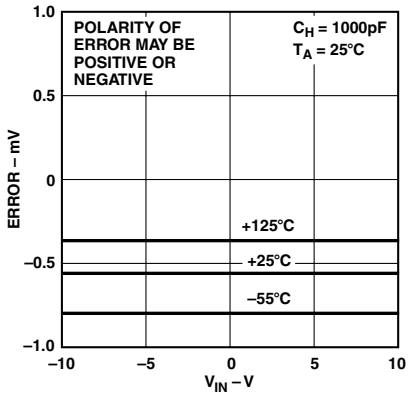
TPC 4. Input Spot Noise vs. Frequency



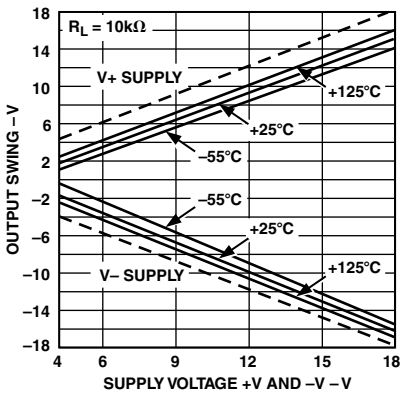
TPC 5. Wideband Noise vs. Bandwidth



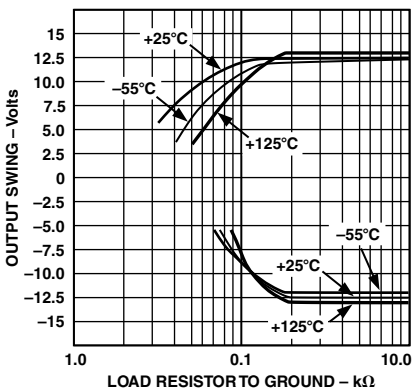
TPC 6. Amplifier B Charge Injection Error vs. Input Voltage and Temperature



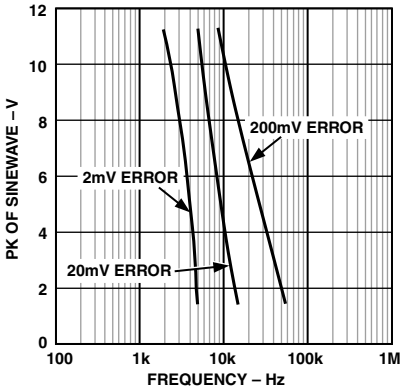
TPC 7. Amplifier A Charge Injection Error vs. Input Voltage and Temperature



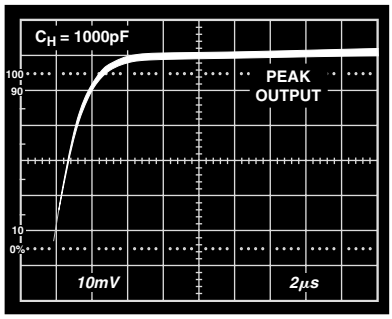
TPC 8. Output Voltage Swing vs. Supply Voltage (Dual Supply Operation)



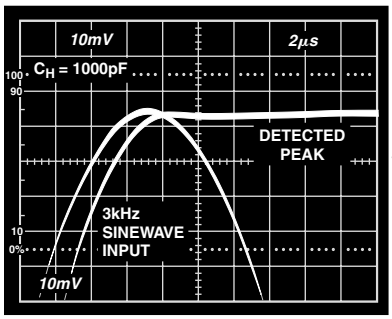
TPC 9. Output Voltage vs. Load Resistance



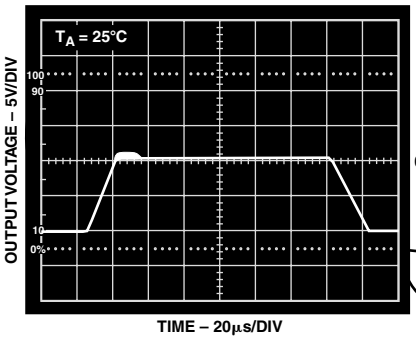
TPC 10. Output Error vs. Frequency and Input Voltage



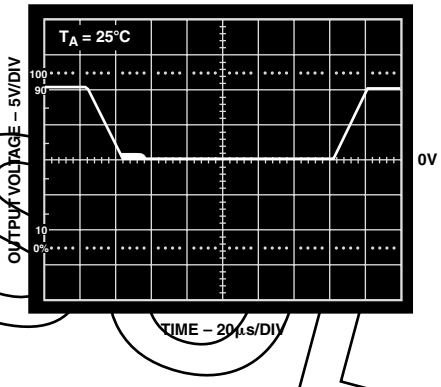
TPC 11. Settling Response



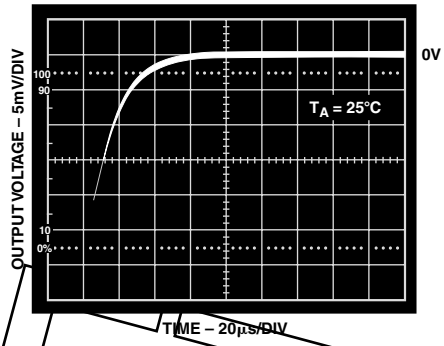
TPC 12. Settling Response



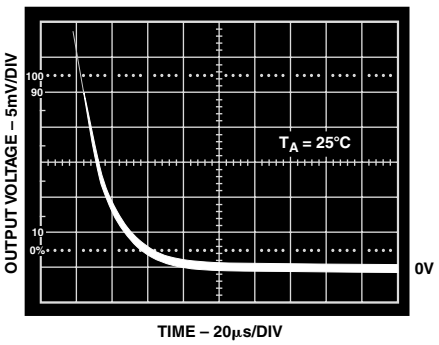
TPC 13. Large-Signal Inverting Response



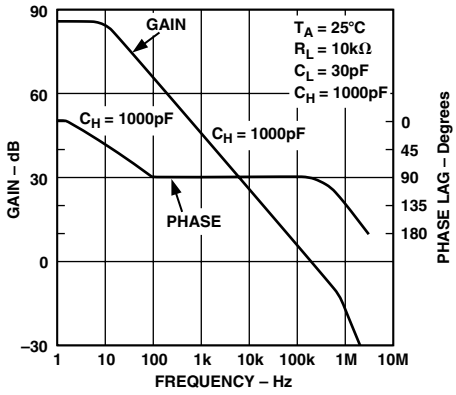
TPC 14. Large-Signal Noninverting Response



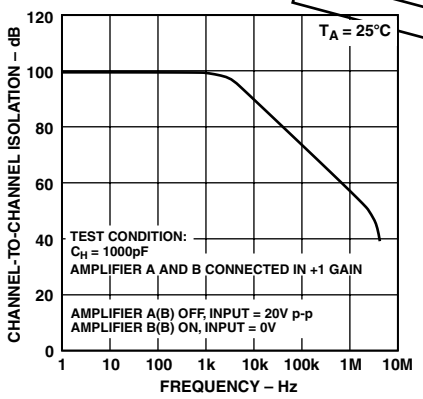
TPC 15. Settling Time for –10 V to 0 V Step Input



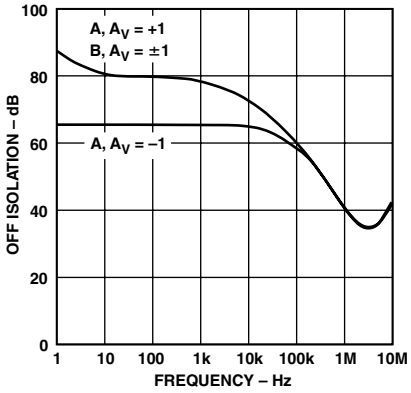
TPC 16. Settling Time for +10 V to 0 V Step Input



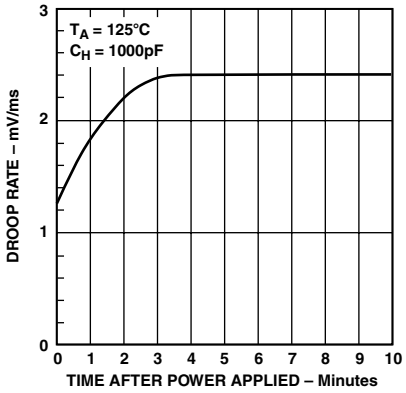
TPC 17. Small-Signal Open-Loop Gain/Phase vs. Frequency



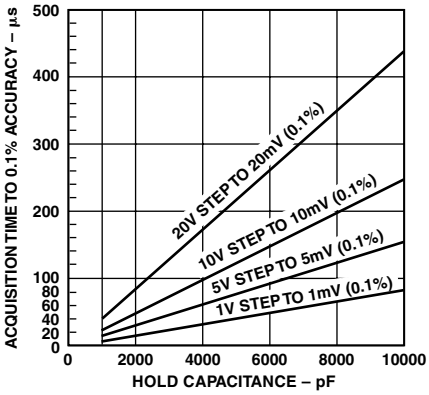
TPC 18. Channel-to-Channel Isolation vs. Frequency



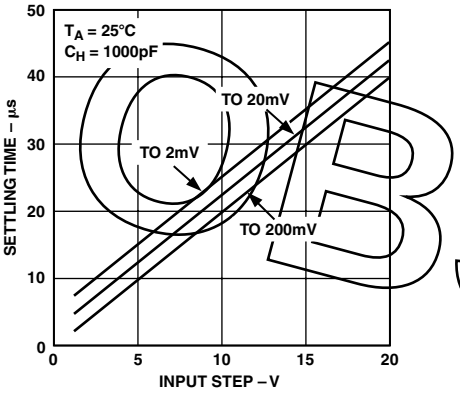
TPC 19. Off Isolation vs. Frequency



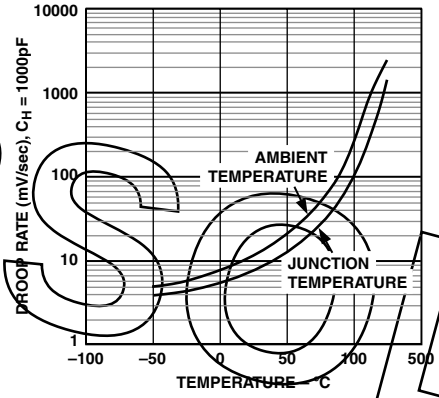
TPC 20. Droop Rate vs. Time after Power On



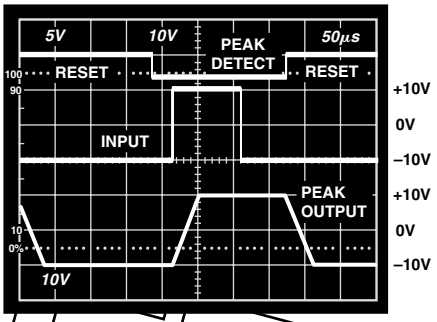
TPC 21. Acquisition Time vs. External Hold Capacitor and Acquisition Step



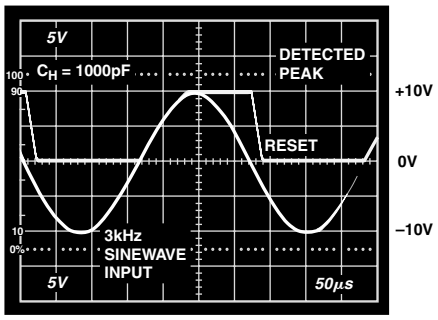
TPC 22. Acquisition Time vs. Input Voltage Step Size



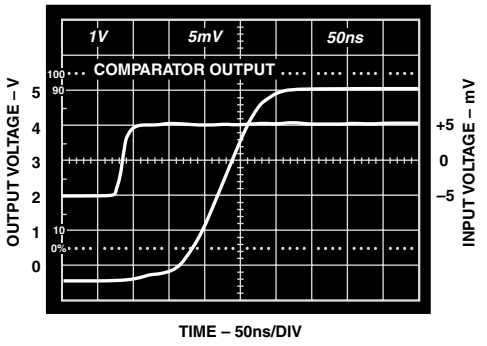
TPC 23. Droop Rate vs. Temperature



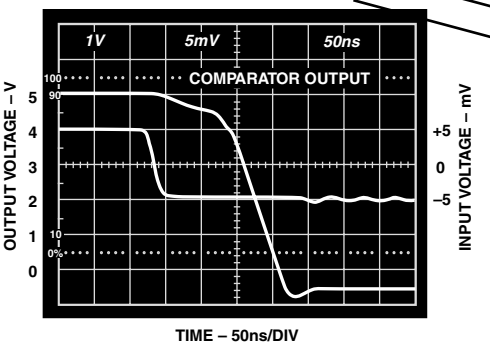
TPC 24. Acquisition of Step Input



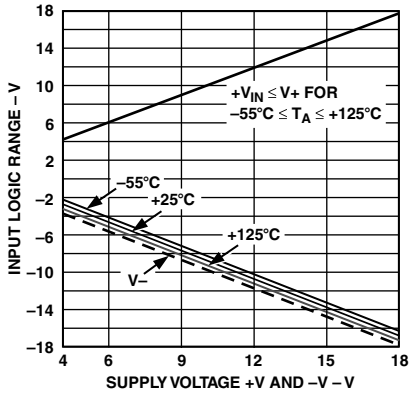
TPC 25. Acquisition of Sine Wave Peak



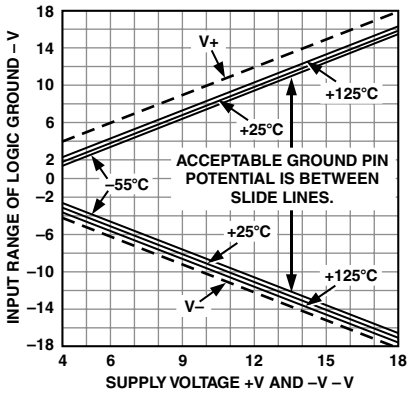
TPC 26. Comparator Output Response Time (2 kΩ Pull-Up Resistor, T_A = 25°C)



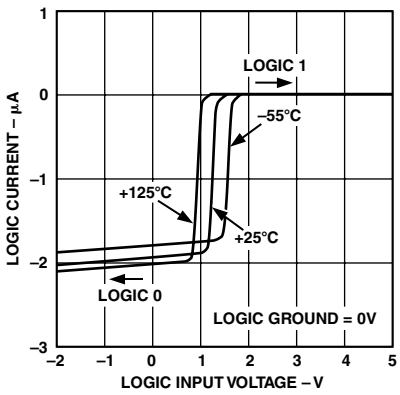
TPC 27. Comparator Output Response Time (2 kΩ Pull-Up Resistor, T_A = 25°C)



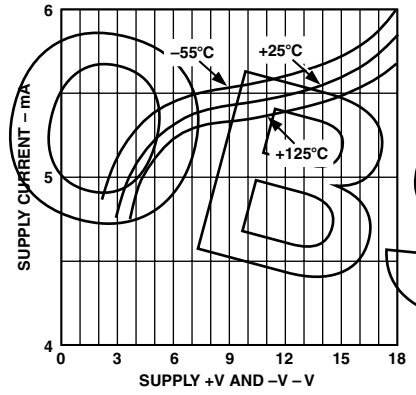
TPC 28. Input Logic Range vs. Supply Voltage



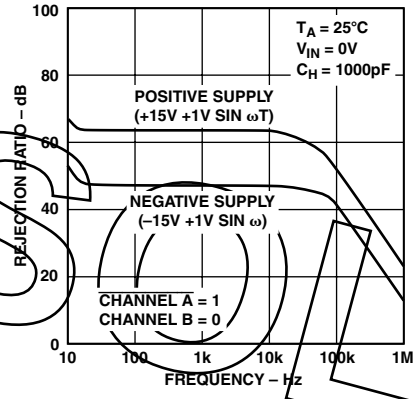
TPC 29. Input Range of Logic Ground vs. Supply Voltage



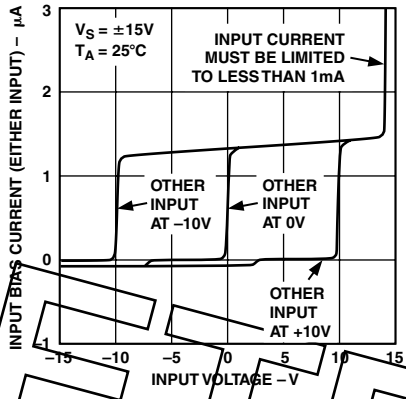
TPC 30. Logic Input Current vs. Logic Input Voltage



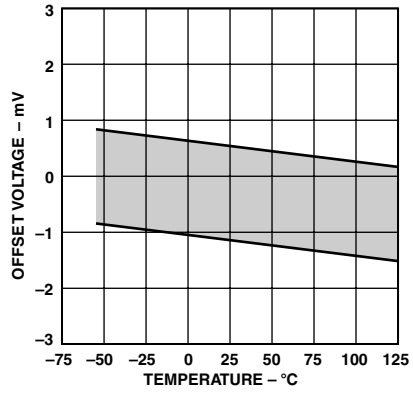
TPC 31. Supply Current vs. Supply Voltage



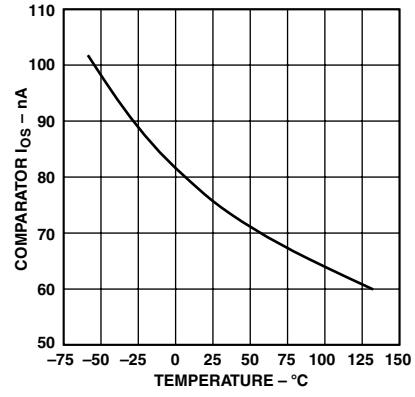
TPC 32. Hold Mode Power Supply Rejection vs. Frequency



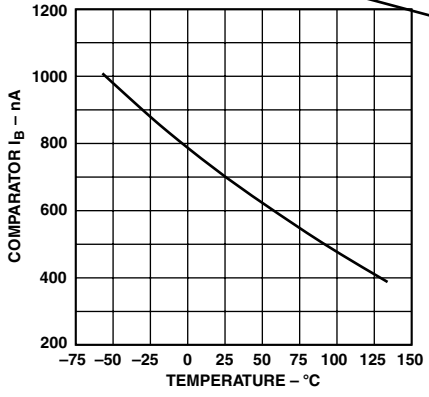
TPC 33. Comparator Input Bias Current vs. Differential Input Voltage



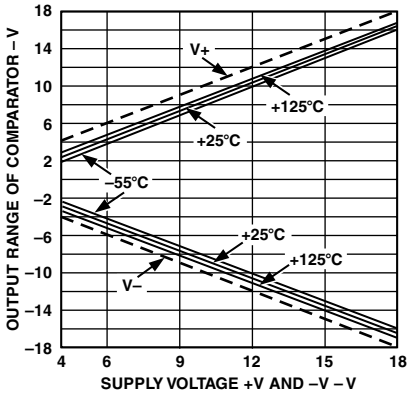
TPC 34. Comparator Offset Voltage vs. Temperature



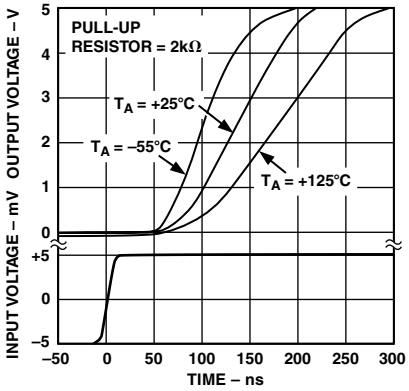
TPC 35. Comparator I_{OS} vs. Temperature



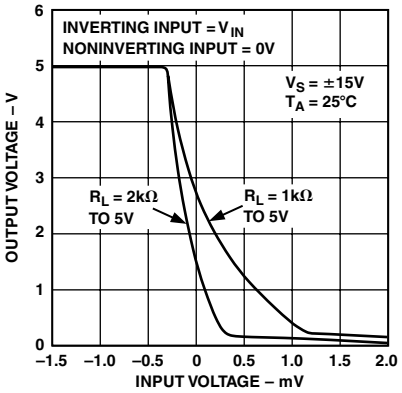
TPC 36. Comparator I_B vs. Temperature



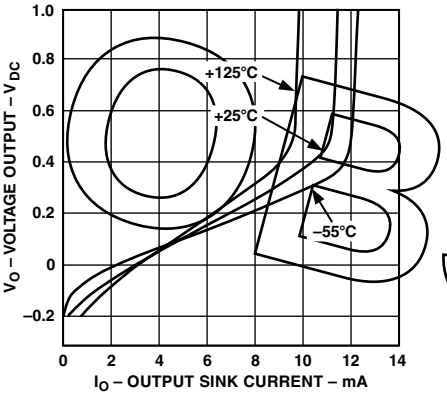
TPC 37. Output Swing of Comparator vs. Supply Voltage



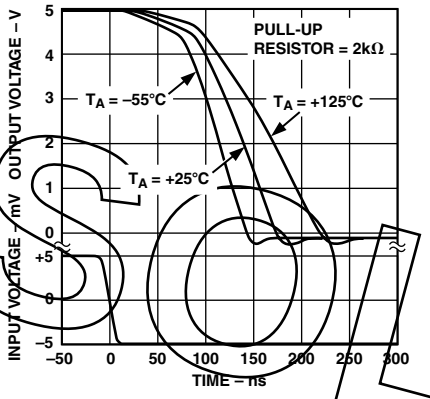
TPC 38. Comparator Response Time vs. Temperature



TPC 39. Comparator Transfer Characteristic



TPC 40. Comparator Output Voltage vs. Output Current and Temperature



TPC 41. Comparator Response Time vs. Temperature

OBSOLETE

THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H, indirectionally (see Figure 1). The output impedance of A plus D_1's dynamic impedance, r_d, make up the resistance which determines the feedback loop pole. The dynamic impedance is

$r_d = \frac{kT}{qI_d}$, where I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

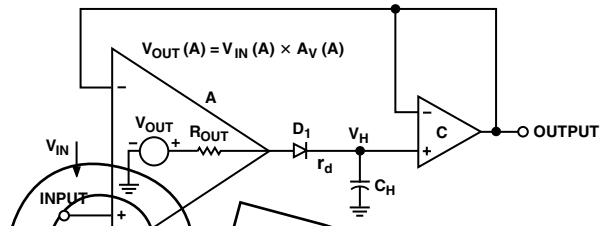


Figure 1. Conventional Voltage Amplifier Peak Detector

When the moving pole is considered with the typical frequency compensation of voltage amplifiers however, there is a loop stability problem. The necessary compensation can increase the required acquisition time. ADI's approach replaces the input voltage amplifier with a transconductance amplifier (see Figure 2).

The PKD01 transfer function can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1+\frac{sC_H}{g_m}+\frac{1}{g_m R_{OUT}}} \approx \frac{1}{1+\frac{sC_H}{g_m}}$$

where: $g_m \approx 1\ \mu A/mV$, $R_{OUT} \approx 20\ M\Omega$.

The diode in series with A's output (see Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

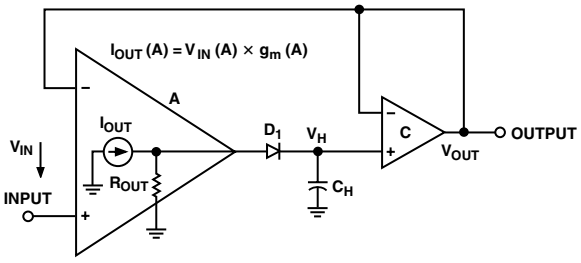


Figure 2. Transconductance Amplifier Peak Detector

Figure 3 shows a simplified schematic of the reset g_m amplifier, B. In the track mode, Q_1 and Q_4 are ON and Q_2 and Q_3 are OFF. A current of 2I passes through D_1, I is summed at B and passes through Q_1, and is summed with $g_m V_{IN}$. The current sink can absorb only 3I, thus the current passing through D_2 can only be: $2K - g_m V_{IN}$. The net current into the hold capacitor node then, is $g_m V_{IN}$ [$I_H = 2I - (2I - g_m V_{IN})$]. In the hold mode, Q_2 and Q_3 are ON while Q_1 and Q_4 are OFF. The net current into the top of D_1 is –I until D_3 turns ON. With Q_1 OFF, the bottom of D_2 is pulled up with a current I until D_4 turns ON, thus, D_1 and D_2 are reverse biased by <0.6 V, and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally, but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

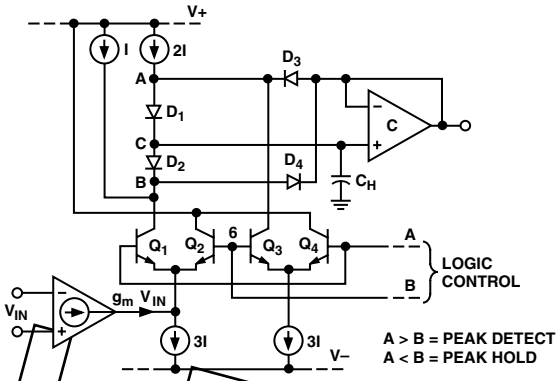


Figure 3. Transconductance Amplifier with Low Glitch Current Switch

The peak transconductance amplifier, A is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse-biased. The voltage clamp limits charge injection to approximately 1 pC and the hold step to 0.6 mV.

Minimizing acquisition time dictates a small C_H capacitance. A 1000 pF value was selected. Droop rate was also minimized by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every 10° temperature change.

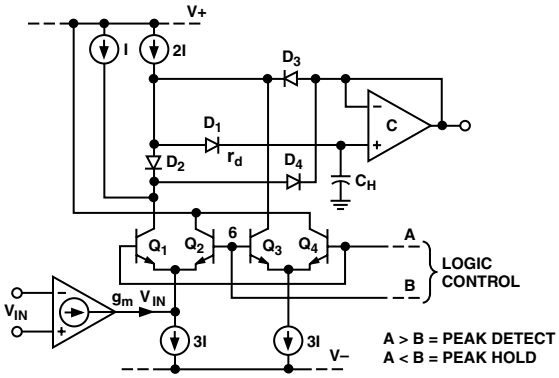


Figure 4. Peak Detecting Transconductance Amplifier with Switched Output

APPLICATIONS INFORMATION

Optional Offset Voltage Adjustment

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1's anode and reduces charge injection. The PKD01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures 5 through 8 are suggested circuits. Each circuit also corrects amplifier C offset voltage error.

A. Nulling Gated Output g_m Amplifier A. Diode D_1 must be conducting to close the feedback circuit during amplifier A V_{OS} adjustment. Resistor network $R_A - R_C$ cause D_1 to conduct slightly. With DET = 0 and V_{IN} = 0 V, monitor the PKD01 output. Adjust the null potentiometer until V_{OUT} = 0 V. After adjustment, disconnect R_C from C_H.

B. Nulling Gated g_m Amplifier B. Set Amplifier B signal input to V_{IN} = 0 V and monitor the PKD01 output. Set DET = 1, RST = 1 and adjust the null potentiometer for V_{OUT} = 0 V. The circuit gain—inverting or noninverting—will determine which null circuit illustrated in Figures 5 through 8 is applicable.

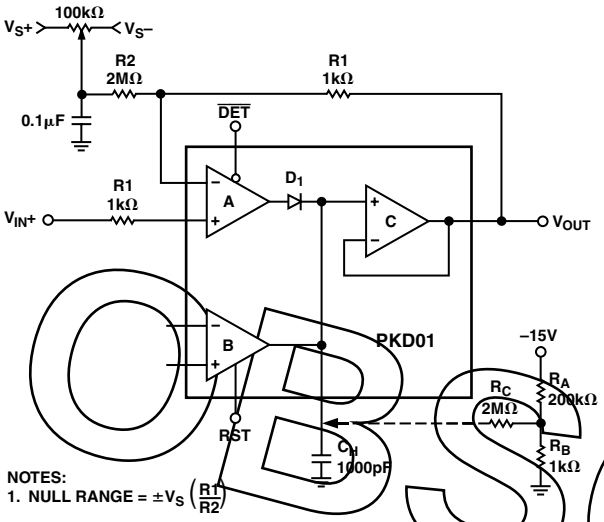


Figure 5. V_{OS} Null Circuit for Unity Gain Positive Peak Detector

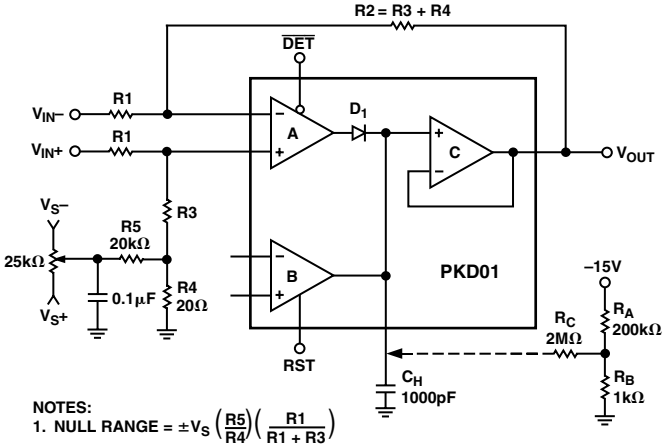


Figure 6. V_{OS} Null Circuit for Differential Peak Detector

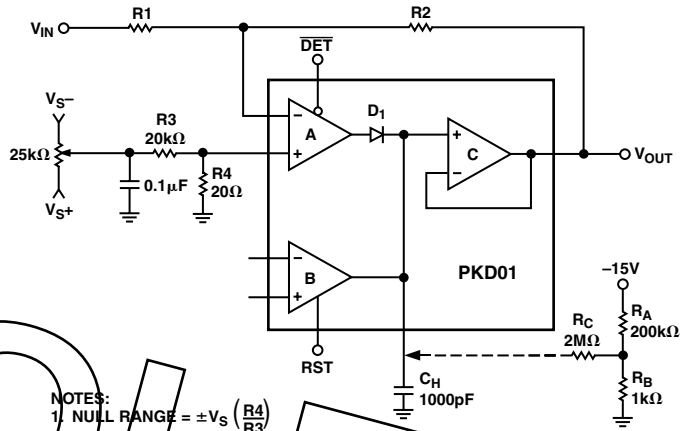


Figure 7. V_{OS} Null Circuit for Negative Peak Detector

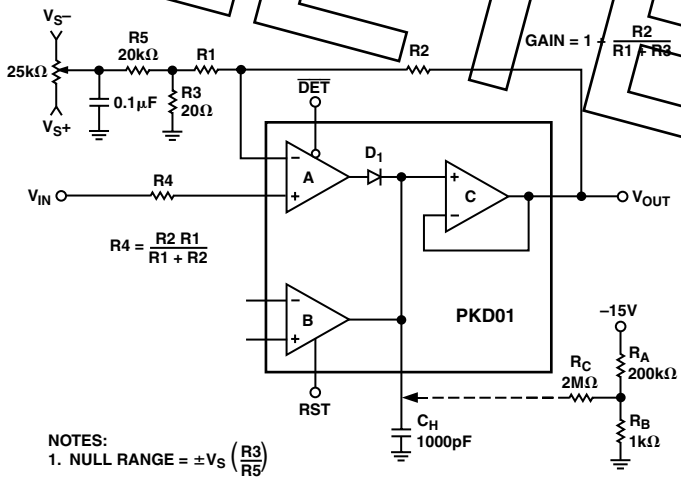


Figure 8. V_{OS} Null Circuit for Positive Peak Detector with Gain

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000 pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for C_H = 1000 pF. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

$$\Delta V_{ZS}(mV) = \frac{1 \times 10^3 (pC)}{C_H(nF)} - 0.6\,mV$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

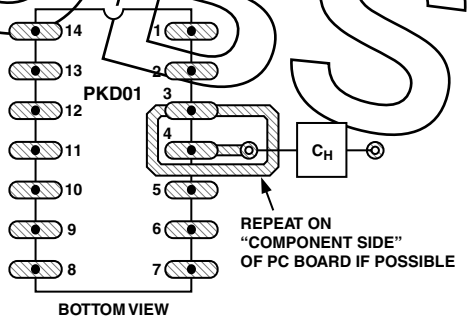


Figure 9. C_H Terminal (Pin 4) Guarding. See Text.

The C_H terminal (Pin 4) is a high impedance point. To minimize gain errors and maintain the PKD01's inherently low droop rate, guarding Pin 4 as shown in Figure 9 is recommended.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It is possible to optimize noise immunity while interfacing to all standard logic families—TTL, DTL, and CMOS. Figure 10 shows the comparator output with external level-setting resistors. Table I gives typical R1 and R2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$$V_{OH}\ (maximum) < V+ - 2.0\ V$$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R1.

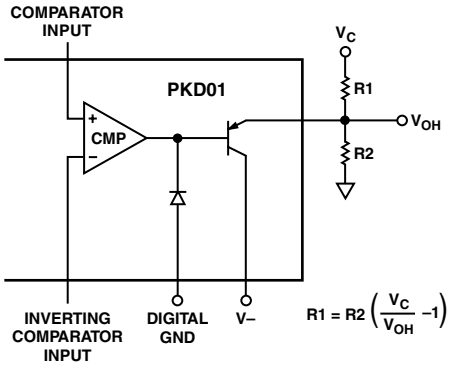


Figure 10. Comparator Output with External Level-Setting Resistors

Table I.

V_C	V_{OH}	R1	R2
5	3.5	2.7 kΩ	6.2 kΩ
5	5.0	2.7 kΩ	∞
15	3.5	4.7 kΩ	1.5 kΩ
15	5.0	4.7 kΩ	2.4 kΩ
15	7.5	7.5 kΩ	7.5 kΩ
15	10.0	7.5 kΩ	15 kΩ

$$R1 \approx \frac{V_C}{I_{SINK}}$$

$$R2 \approx \left(\frac{1}{\frac{V_C}{V_{OH}} - 1}\right)$$

PEAK DETECTOR LOGIC CONTROL (RST, $\overline{DET}$)

The transconductance amplifier outputs are controlled by the digital logic signals RST and $\overline{DET}$. The PKD01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2, thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 V when digital ground is at zero volts.

Other threshold voltages (V_{TH}) may be selected by applying the formula:

$$V_{TH} \approx 1.4\ V + Digital\ Ground\ Potential.$$

For proper operation, digital ground must always be at least 3.5 V below the positive supply and 2.5 V above the negative supply. The RST or $\overline{DET}$ signal must always be at least 2.8 V above the negative supply.

Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$$V_{OL} \approx 0.2\ V + Digital\ Ground\ Potential.$$

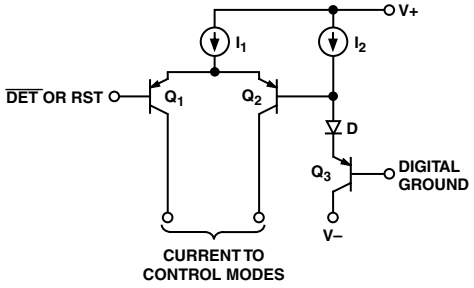


Figure 11. Logic Control

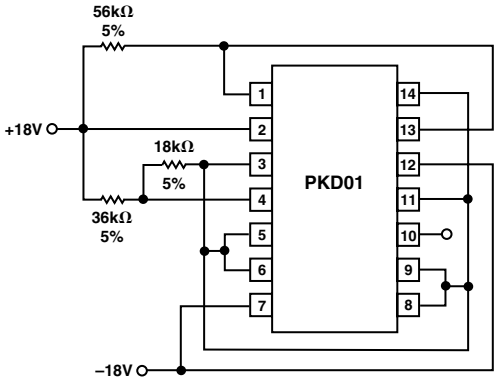


Figure 12. Burn-In Circuit

Typical Circuit Configurations

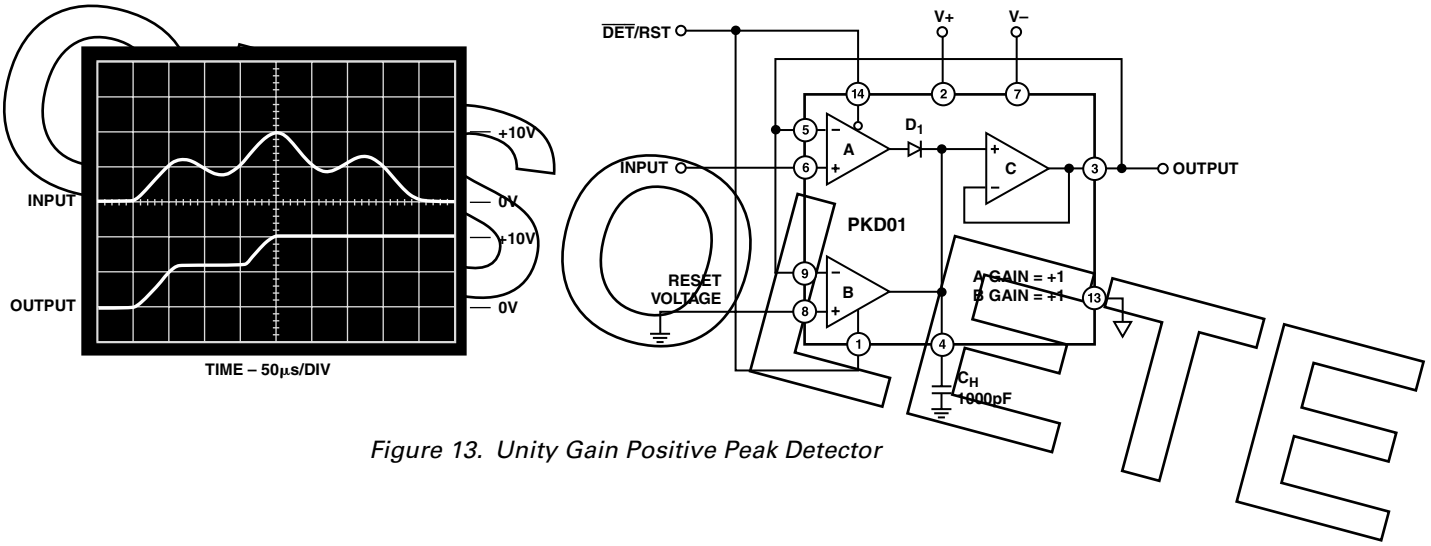


Figure 13. Unity Gain Positive Peak Detector

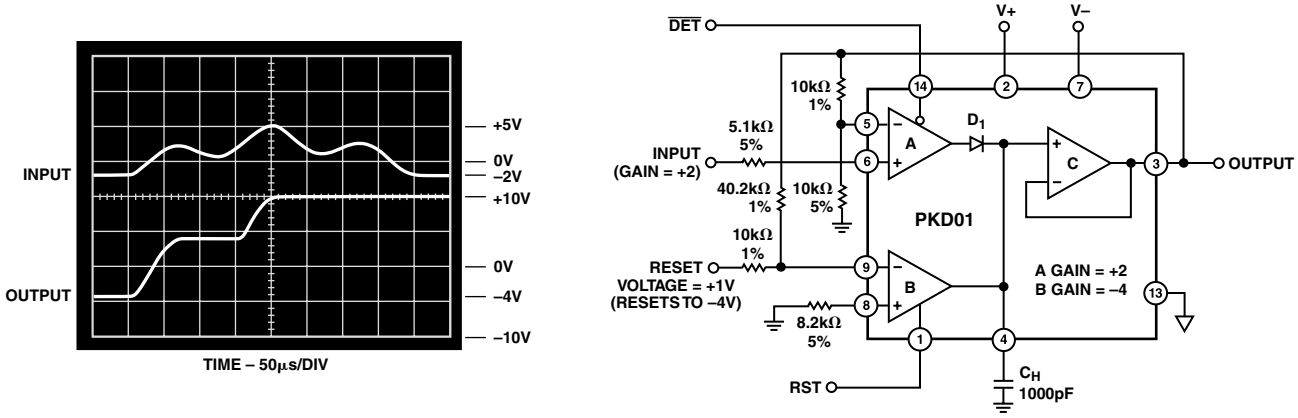


Figure 14. Positive Peak Detector with Gain

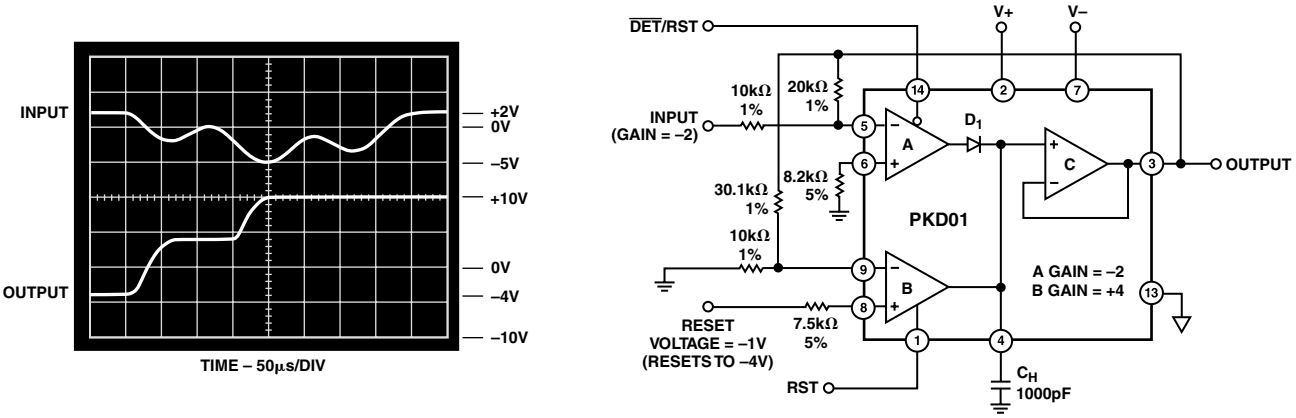


Figure 15. Negative Peak Detector with Gain

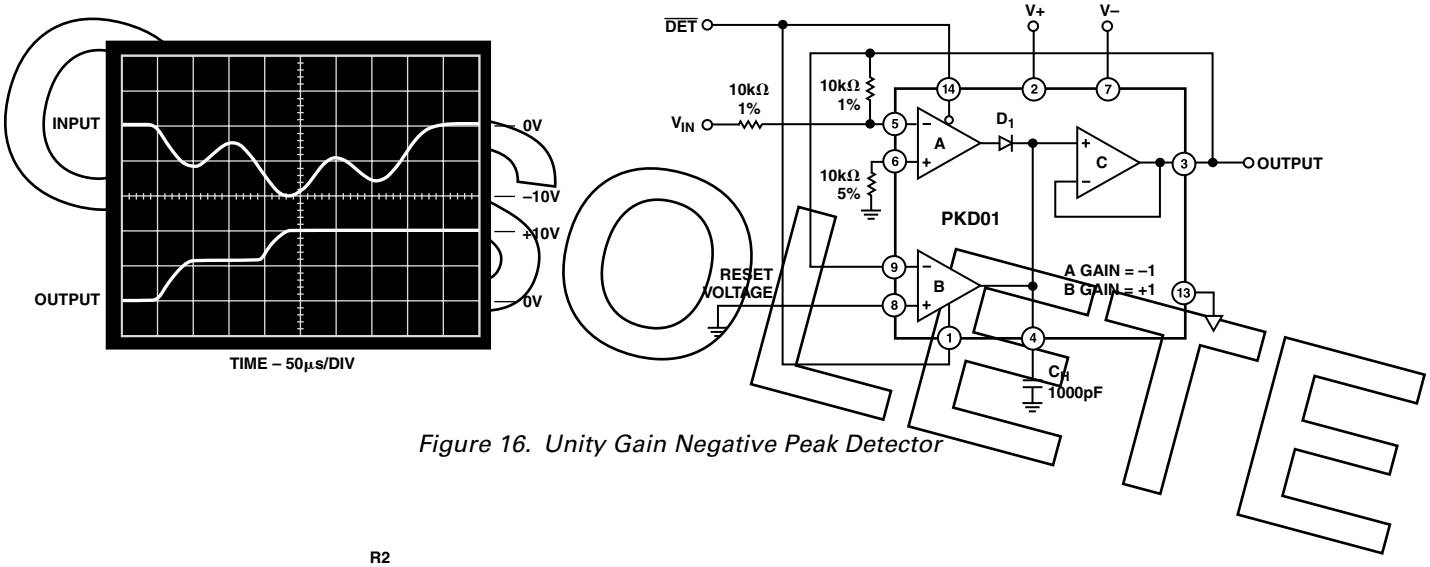
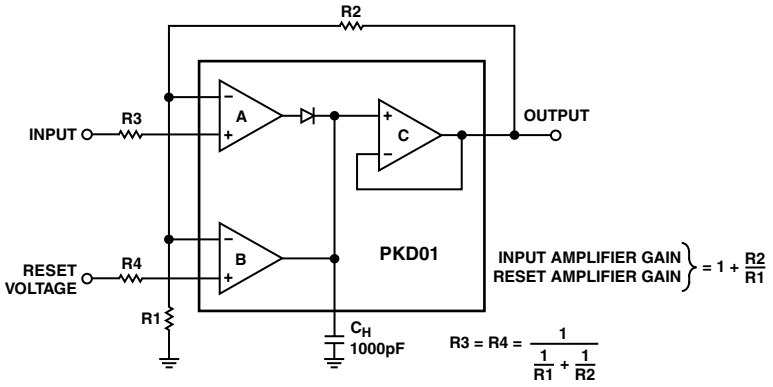


Figure 16. Unity Gain Negative Peak Detector



IF BOTH INPUT SIGNAL (AMPLIFIER A INPUT) AND THE RESET VOLTAGE (AMPLIFIER B INPUT) HAVE THE SAME POSITIVE VOLTAGE GAIN, THE GAIN CAN BE SET BY A SINGLE VOLTAGE DIVIDER FOR BOTH INPUT AMPLIFIERS.

NOTE:
R1, R2, R3 AND R4 > 5kΩ

Figure 17. Alternate Gain Configuration

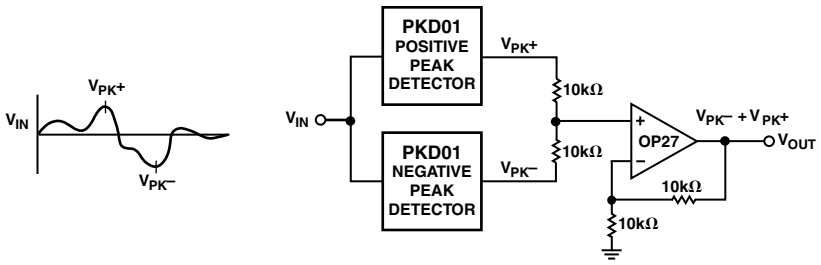


Figure 18. Peak-to-Peak Detector

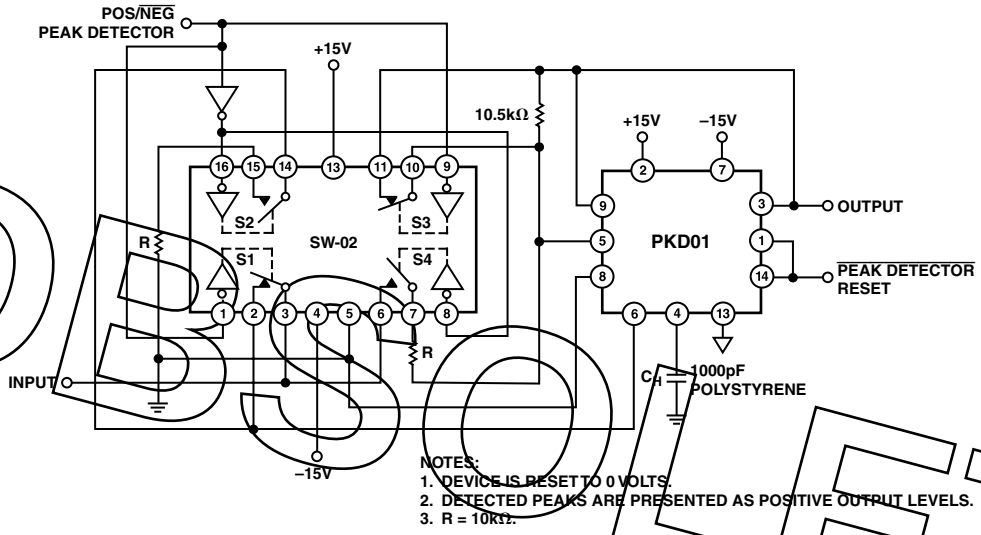


Figure 19. Logic Selectable Positive or Negative Peak Detector

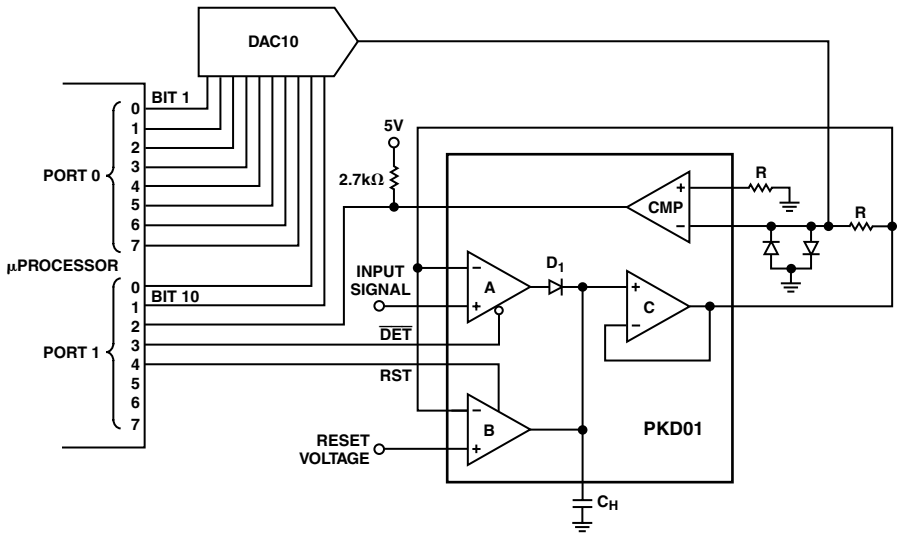


Figure 20. Peak Reading A/D Converter

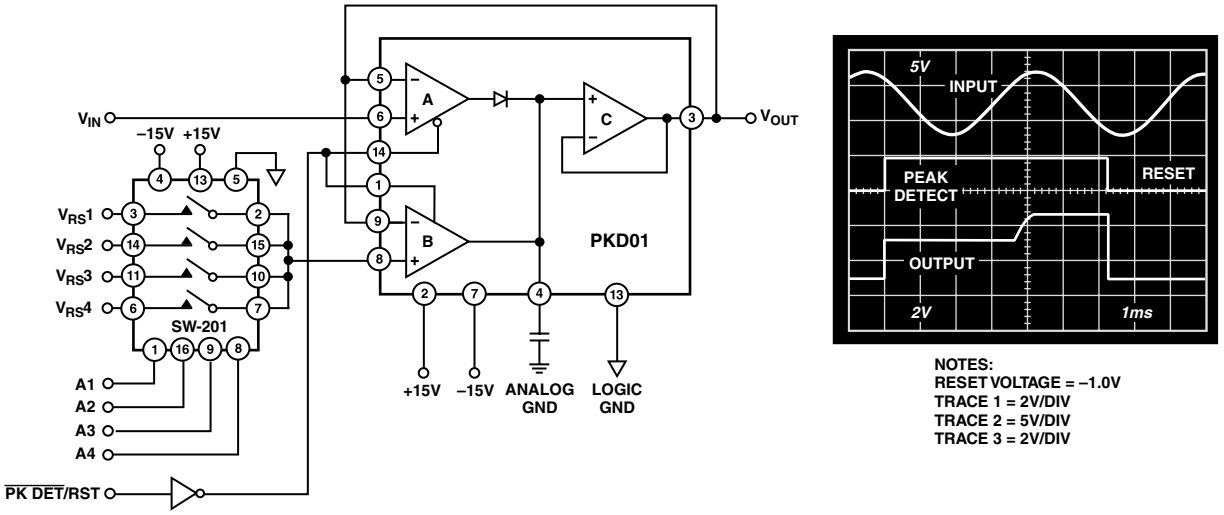


Figure 21. Positive Peak Detector with Selectable Reset Voltage

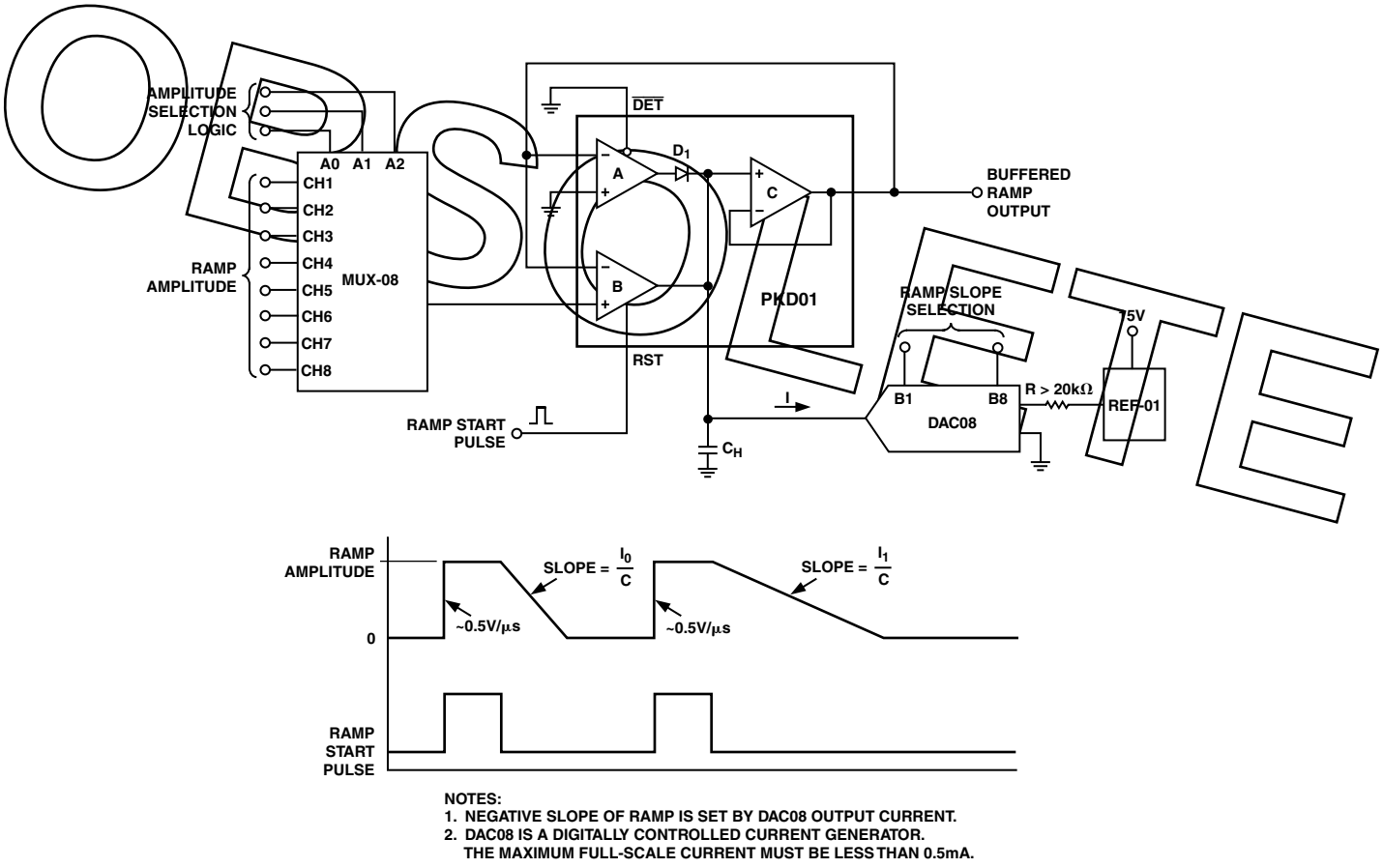
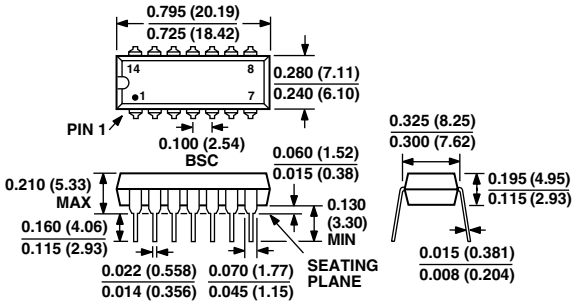


Figure 22. Programmable Low Frequency Ramp Generator

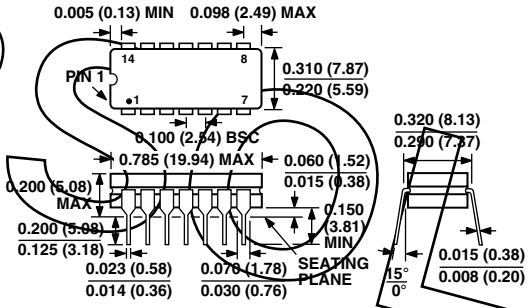
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP (PDIP)
(N-14)



14-Lead Cerdip
(Q-14)



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