

650ns Precision Sample and Hold Amplifier

The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Intersil Dielectric Isolation process to achieve a 650ns acquisition time to 12-bit accuracy and a droop rate of 0.01μV/μs. The circuit consists of an input transconductance amplifier capable of producing large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

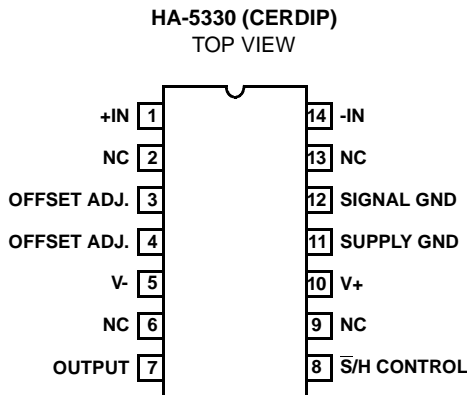
The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

The HA-5330 will operate at reduced supply voltages (to ±10V) with a reduced signal range. The MIL-STD-883 data sheet for this device is available on request.

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|-------------|------------------|--------------|-------------|
| HA1-5330-5 | 0 to 75 | 14 Ld CERDIP | F14.3 |

Pinout



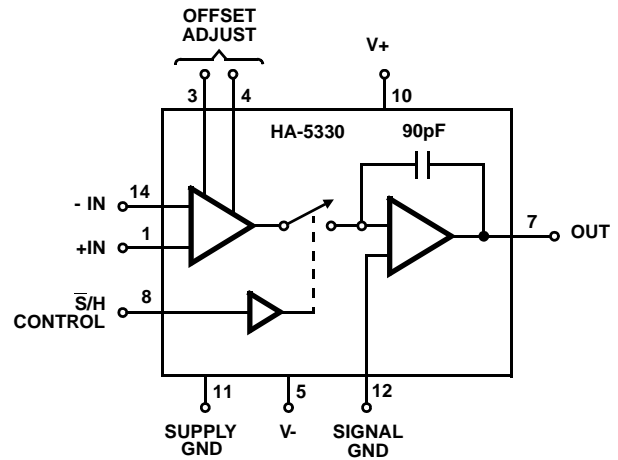
Features

- Very Fast Acquisition 500ns (0.1%) 650ns (0.01%)
- Low Droop Rate 0.01μV/μs
- Very Low Offset 0.2mV
- High Slew Rate. 90V/μs
- Wide Supply Range ±10V to ±20V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Functional Diagram



Absolute Maximum Ratings

Voltage between V+ and SUPPLY/SIG GND +20V
 Voltage between V- and SUPPLY/SIG GND -20V
 Voltage between SUPPLY GND and SIG GND ±2.0V
 Voltage between \bar{S}/H Control and SUPPLY/SIG GND +8V, -6V
 Differential Input Voltage 24V
 Output Current, Continuous (Note 1) ±17mA
 Supply Voltage Range (Typical) ±10V to ±20V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W) θ_{JC} (°C/W)
 CERDIP Package 66 16
 Maximum Junction Temperature (Ceramic Package, Note 2) . . . 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

Operating Conditions

Temperature Range 0°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Internal Power Dissipation may limit Output Current below ±17mA.
2. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below 175°C for the ceramic package.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 15V$; \bar{S}/H Control $V_{IL} = +0.8V$ (Sample); $V_{IH} = +2.0V$ (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN | TYP | MAX | UNITS |
|--|--------------------|-----------|-----------------|-----------------|-------|-------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Range | | Full | ±10 | - | - | V |
| Input Resistance (Note 4) | | 25 | 5 | 15 | - | MΩ |
| Input Capacitance | | 25 | - | 3 | - | pF |
| Offset Voltage | | 25 | - | 0.2 | - | mV |
| | | Full | - | - | 1.5 | mV |
| Offset Voltage Temperature Coefficient | | Full | - | 1 | 10 | μV/°C |
| Bias Current | | 25 | - | ±20 | - | nA |
| | | Full | - | - | ±300 | nA |
| Offset Current | | 25 | - | 20 | - | nA |
| | | Full | - | - | 300 | nA |
| Common Mode Range | | Full | ±10 | - | - | V |
| CMRR | $V_{CM} = \pm 10V$ | Full | 86 | 100 | - | dB |
| TRANSFER CHARACTERISTICS | | | | | | |
| Gain | DC | Full | 2×10^6 | 2×10^7 | - | V/V |
| Gain Bandwidth Product | Note 12 | 25 | - | 4.5 | - | MHz |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage | | Full | ±10 | - | - | V |
| Output Current | | Full | ±10 | - | - | mA |
| Full Power Bandwidth (Note 6) | | 25 | - | 1.4 | - | MHz |
| Output Resistance | Hold Mode | 25 | - | 0.2 | - | Ω |
| | Sample Mode | 25 | - | 10^{-5} | 0.001 | Ω |
| Total Output Noise, DC to 4MHz | Sample Mode | | - | 230 | - | μV _{RMS} |
| | Hold Mode | 25 | - | 190 | - | μV _{RMS} |
| TRANSIENT RESPONSE | | | | | | |
| Rise Time | Note 5 | 25 | - | 70 | - | ns |
| Overshoot | Note 5 | 25 | - | 10 | - | % |

Electrical Specifications $V_{SUPPLY} = \pm 15V$; S/H Control $V_{IL} = +0.8V$ (Sample): $V_{IH} = +2.0V$ (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN | TYP | MAX | UNITS |
|--------------------------------------|-----------------------------|-----------|-----|------|-----|-------|
| Slew Rate | Note 7 | 25 | - | 90 | - | V/μs |
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| Input Voltage | V_{IH} | Full | 2.0 | - | - | V |
| | V_{IL} | Full | - | - | 0.8 | V |
| Input Current | $V_{IL} = 0V$ | Full | - | 10 | 40 | μA |
| | $V_{IH} = 5V$ | Full | - | 10 | 40 | μA |
| SAMPLE/HOLD CHARACTERISTICS | | | | | | |
| Acquisition Time | To 0.1%, Note 8 | 25 | - | 500 | - | ns |
| | | Full | - | - | 700 | ns |
| | To 0.01%, Note 8 | 25 | - | 650 | - | ns |
| | | Full | - | - | 900 | ns |
| Aperture Time (Note 4) | | 25 | - | 20 | - | ns |
| Effective Aperture Delay Time | | 25 | -50 | -25 | 0 | ns |
| Aperture Uncertainty | | 25 | - | 0.1 | - | ns |
| Droop Rate (Note 9) | | 25 | - | 0.01 | - | μV/μs |
| | | Full | - | - | 10 | μV/μs |
| Hold Step Error | Note 10 | 25 | - | 0.5 | - | mV |
| Hold Mode Settling Time | To 0.01% | 25 | - | 100 | 200 | ns |
| Hold Mode Feedthrough | 20V _{P-P} , 100kHz | Full | - | -88 | - | dB |
| POWER SUPPLY CHARACTERISTICS | | | | | | |
| Positive Supply Current | | Full | - | 18 | 24 | mA |
| Negative Supply Current | | Full | - | 19 | 25 | mA |
| Power Supply Rejection | Note 11 | Full | 86 | 100 | - | dB |

NOTES:

- Derived from computer simulation only; not tested.
- $V_I = 200mV$ Step; $R_L = 2k\Omega$; $C_L = 50pF$.
- Full power bandwidth based on slew rate measurement using: $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$. Distortion of wave shape occurs beyond 100kHz due to slew rate enhancement circuitry.
- $V_O = 20V$ Step; $R_L = 2k\Omega$; $C_L = 50pF$.
- $V_O = 10V$ Step; $R_L = 2k\Omega$; $C_L = 50pF$.
- This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
- $V_{IN} = 0V$; $V_{IH} = +3.5V$; $t_R = 22ns$ (V_{IL} to V_{IH}). See graph.
- Based on a 3V delta in each supply, i.e. $15V \pm 1.5V_{DC}$.
- $V_{OUT} = 200mV_{P-P}$, $R_L = 2k\Omega$, $C_L = 50pF$.

Application Information

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuit ideas. See the Intersil Application Note AN517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01µF to 0.1µF, ceramic) should be provided from each power supply terminal to the Supply GND Terminal on pin 11.

Typical Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast successive - approximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

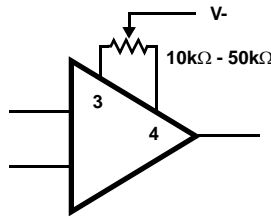


FIGURE 1. HA-5330 OFFSET ADJUST

The ideal ground connections are pin 11 (Supply Ground) directly to the system Supply Common, and pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground).

Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on the internal capacitor).

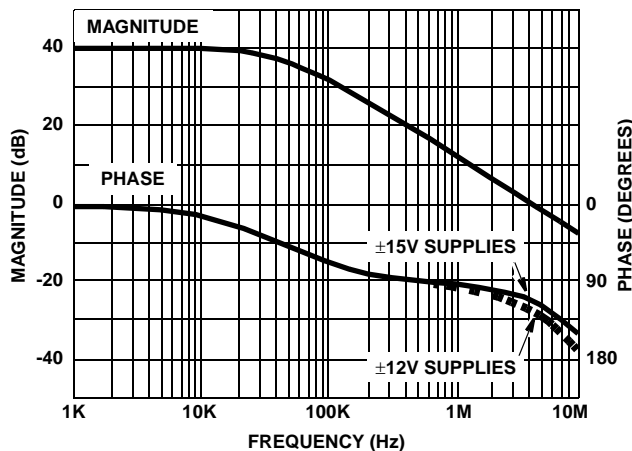


FIGURE 2. MAGNITUDE AND PHASE RESPONSE (CLOSED LOOP GAIN = 100)

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the \bar{S}/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within $\pm 0.1\%$ or $\pm 0.01\%$. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".

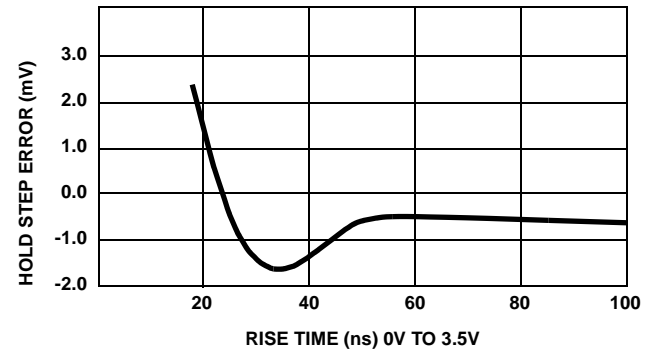


FIGURE 3. HOLD STEP ERROR vs \bar{S}/H CONTROL RISE TIME

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the \bar{S}/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the \bar{S}/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

HA-5330

Die Characteristics

DIE DIMENSIONS:

99 mils x 166 mils x 19 mils
2510 μ m x 4210 μ m x 483 μ m

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16k \AA \pm 2k \AA

PASSIVATION:

Type: Nitride (Si₃N₄) over Silox (SiO₂, 5% Phos.)
Silox Thickness: 12k \AA \pm 2k \AA
Nitride Thickness: 3.5k \AA \pm 1.5k \AA

SUBSTRATE POTENTIAL (POWERED UP):

Signal GND

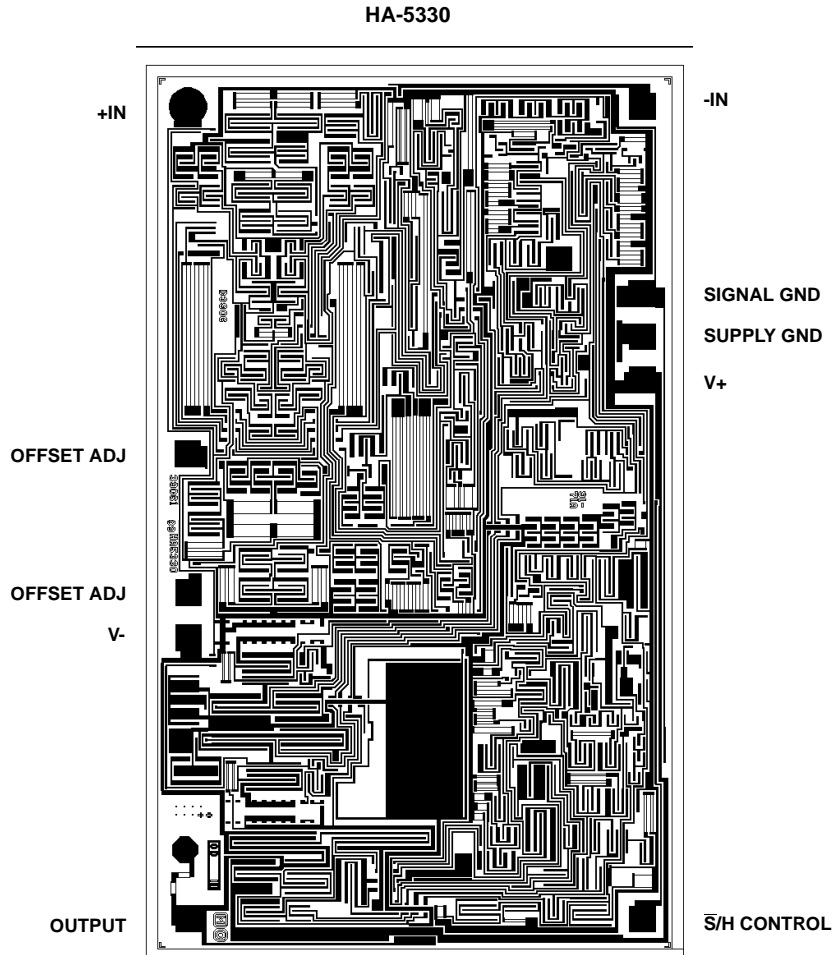
TRANSISTOR COUNT:

205

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com