2 ADC, 8 DAC, 96 kHz, 24-Bit Σ-Δ Codecs

AD1835A

FEATURES

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports up to 96 kHz Sample Rates
- 192 kHz Sample Rate Available on 1 DAC
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Σ-Δ Modulators with Perfect Differential Linearity Restoration for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs—Least Sensitive to Jitter
- Differential Output for Optimum Performance
  - ADCs: –95 dB THD + N, 105 dB SNR, and Dynamic Range
  - DACs: –95 dB THD + N, 108 dB SNR, and Dynamic Range
- On-Chip Volume Controls per Channel with 1024-Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-emphasis Processing
- Supports 256 × f_S, 512 × f_S, and 768 × f_S Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S Compatible, and DSP Serial Port Modes
- TDM Interface Mode Supports 8-In/8-Out Using a Single SHARC® SPORT
- 52-Lead MQFP Plastic Package

APPLICATIONS

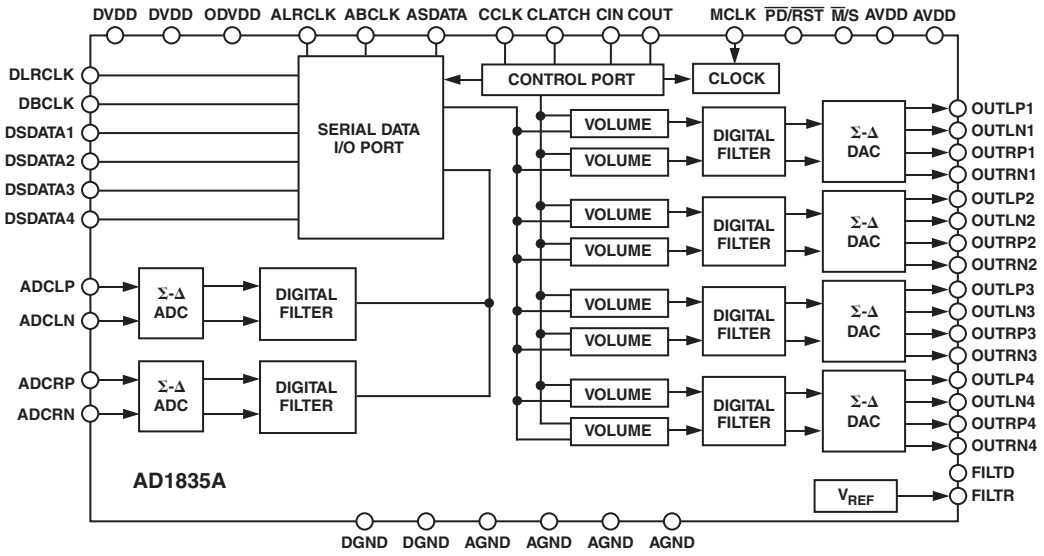
- DVD Video and Audio Players
- Home Theater Systems
- Automotive Audio Systems
- Audio/Visual Receivers
- Digital Audio Effects Processors

PRODUCT OVERVIEW

The AD1835A is a high performance, single-chip codec featuring four stereo DACs and one stereo ADC. Each DAC comprises a high performance digital interpolation filter, a multibit Σ-Δ modulator featuring Analog Devices' patented technology, and a continuous-time voltage out analog section.

(continued on page 11)

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD1835A–SPECIFICATIONS

TEST CONDITIONS

Supply Voltages (AVDD, DVDD)	5.0 V
Ambient Temperature	25°C
Input Clock	12.288 MHz (256 × f_S Mode)
ADC Input Signal	1.0078125 kHz, –1 dBFS (Full Scale)
DAC Input Signal	1.0078125 kHz, 0 dBFS (Full Scale)
Input Sample Rate (f_S)	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 Bits
Load Capacitance	100 pF
Load Impedance	47 kΩ

Performance of all channels is identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).

Parameter	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS				
ADC Resolution		24		Bits
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
No Filter	100	103		dB
A-Weighted (48 kHz and 96 kHz)		105		dB
Total Harmonic Distortion + Noise (THD + N)				
48 kHz		–95	–88.5	dB
96 kHz		–95	–87.5	dB
Interchannel Isolation		100		dB
Interchannel Gain Mismatch		0.025		dB
Analog Inputs				
Differential Input Range (± Full Scale)	–2.828		+2.828	V
Common-Mode Input Voltage		2.25		V
Input Impedance		4		kΩ
Input Capacitance		15		pF
V_{REF}		2.25		V
DC Accuracy				
Gain Error		±5		%
Gain Drift		35		ppm/°C
DIGITAL-TO-ANALOG CONVERTERS				
DAC Resolution		24		Bits
Dynamic Range (20 Hz to 20 kHz, –60 dBFS Input)				
No Filter	103	105		dB
With A-Weighted Filter (48 kHz and 96 kHz)	105	108		dB
Total Harmonic Distortion + Noise (48 kHz and 96 kHz)		–95	–90	dB
Interchannel Isolation		110		dB
DC Accuracy				
Gain Error		±4.0		%
Interchannel Gain Mismatch		0.025		dB
Gain Drift		200		ppm/°C
Interchannel Crosstalk (EIAJ Method)		–120		dB
Interchannel Phase Deviation		±0.1		Degrees
Volume Control Step Size (1023 Linear Steps)		0.098		%
Volume Control Range (Maximum Attenuation)		60		dB
Mute Attenuation		–100		dB
De-emphasis Gain Error		±0.1		dB
Full-Scale Output Voltage at Each Pin (Single-Ended)		1.0 (2.8)		V rms (V p-p)
Output Resistance at Each Pin		180		Ω
Common-Mode Output Voltage		2.25		V
ADC DECIMATION FILTER, 48 kHz*				
Pass Band		21.77		kHz
Pass-Band Ripple		±0.01		dB
Stop Band		26.23		kHz
Stop-Band Attenuation		120		dB
Group Delay		910		µs

Parameter	Min	Typ	Max	Unit
ADC DECIMATION FILTER, 96 kHz*				
Pass Band		43.54		kHz
Pass-Band Ripple		±0.01		dB
Stop Band		52.46		kHz
Stop-Band Attenuation		120		dB
Group Delay		460		µs
DAC INTERPOLATION FILTER, 48 kHz*				
Pass Band			21.77	kHz
Pass-Band Ripple		±0.06		dB
Stop Band	28			kHz
Stop-Band Attenuation	55			dB
Group Delay		340		µs
DAC INTERPOLATION FILTER, 96 kHz*				
Pass Band			43.54	kHz
Pass-Band Ripple		±0.06		dB
Stop Band	52			kHz
Stop-Band Attenuation	55			dB
Group Delay		160		µs
DAC INTERPOLATION FILTER, 192 kHz*				
Pass Band			81.2	kHz
Pass-Band Ripple		±0.06		dB
Stop Band	97			kHz
Stop-Band Attenuation	80			dB
Group Delay		110		µs
DIGITAL I/O				
Input Voltage High	2.4			V
Input Voltage Low			0.8	V
Output Voltage High	ODVDD – 0.4			V
Output Voltage Low			0.4	V
Leakage Current			±10	µA
POWER SUPPLIES				
Supply Voltage (AVDD and DVDD)	4.5	5.0	5.5	V
Supply Voltage (ODVDD)	3.0		DVDD	V
Supply Current I_{ANALOG}		84	95	mA
Supply Current I_{ANALOG}, Power-Down		55	67	mA
Supply Current $I_{DIGITAL}$		64	74	mA
Supply Current $I_{DIGITAL}$, Power-Down		1	4.5	mA
Dissipation				
Operation, Both Supplies		740		mW
Operation, Analog Supply		420		mW
Operation, Digital Supply		320		mW
Power-Down, Both Supplies		280		mW
Power Supply Rejection Ratio				
1 kHz, 300 mV p-p Signal at Analog Supply Pins		–70		dB
20 kHz, 300 mV p-p Signal at Analog Supply Pins		–75		dB

*Guaranteed by design.

Specifications subject to change without notice.

TIMING SPECIFICATIONS

Parameter		Min	Max	Unit	Comments
MASTER CLOCK AND RESET					
t_{MH}	MCLK High	15		ns	
t_{ML}	MCLK Low	15		ns	
t_{PDR}	$\overline{PD}/\overline{RST}$ Low	20		ns	
SPI® PORT					
t_{CCH}	CCLK High	40		ns	
t_{CCL}	CCLK Low	40		ns	
t_{CCP}	CCLK Period	80		ns	
t_{CDS}	CDATA Setup	10		ns	To CCLK Rising
t_{CDH}	CDATA Hold	10		ns	From CCLK Rising
t_{CLS}	CLATCH Setup	10		ns	To CCLK Rising
t_{CLH}	CLATCH Hold	10		ns	From CCLK Rising
t_{COE}	COUT Enable		15	ns	From CLATCH Falling
t_{COD}	COUT Delay		20	ns	From CCLK Falling
t_{COTS}	COUT Three-State		25	ns	From CLATCH Rising
DAC SERIAL PORT (48 kHz and 96 kHz)					
Normal Mode (Slave)					
t_{DBH}	DBCLK High	60		ns	
t_{DBL}	DBCLK Low	60		ns	
f_{DB}	DBCLK Frequency	$64 \times f_S$			
t_{DLS}	DLRCLK Setup	10		ns	To DBCLK Rising
t_{DLH}	DLRCLK Hold	10		ns	From DBCLK Rising
t_{DDS}	DSDATA Setup	10		ns	To DBCLK Rising
t_{DDH}	DSDATA Hold	10		ns	From DBCLK Rising
Packed 128/256 Modes (Slave)					
t_{DBH}	DBCLK High	15		ns	
t_{DBL}	DBCLK Low	15		ns	
f_{DB}	DBCLK Frequency	$256 \times f_S$			
t_{DLS}	DLRCLK Setup	10		ns	To DBCLK Rising
t_{DLH}	DLRCLK Hold	10		ns	From DBCLK Rising
t_{DDS}	DSDATA Setup	10		ns	To DBCLK Rising
t_{DDH}	DSDATA Delay	10		ns	From DBCLK Rising
ADC SERIAL PORT (48 kHz and 96 kHz)					
Normal Mode (Master)					
t_{ABD}	ABCLK Delay		25	ns	From MCLK Rising Edge
t_{ALD}	ALRCLK Delay Low		5	ns	From ABCLK Falling Edge
t_{ABDD}	ASDATA Delay		10	ns	From ABCLK Falling Edge
Normal Mode (Slave)					
t_{ABH}	ABCLK High	60		ns	
t_{ABL}	ABCLK Low	60		ns	
f_{AB}	ABCLK Frequency	$64 \times f_S$			
t_{ALS}	ALRCLK Setup	5		ns	To ABCLK Rising
t_{ALH}	ALRCLK Hold	15		ns	From ABCLK Rising
t_{ABDD}	ASDATA Delay		15	ns	From ABCLK Falling Edge
Packed 128/256 Mode (Master)					
t_{PABD}	ABCLK Delay		40	ns	From MCLK Rising Edge
t_{PALD}	LRCLK Delay		5	ns	From ABCLK Falling Edge
t_{PABDD}	ASDATA Delay		10	ns	From ABCLK Falling Edge

Parameter		Min	Max	Unit	Comments
TDM256 MODE (Master, 48 kHz and 96 kHz)					
t_{TBD}	BCLK Delay		40	ns	From MCLK Rising
t_{FSD}	FSTDM Delay		5	ns	From BCLK Rising
t_{TABDD}	ASDATA Delay		10	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	15		ns	To BCLK Falling
t_{TDDH}	DSDATA1 Hold	15		ns	From BCLK Falling
TDM256 MODE (Slave, 48 kHz and 96 kHz)					
f_{AB}	BCLK Frequency	256 × f_S			
t_{TBCH}	BCLK High	17		ns	
t_{TBCL}	BCLK Low	17		ns	
t_{TFS}	FSTDM Setup	10		ns	To BCLK Falling
t_{TFH}	FSTDM Hold	10		ns	From BCLK Falling
t_{TBDD}	ASDATA Delay		15	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	15		ns	To BCLK Falling
t_{TDDH}	DSDATA1 Hold	15		ns	From BCLK Falling
TDM512 MODE (Master, 48 kHz)					
t_{TBD}	BCLK Delay		40	ns	From MCLK Rising
t_{FSD}	FSTDM Delay		5	ns	From BCLK Rising
t_{TABDD}	ASDATA Delay		10	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	15		ns	To BCLK Falling
t_{TDDH}	DSDATA1 Hold	15		ns	From BCLK Falling
TDM512 MODE (Slave, 48 kHz)					
f_{AB}	BCLK Frequency	512 × f_S			
t_{TBCH}	BCLK High	17		ns	
t_{TBCL}	BCLK Low	17		ns	
t_{TFS}	FSTDM Setup	10		ns	To BCLK Falling
t_{TFH}	FSTDM Hold	10		ns	From BCLK Falling
t_{TBDD}	ASDATA Delay		15	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	15		ns	To BCLK Falling
t_{TDDH}	DSDATA1 Hold	15		ns	From BCLK Falling
AUXILIARY INTERFACE (48 kHz and 96 kHz)					
t_{AXDS}	AAUXDATA Setup	10		ns	To AUXBCLK Rising
t_{AXDH}	AAUXDATA Hold	10		ns	From AUXBCLK Rising
f_{ABP}	AUXBCLK Frequency	64 × f_S			
Slave Mode					
t_{AXBH}	AUXBCLK High	15		ns	
t_{AXBL}	AUXBCLK Low	15		ns	
t_{AXLS}	AUXLRCLK Setup	10		ns	To AUXBCLK Rising
t_{AXLH}	AUXLRCLK Hold	10		ns	From AUXBCLK Rising
Master Mode					
$t_{AUXLRCLK}$	AUXLRCLK Delay	15		ns	From AUXBCLK Falling
$t_{AUXBCLK}$	AUXBCLK Delay	20		ns	From MCLK Rising

Specifications subject to change without notice.

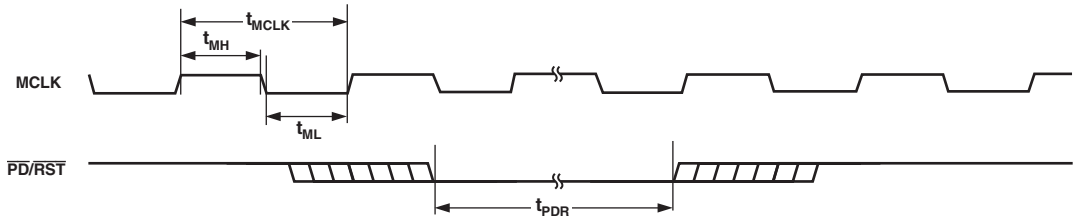

Figure 1. MCLK and $\overline{PD}/\overline{RST}$ Timing

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

AVDD, DVDD, ODVDD to AGND, DGND . . –0.3 V to +6.0 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . –0.3 V to ODVDD + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to AVDD + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TEMPERATURE RANGE

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		+85	°C
Storage	–65		+150	°C

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1835AAS	–40°C to +85°C	52-Lead MQFP	S-52-1
AD1835AAS-REEL	–40°C to +85°C	52-Lead MQFP	S-52-1
AD1835AASZ*	–40°C to +85°C	52-Lead MQFP	S-52-1
AD1835AASZ-REEL*	–40°C to +85°C	52-Lead MQFP	S-52-1
EVAL-AD1835AEB		Evaluation Board	

*Z = Pb-free part.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1835A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.