DATA SHEET

TDA8787
10-bit, 3.0 V analog-to-digital interface for CCD cameras

Preliminary specification
Supersedes data of 1998 Mar 27
File under Integrated Circuits, IC02

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Philips
Semiconductors

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10-bit, 3.0 V analog-to-digital interface for CCD cameras

TDA8787

FEATURES

- Correlated Double Sampling (CDS), Automatic Gain Control (AGC), 10-bit Analog-to-Digital Converter (ADC) and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain range of 36 dB (in steps of 0.1 dB)
- Low power consumption of only 190 mW (typ.)
- Power consumption in standby mode of 4.5 mW (typ.)
- 3.0 V operation and 2.5 to 3.6 V operation for the digital outputs
- Active control pulses polarity selectable via serial interface
- 8-bit DAC included for analog settings
- TTL compatible inputs, CMOS compatible outputs.

APPLICATIONS

- Low-power, low-voltage CCD camera systems.

GENERAL DESCRIPTION

The TDA8787 is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC and a low-power 10-bit ADC together with its reference voltage regulator.

AGC gain is controlled via the serial interface.

The ADC input clamp level is controlled via the serial interface.

An additional DAC is provided for additional system controls; its output voltage range is 1.0 V (p-p) which is available at pin OFDOUT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	3.6	V
I_{CCA}	analog supply current	all clamps active	–	55	70	mA
I_{CCD}	digital supply current		–	8	11	mA
I_{CCO}	digital outputs supply current	f_{pix} = 18 MHz; C_L = 20 pF; input ramp response time is 800 μs	–	1	2	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{i(CDS)(p-p)}$	maximum CDS input voltage (peak-to-peak value)	V_{CC} = 2.85 V	650	–	–	mV
		$V_{CC} \geq$ 3.0 V	800	–	–	mV
$f_{pix(max)}$	maximum pixel rate		18	–	–	MHz
$f_{pix(min)}$	minimum pixel rate		5	–	–	MHz
DR_{AGC}	AGC dynamic range		–	36	–	dB
$N_{tot(rms)}$	total noise from CDS input to ADC output	AGC gain = 0 dB; see Fig.8	–	0.25	–	LSB
P_{tot}	total power consumption	$V_{CCA} = V_{CCD} = V_{CCO}$ = 3 V	–	190	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8787HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

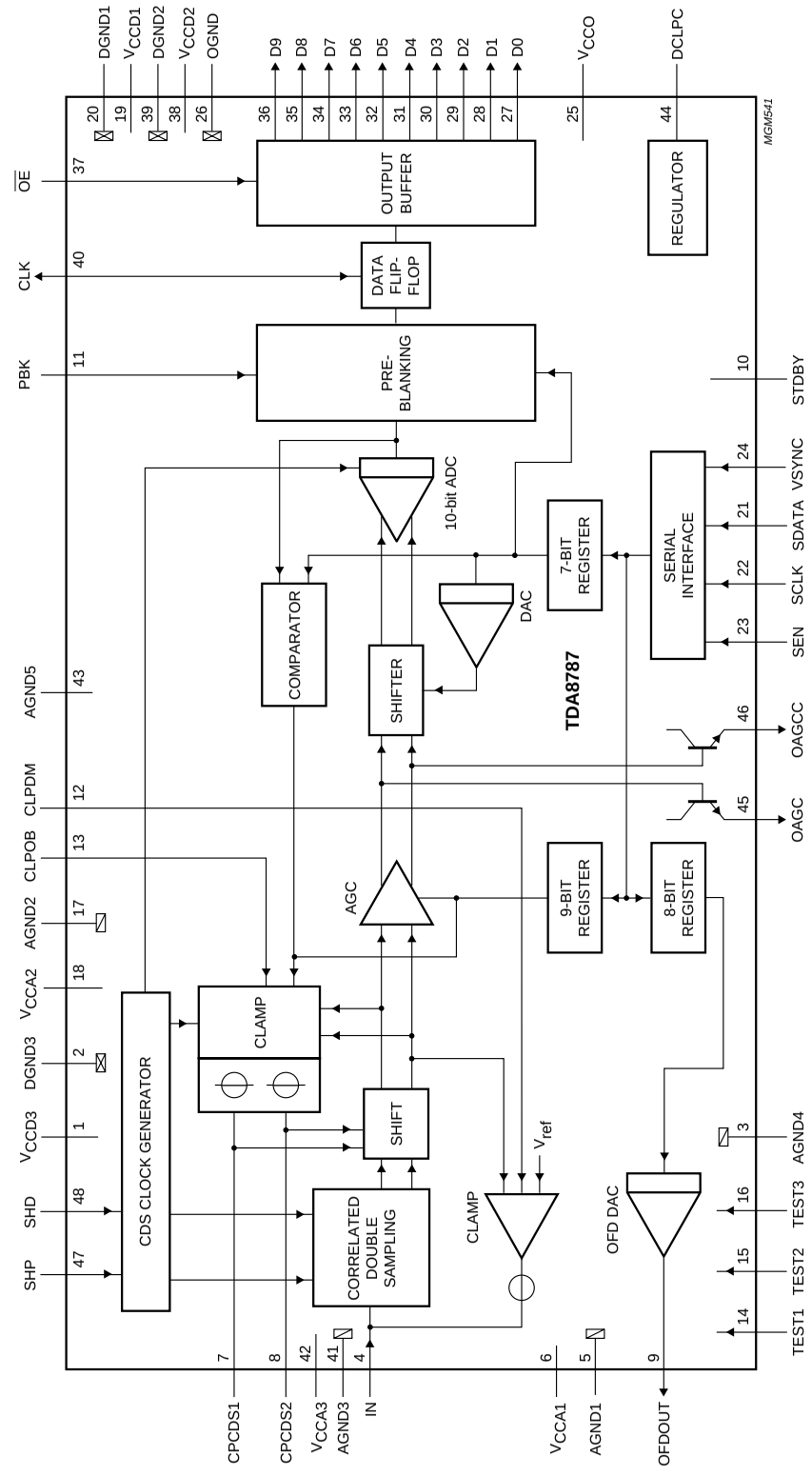


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCD3}	1	digital supply voltage 3
DGND3	2	digital ground 3
AGND4	3	analog ground 4
IN	4	input signal from CCD
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
CPCDS1	7	clamp storage capacitor pin 1
CPCDS2	8	clamp storage capacitor pin 2
OFDOUT	9	analog output of the additional 8-bit control DAC
STDBY	10	standby mode control input (LOW: TDA8787 active; HIGH: TDA8787 standby)
PBK	11	pre-blanking control input
CLPDM	12	clamp pulse input at dummy pixel
CLPOB	13	clamp pulse input at optical black
TEST1	14	test pin input 1 (should be connected to AGND2)
TEST2	15	test pin input 2 (should be connected to AGND1)
TEST3	16	test pin input 3 (should be connected to AGND2)
AGND2	17	analog ground 2
V_{CCA2}	18	analog supply voltage 2
V_{CCD1}	19	digital supply voltage 1
DGND1	20	digital ground 1
SDATA	21	serial data input for serial interface control
SCLK	22	serial clock input for serial interface
SEN	23	strobe pin for serial interface
VSYNC	24	vertical sync pulse input
V_{CCO}	25	output supply voltage
OGND	26	digital output ground
D0	27	ADC digital output 0 (LSB)
D1	28	ADC digital output 1
D2	29	ADC digital output 2
D3	30	ADC digital output 3
D4	31	ADC digital output 4
D5	32	ADC digital output 5
D6	33	ADC digital output 6
D7	34	ADC digital output 7
D8	35	ADC digital output 8
D9	36	ADC digital output 9 (MSB)
$\overline{OE}$	37	output enable control input (LOW: outputs active; HIGH: outputs in high impedance)
V_{CCD2}	38	digital supply 2
DGND2	39	digital ground 2
CLK	40	data clock input

SYMBOL	PIN	DESCRIPTION
AGND3	41	analog ground 3
V_{CCA3}	42	analog supply 3
AGND5	43	analog ground 5
DCLPC	44	regulator decoupling pin
OAGC	45	AGC output (test pin)
OAGCC	46	AGC complementary output (test pin)
SHP	47	preset sample-and-hold pulse input
SHD	48	data sample-and-hold pulse input

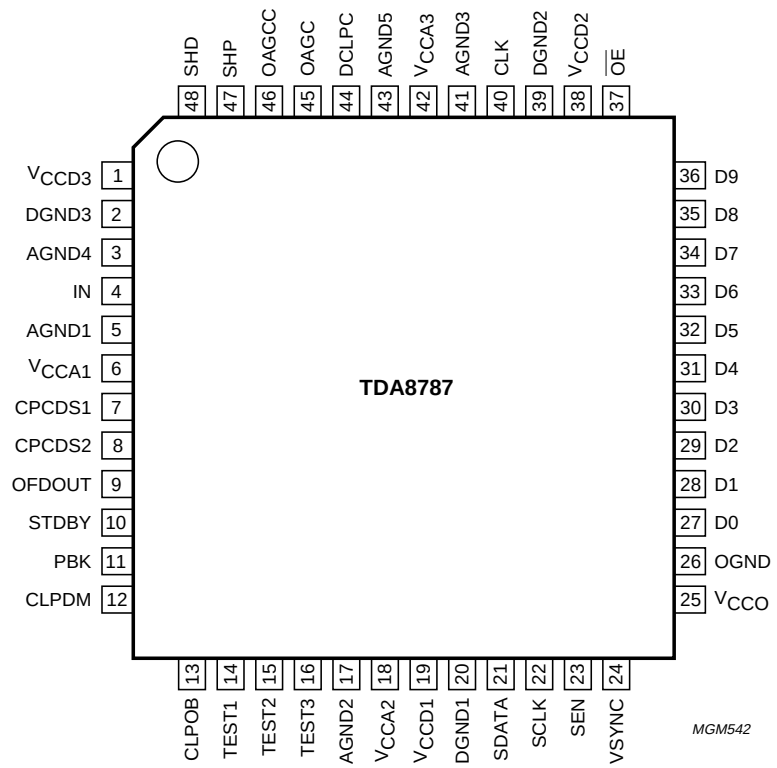


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	between V_{CCA} and V_{CCD}		–1.0	+1.0	V
	between V_{CCA} and V_{CCO}		–1.0	+1.0	V
	between V_{CCD} and V_{CCO}		–1.0	+1.0	V
V_i	input voltage	referenced to AGND	–0.3	+7.0	V
I_o	data output current		–	±10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+75	°C
T_j	junction temperature		–	150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 and +7.0 V provided that the supply voltage difference ΔV_{CC} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

CHARACTERISTICS

V_{CCA} = V_{CCD} = 3.0 V; V_{CCO} = 2.6 V; f_{pix} = 18 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	3.6	V
I_{CCA}	analog supply current	all clamps active	–	55	70	mA
I_{CCD}	digital supply current		–	8	11	mA
I_{CCO}	digital outputs supply current	C_L = 20 pF on all data outputs; input ramp frequency	–	1	2	mA
Digital inputs						
INPUTS: SHP, SHD, STDBY, CLPDM, CLPOB, SCLK, SDATA, SEN, VSYNC, $\overline{OE}$ AND PBK						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	V_{CCD}	V
I_i	input current	$0 \leq V_i \leq V_{CCD}$	–2	–	+2	µA
Clamps						
GLOBAL CHARACTERISTICS OF THE CLAMP LOOPS						
$t_{W(clamp)}$	clamp active pulse width in number of pixels	AGC code = 383 for maximum 4 LSB error	18	–	–	pixels
INPUT CLAMP (DRIVEN BY CLPDM)						
$g_{m(CDS)}$	CDS input clamp transconductance		1.5	2.7	3.5	mS
OPTICAL BLACK CLAMP (DRIVEN BY CLPOB)						
G_{shift}	gain from CPCDS1 and 2 to AGC inputs		–	0.27	–	–
$I_{LSB(cp)}$	charge pump current for ±1 LSB error at ADC output	AGC code = 0	–	±350	–	µA
		AGC code = 383	–	±10	–	µA
$I_{push(cp)}$	available push current of the charge pump		–	650	–	µA
$I_{pull(cp)}$	available pull current of the charge pump		–	–650	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Correlated Double Sampling (CDS)						
$V_{i(CDS)(p-p)}$	maximum peak-to-peak CDS input amplitude (video signal)	V_{CC} = 2.85 V	650	–	–	mV
		$V_{CC} \geq$ 3.0 V	800	–	–	mV
$V_{reset(max)}$	maximum CDS input reset pulse amplitude		500	–	–	mV
$I_{i(IN)}$	input current into pin IN (pin 4)	at floating gate level	–1	–	+1	µA
$t_{CDS(min)}$	CDS control pulses minimum active time	video input = $V_{i(CDS)(p-p)}$; 2 LSB error at ADC output	11	15	–	ns
$t_{h(IN-SHP)}$	CDS input hold time (pin IN) compared to control pulse SHP	$V_{CCA} = V_{CCD}$ = 30 V; T_{amb} = 25 °C; see Fig.9	3	5	7	ns
$t_{h(IN-SHD)}$	CDS input hold time (pin IN) compared to control pulse SHD	$V_{CCA} = V_{CCD}$ = 30 V; T_{amb} = 25 °C; see Fig.9	3	5	7	ns
Amplifier						
DR_{AGC}	AGC dynamic range		–	36	–	dB
ΔG_{AGC}	maximum AGC gain step		–0.3	–	+0.3	dB
Analog-to-Digital Converter (ADC)						
LE_i	integral linearity error	f_{pix} = 18 MHz; ramp input	–	±1.3	±2.5	LSB
LE_d	differential linearity error	f_{pix} = 18 MHz; ramp input	–	±0.5	±0.9	LSB
Total chain characteristics (CDS + AGC + ADC)						
$f_{pix(max)}$	maximum pixel frequency		18	–	–	MHz
t_{CLKH}	CLK pulse width HIGH		15	–	–	ns
t_{CLKL}	CLK pulse width LOW		15	–	–	ns
$t_{d(SHD-CLK)}$	time delay between SHD and CLK	see Fig.9	10	–	–	ns
$t_{su(PBK-CLK)}$	set-up time of PBK compared to CLK		10	–	–	ns
$V_{i(IN)}$	video input dynamic signal for ADC full-scale output	AGC code = 00	800	–	–	mV
		AGC code = 383	12.7	–	–	mV
$N_{tot(rms)}$	total output noise (RMS value)	see Fig.8				
		AGC gain = 0 dB	–	0.25	–	LSB
		AGC gain = 9 dB	–	0.8	–	LSB
$O_{CCD(max)}$	maximum offset between CCD floating level and CCD dark pixel level		–70	–	+70	mV
$V_{n(i)(eq)(rms)}$	equivalent input noise voltage (RMS value)		–	110	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converter (OFDOUT DAC)						
$V_{OFDOUT(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)	R_i = 1 MΩ	–	1.0	–	V
$V_{OFDOUT(0)}$	DC output voltage for code 0		–	AGND	–	V
$V_{OFDOUT(255)}$	DC output voltage for code 255		–	AGND + 1.0	–	V
TC_{DAC}	DAC output range temperature coefficient		–	250	–	ppm/°C
Z_{OFDOUT}	DAC output impedance		–	2000	–	Ω
I_{OFDOUT}	OFD output current drive	static	–	–	100	µA
Digital outputs (f_{pix} = 18 MHz; C_L = 22 pF)						
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{CCO} – 0.5	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
I_{OZ}	output current in 3-state mode	0.5 V < V_o < V_{CCO}	–20	–	+20	µA
$t_{h(o)}$	output hold time	see Fig.9	11	–	–	ns
$t_{d(o)}$	output delay time	C_L = 22 pF; V_{CCO} = 3.0 V	–	28	tbf	ns
		C_L = 22 pF; V_{CCO} = 2.7 V	–	27	tbf	ns
C_L	output load capacitance		–	–	22	pF
Serial interface						
$f_{SCLK(max)}$	maximum frequency of serial interface		5	–	–	MHz

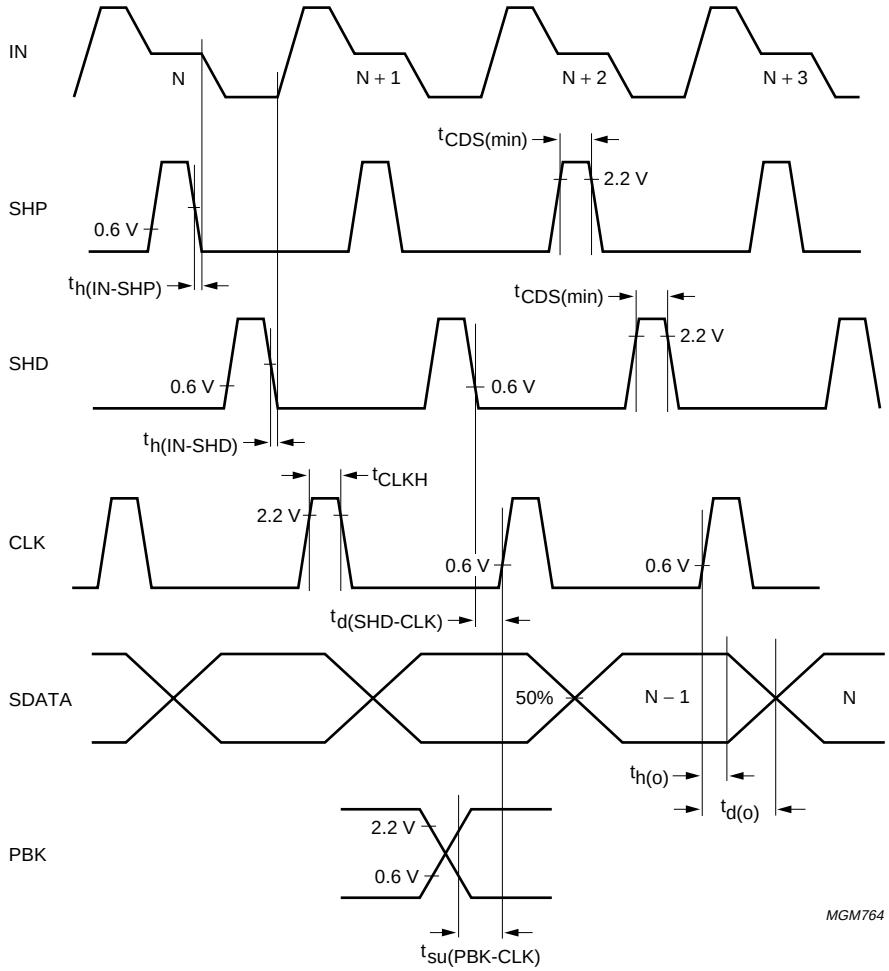


Fig.3 Pixel frequency timing diagram; all polarities active HIGH.

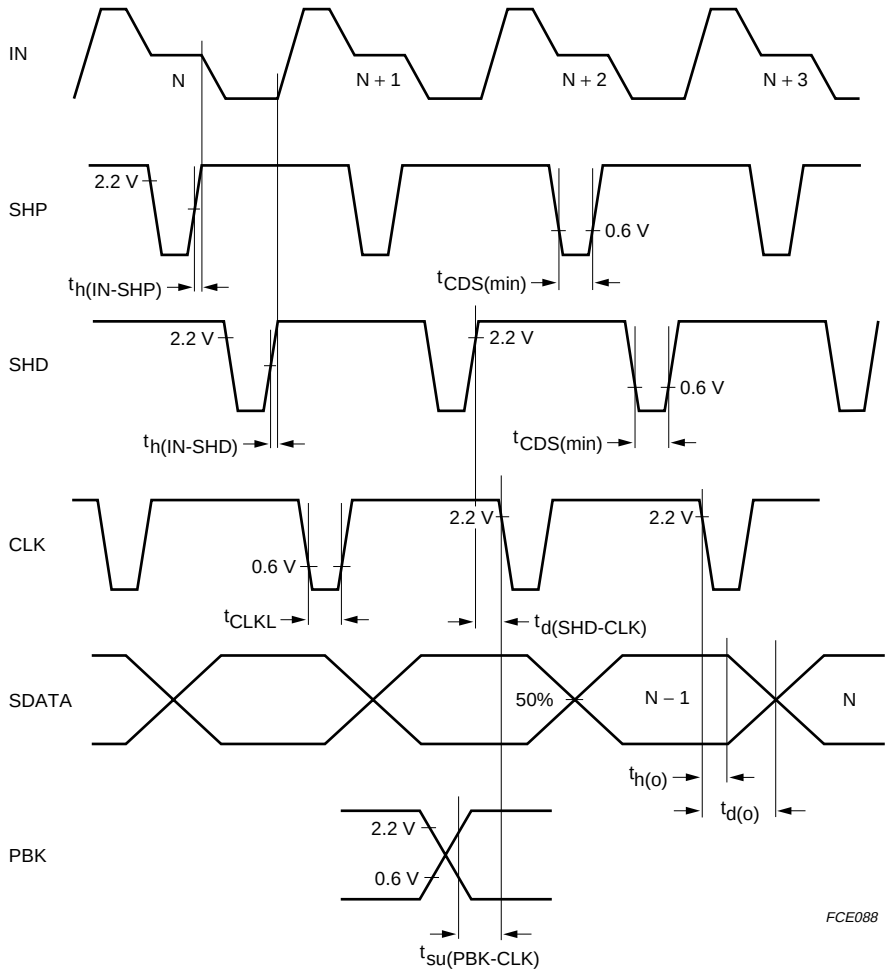


Fig.4 Pixel frequency timing diagram; all polarities active LOW.

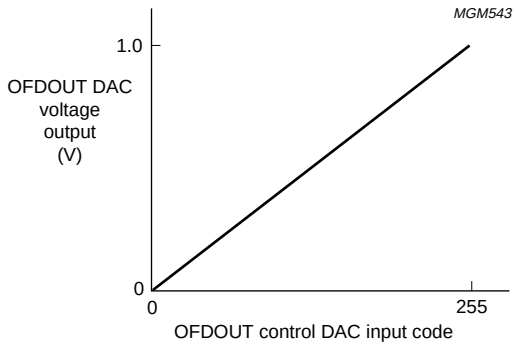
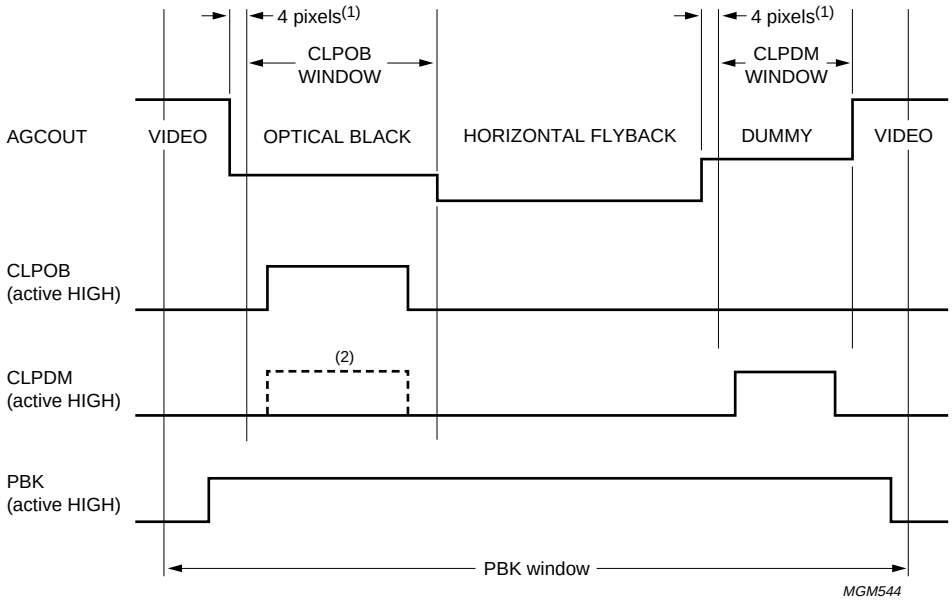


Fig.5 DAC voltage output as a function of DAC input code.



(1) In case the number of clamp pixels is limited to $18t_{W(clamp)}$; otherwise this timing interval can be smaller.
(2) When dummy pixels are not available.

Fig.6 Line frequency timing diagram.

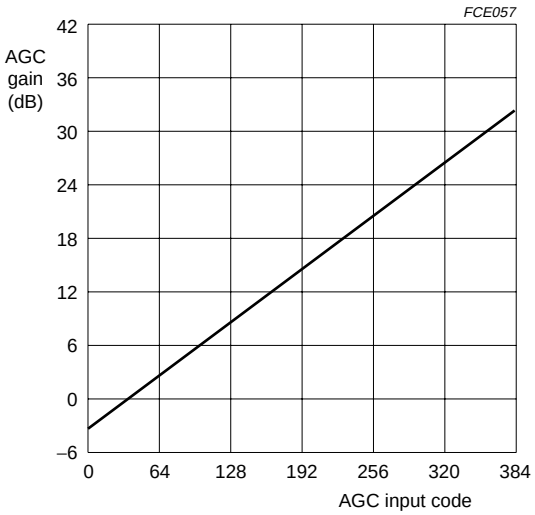
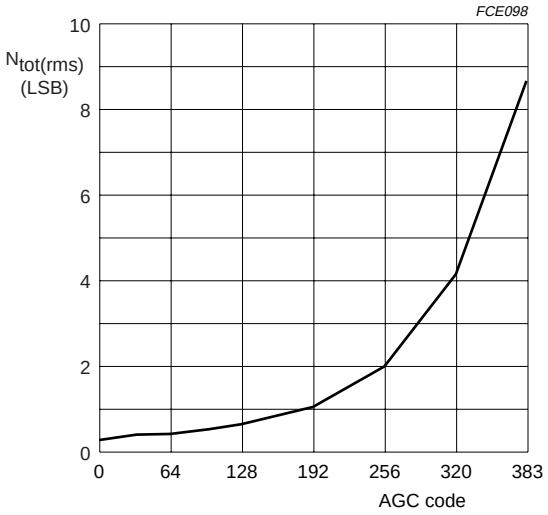


Fig.7 AGC gain as a function of AGC input code.



Noise measurement at ADC outputs:
Coupling capacitor at input is grounded, so only noise contribution of the front-end is evaluated. Front-end works at 18 Mpixels with line of 1024 pixels whose first 40 are used to run CLPOB and the last 40 for CLPDM. Data at the ADC outputs are measured during the other pixels. As a result of this, the standard deviation of the codes statistic is computed, resulting in the noise. No quantization noise is taken into account as no signal is inputted.

Fig.8 Total noise performance as a function of AGC gain.

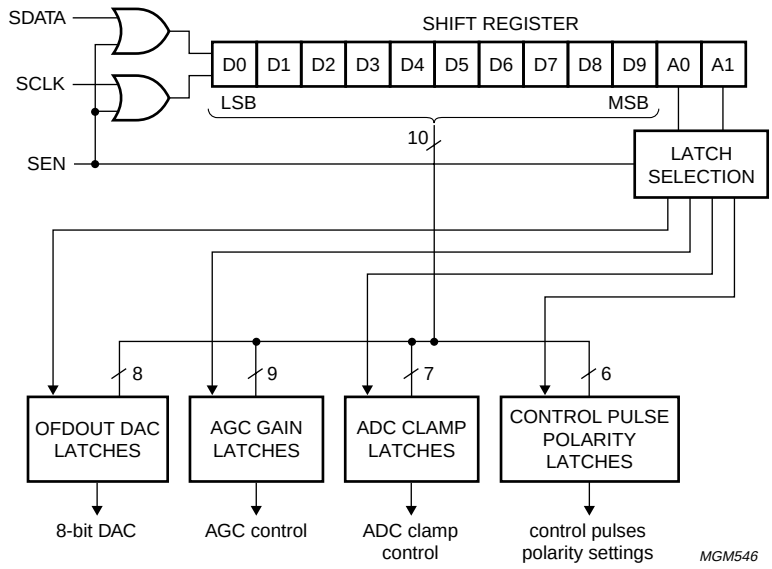
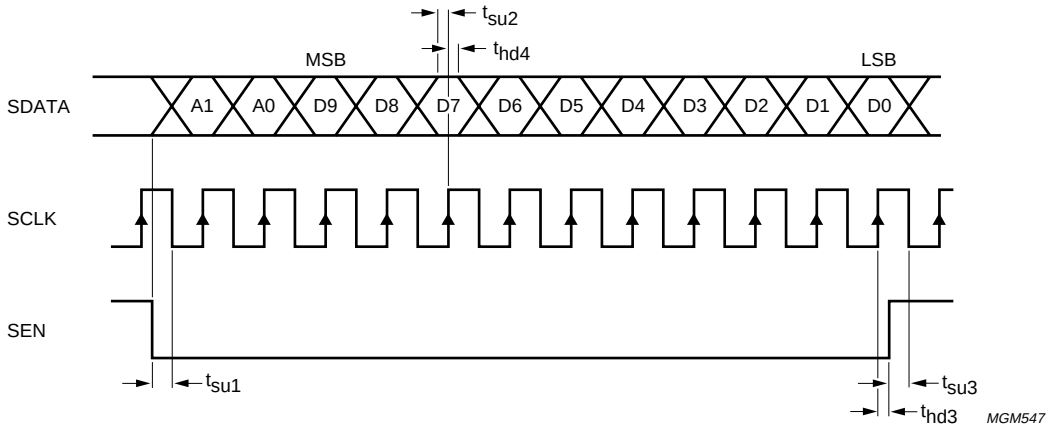


Fig.9 Serial interface block diagram.



$t_{su1} = t_{su2} = t_{su3} = 10$ ns (min.); $t_{hd3} = t_{hd4} = 10$ ns (min.).

Fig.10 Loading sequence of control input data via the serial interface.

Table 1 Serial interface programming

ADDRESS BITS		DATA BITS D9 TO D0
A1	**A0**	
0	0	AGC gain control (D8 to D0); bit D9 should be set to logic 0
0	1	DAC OFDOUT output control (D7 to D0); bits D8 and D9 should be set to logic 0
1	0	ADC clamp reference control (D6 to D0); bits D7, D8 and D9 should be set to logic 0
1	1	control pulses (pins SHP, SHD, CLPDM, CLPOB, PBK and CLK) polarity settings

Table 2 Polarity settings

SYMBOL	PIN	SERIAL CONTROL BIT[1]	ACTIVE EDGE OR LEVEL
SHP and SHD	47 and 48	D0	1 = HIGH; 0 = LOW
CLK	40	D1	1 = rising; 0 = falling
CLPDM	12	D2	1 = HIGH; 0 = LOW
CLPOB	13	D3	1 = HIGH; 0 = LOW
PBK	11	D5	1 = HIGH; 0 = LOW
VSYNC	24	D6	0 = rising; 1 = falling

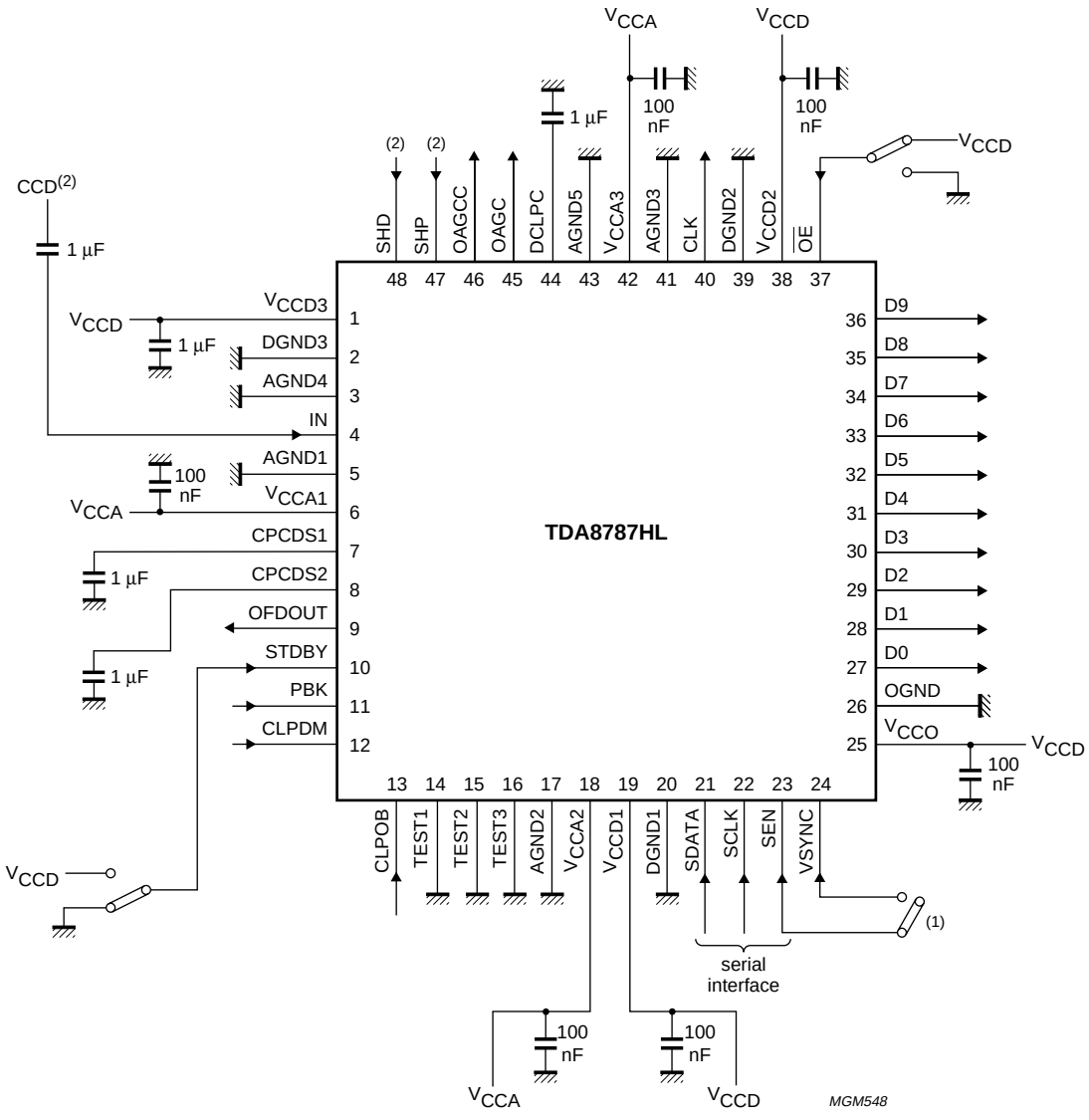
Note

1. Bit D4 is not used.

Table 3 Standby selection

STDBY	ADC DIGITAL OUTPUTS D9 TO D0	$I_{CCA} + I_{CCO} + I_{CCD}$ (TYP.)
1	logic state LOW	1 mA
0	active	64 mA

APPLICATION DIAGRAM



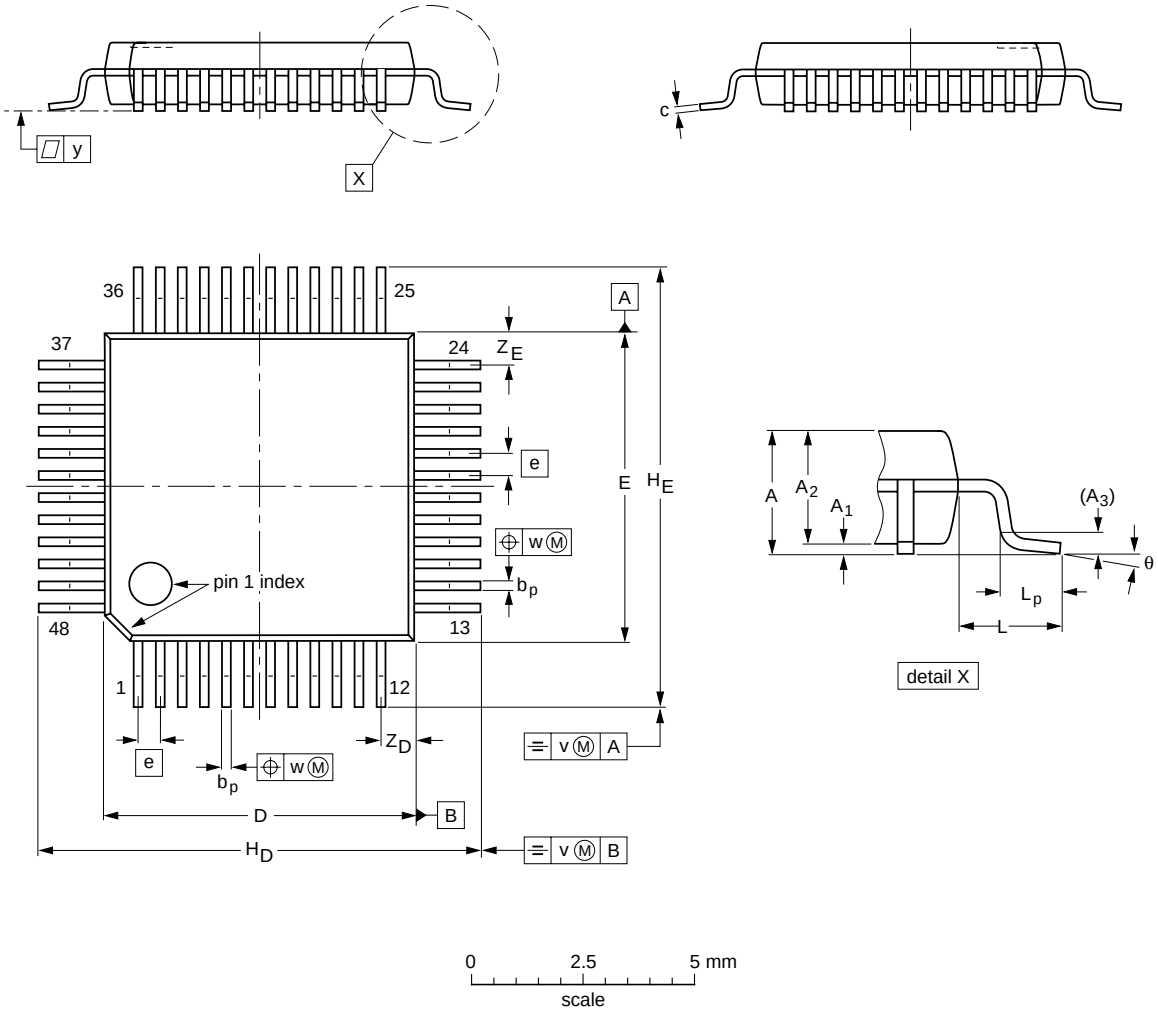
(1) Pins SEN and VSYNC should be interconnected when vertical sync signal is not available.

(2) Input signals IN, SHD and SHP must be adjusted to comply with timing signals $t_{h(IN-SHP)}$ and $t_{h(IN-SHD)}$ (see Chapter “Characteristics”).

Fig.11 Application diagram.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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