14-Bit CCD/CIS Signal Processor

AD9814

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD9814

2.0 Part Number. The complete part number(s) of this specification follow:

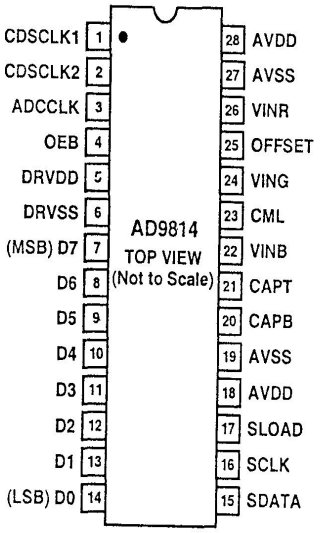
Generic Part Number	Description
AD9814	Complete 14-Bit CCD/CIS Signal Processor

Specific Part Number	Description
AD9814-703F	Standard product

2.1 **Case Outline**.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
F	CDFP3-F28	28 lead bottom-brazed flatpack

Figure 1 - Terminal Connections



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3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect To	Min	Max	Units
VIN, CAPT, CAPB	AVSS	–0.3	AVDD + 0.3	V
Digital Inputs	AVSS	–0.3	AVDD + 0.3	V
AVDD	AVSS	–0.5	+6.5	V
DRVDD	DRVSS	–0.5	+6.5	V
AVSS	DRVSS	–0.3	+0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or othr conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

NOTE:

1/ The input limits are defined as maximum tolerable voltage levels into the AD9814. These levels are not intended to be in the linear input range of the device. Signals beyond the input limits will turn on the overvoltage protection diodes.

3.1 Thermal Characteristics:

Thermal Resistance, Bottom brazed (F) Package

Junction-to-Case (Θ_{JC}) = 22°C/W Max

Junction-to-Ambient (Θ_{JA}) = 60°C/W Max

4.0 Table I. Electrical Table:

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub Group	Limit Min.	Limit Max	Units
RESOLUTION		No Missing Codes	1,2,3	14		Bits
Supply Currents	IAVDD		1,2,3		80	mA
	IDRVDD		1,2,3		10	mA
Power dissipation	PD		1,2,3		450	mW
Power supply rejection	PSR	AVDD= +5.0V ± 0.25V	1,2		0.3	%FSR
			3		0.5	%FSR
ACCURACY (Entire Signal Path) Integral Nonlinearity	INL		1,2	-11	11	LSB
			3	-18	11	LSB

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub Group	Limit Min.	Limit Max	Units
ACCURACY (Entire Signal Path) Differential Nonlinearity	DNL		1	-1	1.25	LSB
			2	-1	1	LSB
			3	-1	1.5	LSB
ACCURACY (Entire Signal Path) Offset Error	VOS		1,2,3	-104	104	mV
ACCURACY (Entire Signal Path) Gain Error	GAIN		1,2,3	-5.3	5.3	%FSR
PGA Gain Ratio	PGA GAIN		1,2,3	5.7	5.9	
DIFFERENTIAL VREF CAPT-CAPB (4V Input Range)	VREF4		1,2,3	1.9	2.1	V
DIFFERENTIAL VREF CAPT-CAPB (2V Input Range)	VREF2		1,2,3	0.94	1.06	V

TABLE I NOTES:

1/ Ta = +25C, Ta max = +125C, Ta min = -55C. AVDD=+5V, DRVDD=+5V, 3-Channel CDS, f_{ADCCLK}=6MHz, $f_{CDSCLK1} = f_{CDSCLK2}$ = 2MHz, PGA Gain = 1, Input Range = 4V, unless otherwise noted.

2/ INL is measured using the “fixed endpoint” method, NOT using a “best-fit” calculation.

3/ The Gain Error specification is dominated by the tolerance of the internal differential voltage reference.

4/ The PGA Gain is approximately “linear in dB” and follows the equation:

$$\text{PGA Gain} = (5.8 / (1 + 4.8 (63 - G) / 63))$$

where G is the register value.

4.1 Table II. Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3 1/ 2/
Group A Test Requirements	1, 2, 3
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	N/A

Notes:
1/ PDA applies to subgroup 1. Delta's excluded from PDA.
2/ See table III for delta limits.

4.2 Table III. Burn-in test 25C delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
IAVDD	80	80	+/-2	mA
VOS	+/-104 (+/-426)	+/-104 (+/-426)	+/-13.2 (+/-54)	mV (LSB)
GAIN	+/-5.3 (+/-868)	+/-5.3 (+/-868)	+/-0.56 (+/-91)	% (LSB)
+INL	+11	+11	+/-6	LSB
-INL	-11	-11	+/-5	LSB
+DNL	+1.25	+1.25	+/-0.5	LSB
-DNL	-1	-1	+/-0.35	LSB

5.0 Life Test/Burn-In:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition D.
5.3 Steady state life test is per MIL-STD-883 Method 1005, test condition D.

6.0 MIL-STD-38535 QMLV exceptions:

6.1 Full WLA per MIL-STD-883 TM 5007 is not available for this product. SEM Inspection only is available per MIL-STD-883, TM2018.
6.2 100% electrical test screening to be performed in MIL-PRF-38535, Class Q certified facility.

Rev	Description of Change	Date
A	Initiate	Sept 9, 2007
B	Update header/footer and add to 1.0 Scope description.	March 7, 2008