DATA SHEET

SAA7191B
Digital Multistandard Colour Decoder, Square Pixel (DMSD-SQP)

Product specification
File under Integrated Circuits, IC22

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Philips Semiconductors

PHILIPS

Digital Multistandard Colour Decoder, Square Pixel (DMSD-SQP)

SAA7191B

CONTENTS

Digital Multistandard Colour Decoder, Square Pixel (DMSD-SQP)

SAA7191B

1 FEATURES

- Separate 8-bit luminance (Y or CVBS) and 8-bit chrominance inputs (CVBS or C) from CVBS, Y/C, S-Video (S-VHS or Hi8) sources
- Luminance and chrominance signal processing for standards PAL-B/G, NTSC-M, SECAM
- Horizontal and vertical sync detection for all standards
- Real-time control output RTCO to be used for frequency-locked digital video encoder (SAA7199B). RTCO contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence.
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross colour cancellation (SECAM)
- 8-bit quantization of input signals
- 768/640 active samples per line equals 50/60 Hz (SQP)
- The YUV bus supports data rates of $780 \times f_H$ equal to 12.2727 MHz for 60 Hz (NTSC-M) and $944 \times f_H$ equal to 14.75 MHz for 50 Hz (PAL-B/G, SECAM) in 4 : 1 : 1 or 4 : 2 : 2 formats (via the I^2C-bus)
- One crystal oscillator of 26.8 MHz

2 GENERAL DESCRIPTION

The SAA7191B is a digital multistandard colour decoder suitable for 8-bit CVBS input signals or for 8-bit luminance and 8-bit chrominance input signals (Y/C).

The SAA7191B is down-compatible with SAA7191. The SAA7191B has additional outputs RTCO, GPSW0 and ODD. These new outputs are in high-impedance state when NFEN-bit = 0.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)		100	250	mA
V_{IL}	input levels	TTL-compatible			
V_{OL}	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7191B	68	PLCC	plastic	SOT188-2

5 BLOCK DIAGRAM

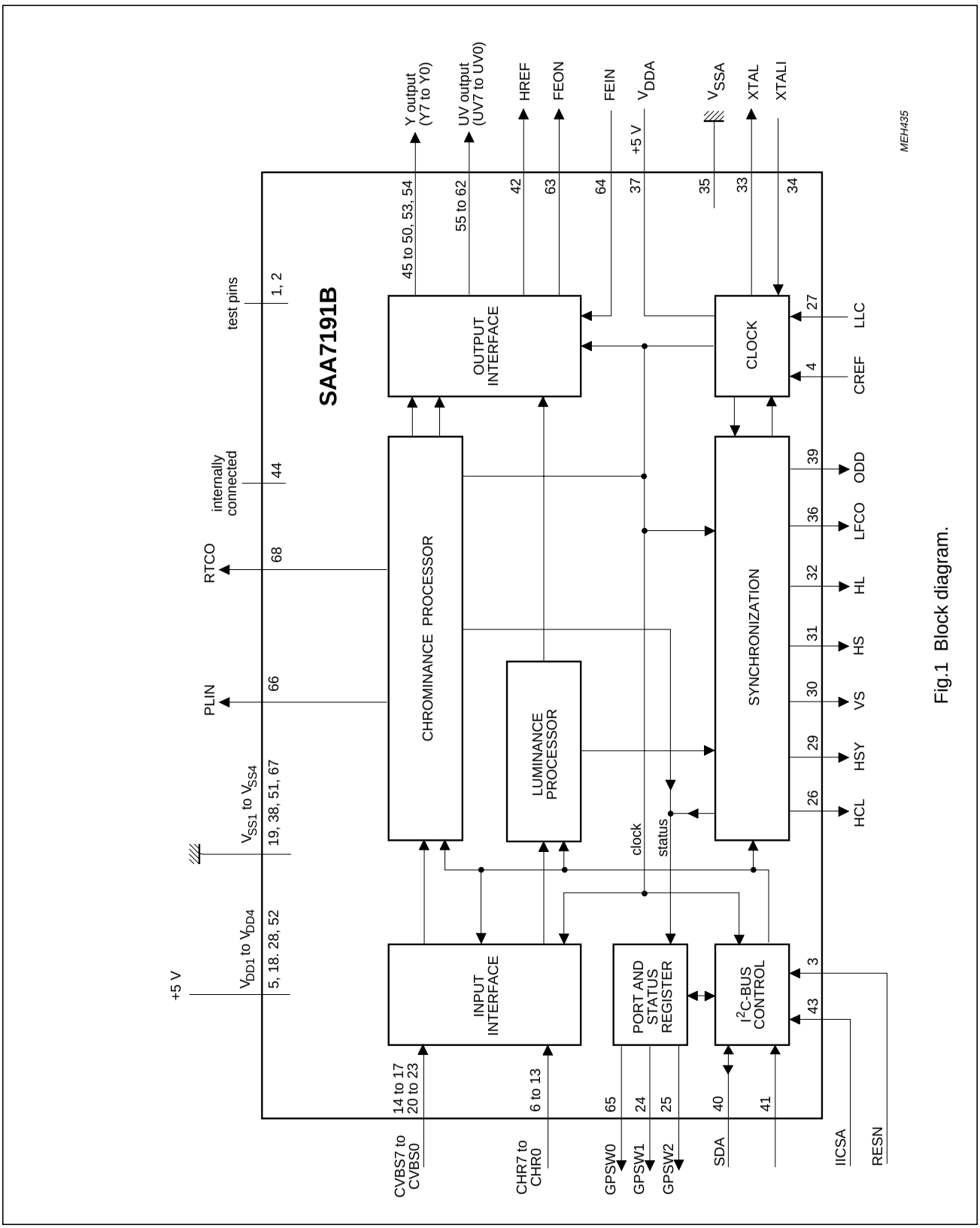


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the YUV-bus
V_{DD1}	5	+5 V supply input 1
CHR0	6	chrominance input data bits CHR7 to CHR0 from a Y/C (VHS, Hi8) source in two's complement format
CHR1	7	
CHR2	8	
CHR3	9	
CHR4	10	
CHR5	11	
CHR6	12	
CHR7	13	
CVBS0	14	luminance respectively CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	luminance respectively CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	Port 1 output for general purpose (programmable)
GPSW2	25	Port 2 output for general purpose (programmable)
HCL	26	black level clamp pulse (programmable), e.g. for TDA8708 (ADC)
LLC	27	line-locked clock input signal (29.5 MHz for 50 Hz system; 24.5454 MHz for 60 Hz system)
V_{DD3}	28	+5 V supply input 3
HSY	29	horizontal sync indicator output signal (programmable), e.g. for TDA8708 (ADC)
VS	30	vertical sync output signal
HS	31	horizontal sync output signal (programmable)
HL	32	horizontal lock flag, HIGH = PLL locked
XTAL	33	26.8 MHz clock output
XTALI	34	26.8 MHz connection for crystal or external oscillator (TTL compatible squarewave)
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (7.375 MHz/6.136363 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH); active only at NFEN-bit = 1
SDA	40	I^2C-bus data line

SYMBOL	PIN	DESCRIPTION
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference output for valid YUV data (for active line 768Y or 640Y samples long)
IICSA	43	set module address input (LOW = 1000 101X; HIGH = 1000 111X)
i.c.	44	internally connected
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0 (colour-difference), part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
FEON	63	output active flag (active LOW when Y and UV data in high-impedance state)
FEIN	64	fast enable input (active LOW to control fast switching due to YUV data)
GPSW0	65	Port 0 output for general purpose (programmable); active only at NFEN-bit = 1
PLIN	66	PAL flag (active LOW at inverted line); SECAM flag (LOW equals DR, HIGH equals DB line)
V_{SS4}	67	ground 4 (0 V)
RTCO	68	real-time control output active at NFEN-bit = 1; Fig.8

6.1 Pin configuration

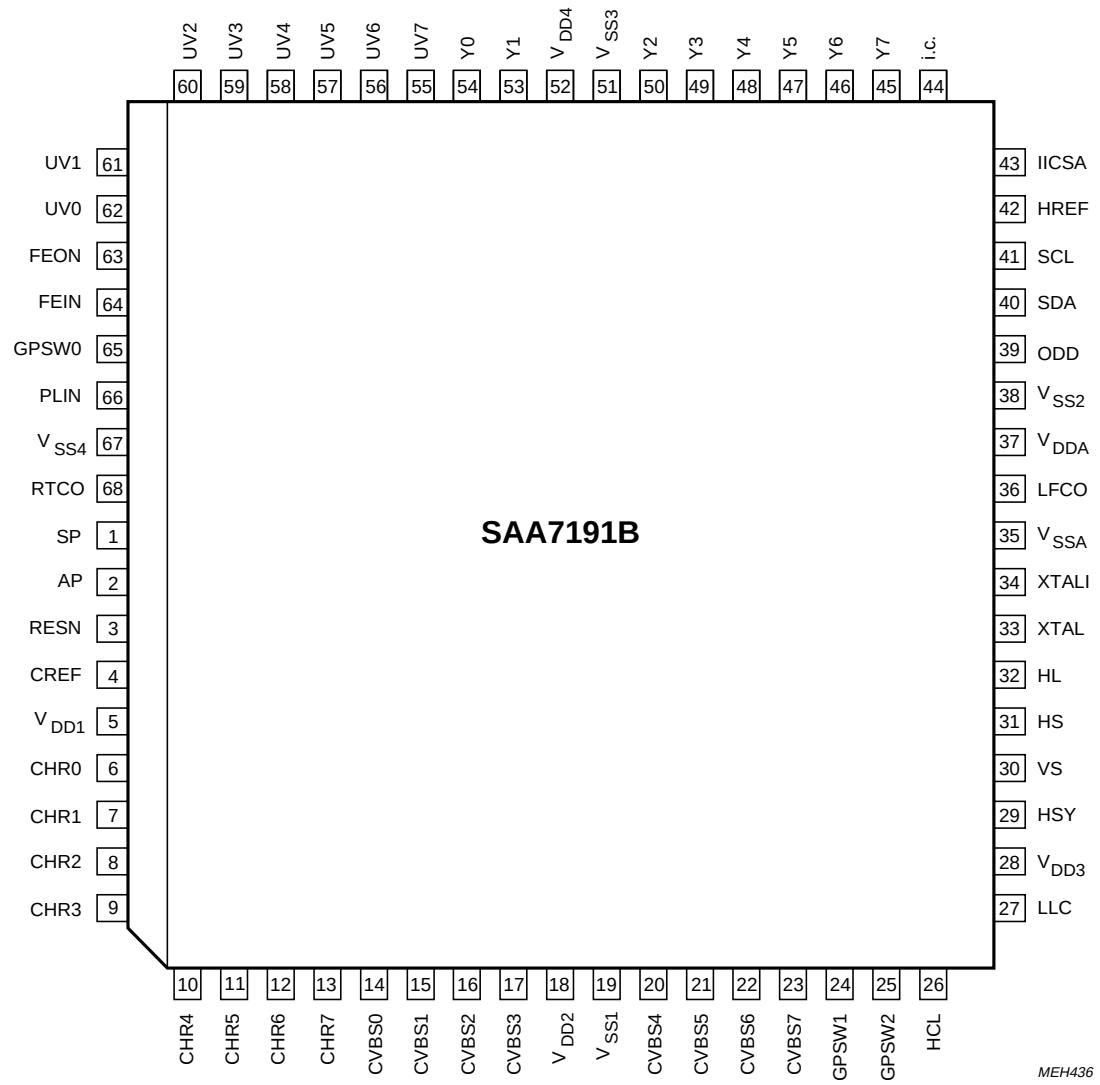


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Chrominance processor

The 8-bit chrominance input signal (CVBS or chrominance format) passes a bandpass filter to eliminate DC components and to decimate the sample rate before it is fed to the two multipliers (quadrature demodulator), Fig.3. Two subcarrier signals from a local oscillator (0 to 90 degree) are fed to the multiplicator inputs of the multipliers. The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.

The two multiplier output signals are converted to a serial data stream and applied to three low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance. The signals, originated from PAL and NTSC, are applied to a comb-filter. The signals, originated from SECAM, are fed through a Cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are fed finally to the output formatter stages and to the output interface.

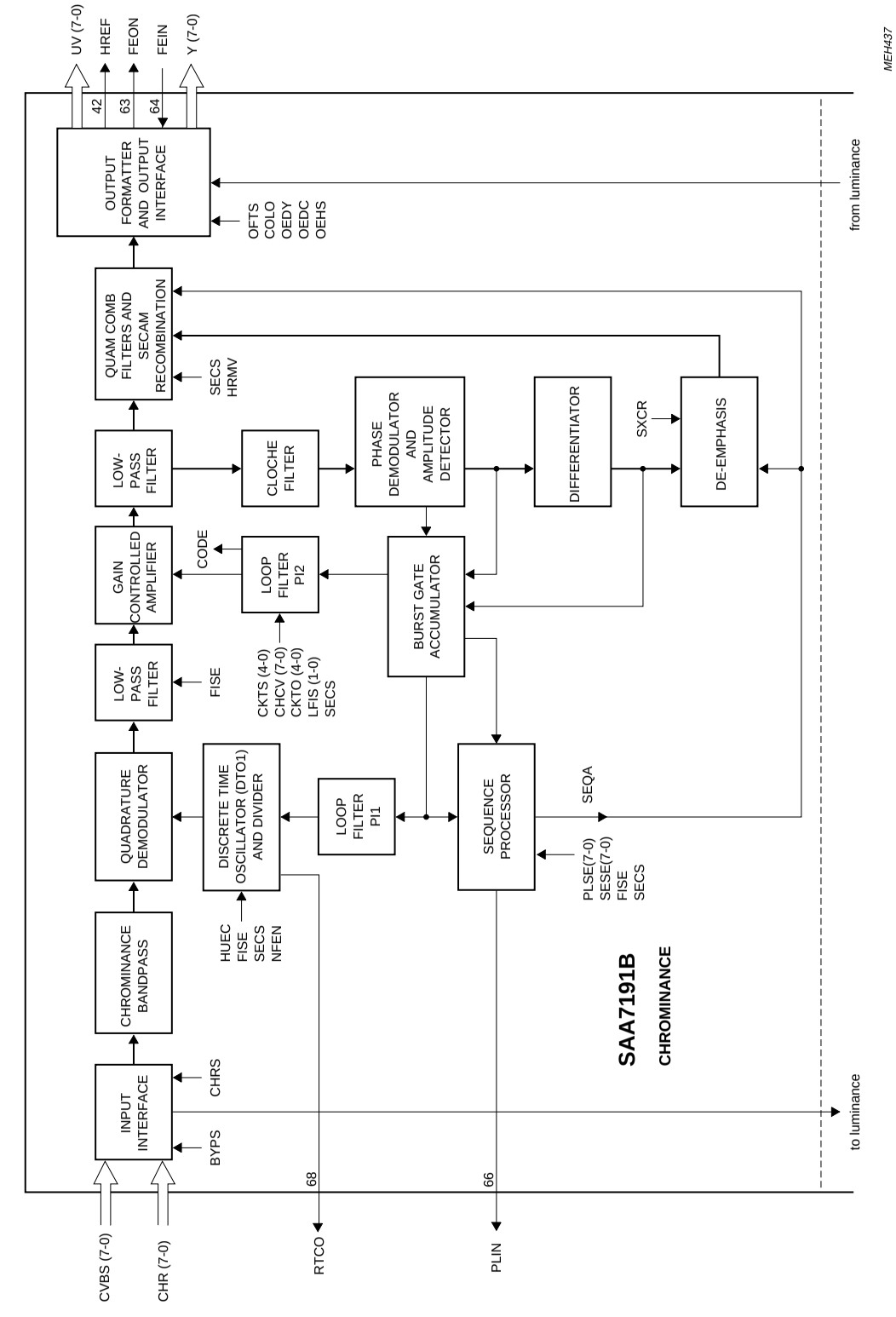


Fig.3 Detailed block diagram; continued in Fig.4.

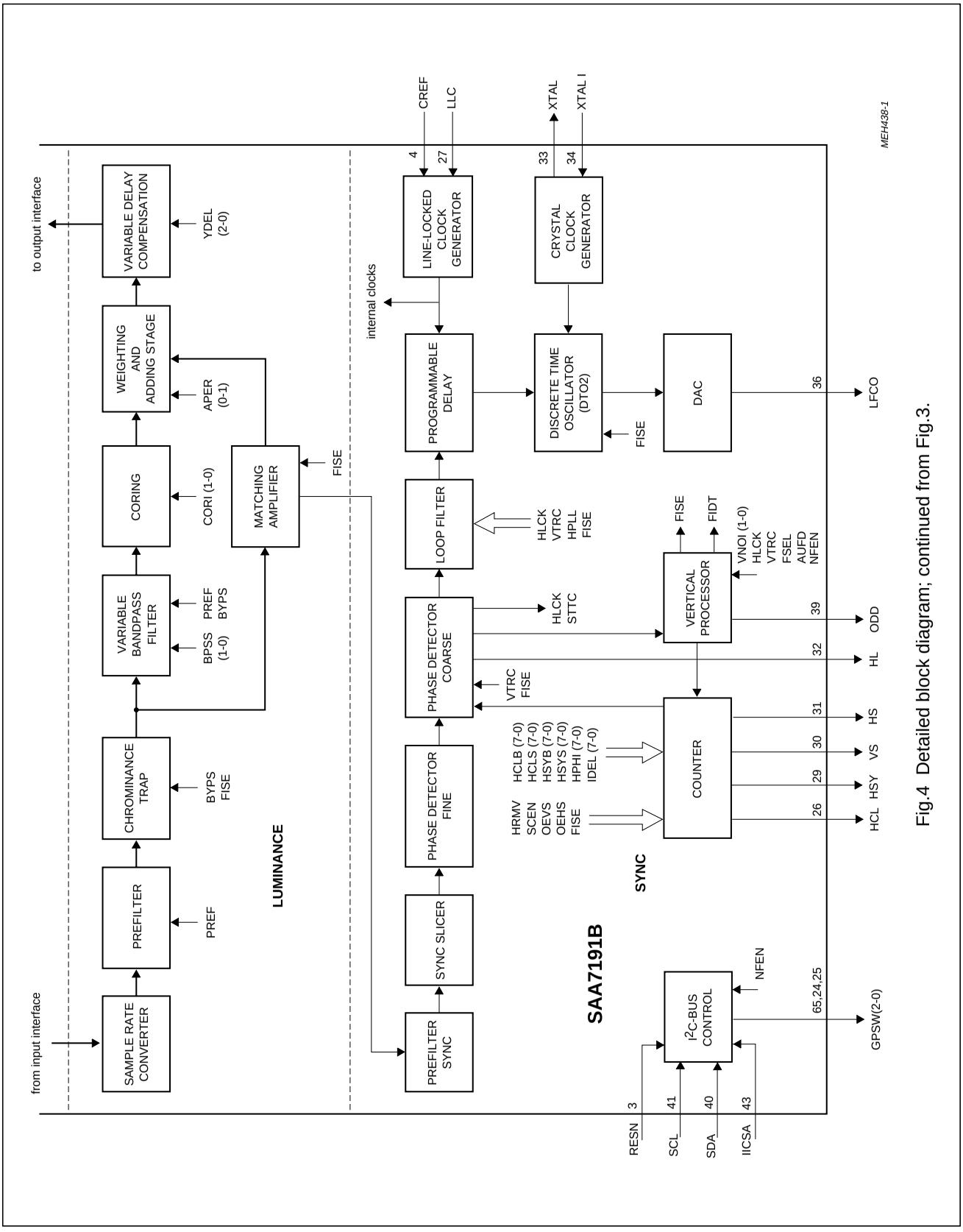


Fig.4 Detailed block diagram; continued from Fig.3.

7.2 Luminance processor

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-VHS, Hi8), is fed through a sample rate converter to reduce the data rate to 14.75 MHz for PAL and SECAM (12.2727 MHz for NTSC), Fig.4.

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_o = 4.43 MHz or f_o = 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be by-passed for S-Video (S-VHS and Hi8) signals.
The high frequency components of the luminance signal can be “peaked” (control for sharpness improvement via the I^{2}C-bus) in two bandpass filters with selectable transfer characteristic.
A coring circuit with selectable characteristic improves the signal once more, this signal is then added to the original (“unpeaked”) signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes. The improved luminance signal is fed to the variable delay compensation.

7.3 Processing delay

The delay from input to output is 220 LLC cycles if YDEL is set to 0. The processing delay will be influenced in future enhancements.

7.4 Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency.
The resulting output signal is applied to the loop filter to accumulate all phase deviations. Adjustable output signals (e. g. HCL and HSY) are generated according to peripheral requirements (TDA8708A, TDA8709A). The output signals HS, VS and PLIN are locked to the timing reference signal HREF (Figures 7 and 8). There is no absolute timing reference guaranteed between the input signal and the HREF signal as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications, which ask for absolute timing accuracy to the input signals.
The loop filter signal drives an oscillator to generate the line frequency control output signal LFCO.

Table 1 Clock frequencies in MHz for 50/60 Hz systems

CLOCK	50 Hz	60 Hz
LLC	29.5	24.545454
LLC2	14.75	12.272727
LLC4	7.375	6.136136
LLC8	3.6875	3.068181

7.5 Line locked clock frequency

LFCO is required in an external PLL (SAA7197) to generate the line locked clock frequency.

7.6 YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I^{2}C-bus in normal selections, or they are controlled by output enable chain (FEIN on pin 64, Fig.5). The YUV-bus data rate equals LLC2 in Table 1. Timing is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference).

YUV-bus formats 4:2:2 and 4:1:1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the multiplexed colour-difference signals (B–Y) and (R–Y). The frame in the following tables is the time, required to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparison to one U and one V sample within one frame.

Table 2 4 : 2 : 2 format
(768 pixels per line for 50 Hz system; 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Notes

1. Data rate: LLC2
2. Sample frequency:
   Y LLC2
   U LLC4
   V LLC4

The quoted frequencies are valid on the YUV-bus.
The time frames are controlled by the HREF signal.

Table 3 4 : 1 : 1 format (768 pixels per line for 50 Hz system and 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Notes

1. Data rate: LLC2
   sample frequency:
   Y LLC2
   U LLC8
   V LLC8

Fast enable is achieved by setting input FEIN to LOW. This signal is used to control fast switching on the digital YUV-bus. HIGH on this pin forces the Y and U/V outputs to a high-impedance state. The signal FEON is LOW when the Y and U/V outputs are in this high-impedance state (Fig.5).
The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Table 4 Digital output control

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)	FEON
X	X	0	active	active	1
0	0	1	Z	Z	0
0	1	1	Z	active	1
1	0	1	active	Z	1
1	1	X	active	active	1

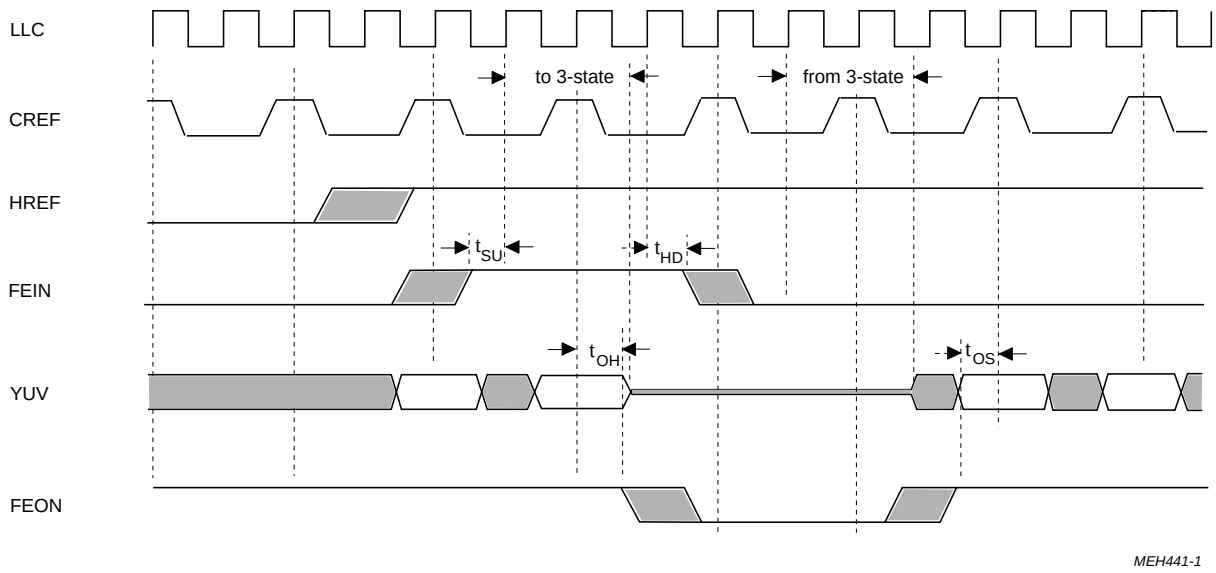


Fig.5 Timing example of fast enable input FEIN.

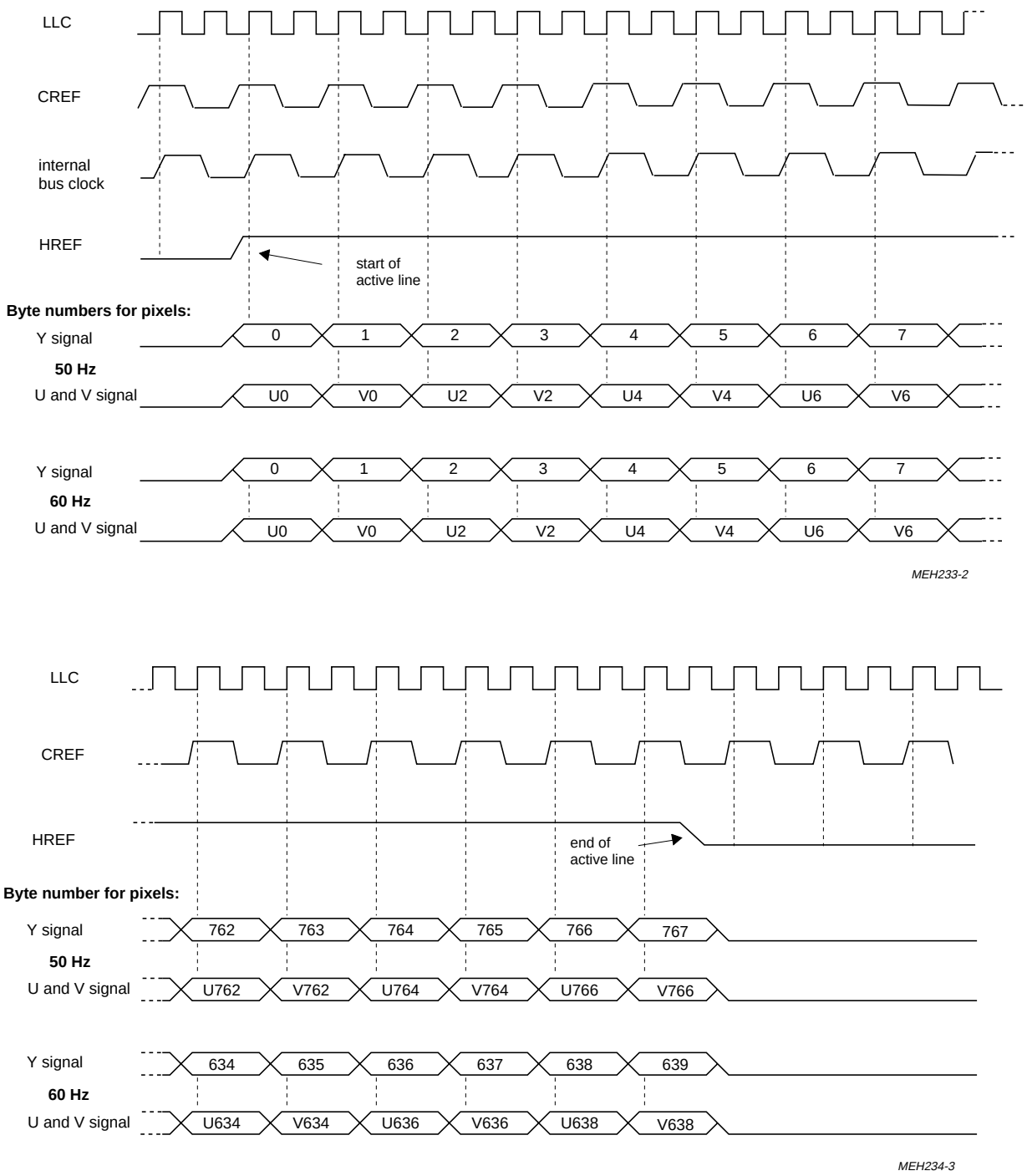
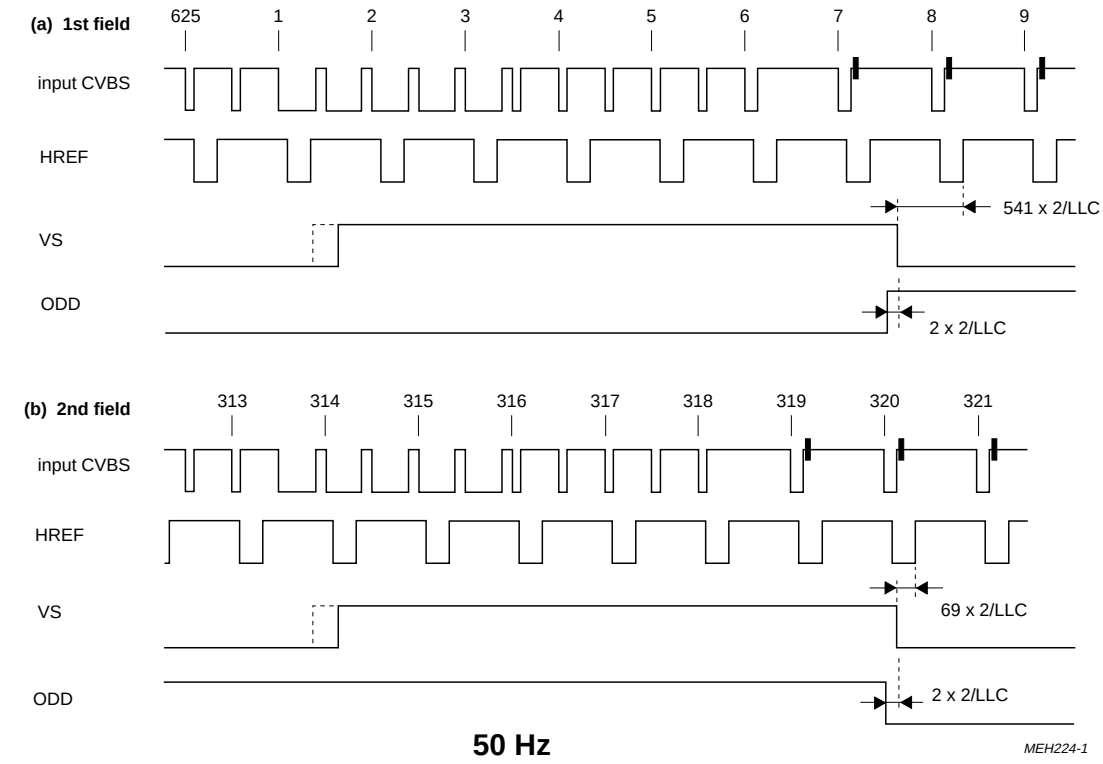


Fig.6 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.



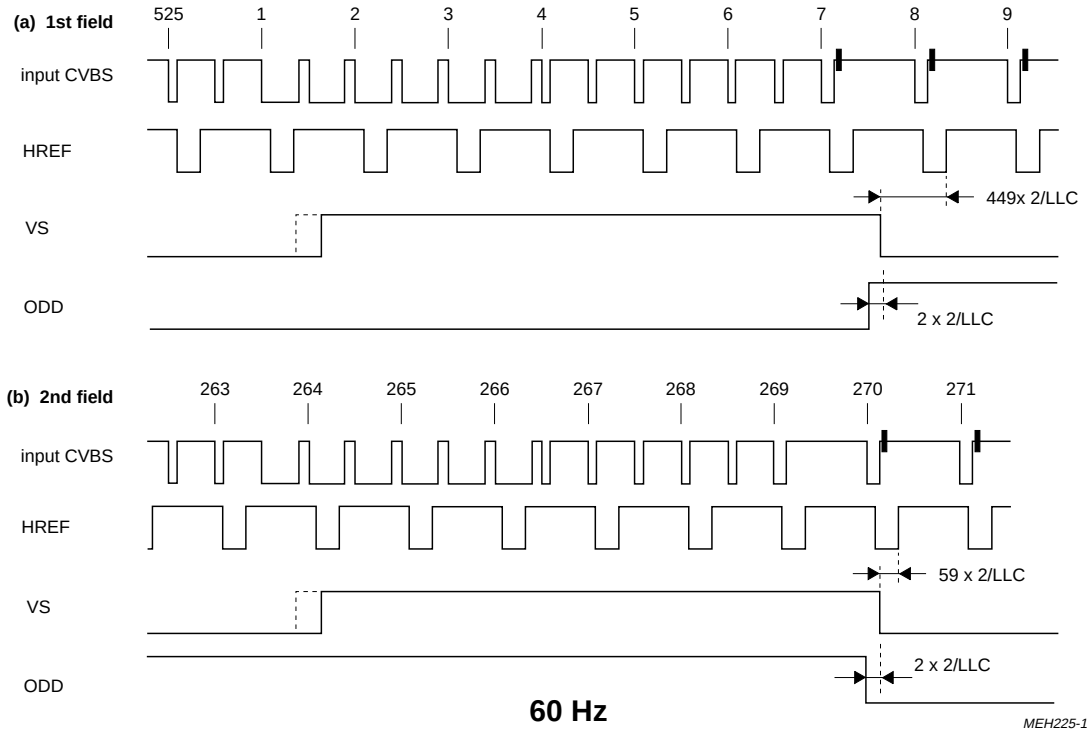
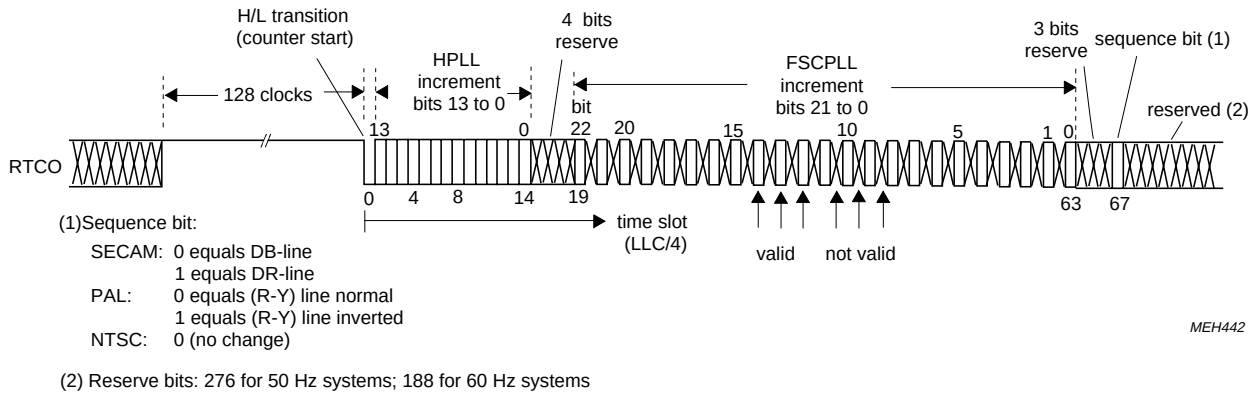


Fig.7 Vertical timing diagram for 50 / 60 Hz.



(1)Sequence bit:

SECAM: 0 equals DB-line
1 equals DR-line
PAL: 0 equals (R-Y) line normal
1 equals (R-Y) line inverted
NTSC: 0 (no change)

(2) Reserve bits: 276 for 50 Hz systems; 188 for 60 Hz systems

Fig.8 RTCO timing.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134);
ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	–0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS\ (1\ to\ 4)}$	–	±100	mV
V_I	voltage on all inputs	–0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	–0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	–	2.5	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling[1] for all pins	–	±2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

9 CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	–	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
V_{IL}	input voltage LOW		–0.5	–	1.5	V
V_{IH}	input voltage HIGH		3	–	V_{DD}+0.5	V
$I_{40,41}$	input current		–	–	±10	µA
I_{ACK}	output current on pin 40	acknowledge	3	–	-	mA
V_{OL}	output voltage at acknowledge	I_{40} = 3 mA	–	–	0.4	V
Data clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 43 and 64), Fig.11						
V_{IL} V_{IH}	LLC input voltage LOW (pin 27) LLC input voltage HIGH		–0.5 2.4	– –	0.6 V_{DD}+0.5	V V
V_{IL} V_{IH}	other input voltage LOW other input voltage HIGH		–0.5 2.0	– –	0.8 V_{DD}+0.5	V V
I_{LI}	input leakage current		–	–	10	µA
C_I	input capacitance	data inputs; note 1 I/O high-ohmic clock inputs	– – –	– – –	8 8 10	pF pF pF
$t_{SU.DAT}$	input data set-up time	Fig.9	11	–	–	ns
$t_{HD.DAT}$	input data hold time		3	–	–	ns
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	–	2.6	V
V_{36}	output voltage range		1	–	V_{DD}	V
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62)			Figures 10 and 15 to 25			
V_{OL}	output voltage LOW	notes 1 and 2	0	–	0.6	V
V_{OH}	output voltage HIGH		2.4	–	V_{DD}	V
C_L	load capacitance		15	–	50	pF
Control outputs (pins 24 to 26, 29, 31, 32, 39, 63, 65, 66 and 68); Fig.12						
V_{OL}	output voltage LOW	notes 1 and 2	0	–	0.6	V
V_{OH}	output voltage HIGH		2.4	–	V_{DD}	V
C_L	load capacitance		7.5	–	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing of YUV-bus and control outputs		Fig.8				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF	13	–	–	ns
		controls at C_L = 7.5 pF	13	–	–	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	14	–	–	ns
		controls at C_L = 25 pF	14	–	–	ns
t_{SZ}	data output disable transition time	to 3-state condition	16	–	–	ns
t_{ZS}	data output enable transition time	from 3-state condition	14	–	–	ns
t_{RTCO}	RTCO timing			Fig.8		
Chrominance PLL						
f_C	catching range		±400	–	–	Hz
Crystal oscillator		Fig.10				
f_n	nominal frequency	3rd harmonic	–	26.8	–	MHz
$\Delta f / f_n$	permissible deviation f_n		–	–	±50	10^{-6}
	temperature deviation from f_n		–	–	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	–	70	°C
	load capacitance C_L		8	–	–	pF
	series resonance resistance R_S		–	50	80	Ω
	motional capacitance C_1		–	1.1±20%	–	fF
	parallel capacitance C_0		–	3.5±20%	–	pF
	Philips catalogue number		9922 520 30004			
Line locked clock input LLC (pin 27)		Fig.9				
t_{LLC}	cycle time	note 3	31	–	45	ns
t_p	duty factor	t_{LLCH} / t_{LLC}	40	–	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns

Notes

1. Data output signals are Y7 to Y0 and UV7 to UV0. All others are control output signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

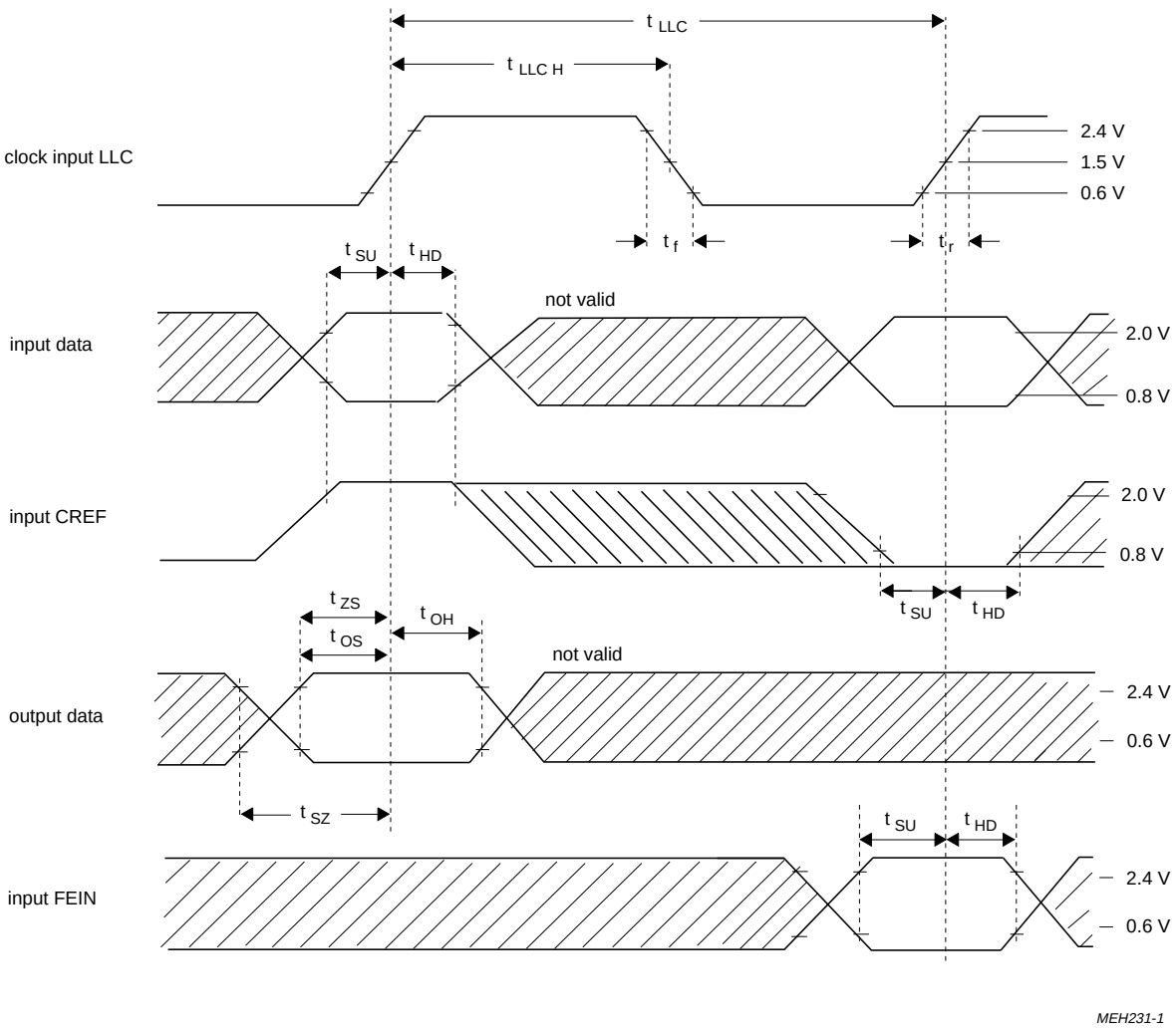


Fig.9 Data input and output timing diagram.

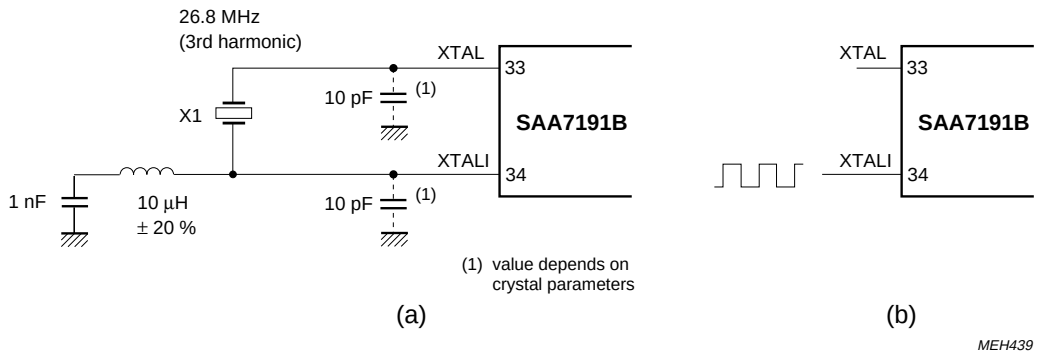
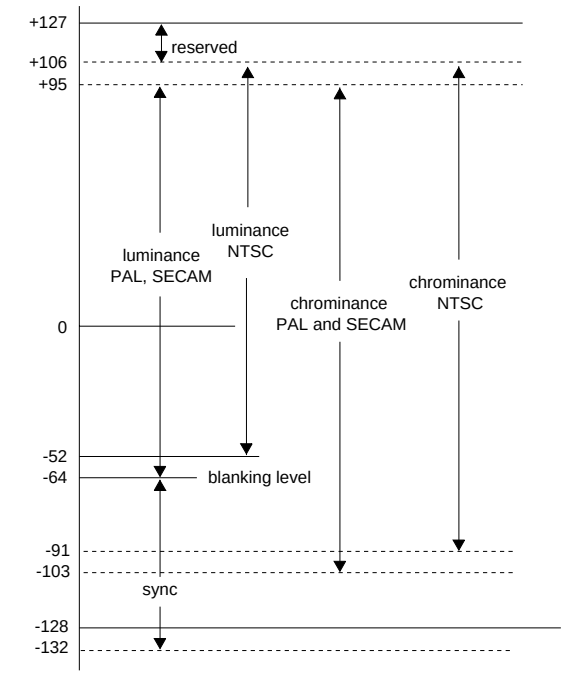
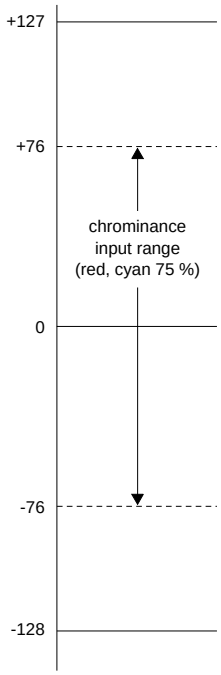


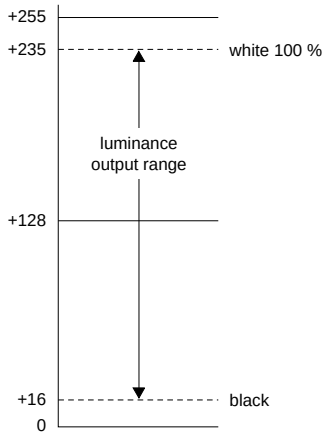
Fig.10 Oscillator application (a) and optional clock from external source (b).



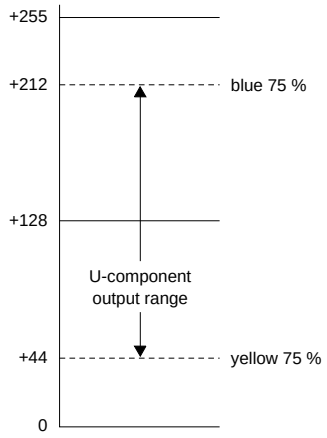
(a) CVBS7 to CVBS0 input signal range.



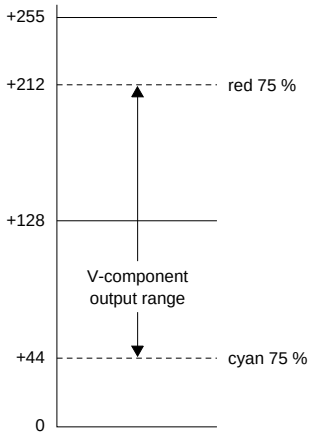
(b) CHR7 to CHR0 input signal range.



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

MEH254-1

1. All levels are related to EBU colour bar.
2. Values in decimal at 100% luminance and 75% chrominance amplitude.

Fig.11 Input and output signal ranges.

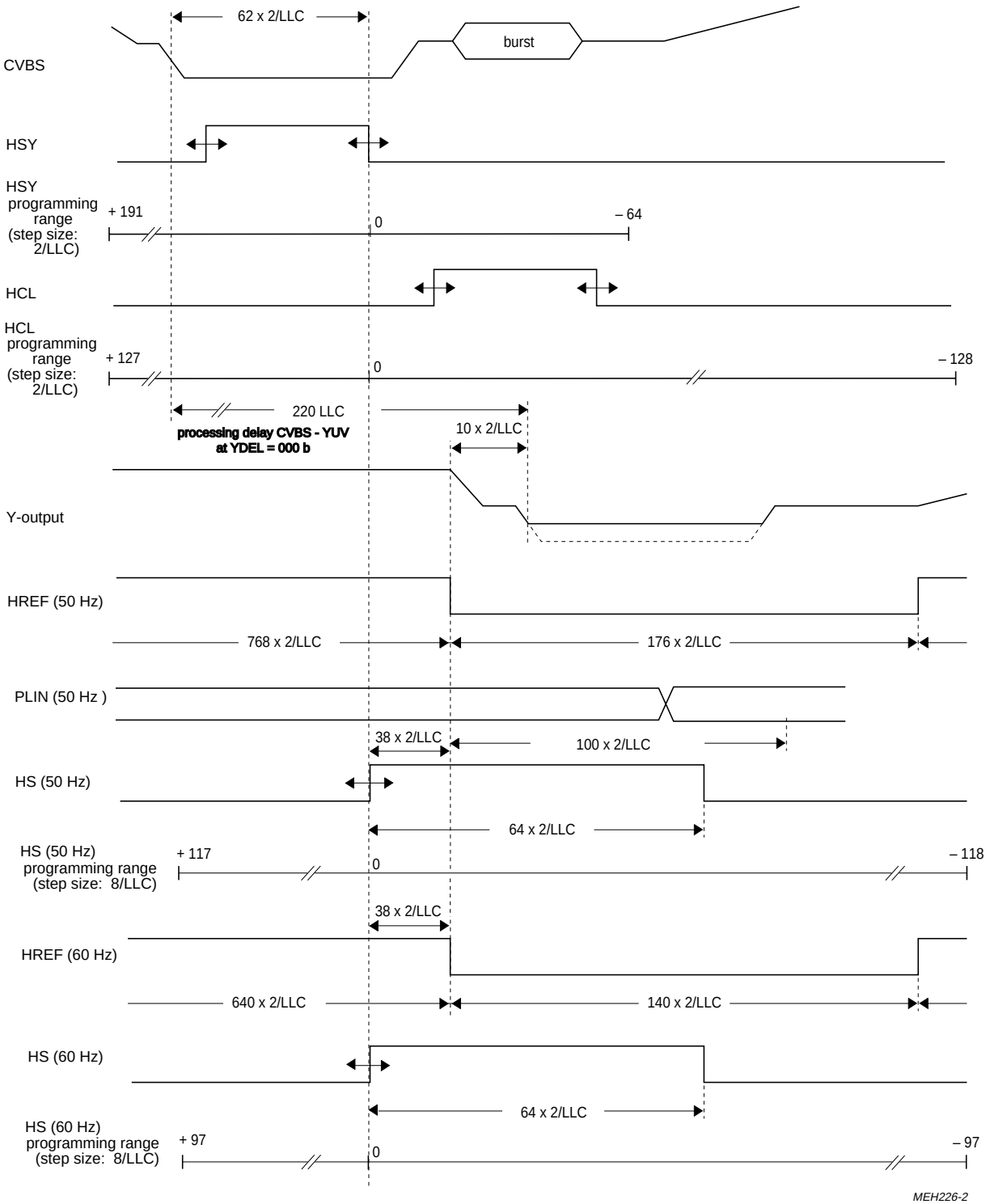


Fig.12 Horizontal sync at HRMV = 0 and HRFS = 0 for 50/60 Hz (signals HSY, HCL, HREF and PLIN).

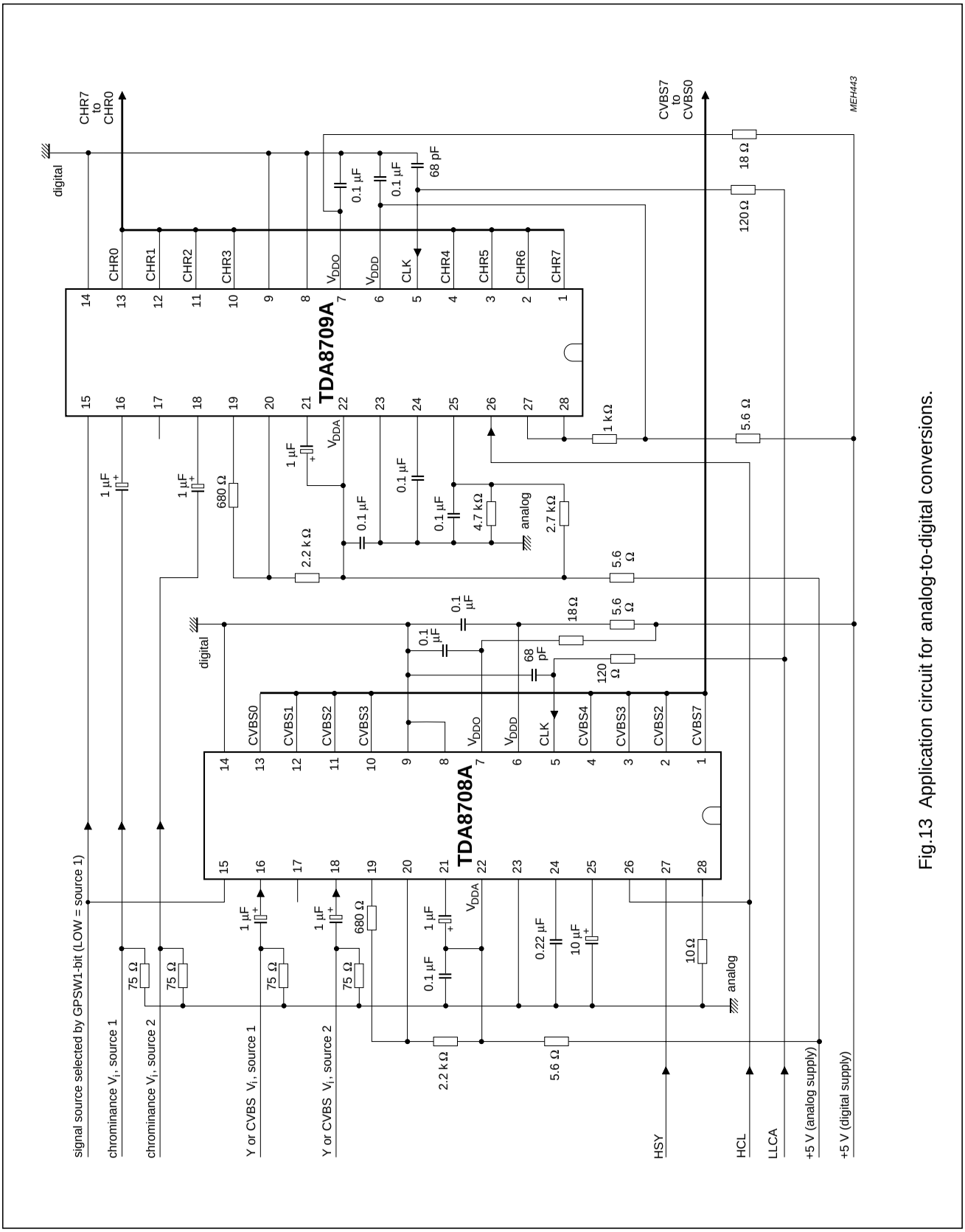


Fig.13 Application circuit for analog-to-digital conversions.

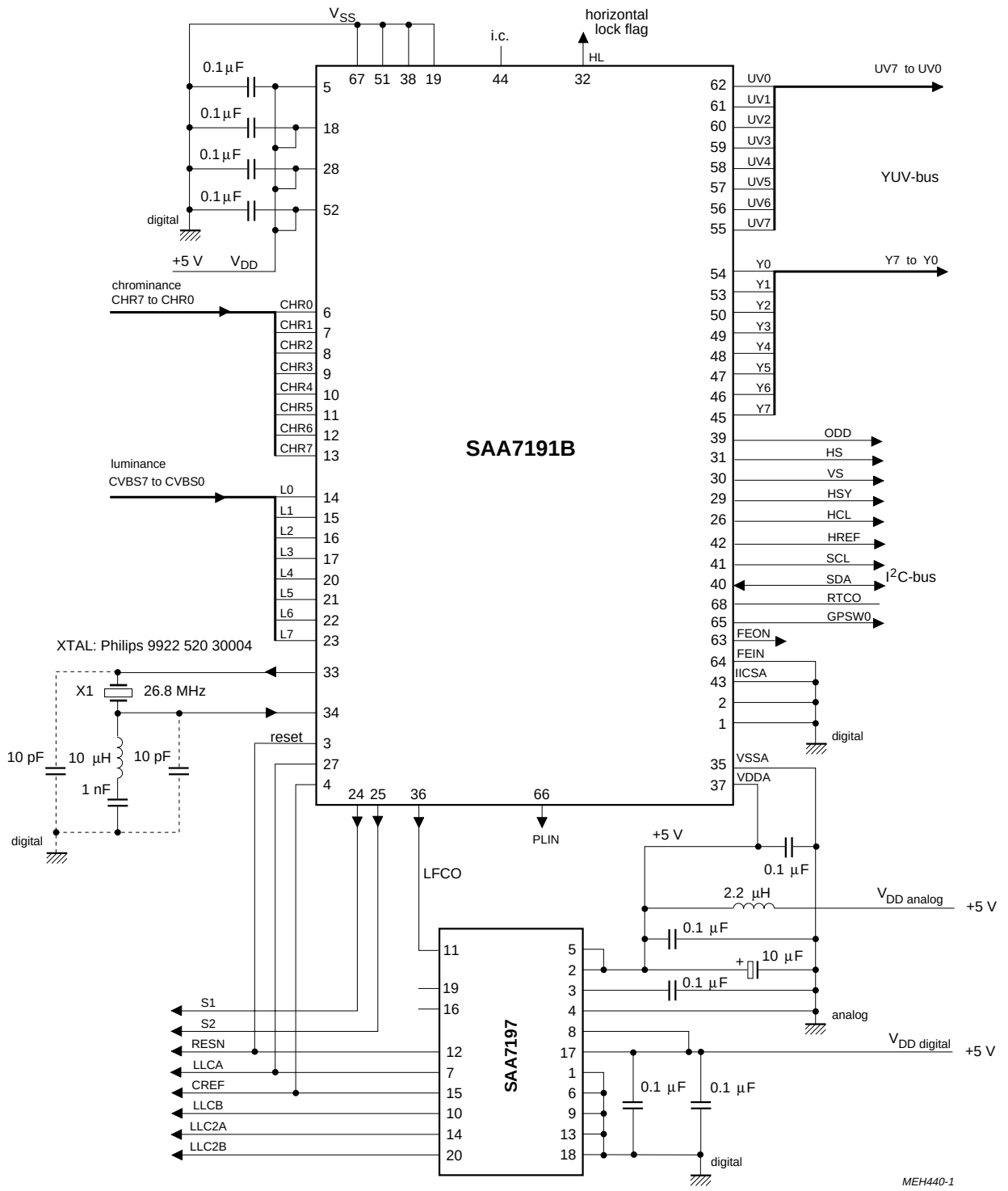


Fig.14 Application circuit for digital multistandard colour decoder.

10 I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S	=	start condition
SLAVE ADDRESS	=	1000 101X (IICSA = LOW) or 1000 111X (IICSA = HIGH)
A	=	acknowledge, generated by the slave
SUBADDRESS(1)	=	subaddress byte (Table 5)
DATA	=	data byte (Table 5)
P	=	stop condition
X	=	read/write control bit X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)

Note

1. If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 5 I²C-bus; DATA for status byte (X = 1 in address byte; 8Bh at IICSA = LOW or 8Fh at IICSA = HIGH).

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	X	X	X	X	CODE

Function of the bits:

STTC	Horizontal time constant information for future application with logical combfilter only:	0 = TV time constant (slow); 1 = VCR time constant (fast)
HLCK	Horizontal PLL information:	0 = HPLL locked; 1 = HPLL unlocked
FIDT	Field information:	0 = 50 Hz system detected; 1 = 60 Hz system detected
CODE	Colour information:	0 = no colour detected; 1 = colour detected

Table 6 I²C-bus; subaddress and data bytes for writing (X = 0 in address byte; 8Ah at IICSA = LOW or 8Eh at IICSA = HIGH).

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H sync begin, 50 Hz	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H sync stop, 50 Hz	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H clamp begin, 50 Hz	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H clamp stop, 50 Hz	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H sync after PHI1, 50 Hz	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
Luminance control	06	BYPS	PREF	BPSS1	BPSS0	CORI1	CORI0	APER1	APER0
Hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Colour killer threshold QAM	08	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	0	0	0
Colour-killer threshold SECAM	09	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0	0	0	0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
Chroma gain control settings	0C	COLO	LFIS1	LFIS0	0	0	0	0	0
Standard/mode control	0D	VTRC	0	0	0	NFEN	HRMV	GPSW0	SECS
I/O and clock control	0E	HPLL	OEDC	OEHS	OEVS	OEDY	CHRS	GPSW2	GPSW1
Control #1	0F	AUFD	FSEL	SXCR	SCEN	OFTS	YDEL2	YDEL1	YDEL0
Control #2	10	0	0	0	0	0	HRFS	VNOI1	VNOI0
Chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
Not used, is acknowledged	12	0	0	0	0	0	0	0	0
Not used, is acknowledged	13	0	0	0	0	0	0	0	0
H sync begin, 60 Hz	14	HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0
H sync stop, 60 Hz	15	HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0
H clamp begin, 60 Hz	16	HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0
H clamp stop, 60 Hz	17	HC6S7	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0
H sync after PHI1, 60 Hz	18	HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0

Notes

1. Default values of register contents to obtain a picture see Table 6.
2. All unused control bits **must be** programmed with “0” (zero) as indicated in Table 5.

Function of the bits of Table 5

<table>
<tr><td>IDEL7 to IDEL0
“00”</td><td>Increment delay time (dependent on application), step size = 4 / LLC. The delay time is selectable from –4 / LLC (–1 decimal multiplier) to –1024 / LLC (–256 decimal multiplier) equals data FF to 00 (hex). Different processing times in the chrominance channel and the clock generation could result in phase errors in the chrominance processing by transients in clock frequency. An adjustable delay (IDEL) is necessary if the processing time in the clock generation is unknown.</td></tr>
<tr><td>HSYB7 to HSYB0
“01”</td><td>Horizontal sync begin for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two’s complement numbers with “hidden” sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HSYS7 to HSYS0
“02”</td><td>Horizontal sync stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two’s complement numbers with “hidden” sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HCLB7 to HCLB0
“03”</td><td>Horizontal clamp start for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HCLS7 to HCLS0
“04”</td><td>Horizontal clamp stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HPHI7 to HPHI0
“05”</td><td>Horizontal sync after PHI1 for 50 Hz, step size = 8 / LLC. The delay time is selectable from –936 /LLC (+117 decimal multiplier) to +944/LLC (–118 decimal multiplier) equals data 75 to 8A (hex).</td></tr>
<tr><td>BYPS
“06”</td><td>input mode select bit: 0 = CVBS mode (chrominance trap active)
1 = S-Video mode (chrominance trap bypassed)</td></tr>
<tr><td>PREF</td><td>use of pre-filter: 0 = pre-filter off; 1 = pre-filter on;
PREF may be used if chrominance trap is active.</td></tr>
<tr><td>BPSS1 to BPSS0</td><td>Aperture bandpass to select different characteristics with maximums (0.2 to 0.3 × LLC / 2):
<table>
<tr><th>BPSS1</th><th>BPSS0</th><th>characteristics</th></tr>
<tr><td>0</td><td>0</td><td rowspan="4">Figures 16 to 25</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>CORI1 to CORI0
“06”</td><td>Coring range for high frequency components according to 8-bit luminance, Fig.15.
<table>
<tr><th>CORI1</th><th>CORI0</th><th>coring</th></tr>
<tr><td>0</td><td>0</td><td>coring off</td></tr>
<tr><td>0</td><td>1</td><td>±1 LSB</td></tr>
<tr><td>1</td><td>0</td><td>±2 LSB</td></tr>
<tr><td>1</td><td>1</td><td>±3 LSB</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>APER1 to APER0
“06”</td><td>Aperture bandpass filter weights high frequency components of luminance signal:
<table><tr><th>APER1</th><th>APER0</th><th>factor</th></tr><tr><td>0</td><td>0</td><td>0)</td></tr><tr><td>0</td><td>1</td><td>0.25)</td></tr><tr><td>1</td><td>0</td><td>0.5)</td></tr><tr><td>1</td><td>1</td><td>1)</td></tr></table>Figure 16 to 25</td></tr>
<tr><td>HUE7 to HUE0
“07”</td><td>Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.</td></tr>
<tr><td>CKTQ4 to CKTQ0
“08”</td><td>Colour-killer threshold QAM from approximately −30 dB to −18 dB, equals data bytes F8 to 07 (hex)</td></tr>
<tr><td>CKTS4 to CKTS0
“09”</td><td>Colour-killer threshold SECAM from approximately −30 dB to −18 dB, equals data bytes. F8 to 07 (hex)</td></tr>
<tr><td>PLSE7 to PLSE0
“0A”</td><td>PAL switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>SESE7 to SESE0
“0B”</td><td>SECAM switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>COLO
“0C”</td><td>Colour on bit: 0 = automatic colour-killer enabled; 1 = forced colour on.</td></tr>
<tr><td>LFIS1 to LFIS0
“0C”</td><td>Chrominance gain control (AGC filter):
<table><tr><th>LFIS1</th><th>LFIS0</th><th></th><th>loop filter time constant</th></tr><tr><td>0</td><td>0</td><td>=</td><td>slow</td></tr><tr><td>0</td><td>1</td><td>=</td><td>medium</td></tr><tr><td>1</td><td>0</td><td>=</td><td>fast</td></tr><tr><td>1</td><td>1</td><td>=</td><td>actual gain, stored for test purposes only</td></tr></table></td></tr>
<tr><td>VTRC
“0D”</td><td>VTR/TV mode bit : 0 = TV mode (slow time constant); 1 = VTR mode (fast time constant)</td></tr>
<tr><td>NFEN</td><td>SAA7191B-specified functions enable (RTCO, ODD and GPSW0 outputs)
0 = outputs set to high-impedance (circuit equals SAA7191); 1 = outputs active</td></tr>
<tr><td>HRMV</td><td>HREF generation: 0 = like SAA7191; 1 = HREF is 8 x LLC2 clocks earlier</td></tr>
<tr><td>GPSWO</td><td>General purpose switch 0: 0 = output pin 65 LOW; 1 = output pin 65 HIGH</td></tr>
<tr><td>SECS</td><td>SECAM mode bit : 0 = other standards; 1 = SECAM</td></tr>
</table>

<table>
<tr><td>HPLL
“0E”</td><td>Horizontal clock PLL: 0 = PLL closed;
1 = PLL circuit open and horizontal frequency fixed.</td></tr>
<tr><td>OEDC</td><td>Colour-difference output enable: 0 = data outputs UV7 to UV0 can be set to high-impedance via FEIN
1 = data outputs UV7 to UV0 active.</td></tr>
<tr><td>OEHS</td><td>H-sync output enable (pins 31 and 42): 0 = HS and HREF outputs high-impedance
1 = HS and HREF outputs active.</td></tr>
<tr><td>OEVS</td><td>V-sync output enable (pin 30): 0 = VS output high-impedance
1 = VS output active.</td></tr>
<tr><td>OEDY</td><td>Luminance output enable:
0 = data outputs Y7 to Y0 can be set to high-impedance via FEIN
1 = data outputs Y7 to Y0 active.</td></tr>
<tr><td>CHRS</td><td>S-VHS bit (chrominance from CVBS or from chrominance input):
0 = controlled by BYPS-bit (subaddress 06)
1 = chrominance from chrominance input (CHR7 to CHR0)</td></tr>
<tr><td>GPSW2 to GPSW1 to “0E”</td><td>General purpose switches:<table><tr><th>GPSW2</th><th>GPSW1</th><th>set port output pins 24 (GPSW2) and 25 (GPSW1)</th></tr><tr><td>0</td><td>0</td><td rowspan="4">use is dependent on application</td></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table></td></tr>
</table>

AUFD “0F”

Automatic field detection: 0 = field selection by FSEL-bit; 1 = automatic field detection.

FSEL

Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)

SXCR

SECAM cross-colour reduction: 0 = reduction off; 1 = reduction on.

SCEN

Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 26 and 29); 1 = HCL and HSY outputs active

OFTS

Select output format: 0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.

YDEL2 to YDEL0

Luminance delay compensation:

YDEL2	YDEL1	YDEL0	figure	
0	0	0	0 × 2 / LLC	
0	0	1	+1 × 2 / LLC	
0	1	0	+2 × 2 / LLC	step size = 2 / LLC =
0	1	1	+3 × 2 / LLC	67.8 ns for 50 Hz
1	0	0	−4 × 2 / LLC	81.5 ns for 60 Hz
1	0	1	−3 × 2 / LLC	
1	1	0	−2 × 2 / LLC	
1	1	1	−1 × 2 / LLC	

HFRS “10”

Select HREF position: 0 = normal, HREF is matched to YUV output port; 1 = HREF is matched to CVBS input port.

VNOI1 to VNOI0

Vertical noise reduction

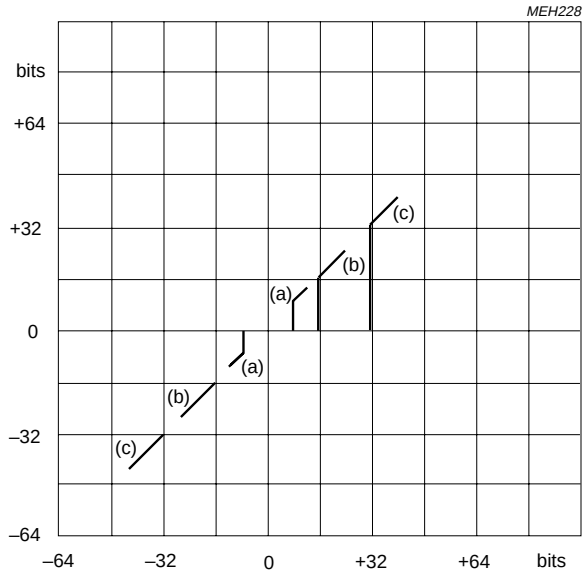
VNOI1	VNOI0	mode
0	0	normal
0	1	searching window
1	0	auto-deflection
1	1	vertical noise reduction bypassed

CHCV7U to CHCV0V “11”

Chrominance gain control (nominal values) for QAM-modulated input signals, effects output amplitude (SECAM with fixed gain):

D7	D6	D5	D4	D3	D2	D1	D0	gain	
1	1	1	1	1	1	1	1	maximum gain	
	:				:			to	)
0	1	0	1	1	0	0	1	CCIR level for PAL)	) default programmed
	:				:			to	) values dependent
0	0	1	0	1	1	0	0	CCIR level for NTSC)	) on application
	:				:			to	)
0	0	0	0	0	0	0	0	minimum gain	

HS6B7 to HS6B0 “14”	Horizontal sync begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two’s complement numbers with “hidden” sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HS6S7 to HS6S0 “15”	Horizontal sync begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two’s complement numbers with “hidden” sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HC6B7 to HC6B0 “16”	Horizontal clamp begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HC6S7 to HC6S0 “17”	Horizontal clamp stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HP6I7 to HP6I0 “18”	Horizontal sync after PHI1 for 60 Hz, step size = 8 / LLC. The delay time is selectable from –776/LLC (+97 decimal multiplier) to +776 /LLC (–97 decimal multiplier) equals data 61 to 9F (hex).



(a) CORI1 = 0; CORI0 = 1
(b) CORI1 = 1; CORI0 = 0
(c) CORI1 = 1; CORI0 = 1

Fig.15 Coring function adjustment by subaddress 06 to affect the bandfilter output signal. The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to 3LSB (Y0 to Y2) with respect to the 8-bit luminance output

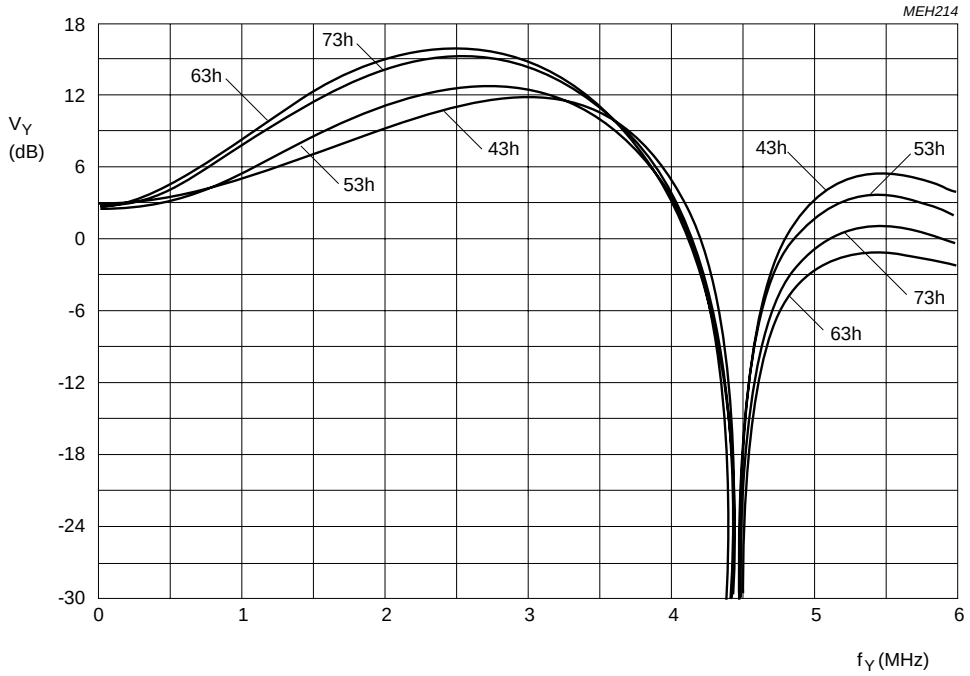


Fig.16 Luminance control in **50 Hz** / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

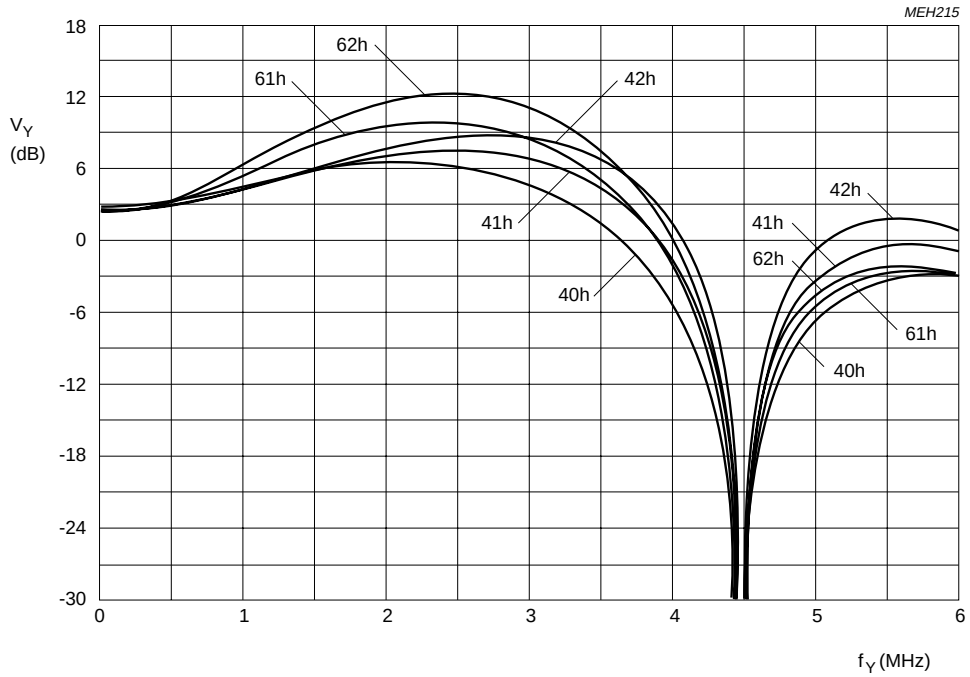


Fig.17 Luminance control in **50 Hz** / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

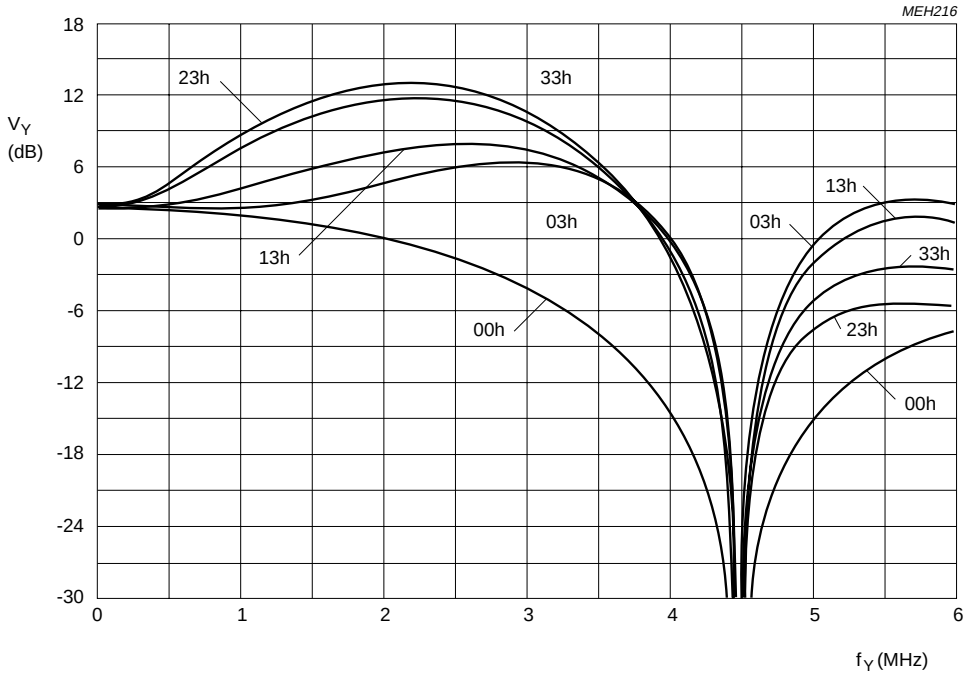


Fig.18 Luminance control in **50 Hz** / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum aperture bandpass filter characteristic.

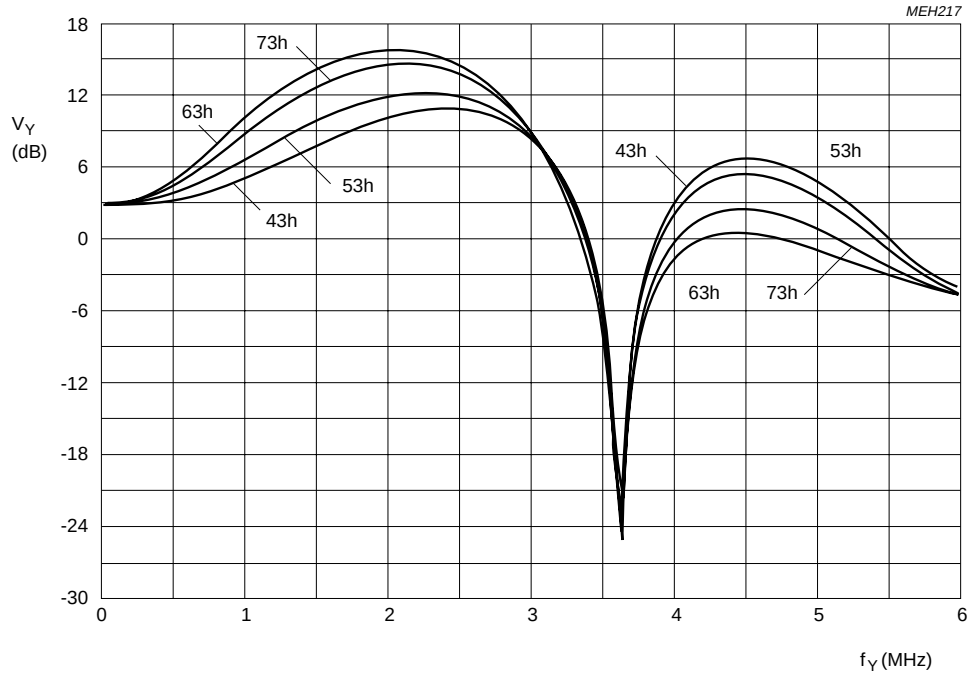


Fig.19 Luminance control in **60 Hz** / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

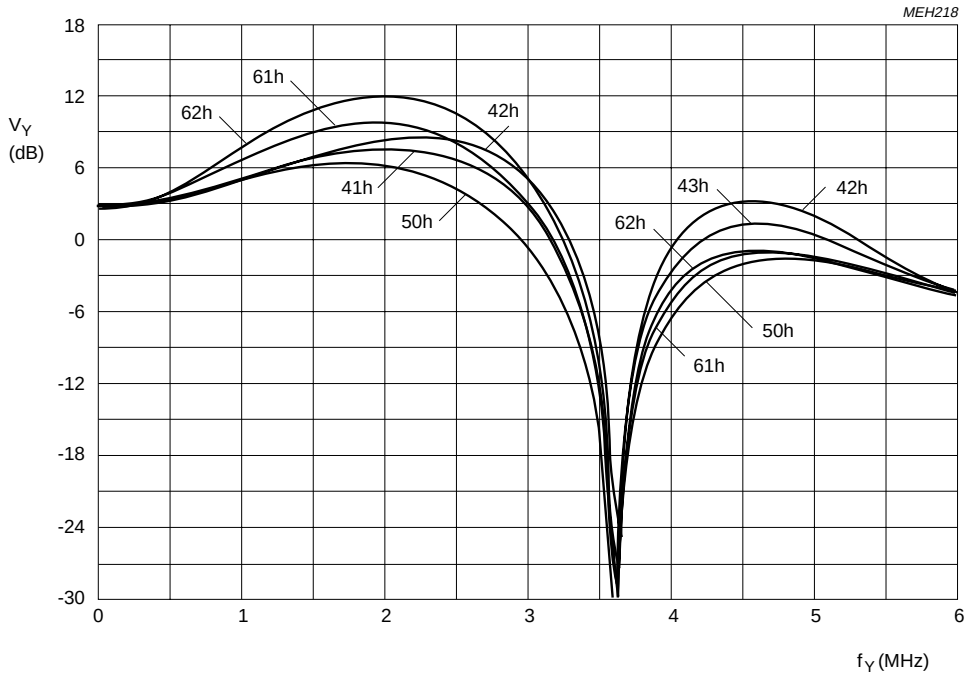


Fig.20 Luminance control in **60 Hz** / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

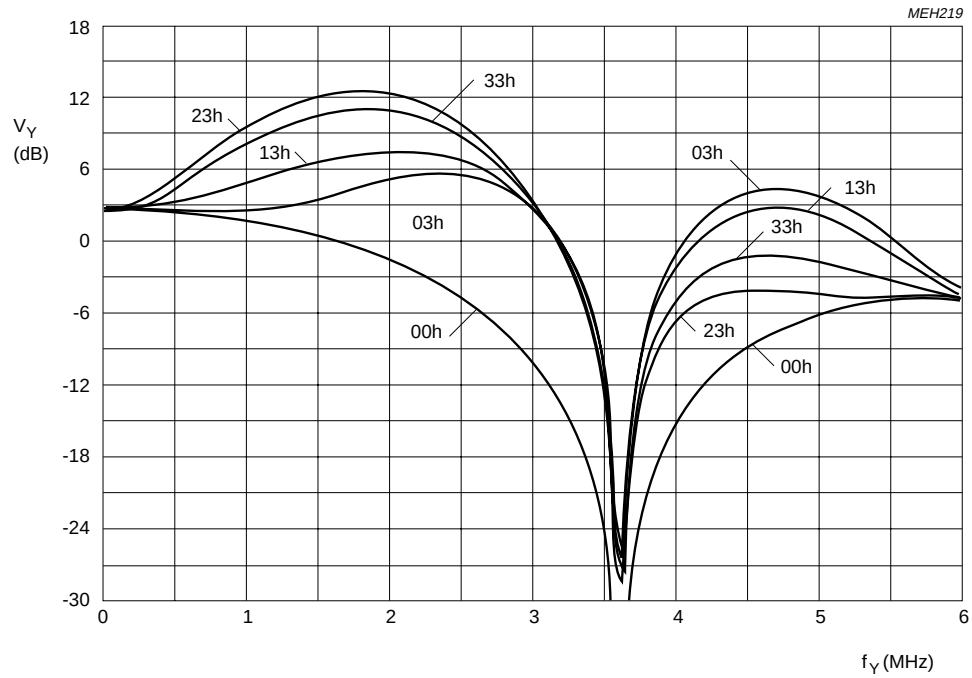


Fig.21 Luminance control in **60 Hz** / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum and minimum aperture bandpass filter characteristics.

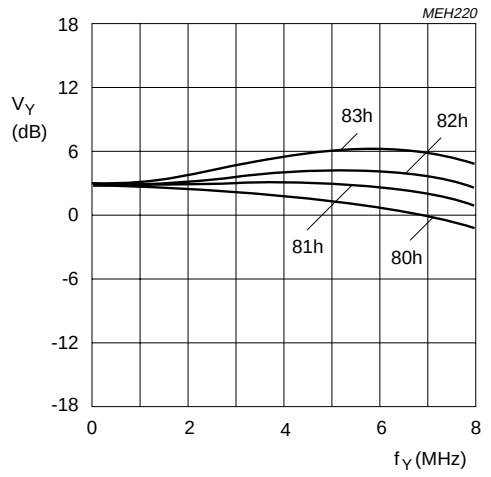


Fig.22 Luminance control in **50 Hz** / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass filter characteristics.

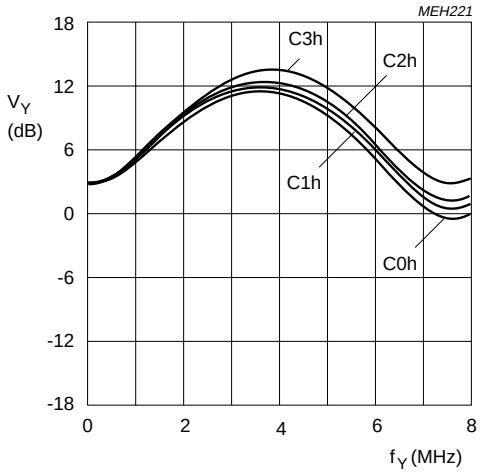


Fig.23 Luminance control in **50 Hz** / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

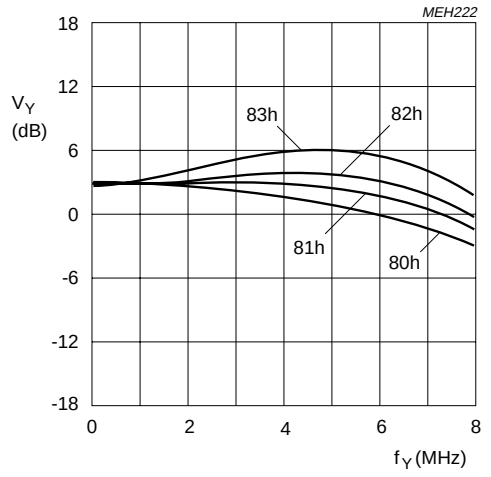


Fig.24 Luminance control in **60 Hz** / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass filter characteristics.

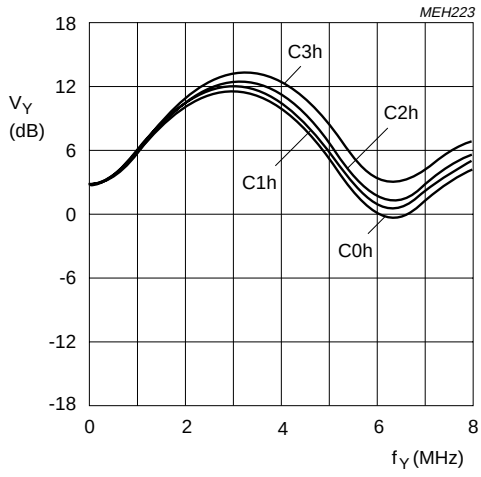


Fig.25 Luminance control in **60 Hz** / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

11 PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 13 and 14. (All numbers of the Table 6 are hex values). Slave address byte is 8A at pin 43 = 0 V (or 8E at pin 43 = +5 V).

Table 7 Recommended default values

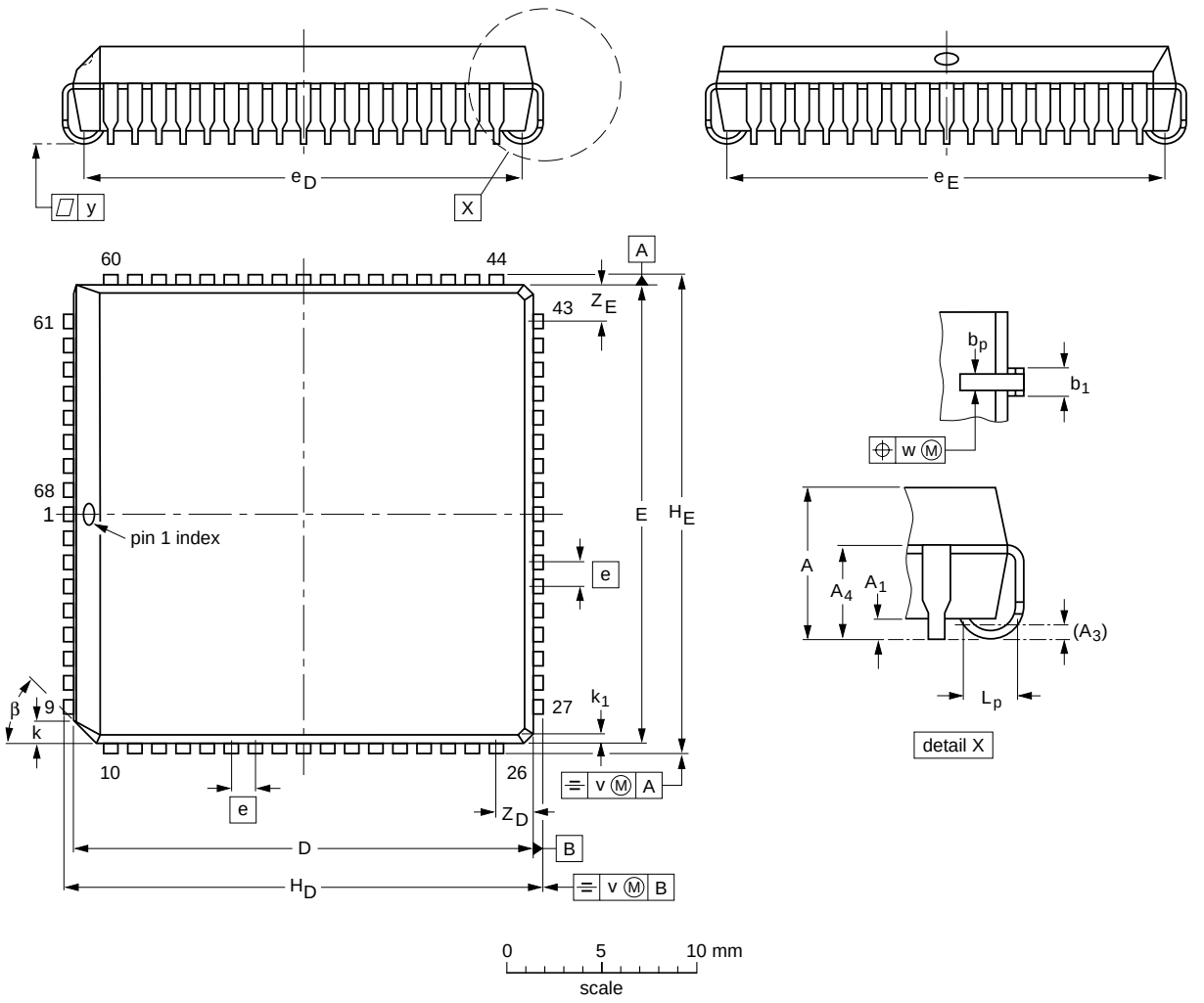
SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	50
01	HSYB(7-0)	H sync beginning for 50 Hz	30
02	HSYS(7-0)	H sync stop for 50 Hz	00
03	HCLB(7-0)	H clamping beginning for 50 Hz	E8
04	HCLS(7-0)	H clamping stop for 50 Hz	B6
05	HPHI(7-0)	H sync position for 50 Hz	F4
06	BYPS, PREF, BPSS(1-0)		
	CORI(1-0), APER(1-0)	luminance bandwidth control:	01[1]
07	HUEC(7-0)	hue control (0 degree)	00
08	CKTQ(4-0)	colour-killer threshold QUAM	F8
09	CKTS(4-0)	colour-killer threshold SECAM	F8
0A	PLSE(7-0)	PAL switch sensitivity	90
0B	SESE(7-0)	SECAM switch sensitivity	90
0C	COLO, LFIS(1-0)	chroma gain control settings	00
0D	VTRC, NFEN,HRMV, GPSW0 and SECS	standard/mode control	00[2][4], 01[3][4]
0E	HPLL, OEDC, OEHS, OEVS OEDY, CHRS, GPSW(2-1)	I/O and clock control	79, 7E[5]
0F	AUFD, FSEL, SXCR, SCEN, OFTS, YDEL(2-0)	miscellaneous control #1	91[6], 99[7]
10	HRFS, VNOI(1-0)	miscellaneous control #2	00
11	CHCV(7-0)	chrominance gain nominal value	2C[8], 59[9]
12	–	set to zero	00
13	–	set to zero	00
14	HS6B(7-0)	H sync beginning for 60 Hz	34
15	HS6S(7-0)	H sync stop for 60 Hz	0A
16	HC6B(7-0)	H clamping beginning for 60 Hz	F4
17	HC6S(7-0)	H clamping stop for 60 Hz	CE
18	HP6I(7-0)	H sync position for 60 Hz	F4

Notes

1. dependent on application (Figures 16 to 25)
2. for QUAM standards
3. for SECAM
4. HPLL is in TV mode; value for VCR mode is 80 (81 for SECAM VCR mode)
5. for Y/C mode
6. 4:1:1 format
7. 4:2:2 format
8. nominal value for UV CCIR level with NTSC source
9. nominal value for UV CCIR level with PAL source

12 PACKAGE OUTLINE

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

13 SOLDERING

13.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

13.2 Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

13.3 Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

15 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

16 PURCHASE OF PHILIPS I²C COMPONENTS

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