Integrated Digital CCIR-601 to PAL/NTSC Video Encoder

ADV7177/ADV7178

FEATURES

ITU-R BT601/656 YCrCb to PAL/NTSC video encoder
High quality, 9-bit video DACs
Integral nonlinearity <1 LSB at 9 bits
NTSC-M, PAL-M/N, PAL-B/D/G/H/I
Single 27 MHz crystal/clock required (±2 oversampling)
75 dB video SNR
32-bit direct digital synthesizer for color subcarrier
Multistandard video output support:
- **Composite (CVBS)**
- **Component S-video (Y/C)**
- **Component YUV or RGB**

Video input data port supports:
- **CCIR-656 4:2:2 8-bit parallel input format**
- **4:2:2 16-bit parallel input format**

Full video output drive or low signal drive capability
- **34.7 mA max into 37.5 Ω (doubly terminated 75 R)**
- **5 mA min with external buffers**

Programmable simultaneous composite and S-VHS (VHS) Y/C or RGB (SCART)/YUV video outputs
Programmable luma filters (low-pass/notch/extended)
Programmable VBI (vertical blanking interval)
Programmable subcarrier frequency and phase
Programmable luma delay
Individual on/off control of each DAC
CCIR and square pixel operation
Color-signal control/burst-signal control
Interlaced/noninterlaced operation
Complete on-chip video timing generator
OSD support (ADV7177 only)
Programmable multimode master/slave operation
Macrovision AntiTaping Rev. 7.01 (ADV7178 only)[1]
Closed captioning support
On-board voltage reference
2-wire serial MPU interface (I²C®-compatible)
Single-supply 5 V or 3 V operation
Small 44-lead MQFP package
Synchronous 27 MHz/13.5 MHz clock output

APPLICATIONS

MPEG-1 and MPEG-2 video, DVD, digital satellite, cable systems (set-top boxes/IRDs), digital TVs, CD video/karaoke, video games, PC video/multimedia

[1] The Macrovision anticopy process is licensed for noncommercial home use only, which is its sole intended use in the device. Please contact sales office for latest Macrovision version available. ITU-R and CCIR are used interchangeably in this document (ITU-R has replaced CCIR recommendations).

FUNCTIONAL BLOCK DIAGRAM

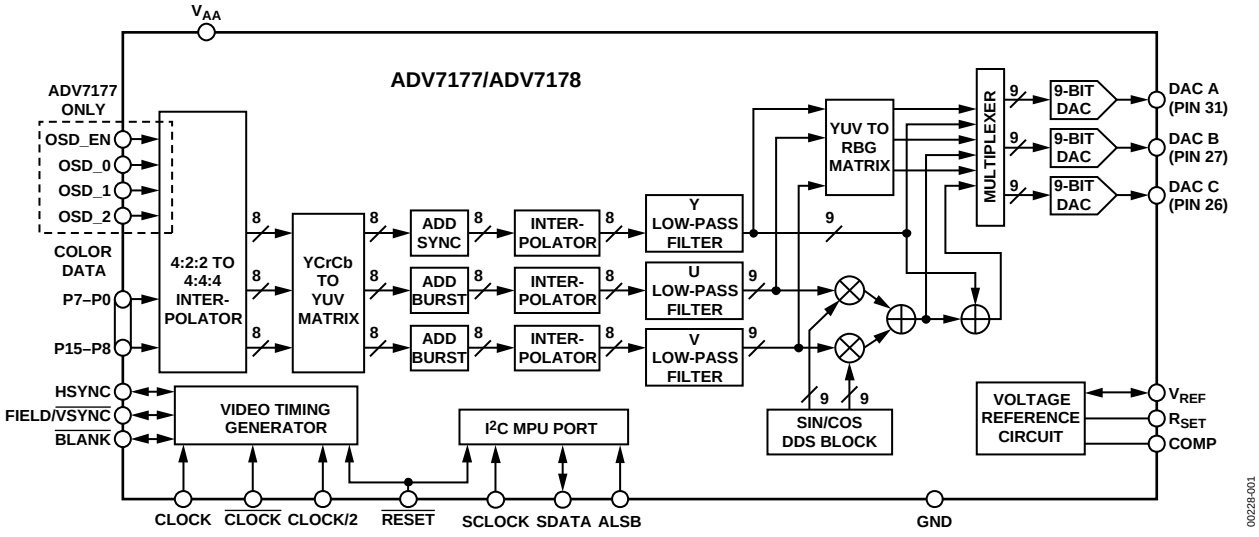

Figure 1.

Rev. C

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3/02—Rev. A to Rev. B

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GENERAL DESCRIPTION

The ADV7177/AD7178 are integrated digital video encoders that convert digital CCIR-601 4:2:2 8- or 16-component video data into a standard analog baseband television signal compatible with worldwide standards. The 4:2:2 YUV video data is interpolated to 2× the pixel rate. The color-difference components (UV) are quadrature modulated using a subcarrier frequency generated by an on-chip, 32-bit digital synthesizer (also running at 2× the pixel rate). The 2× pixel rate sampling allows for better signal-to-noise ratio. A 32-bit DDS with a 9-bit look-up table produces a superior subcarrier in terms of both frequency and phase. In addition to the composite output signal, there is the facility to output S-video (Y/C video), YUV or RGB video.

Each analog output is capable of driving the full video-level (34.7 mA) signal into an unbuffered, doubly terminated 75 Ω load. With external buffering, the user has the additional option to scale back the DAC output current to 5 mA min, thereby significantly reducing the power dissipation of the device.

The ADV7177/ADV7178 also support both PAL and NTSC square pixel operation.

The output video frames are synchronized with the incoming data timing reference codes. Optionally, the encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD timing signals. These timing signals can be adjusted to change pulse width and position while the parts are in master mode. The encoder requires a single, 2× pixel rate (27 MHz) clock for standard operation. Alternatively, the encoder requires a 24.5454 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal timing is generated on-chip.

The ADV7177/ADV7178 modes are set up over a 2-wire serial bidirectional port (I^2C-compatible) with two slave addresses.

Functionally, the ADV7178 and the ADV7177 are the same except that the ADV7178 can output the Macrovision anticopy algorithm, and OSD is only supported on the ADV7177.

The ADV7177/ADV7178 are packaged in a 44-lead, thermally enhanced MQFP package.

SPECIFICATIONS

5 V SPECIFICATIONS

V_{AA} = 5 V ± 5%,[1] V_{REF} = 1.235 V, R_{SET} = 300 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				9	Bits
Accuracy (Each DAC)					
Integral Nonlinearity				±1.0	LSB
Differential Nonlinearity	Guaranteed monotonic			±1.0	LSB
DIGITAL INPUTS[3]					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}[4]	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Current, I_{IN}[5]	V_{IN} = 0.4 V or 2.4 V			± 50	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[3]					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS[3]					
Output Current[6]	R_{SET} = 300 Ω, R_L = 75 Ω	16.5	17.35	18.5	mA
Output Current[7]			5		mA
DAC-to-DAC Matching			0.6	5	%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			15		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
VOLTAGE REFERENCE[3]					
Reference Range, V_{REF}	$I_{VREFOUT}$ = 20 μA	1.112	1.235	1.359	V
POWER REQUIREMENTS[3, 8]					
V_{AA}		4.75	5.0	5.25	V
Low Power Mode					
I_{DAC} (max)[9]			62		mA
I_{DAC} (min)[9]			25		mA
I_{CCT}[10]			100	150	mA
Power-Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.
[2] Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] Guaranteed by characterization.
[4] All digital input pins except pins $\overline{\text{RESET}}$, OSD0, and CLOCK.
[5] Excluding all digital input pins except pins $\overline{\text{RESET}}$, OSD0, and CLOCK.
[6] Full drive into 75 Ω load.
[7] Minimum drive current (used with buffered/scaled output load).
[8] Power measurements are taken with clock frequency = 27 MHz. Max T_J = 110°C.
[9] I_{DAC} is the total current (min corresponds to 5 mA output per DAC, max corresponds to 18.5 mA output per DAC) to drive all three DACs. Turning off individual DACs reduces I_{DAC} correspondingly.
[10] I_{CCT} (circuit current) is the continuous current required to drive the device.

3.3 V SPECIFICATIONS

V_{AA} = 3.0 V to 3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 300 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				9	Bits
Accuracy (Each DAC)					
Integral Nonlinearity				±0.5	LSB
Differential Nonlinearity	Guaranteed monotonic			±0.5	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2		V
Input Low Voltage, V_{INL}			0.8		V
Input Current, I_{IN}[3, 4]	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Current, I_{IN}[3, 5]	V_{IN} = 0.4 V or 2.4 V			±50	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA		2.4		V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA		0.4		V
Three-State Leakage Current[3]				10	μA
Three-State Output Capacitance[3]			10		pF
ANALOG OUTPUTS[3]					
Output Current[6, 7]	R_{SET} = 300 Ω, R_L = 75 Ω	16.5	17.35	18.5	mA
Output Current[8]			5		mA
DAC-to-DAC Matching			2.0		%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			15		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
POWER REQUIREMENTS[3, 9]					
V_{AA}		3.0	3.3	3.6	V
Normal Power Mode					
I_{DAC} (max)[10]	R_{SET} = 300 Ω, R_L = 150 Ω		113	116	mA
I_{DAC} (min)[3]			15		mA
I_{CCT}			45		mA
Low Power Mode					
I_{DAC} (max)[3]			60		mA
I_{DAC} (min)[3]			25		mA
I_{CCT}[11]			45		mA
Power-Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.
[2] Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] Guaranteed by characterization.
[4] All digital input pins except pins $\overline{\text{RESET}}$, OSD0, and CLOCK.
[5] Excluding all digital input pins except pins $\overline{\text{RESET}}$, OSD0, and CLOCK.
[6] Full drive into 75 Ω load.
[7] DACs can output 35 mA typically at 3.3 V (R_{SET} = 150 Ω and R_L = 75 Ω), optimum performance obtained at 18 mA DAC current (R_{SET} = 300 Ω and R_L = 150 Ω).
[8] Minimum drive current (used with buffered/scaled output load).
[9] Power measurements are taken with clock frequency = 27 MHz. Max T_J = 110°C.
[10] I_{DAC} is the total current (min corresponds to 5 mA output per DAC, max corresponds to 38 mA output per DAC) to drive all three DACs. Turning off individual DACs reduces IDAC correspondingly.
[11] I_{CCT} (circuit current) is the continuous current required to drive the device.

5 V DYNAMIC SPECIFICATIONS

V_{AA} = 4.75 V to 5.25 V,[1] V_{REF} = 1.235 V, R_{SET} = 300 Ω. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted.

Table 3.

Parameter	Conditions[1]	Min	Typ	Max	Unit
FILTER CHARACTERISTICS					
Luma Bandwidth[3] (Low-Pass Filter)	NTSC Mode				
Stop-Band Cutoff	>54 dB Attenuation	7.0			MHz
Pass-Band Cutoff, $F_{3\ dB}$	>3 dB Attenuation	4.2			MHz
Chroma Bandwidth	NTSC Mode				
Stop-Band Cutoff	>40 dB Attenuation	3.2			MHz
Pass-Band Cutoff, $F_{3\ dB}$	>3 dB Attenuation	2.0			MHz
Luma Bandwidth[3] (Low-Pass Filter)	PAL Mode				
Stop-Band Cutoff	>50 dB Attenuation	7.4			MHz
Pass-Band Cutoff, $F_{3\ dB}$	>3 dB Attenuation	5.0			MHz
Chroma Bandwidth	PAL Mode				
Stop-Band Cutoff	>40 dB Attenuation	4.0			MHz
Pass-Band Cutoff $F_{3\ dB}$	>3 dB Attenuation	2.4			MHz
Differential Gain[4]	Lower Power Mode		2.0		%
Differential Phase[4]	Lower Power Mode		1.5		Degrees
SNR[4] (Pedestal)	RMS		75		dB rms
	Peak Periodic		70		dB p-p
SNR[4] (Ramp)	RMS		57		dB rms
	Peak Periodic		56		dB p-p
Hue Accuracy[4]			1.2		Degrees
Color Saturation Accuracy[4]			1.4		%
Chroma Nonlinear Gain[4]	Referenced to 40 IRE		1.0		± %
Chroma Nonlinear Phase[4]	NTSC		0.4		± Degrees
	PAL		0.6		± Degrees
Chroma/Luma Intermod[4]	Referenced to 714 mV (NTSC)		0.2		± %
	Referenced to 700 mV (PAL)		0.2		± %
Chroma/Luma Gain Inequality[4]			0.6		± %
Chroma/Luma Delay Inequality[4]			2.0		ns
Luminance Nonlinearity[4]			1.2		± %
Chroma AM Noise[4]			64		dB
Chroma PM Noise[4]			62		dB

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.
[2] Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] These specifications are for the low-pass filter only and are guaranteed by design. For other internal filters, see Table 10.
[4] Guaranteed by characterization.

3.3 V DYNAMIC SPECIFICATIONS

V_{AA} = 3.0 V to 3.6 V,[1] V_{REF} = 1.235 V, R_{SET} = 300 Ω. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted.

Table 4.

Parameter	Conditions[1]	Min	Typ	Max	Unit
FILTER CHARACTERISTICS					
Luma Bandwidth[3] (Low-Pass Filter)	NTSC mode				
Stop-Band Cutoff	>54 dB attenuation	7.0			MHz
Pass-Band Cutoff, $F_{3\ dB}$	>3 dB attenuation	4.2			MHz
Chroma Bandwidth	NTSC mode				
Stop-Band Cutoff	>40 dB attenuation	3.2			MHz
Pass-Band Cutoff, $F_{3\ dB}$	>3 dB attenuation	2.0			MHz
Luma Bandwidth[3] (Low-Pass Filter)	PAL mode				
Stop-Band Cutoff	>50 dB attenuation	7.4			MHz
Pass-Band Cutoff, $F_{3\ dB}$	>3 dB attenuation	5.0			MHz
Chroma Bandwidth	PAL mode				
Stop-Band Cutoff	>40 dB attenuation	4.0			MHz
Pass-Band Cutoff, $F_{3\ dB}$	>3 dB attenuation	2.4			MHz
Differential Gain[4]	Normal power mode		1.0		%
Differential Phase[4]	Normal power mode		1.0		Degrees
SNR[4] (Pedestal)	RMS		70		dB rms
	Peak periodic		64		dB p-p
SNR[4] (Ramp)	RMS		56		dB rms
	Peak periodic		54		dB p-p
Hue Accuracy[4]			1.2		Degrees
Color Saturation Accuracy[4]			1.4		%
Luminance Nonlinearity[4]			1.4		± %
Chroma AM Noise[4]	NTSC		64		dB
Chroma PM Noise[4]	NTSC		62		dB
Chroma AM Noise[4]	PAL		64		dB
Chroma PM Noise[4]	PAL		62		dB

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.
[2] Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] These specifications are for the low-pass filter only and are guaranteed by design. For other internal filters, see Table 7.
[4] Guaranteed by characterization.

5 V TIMING SPECIFICATIONS

V_{AA} = 4.75 V to 5.25 V,[1] V_{REF} = 1.235 V, R_{SET} = 300 Ω. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted.

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		100	kHz
SCLOCK High Pulse Width, t_1		4.0			µs
SCLOCK Low Pulse Width, t_2		4.7			µs
Hold Time (Start Condition), t_3	After this period, the first clock is generated	4.0			µs
Setup Time (Start Condition), t_4	Relevant for repeated start condition	4.7			µs
Data Setup Time, t_5		250			ns
SDATA, SCLOCK Rise Time, t_6				1	µs
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		4.7			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			5		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[3, 4, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}				24	ns
Digital Output Hold Time, t_{14}			4		ns
Pipeline Delay, t_{15}			37		Clock Cycles
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns
INTERNAL CLOCK CONTROL					
Clock/2 Rise Time, t_{16}			7		ns
Clock/2 Fall Time, t_{17}			7		ns
OSD TIMING[4]					
OSD Setup Time, t_{18}			6		ns
OSD Hold Time, t_{19}			2		ns

[1] The max/min specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] TTL input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.
[4] Guaranteed by characterization.
[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.
[6] Pixel port consists of the following:
Pixel inputs: P15–P0
Pixel controls: $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock input: CLOCK

3.3 V TIMING SPECIFICATIONS

V_{AA} = 3.0 V–3.6 V,[1] V_{REF} = 1.235 V, R_{SET} = 300 Ω. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted.

Table 6.

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		100	kHz
SCLOCK High Pulse Width, t_1		4.0			µs
SCLOCK Low Pulse Width, t_2		4.7			µs
Hold Time (Start Condition), t_3	After this period the first clock is generated	4.0			µs
Setup Time (Start Condition), t_4	Repeated for start condition	4.7			µs
Data Setup Time, t_5		250			ns
SDATA, SCLOCK Rise Time, t_6				1	µs
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		4.7			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[3, 4, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}				24	ns
Digital Output Hold Time, t_{14}			4		ns
Pipeline Delay, t_{15}			37		Clock cycles
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns
INTERNAL CLOCK CONTROL					
Clock/2 Rise Time, t_{16}			10		ns
Clock/2 Fall Time, t_{17}			10		ns
OSD TIMING[4]					
OSD Setup Time, t_{18}			10		ns
OSD Hold Time, t_{19}			2		ns

[1] The max/min specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] TTL input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.
[4] Guaranteed by characterization.
[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.
[6] Pixel port consists of the following:
Pixel inputs: P15–P0
Pixel controls: $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock input: CLOCK

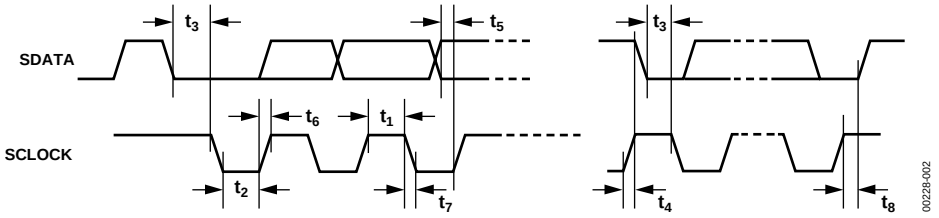


Figure 2. MPU Port Timing Diagram

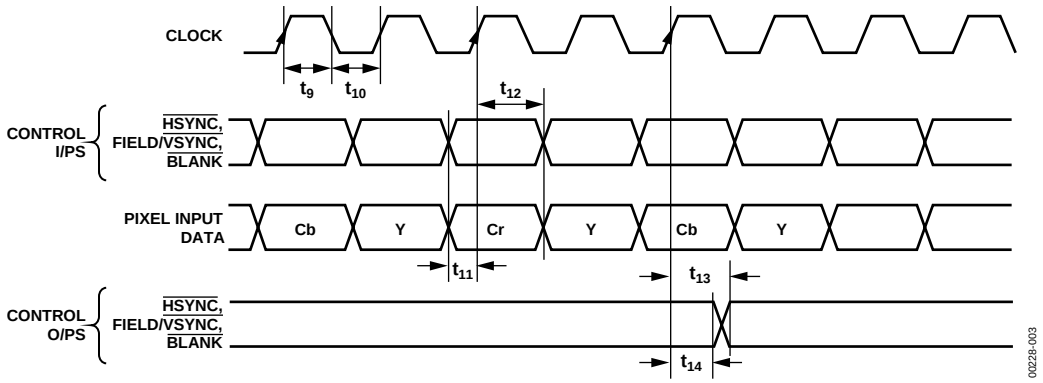


Figure 3. Pixel and Control Data Timing Diagram

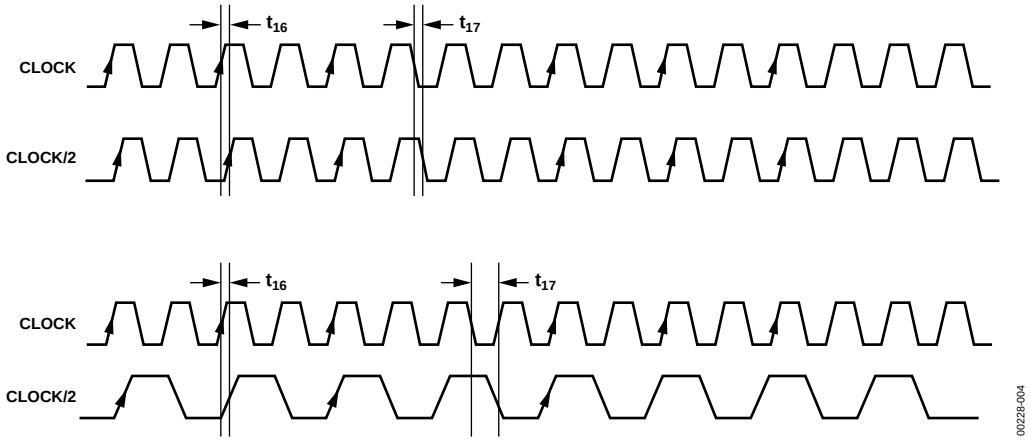


Figure 4. Internal Timing Diagram

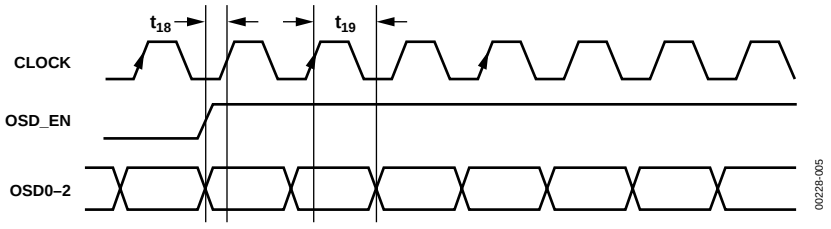


Figure 5. OSD Timing Diagram

ABSOLUTE MAXIMUM RATINGS

STRESS RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7.

Parameter	Rating
V_{AA} to GND	7 V
Voltage on Any Digital Input Pin	GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S)	–65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10 sec)	260°C
Analog Outputs to GND[1]	GND – 0.5 V to V_{AA}

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

PACKAGE THERMAL PERFORMANCE

The 44-lead MQFP package used for this device has a junction-to-ambient thermal resistance (θ_{JA}) in still air on a 4-layer PCB of 53.2°C/W. The junction-to-case thermal resistance (θ_{JC}) is 18.8°C/W. Care must be taken when operating the part in certain conditions to prevent overheating. Table 8 lists the conditions to use when using the part.

Table 8. Allowable Operating Conditions

Condition	5 V	3 V
3 DACs on, double 75 R[1]	No	Yes
3 DACs on, low power[2]	Yes	Yes
3 DACs on, buffered[3]	Yes	Yes
2 DACs on, double 75 R	No	Yes
2 DACs on, low power	Yes	Yes
2 DACs on, buffered	Yes	Yes

[1] DAC on, double 75 R refers to a condition where the DACs are terminated into a double 75 R load and low power mode is disabled.
[2] DAC on, low power refers to a condition where the DACs are terminated in a double 75 R load and low power mode is enabled.
[3] DAC on, buffered refers to a condition where the DAC current is reduced to 5 mA and external buffers are used to drive the video loads.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

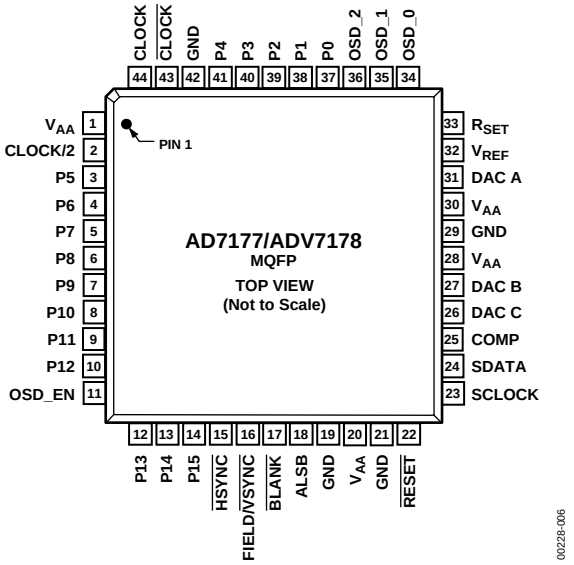


Figure 6. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Function
1, 20, 28, 30	V_{AA}	P	Power Supply.
2	CLOCK/2	O	Synchronous Clock Output Signal. Can be either 27 MHz or 13.5 MHz; this can be controlled by MR32 and MR33 in Mode Register 3.
3 to 10, 12 to 14, 37 to 41	P5 to P12, P13 to 14, P0 to P4	I	8-Bit, 4:2:2 Multiplexed YCrCb Pixel Port (P7–P0) or 16-Bit YCrCb Pixel Port (P15–P0). P0 represents the LSB.
11	OSD_EN	I	Enables OSD input data on the video outputs.
15	$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin can be configured to output (master mode) or accept (slave mode) Sync signals.
16	FIELD/ $\overline{\text{VSYNC}}$	I/O	Dual Function Field (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin can be configured to output (master mode) or accept (slave mode) these control signals.
17	$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic 0. This signal is optional.
18	ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
19, 21, 29, 42	GND	G	Ground Pin.
22	$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7177/ADV7178 into default mode. This is NTSC operation, Timing Slave Mode 0, 8-bit operation, 2× composite and S VHS out.
23	SCLOCK	I	MPU Port Serial Interface Clock Input.
24	SDATA	I/O	MPU Port Serial Data Input/Output.
25	COMP	O	Compensation Pin. Connect a 0.1 µF capacitor from COMP to V_{AA}.
26	DAC C	O	DAC C Analog Output.
27	DAC B	O	DAC B Analog Output.
31	DAC A	O	DAC A Analog Output.
32	V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
33	R_{SET}	I	A 300 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the video signals.
34–36	OSD_0 to OSD_2	I	On Screen Display Inputs.
43	$\overline{\text{CLOCK}}$	O	Crystal Oscillator Output (to crystal). Leave unconnected if no crystal is used.
44	CLOCK	I	Crystal Oscillator Input. If no crystal is used, this pin can be driven by an external TTL clock source; it requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.

TYPICAL PERFORMANCE CHARACTERISTICS

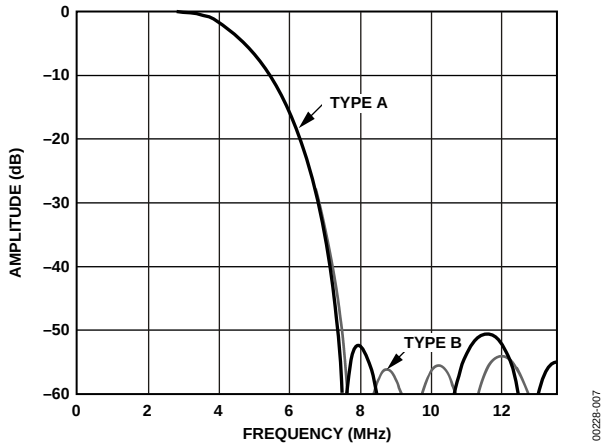


Figure 7. NTSC Low-Pass Filter

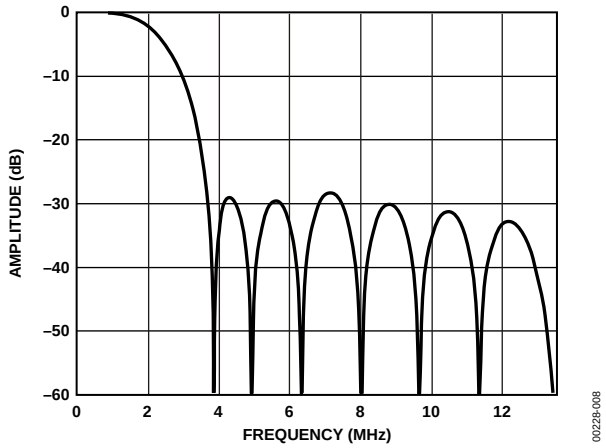


Figure 8. NTSC Notch Filter

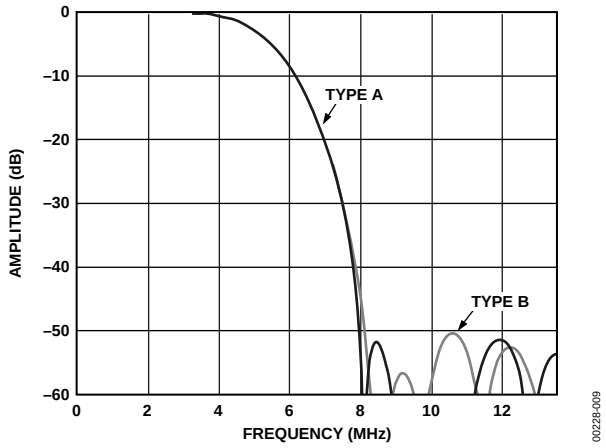


Figure 9. PAL Low-Pass Filter

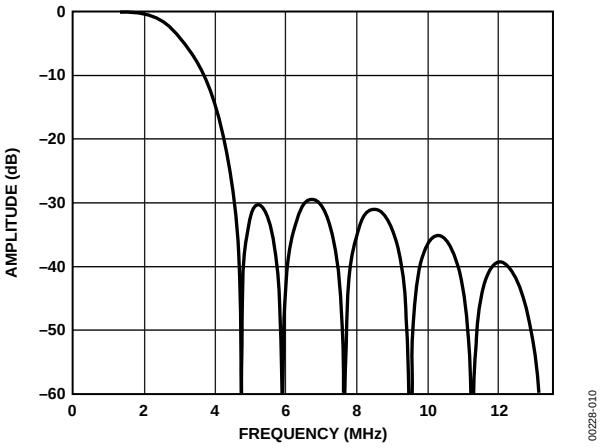


Figure 10. PAL Notch Filter

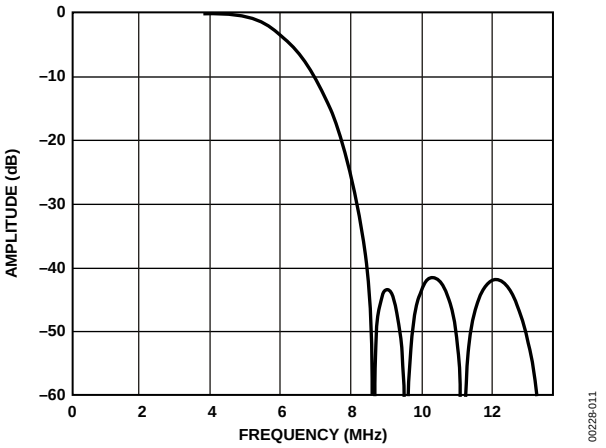


Figure 11. NTSC/PAL Extended Mode Filter

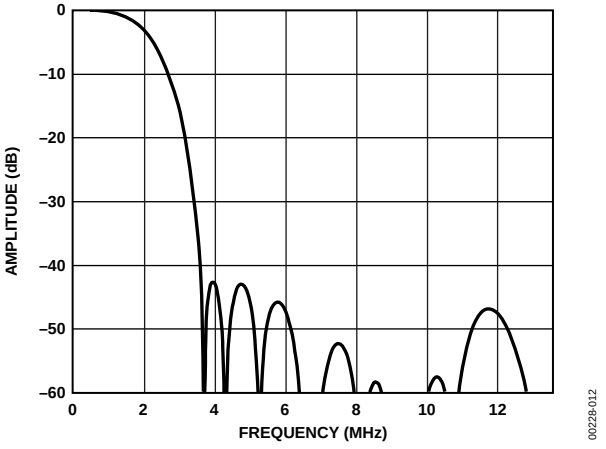


Figure 12. NTSC UV Filter

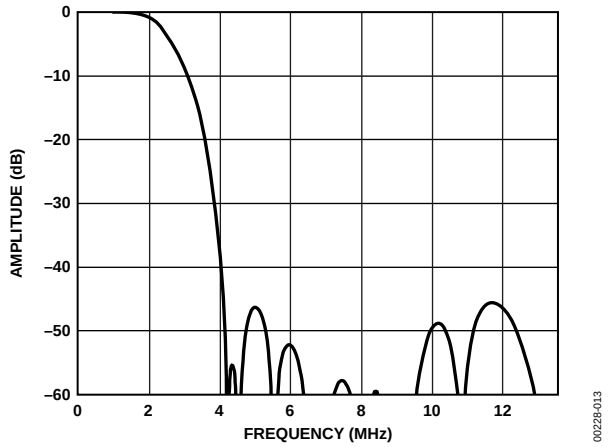


Figure 13 . PAL UV Filter

THEORY OF OPERATION

DATA PATH DESCRIPTION

For PAL B, D, G, H, I, M, N and NTSC M, N modes, YCrCb 4:2:2 data is input via the CCIR-656-compatible pixel port at a 27 MHz data rate. The pixel data is demultiplexed to form three data paths. Y typically has a range of 16 to 235, Cr and Cb typically have a range of 128 ± 112; however, it is possible to input data from 1 to 254 on both Y, Cb and Cr. The ADV7177/ADV7178 support PAL (B, D, G, H, I, N, M) and NTSC (with and without pedestal) standards. The appropriate SYNC, $\overline{\text{BLANK}}$, and burst levels are added to the YCrCb data. Macrovision AntiTaping (ADV7178 only), closed captioning, OSD (ADV7177 only), and teletext levels are also added to Y, and the resulting data is interpolated to a rate of 27 MHz. The interpolated data is filtered and scaled by three digital FIR filters.

The U and V signals are modulated by the appropriate subcarrier sine/cosine phases and added together to make up the chrominance signal. The luma (Y) signal can be delayed 1 to 3 luma cycles (each cycle is 74 ns) with respect to the chroma signal. The luma and chroma signals are then added together to make up the composite video signal. All edges are slew-rate limited.

The YCrCb data is also used to generate RGB data with appropriate SYNC and $\overline{\text{BLANK}}$ levels. The RGB data is in synchronization with the composite video output. Alternatively, analog YUV data can be generated instead of RGB.

The three 9-bit DACs can be used to output:

- RGB video
- YUV video
- One composite video signal + LUMA and CHROMA (S-video).

Alternatively, each DAC can be individually powered off if not required.

Video output levels are illustrated in the section NTSC Waveforms With Pedestal.

Internal Filter Response

The Y filter supports several different frequency responses, including two 4.5 MHz/5.0 MHz low-pass responses, PAL/NTSC subcarrier notch responses, and a PAL/NTSC extended response. The U and V filters have a 1.0 MHz/1.3 MHz low-pass response for NTSC/PAL. These filter characteristics are illustrated in the Typical Performance Characteristics section.

Color-Bar Generation

The devices can be configured to generate 100/7.5/75/7.5 color bars for NTSC or 100/0/75/0 for PAL color bars. These are enabled by setting MR17 of Mode Register 1 to Logic 1.

Square Pixel Mode
The ADV7177/ADV7178 can be used to operate in square pixel mode. For NTSC operation, an input clock of 24.5454 MHz is required. Alternatively, an input clock of 29.5 MHz is required for PAL operation. The internal timing logic adjusts accordingly for square pixel mode operation.

Color Signal Control
The color information can be switched on and off the video output by using Bit MR24 of Mode Register 2.

Burst Signal Control
The burst information can be switched on and off the video output using Bit MR25 of Mode Register 2.

NTSC Pedestal Control
The pedestal on both odd and even fields can be controlled on a line-by-line basis by using the NTSC pedestal control registers. This allows the pedestals to be controlled during the vertical blanking interval.

PIXEL TIMING DESCRIPTION

The ADV7177/ADV7178 can operate in either 8-bit or 16-bit YCrCb mode.

8-Bit YCrCb Mode

This default mode accepts multiplexed YCrCb inputs through the P7 to P0 pixel inputs. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc. The Y, Cb and Cr data are input on a rising clock edge.

16-Bit YCrCb Mode

This mode accepts Y inputs through the P7 to P0 pixel inputs and multiplexed CrCb inputs through the P15 to P8 pixel inputs. The data is loaded on every second rising edge of CLOCK. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc.

OSD

The ADV7177 supports OSD. There are twelve, 8-bit OSD registers loaded with data from the four most significant bits of Y, Cb, Cr input pixel data bytes. A choice of eight colors can, therefore, be selected via the OSD_0, OSD_1, OSD_2 pins, each color being a combination of 12 bits of Y, Cb, Cr pixel data. The display is under control of the OSD_EN pin. The OSD window can be an entire screen or just one pixel, and its size may change by using the OSD_EN signal to control the width on a line-by-line basis. Figure 5 illustrates OSD timing on the ADV7177.

VIDEO TIMING DESCRIPTION

The ADV7177/ADV7178 are intended to interface to off-the-shelf MPEG1 and MPEG2 decoders. Consequently, the ADV7177/ADV7178 accept 4:2:2 YCrCb pixel data via a CCIR-656 pixel port, and have several video timing modes allowing them to be configured as either a system master video timing generator or a slave to the system video timing generator. The ADV7177/ADV7178 generate all of the required horizontal and vertical timing periods and levels for the analog video outputs. It is important to note that the CCIR-656 data stream should not contain ancillary data packets as per the BT1364 specification. This data can corrupt the internal synchronization circuitry of the devices, resulting in loss of synchronization on the output.

The ADV7177/ADV7178 calculate the width and placement of analog sync pulses, blanking levels, and color burst envelopes. Color bursts are disabled on appropriate lines, and serration and equalization pulses are inserted where required.

In addition, the ADV7177/ADV7178 support a PAL or NTSC square pixel operation in slave mode. The parts require an input pixel clock of 24.5454 MHz for NTSC and an input pixel clock of 29.5 MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7177/ADV7178 have four distinct master and four distinct slave timing configurations. Timing control is established with the bidirectional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulse widths and where they occur in relation to each other.

Vertical Blanking Data Insertion (VBI)

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not bear line sync or pre- and post-equalization pulses (see the Typical Performance Characteristics section). This mode of operation is called partial blanking and is selected by setting MR31 to 1. It allows the insertion of any VBI data (opened VBI) into the encoded output waveform. This data is present in the digitized incoming YCbCr data stream (for example, WSS data, CGMS, and VPS). Alternatively, the entire VBI can be blanked (no VBI data inserted) on these lines by setting MR31 to 0.

Table 10. Luminance Internal Filter Specifications

Filter Selection	MR04	MR03	Pass-Band Cutoff (MHz)	Pass-Band Ripple (dB)	Stop-Band Cutoff (MHz)	Stop-Band Attenuation (dB)	$F_{3\,dB}$
NTSC	0	0	2.3	0.026	7.0	>54	4.2
PAL	0	0	3.4	0.098	7.3	>50	5.0
NTSC	0	1	1.0	0.085	3.57	>27.6	2.1
PAL	0	1	1.4	0.107	4.43	>29.3	2.7
NTSC/PAL	1	0	4.0	0.150	7.5	>40	5.35
NTSC	1	1	2.3	0.054	7.0	>54	4.2
PAL	1	1	3.4	0.106	7.3	>50.3	5.0

Table 11. Chrominance Internal Filter Specifications

Filter Selection	Pass-Band Cutoff (MHz)	Pass-Band Ripple (dB)	Stop-Band Cutoff (MHz)	Stop-Band Attenuation (dB)	Attenuation @ 1.3 MHz (dB)	$F_{3\,dB}$
NTSC	1.0	0.085	3.2	>40	0.3	2.05
PAL	1.3	0.04	4.0	>40	0.02	2.45

TIMING AND CONTROL

Mode 0 (CCIR-656): Slave Option

Timing Register 0 TR0 = X X X X X 0 0 0

The ADV7177/ADV7178 are controlled by the start active video (SAV) and end active video (EAV) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 14. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode.

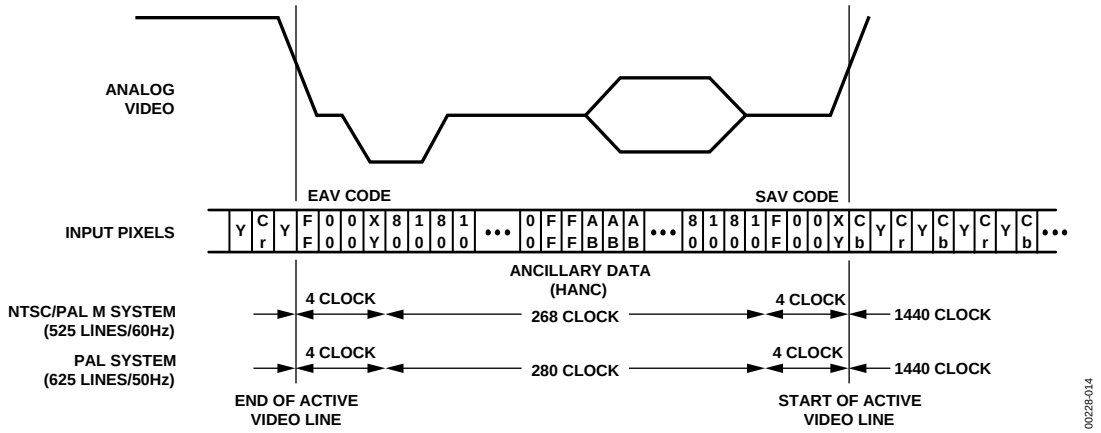


Figure 14. Timing Mode 0 (Slave Mode)

Mode 0 (Ccir-656): Master Option

Timing Register 0 TR0 = X X X X X 0 0 1

The ADV7177/ADV7178 generate H, V, and F signals required for the SAV and EAV time codes in the CCIR-656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin, and the F bit is output on the FIELD/$\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 15 (NTSC) and Figure 16 (PAL). The H, V, and F transitions relative to the video waveform are illustrated in Figure 17.

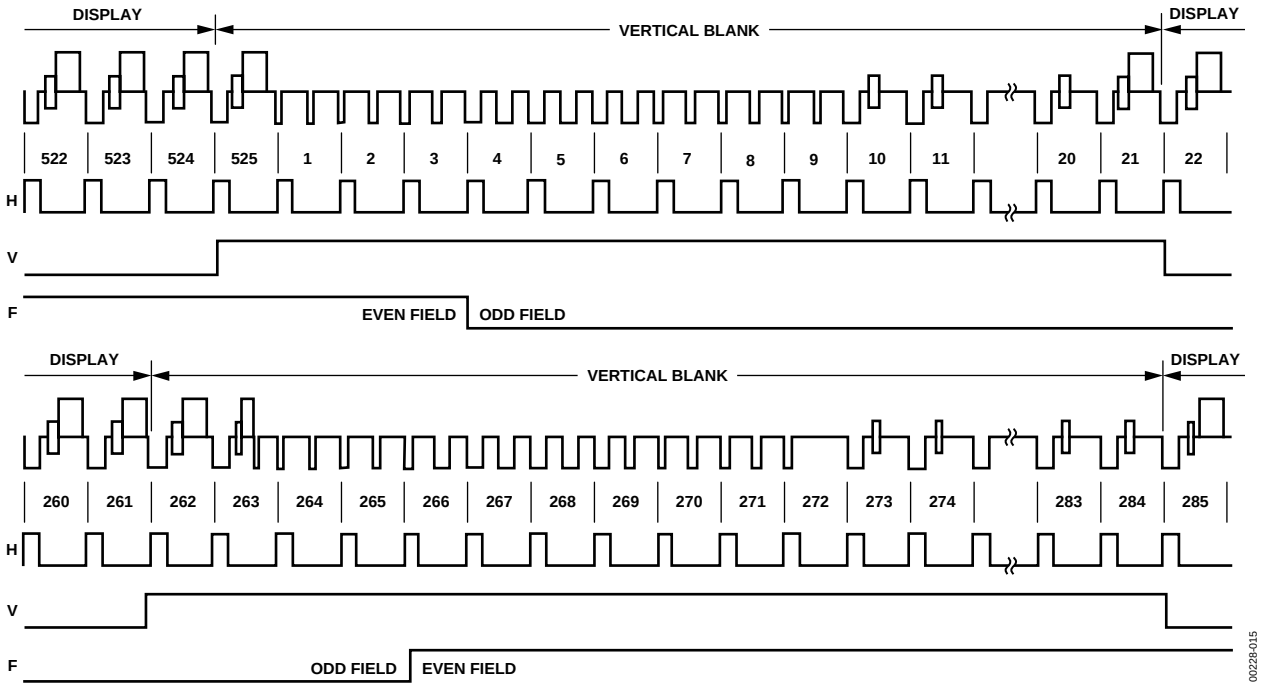


Figure 15. Timing Mode 0 (NTSC Master Mode)

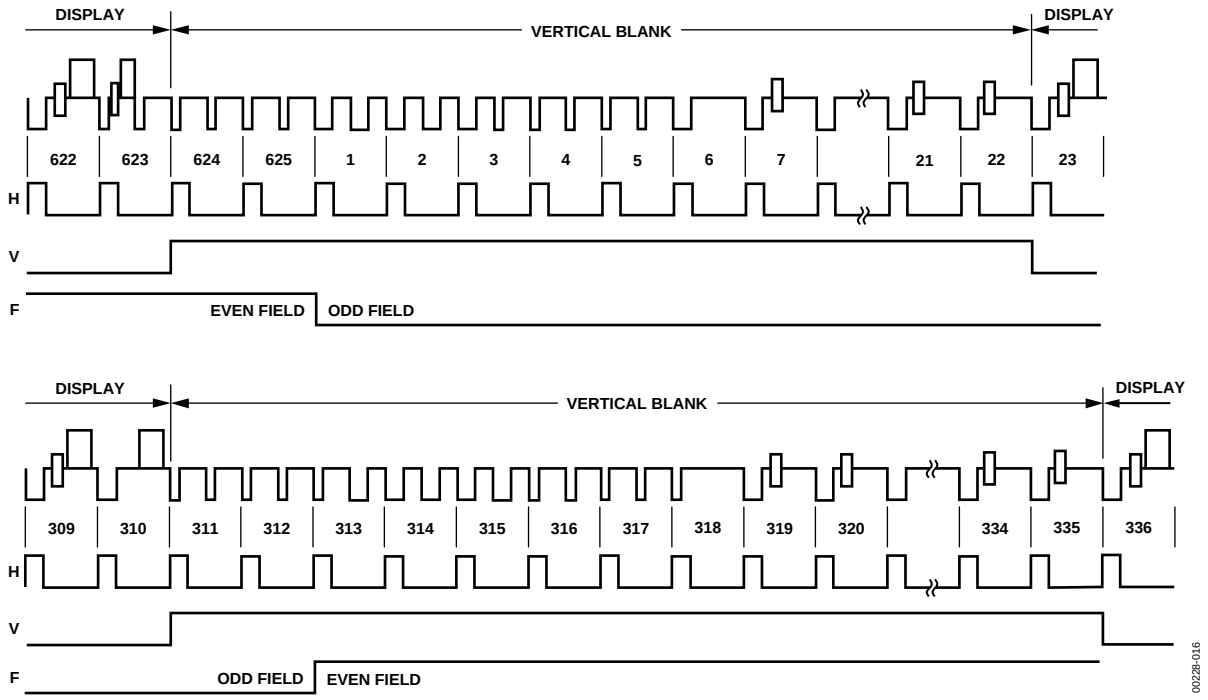


Figure 16. Timing Mode 0 (PAL Master Mode)

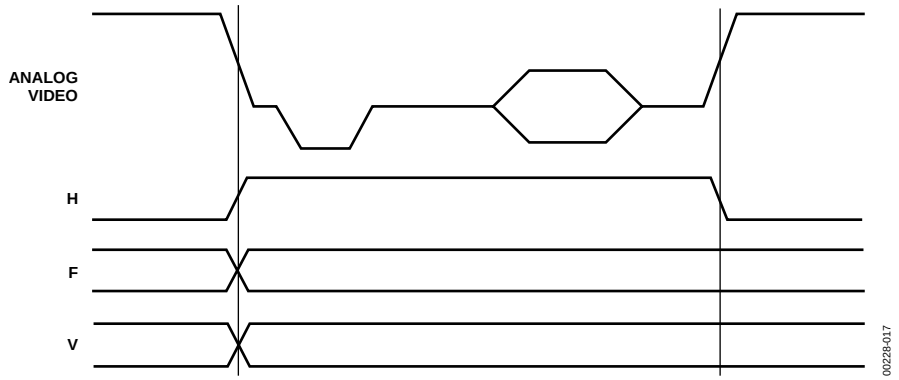


Figure 17. Timing Mode 0 Data Transitions (Master Mode)

Mode 1: Slave Option $\overline{HSYNC}$, $\overline{BLANK}$, FIELD

Timing Register 0 TR0 = X X X X X 0 1 0

In this mode, the ADV7177/ADV7178 accepts horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when HSYNC is low indicates a new frame, that is, vertical retrace. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7177/ADV7178 automatically blank all normally blank lines. Mode 1 is illustrated in Figure 18 (NTSC) and Figure 19 (PAL).

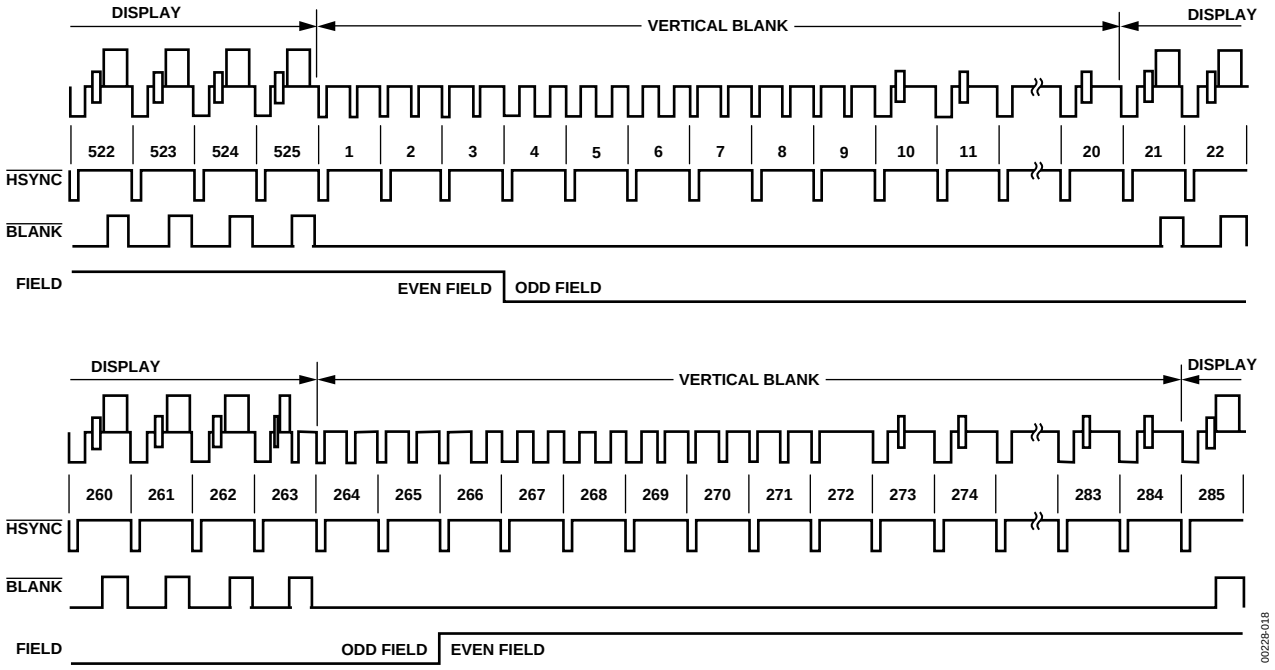


Figure 18. Timing Mode 1 (NTSC)

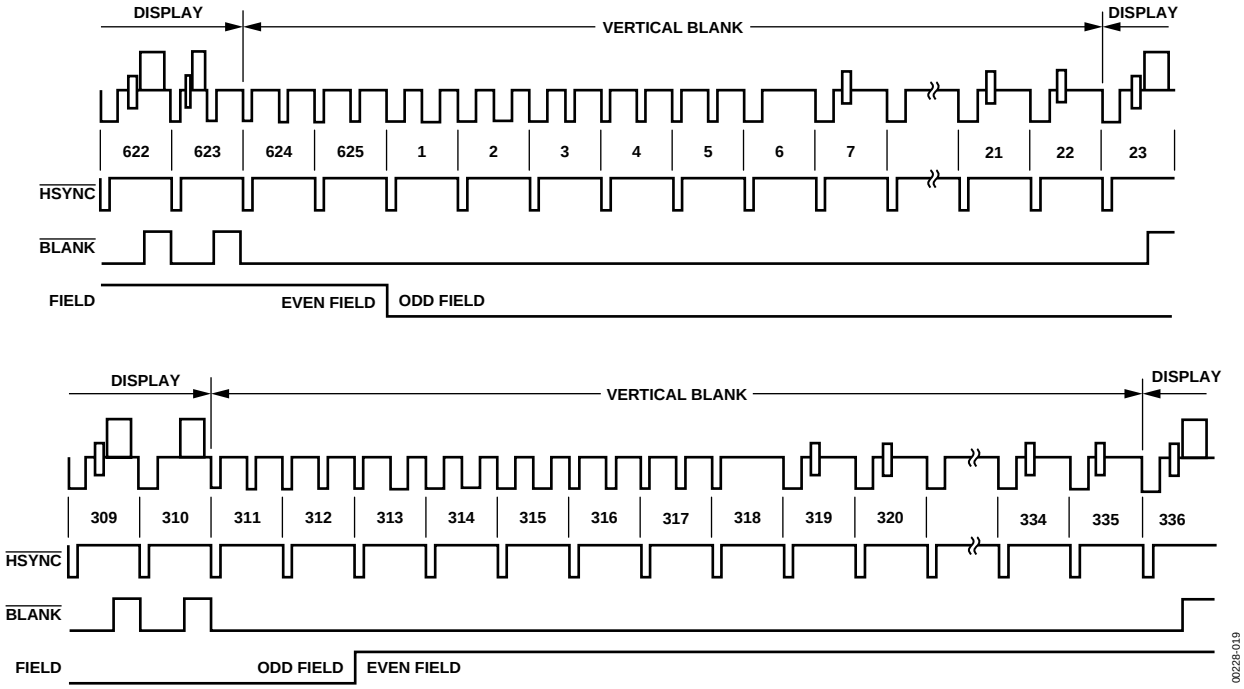


Figure 19. Timing Mode 1 (PAL)

Mode 1: Master Option HSYNC, BLANK, FIELD

Timing Register 0 TR0 = X X X X X 0 1 1

In this mode, the ADV7177/ADV7178 can generate horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when HSYNC is low indicates a new frame, that is, vertical retrace. The BLANK signal is optional. When the BLANK input is disabled, the ADV7177/ADV7178 automatically blank all normally blank lines. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 18 (NTSC) and Figure 19 (PAL). Figure 20 illustrates the HSYNC, BLANK, and FIELD for an odd or even field transition relative to the pixel data.

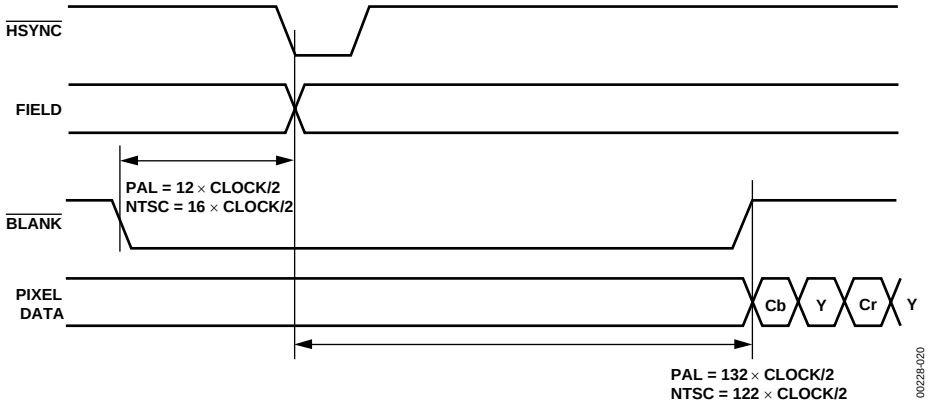


Figure 20. Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2: Slave Option $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{BLANK}$

Timing Register 0 TR0 = X X X X X 1 0 0

In this mode, the ADV7177/ADV7178 accept horizontal and vertical SYNC signals. A coincident low transition of both $\overline{HSYNC}$ and $\overline{VSYNC}$ inputs indicates the start of an odd field. A $\overline{VSYNC}$ low transition when $\overline{HSYNC}$ is high indicates the start of an even field. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7177/ADV7178 automatically blank all normally blank lines as per the BT-470 specification. Mode 2 is illustrated in Figure 21 (NTSC) and Figure 22 (PAL).

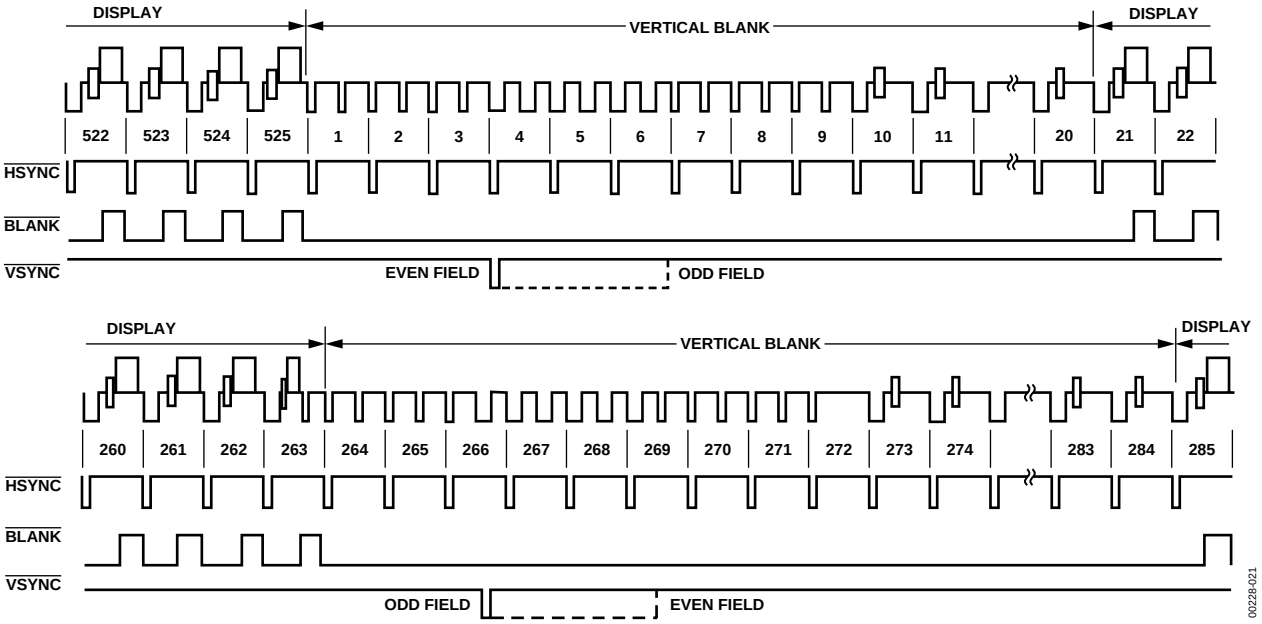


Figure 21. Timing Mode 2 (NTSC)

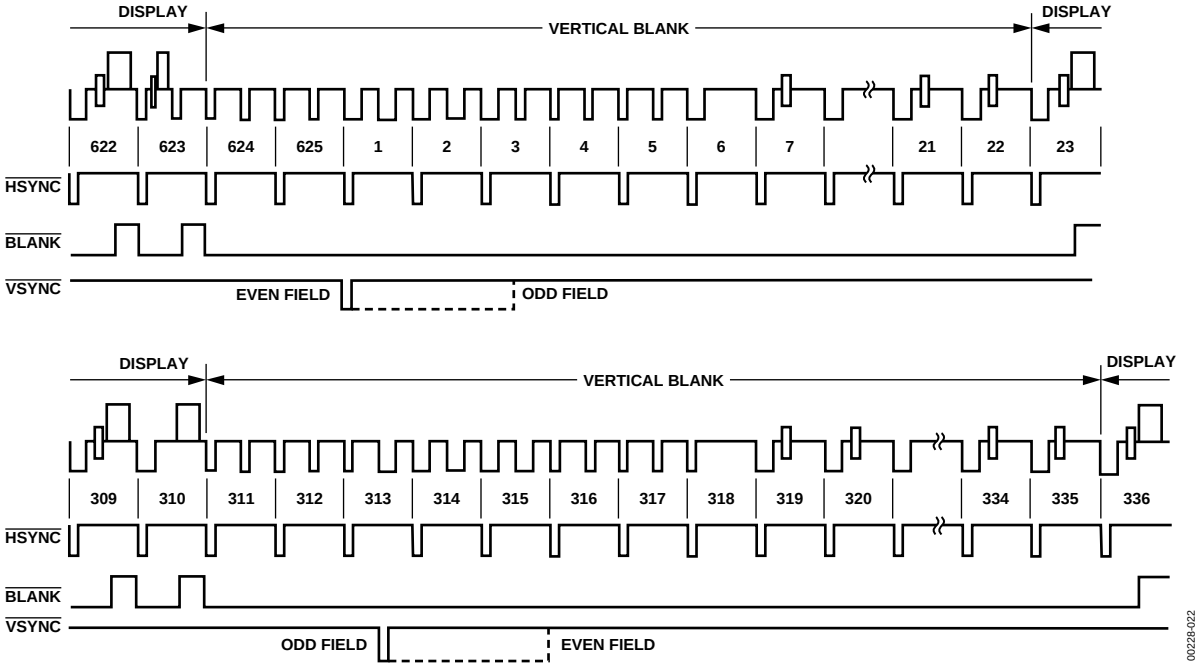


Figure 22. Timing Mode 2 (PAL)

Mode 2: Master Option $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{BLANK}$

Timing Register 0 TR0 = X X X X X 1 0 1

In this mode, the ADV7177/ADV7178 can generate horizontal and vertical SYNC signals. A coincident low transition of both $\overline{HSYNC}$ and $\overline{VSYNC}$ inputs indicates the start of an odd field. A $\overline{VSYNC}$ low transition when $\overline{HSYNC}$ is high indicates the start of an even field. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7177/ADV7178 automatically blank all normally blank lines as per the BT-470 specification. Mode 2 is illustrated in Figure 21 (NTSC) and Figure 22 (PAL). Figure 23 illustrates the $\overline{HSYNC}$, $\overline{BLANK}$, and $\overline{VSYNC}$ for an even-to-odd field transition relative to the pixel data. Figure 24 illustrates the $\overline{HSYNC}$, $\overline{BLANK}$, and $\overline{VSYNC}$ for an odd-to-even field transition relative to the pixel data.

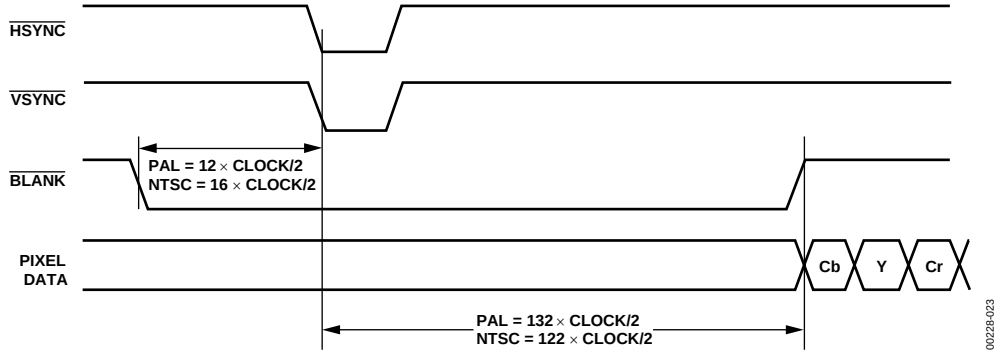


Figure 23. Timing Mode 2, Even-to-Odd Field Transition, Master/Slave

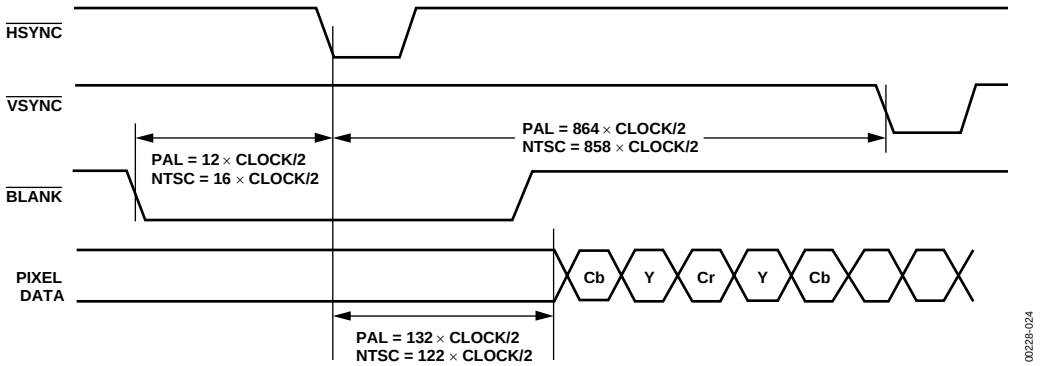


Figure 24. Timing Mode 2, Odd-to-Even Field Transition, Master/Slave

Mode 3: Master/Slave Option $\overline{HSYNC}$, $\overline{BLANK}$, FIELD

Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1

In this mode, the ADV7177/ADV7178 accept or generate horizontal SYNC and odd/even field signals. A transition of the field input when $\overline{HSYNC}$ is high indicates a new frame, that is, vertical retrace. The $\overline{BLANK}$ signal is optional. When the $\overline{BLANK}$ input is disabled, the ADV7177/ADV7178 automatically blank all normally blank lines as per the BT-470 specification. Mode 3 is illustrated in Figure 25 (NTSC) and Figure 26 (PAL).

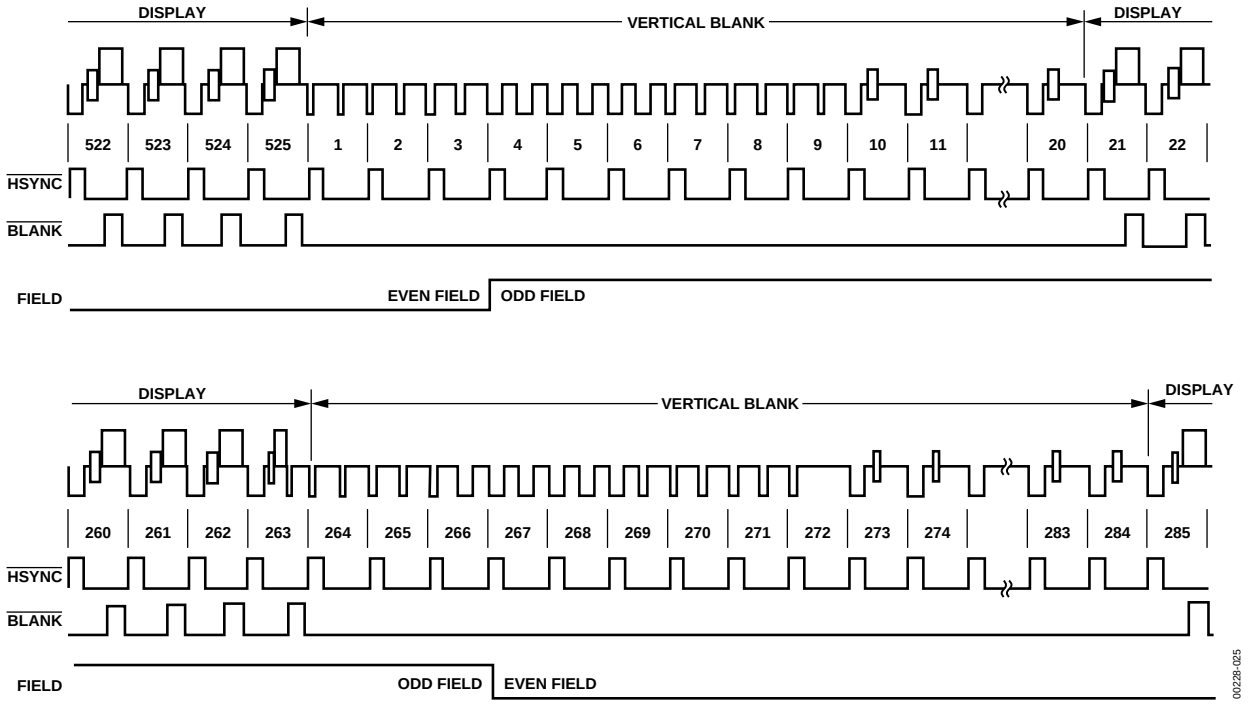


Figure 25. Timing Mode 3 (NTSC)

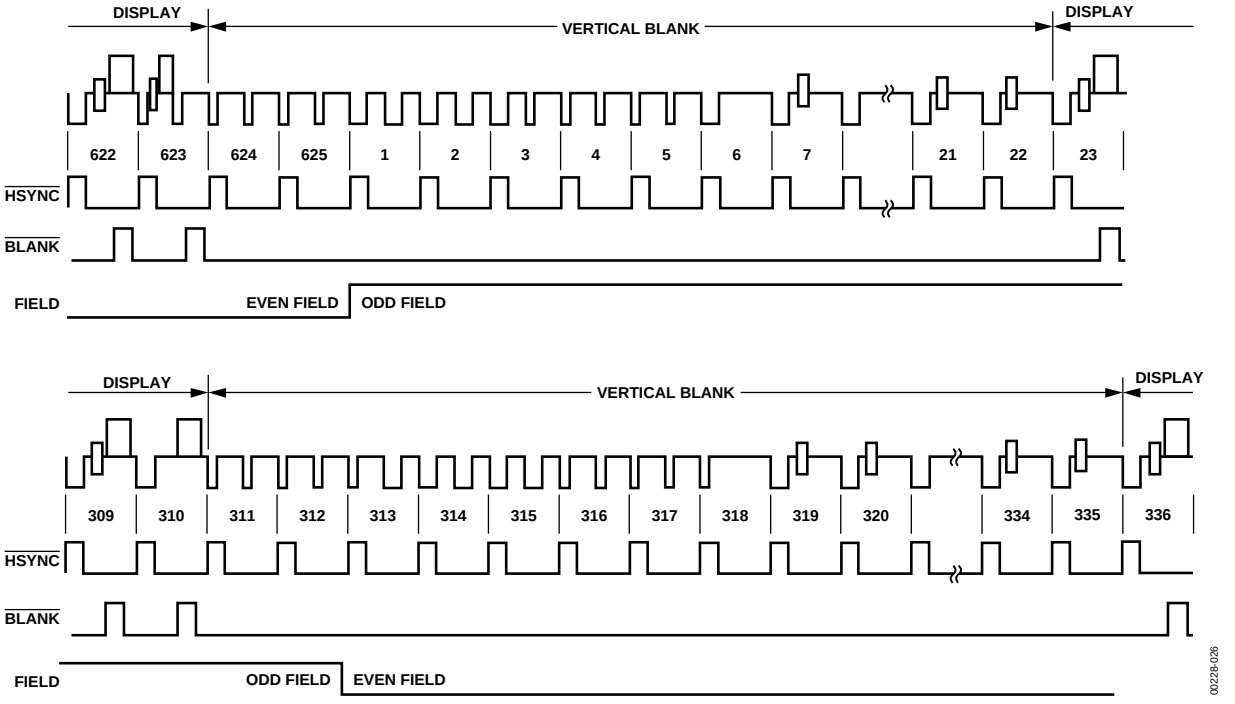


Figure 26. Timing Mode 3 (PAL)

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high-to-low transition on the $\overline{\text{RESET}}$ pin. This initializes the pixel port so that the pixel inputs, P7 to P0, are selected. After reset, the devices are automatically set up to operate in NTSC mode. Subcarrier frequency code 21F07C16HEX is loaded into the subcarrier frequency registers. All other registers, except Mode Register 0, are set to 00HEX. All bits in Mode Register 0 are set to Logic 0 except Bit MR02. Bit MR02 of Mode Register 0 is set to Logic 1. This enables the 7.5 IRE pedestal.

MPU PORT DESCRIPTION

The ADV7178 and ADV7177 support a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. Two inputs, serial data (SDATA) and serial clock (SCLOCK), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7178 and ADV7177 each have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 27 and Figure 28. The LSB sets either a read or write operation. Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7177/ ADV7178 to Logic 0 or Logic 1.

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDATA while SCLOCK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{\text{W}}$ bit). The bits transfer from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the start condition and the correct transmitted address. The R/$\overline{\text{W}}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. A Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7177/ADV7178 act as standard slave devices on the bus. The data on the SDATA pin is 8 bits long, supporting the 7-bit addresses, plus the R/$\overline{\text{W}}$ bit. The ADV7178 has 36 sub-addresses and the ADV7177 has 31 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The auto-increment of the subaddresses allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers, with one exception. The subcarrier frequency registers should be updated in sequence, starting with Subcarrier Frequency Register 0. The auto-increment function should then be used to increment and access Subcarrier Frequency Registers 1, 2 and 3. The subcarrier frequency registers should not be accessed independently.

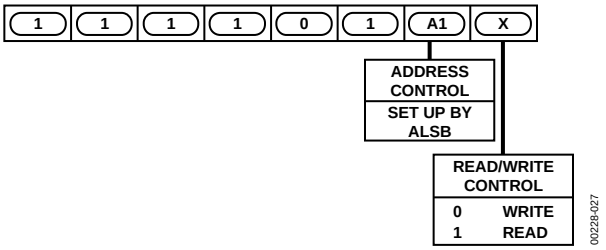


Figure 27. ADV7177 Slave Address

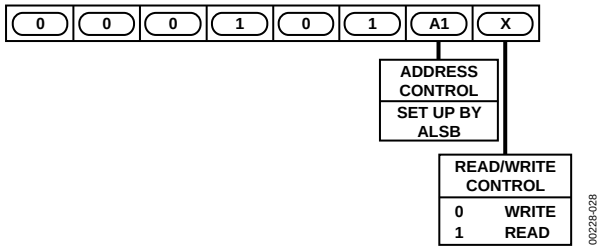


Figure 28. ADV7178 Slave Address

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLOCK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the devices do not issue an acknowledge and return to the idle condition. If, in auto-increment mode, the user exceeds the highest subaddress, the following actions are taken.

In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.

In write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADV7177/ADV7178, and the parts return to the idle condition.

Figure 29 illustrates an example of data transfer for a read sequence and the start and stop conditions. Figure 30 shows bus write and read sequences.

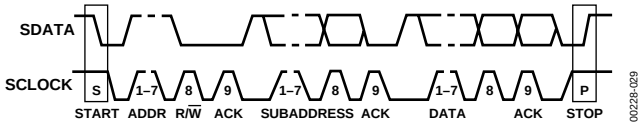


Figure 29. Bus Data Transfer

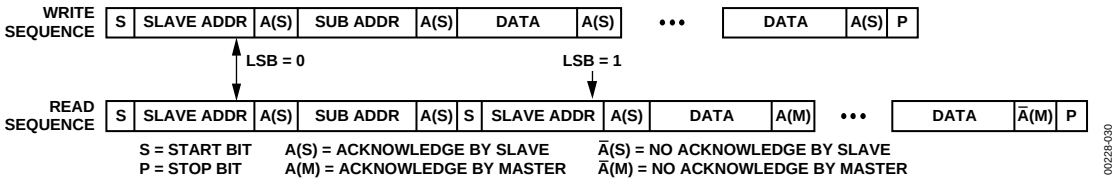


Figure 30. Write and Read Sequences

REGISTERS

REGISTER ACCESS

The MPU can write to or read from all of the ADV7177 and ADV7178 registers except the subaddress register, which is a write-only register. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. A read/write operation is performed from/to the target address, which then increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

This section describes each register, including the subaddress register, mode registers, subcarrier frequency registers, subcarrier phase register, timing registers, closed captioning extended data registers, closed captioning data registers, and the NTSC pedestal control registers in terms of configuration.

Subaddress Register (SR7–SR0)

The communications register is an 8-bit, write-only register. After the parts have been accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to/from which register the operation takes place.

Figure 31 shows the various operations under the control of the subaddress register. Zero should always be written to SR7–SR6.

Register Select (SR5–SR0)

These bits are set up to point to the required starting address.

MODE REGISTER 0 MR0 (MR07–MR00)

Address [SR4–SR0] = 00H

Figure 32 shows the various operations under the control of Mode Register 0. This register can be read from as well as written to.

MR0 BIT DESCRIPTION

Output Video Standard Selection (MR01–MR00)

These bits are used to set up the encode mode. The ADV7177/ADV7178 can be set up to output NTSC, PAL (B, D, G, H, I), and PAL (M) standard video.

Pedestal Control (MR02)

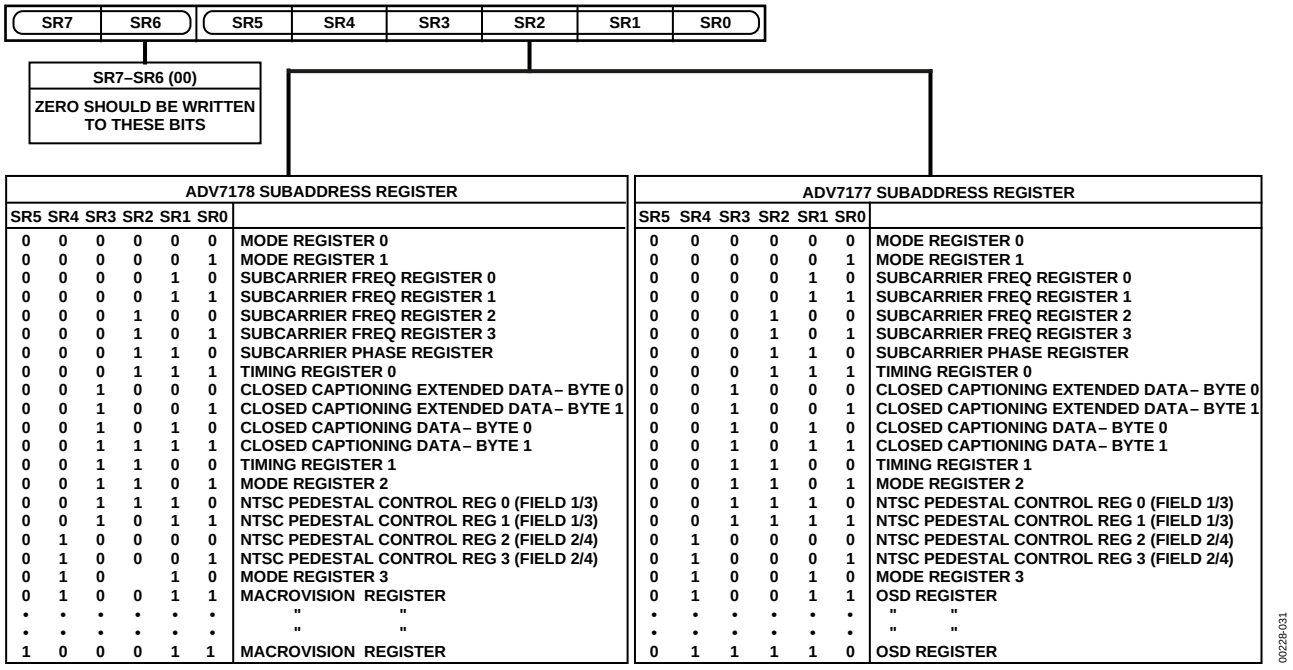
This bit specifies whether a pedestal is to be generated on the NTSC composite video signal. This bit is invalid if the ADV7177/ADV7178 is configured in PAL mode.

Luminance Filter Control (MR04–MR03)

The luminance filters are divided into two sets (NTSC/PAL) of four filters, low-pass A, low-pass B, notch, and extended. When PAL is selected, Bits MR03 and MR04 select one of four PAL luminance filters; likewise, when NTSC is selected, Bits MR03 and MR04 select one of four NTSC luminance filters. The Typical Performance Characteristics section shows the filters.

RGB Sync (MR05)

This bit is used to set up the RGB outputs with the sync information encoded on all RGB outputs.



ADV7178 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	SUBCARRIER FREQ REGISTER 0
0	0	0	0	1	1	SUBCARRIER FREQ REGISTER 1
0	0	0	1	0	0	SUBCARRIER FREQ REGISTER 2
0	0	0	1	0	1	SUBCARRIER FREQ REGISTER 3
0	0	0	1	1	0	SUBCARRIER PHASE REGISTER
0	0	0	1	1	1	TIMING REGISTER 0
0	0	1	0	0	0	CLOSED CAPTIONING EXTENDED DATA– BYTE 0
0	0	1	0	0	1	CLOSED CAPTIONING EXTENDED DATA– BYTE 1
0	0	1	0	1	0	CLOSED CAPTIONING DATA– BYTE 0
0	0	1	1	1	1	CLOSED CAPTIONING DATA– BYTE 1
0	0	1	1	0	0	TIMING REGISTER 1
0	0	1	1	0	1	MODE REGISTER 2
0	0	1	1	1	0	NTSC PEDESTAL CONTROL REG 0 (FIELD 1/3)
0	0	1	0	1	1	NTSC PEDESTAL CONTROL REG 1 (FIELD 1/3)
0	1	0	0	0	0	NTSC PEDESTAL CONTROL REG 2 (FIELD 2/4)
0	1	0	0	0	1	NTSC PEDESTAL CONTROL REG 3 (FIELD 2/4)
0	1	0		1	0	MODE REGISTER 3
0	1	0	0	1	1	MACROVISION REGISTER
•	•	•	•	•	•	" "
•	•	•	•	•	•	" "
1	0	0	0	1	1	MACROVISION REGISTER

ADV7177 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	SUBCARRIER FREQ REGISTER 0
0	0	0	0	1	1	SUBCARRIER FREQ REGISTER 1
0	0	0	1	0	0	SUBCARRIER FREQ REGISTER 2
0	0	0	1	0	1	SUBCARRIER FREQ REGISTER 3
0	0	0	1	1	0	SUBCARRIER PHASE REGISTER
0	0	0	1	1	1	TIMING REGISTER 0
0	0	1	0	0	0	CLOSED CAPTIONING EXTENDED DATA– BYTE 0
0	0	1	0	0	1	CLOSED CAPTIONING EXTENDED DATA– BYTE 1
0	0	1	0	1	0	CLOSED CAPTIONING DATA– BYTE 0
0	0	1	0	1	1	CLOSED CAPTIONING DATA– BYTE 1
0	0	1	1	0	0	TIMING REGISTER 1
0	0	1	1	0	1	MODE REGISTER 2
0	0	1	1	1	0	NTSC PEDESTAL CONTROL REG 0 (FIELD 1/3)
0	0	1	1	1	1	NTSC PEDESTAL CONTROL REG 1 (FIELD 1/3)
0	1	0	0	0	0	NTSC PEDESTAL CONTROL REG 2 (FIELD 2/4)
0	1	0	0	0	1	NTSC PEDESTAL CONTROL REG 3 (FIELD 2/4)
0	1	0	0	1	0	MODE REGISTER 3
0	1	0	0	1	1	OSD REGISTER
•	•	•	•	•	•	" "
•	•	•	•	•	•	" "
0	1	1	1	1	0	OSD REGISTER

Figure 31. Subaddress Register

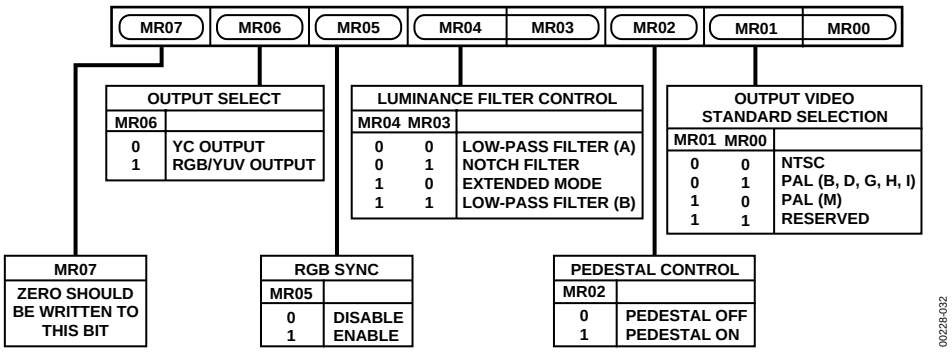


Figure 32. Mode Register 0 (MR0)

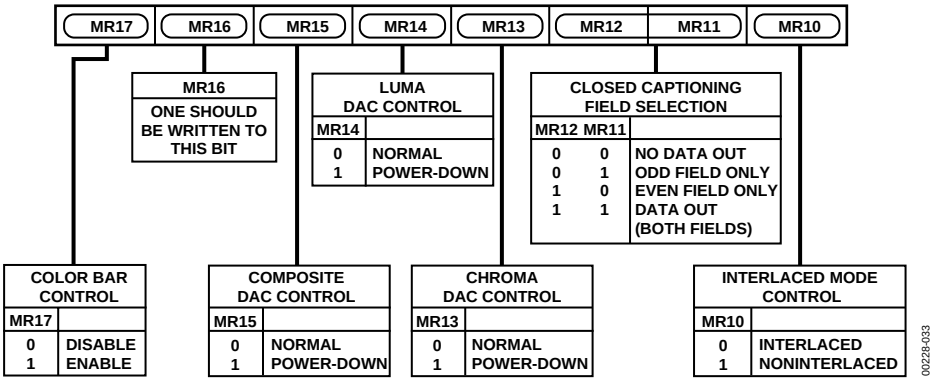


Figure 33. Mode Register 1 (MR1)

Output Select (MR06)

This bit specifies if the part is in composite video or RGB/YUV mode. Note that the main composite signal is still available in RGB/YUV mode.

MODE REGISTER 1 MR1 (MR17–MR10)

Address (SR4–SR0) = 01H

Figure 33 shows the various operations under the control of Mode Register 1. This register can be read from as well as written to.

MR1 BIT DESCRIPTION

Interlaced Mode Control (MR10)

This bit is used to set up the output to interlaced or noninterlaced mode. This mode is relevant only when the part is in composite video mode.

Closed Captioning Field Selection (MR12–MR11)

These bits control the fields on which closed captioning data is displayed; closed captioning information can be displayed on an odd field, even field, or both fields.

DAC Control (MR15–MR13)

These bits can be used to power down the DACs to reduce the power consumption of the ADV7177/ADV7178 if any of the DACs are not required in the application.

Color Bar Control (MR17)

This bit can be used to generate and output an internal color-bar test pattern. The color-bar configuration is 100/7.5/75/7.5 for NTSC and 100/0/75/0 for PAL. Note that when color bars are enabled, the ADV7177/ADV7178 are configured in a master timing mode as per the one selected by bits TR01 and TR02.

SUBCARRIER FREQUENCY REGISTER 3–0

FSC3–FSC0

Address [SR4–SR0] = 05H–02H

These 8-bit-wide registers are used to set up the subcarrier frequency. The value of these registers is calculated by using the following equation, in which the asterisk (*) means rounded to the nearest integer:

$$\frac{No.of\ Subcarrier\ Frequency\ Values\ in\ One\ Line of\ Video\ Line}{No.of\ 27\ MHz\ Clock\ Cycles in One\ Video\ Line} \times 2^{32} *$$

For example, in NTSC mode

$$Subcarrier\ \ Frequency\ Value = \frac{227.5}{1716} \times 2^{32} = 569408542 \quad d = 21F07C1Fh$$

Note that on power-up, FSC Register 0 is set to 16h. A value of 1F as derived above is recommended.

Program as
FSC Register 0: 1Fh
FSC Register 2: 7Ch
FSC Register 3: F0h
FSC Register 4: 21h

Figure 34 shows how the frequency is set up by the four registers.

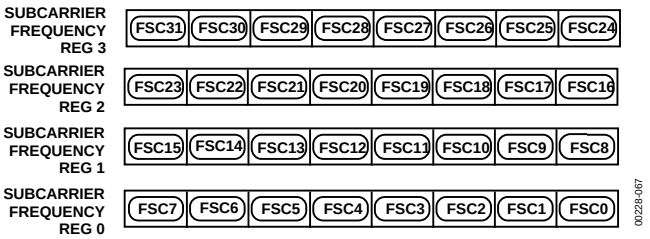


Figure 34. Subcarrier Frequency Register

SUBCARRIER PHASE REGISTER (FP7–FP0)

Address [SR4–SR0] = 06H

This 8-bit-wide register is used to set up the subcarrier phase. Each bit represents 1.41 degrees.

TIMING REGISTER 0 (TR07–TR00)

Address [SR4–SR0] = 07H

Figure 37 shows the various operations under the control of Timing Register 0. This register can be read from as well as written to. This register can be used to adjust the width and position of the master mode timing signals.

TR0 BIT DESCRIPTION

Master/Slave Control (TR00)

This bit controls whether the ADV7177/ADV7178 are in master or slave mode. This register can be used to adjust the width and position of the master timing signals.

Timing Mode Selection (TR02–TR01)

These bits control the timing mode of the ADV7177/ADV7178. These modes are described in the Timing and Control section.

Input Control (TR03)

This bit controls whether the $\overline{\text{BLANK}}$ input is used when the part is in slave mode.

Luma Delay (TR05–TR04)

These bits control the addition of a luminance delay. Each bit represents a delay of 74 ns.

Pixel Port Control (TR06)

This bit is used to set the pixel port to accept 8-bit or 16-bit data. If an 8-bit input is selected, the data is set up on Pins P7–P0.

Timing Register Reset (TR07)

Toggling TR07 from low to high and low again resets the internal timing counters. This bit should be toggled after power-up, reset, or after changing to a new timing mode.

CLOSED CAPTIONING EVEN FIELD DATA REGISTER 1–0 (CED15–CED0)

Address [SR4–SR0] = 09H–08H

These 8-bit-wide registers are used to set up the closed captioning extended data bytes on even fields. Figure 35 shows how the high and low bytes are set up in the registers.

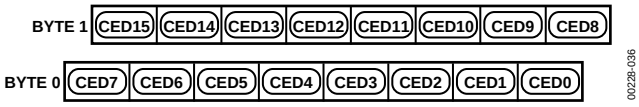


Figure 35. Closed Captioning Extended Data Register

CLOSED CAPTIONING ODD FIELD DATA REGISTER 1–0 (CCD15–CCD0)

Subaddress [SR4–SR0] = 0BH–0AH

These 8-bit-wide registers are used to set up the closed captioning data bytes on odd fields. Figure 36 shows how the high and low bytes are set up in the registers.

Figure 36. Closed Captioning Data Register

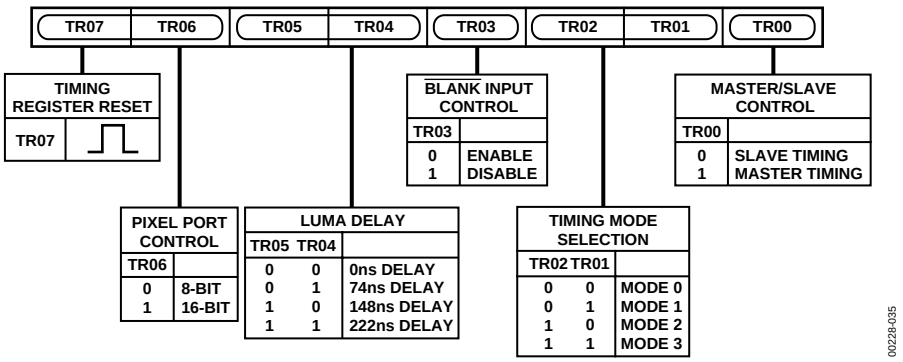


Figure 37. Timing Register 0

TIMING REGISTER 1 (TR17–TR10)

Address [SR4–SR0] = 0CH

Timing Register 1 is an 8-bit-wide register. Figure 38 shows the various operations under the control of Timing Register 1. This register can be read from as well as written to. This register can be used to adjust the width and position of the master mode timing signals.

TR1 BIT DESCRIPTION

$\overline{\text{HSYNC}}$ Width (TR11–TR10)

These bits adjust the $\overline{\text{HSYNC}}$ pulse width.

$\overline{\text{HSYNC}}$ to FIELD/$\overline{\text{VSYNC}}$ Delay (TR13–TR12)

These bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD/$\overline{\text{VSYNC}}$ output.

$\overline{\text{HSYNC}}$ to FIELD Rising Edge Delay (TR15–TR14)

When the device is in Timing Mode 1, these bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD output rising edge.

$\overline{\text{VSYNC}}$ Width (TR15–TR14)

When the ADV7177/ADV7178 are in Timing Mode 2, these bits adjust the $\overline{\text{VSYNC}}$ pulse width.

$\overline{\text{HSYNC}}$ to Pixel Data Adjust (TR17–TR16)

This enables the $\overline{\text{HSYNC}}$ to be adjusted with respect to the pixel data and allows the Cr and Cb components to be swapped. This adjustment is available in both master and slave timing modes.

MODE REGISTER 2 MR2 (MR27–MR20)

Address [SR4-SR0] = 0DH

Mode Register 2 is an 8-bit-wide register. Figure 39 shows the various operations under the control of Mode Register 2. This register can be read from as well as written to.

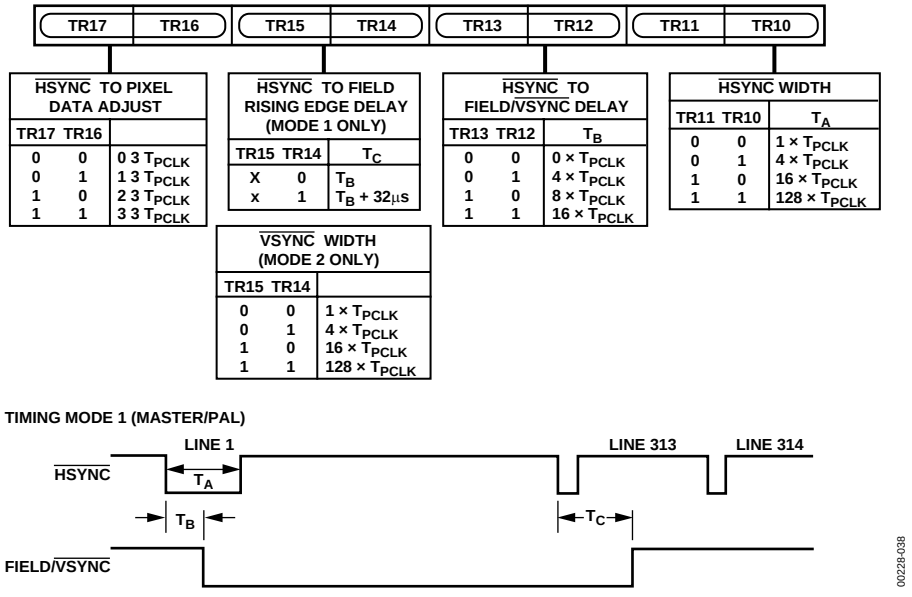


Figure 38. Timing Register 1

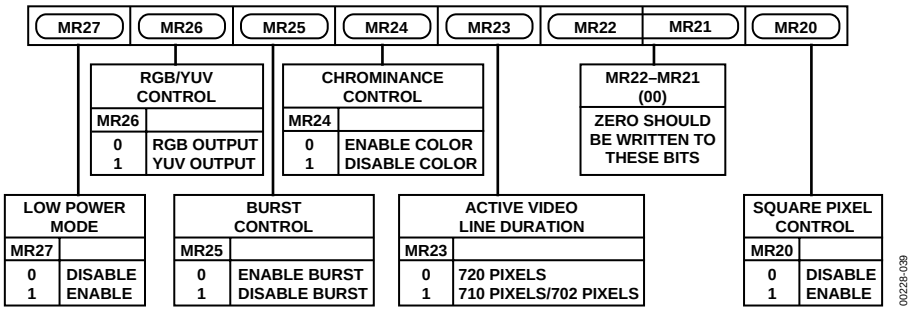


Figure 39. Mode Register 2

MR2 BIT DESCRIPTION

Square Pixel Control (MR20)

This bit is used to set up square pixel mode. This is available in slave mode only. For NTSC, a 24.5454 MHz clock must be supplied. For PAL, a 29.5 MHz clock must be supplied.

Active Video Line Duration (MR23)

This bit switches between two active video line durations. A 0 selects CCIR Rec. 601 (720 pixels PAL/NTSC) and a 1 selects ITU-R.BT470 "analog" standard for active video duration (710 pixels NTSC, 702 pixels PAL).

Chrominance Control (MR24)

This bit enables the color information to be switched on and off the video output.

Burst Control (MR25)

This bit enables the burst information to be switched on and off the video output.

RGB/YUV Control (MR26)

This bit enables the output from the RGB DACs to be set to YUV output video standard. Bit MR06 of Mode Register 0 must be set to Logic 1 before MR26 is set.

Table 12. DAC Output Configuration Matrix

MR06	MR26	DAC A	DAC B	DAC C
0	0	CVBS	Y	C
0	1	CVBS	Y	C
1	0	B	G	R
1	1	U	Y	V

In Table 12,

CVBS: Composite video baseband signal

Y: Luminance component signal, YUV or Y/C mode

C: Chrominance signal, for Y/C mode

U: Chrominance component signal, for YUV mode

V: Chrominance component signal, for YUV mode

R: Red component video, for RGB mode

G: Green component video, for RGB mode

B: Blue component video, for RGB mode

Low Power Control (MR27)

This bit enables the lower power mode of the ADV7177 and the ADV7178. This reduces DAC current by 50%.

NTSC PEDESTAL REGISTERS 3–0 PCE15–0, PCO15–0

(Subaddress [SR4–SR0] = 11–0EH)

These 8-bit-wide registers set up the NTSC pedestal on a line-by-line basis in the vertical blanking interval for both odd and even fields. Figure 40 show the four control registers. A Logic 1 in any of the bits of these registers has the effect of turning the pedestal off on the equivalent line when used in NTSC.

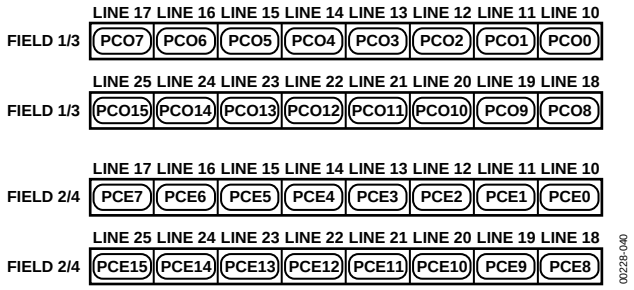


Figure 40. Pedestal Control Registers

MODE REGISTER 3 MR3 (MR37–MR30)

Address [SR4–SR0] = 12H

Mode Register 3 is an 8-bit-wide register. Figure 41shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION

Revision Code (MR30)

This bit is read only and indicates the revision of the device.

VBI_Pass-Through (MR31)

This bit determines whether or not data in the vertical blanking interval (VBI) is output to the analog outputs or blanked. VBI data insertion is not available in Slave Mode 0. Also, if $\overline{\text{BLANK}}$ input control (TR03) is enabled, and VBI_Pass-Through is enabled, TR03 has priority, that is, VBI data insertion does not work.

Clock Output (MR33–MR32)

These bits control the synchronous clock output signal. The clock can be 27 MHz, 13.5 MHz, or disabled, depending on the values of these bit.

OSD Enable (MR35)

A Logic 1 in MR35 enables the OSD function on the ADV7177.

Input Default Color (MR36)

This bit determines the default output color from the DACs for zero input data (or disconnected). A Logic 0 means that the color corresponding to 00000000 is displayed. A Logic 1 forces the output color to black for 00000000 input video data.

Reserved (MR37)

Zero should be written to this bit.

OSD REGISTER 0–11

Address [SR4–SR0] = 13H–1EH

There are 12 OSD registers as shown in Figure 42. There are four bits for each Y, Cb, and Cr value, and there are four zeros added to give the complete byte for each value loaded internally. (Y0 = [$Y0_3$, $Y0_2$, $Y0_1$, $Y0_0$, 0, 0, 0, 0], Cb = [Cb_3, Cb_2, Cb_1, Cb0, 0, 0, 0, 0,], Cr = [Cr_3, Cr_2, Cr_1, Cr_0, 0, 0, 0, 0].)

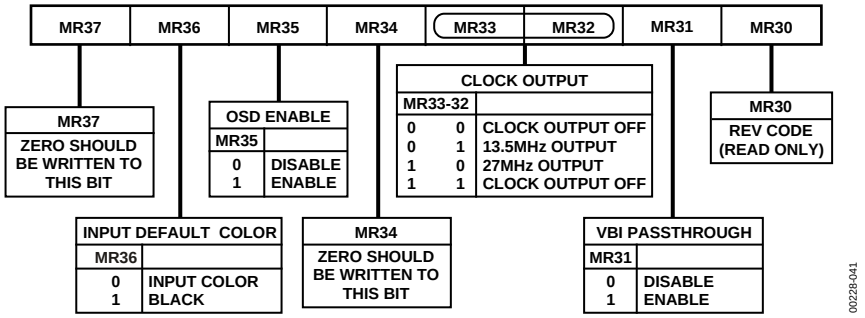


Figure 41. Mode Register 3

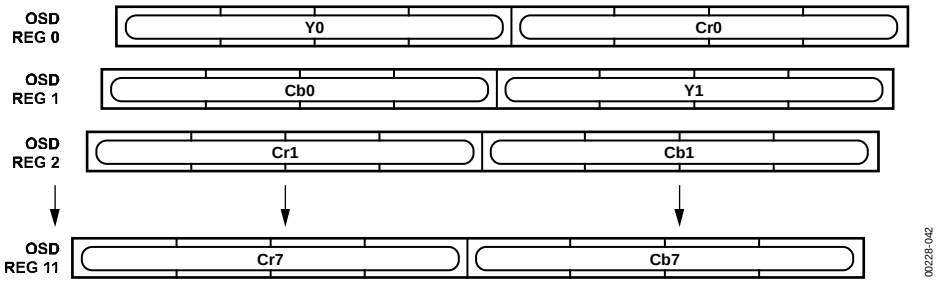


Figure 42. OSD Registers

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7177/ADV7178 are highly integrated circuits containing both precision analog circuitry and high speed digital circuitry. The parts have been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that the same design and layout techniques be applied to the system-level design so that high speed and accurate performance is achieved. Figure 43 shows the analog interface between the device and monitor. The layout should be optimized for lowest noise on the ADV7177/ADV7178 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized to minimize inductive ringing.

GROUND PLANES

The ground plane should encompass all ADV7177/ADV7178 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7177/ADV7178, the analog output traces, and all digital signal traces leading up to the ADV7177/ADV7178. The ground plane is the board's common ground plane.

POWER PLANES

The ADV7177/ADV7178 and any associated analog circuitry should have their own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7177/ADV7178.

The metallization gap separating the device power plane and board power plane should be as narrow as possible to minimize the obstruction to the flow of heat from the device into the general board.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7177/ADV7178 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged so that the plane-to-plane noise is common mode.

SUPPLY DECOUPLING

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 µF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7177/ADV7178 must have at least one 0.1 µF decoupling capacitor to GND. These capacitors should be placed as close to the device as possible. Note that while the ADV7177/ADV7178 contains circuitry to reject power-supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a 3-terminal voltage regulator for supplying power to the analog power plane.

DIGITAL SIGNAL INTERCONNECT

The digital inputs to the ADV7177/ADV7178 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7177/ADV7178 should be avoided to reduce noise pickup. Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}) and not to the analog power plane.

ANALOG SIGNAL INTERCONNECT

The ADV7177/ADV7178 should be located as close to the output connectors as possible to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, not the analog power plane, to maximize the high frequency power-supply rejection. Digital inputs, especially pixel data inputs and clocking signals, should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the outputs should each have a 75 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV7177/ADV7178 to minimize reflections.

The ADV7177/ADV7178 should have no floating inputs. Any inputs that are not required should be tied to ground.

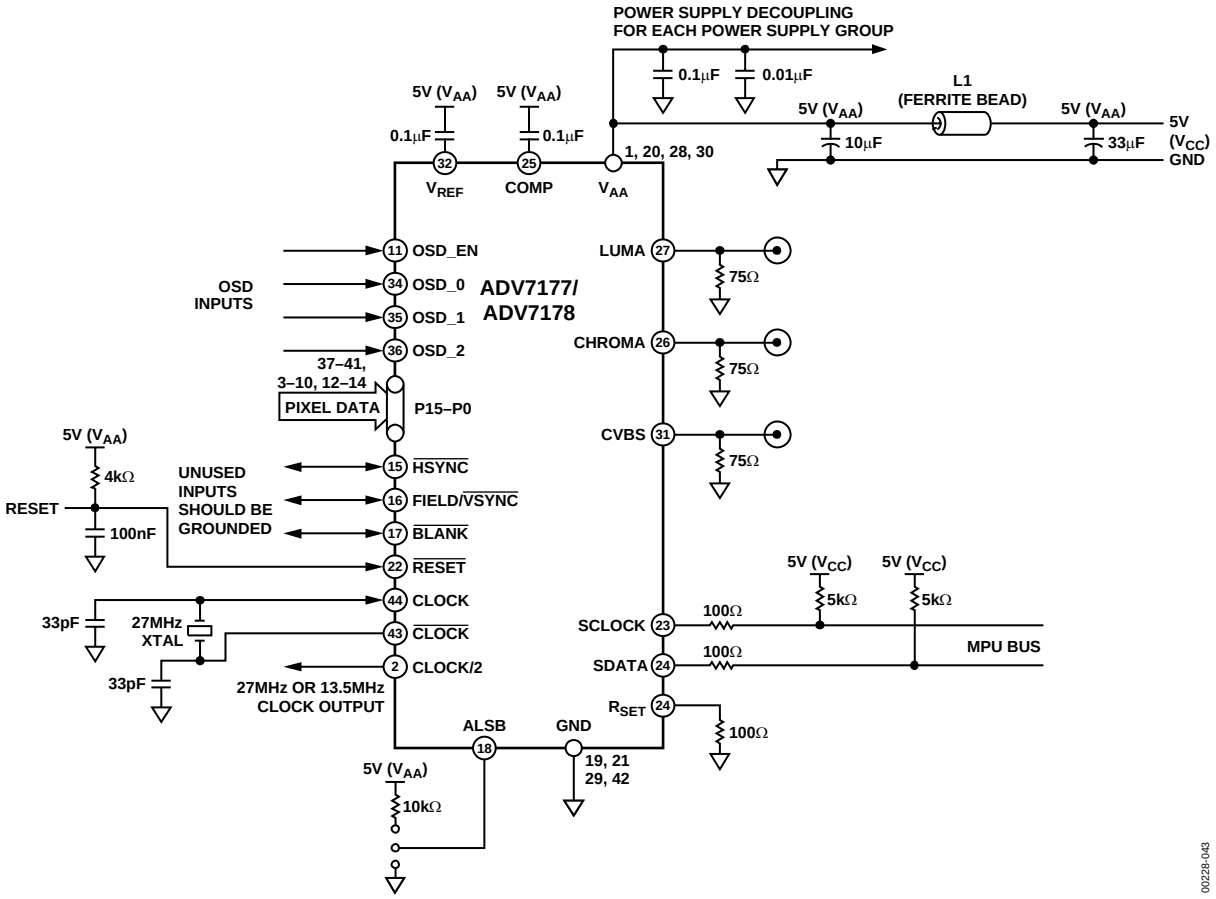


Figure 43. Recommended Analog Circuit Layout

CLOSED CAPTIONING

The ADV7177/ADV7178 support closed captioning, which conforms to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase locked to the caption data. After the clock run-in signal, the blanking level is held for 2 data bits and is followed by a Logic 1 start bit. The start bit is followed by16 bits of data. These consist of two, 8-bit bytes, seven data bits and one odd parity bit. The data for these bytes is stored in closed captioning Data Registers 0 and 1.

The ADV7177/ADV7178 also supports the extended closed captioning operation, which is active during even fields, and is encoded on Scan Line 284. The data for this operation is stored in closed captioning extended Data Registers 0 and 1. All clock run-in signals and timing to support closed captioning on Line 21 and Line 284 are generated automatically by the ADV7177/ ADV7178. All pixels inputs are ignored during Line 21 and Line 284.

FCC Code of Federal Regulations (CFR) 47 Section 15.119 and EIA608 describe the closed captioning information for Line 21 and Line 284.

The ADV7177/ADV7178 uses a single buffering method. This means that the closed captioning buffer is only 1 byte deep, therefore there is no frame delay in outputting the closed captioning data unlike other 2-byte-deep buffering systems. The data must be loaded at least one line before (Line 20 or Line 283) it is outputted on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which in turn loads the new data (2 bytes) every field. If no new data is required for transmission, zeros must be inserted in both data registers; this is called nulling.

It is also important to load control codes, all of which are double bytes on Line 21, or a TV does not recognize them. If you have a message such as "Hello World," which has an odd number of characters, it is important to pad it out to an even number to include the end-of-caption, 2-byte control code in the same field.

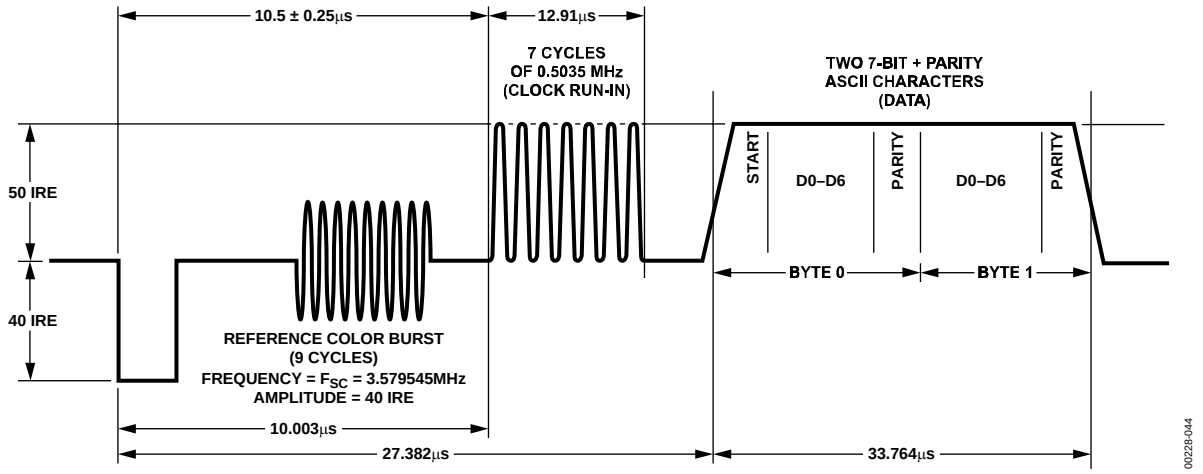


Figure 44. Closed Captioning Waveform (NTSC)

WAVEFORM ILLUSTRATIONS

NTSC WAVEFORMS WITH PEDESTAL

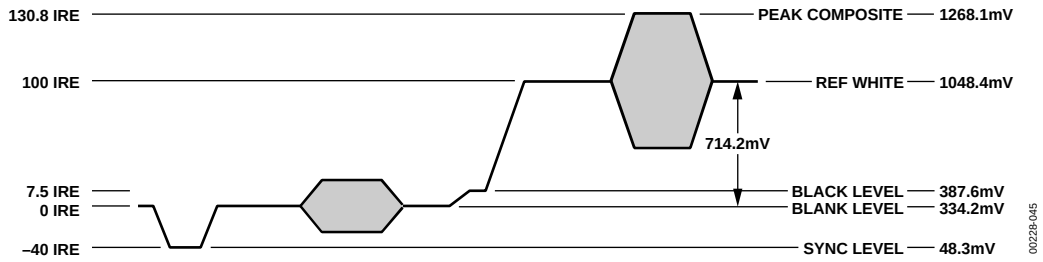


Figure 45. NTSC Composite Video Levels

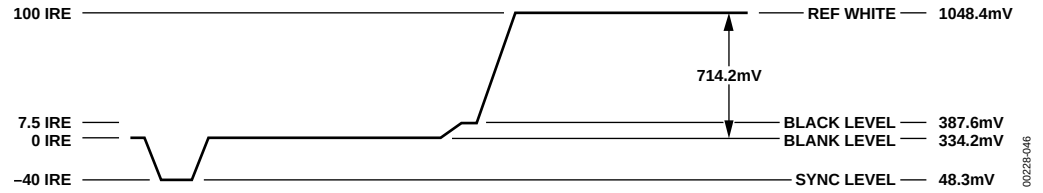


Figure 46. NTSC Luma Video Levels

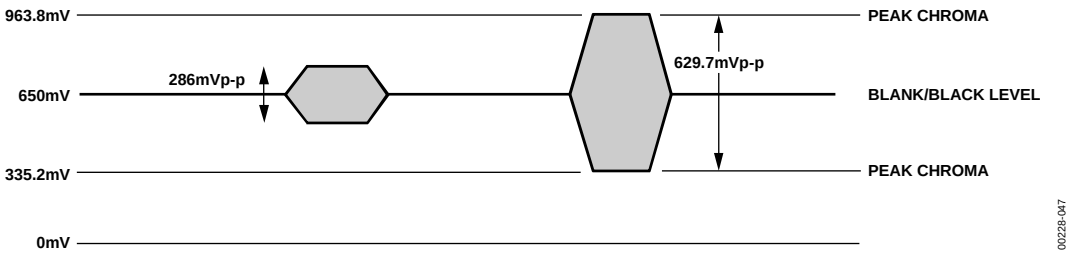


Figure 47. NTSC Chroma Video Levels

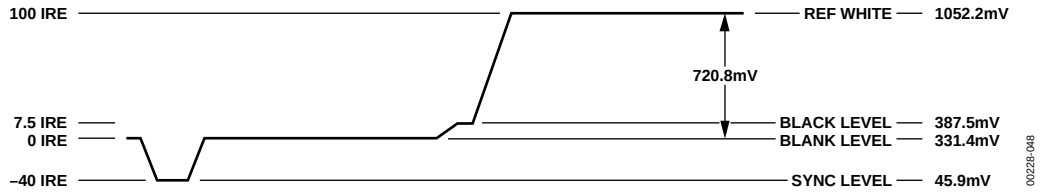


Figure 48. NTSC RGB Video Levels

NTSC WAVEFORMS WITHOUT PEDESTAL

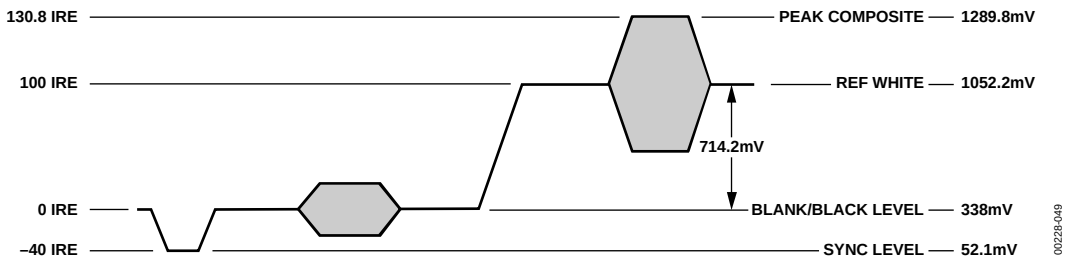


Figure 49. NTSC Composite Video Levels

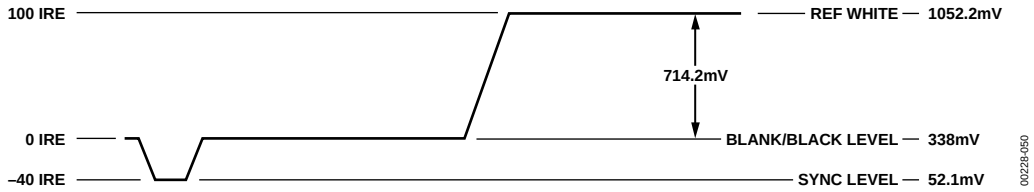


Figure 50. NTSC Luma Video Levels

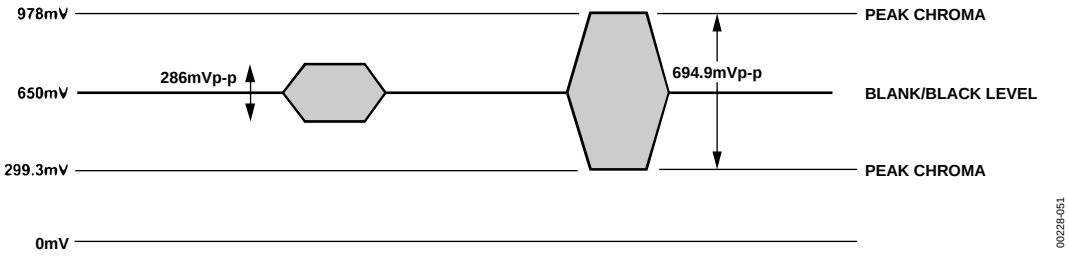


Figure 51. NTSC Chroma Video Levels

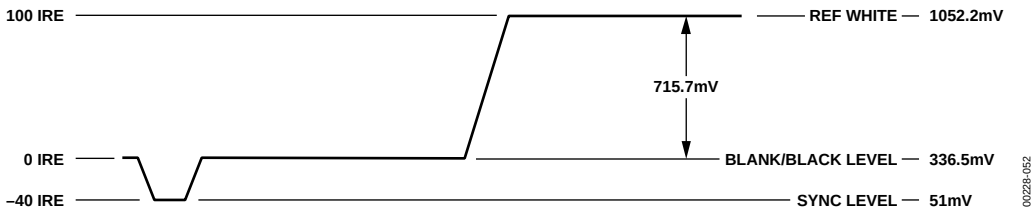


Figure 52. NTSC RGB Video Levels

PAL WAVEFORMS

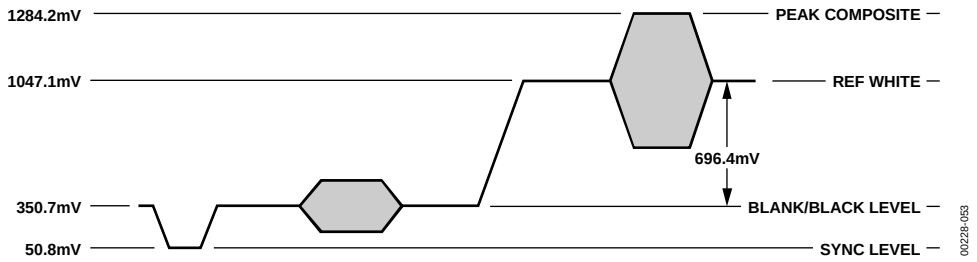


Figure 53. PAL Composite Video Levels

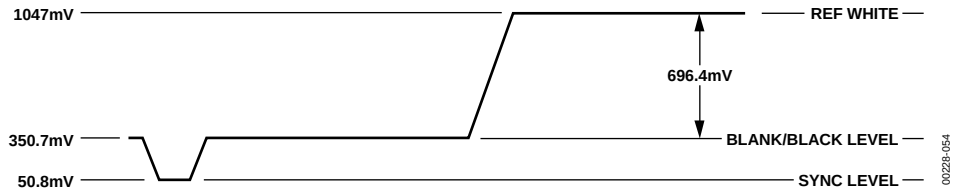


Figure 54. PAL Luma Video Levels

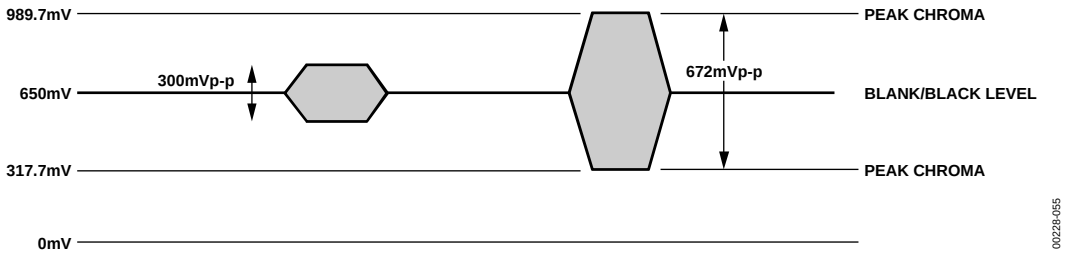


Figure 55. PAL Chroma Video Levels

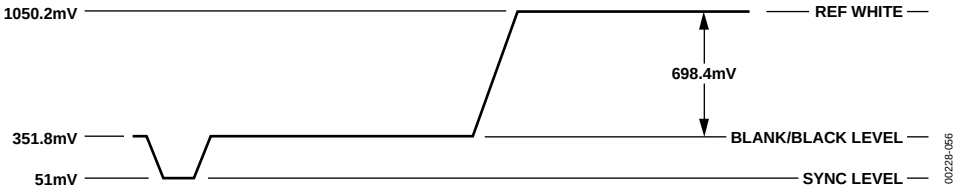


Figure 56. PAL RGB Video Levels

UV WAVEFORMS

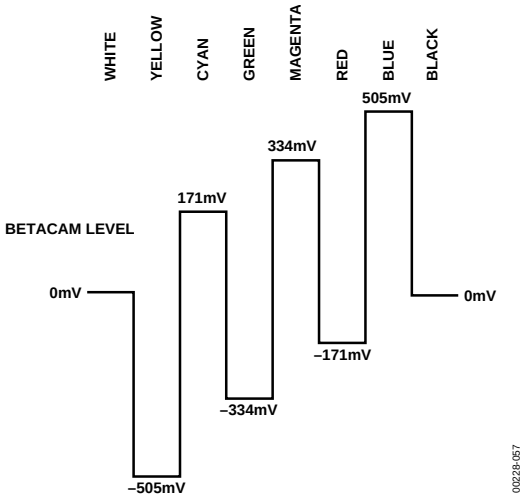


Figure 57. NTSC 100% Color Bars Without Pedestal, U Levels

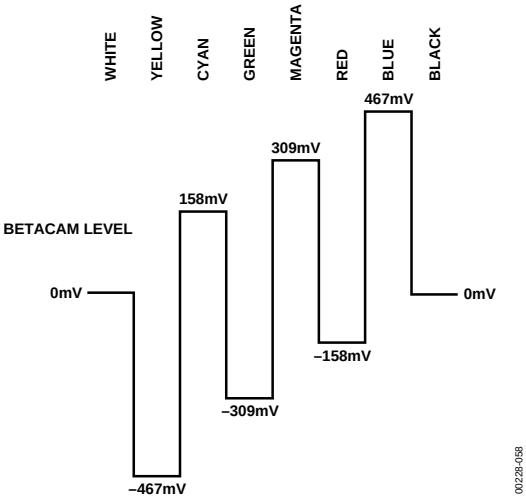


Figure 58. NTSC 100% Color Bars With Pedestal, U Levels

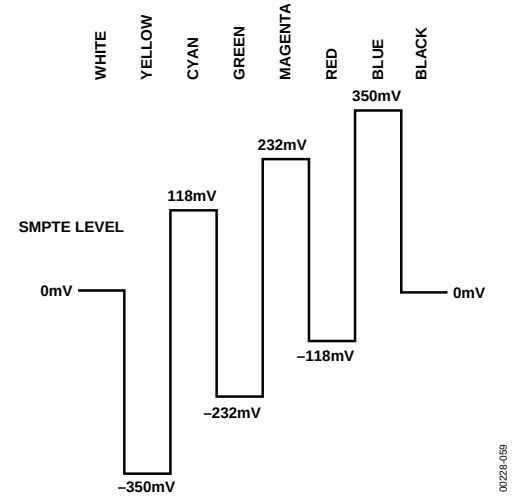


Figure 59. PAL 1005 Color Bars, U Levels

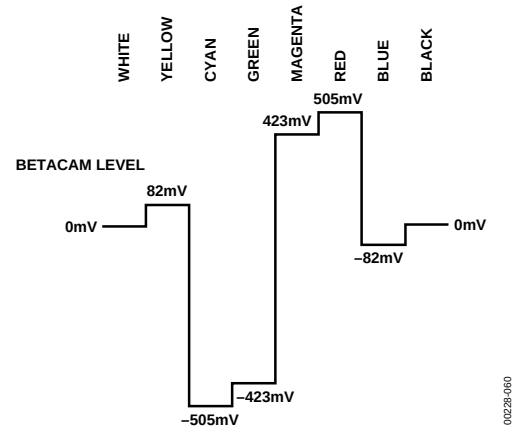


Figure 60. NTSC 100% Color Bars Without Pedestal, V Levels

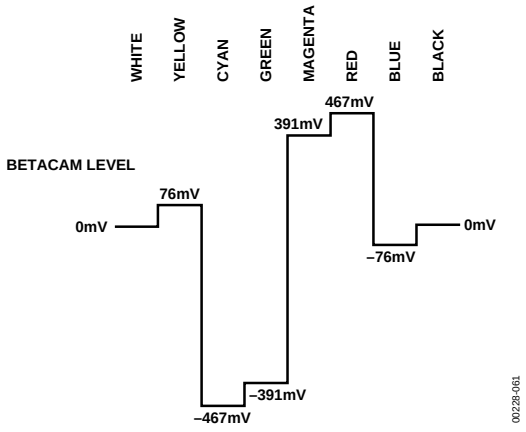


Figure 61. NTSC 100% Color Bars With Pedestal, V Levels

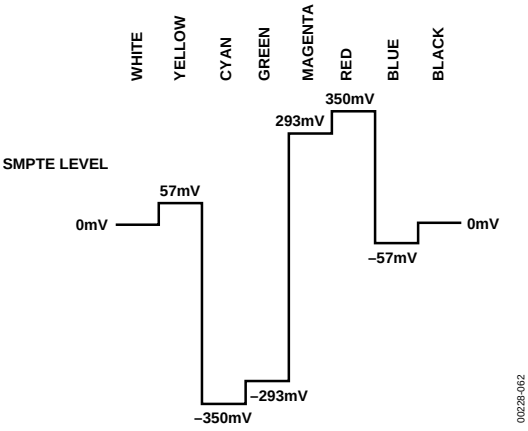


Figure 62. PAL 100% Color Bars, V Levels

REGISTER VALUES

The ADV7177/ADV7178 registers can be set depending on the user standard required.

The following examples give the various register formats for several video standards. In each case the output is set to composite output with all DACs powered up and with the $\overline{\text{BLANK}}$ input control disabled. Also, the burst and color information are enabled on the output and the internal color bar generator is switched off. In the examples shown, the timing mode is set to Mode 0 in slave format. TR02–TR00 of the Timing Register 0 control the timing modes. For a detailed explanation of each bit in the command registers, see the Register Programming section. TR07 should be toggled after setting up a new timing mode. Timing Register 1 provides added control over the position and duration of the timing signals. In the examples, this register is programmed in default mode.

NTSC (FSC = 3.5795454 MHz)

Address Data

Table 13.

Address (Hex)	Register Name	Value (Hex)
00	Mode Register 0	04
01	Mode Register 1	00
02	Subcarrier Frequency Register 0	1F[1]
03	Subcarrier Frequency Register 1	7C
04	Subcarrier Frequency Register 2	F0
05	Subcarrier Frequency Register 3	21
06	Subcarrier Phase Register	00
07	Timing Register 0	08
08	Closed Captioning Register 0	00
09	Closed Captioning Ext. Register 1	00
0A	Closed Captioning Register 0	00
0B	Closed Captioning Register 1	00
0C	Timing Register 1	00
0D	Mode Register 2	80
0E	Pedestal Control Register 0	00
0F	Pedestal Control Register 1	00
10	Pedestal Control Register 2	00
11	Pedestal Control Register 3	00
12	Mode Register 3	00

[1] Fsc0 = 16h on default/power-up. This should be set to 1Fh.

PAL B, D, G, H, I (FSC = 4.43361875 MHz)

Address Data

Table 14.

Address (Hex)	Register Name	Value (Hex)
00	Mode Register 0	01
01	Mode Register 1	00
02	Subcarrier Frequency Register 0	CB
03	Subcarrier Frequency Register 1	8A
04	Subcarrier Frequency Register 2	09
05	Subcarrier Frequency Register 3	2A
06	Subcarrier Phase Register 0	0
07	Timing Register 0	08
08	Closed Captioning Ext. Register 0	00
09	Closed Captioning Ext. Register 1	00
0A	Closed Captioning Register 0	00
0B	Closed Captioning Register 1	00
0C	Timing Register 1	00
0D	Mode Register 2	80
0E	Pedestal Control Register 0	00
0F	Pedestal Control Register 1	00
10	Pedestal Control Register 2	00
11	Pedestal Control Register 3	00
12	Mode Register 3	00

PAL M (FSC = 3.57561149 MHz)

Address Data

Table 15.

Address (Hex)	Register Name	Value (Hex)
00	Mode Register 0	06
01	Mode Register 1	00
02	Subcarrier Frequency Register 0	A3
03	Subcarrier Frequency Register 1	EF
04	Subcarrier Frequency Register 2	E6
05	Subcarrier Frequency Register 3	21
06	Subcarrier Phase Register 0	0
07	Timing Register 0	08
08	Closed Captioning Ext. Register 0	00
09	Closed Captioning Ext. Register 1	00
0A	Closed Captioning Register 0	00
0B	Closed Captioning Register 1	00
0C	Timing Register 1	00
0D	Mode Register 2	80
0E	Pedestal Control Register 0	00
0F	Pedestal Control Register 1	00
10	Pedestal Control Register 2	00
11	Pedestal Control Register 3	00
12	Mode Register 3	00

OPTIONAL OUTPUT FILTER

If an output filter is required for the CVBS, Y, UV, Chroma, and RGB outputs of the ADV7177/ADV7178, the filter in Figure 63 can be used. Plots of the filter characteristics are shown in Figure 64. An output filter is not required if the outputs of the ADV7177/ADV7178 are connected to an analog monitor or an analog TV; however, if the output signals are applied to a system where sampling is used (for example, digital TV), a filter is required to prevent aliasing.

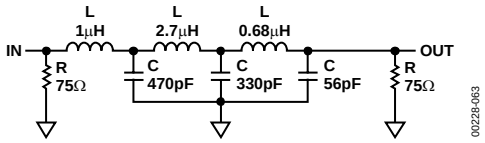


Figure 63. Output Filter

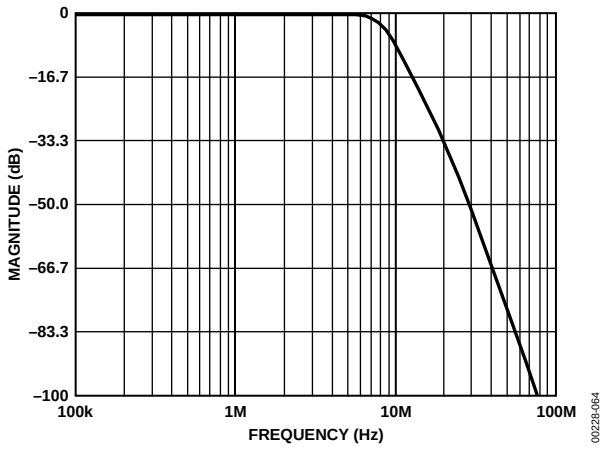


Figure 64. Output Filter Plot

OPTIONAL DAC BUFFERING

For external buffering of the ADV7177/ADV7178 DAC outputs, the configuration in Figure 65 is recommended. This configuration shows the DAC outputs running at half (18 mA) their full-current (34.7 mA) capability. This allows the devices to dissipate less power; the analog current is reduced by 50% with a RSET of 300 Ω and a RLOAD of 75 Ω. This mode is recommended for 3.3 V operation as optimum performance is obtained from the DAC outputs at 18 mA with a V_{AA} of 3.3 V. This buffer also adds extra isolation on the video outputs, as the buffer circuit in Figure 66 shows. When calculating absolute output full current and voltage, use the following equation:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

$$I_{OUT} = \frac{(V_{REF} \times K)}{R_{SET}}$$

where K = 4.2146 constant, V_{REF} = 1.235 V

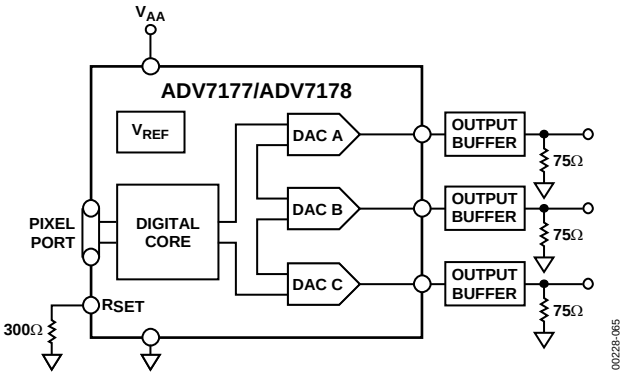


Figure 65. Output DAC Buffering Configuration

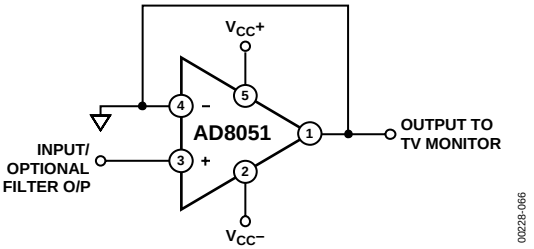


Figure 66. Recommended Output DAC Buffer

OUTLINE DIMENSIONS

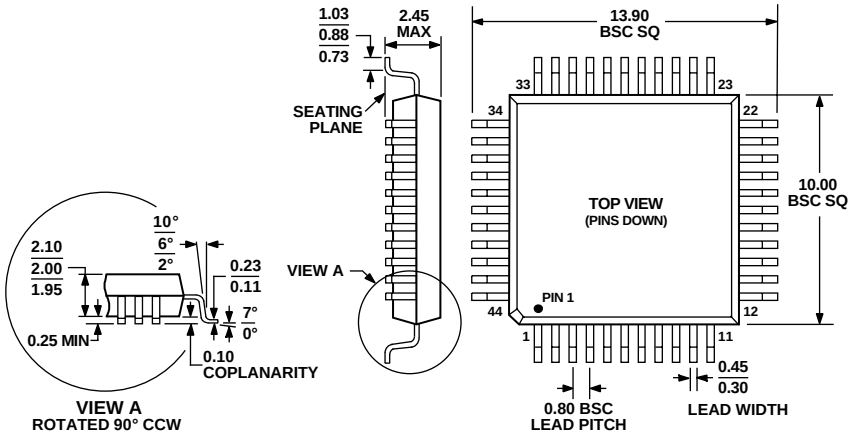


Figure 67. Metric Quad Flat Package [MQFP]
(S-44-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7177KS	0°C to 70°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
ADV7177KS-REEL	0°C to 70°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
ADV7177KSZ[1]	0°C to 70°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
ADV7177KSZ-REEL[1]	0°C to 70°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
ADV7178KS	0°C to 70°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2
ADV7178KS-REEL	0°C to 70°C	44-Lead Metric Quad Flat Package (MQFP)	S-44-2

[1] Z = Pb-free part.

NOTES

C00228–0-3/05(C)