CY7C68000
TX2™ USB 2.0 UTMI Transceiver

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1.0 EZ-USB TX2™ Features

The Cypress EZ-USB TX2™ is a Universal Serial Bus (USB) specification revision 2.0 transceiver, serial/deserializer, to a parallel interface of either 16 bits at 30 MHz or eight bits at 60 MHz. The TX2 provides a high-speed physical layer interface that operates at the maximum allowable USB 2.0 bandwidth. This allows the system designer to keep the complex high-speed analog USB components external to the digital ASIC which decreases development time and associated risk. A standard interface is provided that is USB 2.0-certified and is compliant with Transceiver Macrocell Interface (UTMI) specification version 1.05 dated 3/29/01.

Two packages are defined for the family: 56-pin SSOP and 48-pin FBGA.

The function block diagram is shown in *Figure 1-1*.

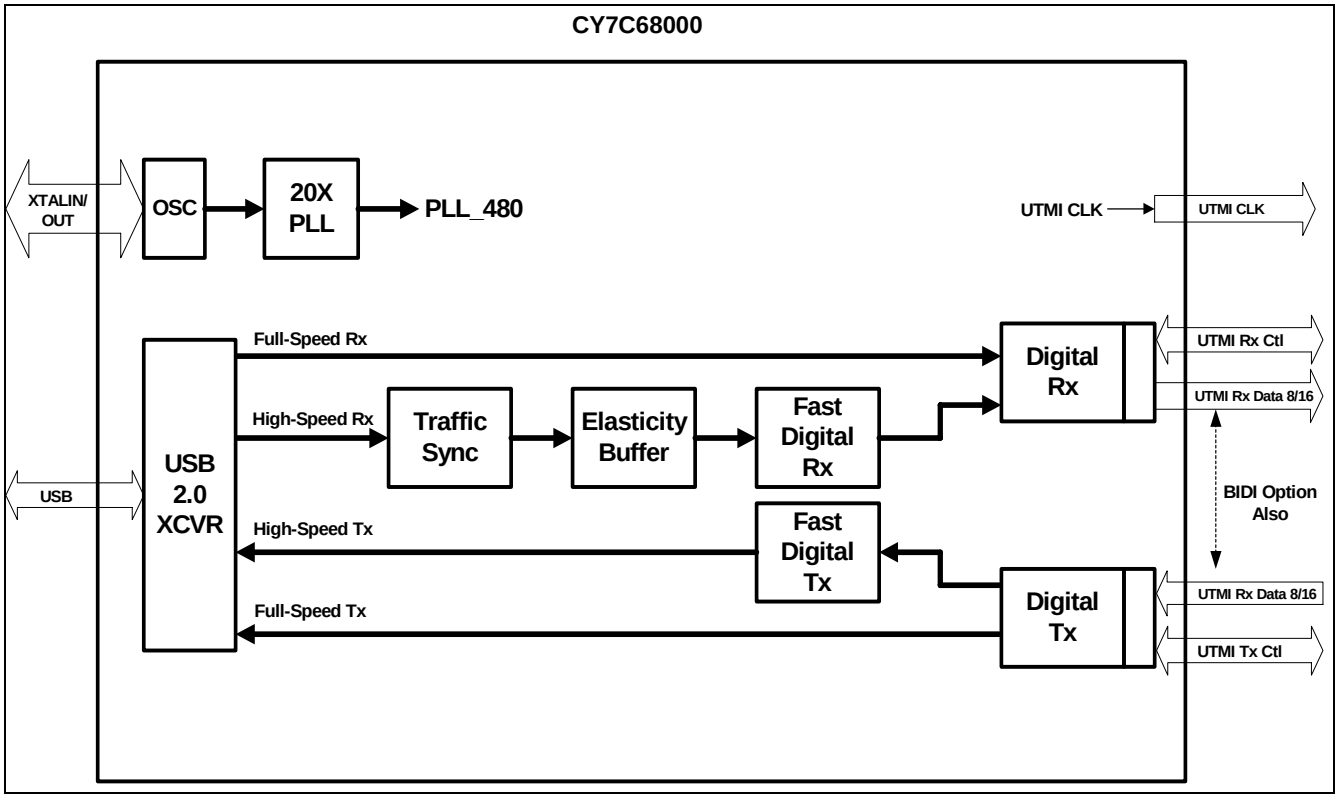

Figure 1-1. Block Diagram

- **UTMI-compliant/USB-2.0-certified**
- **Operates in both USB 2.0 high speed (HS), 480 Mbits/second, and full speed (FS), 12 Mbits/second**
- **Serial-to-parallel and parallel-to-serial conversions**
- **8-bit unidirectional, 8-bit bidirectional, or 16-bit bidirectional external data interface**
- **Synchronous field and EOP detection on receive packets**
- **Synchronous field and EOP generation on transmit packets**
- **Data and clock recovery from the USB serial stream**
- **Bit stuffing/unstuffing; bit stuff error detection**
- **Staging register to manage data rate variation due to bit stuffing/unstuffing**
- **16-bit 30-MHz, and 8-bit 60-MHz parallel interface**
- **Ability to switch between FS and HS terminations and signaling**
- **Supports detection of USB reset, suspend, and resume**
- **Supports HS identification and detection as defined by the USB 2.0 Specification**
- **Supports transmission of resume signaling**
- **3.3V operation**
- **Two package options—48-pin FBGA, and 56-pin SSOP**
- **All required terminations, including 1.5-K ohm pull-up on DPLUS, are internal to chip**
- **Supports USB 2.0 test modes**.

2.0 Applications

- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Cameras
- Scanners
- Home PNA
- Wireless LAN
- MP3 players
- Networking.

3.0 Functional Overview

3.1 USB Signaling Speed

TX2 operates at two of the rates defined in the USB Specification 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps.

TX2 does not support the low-speed (LS) signaling rate of 1.5 Mbps.

3.2 Transceiver Clock Frequency

TX2 has an on-chip oscillator circuit that uses an external 24-MHz (±100-ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500-µW drive level
- 27–33 pF (5% tolerance) load capacitors.

An on-chip phase-locked loop (PLL) multiplies the 24-MHz oscillator up to 30/60 MHz, as required by the transceiver parallel data bus. The default UTMI interface clock (CLK) frequency is determined by the DataBus16_8 pin.

3.3 Buses

The two packages allow for either 8- or 8/16-bit bidirectional data bus for data transfers to a controlling unit.

The 48-pin package allows only 8-bit transfers while the 56-pin package adds an additional eight bits to allow for a selection of 8- or 16-bit transfers.

3.4 Reset Pin

An input pin (Reset) resets the chip. This pin has hysteresis and is active HIGH according to the UTMI specification. The internal PLL stabilizes approximately 200 µs after V_{CC} has reached 3.3V.

3.5 Line State

The Line State output pins LineState[1:0] are driven by combinational logic and may be toggling between the “J” and the “K” states. They are synchronized to the CLK signal for a valid signal. On the CLK edge the state of these lines reflect the state of the USB data lines. Upon the clock edge the 0-bit of the LineState pins is the state of the DPLUS line and the one bit of LineState is the DMINUS line. When synchronized, the set-up and hold timing of the LineState is identical to the parallel data bus.

3.6 Full-speed vs. High-speed Select

The FS vs. HS is done through the use of both XcvrSelect and the TermSelect input signals. The TermSelect signal enables the 1.5 K ohm pull-up on to the DPLUS pin. When TermSelect is driven LOW, a SE0 is asserted on the USB providing the HS termination and generating the HS Idle state on the bus. The XcvrSelect signal is the control which selects either the FS transceivers or the HS transceivers. By setting this pin to a “0” the HS transceivers are selected and by setting this bit to a “1” the FS transceivers are selected.

3.7 Operational Modes

The operational modes are controlled by the OpMode signals. The **OpMode** signals are capable of inhibiting normal operation of the transceiver and evoking special test modes. These modes take effect immediately and take precedence over any pending data operations. The transmission data rate when in **OpMode** depends on the state of the **XcvrSelect** input.

OpMode[1:0]	Mode	Description
00	0	Normal operation
01	1	Non-driving
10	2	Disable Bit Stuffing and NRZI encoding
11	3	Reserved

Mode 0 allows the transceiver to operate with normal USB data decoding and encoding.

Mode 1 allows the transceiver logic to support a soft disconnect feature which three-states both the HS and FS transmitters, and removes any termination from the USB, making it appear to an upstream port that the device has been disconnected from the bus.

Mode 2 disables Bit Stuff and NRZI encoding logic so 1s loaded from the data bus becomes Js on the **DPLUS**/**DMINUS** lines and 0s become Ks.

4.0 DPLUS/DMINUS Impedance Termination

The CY7C68000 does not require external resistors for USB data line impedance termination or an external pull up resistor on the DPLUS line. These resistors are incorporated into the part. They are factory trimmed to meet the requirements of USB 2.0. Incorporating these resistors also reduces the pin count on the part.

5.0 Pin Assignments

The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 48- and 56-pin packages.

The 48-pin package is the lowest-cost version and provides an 8-bit, 60-MHz interface.

The 56-pin package is the full version, offering an 8-bit (60-MHz) or 16-bit (30-MHz) bus interface. The two signals required for 16-bit operation are ValidH and DataBus16_8, and are present only in the 56-pin version.

48-pin FBGA

A1	A2	A3	A4	A5	A6
AGND	**DMINUS**	**DPLUS**	**Reserved**	**XTALOUT**	**XTALIN**
B1	B2	B3	B4	B5	B6
AGND	**GND**	**Reserved**	**GND**	**V_{CC}**	**AV_{CC}**
C1	C2	C3	C4	C5	C6
CLK	**GND**	**V_{CC}**	**V_{CC}**	**V_{CC}**	**AV_{CC}**
D1	D2	D3	D4	D5	D6
GND	**GND**	**V_{CC}**	**NC**	**RESET**	**TXVALID**
E1	E2	E3	E4	E5	E6
RXVALID	**RXACTIVE**	**TERMSELECT**	**XCVRSELECT**	**SUSPEND**	**TXREADY**
F1	F2	F3	F4	F5	F6
OPMODE1	**Reserved**	**OPMODE0**	**Reserved**	**Reserved**	**Reserved**
G1	G2	G3	G4	G5	G6
LINESTATE1	**Reserved**	**D7**	**D5**	**D3**	**D1**
H1	H2	H3	H4	H5	H6
LINESTATE0	**RXERROR**	**D6**	**D4**	**D2**	**D0**

Figure 5-1. CY7C68000 48-pin FBGA Pin Assignment

56-pin SSOP

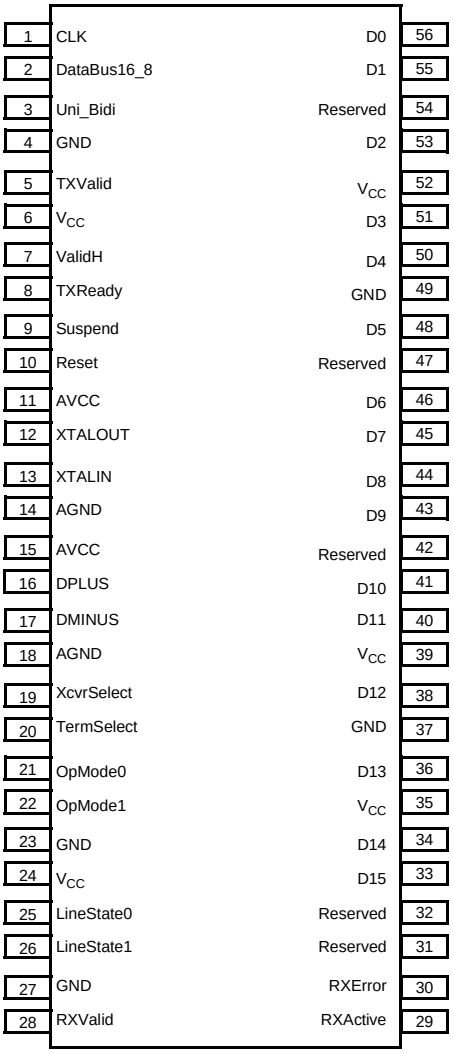

Figure 5-2. CY7C68000 56-pin SSOP Pin Assignment

5.1 CY7C68000 Pin Descriptions

Table 5-1. Pin Descriptions [1]

56	48	Name	Type	Default	Description
11	B6	AVCC	Power	N/A	**Analog V_{CC}**. This signal provides power to the analog section of the chip.
15	C6	AVCC	Power	N/A	**Analog V_{CC}**. This signal provides power to the analog section of the chip.
14	A1	AGND	Power	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
18	B1	AGND	Power	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
16	A3	DPLUS	I/O/Z	Z	**USB DPLUS Signal**. Connect to the USB DPLUS signal.
17	A2	DMINUS	I/O/Z	Z	**USB DMINUS Signal**. Connect to the USB DMINUS signal.

Note:
1. Unused inputs should not be left floating. Tie either HIGH or LOW as appropriate. Outputs that are three-statable should only be pulled up or down to ensure signals at power-up and in standby.

Table 5-1. Pin Descriptions (continued)[1]

56	48	Name	Type	Default	Description
56	H6	D0	I/O		**Bidirectional Data Bus**. This bidirectional bus is used as the entire data bus in the 8-bit mode or the least significant eight bits in the 16-bit mode.
55	G6	D1	I/O		
53	H5	D2	I/O		
51	G5	D3	I/O		
50	H4	D4	I/O		
48	G4	D5	I/O		
46	H3	D6	I/O		
45	G3	D7	I/O		
44	–	D8	I/O		**Bidirectional Data Bus**. This bidirectional bus is used as the upper eight bits of the data bus when in the 16-bit mode, and not used when in the 8-bit mode. (56-pin only)
43	–	D9	I/O		
41	–	D10	I/O		
40	–	D11	I/O		
38	–	D12	I/O		
36	–	D13	I/O		
34	–	D14	I/O		
33	–	D15	I/O		
1	C1	CLK	Output		**Clock**. This output is used for clocking the receive and transmit parallel data on the D[15:0] bus.
10	D5	Reset	Input	N/A	**Active HIGH Reset**. Resets the entire chip. This pin is normally tied to V_{CC} through a 0.1-µF capacitor and to GND through a 100K resistor for a 10 msec RC time constant.
19	E4	XcvrSelect	Input	N/A	**Transceiver Select**. This signal selects between the Full Speed (FS) and the High Speed (HS) transceivers: 0: HS transceiver enabled 1: FS transceiver enabled
20	E3	TermSelect	Input	N/A	**Termination Select**. This signal selects between the between the Full Speed (FS) and the High Speed (HS) terminations: 0: HS termination 1: FS termination
9	E5	Suspend	Input	N/A	**Suspend**. Places the CY7C68000 in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operations. While suspended, **TermSelect** must always be in FS mode to ensure that the 1.5 K ohm pull-up on DPLUS remains powered. 0: CY7C68000 circuitry drawing suspend current 1: CY7C68000 circuitry drawing normal current
26	G1	LineState1	Output		**Line State**. These signals reflect the current state of the single-ended receivers. They are combinatorial until a “usable” CLK is available then they are synchronized to CLK. They directly reflect the current state of the DPLUS (LineState0) and DMINUS (LineState1). D- D+ Description 0 0 0: SE0 0 1 1: ‘J’ State 1 0 2: ‘K’ State 1 1 3: SE1

Table 5-1. Pin Descriptions (continued)[1]

56	48	Name	Type	Default	Description
25	H1	LineState0	Output		**Line State**. These signals reflect the current state of the single-ended receivers. They are combinatorial until a “usable” CLK is available then they are synchronized to CLK. They directly reflect the current state of the DPLUS (LineState0) and DMINUS (LineState1). D- D+ Description 00–0: SE0 01–1: ‘J’ State 10–2: ‘K’ State 11–3: SE1.
22	F1	OpMode1	Input		**Operational Mode**. These signals select among various operational modes: 10 Description 00–0: Normal Operation 01–1: Non-driving 10–2: Disable Bit Stuffing and NRZI encoding 11–3: Reserved.
21	F3	OpMode0	Input		**Operational Mode.** These signals select among various operational modes: 10 Description 00–0: Normal Operation 01–1: Non-driving 10–2: Disable Bit Stuffing and NRZI encoding 11–3: Reserved.
5	D6	TXValid	Input		**Transmit Valid**. Indicates that the data bus is valid. The assertion of Transmit Valid initiates SYNC on the USB. The negation of Transmit Valid initiates EOP on the USB. The start of SYNC must be initiated on the USB no less than one or no more that two CLKs after the assertion of TXValid. In HS (XcvrSelect = 0) mode, the SYNC pattern must be asserted on the USB between 8- and 16-bit times after the assertion of TXValid is detected by the Transmit State Machine. In FS (Xcvr = 1), the SYNC pattern must be asserted on the USB no less than one or more than two CLKs after the assertion of TXValid is detected by the Transmit State Machine.
8	E6	TXReady	Output		**Transmit Data Ready**. If TXValid is asserted, the SIE must always have data available for clocking in to the TX Holding Register on the rising edge of CLK. If TXValid is TRUE and TXReady is asserted at the rising edge of CLK, the CY7C68000 will load the data on the data bus into the TX Holding Register on the next rising edge of CLK. At that time, the SIE should immediately present the data for the next transfer on the data bus.
28	E1	RXValid	Output		**Receive Data Valid**. Indicates that the **DataOut** bus has valid data. The Receive Data Holding Register is full and ready to be unloaded. The SIE is expected to latch the **DataOut** bus on the clock edge.
29	E2	RXActive	Output		**Receive Active**. Indicates that the receive state machine has detected SYNC and is active. RXActive is negated after a bit stuff error or an EOP is detected.
30	H2	RXError	Output		**Receive Error**. 0 Indicates no error. 1 Indicates that a receive error has been detected.
7	–	ValidH	I/O		**ValidH**. This signal indicates that the high-order eight bits of a 16-bit data word presented on the **Data** bus are valid. When **DataBus16_8** = 1 and **TXValid** = 0, **ValidH** is an output, indicating that the high-order receive data byte on the **Data** bus is valid. When **DataBus16_8** = 1 and **TXValid** = 1, **ValidH** is an input and indicates that the high-order transmit data byte, presented on the **Data** bus by the transceiver, is valid. When **DataBus16_8** = **0, ValidH** is undefined. The status of the receive low-order data byte is determined by **RXValid** and are present on D0–D7.

Table 5-1. Pin Descriptions (continued)[1]

56	48	Name	Type	Default	Description
2	–	DataBus16_8	Input		**Data Bus 16_8**. Selects between 8- and 16-bit data transfers. 1–16-bit data path operation enabled. CLK = 30 MHz. 0–8-bit data path operation enabled. When Uni_Bidi = 0, D[8:15] are undefined. When Uni_Bidi =1, D[0:7] are valid on RxValid and D[8:15] are valid on TxValid. CLK = 60 MHz Note that 16-bit operation is only an option for a HS/FS transceiver implementation.[2]
13	A6	XTALIN	Input	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and 20-pF capacitor to GND. It is also correct to drive XTALIN with an external 24-MHz square wave derived from another clock source.
12	A5	XTALOUT	Output	N/A	**Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and 30-pF (nominal) capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
3	–	Uni_Bidi	Input		**Driving this pin HIGH enables the unidirectional mode when the 8-bit interface is selected**. Uni_Bidi is static after power on reset (POR).
6	B5	V_{CC}	Power		V_{CC}. Connect to 3.3V power source.
24	C3	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
35	C4	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
39	C5	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
52	D3	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
4	B2	GND	Ground	N/A	Ground.
23	B4	GND	Ground	N/A	Ground.
27	C2	GND	Ground	N/A	Ground.
37	D1	GND	Ground	N/A	Ground.
49	D2	GND	Ground	N/A	Ground.
31	G1	Reserved	INPUT		Connect pin to Ground.
54	F6	Reserved	INPUT		Connect pin to Ground.
47	F5	Reserved	INPUT		Connect pin to Ground.
42	F4	Reserved	INPUT		Connect pin to Ground.
32	F2	Reserved	INPUT		Connect pin to Ground.
–	A4	Reserved	INPUT		Connect pin to Ground.
–	B3	Reserved	INPUT		Connect pin to Ground.

Note:
2. **DataBus16_8** is static after Power-on Reset (POR) and is only sampled by the macrocell on the negation of Reset.

6.0 Absolute Maximum Ratings

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Supplied ..... 0°C to +70°C
Supply Voltage to Ground Potential ..... –0.5V to +4.0V
DC Input Voltage to Any Input Pin ..... 5.25 V
DC Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V
Power Dissipation ..... 630 mW
Static Discharge Voltage ..... > 2000V
Max Output Current, per IO pin ..... 4 mA
Max Output Current, all 21–IO pins (56-pin package) and 12–IO pins (48-pin package) ..... 84/48 mA

7.0 Operating Conditions

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C
Supply Voltage ..... +3.0V to +3.6V
Ground Voltage 0V
F_{OSC} (Oscillator or Crystal Frequency) ..... 24 MHz ± 100 ppm
..... Parallel Resonant

8.0 DC Characteristics

Table 8-1. DC Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage		2		5.25	V
V_{IL}	Input Low Voltage		–0.5		0.8	V
I_I	Input Leakage Current	$0 < V_{IN} < V_{CC}$			±10	µA
V_{OH}	Output Voltage High	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current High				4	mA
I_{OL}	Output Current Low				4	mA
C_{IN}	Input Pin Capacitance	Except DPLUS/DMINUS/CLK			10	pF
		DPLUS/DMINUS/CLK			15	pF
C_{LOAD}	Maximum Output Capacitance	Output pins			30	pF
I_{SUSP}	Suspend Current	Includes 1.5k-ohm internal pull-up		235	293	µA
		Without 1.5k-ohm internal pull-up		15	55	µA
I_{CC}	Supply Current HS Mode	Normal operation OPMOD[1:0] = 00			175	mA
I_{CC}	Supply Current FS Mode	Normal operation OPMOD[1:0] = 00			90	mA

8.1 USB 2.0 Transceiver

USB 2.0 certified in FS and HS modes.

9.0 AC Electrical Characteristics

9.1 USB 2.0 Transceiver

USB 2.0 certified in FS and HS.

9.2 Timing Diagram

9.2.1 HS/FS Interface Timing–60 MHz

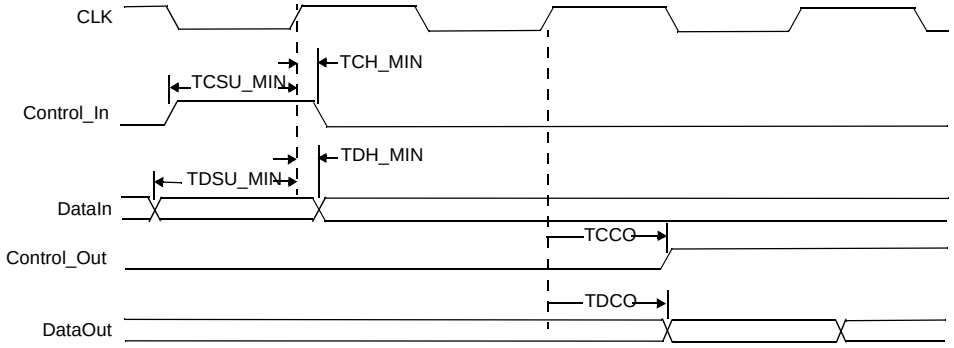

Figure 9-1. 60-MHz Interface Timing Constraints

Table 9-1. 60-MHz Interface Timing Constraints Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{CSU_MIN}	Minimum set-up time for TXValid	8			ns	
T_{CH_MIN}	Minimum hold time for TXValid	1			ns	
T_{DSU_MIN}	Minimum set-up time for Data (transmit direction)	8			ns	
T_{DH_MIN}	Minimum hold time for Data (transmit direction)	1			ns	
T_{CCO}	Clock to Control out time for TXReady, RXValid, RXActive and RXError	1		8	ns	
T_{CDO}	Clock to Data out time (Receive direction)	1		8	ns	

9.2.2 HS/FS Interface Timing–30 MHz

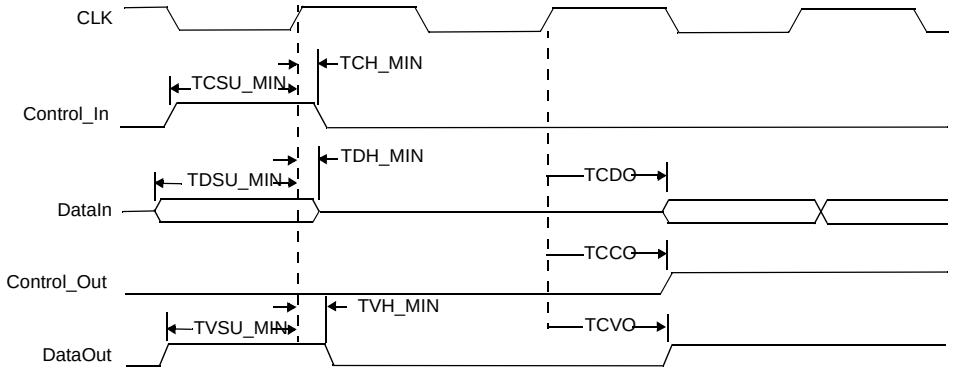

Figure 9-2. 30-MHz Timing Interface Timing Constraints

Table 9-2. 30 MHz Timing Interface Timing Constraints Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{CSU_MIN}	Minimum set-up time for TXValid	20			ns	
T_{CH_MIN}	Minimum hold time for TXValid	1			ns	
T_{DSU_MIN}	Minimum set-up time for Data (Transmit direction)	20			ns	
T_{DH_MIN}	Minimum hold time for Data (Transmit direction)	1			ns	

Table 9-2. 30 MHz Timing Interface Timing Constraints Parameters (continued)

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{CCO}	Clock to Control Out time for TXReady, RXValid, RXActive and RXError	1		20	ns	
T_{CDO}	Clock to Data out time (Receive direction)	1		20	ns	
T_{VSU_MIN}	Minimum set-up time for ValidH (transmit Direction)	20			ns	
T_{VH_MIN}	Minimum hold time for ValidH (Transmit direction	1			ns	
T_{CVO}	Clock to ValidH out time (Receive direction)	1		20	ns	

10.0 Ordering Information

Table 10-1. Ordering Information

Ordering Code	Package Type
CY7C68000-48BAC	48 FBGA
CY7C68000-56PVC	56 SSOP
CY7C68000-56PVCT	56 SSOP Tape/Reel

11.0 Package Diagrams

The TX2 is available in two packages:

- 56-pin SSOP
- 48-pin FBGA.

56-lead Shrunk Small Outline Package O56

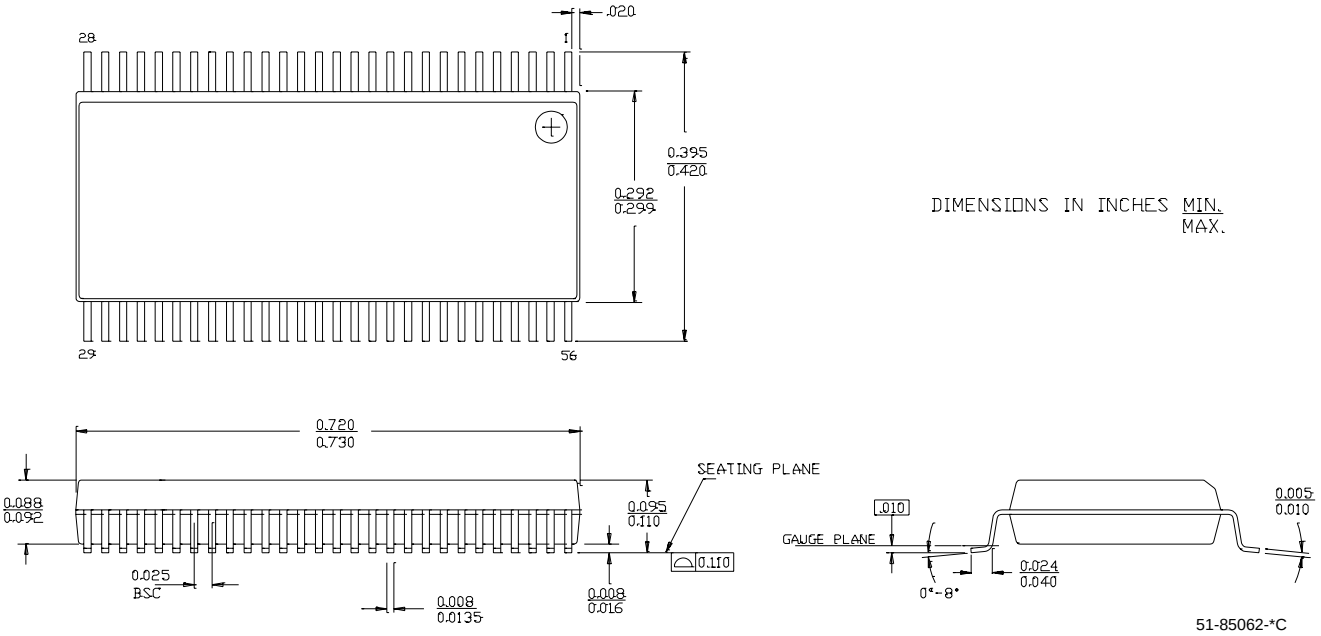

Figure 11-1. 56-lead Shrunk Small Outline Package O56

48-ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A

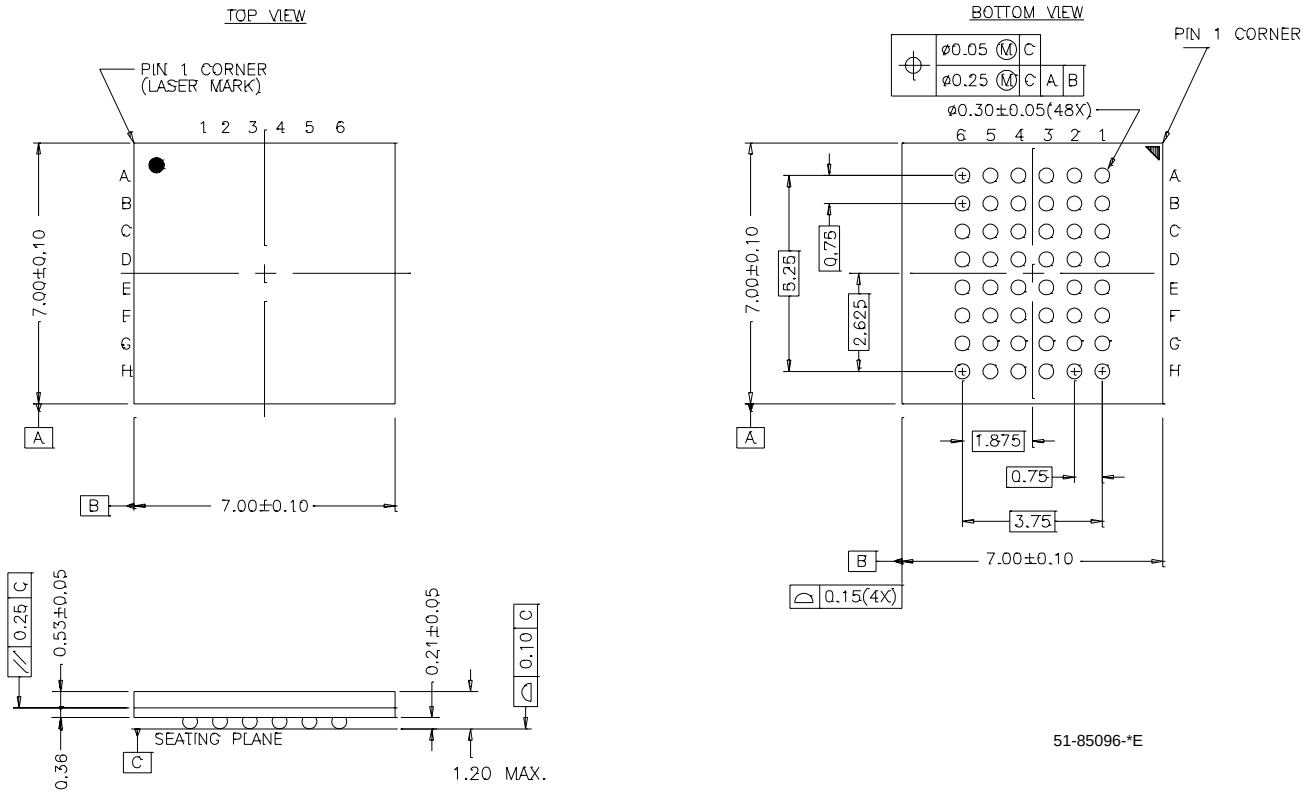

Figure 11-2. 48-pin Fine Pitch Ball Grid Array (7 x 7 x 1.2 mm) BA48A

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Document History Page

Document Title: CY7C68000 TX2™ USB 2.0 UTMI Transceiver Document Number: 38-08016				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112019	03/01/02	KKU	New data sheet
*A	113885	07/01/02	KKU	Updated pinouts on BGA package, signal names. Added timing diagrams.
*B	118521	11/18/02	KKU/ BHA	Added USB Logo. Updated characterization data. Changed from Preliminary to Final.
*C	124507	02/21/03	BHA	Changed ISB Suspend Current maximums.