ISP1301

USB On-The-Go transceiver

Rev. 05 — 2 September 2009 Product data sheet

1. General description

The ISP1301 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver device that is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB Specification Rev. 1.0a*. The ISP1301 can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates.

It is ideal for use in portable electronics devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) and any system chip set (with the USB host or device function built-in but without the USB physical layer) to interface to the physical layer of the USB.

The ISP1301 can interface to devices with digital I/O voltages in the range of 1.65 V to 3.6 V.

The ISP1301 is available in HVQFN24 package.

2. Features

- Fully complies with:
  - *Universal Serial Bus Specification Rev. 2.0*
  - *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a*
  - *On-The-Go Transceiver Specification (CEA-2011) Rev. 1.0*
- Can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates
- Ideal for system ASICs or chip sets with built-in USB OTG dual-role core
- Supports mini USB analog carkit interface
- Supports various serial data interface protocols; transparent general-purpose buffer mode allows you to control the direction of data transfer
- Supports data line and V_{BUS} pulsing session request
- Contains Host Negotiation Protocol (HNP) command and status registers
- Supports serial I^2C-bus interface for OTG status and command controls
- 2.7 V to 4.5 V power supply input range for the ISP1301
- Built-in charge pump regulator outputs 5 V at current greater than 8 mA
- Supports external charge pump
- Supports wide range interfacing I/O voltage ($V_{CC(I/O)}$ = 1.65 V to 3.6 V) for digital control logics
- 8 kV built-in ElectroStatic Discharge (ESD) protection on the DP, DM, V_{BUS} and ID lines
- Full industrial grade operation from −40 °C to +85 °C

- Available in a small HVQFN24 (4×4 mm^2) halogen-free and lead-free package

3. Applications

- Mobile phone
- Digital camera
- Personal digital assistant
- Digital video recorder

4. Ordering information

Table 1. Ordering information

Commercial product code	Package description	Packing	Minimum sellable quantity
ISP1301BSTS	HVQFN24; $4 \times 4 \times 0.85$ mm	7 inch tape and reel non-dry pack	1500 pieces
ISP1301BSFA	HVQFN24, $4 \times 4 \times 0.85$ mm	single tray non-dry pack	490 pieces

5. Block diagram

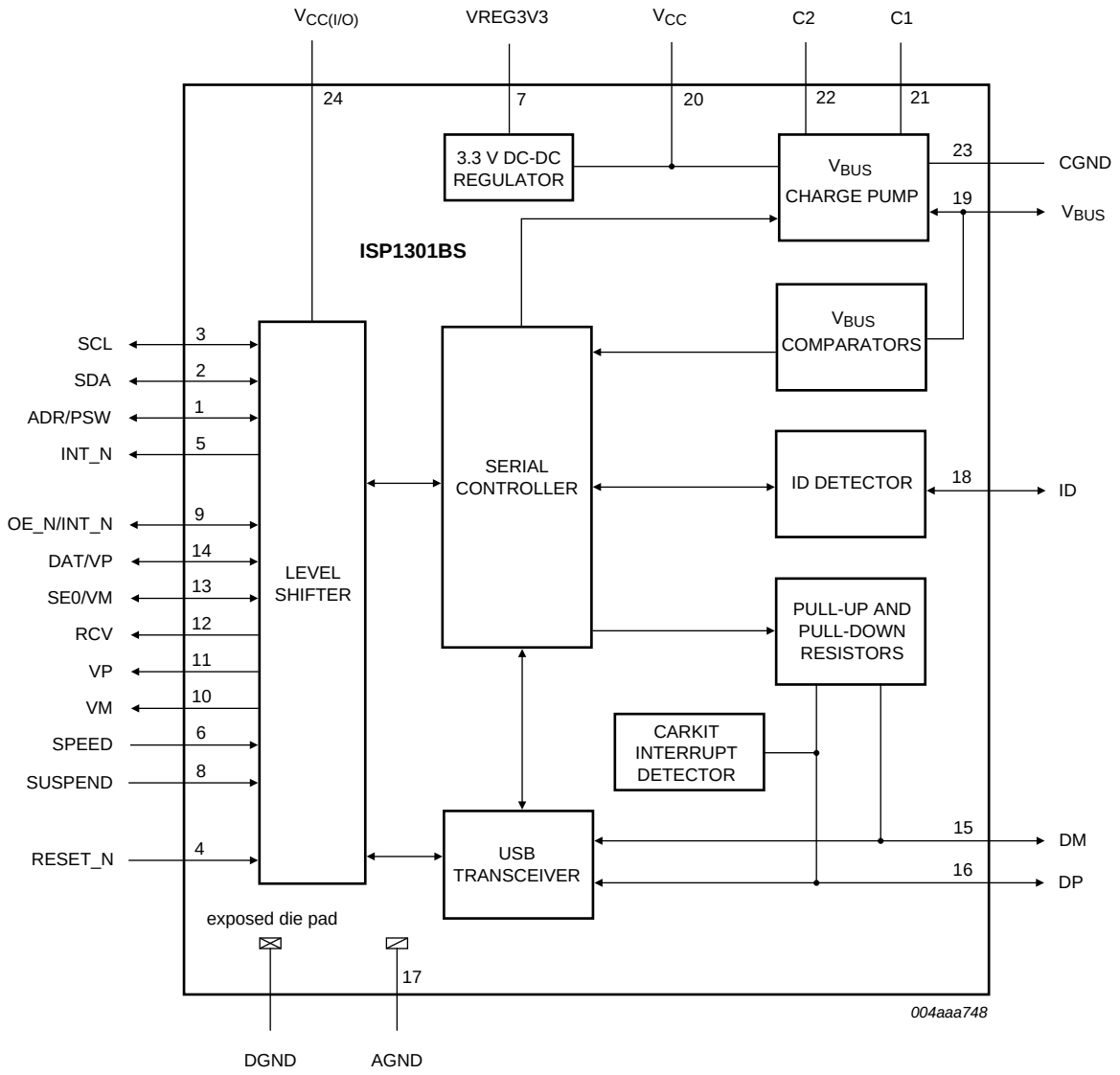
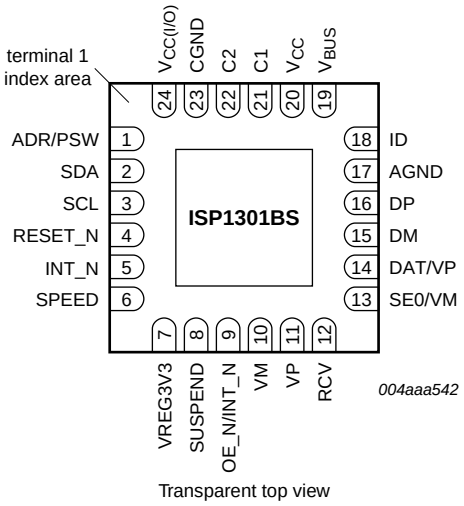


Fig 1. Block diagram

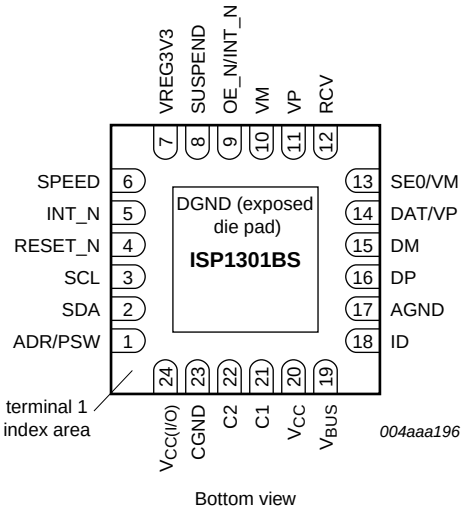
6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration HVQFN24 (top view)



Bottom view

Fig 3. Pin configuration HVQFN24 (bottom view)

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type[2]	Reset state	Description[3]
ADR/PSW	1	I/O	high-Z	**ADR input —** sets the least-significant I²C-bus address bit of the ISP1301; latched-on reset (including power-on reset) **PSW output —** enables or disables the external charge pump after reset bidirectional; push-pull input; 3-state output
SDA	2	I/OD	high-Z	serial I²C-bus data input and output bidirectional; push-pull input; open-drain output
SCL	3	I/OD	high-Z	serial I²C-bus clock input and output bidirectional; push-pull input; open-drain output
RESET_N	4	I	-	asynchronous reset; active LOW push-pull input
INT_N	5	OD	high-Z	interrupt output; active LOW open-drain output
SPEED	6	I	-	speed selection input for the ATX; effective when bit SPD_SUSP_CTRL = 0: • LOW: low-speed • HIGH: full-speed push-pull input
VREG3V3	7	P	-	output of the internal voltage regulator; an external decoupling capacitor of 0.1 μF is required
SUSPEND	8	I	-	suspend selection input for the ATX; effective when bit SPD_SUSP_CTRL = 0: • LOW: normal operating • HIGH: suspend push-pull input
OE_N/ INT_N	9	I/O	high-Z	**OE_N input —** enables driving DP and DM when in USB mode **INT_N output —** interrupt (push pull) when suspended and bit OE_INT_EN = 1 bidirectional; push-pull input; 3-state output
VM	10	O	-	single-ended DM receiver output push-pull output
VP	11	O	-	single-ended DP receiver output push-pull output
RCV	12	O	0	differential receiver output; reflects the differential value of DP and DM push-pull output
SE0/VM	13	I/O	-[4]	**SE0 (input and output) —** SE0 functions in DAT_SE0 USB mode **VM (input and output) —** VM functions in VP_VM USB mode bidirectional; push-pull input; 3-state output

Table 2. Pin description *…continued*

Symbol[1]	Pin	Type[2]	Reset state	Description[3]
DAT/VP	14	I/O	-[4]	**DAT (input and output) —** DAT functions in DAT_SE0 USB mode **VP (input and output) —** VP functions in VP_VM USB mode bidirectional; push-pull input; 3-state output
DM	15	AI/O	-	USB data minus pin (D−)
DP	16	AI/O	-	USB data plus pin (D+)
AGND	17	P	-	analog ground
ID	18	AI/O	-	identification detector input and output; connected to the ID pin of the USB mini receptacle
V_{BUS}	19	AI/O	-	V_{BUS} line input and output of the USB interface; place an external decoupling capacitor of 0.1 μF close to this pin
V_{CC}	20	P	-	supply voltage (2.7 V to 4.5 V)
C1	21	AI/O	-	charge pump capacitor pin 1; typically use a 100 nF capacitor between pins C1 and C2
C2	22	AI/O	-	charge pump capacitor pin 2; typically use a 100 nF capacitor between pins C1 and C2
CGND	23	P	-	ground for the charge pump
$V_{CC(I/O)}$	24	P	-	supply voltage for the interface logic signals (1.65 V to 3.6 V)
DGND	exposed die pad	P	-	digital ground

[1] Symbol names ending with underscore N (for example, NAME_N) indicate active LOW signals.

[2] I = input; O = output; I/O = digital input/output; OD = open-drain output; AI/O = analog input/output; P = power or ground pin.

[3] A detailed description of these pins can be found in Section 7.10.

[4] High-Z when pin OE_N/INT_N is LOW. Driven LOW when pin OE_N/INT_N is HIGH.

7. Functional description

7.1 Serial controller

The serial controller includes the following functions:

- I^2C-bus slave interface
- Interrupt generator
- Mode Control registers
- OTG registers
- Interrupt related registers
- Device identification registers

The serial controller acts as an I^2C-bus slave, and uses the SCL and SDA pins to communicate with the OTG Controller.

For details on serial controller, see Section 10.

7.2 V_{BUS} charge pump

The charge pump supplies current to the V_{BUS} line. It can operate in any of the following modes:

- Output 5 V at current greater than 8 mA
- Pull-up V_{BUS} to 3.3 V through a resistor ($R_{UP(VBUS)}$) to initiate V_{BUS} pulsing SRP
- Pull-down V_{BUS} to ground through a resistor ($R_{DN(VBUS)}$) to discharge V_{BUS} before initiating SRP

7.3 V_{BUS} comparators

V_{BUS} comparators provide indications regarding the voltage level on V_{BUS}.

7.3.1 V_{BUS} valid comparator

This comparator is used by an A-device to determine whether the voltage on V_{BUS} is at a valid level for operation. The minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered to be a fault. During power-up, it is expected that the comparator output will be ignored.

7.3.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Both the A-device and the B-device use this comparator to detect when a session is started. The A-device also uses this comparator to indicate when a session is completed. The session valid threshold of the ISP1301 is between 0.8 V and 2.0 V.

7.3.3 Session end comparator

The session end comparator determines when V_{BUS} is below the B-device session end threshold of 0.2 V to 0.8 V.

7.4 ID detector

In either active or suspended power mode, the ID detector senses the condition of the ID line and differentiates between the following three conditions:

- Pin ID is floating; bit ID_FLOAT = 1
- Pin ID is shorted to ground; bit ID_GND = 1
- Pin ID is connected to ground through resistor R_{ACC_ID}; bit ID_FLOAT = 0 and bit ID_GND = 0

The ID detector also has a switch that can be used to ground pin ID. This switch is controlled by bit ID_PULLDOWN in the serial controller.

7.5 Pull-up and pull-down resistors

The pull-up and pull-down resistors include the following switchable resistors:

- Pin DP pull-up
- Pin DP pull-down
- Pin DM pull-up
- Pin DM pull-down

The pull-up resistor is a context variable as described in the *ECN_27%_Resistor* document. The variable pull-up resistor hardware is implemented to meet the USB ECN_27% specification.

7.6 Analog USB Transceiver (ATX)

The behavior of the USB transceiver depends on operation mode of the ISP1301:

- In USB mode, the USB transceiver block performs USB full-speed or low-speed transceiver functions. This includes differential driver, differential receiver and single-ended receivers.
- In transparent general purpose buffer mode or UART mode, USB transceiver block functions as a level shifter between pins DAT/VP and SE0/VM and pins DP and DM.

7.7 3.3 V DC-DC regulator

The built-in 3.3 V DC-DC regulator conditions the supply voltage (V_{CC}) for use in the ISP1301:

- V_{CC} = 3.6 V to 4.5 V: the regulator will output 3.3 V ± 10 %
- V_{CC} < 3.6 V: the regulator will be bypassed

The output of the regulator can be monitored on the VREG3V3 pin.

7.8 Carkit interrupt detector

The carkit interrupt detector is a comparator that detects when the DP line is below the carkit interrupt threshold $V_{PH\_CR\_INT}$ (0.4 V to 0.6 V). The carkit interrupt detector is enabled in audio mode only (bit AUDIO_EN = 1).

7.9 Power-On Reset (POR)

When V_{CC} is powered on, an internal POR is generated. The internal POR pulse width (t_{PORP}) will be typically 200 ns. The pulse is started when V_{CC} rises above $V_{POR(trip)}$.

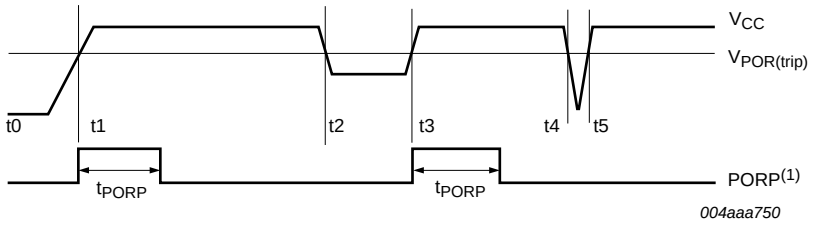
The POR function can be explained by viewing dips at t2 to t3 and t4 to t5 on the V_{CC} curve (Figure 4).

t0 — The internal POR starts with a LOW level.

t1 — The detector will see the passing of the trip level and a delay element will add another t_{PORP} before it drops to LOW.

t2-t3 — The internal POR pulse will be generated whenever V_{CC} drops below $V_{POR(trip)}$ for more than 11 μs.

t4-t5 — The dip is too short (< 11 μs) and the internal POR pulse will not react and will remain LOW.



(1) PORP = Power-On Reset Pulse

Fig 4. Internal POR timing

7.10 Detailed description of pins

7.10.1 ADR/PSW

The ADR/PSW pin has two functions. On reset (including power-on reset), the level on this pin is latched as ADR_REG, which represents the Least Significant Bit (LSB) of the I^2C-bus address of the ISP1301. If bit ADR_REG = 0, the I^2C-bus address for the ISP1301 is 010 1100 (2Ch); if bit ADR_REG = 1, the I^2C-bus address for the ISP1301 is 010 1101 (2Dh).

After reset, the ADR/PSW pin can be programmed as an output. If in the Mode Control 2 register bit PSW_OE = 1, then the ADR/PSW output will be enabled. The logic level will be determined by bit ADR_REG. If bit ADR_REG = 0, then the ADR/PSW pin will be driven HIGH. If bit ADR_REG = 1, then the ADR/PSW pin will be driven LOW.

The ADR/PSW pin can be used to turn on or off the external charge pump. The ISP1301 built-in charge pump supports V_{BUS} current at 8 mA. If the application needs more current support (for example, 50 mA), an external charge pump may be needed. In this case, the ADR/PSW pin can act as a power switch for the external charge pump. Figure 5 shows an example of using external charge pump.

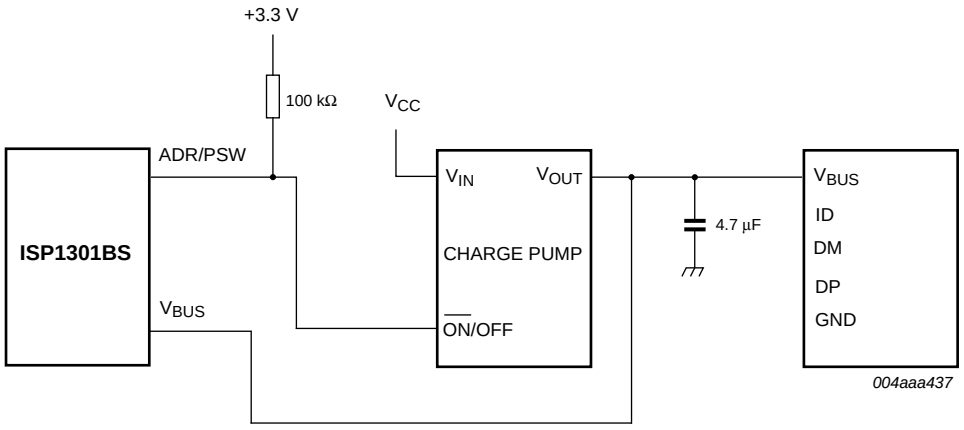


Fig 5. Using external charge pump

7.10.2 SCL and SDA

The SCL (serial clock) and SDA (serial data) signals implement a two-wire serial I^2C-bus.

7.10.3 RESET_N

Active LOW asynchronous reset for all digital logic. Either connect this pin to $V_{CC(I/O)}$ for power-on reset or apply a minimum of 10 µs LOW pulse for hardware reset.

7.10.4 INT_N

The INT_N (interrupt) pin is asserted while an interrupt condition exists. It is de-asserted when the Interrupt Latch register is cleared. The INT_N pin is open-drain, and, therefore, can be connected using a wired-AND with other interrupt signals.

7.10.5 OE_N/INT_N

Pin OE_N/INT_N is normally an input to the ISP1301.

When bit TRANSP_EN = 0 and bit UART_EN = 0, the OE_N/INT_N pin controls the direction of DAT/VP, SE0/VM, DP and DM as indicated in Table 4.

When suspended (either pin SUSPEND = HIGH or bit SUSPEND_REG = 1) and bit OE_INT_EN = 1, pin OE_N/INT_N becomes a push-pull output (active LOW) to indicate the interrupt condition.

7.10.6 SE0/VM, DAT/VP, RCV, VM and VP

The ISP1301 transmits USB data on the USB line under the following conditions:

- Bit TRANSP_EN = 0
- Bit UART_EN = 0
- Pin OE_N/INT_N = LOW

Table 10 shows the operation of the SE0/VM and DAT/VP pins during the transmit operation. The RCV pin is not used during transmit.

The ISP1301 receives USB data from the USB line under the following conditions:

- Bit TRANSP_EN = 0
- Bit UART_EN = 0
- Pin OE_N/INT_N = HIGH

Table 12 shows the operation of the SE0/VM, DAT/VP and RCV pins during the receive operation.

The VP and VM pins are single-ended receiver outputs of the DP and DM pins, respectively.

7.10.7 DP and DM

The DP (data plus) and DM (data minus) pins implement the USB data signals. When in transparent general-purpose buffer mode, the ISP1301 operates as a level shifter between the (DAT/VP, SE0/VM) and (DP, DM) pins.

7.10.8 ID

The ID (identification) pin is connected to the ID pin on the USB mini receptacle. An internal pull-up resistor (to VREG3V3) is connected to this pin. When bit ID_PULLDOWN is set, the ID pin will be shorted to ground.

7.10.9 V_{BUS}

This pin acts as an input to the V_{BUS} comparator or an output from the charge pump.

When the VBUS_DRV bit of the OTG Control register is asserted, the ISP1301 tries to drive V_{BUS} to a voltage of 4.4 V to 5.25 V, with an output current capability of at least 8 mA.

7.10.10 V_{CC}

This pin is an input and supplies power to the ISP1301. The ISP1301 operates when V_{CC} is between 2.7 V and 4.5 V.

7.10.11 C1 and C2

The C1 and C2 pins are to connect the flying capacitor of the charge pump. The output current capacity of the charge pump depends on the value of the capacitor. For maximum efficiency, place capacitors as close as possible to the pins.

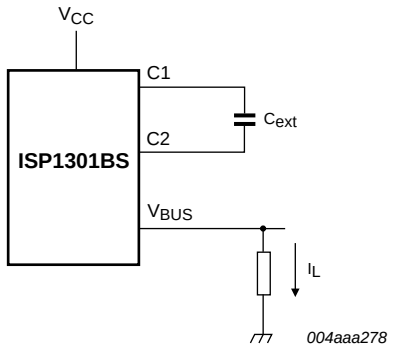


Fig 6. Charge pump capacitor

Table 3. Recommended charge pump capacitor value

C_{ext}	V_{CC}	I_L (max)[1]
47 nF	2.7 V to 4.5 V	8 mA
100 nF	2.7 V to 4.5 V	8 mA
	3.0 V to 4.5 V	18 mA

[1] For output voltage V_{BUS} > 4.7 V (bit VBUS_VLD = 1).

7.10.12 $V_{CC(I/O)}$

This pin is an input and sets logic thresholds. It also powers the pads of the following logic pins:

- ADR/PSW
- DAT/VP, SE0/VM and RCV
- VM and VP
- INT_N
- OE_N/INT_N
- RESET_N
- SPEED
- SUSPEND
- SCL and SDA

7.10.13 AGND, CGND and DGND

AGND, CGND and DGND are ground pins for analog, charge pump and digital circuits, respectively. These pins can be connected separately or together depending on the system performance requirements.

8. Modes of operation

There are four types of modes in the ISP1301:

- Power modes
- Direct I^2C-bus mode
- USB modes
- Transparent modes

8.1 Power modes

Power modes of the ISP1301 are as follows:

- Active power mode: power is on.
- USB suspend mode: to reduce power consumption, the USB differential receiver is powered down.
- Global power-down mode: set bit GLOBAL_PWR_DN = 1 of the Mode Control 2 register; the differential transmitter and receiver, clock generator, charge pump, and all biasing circuits are turned off to reduce power consumption to the minimum possible; for details on waking up the clock, see Section 11.

8.2 Direct I²C-bus mode

In direct I²C-bus mode, an external I²C-bus master (OTG Controller) directly communicates with the serial controller through the SCL and SDA lines. The serial controller has a built-in I²C-bus slave function.

In this mode, an external I²C-bus master can access the internal registers of the device (Status, Control, Interrupt, and so on) through the I²C-bus interface.

The supported I²C-bus bit rate is 100 kbit/s (maximum).

The ISP1301 is in direct I²C-bus mode when either bit TRANSP_EN bit = 0 or pin OE_N/INT_N is de-asserted.

8.3 USB modes

The four USB modes of the ISP1301 are:

- VP_VM unidirectional mode
- VP_VM bidirectional mode
- DAT_SE0 unidirectional mode
- DAT_SE0 bidirectional mode

In VP_VM USB mode, the DAT/VP pin is used for the VP function, the SE0/VM pin is used for the VM function, and the RCV pin is used for the RCV function.

In DAT_SE0 USB mode, the DAT/VP pin is used for the DAT function, the SE0/VM pin is used for the SE0 function, and the RCV pin is not used.

In unidirectional mode, the DAT/VP and SE0/VM pins are always inputs. In bidirectional mode, the direction of these signals depends on the OE_N/INT_N input.

Table 6 specifies the functionality of the device during the four USB modes.

The ISP1301 is in USB mode when both the TRANSP_EN and UART_EN bits are cleared.

8.4 Transparent modes

8.4.1 Transparent general-purpose buffer mode

In transparent general-purpose buffer mode, the DAT/VP and SE0/VM pins are connected to the DP and DM pins, respectively. Using bits TRANSP_BDIR1 and TRANSP_BDIR0 of the Mode Control 2 register as specified in Table 8, you can control the direction of data transfer. The ISP1301 is in transparent general-purpose buffer mode if bit TRANSP_EN = 1 and bit DAT_SE0 = 1.

8.4.2 Transparent UART mode

When in transparent UART mode, the ATX behaves as two logic level translator between the following pins:

- For the TxD signal: from SE0/VM ($V_{CC(I/O)}$ level) to DM (+3.3 V level).
- For the RxD signal: from DP (+3.3 V level) to DAT/VP ($V_{CC(I/O)}$ level).

In UART mode, the OTG Controller is allowed to connect a UART to the DAT/VP and SE0/VM pins of the ISP1301.

UART mode is entered by setting the UART_EN bit in the Mode Control 1 register. UART mode is equivalent to one of transparent general purpose buffer mode (bit TRANSP_BDIR1 = 1, bit TRANSP_BDIR0 = 0).

8.4.3 Summary tables

Table 4. Device operating modes

Mode	USB suspend condition[1]	Bit DAT_SE0	Pin OE_N/INT_N	Bit TRANSP_EN	Bit UART_EN	Description
Direct I²C-bus mode						
Direct I²C-bus mode	X	X	X	0	X	-
	X	X	HIGH	1	X	
	X	1	X	1	X	
USB modes						
USB suspend mode	1	X	X	0	0	see Table 5 and Table 7
USB functional mode	0	X	X	0	0	ATX is fully functional; see Table 6
Transparent modes						
Transparent general-purpose buffer mode	X	1	X	1	0	ATX is not functional; see Table 8
Transparent UART mode	X	X	X	X	1	DAT/VP ← DP (RxD signal of UART) SE0/VM → DM (TxD signal of UART); ATX is not functional

[1] Conditions:
a) bit SPD_SUSP_CTRL = 0 and pin SUSPEND = HIGH, or
b) bit SPD_SUSP_CTRL = 1 and bit SUSPEND_REG = 0.

Table 5. USB suspend mode: I/O

Pin	Function
DP as output	can be driven if pin OE_N/INT_N is active LOW, otherwise high-Z[1]
DM as output	can be driven if pin OE_N/INT_N is active LOW, otherwise high-Z[1]
V_{BUS}	can be driven depending on bit VBUS_DRV
SCL	connected to SCL I/O of the I²C-bus slave
SDA	connected to SDA I/O of the I²C-bus slave

[1] In USB suspend mode, the ISP1301 can drive the DP and DM lines, if the OE_N/INT_N input (when the OE_INT_EN bit is not set) is LOW. In such a case, these outputs are driven as in USB functional modes, but with the full-speed characteristics, irrespective of the value of the SPEED input pin or the SPEED_REG bit.

Table 6. USB functional modes: I/O values

USB mode[1]		Bit		Pin					
		DAT_SE0	BI_DI	OE_N/ INT_N	DAT/VP	SE0/VM	VP	VM	RCV
VP_VM	unidirectional	0	0	X	TxD+[2]	TxD−[2]	RxD+[3]	RxD−[3]	RxD[6]
	bidirectional	0	1	LOW	TxD+[2]	TxD−[2]			
		0	1	HIGH	RxD+[3]	RxD−[3]			
DAT_SE0	unidirectional	1	0	X	TxD[4]	FSE0[5]			
	bidirectional	1	1	LOW	TxD[4]	FSE0[5]			
		1	1	HIGH	RxD[6]	RSE0[7]			

[1] Some of the modes and signals are provided to achieve backward compatibility with IP cores.

[2] TxD+ and TxD− are single-ended inputs to drive the DP and DM outputs, respectively, in single-ended mode.

[3] RxD+ and RxD− are the outputs of the single-ended receivers connected to DP and DM, respectively.

[4] TxD is the input to drive DP and DM in DAT_SE0 mode.

[5] FSE0 is to force an SE0 on the DP and DM lines in DAT_SE0 mode.

[6] RxD is the output of the differential receiver.

[7] RSE0 is an output indicating that an SE0 has been received on the DP and DM lines.

Table 7. USB suspend mode: I/O values

USB suspend mode	Input pin		Output pin				
	DP	DM	DAT/VP	SE0/VM	VP	VM	RCV
DAT_SE0 (bit DAT_SE0 = 1)	LOW	LOW	LOW	HIGH	LOW	LOW	X
	HIGH	LOW	HIGH	LOW	HIGH	LOW	X
	LOW	HIGH	LOW	LOW	LOW	HIGH	X
	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	X
VP_VM (bit DAT_SE0 = 0)	LOW	LOW	LOW	LOW	LOW	LOW	X
	HIGH	LOW	HIGH	LOW	HIGH	LOW	X
	LOW	HIGH	LOW	HIGH	LOW	HIGH	X
	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	X

Table 8. Transparent general-purpose buffer mode

Bit TRANSP_BDIR[1:0]	Direction of the data flow	
00	DAT/VP → DP	SE0/VM → DM
01	DAT/VP → DP	SE0/VM ← DM
10	DAT/VP ← DP	SE0/VM → DM
11	DAT/VP ← DP	SE0/VM ← DM

9. USB transceiver

9.1 Differential driver

The operation of the driver is described in Table 9. The register bits and the pins used in the column heading are described in Section 10.1 and Section 7.10, respectively.

Table 9. Transceiver driver operation setting

Suspend[1]	Bit TRANSP_EN	Pin OE_N/INT_N	Bit DAT_SE0	Differential driver
0	0	LOW	0	output value from DAT/VP to DP and SE0/VM to DM
0	0	LOW	1	output value from DAT/VP to DP and DM if SE0/VM is 0; otherwise, drive both DP and DM LOW
1	0	LOW	X	output value from DAT/VP to DP and DM
X	X	HIGH	X	high-Z
X	1	X	X	high-Z

[1] Can be controlled by using either the SUSPEND pin or the SUSPEND_REG bit.

Table 10. USB functional mode: transmit operation

USB mode	Input pin		Output pin	
	DAT/VP	SE0/VM	DP	DM
DAT_SE0	LOW	LOW	LOW	HIGH
	HIGH	LOW	HIGH	LOW
	LOW	HIGH	LOW	LOW
	HIGH	HIGH	LOW	LOW
VP_VM	LOW	LOW	LOW	LOW
	HIGH	LOW	HIGH	LOW
	LOW	HIGH	LOW	HIGH
	HIGH	HIGH	HIGH	HIGH

9.2 Differential receiver

Table 11 describes the operation of the differential receiver. The register bits and the pins used in the column heading are described in Section 10.1 and Section 7.10, respectively.

The detailed behavior of the receive transceiver operation is given in Table 12.

Table 11. Differential receiver operation settings

Suspend[1]	Bit TRANSP_EN	Pin OE_N/INT_N	Bit DAT_SE0	Differential receiver
1	X	X	X	X
X	X	LOW	X	0
X	1	X	X	0
0	0	HIGH	1	output differential value from DP and DM to DAT/VP and RCV
0	0	HIGH	0	output differential value from DP and DM to RCV

[1] Can be controlled by using either the SUSPEND pin or the SUSPEND_REG bit.

Table 12. USB functional mode: receive operation

USB mode	Suspend[1]	Input pin		Output pin		
		DP	DM	DAT/VP	SE0/VM	RCV
DAT_SE0	0	LOW	LOW	RCV	HIGH	last value of RCV
DAT_SE0	0	HIGH	LOW	HIGH	LOW	HIGH
DAT_SE0	0	LOW	HIGH	LOW	LOW	LOW
DAT_SE0	0	HIGH	HIGH	RCV	LOW	last value of RCV
DAT_SE0	1	LOW	LOW	LOW	HIGH	X
DAT_SE0	1	HIGH	LOW	HIGH	LOW	X
DAT_SE0	1	LOW	HIGH	LOW	LOW	X
DAT_SE0	1	HIGH	HIGH	HIGH	LOW	X
VP_VM	0	LOW	LOW	LOW	LOW	last value of RCV
VP_VM	0	HIGH	LOW	HIGH	LOW	HIGH
VP_VM	0	LOW	HIGH	LOW	HIGH	LOW
VP_VM	0	HIGH	HIGH	HIGH	HIGH	last value of RCV
VP_VM	1	LOW	LOW	LOW	LOW	X
VP_VM	1	HIGH	LOW	HIGH	LOW	X
VP_VM	1	LOW	HIGH	LOW	HIGH	X
VP_VM	1	HIGH	HIGH	HIGH	HIGH	X

[1] Can be controlled by using either the SUSPEND pin or the SUSPEND_REG bit.

10. Serial controller

10.1 Register map

Table 13 provides an overview of the serial controller registers.

Table 13. Serial controller registers

Register	Width (bits)	Access[1]	Memory address	Functionality	Reference
Vendor ID	16	R	00h to 01h	device identification registers	Section 10.1.1 on page 18
Product ID	16	R	02h to 03h		
Version ID	16	R	14h to 15h		
Mode Control 1	8	R/S/C	**Set —** 04h **Clear —** 05h	mode control registers	Section 10.1.2 on page 19
Mode Control 2	8	R/S/C	**Set —** 12h **Clear —** 13h		
OTG Control	8	R/S/C	**Set —** 06h **Clear —** 07h	OTG registers	Section 10.1.3 on page 20
OTG Status	8	R	10h		
Interrupt Source	8	R	08h	interrupt related registers	Section 10.1.4 on page 21
Interrupt Latch	8	R/S/C	**Set —** 0Ah **Clear —** 0Bh		
Interrupt Enable Low	8	R/S/C	**Set —** 0Ch **Clear —** 0Dh		
Interrupt Enable High	8	R/S/C	**Set —** 0Eh **Clear —** 0Fh		

[1] The R/S/C access type represents a field that can be read, set or cleared (set to 0). A register can be read from either of the indicated addresses: set or clear. Writing logic 1 to the set address causes the associated bit to be set. Writing logic 1 to the clear address causes the associated bit to be cleared. Writing logic 0 to an address has no effect.

10.1.1 Device identification registers

10.1.1.1 Vendor ID register (Read: 00h to 01h)

Table 14 provides the bit description of the Vendor ID register.

Table 14. Vendor ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	VENDORID[15:0]	R	04CCh	ST-Ericsson' Vendor ID

10.1.1.2 Product ID register (Read: 02h to 03h)

The bit description of this register is given in Table 15.

Table 15. Product ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	PRODUCTID[15:0]	R	1301h	Product ID of the ISP1301

10.1.1.3 Version ID register (Read: 14h to 15h)

Table 16 shows the bit description of this register.

Table 16. Version ID register: bit description

Bit	Symbol	Access	Value	Description
15 to 0	VERSIONID[15:0]	R	0210h	Version number of the ISP1301

10.1.2 Mode control registers

10.1.2.1 Mode Control 1 register (Set/Clear: 04h/05h)

The bit allocation of the Mode Control 1 register is given in Table 17.

Table 17. Mode Control 1 register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	UART_EN	OE_INT_EN	BDIS_ACON_EN	TRANSP_EN	DAT_SE0	SUSPEND_REG	SPEED_REG
Reset	-	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 18. Mode Control 1 register: bit description

Bit	Symbol	Description
7	-	reserved
6	UART_EN	When set, the ATX is in transparent UART mode.
5	OE_INT_EN	When set and when in suspend mode, pin OE_N/INT_N becomes an output and is asserted when an interrupt occurs.
4	BDIS_ACON_EN	Enables the A-device to connect if the B-device disconnect is detected; see Section 10.3.
3	TRANSP_EN	When set, the ATX is in transparent mode.
2	DAT_SE0	**0 —** VP_VM mode **1 —** DAT_SE0 mode; see Table 6 and Table 7
1	SUSPEND_REG	Sets the ISP1301 in suspend mode, if bit SPD_SUSP_CTRL = 1. **0 —** active-power mode **1 —** USB suspend mode
0	SPEED_REG	Sets the rise time and the fall time of the transmit driver in USB modes, if bit SPD_SUSP_CTRL = 1. **0 —** USB low-speed mode **1 —** USB full-speed mode

10.1.2.2 Mode Control 2 register (Set/Clear: 12h/13h)

For the bit allocation of this register, see Table 19.

Table 19. Mode Control 2 register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	EN2V7	PSW_OE	AUDIO_EN	TRANSP_BDIR1	TRANSP_BDIR0	BI_DI	SPD_SUSP_CTRL	GLOBAL_PWR_DN
Reset	0	0	0	0	0	1	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 20. Mode Control 2 register: bit description

Bit	Symbol	Description
7	EN2V7	**0 —** V_{CC} = 3.0 V to 4.5 V **1 —** V_{CC} = 2.7 V to 4.5 V **Remark:** For the operating condition to be USB compliant, it is recommended to always set this bit as logic 0. Setting this bit as logic 1 may not cause any functional problems, but it might cause some USB specification violation in terms of voltage levels required for the USB signals.
6	PSW_OE	**0 —** ADR/PSW pin acts as an input **1 —** ADR/PSW pin is driven
5	AUDIO_EN	**0 —** SE receiver is enabled; cr_int detector is disabled **1 —** SE receiver is turned off (pin VP = LOW, pin VM = LOW); cr_int detector is enabled
4 to 3	TRANSP_BDIR[1:0]	controls the direction of data transfer in transparent general-purpose buffer mode; see Table 8
2	BI_DI	**0 —** direction of DAT/VP and SE0/VM are fixed (transmit only) **1 —** direction of DAT/VP and SE0/VM are controlled by pin OE_N/INT_N; see Table 6
1	SPD_SUSP_CTRL	control of speed and suspend in USB modes: **0 —** controlled by pins SPEED and SUSPEND **1 —** controlled by bit SPEED_REG and bit SUSPEND_REG of the Mode Control 1 register
0	GLOBAL_PWR_DN	**0 —** normal operation **1 —** sets the ISP1301 to Power-down mode Activities on the I^2C-bus or any OTG event can wake-up the chip; see Section 11

10.1.3 OTG registers

10.1.3.1 OTG Control register (Set/Clear: 06h/07h)

Table 21 provides the bit allocation of the OTG Control register.

Table 21. OTG Control register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VBUS_CHRG	VBUS_DISCHRG	VBUS_DRV	ID_PULLDOWN	DM_PULLDOWN	DP_PULLDOWN	DM_PULLUP	DP_PULLUP
Reset	0	0	0	0	1	1	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 22. OTG Control register: bit description

Bit	Symbol	Description
7	VBUS_CHRG	charge V_{BUS} through a resistor to 3.3 V
6	VBUS_DISCHRG	discharge V_{BUS} through a resistor to ground
5	VBUS_DRV	drive V_{BUS} to 5 V through the charge pump
4	ID_PULLDOWN	connect the ID pin to ground
3	DM_PULLDOWN	connect the DM pull-down resistor to ground

Table 22. OTG Control register: bit description …continued

Bit	Symbol	Description
2	DP_PULLDOWN	connect the DP pull-down resistor to ground
1	DM_PULLUP	connect the DM pull-up resistor to 3.3 V
0	DP_PULLUP	connect the DP pull-up resistor to 3.3 V

10.1.3.2 OTG Status register (Read: 10h)

Table 23 shows the bit allocation of the OTG Status register.

Table 23. OTG Status register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	B_SESS_VLD	B_SESS_END	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 24. OTG Status register: bit description

Bit	Symbol	Description
7	B_SESS_VLD	set when the V_{BUS} voltage is above the B-device session valid threshold (2.0 V to 4.0 V)
6	B_SESS_END	set when the V_{BUS} voltage is below the B-device session end threshold (0.2 V to 0.8 V)
5 to 0	-	reserved

10.1.4 Interrupt related registers

10.1.4.1 Interrupt Source register (Read: 08h)

This register indicates the current state of the signals that can generate an interrupt. The bit allocation of the Interrupt Source register is given in Table 25.

Table 25. Interrupt Source register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 26. Interrupt Source register: bit description

Bit	Symbol	Description
7	CR_INT	DP pin is above the carkit interrupt threshold (0.4 V to 0.6 V)
6	BDIS_ACON	set when bit BDIS_ACON_EN is set, and the ISP1301 asserts bit DP_PULLUP after detecting the B-device disconnect
5	ID_FLOAT	ID pin is floating
4	DM_HI	DM pin is HIGH
3	ID_GND	ID pin is connected to ground
2	DP_HI	DP pin is HIGH
1	SESS_VLD	session valid comparator; threshold = 0.8 V to 2.0 V
0	VBUS_VLD	A-device V_{BUS} valid comparator; threshold > 4.4 V

10.1.4.2 Interrupt Latch register (Set/Clear: 0Ah/0Bh)

This register indicates the source that generated the interrupt. The bit allocation of the Interrupt Latch register is given in Table 27.

Table 27. Interrupt Latch register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 28. Interrupt Latch register: bit description

Bit	Symbol	Description
7	CR_INT	interrupt for CR_INT status change
6	BDIS_ACON	interrupt for BDIS_ACON status change
5	ID_FLOAT	interrupt for ID_FLOAT status change
4	DM_HI	interrupt for DM_HI status change
3	ID_GND	interrupt for ID_GND status change
2	DP_HI	interrupt for DP_HI status change
1	SESS_VLD	interrupt for SESS_VLD status change
0	VBUS_VLD	interrupt for VBUS_VLD status change

10.1.4.3 Interrupt Enable Low register (Set/Clear: 0Ch/0Dh)

This register enables interrupts on transition from true to false. For the bit allocation of this register, see Table 29.

Table 29. Interrupt Enable Low register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 30. Interrupt Enable Low register: bit description

Bit	Symbol	Description
7	CR_INT	interrupt enable for CR_INT status change from 1 to 0
6	BDIS_ACON	interrupt enable for BDIS_ACON status change from 1 to 0
5	ID_FLOAT	interrupt enable for ID_FLOAT status change from 1 to 0
4	DM_HI	interrupt enable for DM_HI status change from 1 to 0
3	ID_GND	interrupt enable for ID_GND status change from 1 to 0
2	DP_HI	interrupt enable for DP_HI status change from 1 to 0
1	SESS_VLD	interrupt enable for SESS_VLD status change from 1 to 0
0	VBUS_VLD	interrupt enable for VBUS_VLD status change from 1 to 0

10.1.4.4 Interrupt Enable High register (Set/Clear: 0Eh/0Fh)

The Interrupt Enable High register enables interrupts on transition from FALSE to TRUE. Table 31 provides the bit allocation of this register.

Table 31. Interrupt Enable High register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CR_INT	BDIS_ ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 32. Interrupt Enable High register: bit description

Bit	Symbol	Description
7	CR_INT	interrupt enable for CR_INT status change from 0 to 1
6	BDIS_ACON	interrupt enable for BDIS_ACON status change from 0 to 1
5	ID_FLOAT	interrupt enable for ID_FLOAT status change from 0 to 1
4	DM_HI	interrupt enable for DM_HI status change from 0 to 1
3	ID_GND	interrupt enable for ID_GND status change from 0 to 1
2	DP_HI	interrupt enable for DP_HI status change from 0 to 1
1	SESS_VLD	interrupt enable for SESS_VLD status change from 0 to 1
0	VBUS_VLD	interrupt enable for VBUS_VLD status change from 0 to 1

10.2 Interrupts

Table 26 indicates the signals that can generate interrupts. Any of the signals given in Table 26 can generate an interrupt when the signal becomes either LOW or HIGH. After an interrupt has been generated, the OTG Controller should be able to read the status of each signal and the bit that indicates whether that signal generated the interrupt.

A bit in the Interrupt Latch register is set when any of these occurs:

- Writing logic 1 to its set address causes the corresponding bit to be set.
- The corresponding bit in the Interrupt Enable High register is set, and the associated signal changes from LOW to HIGH.
- The corresponding bit in the Interrupt Enable Low register is set, and the associated signal changes from HIGH to LOW.

The Interrupt Latch register bit is cleared by writing logic 1 to its clear address.

10.3 Auto-connect

The Host Negotiation Protocol (HNP) in the OTG supplement specifies the following sequence of events to transfer the role of the host from the A-device to the B-device:

1. The A-device puts the bus in the suspend state.
2. The B-device simulates a disconnect by de-asserting its DP pull-up.
3. The A-device detects SE0 on the bus, and asserts its DP pull-up.
4. The B-device detects that the DP line is HIGH, and takes the role of the host.

The OTG supplement specifies that the time between the B-device de-asserting its DP pull-up and the A-device asserting its pull-up must be less than 3 ms. For an A-device with a slow interrupt response time, 3 ms may not be enough time to write an I^2C-bus command to the ISP1301 to assert the DP pull-up. An alternative method is for the A-device transceiver to automatically assert the DP pull-up after detecting an SE0 from the B-device.

The sequence of events is: After finishing data transfers between the A-device and the B-device and before suspending the bus, the A-device sends SOFs. The B-device receives these SOFs, and does not transmit any packet back to the A-device. During this time, the A-device sets the BDIS_ACON_EN bit in the ISP1301. This enables the ISP1301 to look for SE0 whenever the A-device is not transmitting (that is, whenever the OE_N/INT_N pin of the ISP1301 is not asserted). After the BDIS_ACON_EN bit is set, the A-device stops transmitting SOFs and allows the bus to go to the idle state. If the B-device disconnects, the bus goes to SE0, and the ISP1301 logic automatically turns on the A-device pull-up.

11. Clock wake-up scheme

The following subsections explain the ISP1301 clock stop timing, events triggering the clock to wake up, and the timing of the clock wake-up.

11.1 Power-down event

The clock is stopped when the GLOBAL_PWR_DN bit is set. It takes approximately 8 ms for the clock to stop from the time the power-down condition is detected. The clock always stops at its falling edge. The waveform is given in Figure 7.

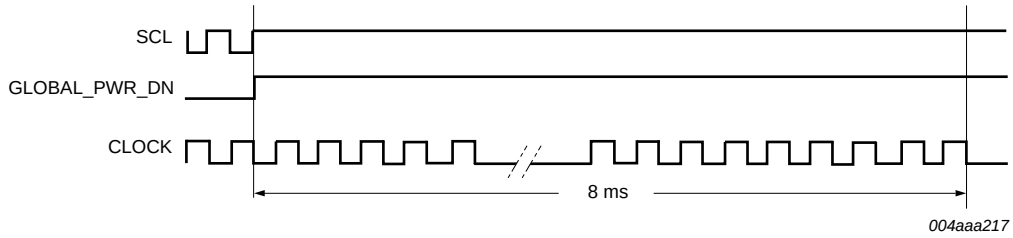


Fig 7. Clock stopped using the GLOBAL_PWR_DN bit

11.2 Clock wake-up events

The clock wakes up when any of the following events occur on the ISP1301 pins:

- SCL goes LOW.
- V_{BUS} goes above the session valid threshold (0.8 V to 2.0 V), provided the SESS_VLD bit in the Interrupt Enable High register is set.
- ID changes when mini-A plug is inserted, provided the ID_FLOAT bit in the Interrupt Enable Low register is set.
- ID changes when mini-A plug is removed, provided the ID_FLOAT bit in the Interrupt Enable High register is set.
- DP goes HIGH, provided the DP_HI bit in the Interrupt Enable High register is set.
- DM goes HIGH, provided the DM_HI bit in the Interrupt Enable High register is set.

The event triggers the clock to start and a stable clock is guaranteed after about six clock periods, which is approximately 8 μs. The startup analog clock time is 10 μs. Therefore, the total estimated start time after a triggered event is about 20 μs. The clock will always start at its rising edge.

Waveforms of the clock wake-up because of different events are given in Figure 8, Figure 9, Figure 10, Figure 11 and Figure 12.

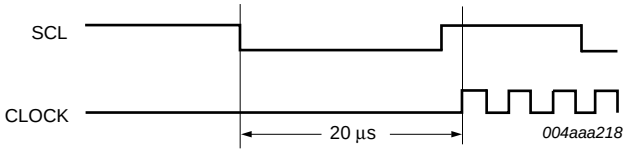


Fig 8. Clock wake-up using SCL

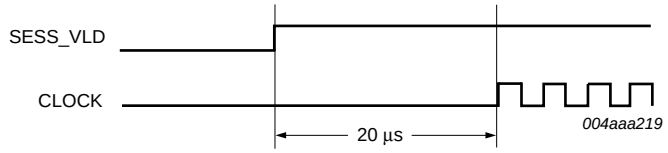


Fig 9. Clock wake-up by V_{BUS}

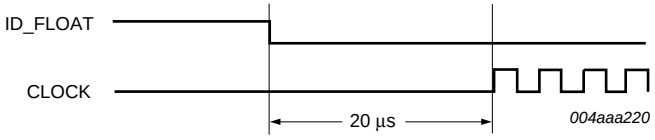


Fig 10. Clock wake-up by ID change (1)

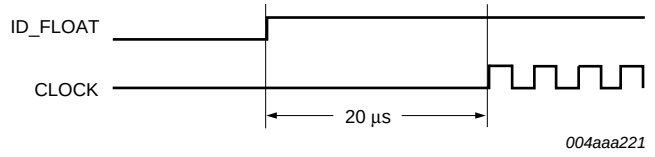


Fig 11. Clock wake-up by ID change (2)

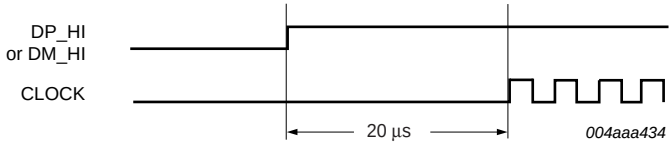


Fig 12. Clock wake-up by data line SRP

When an event is triggered and the clock is started, it will remain active for 8 ms. If the GLOBAL_PWR_DN bit is not cleared within this 8 ms period, the clock will stop. If the clock wakes up because of any event other than SCL going LOW, an interrupt will be generated once the clock is active.

12. I²C-bus protocol

For detailed information, refer to *The I²C-bus specification; version 2.1*.

12.1 I²C-bus byte transfer format

Table 33. I²C-bus byte transfer format

S[1]	Byte 1	A[2]	Byte 2	A[2]	Byte 3	A[2]	..	A[2]	P[3]
	8 bits		8 bits		8 bits		..		

[1] S = Start.

[2] A = Acknowledge.

[3] P = Stop.

12.2 I²C-bus device address

Table 34. I²C-bus device address byte 1 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	A6	A5	A4	A3	A2	A1	A0	R/W_N
Value	0	1	0	1	1	0	[1]	X

[1] The value of A0 (LSB) is loaded from pin ADR/PSW during reset (including power-on reset). If pin ADR/PSW = HIGH, bit A0 = 1; otherwise bit A0 = 0.

Table 35. I²C-bus device address byte 1 bit description

Bit	Symbol	Description
7 to 1	A[6:0]	**Device address**: The device address of the ISP1301 is: 01 0110 (A0).
0	R/W_N	Read or write command. **0** — write **1** — read

12.3 Write format

A write operation can be performed as:

- One-byte write to the specified register address.
- Multi-byte write to N consecutive registers, starting from the specified start address. N defines the number of registers to write. If N = 1, only the start register is written.

12.3.1 One-byte write

Figure 13 illustrates the byte sequence.

Table 36. Transfer format description for one-byte write

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits address of register K
ACK	slave generates an acknowledgment

Table 36. Transfer format description for one-byte write …continued

Byte	Description
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
P	master generates a STOP condition

12.3.2 Multiple-byte write

Figure 13 illustrates the byte sequence.

Table 37. Transfer format description for multiple-byte write

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits address of register K. This is the start address for writing multiple data bytes to consecutive registers. After a byte is written, the register address is automatically incremented by 1. **Remark:** If the master writes to a non existent register, the slave must send a 'not ACK' and also must not increment the index address.
ACK	slave generates an acknowledgment
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
Write data K + 1	master writes data to register K + 1
ACK	slave generates an acknowledgment
:	:
Write data K + N – 1	master writes data to register K + N – 1. When the incremented address K + N – 1 becomes > 255, the register address rolls over to 0. Therefore, it is possible that some registers may be overwritten, if the transfer is not stopped before the rollover.
ACK	slave generates an acknowledgment
P	master generates a STOP condition

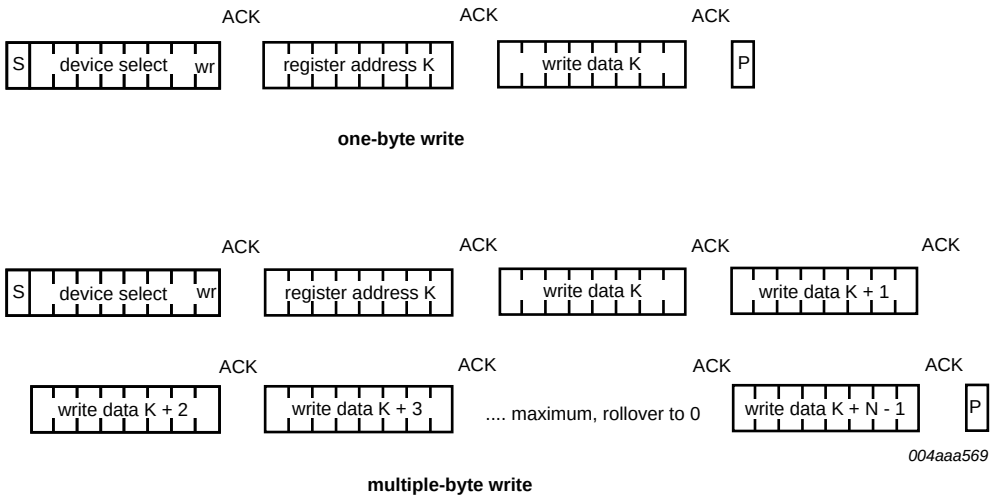


Fig 13. Writing data to the ISP1301 registers

12.4 Read format

A read operation can be performed in two ways:

- Current address read: to read the register at the current address.
  - Single register read
- Random address read: to read N registers starting at a specified address. N defines the number of registers to be read. If N = 1, only the start register is read.
  - Single register read
  - Multiple register read

12.4.1 Current address read

Figure 14 illustrates the byte sequence.

Table 38. Transfer format description for current address read

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. If the start address is not specified, the read operation starts from where the index register is pointing to because of a previous read or write operation.
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a stop condition

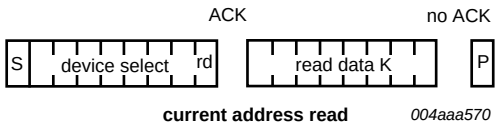


Fig 14. Current address read

12.4.2 Random address read

12.4.2.1 Single read

Figure 15 illustrates the byte sequence.

Table 39. Transfer format description for single-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits device address and writes command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K to be read from
ACK	slave generates an acknowledgment
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
S	master restarts with a START condition
Read data K	slave transmits and master reads data from register K
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a STOP condition

12.4.2.2 Multiple read

Figure 15 illustrates the byte sequence.

Table 40. Transfer format description for multiple-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K to be read from
ACK	slave generates an acknowledgment
S	master restarts with a START condition
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. After a byte is read, the address is automatically incremented by 1.
ACK	master generates an acknowledgment
Read data K + 1	slave transmits and master reads data from register K + 1
ACK	master generates an acknowledgment
:	:

Table 40. Transfer format description for multiple-byte read *…continued*

SDA line	Description
Read data K + N – 1	slave transmits and master reads data register K + N – 1. This is the last register to read. After incrementing, the address rolls over to 0. Here, N represents the number of addresses available in the slave.
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a STOP condition

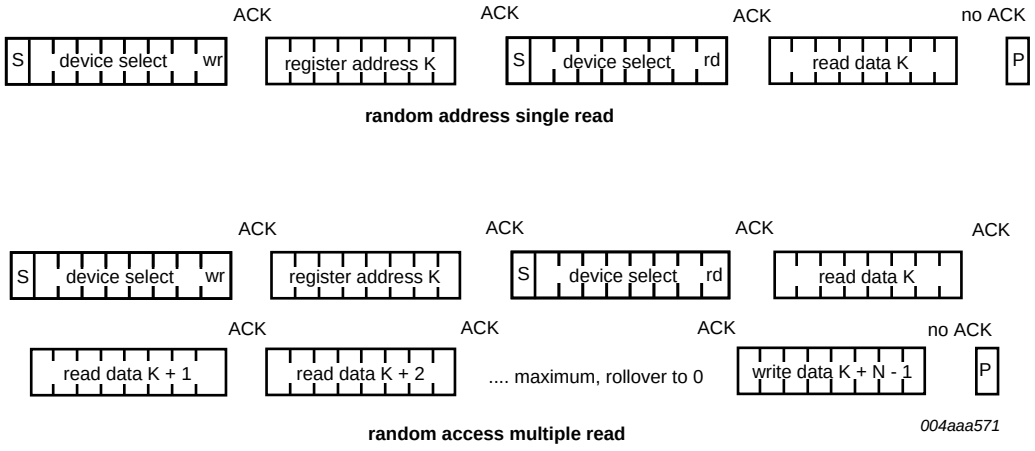


Fig 15. Random address read

13. Limiting values

Table 41. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+4.6	V
V_I	input voltage	V_I = –1.8 V to +5.4 V		–0.5	$V_{CC(I/O)}$ + 0.5	V
I_{lu}	latch-up current			-	100	mA
V_{esd}	electrostatic discharge voltage	I_{LI} < 1 μA				
		pins DP, DM, ID, V_{BUS}, AGND, CGND and DGND	[1]	–8	+8	kV
		all other pins		–2	+2	kV
T_{stg}	storage temperature			–60	+125	°C

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model). A 4.7 μF capacitor is needed from VREG3V3 and V_{BUS} to ground.

14. Recommended operating conditions

Table 42. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			2.7[1]	-	3.6	V
$V_{CC(I/O)}$	input/output supply voltage		[2]	1.65	-	3.6	V
V_I	input voltage			0	-	$V_{CC(I/O)}$	V
$V_{IA(I/O)}$	input voltage on analog I/O pins		[3]	0	-	3.6	V
$V_{(pu)OD}$	open-drain pull-up voltage		[4]	0	-	3.6	V
T_{amb}	ambient temperature			–40	-	+85	°C

[1] For the operating condition to be USB compliant, it is not recommended to go below 3.0 V. Voltages less than 3.0 V may not cause any functional problems but it might cause some USB specification violation in terms of voltage levels required for the USB signals.

[2] $V_{CC(I/O)}$ should be less than or equal to V_{CC}.

[3] Input voltage on analog I/O pins DP and DM.

[4] Open-drain output pull-up voltage on pins SCL, SDA and INT_N.

15. Static characteristics

Table 43. Static characteristics: supply pins

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Charge pump disabled							
$V_{O(REG3V3)}$	output voltage from internal 3.3 V regulator	V_{CC} = 3.0 V to 4.5 V	[1]	3.0	-	3.6	V
		V_{CC} = 2.7 V to 3.0 V		2.7	-	3.0	V
$V_{POR(trip)}$	power-on reset trip voltage			1.5	-	2.5	V
I_{CC}	supply current	transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins DP and DM	[2]	-	4	8	mA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	transmitting and receiving at 12 Mbit/s	[2]	-	1	2	mA
$I_{CC(idle)}$	idle and SE0 supply current	idle: V_{DP} > 2.7 V, V_{DM} < 0.3 V; SE0: V_{DP} < 0.3 V, V_{DM} < 0.3 V	[3]	-	-	300	µA
$I_{CC(I/O)(static)}$	static supply current on pin $V_{CC(I/O)}$	idle, SE0 or suspend		-	-	20	µA
$I_{CC(pd)}$	Power-down mode supply current	bit GLOBAL_PWR_DN = 1	[3]	-	-	20	µA
Charge pump enabled							
$I_{CC(cp)}$	charge pump supply current	I_{load} = 8 mA; ATX is idle		-	-	20	mA
		I_{load} = 0 mA; ATX is idle		-	-	300	µA

[1] In suspend mode, the minimum voltage is 2.7 V.

[2] Maximum value characterized only, not tested in production.

[3] Excluding any load current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typical).

Table 44. Static characteristics: digital pins

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input levels							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.6V_{CC(I/O)}$	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		-	-	0.4	V
		I_{OL} = 100 µA		-	-	0.15	V
V_{OH}	HIGH-level output voltage	I_{OH} = 2 mA	[1]	$V_{CC(I/O)}$ − 0.4	-	-	V
		I_{OH} = 100 µA		$V_{CC(I/O)}$ − 0.15	-	-	V
Leakage current							
I_{LI}	input leakage current			−1	-	+1	µA
Open-drain outputs							
I_{OZ}	off-state output current			−5	-	+5	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	10	pF

[1] Not applicable for open-drain outputs.

Table 45. Static characteristics: analog I/O pins DP and DM

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{DI}	differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	differential common-mode range	includes V_{DI} range	0.8	-	2.5	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	R_L of 1.5 kΩ to +3.6 V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L of 15 kΩ to GND				
		V_{CC} = 3.0 V to 4.5 V	2.8	-	3.6	V
		V_{CC} = 2.7 V to 3.0 V	2.6	-	3.0	V
Leakage current						
I_{LZ}	off-state leakage current		−1	-	+1	μA
Capacitance						
C_{in}	input capacitance	pin to GND	-	-	10	pF
Resistance						
$R_{DN(DP)}$	pull-down resistance on pin DP		14.25	-	24.8	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM		14.25	-	24.8	kΩ
$R_{UP(DP)}$	pull-up resistance on pin DP	bus idle	900	-	1575	Ω
		bus driven	1425	-	3090	Ω
$R_{UP(DM)}$	pull-up resistance on pin DM	bus idle	900	-	1575	Ω
		bus driven	1425	-	3090	Ω
Z_{DRV}	driver output impedance	steady-state drive [1]	34	-	44	Ω
Z_{INP}	input impedance		10	-	-	MΩ
Termination						
V_{TERM}	termination voltage	for the upstream port pull-up resistor (R_{PU})	3.0	-	3.6	V

[1] Includes external series resistors of 33 Ω ± 1 % each on DP and DM.

Table 46. Static characteristics: analog I/O pin ID

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Resistance						
$R_{UP(ID)}$	ID pull-up resistance	on pin ID to VREG3V3	77	-	130	kΩ
$R_{DN(ID)}$	pull-down resistance on pin ID	bit ID_PULLDOWN = 1	-	-	10	Ω
R_{A_ID}	A-device ID impedance to GND	bit ID_GND = 1	-	-	1	kΩ
R_{B_ID}	B-device ID impedance to GND	bit ID_FLOAT = 1	800	-	-	kΩ
R_{ACC_ID}	accessory device ID impedance to GND	bit ID_GND = 0; bit ID_FLOAT = 0	20	-	200	kΩ

Table 47. Static characteristics: charge pump

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Current						
I_{load}	load current	C_{ext} = 100 nF; V_{BUS} = 4.65 V	8.0	-	-	mA
Voltage						
$V_{O(VBUS)}$	output voltage on pin V_{BUS}	I_{load} = 8 mA; C_{ext} = 100 nF	4.65	5	5.25	V
$V_{L(VBUS)}$	leakage voltage on pin V_{BUS}	charge pump disabled	-	-	0.2	V
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	4.65	V
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V
$V_{hys(B\_SESS\_END)}$	B-device session end hysteresis voltage		-	150	-	mV
$V_{A\_SESS\_VLD}$	A-device session valid voltage		0.8	-	2.0	V
$V_{hys(A\_SESS\_VLD)}$	A-device session valid hysteresis voltage		-	200	-	mV
$V_{B\_SESS\_VLD}$	B-device session valid voltage		2.0	-	4.0	V
$V_{hys(B\_SESS\_VLD)}$	B-device session valid hysteresis voltage		-	200	-	mV
η_{cp}	charge pump efficiency	I_{load} = 8 mA; V_{CC} = 3 V	-	75	-	%
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to VREG3V3 when VBUS_CHRG = 1	460	-	1000	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when VBUS_DISCHRG = 1	660	-	1200	Ω
$R_{I(idle)(VBUS)(A)}$	idle input resistance on pin V_{BUS} (A-device)	ID pin connected to GND	40	-	100	kΩ

16. Dynamic characteristics

Table 48. Dynamic characteristics: reset and clock

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset						
$t_{W(RESET\_N)}$	external RESET_N pulse width		10	-	-	µs
Internal clock						
f_{clk}	clock frequency	bit GLOBAL_PWR_DN = 0	700	1000	1300	kHz

Table 49. Dynamic characteristics: digital I/O pins

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TOI}	bus turnaround time (O/I)	OE_N/INT_N to DAT/VP and SE0/VM; see Figure 20	0	-	5	ns
t_{TIO}	bus turnaround time (I/O)	OE_N/INT_N to DAT/VP and SE0/VM; see Figure 20	0	-	5	ns

Table 50. Dynamic characteristics: analog I/O pins DP and DM

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
t_{FR}	rise time	C_L = 50 pF to 125 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 16		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF to 125 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 16		4	-	20	ns
FRFM	differential rise time/fall time matching	excluding the first transition from idle state	[1]	90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from idle state; see Figure 17	[2]	1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	DAT/VP, SE0/VM to DP, DM; see Figure 17 and Figure 21		-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	DAT/VP, SE0/VM to DP, DM; see Figure 17 and Figure 21		-	-	18	ns
t_{PHZ}	driver disable delay from HIGH level	OE_N/INT_N to DP, DM; see Figure 18 and Figure 22		-	-	15	ns
t_{PLZ}	driver disable delay from LOW level	OE_N/INT_N to DP, DM; see Figure 18 and Figure 22		-	-	15	ns

Table 50. Dynamic characteristics: analog I/O pins DP and DM *...continued*

V_{CC} = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}	driver enable delay to HIGH level	OE_N/INT_N to DP, DM; see Figure 18 and Figure 22	-	-	15	ns
t_{PZL}	driver enable delay to LOW level	OE_N/INT_N to DP, DM; see Figure 18 and Figure 22	-	-	15	ns
Receiver timing						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RCV; see Figure 19 and Figure 23	-	-	15	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RCV; see Figure 19 and Figure 23	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to VP and DAT/VP, VM and SE0/VM; see Figure 19 and Figure 23	-	-	18	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to VP and DAT/VP, VM and SE0/VM; see Figure 19 and Figure 23	-	-	18	ns

[1] t_{FR} / t_{FF}.

[2] Characterized only; not tested. Limits guaranteed by design.

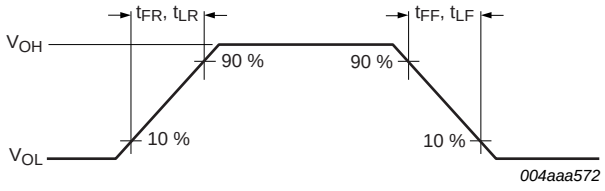


Fig 16. Rise time and fall time

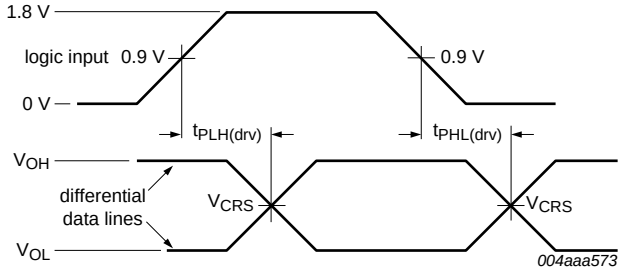


Fig 17. Timing of DAT/VP and SE0/VM to DP and DM

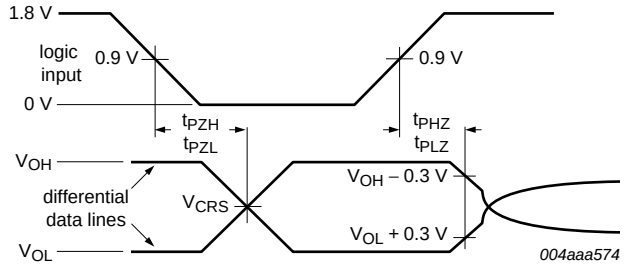


Fig 18. Timing of OE_N/INT_N to DP and DM

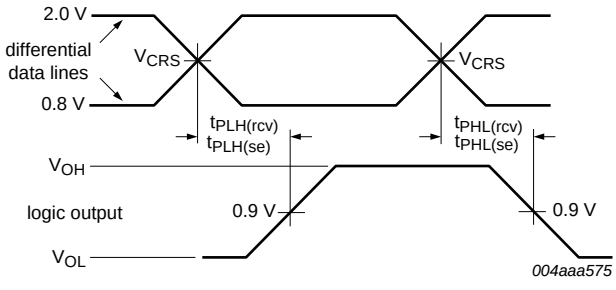


Fig 19. Timing of DP and DM to RCV, VP or DAT/VP and VM or SE0/VM

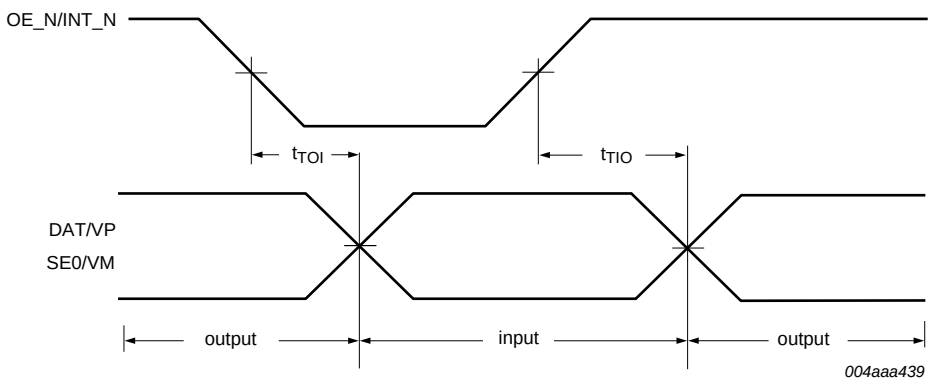
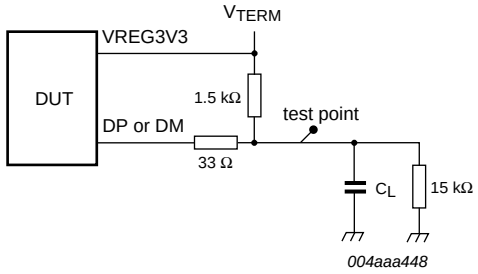
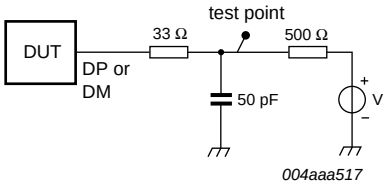


Fig 20. SIE interface bus turnaround timing



Load capacitance C_L = 50 pF (minimum or maximum timing).

Fig 21. Load on pins DP and DM



V = 0 V for t_{PZH} and t_{PHZ}.

V = VREG3V3 for t_{PZL} and t_{PLZ}.

Fig 22. Load on pins DP and DM for enable time and disable time

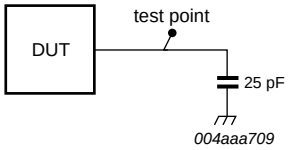


Fig 23. Load on pins VM, SE0/VM, VP, DAT/VP and RCV

Table 51. Characteristics of I²C-bus lines (SDA, SCL)

Symbol	Parameter	Conditions	Standard mode		Unit
			Min	Max	
f_{SCL}	SCL clock frequency		-	100	kHz
$t_{HD;STA}$	hold time for the START condition		4.0	-	µs
$t_{(SCL)L}$	LOW period of the SCL clock		4.7	-	µs
$t_{(SCL)H}$	HIGH period of the SCL clock		4.0	-	µs
$t_{SU;STA}$	setup time for the START condition		4.7	-	µs
$t_{SU;DAT}$	data setup time		250	-	ns
$t_{HD;DAT}$	data hold time		0	-	µs
t_r	rise time	SDA and SCL signals	-	1000	ns
t_f	fall time	SDA and SCL signals	-	300	ns
$t_{SU;STO}$	STOP condition setup time		4.0	-	µs
t_{BUF}	bus free time between a STOP and START condition		4.7	-	µs

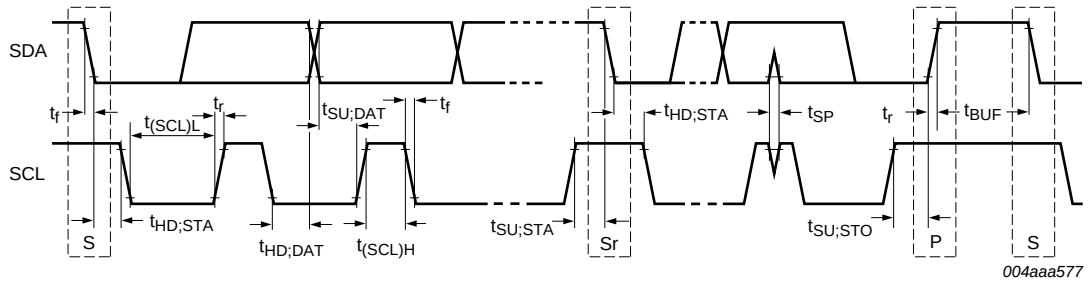


Fig 24. Definition of timing for standard-mode devices on the I²C-bus

17. Application information

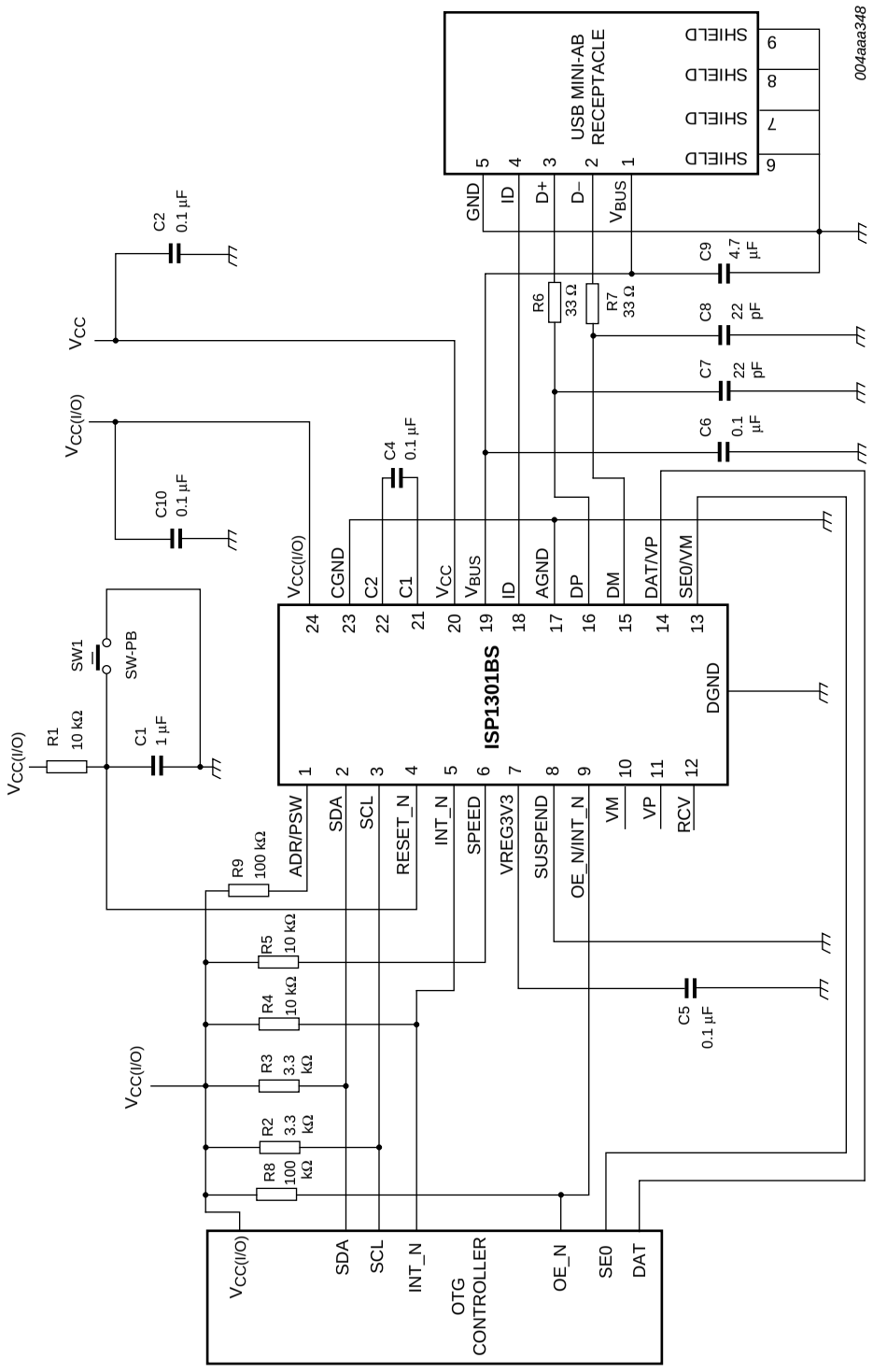


Fig 25. Application diagram for the OTG Controller with the DAT_SE0 SIE interface

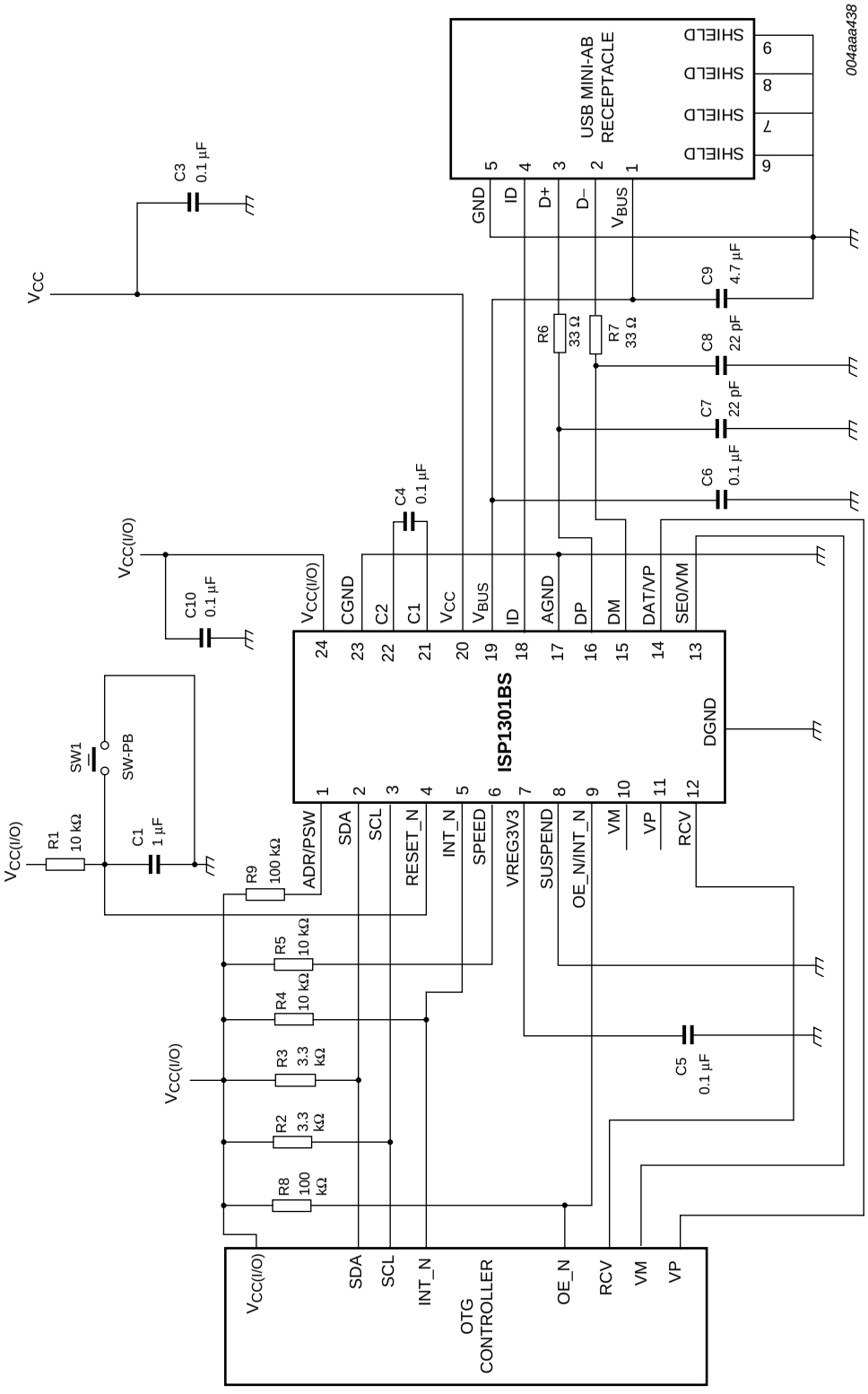
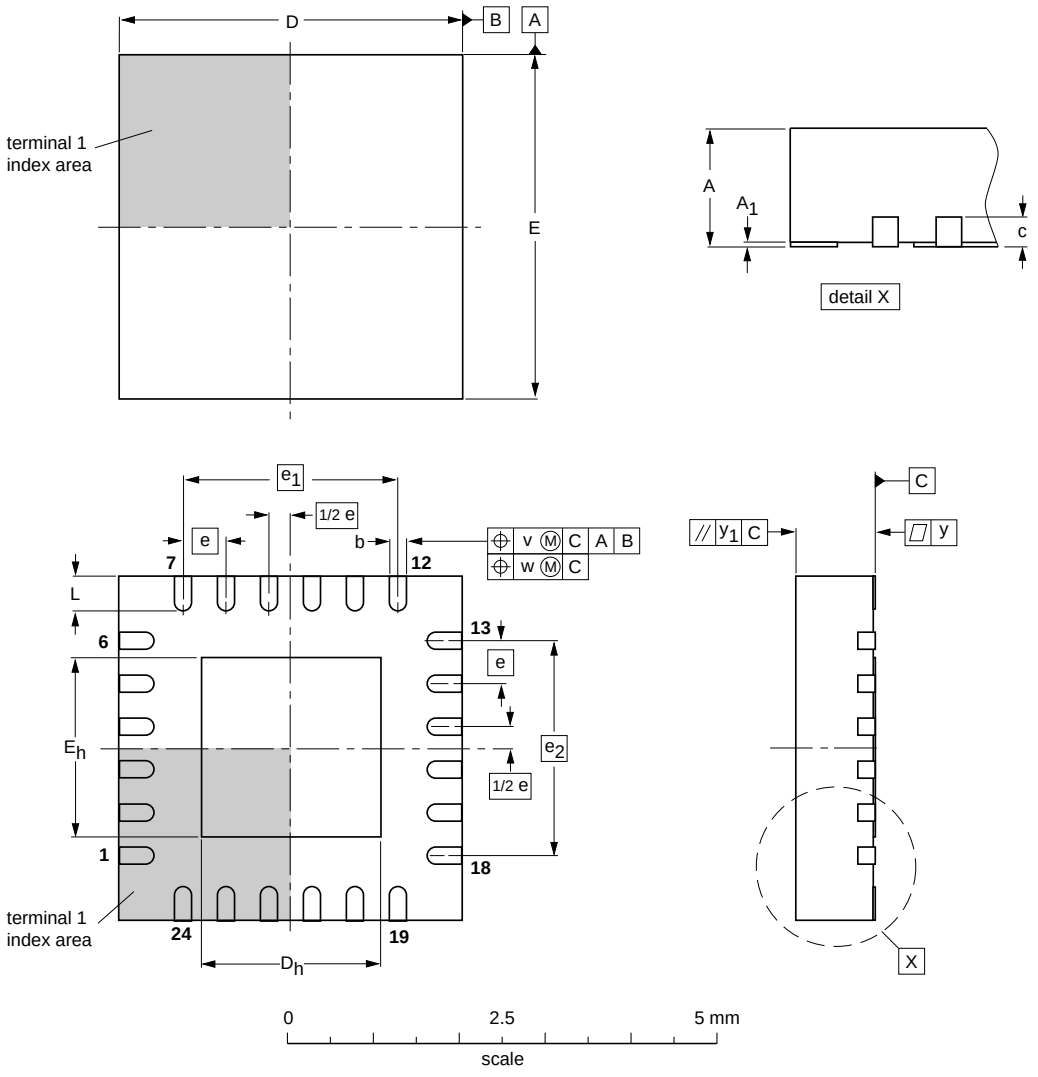


Fig 26. Application diagram for the OTG Controller with the VP_VM SIE interface

18. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 27. Package outline SOT616-1 (HVQFN24)

19. Abbreviations

Table 52. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
ATX	Analog USB Transceiver
HNP	Host Negotiation Protocol
ESD	ElectroStatic Discharge
I^2C-bus	Inter IC-bus
IC	Integrated Circuit
LSB	Least Significant Bit
OTG	On-The-Go
PDA	Personal Digital Assistant
PLD	Programmable Logic Device
POR	Power-On Reset
PORP	Power-On Reset Pulse
SE0	Single-Ended Zero
SOF	Start-Of-Frame
SRP	Session Request Protocol
USB	Universal Serial Bus
USB-IF	USB Implementers Forum

20. References

[1] ECN_27%_Resistor (Pull-up/pull-down Resistors ECN)

[2] Universal Serial Bus Specification Rev. 2.0

[3] On-The-Go Supplement to the USB Specification Rev. 1.0a

[4] On-The-Go Transceiver Specification (CEA-2011) Rev. 1.0

[5] The I2C-bus specification; version 2.1

21. Revision history

Table 53. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1301_5	20090902	Product data sheet	-	ISP1301_4
Modifications:	Table 1 “Ordering information”: updated.			
ISP1301_4	20090624	Product data sheet	-	ISP1301_3
ISP1301_3	20060221	Product data sheet	-	ISP1301-02
ISP1301-02 (9397 750 14337)	20050104	Product data	-	ISP1301-01
ISP1301-01 (9397 750 11355)	20040414	Product data	-	-

22. Tables

23. Figures

24. Contents

continued >>

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