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As from February 2nd 2009, ST and Ericsson have merged Ericsson Mobile Platforms and ST-NXP Wireless into a 50/50 joint venture "ST-Ericsson".
As a result, the following changes are applicable to the attached document.

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ISP1705

ULPI Hi-Speed USB transceiver

Rev. 02 — 21 January 2009   **Product data sheet**

1. General description

The ISP1705 is a UTMI+ Low Pin Interface (ULPI) Hi-Speed Universal Serial Bus (USB) transceiver that is fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

The ISP1705 can transmit and receive USB data at high speed (480 Mbit/s), full speed (12 Mbit/s) and low speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to the USB host, peripheral or OTG controller with Single Data Rate (SDR) or Dual Data Rate (DDR) ULPI link. The ISP1705 can transparently transmit and receive UART signaling.

It is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) or any system chip set to interface with the physical layer of the USB through an 8-pin (DDR) or 12-pin (SDR) interface.

The ISP1705 can interface to devices with digital I/O voltages in the range of 3.0 V to 3.6 V.

The ISP1705 is available in HVQFN36 and TFBGA36 packages.

2. Features

- Fully complies with:
  - ◆ USB: *Universal Serial Bus Specification Rev. 2.0*
  - ◆ OTG: *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
  - ◆ ULPI: *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
- Interfaces to USB host, peripheral or OTG cores; optimized for portable devices or system ASICs with built-in ULPI link
- Complete Hi-Speed USB physical front-end solution that supports high speed (480 Mbit/s), full speed (12 Mbit/s) and low speed (1.5 Mbit/s)
  - ◆ Integrated 45 $\Omega \pm 10$ % high-speed termination resistors, 1.5 k$\Omega \pm 5$ % full-speed device pull-up resistor, and 15 k$\Omega \pm 5$ % host termination resistors
  - ◆ Integrated parallel-to-serial and serial-to-parallel converters to transmit and receive
  - ◆ USB clock and data recovery to receive USB data up to ±500 ppm
  - ◆ Insertion of stuff bits during transmit and discarding of stuff bits during receive
  - ◆ Non-Return-to-Zero Inverted (NRZI) encoding and decoding
  - ◆ Supports bus reset, suspend, resume and high-speed detection handshake (chirp)

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■ Complete USB OTG physical front-end that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)

◆ Supports external charge pump or external V_{BUS} power switch

◆ Complete control over USB termination resistors

◆ Data line and V_{BUS} pulsing session request methods

◆ Integrated V_{BUS} voltage comparators

◆ Integrated cable (ID) detector

■ Flexible system integration and very low power consumption, optimized for portable devices

◆ 3.0 V to 4.5 V supply voltage input range

◆ Internal voltage regulator supplies 2.7 V or 3.3 V and 1.8 V

◆ Supports interfacing I/O voltage of 3.0 V to 3.6 V; separate I/O voltage supply pins minimize crosstalk

◆ Power down internal regulators in Power-down mode when $V_{CC(I/O)}$ is not present or when the chip is not selected

◆ Typical operating current of 13 mA to 32 mA, depending on the USB speed and bus utilization

◆ Typical current consumption I_{CC} is 70 μA for host and 240 μA for peripheral in suspend mode, and 0.5 μA in Power-down mode

◆ 3-state ULPI interface by the CHIP_SEL or CHIP_SEL_N pin, allowing bus reuse by other applications

■ Highly optimized ULPI compliant

◆ 60 MHz, 8-pin or 12-pin interface between the core and the transceiver, including a 4-bit DDR bus or an 8-bit SDR bus

◆ DDR or SDR interface selectable by pin

◆ Supports 60 MHz output clock configuration

◆ Integrated Phase-Locked Loop (PLL) supporting input clock frequencies of 13 MHz, 19.2 MHz, 24 MHz or 26 MHz

◆ Crystal or clock frequency selectable by pin

◆ Fully programmable ULPI-compliant register set

◆ 3-pin or 6-pin full-speed or low-speed serial mode

◆ Internal Power-On Reset (POR) circuit

■ UART interface:

◆ Supports transparent UART signaling on the DP and DM pins for the UART accessory application

◆ 2.7 V UART signaling on the DP and DM pins

◆ Entering UART mode by register setting

◆ Exiting UART mode by asserting STP or by toggling the CHIP_SEL or CHIP_SEL_N pin

■ Full industrial grade operating temperature range from −40 °C to +85 °C

■ ESD compliance:

◆ JESD22-A114D ±2 kV contact Human Body Model (HBM)

◆ JESD22-A115-A ±200 V Machine Model (MM)

◆ JESD22-C101-C ±500 V Charged Device Model (CDM)

◆ IEC 61000-4-2 ±8 kV contact on the DP and DM pins

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■ Available in small HVQFN36 and TFBGA36 Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free packages

3. Applications

■ Digital still camera

■ Digital TV

■ Digital Video Disc (DVD) recorder

■ External storage device, for example:

◆ Magneto-Optical (MO) drive

◆ Optical drive (CD-ROM, CD-RW, CD-DVD)

◆ Zip drive

■ Mobile phone

■ MP3 player

■ PDA

■ Printer

■ Scanner

■ Set-Top Box (STB)

■ Video camera

4. Ordering information

Table 1.   Ordering information

Type number	Package		
	Name	**Description**	**Version**
ISP1705HN	HVQFN36	plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body $5 \times 5 \times 0.85$ mm	SOT818-1
ISP1705AET	TFBGA36	plastic thin fine-pitch ball grid array package; 36 balls; body $3.5 \times 3.5 \times 0.8$ mm	SOT912-1

5. Marking

Table 2.   Marking codes

Type number	Marking code[1]
ISP1705HN	1705
ISP1705AET	705A

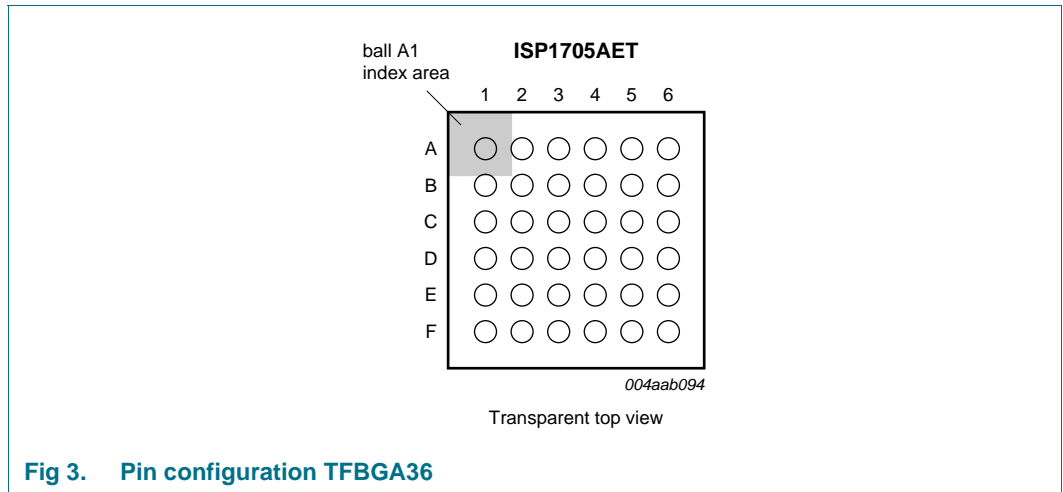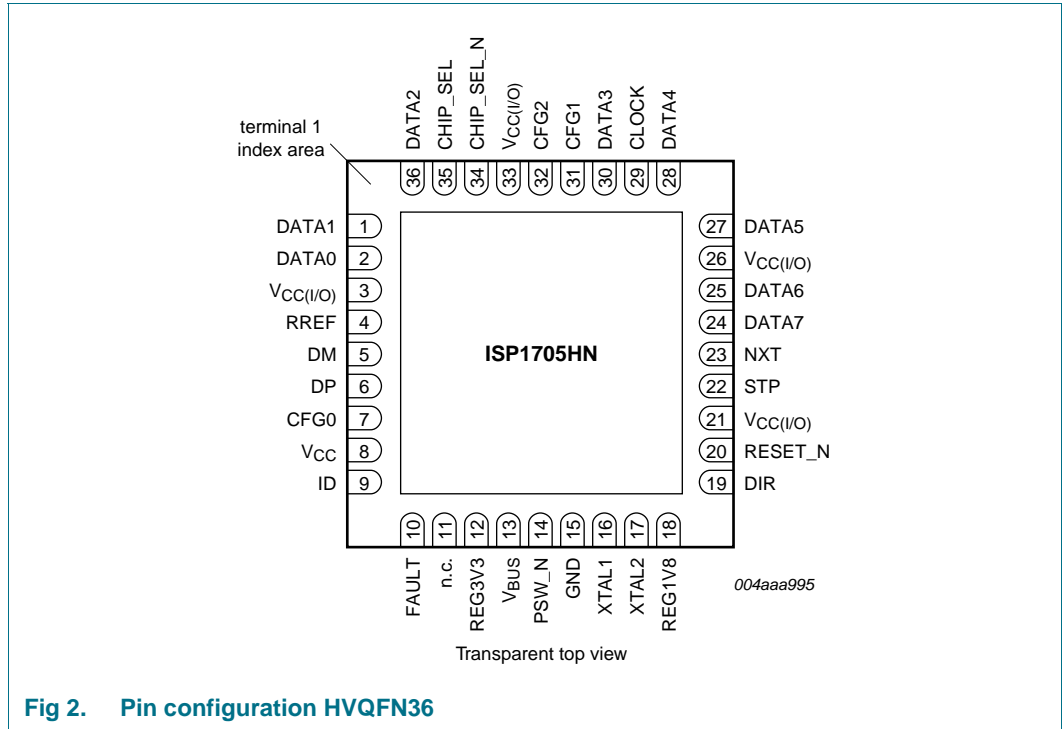[1]   The package marking is the first line of text on the IC package and can be used for IC identification.

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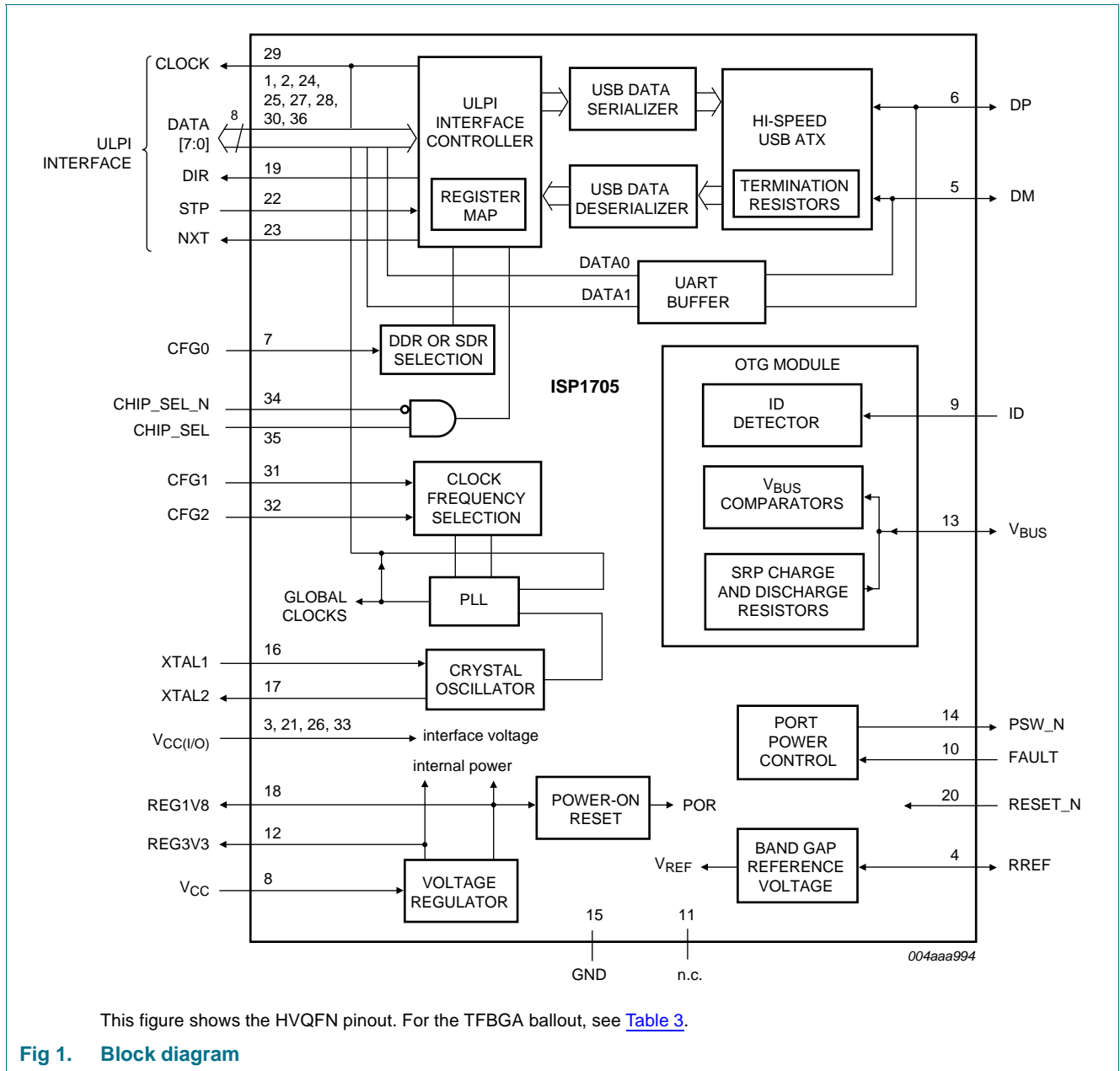
6. Block diagram

This figure shows the HVQFN pinout. For the TFBGA ballout, see Table 3.

Fig 1.   Block diagram

7. Pinning information

7.1 Pinning

Fig 2. Pin configuration HVQFN36

Fig 3. Pin configuration TFBGA36

7.2 Pin description

Table 3. **Pin description**

Symbol[1]	Pin		Type[2]	Description[3]
	HVQFN36 (ISP1705HN)	**TFBGA36 (ISP1705AET)**		
DATA1	1	A1	I/O	ULPI data pin 1 3-state output; plain input
DATA0	2	B1	I/O	ULPI data pin 0 3-state output; plain input
$V_{CC(I/O)}$	3	B2	P	input I/O supply voltage; 3.0 V to 3.6 V; a 0.1 µF decoupling capacitor is recommended
RREF	4	C2	AI/O	resistor reference; connect through a 12 kΩ ± 1 % resistor to GND
DM	5	C1	AI/O	connect to the D− pin of the USB connector • USB mode: D− input or output • UART mode: TXD output
DP	6	D1	AI/O	connect to the D+ pin of the USB connector • USB mode: D+ input or output • UART mode: RXD input During UART mode, an internal 125 kΩ ± 20 % pull-up resistor is present on this pin.
CFG0	7	E1	I	select SDR or DDR ULPI interface: • SDR: connect this pin to GND • DDR: connect this pin to REG3V3 plain input; TTL
V_{CC}	8	F3	P	input supply voltage or battery source; 3.0 V to 4.5 V **Remark:** Below 3.0 V, USB full-speed and low-speed transactions are not guaranteed to work, though some devices may work with the ISP1705 at these voltages.
ID	9	D3	I	identification (ID) pin of the micro-USB connector; if this pin is not in use, connect it directly to the REG3V3 pin (an internal 400 kΩ pull-up resistor is present on this pin) plain input; TTL
FAULT	10	E2	I	input for the V_{BUS} digital overcurrent or fault detector signal; if this pin is not in use, connect it to GND plain input; 5 V tolerant
n.c.	11	F1, F2	-	not connected
REG3V3	12	E3	P	3.3 V regulator output for USB mode or 2.7 V regulator output for UART mode; requires parallel 0.1 µF and 4.7 µF capacitors; internally powers ATX and other analog circuits; must not be used to power external circuits
V_{BUS}	13	F4	AI/O	connect to the V_{BUS} pin of the USB connector; if this pin is not in use, leave it open ($R_{I(idle)(VBUS)}$ is present on this pin)
PSW_N	14	D4	OD	active-LOW external V_{BUS} power switch or external charge pump enable open-drain output; 4 mA current sinking capability; 5 V tolerant
GND	15	C5, D2, E4	-	ground

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Table 3.   **Pin description** …*continued*

Symbol[1]	Pin		Type[2]	Description[3]
	HVQFN36 (ISP1705HN)	TFBGA36 (ISP1705AET)		
XTAL1	16	F5	AI/O	crystal oscillator or clock input; 1.8 V peak input allowed; frequency depends on status on the CFG1 pin
XTAL2	17	F6	AI/O	crystal oscillator output; when a crystal oscillator is used, leave this pin open
REG1V8	18	E6	P	1.8 V regulator output; requires parallel 0.1 μF and 4.7 μF capacitors; internally powers the digital core; must not be used to power external circuits
DIR	19	E5	O	ULPI direction signal 3-state output
RESET_N	20	C4	I	active-LOW, asynchronous reset input plain input
$V_{CC(I/O)}$	21	B5	P	input I/O supply voltage; 3.0 V to 3.6 V; a 0.1 μF decoupling capacitor is recommended
STP	22	D6	I	ULPI stop signal plain input
NXT	23	D5	O	ULPI next signal 3-state output
DATA7	24	C6	I/O	ULPI data pin 7 3-state output; plain input
DATA6	25	B6	I/O	ULPI data pin 6 3-state output; plain input
$V_{CC(I/O)}$	26	-	P	input I/O supply voltage; 3.0 V to 3.6 V; a 0.1 μF decoupling capacitor is recommended
DATA5	27	A6	I/O	ULPI data pin 5 3-state output; plain input
DATA4	28	A5	I/O	ULPI data pin 4 3-state output; plain input
CLOCK	29	A4	O	60 MHz clock output when crystal is attached or clock is applied on the XTAL1 pin 3-state output
DATA3	30	A3	I/O	ULPI data pin 3 3-state output; plain input
CFG1	31	B4	I	select crystal or clock frequency with CFG2; see Table 6 plain input
CFG2	32	B3	I	select crystal or clock frequency with CFG1; see Table 6 plain input
$V_{CC(I/O)}$	33	-	P	input I/O supply voltage; 3.0 V to 3.6 V; a 0.1 μF decoupling capacitor is recommended
CHIP_SEL_N	34	C3	I	active-LOW chip select input; when this pin is not in use, connect it to GND plain input

Table 3. **Pin description** *…continued*

Symbol[1]	Pin		Type[2]	Description[3]
	HVQFN36 (ISP1705HN)	**TFBGA36 (ISP1705AET)**		
CHIP_SEL	35	-	I	active-HIGH chip select input; when this pin is not in use, connect it to $V_{CC(I/O)}$ plain input
DATA2	36	A2	I/O	ULPI data pin 2 3-state output; plain input
GND	exposed die pad	-	P	ground

[1] Symbol names ending with underscore N (for example, NAME_N) indicate active-LOW signals.

[2] I = input; O = output; I/O = digital input/output; OD = open-drain output; AI/O = analog input/output; P = power supply or ground pin.

[3] A detailed description of these pins can be found in Section 8.12.

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8. Functional description

8.1 ULPI interface controller

The ISP1705 provides a 12-pin interface that is compliant with *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*. This interface must be connected to a USB link.

The ULPI interface controller provides the following functions:

- ULPI-compliant interface and register set
- Allows full control over the USB peripheral or host functionality
- Parses the USB transmit and receive data
- Prioritizes the USB receive data, USB transmit data, interrupts and register operations
- Low-power mode
- Transparent UART mode
- 3-pin serial mode
- 6-pin serial mode
- Generates RXCMDs (status updates)
- Maskable interrupts

For more information on the ULPI protocol, see Section 10.

8.2 USB serializer and deserializer

The USB data serializer prepares data to transmit on the USB bus. To transmit data, the USB link sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing and NRZI encoding. For packets with a PID, the serializer adds a SYNC pattern to the start of the packet, and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept any more data, the ULPI interface controller deasserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, and then performs serial-to-parallel conversion, NRZI decoding and discarding of stuff bits on the data payload. The ULPI interface controller sends data to the USB link by asserting DIR, and then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit stuff errors, elasticity buffer underrun or overrun, and byte-alignment errors.

8.3 Hi-Speed USB (USB 2.0) ATX

The Hi-Speed USB ATX block is an analog front-end containing the circuitry needed to transmit, receive and terminate the USB bus in high speed, full speed and low speed, for USB peripheral, host or OTG implementations. The following circuitry is included:

- Differential drivers to transmit data at high speed, full speed and low speed
- Differential and single-ended receivers to receive data at high speed, full speed and low speed
- Squelch circuit to detect high-speed bus activity

- High-speed disconnect detector
- 45 Ω high-speed bus terminations on pins DP and DM
- 1.5 kΩ pull-up resistor on pin DP
- 15 kΩ bus terminations on pins DP and DM

For details on controlling resistor settings, see Table 15.

8.4 Voltage regulator

The ISP1705 contains a built-in voltage regulator that conditions the V_{CC} supply for use inside the ISP1705. The voltage regulator:

- Supports input supply range 3.0 V < V_{CC} < 4.5 V.
- Can be supplied from a battery with the voltage range mentioned above.
- Supplies internal digital circuitry with 1.8 V and analog circuitry with 3.3 V or 2.7 V.
- In USB mode, automatically bypasses the internal 3.3 V regulator when V_{CC} < 3.5 V: the internal analog circuitry directly draws power from the V_{CC} pin. In UART mode, the bypass switch will be disabled.
- Will be shut down when $V_{CC(I/O)}$ is not present or when chip select is deasserted.

8.5 Crystal oscillator and PLL

The ISP1705 has a built-in crystal oscillator and a Phase-Locked Loop (PLL) for clock generation. When a crystal is in use, the built-in crystal oscillator generates a square wave clock for internal use. A square wave clock of the same frequency can also be driven directly into the XTAL1 pin. Using an existing square wave clock can save the cost of a crystal and also reduce the board space. The crystal or clock frequencies supported are 13 MHz, 19.2 MHz, 24 MHz and 26 MHz.

The PLL takes the square wave clock from the crystal oscillator and multiplies or divides it into various frequencies for internal use.

The PLL produces the following frequencies, irrespective of the clock source:

- 1.5 MHz for low-speed USB data
- 12 MHz for full-speed USB data
- 60 MHz clock for the ULPI interface controller
- 480 MHz for high-speed USB data
- Other internal frequencies for data conversion and data recovery

8.6 UART buffer

The UART buffer includes circuits to support the transparent UART signaling between the DATA0 or DATA1 pin and the DM or DP pin.

When the ISP1705 is put into UART mode, it acts as a voltage level shifter between the following pins:

- From DATA0 ($V_{CC(I/O)}$ level) to DM (2.7 V level) for the UART TXD signaling path.
- From DP (2.7 V level) to DATA1 ($V_{CC(I/O)}$ level) for the UART RXD signaling path.

8.7 OTG module

This module contains several sub-blocks that provide all the functionality required by the USB OTG specification. Specifically, it provides the following circuits:

- The ID detector to sense the ID pin of the micro-USB cable. The ID pin dictates which device is initially configured as a host and which as a peripheral.
- V_{BUS} comparators to determine the V_{BUS} voltage level. This is required for the V_{BUS} detection, SRP and HNP.
- Resistors to temporarily charge and discharge V_{BUS}. This is required for SRP.

8.7.1 ID detector

The ID detector detects which end of the micro-USB cable is plugged in. The ID detector must first be enabled by setting the ID_PULLUP register bit to logic 1. If the ISP1705 senses a state of the ID pin that is different from the previously reported state, an RXCMD status update will be sent to the USB link, or an interrupt will be asserted.

- If the micro-B end of the cable is plugged in (or nothing is plugged in), the ISP1705 will report that ID_GND is logic 1. The USB link must be in the B-device state.
- If the micro-A end of the cable is plugged in, the ISP1705 will report that ID_GND is logic 0. The USB link must be in the A-device state.

The ID pin has a weak pull-up resistor ($R_{weakPU(ID)}$) permanently enabled to avoid the floating condition.

8.7.2 V_{BUS} comparators

The ISP1705 provides three comparators to detect the V_{BUS} voltage level. The comparators are explained in the following subsections.

8.7.2.1 V_{BUS} valid comparator

This comparator is used by hosts and A-devices to determine whether the voltage on V_{BUS} is at a valid level for operation. The ISP1705 minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered invalid. During power-up, it is expected that the comparator output will be ignored.

8.7.2.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Peripherals, A-devices and B-devices use this comparator to detect when a session is started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold of the ISP1705 is between 0.8 V to 2.0 V.

8.7.2.3 Session end comparator

The session end comparator determines when V_{BUS} is below the B-device session end threshold of 0.2 V to 0.8 V. The B-device uses this threshold to determine when a session has ended.

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8.7.3 SRP charge and discharge resistors

The ISP1705 provides on-chip resistors for short-term charging and discharging of V_{BUS}. These are used by the B-device to request a session, prompting the A-device to restore the V_{BUS} voltage. First, the B-device makes sure that V_{BUS} is fully discharged from the previous session by setting the DISCHRG_VBUS register bit to logic 1 and waiting for SESS_END to be logic 1. Then the B-device charges V_{BUS} by setting the CHRG_VBUS register bit to logic 1. The A-device sees that V_{BUS} is charged above the session valid threshold and starts a session by turning on the V_{BUS} voltage.

8.8 Port power control

For an OTG or host application, the ISP1705 uses the PSW_N pin to control the external power switch for the V_{BUS} 5 V supply. The overcurrent detector output of the external power switch can be connected to the FAULT pin of the ISP1705 to indicate to the ULPI link the V_{BUS} overcurrent status. For the connection scheme, see Figure 4.

When the FAULT pin is not used, connect it to GND.
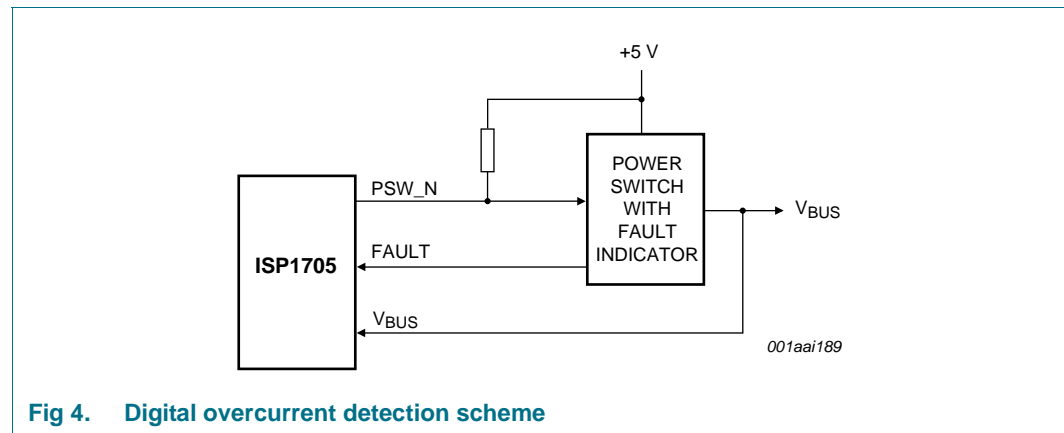
Fig 4. **Digital overcurrent detection scheme**

8.9 Band gap reference voltage

The band gap circuit provides a stable internal voltage reference to bias the analog circuitry. This band gap circuit requires an accurate external reference resistor. Connect a 12 kΩ $\pm$ 1 % resistor between the RREF pin and GND.

8.10 Power-On Reset (POR)

An internal POR pulse is generated when REG1V8 rises above $V_{POR(trip)}$. The internal POR pulse will be generated whenever REG1V8 drops below $V_{POR(trip)}$ for more than $t_{w(REG1V8\_L)}$.

To give a better view of the functionality, Figure 5 shows a possible curve of REG1V8. The internal POR starts with logic 0 at t0. At t1, the detector will see the passing of the trip level so that a POR pulse is generated to reset all internal circuits. If REG1V8 dips from t2 to t3 for greater than $t_{w(REG1V8\_L)}$, another POR pulse is generated. If the dip from t4 to t5 is less than $t_{w(REG1V8\_L)}$, the internal POR pulse will not be generated and will remain LOW.
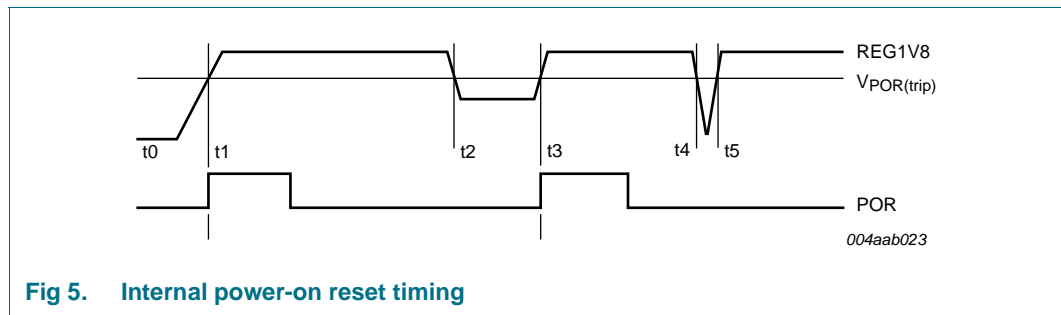
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Fig 5.   Internal power-on reset timing

8.11 Power-up, reset and bus idle sequence

Figure 6 shows a typical start-up sequence.

On power-up, the ISP1705 performs an internal power-on reset and asserts DIR to indicate to the link that the ULPI bus cannot be used. When the internal PLL is stable, the ISP1705 deasserts DIR and drives a 60 MHz clock on the CLOCK pin. The power-up time depends on the V_{CC} supply rise time, the crystal start-up time, and the PLL start-up time $t_{startup(PLL)}$. When DIR is deasserted, the link must drive the data bus to a valid level. By default, the link must drive data to LOW. Before beginning USB packets, the link must set the RESET bit in the FUNC_CTRL register (see Section 11.5) to reset the ISP1705. After the RESET bit is set, the ISP1705 will assert DIR until the internal reset completes. The ISP1705 will automatically deassert DIR and clear the RESET bit when the reset has completed. After every reset, an RXCMD is sent to the link to update USB status information. After this sequence, the ULPI bus is ready for use and the link can start USB operations.

If chip select is non-active, the ISP1705 will be kept in Power-down mode. In Power-down mode, all ULPI interface pins will be put in 3-state, the internal regulator will be shut down, and the total current consumption in Power-down mode will be less than that in low-power mode.

The link can do a hardware reset to the ISP1705 by toggling chip select. The recommended sequence is:

1. De-activate chip select.
2. Wait for at least t_{PWRDN}.
3. Activate chip select.

If the low-power mode is entered when $V_{CC(I/O)}$ is lost, see Table 9.

The recommended power-up sequence for the link is:

1. Apply the V_{CC} and $V_{CC(I/O)}$ voltage.
2. Activate chip select.
3. The link waits for at least t_{PWRUP}, ignoring all the ULPI pin statuses.
4. The link may start to detect the DIR status level. If DIR is detected LOW, the link may send a RESET command.

The ULPI interface is ready for use.
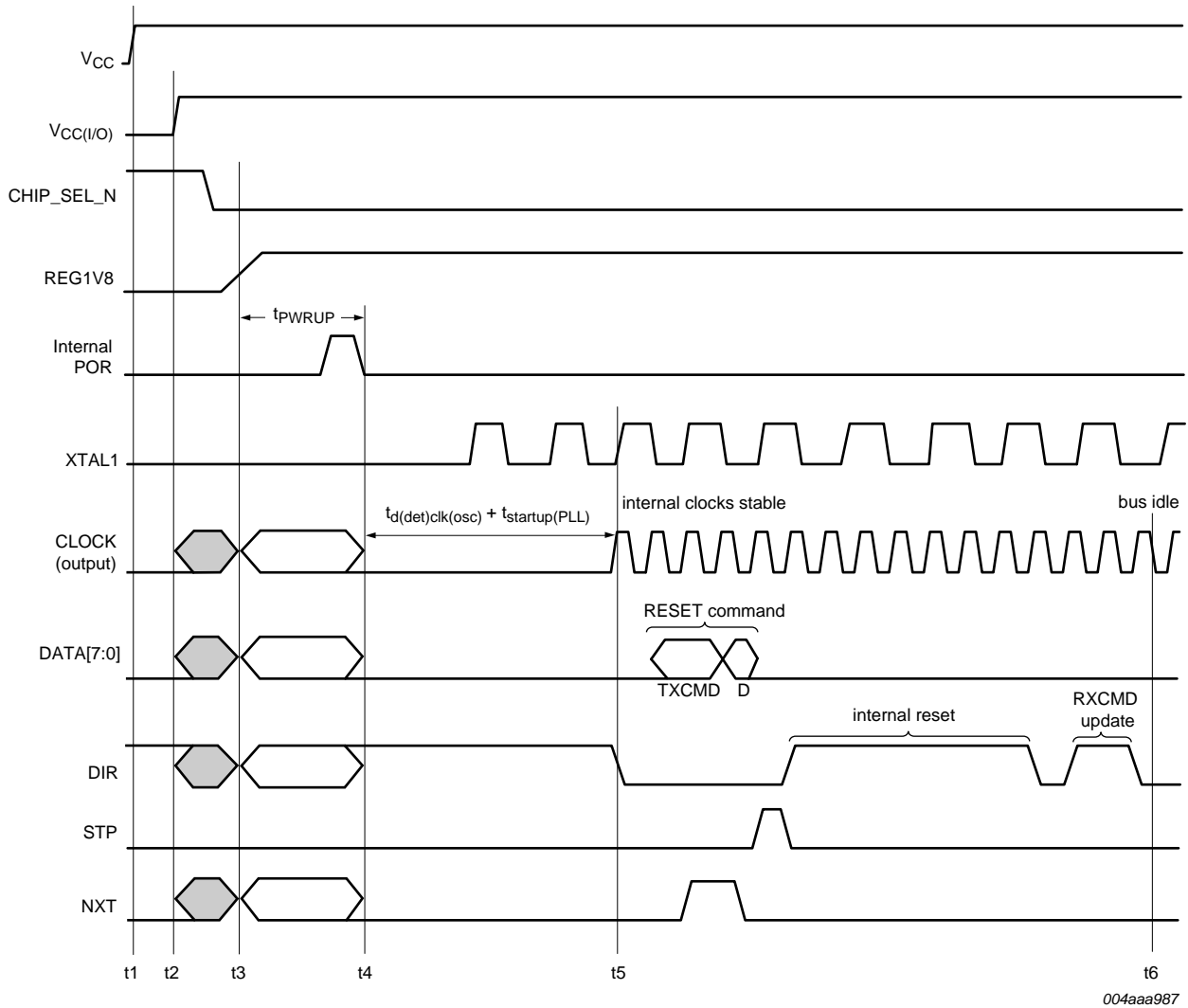
t1 = V_{CC} is applied to the ISP1705.

t2 = $V_{CC(I/O)}$ is turned on. ULPI interface pins CLOCK, DATA[7:0], DIR and NXT are in 3-state as long as chip select is non-active.

t3 = Chip select turns from non-active to active. The ISP1705 regulator starts to turn on. ULPI pads are not in 3-state and may drive to either LOW or HIGH. It is recommended that the link ignores ULPI pins status during t_{PWRUP}.

t4 = Power-on reset threshold is reached and the POR pulse is generated. After the POR pulse, ULPI pins are driven to a defined level. DIR is driven to HIGH and the other pins are driven to LOW.

t5 = The PLL is stabilized after $t_{d(det)clk(osc)} + t_{startup(PLL)}$. The CLOCK pin starts to output 60 MHz. The DIR pin will transition from HIGH to LOW. The link must drive DATA[7:0] and STP to LOW as the idle state. The link will then issue a reset command to initialize the ISP1705.

t6 = The power-up sequence is completed and the ULPI bus interface is ready for use.

Fig 6.   Power-up and reset sequence required before the ULPI bus is ready for use

8.11.1 Interface protection

By default, the ISP1705 enables a weak pull-up resistor on STP. If the STP pin is unexpectedly HIGH at any time, the ISP1705 will protect the ULPI interface by enabling weak pull-down resistors on DATA[7:0].

The interface protect feature prevents unwanted activity of the ISP1705 whenever the ULPI interface is not correctly driven by the link. For example, when the link powers up more slowly than the ISP1705.

The interface protect feature can be disabled by setting the INTF_PROT_DIS bit to logic 1.

8.11.2 Interface behavior with respect to RESET_N during normal mode

The use of the RESET_N pin is optional. When RESET_N is asserted (LOW), all logic in the ISP1705 will be reset, including the analog circuitry and ULPI registers.

During reset, the link must pull down DATA[7:0] to 00h and drive STP to LOW for one cycle before reset assertion until the next rising edge of the clock after reset deassertion, otherwise undefined behavior may result. Ensure that there is no glitch or noise on DATA[7:0] during reset. When RESET_N is deasserted (HIGH), a 60 MHz clock will start and the link must operate the bus according to the ULPI bus protocol.

Figure 7 shows the ULPI interface behavior when RESET_N is asserted (LOW), and subsequently deasserted (HIGH). The behavior of Figure 7 applies only when chip select is asserted. If RESET_N is not used, it must be connected to $V_{CC(I/O)}$.
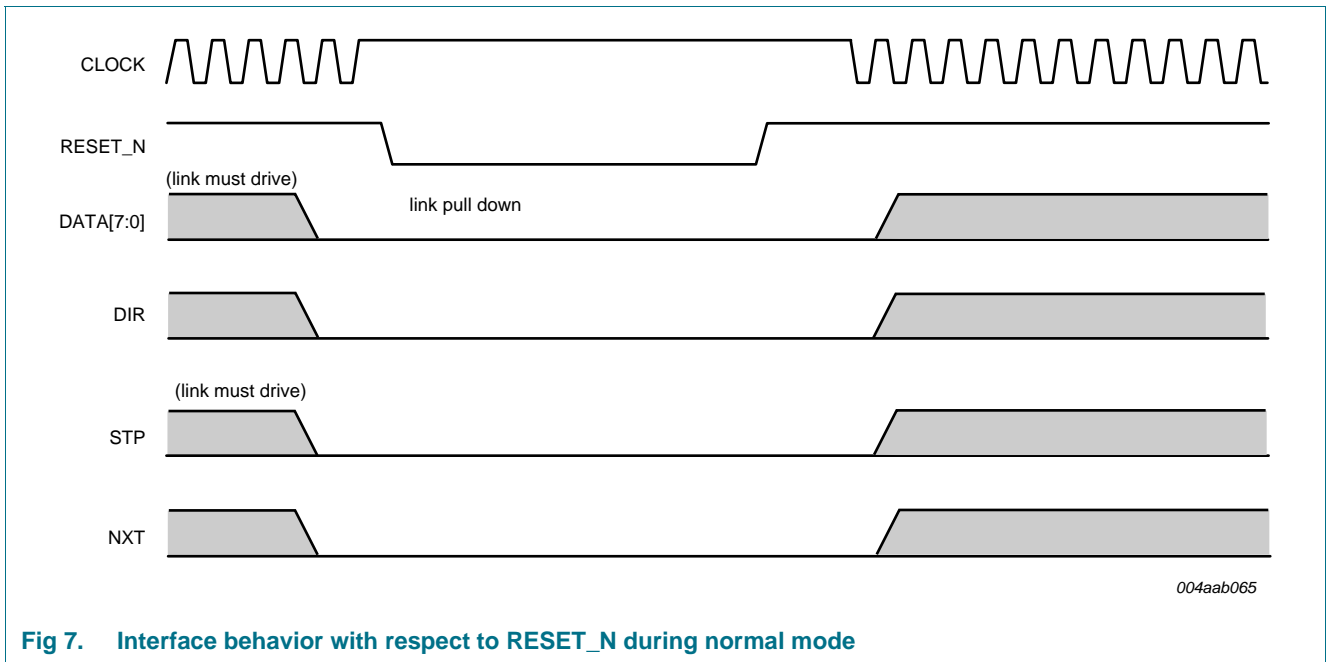

Fig 7. Interface behavior with respect to RESET_N during normal mode

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8.11.3　Interface behavior with respect to chip select

The use of chip select as a power-down control signal is optional. When chip select is deasserted, the ISP1705 will 3-state ULPI pins and power-down the internal circuitry. If chip select is not used as a power-down control signal, CHIP_SEL_N must be connected to LOW. Figure 8 shows the ULPI interface behavior when chip select is asserted and subsequently deasserted.

Fig 8.　Interface behavior with respect to chip select
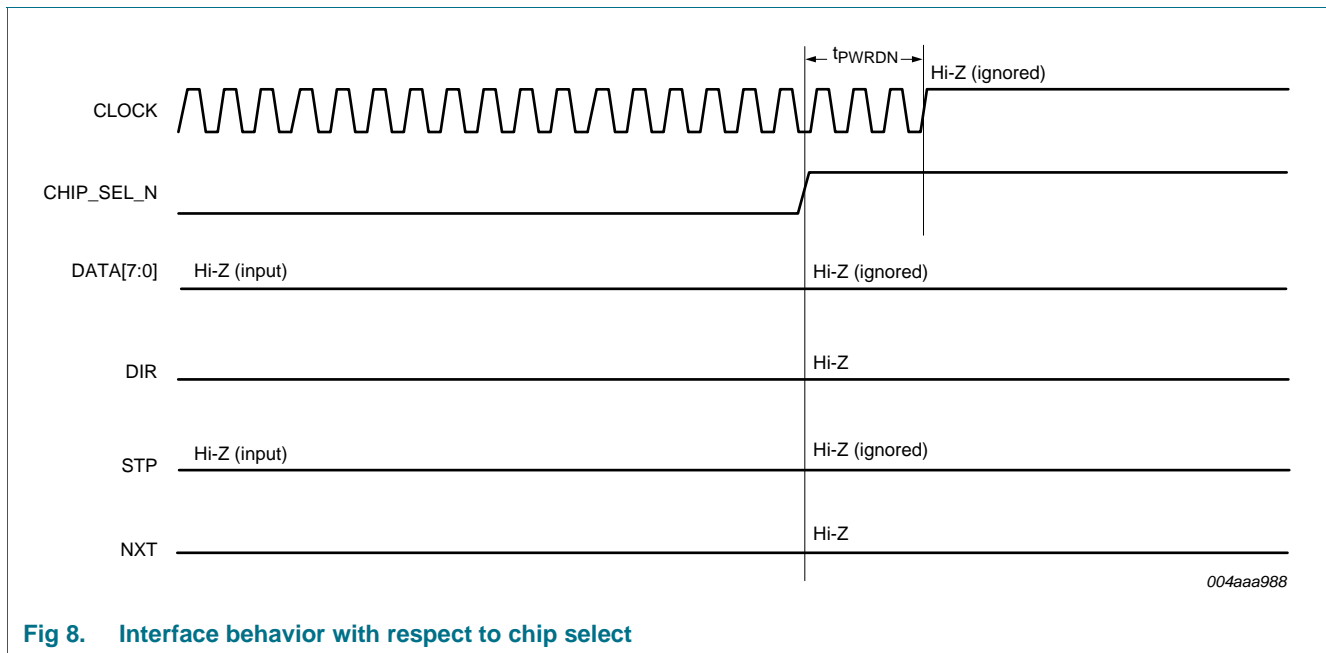
8.12　Detailed description of pins

8.12.1　DATA[7:0]

Bidirectional data bus pins. The USB link must drive DATA[7:0] to LOW when the ULPI bus is idle. When the link has data to transmit to the PHY, it drives a nonzero value. Weak pull-down resistors are incorporated into DATA[7:0] pins as part of the interface protect feature. For details, see Section 8.11.1.

DATA[7:0] pins can also be 3-stated when chip select is deasserted.

These pins can be reconfigured to carry various data types when the chip is not in synchronous mode. For details, see Section 9.2.

8.12.2　$V_{CC(I/O)}$

The input supply power pin that sets the I/O voltage level. A 0.1 μF decoupling capacitor is recommended on each $V_{CC(I/O)}$ pin. $V_{CC(I/O)}$ powers the on-chip pads of the following pins:

- CFG1
- CFG2
- CHIP_SEL
- CHIP_SEL_N
- CLOCK

- DATA[7:0]
- DIR
- NXT
- STP
- RESET_N

8.12.3 RREF

Resistor reference analog I/O pin. A 12 kΩ ± 1 % resistor must be connected between the RREF pin and GND. This provides an accurate voltage reference that biases internal analog circuitry. Less accurate resistors cannot be used. It will affect the biasing current for analog circuits, thus the USB signal quality.

8.12.4 DP and DM

When the ISP1705 is in USB mode, the DP pin functions as the USB data plus line, and the DM pin functions as the USB data minus line.

When the ISP1705 is in transparent UART mode, the DP pin functions as the UART RXD input pin, and the DM pin functions as the UART TXD output pin.

The DP and DM pins must be connected to the D+ and D− pins of the USB receptacle.

8.12.5 CFG0

This input pin is used to select the SDR or DDR interface. For the SDR interface, connect this pin to GND. For the DDR interface, connect this pin to REG3V3.

8.12.6 V_{CC}

Main input supply voltage for the ISP1705. The ISP1705 operates correctly when V_{CC} is between 3.0 V and 4.5 V. A 0.1 μF decoupling capacitor is recommended.

8.12.7 ID

For OTG applications, the ID (identification) pin is connected to the ID pin of the micro-AB receptacle. As defined in *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*, the ID pin dictates the initial role of the link. If ID is detected as HIGH, the link must assume the role of a peripheral. If ID is detected as LOW, the link must assume a host role. Roles can be swapped at a later time by using HNP.

The ISP1705 provides an internal pull-up resistor ($R_{UP(ID)}$) to sense the state of the ID pin. The pull-up resistor must first be enabled by setting the ID_PULLUP register bit to logic 1. If the state of ID has changed, the ISP1705 will send an RXCMD or interrupt to the link. If the link does not receive any RXCMD or interrupt by time t_{ID}, then the ID state has not changed.

The ISP1705 also provides an internal weak pull-up resistor ($R_{weakPU(ID)}$). This weak pull-up resistor is always enabled to avoid a possible floating condition on the ID pin.

8.12.8 FAULT

This pin is used to detect the V_{BUS} fault condition. If the function is not used, this pin must be connected to ground to avoid floating input.

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If an external V_{BUS} overcurrent or fault detection circuit is used, the output fault indicator of that circuit can be connected to the FAULT input pin. The USE_EXT_VBUS_IND bit in the OTG_CTRL register (see Section 11.7) and the IND_PASSTHRU bit in the INTF_CTRL register (see Section 11.6) must be set to logic 1. The ISP1705 will inform the link of V_{BUS} fault events by sending RXCMDs on the ULPI bus.

The FAULT input pin is mapped to the A_VBUS_VLD bit in RXCMD. Any changes to the FAULT input will trigger RXCMD carrying the FAULT condition with A_VBUS_VLD.

For details, see Section 10.3.2 and Section 10.3.3.

8.12.9 REG3V3 and REG1V8

These are output voltage pins from the internal regulator. These supplies are used internally to power digital and analog circuits.

For proper operation of the regulator, pins REG3V3 and REG1V8 must each be connected to a 0.1 µF capacitor in parallel with a 4.7 µF low ESR capacitor.

REG3V3 powers on-chip pads of the following pins:

- CFG0
- DM
- DP
- FAULT
- ID
- PSW_N
- RREF

8.12.10 V$_{BUS}$

This I/O pin acts as an input to V_{BUS} comparators, and also as a power supply pin for SRP charge and discharge resistors. For details, see Figure 9.

The V_{BUS} pin requires a capacitive load. Table 4 provides the recommended capacitor values for various applications.

Table 4.   Recommended V$_{BUS}$ capacitor value

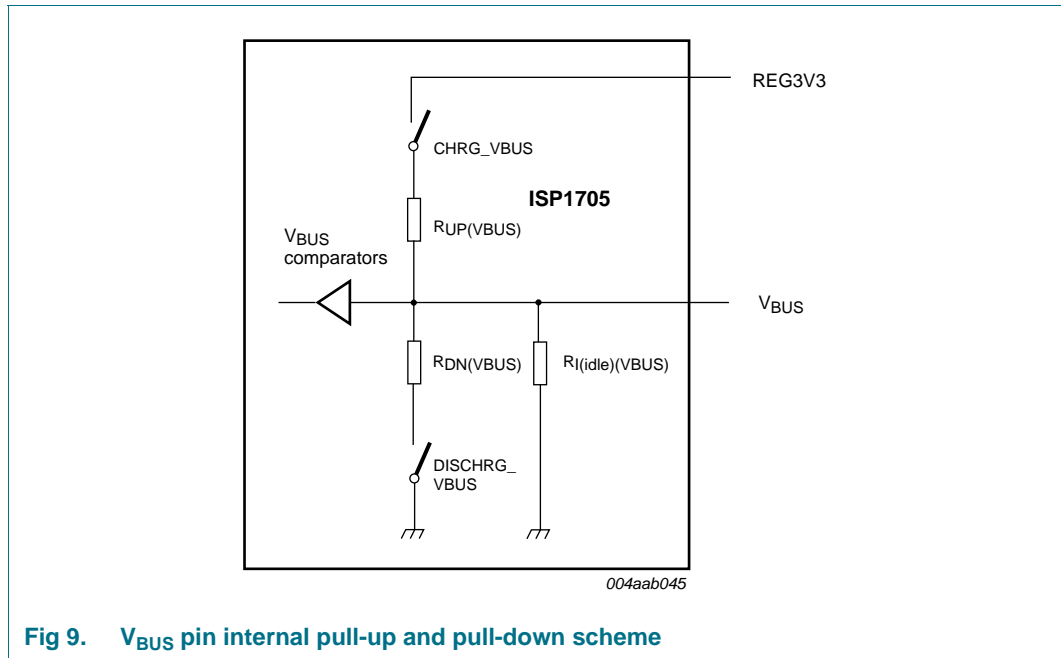| Application	V$_{BUS}$ capacitor (C$_{VBUS}$)
OTG	1 µF to 6.5 µF, 10 V
Standard host	120 µF ± 20 %, 10 V
Standard peripheral	1 µF to 10 µF, 10 V

Fig 9. V$_{BUS}$ **pin internal pull-up and pull-down scheme**

8.12.11 PSW_N

The PSW_N pin is an active-LOW open-drain output pin. It is used to control external charge pumps or V$_{BUS}$ power switches to supply V$_{BUS}$. When in use, an external pull-up resistor is required. This allows for per-port or ganged power control.

To enable the external power source by driving PSW_N to LOW, the link must set the DRV_VBUS_EXT bit in the OTG_CTRL register (see Section 11.7) to logic 1.

Table 5 summarizes settings to drive 5 V on V$_{BUS}$.

Table 5.　OTG_CTRL register power control bits

DRV_VBUS_EXT	Power source used
0	external 5 V V$_{BUS}$ power source disabled (PSW_N = HIGH)
1	external 5 V V$_{BUS}$ power source enabled (PSW_N = LOW)

8.12.12 XTAL1 and XTAL2

XTAL1 is the crystal oscillator input, and XTAL2 is the crystal oscillator output. The allowed crystal or clock frequency on the XTAL1 pin is selectable by the CFG1 and CFG2 pins, as shown in Table 6.

Table 6.　Allowed crystal or clock frequency on the XTAL1 pin

Pin CFG1	Pin CFG2	Allowed crystal or clock frequency on the XTAL1 pin
LOW	LOW	19.2 MHz
LOW	HIGH	26 MHz
HIGH	LOW	24 MHz
HIGH	HIGH	13 MHz

When a clock is driven into XTAL1, XTAL2 must be left open.

If a crystal is attached, it requires a capacitor on each terminal of the crystal to GND. The recommended crystal specification and required external capacitors are given in Table 7 and Table 8.

Table 7.   External capacitor values for 13 MHz or 19.2 MHz clock frequency

Load capacitance C_L of the crystal[1]	Maximum series resistance R_S of the crystal[1]	External capacitor C_{XTAL} value
10 pF	< 180 Ω	18 pF
20 pF	< 100 Ω	39 pF

[1]   Specified by the crystal manufacturer.

Table 8.   External capacitor values for 24 MHz or 26 MHz clock frequency

Load capacitance C_L of the crystal[1]	Maximum series resistance R_S of the crystal[1]	External capacitor C_{XTAL} value
10 pF	< 140 Ω	18 pF
20 pF	< 60 Ω	39 pF

[1]   Specified by the crystal manufacturer.

8.12.13   DIR

ULPI direction output pin. Synchronous to the rising edge of CLOCK. Controls the direction of the data bus. By default, the ISP1705 holds DIR at LOW, causing the data bus to be an input. When DIR is LOW, the ISP1705 listens for data from the link. The ISP1705 pulls DIR to HIGH only when it has data to send to the link, which is for one of two reasons:

- To send data (USB receive or register reads) and RXCMD status updates to the link.
- To block the link from driving the data bus during power-up, reset and low power (suspend) mode.

This pin can be 3-stated when chip select is deasserted.

8.12.14   RESET_N

An active-LOW asynchronous reset pin that resets all circuits in the ISP1705. The ISP1705 contains an internal power-on reset circuit, and therefore using the RESET_N pin is optional. If RESET_N is not used, it must be connected to $V_{CC(I/O)}$.

For details on using RESET_N, see Section 8.11.2.

8.12.15   STP

ULPI stop input pin. Synchronous to the rising edge of CLOCK. The link must assert STP to signal the end of a USB transmit packet or a register write operation. When DIR is asserted, the link can optionally assert STP for one clock cycle to abort the ISP1705, causing it to deassert DIR in the next clock cycle.

8.12.16   NXT

ULPI next data output pin. Synchronous to the rising edge of CLOCK. The ISP1705 holds NXT at LOW, by default. When DIR is LOW and the link is sending data to the ISP1705, NXT will be asserted to notify the link to provide the next data byte. When DIR is HIGH

and the ISP1705 is sending data to the link, NXT will be asserted to notify the link that another valid byte is on the bus. NXT is not used for register read data or the RXCMD status update.

This pin can be 3-stated when chip select is deasserted.

8.12.17 CLOCK

A 60 MHz interface clock to synchronize the ULPI bus. All ULPI pins are synchronous to the rising edge of CLOCK.

The ISP1705 provides two clocking options:

- A crystal is attached between the XTAL1 and XTAL2 pins.
- A clock is driven into the XTAL1 pin, with the XTAL2 pin left unconnected.

8.12.18 CFG1, CFG2

These input pins are used to select the crystal or clock frequency. For details, see Table 6.

8.12.19 CHIP_SEL, CHIP_SEL_N

When chip select is deasserted, ULPI pins DATA[7:0], CLOCK, DIR and NXT are 3-stated and the STP input is ignored; internal circuits are powered-down as well.

When chip select is asserted, the ISP1705 will operate normally.

Both the CHIP_SEL and CHIP_SEL_N pins must be asserted for the chip select to function. If any of the two is deasserted, the chip will enter Power-down mode.

8.12.20 GND

Global ground signal. To ensure the correct operation of the ISP1705, GND must be soldered to the cleanest available ground.

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9. Modes of operation

9.1 Power modes

When both $V_{CC(I/O)}$ and V_{CC} are not powered, there will be no leakage from the V_{BUS} pin to all the remaining pins, including V_{CC} and $V_{CC(I/O)}$. Applying V_{BUS} within the normal range will not damage the ISP1705 chip.

When both V_{CC} and $V_{CC(I/O)}$ are powered and are within the operating voltage range, the ISP1705 will be fully functional as in normal mode.

When $V_{CC(I/O)}$ is powered and the V_{CC} voltage is below the operating range of the ISP1705, the application system must detect the low voltage condition and set chip select to deassert (that is, put the ISP1705 in Power-down mode). This is to protect the ULPI and USB interfaces from driving wrong levels. Under this condition, the $V_{CC(I/O)}$ voltage will not leak to USB pins (V_{BUS}, DP, DM and ID) and the V_{CC} pin. All the digital pins (see Section 8.12.2) powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to a defined state or terminated by using pull-up or pull-down resistors to avoid a floating input condition. Other pins (see Section 8.12.9) are not powered.

9.1.1 Normal mode

In normal mode, both V_{CC} and $V_{CC(I/O)}$ are powered. Chip select is asserted. The ISP1705 is fully functional.

9.1.2 Power-down mode

When $V_{CC(I/O)}$ is not present or when chip select is deasserted, the ISP1705 is put into Power-down mode. In this mode, internal regulators are powered down to keep the V_{CC} current to a minimum. The voltage on the V_{CC} pin will not leak to the $V_{CC(I/O)}$ and/or V_{BUS} pins. In this mode, the ISP1705 pin states are given in Table 9.

Table 9. Pin states in Power-down mode

Pin name[1]	Pin state when $V_{CC(I/O)}$ is not present	Pin state when $V_{CC(I/O)}$ is present and chip select is not active
V_{CC}	3.0 V to 4.5 V	3.0 V to 4.5 V
$V_{CC(I/O)}$	not powered[2]	3.0 V to 3.6 V
CHIP_SEL, CHIP_SEL_N	not powered[2]	HIGH
CFG1, CFG2, RESET_N, CLOCK, STP, NXT, DIR, DATA[7:0]	not powered[2]	3.0 V to 3.3 V
CFG0, DP, DM, ID, REG1V8, REG3V3, XTAL1, XTAL2, RREF, PSW_N, FAULT	not powered[2]	not powered[2]

[1] When I/O pins are not powered, the input buffer is disabled and will ignore the external input level. The input pins, however, should not be driven by another voltage source to prevent leakage.

[2] These pins must not be externally driven to HIGH. Otherwise, the ISP1705 behavior is undefined and leakage current will occur.

When $V_{CC(I/O)}$ is not present, all the digital pins (see Section 8.12.2) that are powered by $V_{CC(I/O)}$ are not powered. Other pins (see Section 8.12.9) are also not powered.

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When the ISP1705 is put into Power-down mode by disabling chip select, all the digital pins (see Section 8.12.2) that are powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to defined states or terminated by using pull-up or pull-down resistors to avoid a floating input condition. Other pins (see Section 8.12.9) are not powered. In this mode, minimum current will be drawn by $V_{CC(I/O)}$ to detect the chip select status.

9.2 ULPI modes

The ISP1705 ULPI interface can be programmed to operate in five modes. In each mode, the signals on the data bus are reconfigured as described in the following subsections. Setting more than one mode will lead to undefined behavior.

9.2.1 Synchronous mode

This is default mode. On power-up, and when CLOCK is stable, the ISP1705 will enter synchronous mode.

In synchronous mode, the link must synchronize all ULPI signals to CLOCK, meeting the set-up and hold times as defined in Section 15.

This mode is used by the link to perform the following tasks:

- High-speed detection handshake (chirp)
- Transmit and receive USB packets
- Read from and write to registers
- Receive USB status updates (RXCMDs) from the ISP1705

For more information on various synchronous mode protocols, see Section 10.

Table 10. ULPI signal description

Signal name	Direction on the ISP1705[1]	Signal description
CLOCK	O	**60 MHz interface clock**: When a crystal is attached or a clock is driven into the XTAL1 pin, the ISP1705 will drive a 60 MHz output clock. During low-power, serial and UART modes, the clock can be turned off to save power.
DATA[7:0]	I/O	**8-bit data bus**: In synchronous mode, the link drives DATA[7:0] to LOW by default. The link initiates transfers by sending a nonzero data pattern called a TXCMD (transmit command). In synchronous mode, the direction of DATA[7:0] is controlled by DIR. Contents of DATA[7:0] lines must be ignored for exactly one clock cycle whenever DIR changes state. This is called a turnaround cycle. Data lines have fixed directions and different meanings in low-power, 3-pin serial and UART modes.

Table 10.   **ULPI signal description** …*continued*

Signal name	Direction on the ISP1705[1]	Signal description
DIR	O	**Direction**: Controls the direction of data bus DATA[7:0].
		In synchronous mode, the ISP1705 drives DIR to LOW by default, making the data bus an input so the ISP1705 can listen for TXCMD from the link. The ISP1705 drives DIR to HIGH only when it has data for the link. When DIR and NXT are HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called an RXCMD (receive command). The only exception to this rule is when the PHY returns register read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which DATA[7:0] is not valid and must be ignored by the link.
		DIR is always asserted during low-power, serial and UART modes.
STP	I	**Stop**: In synchronous mode, the link drives STP to HIGH for one cycle after the last byte of data is sent to the ISP1705. The link can optionally assert STP to force DIR to be deasserted.
		In low-power, serial and UART modes, the link holds STP at HIGH to wake up the ISP1705, causing the ULPI bus to return to synchronous mode.
NXT	O	**Next**: In synchronous mode, the ISP1705 drives NXT to HIGH to throttle data. If DIR is LOW, the ISP1705 asserts NXT to notify the link to place the next data byte on DATA[7:0] in the following clock cycle. If DIR is HIGH, the ISP1705 asserts NXT to notify the link that a valid USB data byte is on DATA[7:0] in the current cycle. The ISP1705 always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register read data is to be returned to the link in the current cycle.
		NXT is not used in low-power, serial and UART modes.

[1]   I = input; O = output.

9.2.2   Low-power mode

When the USB bus is idle, the link can place the ISP1705 into low-power mode (also called suspend mode). In low-power mode, the data bus definition changes to that shown in Table 11. To enter low-power mode, the link sets the SUSPENDM bit in the FUNC_CTRL register (see Section 11.5) to logic 0. To exit low-power mode, the link asserts the STP signal. After exiting low-power mode, the ISP1705 will send an RXCMD to the link if a change was detected in any interrupt source, and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

The ISP1705 will draw only suspend current from the V_{CC} supply; see Table 54.

During low-power mode, the clock on XTAL1 may be stopped. The clock must be started again before asserting STP to exit low-power mode.

For more information on low-power mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 11.   **Signal mapping during low-power mode**

Signal	Maps to	Direction[1]	Description
LINESTATE0	DATA0	O	combinatorial LINESTATE0 directly driven by the analog receiver
LINESTATE1	DATA1	O	combinatorial LINESTATE1 directly driven by the analog receiver

Table 11.   Signal mapping during low-power mode …continued

Signal	Maps to	Direction[1]	Description
Reserved	DATA2	O	reserved; the ISP1705 will drive this pin to LOW
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1705 will drive these pins to LOW

[1]   I = input; O = output.

9.2.3   6-pin full-speed or low-speed serial mode

If the link requires a 6-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1705 to 6-pin serial mode. In 6-pin serial mode, the data bus definition changes to that shown in Table 12. To enter 6-pin serial mode, the link sets the 6PIN_FSLS_SERIAL bit in the INTF_CTRL register (see Section 11.6) to logic 1. To exit 6-pin serial mode, the link asserts the STP signal. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed functionality. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 6-pin serial mode.

For more information on 6-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 12.   Signal mapping for 6-pin serial mode

Signal	Maps to	Direction[1]	Description
TX_ENABLE	DATA0	I	active-HIGH transmit enable
TX_DAT	DATA1	I	transmit differential data on DP and DM
TX_SE0	DATA2	I	transmit single-ended zero on DP and DM
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
RX_DP	DATA4	O	single-ended receive data from DP
RX_DM	DATA5	O	single-ended receive data from DM
RX_RCV	DATA6	O	differential receive data from DP and DM
Reserved	DATA7	O	reserved; the ISP1705 will drive this pin to LOW

[1]   I = input; O = output.

9.2.4   3-pin full-speed or low-speed serial mode

If the link requires a 3-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1705 to 3-pin serial mode. In 3-pin serial mode, the data bus definition changes to that shown in Table 13. To enter 3-pin serial mode, the link sets the 3PIN_FSLS_SERIAL bit in the INTF_CTRL register (see Section 11.6) to logic 1. To exit 3-pin serial mode, the link asserts the STP signal. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed functionality. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 3-pin serial mode.

For more information on 3-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1.*

Table 13.   Signal mapping for 3-pin serial mode

Signal	Maps to	Direction[1]	Description
TX_ENABLE	DATA0	I	active-HIGH transmit enable
DAT	DATA1	I/O	transmit differential data on DP and DM when TX_ENABLE is HIGH
			receive differential data from DP and DM when TX_ENABLE is LOW
SE0	DATA2	I/O	transmit single-ended zero on DP and DM when TX_ENABLE is HIGH
			receive single-ended zero from DP and DM when TX_ENABLE is LOW
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1705 will drive these pins to LOW

[1]   I = input; O = output.

9.2.5 Transparent UART mode

In transparent UART mode, the ISP1705 functions as a voltage level shifter between following pins:

- From pin DATA0 ($V_{CC(I/O)}$ level) to pin DM (2.7 V level).
- From pin DP (2.7 V level) to pin DATA1 ($V_{CC(I/O)}$ level).

The USB transceiver is used to drive the UART transmitting signal on the DM line. The rise time and the fall time of the transmitting signal is determined by whether a full-speed or low-speed transceiver is in use. It is recommended to use a low-speed transceiver if the UART bit rate is below 921 kbit/s for better EMI performance. If the UART bit rate is equal to or above 921 kbit/s, a full-speed transceiver can be used.

In transparent UART mode, data bus definitions change to that shown in Table 14.

Table 14.   UART signal mapping

Signal	Maps to	Direction[1]	Description
TXD	DATA0	I	UART TXD signal that is routed to the DM pin
RXD	DATA1	O	UART RXD signal that is routed from the DP pin
Reserved	DATA2	O	reserved; the ISP1705 will drive this pin to LOW in UART mode
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1705 will drive these pins to LOW in UART mode

[1]   I = input; O = output.

Transparent UART mode is entered by setting some register bits in ULPI registers. The recommended sequence is:

1. Set the XCVRSELECT[1:0] bits in the FUNC_CTRL register (see Section 11.5) to 10b (low speed) or 01b (full speed). This setting affects the rise time and the fall time of the UART transmitting signal on the DM line.

2. Set the DP_PULLDOWN and DM_PULLDOWN bits in the OTG_CTRL register (see Section 11.7) to logic 0.

3. Set the TERMSELECT bit in the FUNC_CTRL register (see Section 11.5) to logic 0 (power-on default value).

   Remark: Mandatory when a full-speed driver is used and optional for a low-speed driver.

4. Set the TXD_EN and RXD_EN bits in the CARKIT_CTRL register (see Section 11.14) to logic 1. These two bits must be set together in one TXCMD.

5. Set the CARKIT_MODE bit in the INTF_CTRL register (see Section 11.6) to logic 1.

   Remark: The CARKIT_MODE, TXD_EN and RXD_EN bits must be set to logic 1. The sequence of setting these register bits is ignored.

After the register configuration is complete:

1. A weak pull-up resistor will be enabled on the DP and DATA0 pins. This is to avoid the possible floating condition on these input pins when UART mode is enabled.

2. The 39 Ω serial termination resistors on the DP and DM pins will be enabled.

3. One clock cycle after DIR goes from LOW to HIGH, the ISP1705 will drive the data bus for five clock cycles. This is to charge the DATA0 pin to a HIGH level for a slow link. However, the link can start driving DATA0 to HIGH immediately after the turnaround cycle.

4. UART buffers between DATA0 or DATA1 and DM or DP are enabled. Transparent UART mode is entered.

   Remark: The DP pin will be slowly charged up to HIGH by the weak pull-up resistor. The time needed depends on the capacitive loading on DP.

By default, the clock is powered down when the ISP1705 enters UART mode. If the link requires CLOCK to be running in UART mode, it can set the CLOCK_SUSPENDM bit in the INTF_CTRL register (see Section 11.6) to logic 1 before entering UART mode.

Transparent UART mode is exited by asserting the STP pin to HIGH or by toggling chip select.

The INT pin is asserted and latched whenever an unmasked interrupt event occurs. When the link detects INT as HIGH, it must wake up the PHY from transparent UART mode by asserting STP. When the PHY is in synchronous mode, the link can read the USB_INTR_L register (see Section 11.11) to determine the source of the interrupt. Note that the ISP1705 does not implement the optional Carkit Interrupt registers.

An alternative way to exit UART mode is to set chip select to non-active for more than t_{PWRDN} and then set it to active. A power-on reset will be generated and the ULPI bus will be put in default synchronous mode.

(1) Clock remains powered when the CLOCK_SUSPENDM register bit is set to logic 1.

(2) Clock is powered down when the CLOCK_SUSPENDM register bit is logic 0 (default).

Fig 10. Interface behavior when entering UART mode

(1) Clock remains powered when the CLOCK_SUSPENDM register bit is set to logic 1.

(2) Clock is powered down when the CLOCK_SUSPENDM register bit is logic 0 (default).

Fig 11. Interface behavior when exiting UART mode

9.3 USB state transitions

A Hi-Speed USB peripheral, host or OTG device handles more than one electrical state as defined in *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*. The ISP1705 accommodates various states through register settings of the XCVRSELECT[1:0], TERMSELECT, OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN bits.

Table 15 summarizes operating states. The values of register settings in Table 15 will force resistor settings as also given in Table 15. Resistor setting signals are defined as follows:

- RPU_DP_EN enables the 1.5 kΩ pull-up resistor on DP
- RPD_DP_EN enables the 15 kΩ pull-down resistor on DP
- RPD_DM_EN enables the 15 kΩ pull-down resistor on DM
- HSTERM_EN enables the 45 Ω termination resistors on DP and DM

It is up to the link to set the desired register settings.

Table 15. Operating states and their corresponding resistor settings

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_ DP_EN	RPD_ DP_EN	RPD_ DM_EN	HSTERM_ EN
General settings									
3-state drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b
Power up or $V_{BUS} < V_{B\_SESS\_END}$	01b	0b	00b	1b	1b	0b	1b	1b	0b
Host settings									
Host chirp	00b	0b	10b	1b	1b	0b	1b	1b	1b
Host high-speed	00b	0b	00b	1b	1b	0b	1b	1b	1b
Host full-speed	X1b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed suspend	01b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed resume	01b	1b	10b	1b	1b	0b	1b	1b	0b
Host low-speed	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed suspend	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed resume	10b	1b	10b	1b	1b	0b	1b	1b	0b
Host Test J or Test K	00b	0b	10b	1b	1b	0b	1b	1b	1b
Peripheral settings									
Peripheral chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral high speed	00b	0b	00b	0b	0b	0b	0b	0b	1b
Peripheral full speed	01b	1b	00b	0b	0b	1b	0b	0b	0b

Table 15. Operating states and their corresponding resistor settings *…continued*

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_ DP_EN	RPD_ DP_EN	RPD_ DM_EN	HSTERM_ EN
Peripheral high speed or full speed suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high speed or full speed resume	01b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b	0b	0b	0b	1b
OTG settings									
OTG device peripheral chirp	00b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral high speed	00b	0b	00b	0b	1b	0b	0b	1b	1b
OTG device peripheral full speed	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high speed and full speed suspend	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high speed and full speed resume	01b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral Test J or Test K	00b	0b	10b	0b	1b	0b	0b	1b	1b

10. Protocol description

10.1 ULPI references

The ISP1705 provides a 12-pin ULPI interface to communicate with the link. It is highly recommended that users of the ISP1705 read *UTMI+ Specification Rev. 1.0* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Commands between the ISP1705 and the link are described in the following subsections.

10.2 TXCMD

By default, the link must drive the ULPI bus to its idle state of 00h. To send commands and USB packets, the link drives a nonzero value on DATA[7:0] to the ISP1705 by sending a byte called TXCMD. Commands include USB packet transmissions, and register reads and writes. Once the TXCMD is interpreted and accepted by the ISP1705, the NXT signal is asserted and the link can follow up with the required number of data bytes. The TXCMD byte format is given in Table 16. Any values other than those in Table 16 are illegal and will result in undefined behavior.

Various TXCMD packet and register sequences are given in later sections.

Table 16.   TXCMD byte format

Command type name	Command code DATA[7:6]	Command payload DATA[5:0]	Command name	Command description
Idle	00b	00 0000b	NOOP	No operation. 00h is the idle value of the data bus. The link must drive NOOP by default.
Packet transmit	01b	00 0000b	NOPID	Transmit USB data that does not have a PID, such as chirp and resume signaling. The ISP1705 starts transmitting only after accepting the next data byte.
		00 XXXXb	PID	Transmit USB packet. DATA[3:0] indicates USB packet identifier PID[3:0].
Register write	10b	10 1111b	EXTW	Extended register write command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGW	Register write command with 6-bit immediate address.
Register read	11b	10 1111b	EXTR	Extended register read command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGR	Register read command with 6-bit immediate address.

10.3 RXCMD

The ISP1705 communicates status information to the link by asserting DIR and sending an RXCMD byte on the data bus. The RXCMD data byte format follows *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and is given in Table 17.

The ISP1705 will automatically send an RXCMD whenever there is a change in any of the RXCMD data fields. The link must be able to accept an RXCMD at any time; including single RXCMDs, back-to-back RXCMDs, and RXCMDs at any time during USB receive packets when NXT is LOW. An example is shown in Figure 12. For details and diagrams, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 17.   RXCMD byte format

DATA	Name	Description and value
1 to 0	LINESTATE	**LINESTATE signals**: For a definition of LINESTATE, see Section 10.3.1. **DATA0 —** LINESTATE0 **DATA1 —** LINESTATE1
3 to 2	V_{BUS} state	**Encoded V_{BUS} voltage state**: For an explanation of the V_{BUS} state, see Section 10.3.2.
5 to 4	RxEvent	**Encoded USB event signals**: For an explanation of RxEvent, see Section 10.3.4.
6	ID	Reflects the state of the ID pin. Valid 50 ms after ID_PULLUP is set to logic 1.
7	ALT_INT	By default, this signal is not used and is not needed in typical designs. Optionally, the link can enable the BVALID_RISE and/or BVALID_FALL bits in the PWR_CTRL register (see Section 11.15). Corresponding changes in BVALID will cause an RXCMD to be sent to the link with the ALT_INT bit asserted.

004aaa695
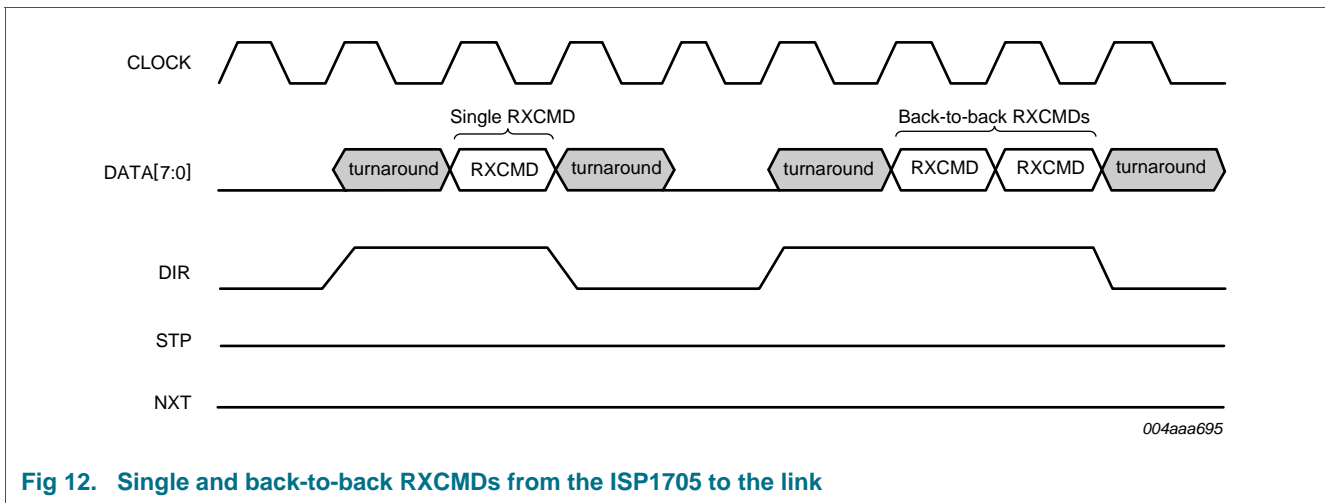
Fig 12.   Single and back-to-back RXCMDs from the ISP1705 to the link

10.3.1 Linestate encoding

LINESTATE[1:0] reflects the current state of DP and DM. Whenever the ISP1705 detects a change in DP or DM, an RXCMD will be sent to the link with the new LINESTATE[1:0] value. The value given on LINESTATE[1:0] depends on the setting of various registers.

Table 18 shows the LINESTATE[1:0] encoding for upstream facing ports, which applies to peripherals. Table 19 shows the LINESTATE[1:0] encoding for downstream facing ports, which applies to host controllers. Dual-role devices must choose the correct table, depending on whether it is in peripheral or host mode.

Table 18. **LINESTATE[1:0] encoding for upstream facing ports: peripheral**
DP_PULLDOWN = 0.[1]

Mode	Value	Full speed	High speed	Chirp
XCVRSELECT[1:0]		01, 11	00	00
TERMSELECT		1	0	1
LINESTATE[1:0]	00	SE0	squelch	squelch
	01	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

Table 19. **LINESTATE[1:0] encoding for downstream facing ports: host**
DP_PULLDOWN and DM_PULLDOWN = 1.[1]

Mode	Value	Low speed	Full speed	High speed	Chirp
XCVRSELECT[1:0]		10	01, 11	00	00
TERMSELECT		1	1	0	0
OPMODE[1:0]		X	X	00, 01 or 11	10
LINESTATE[1:0]	00	SE0	SE0	squelch	squelch
	01	LS-K	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	LS-J	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

10.3.2 V_{BUS} state encoding

USB devices must monitor the V_{BUS} voltage for purposes such as overcurrent detection, starting a session and SRP. The V_{BUS} state field in the RXCMD is an encoding of the voltage level on V_{BUS}.

The SESS_END and SESS_VLD indicators in the V_{BUS} state are directly taken from the internal comparators built-in to the ISP1705, and encoded as shown in Table 17 and Table 20.

Table 20. **Encoded V_{BUS} voltage state**

Value	V_{BUS} voltage	SESS_END	SESS_VLD	A_VBUS_VLD
00	$V_{BUS} < V_{B\_SESS\_END}$	1	0	0
01	$V_{B\_SESS\_END} \leq V_{BUS} < V_{A\_SESS\_VLD}$	0	0	0
10	$V_{A\_SESS\_VLD} \leq V_{BUS} < V_{A\_VBUS\_VLD}$	X	1	0
11	$V_{BUS} \geq V_{A\_VBUS\_VLD}$	X	X	1

The A_VBUS_VLD indicator in the V_{BUS} state provides several options and must be configured based on current draw requirements. A_VBUS_VLD can input from one or more V_{BUS} voltage indicators, as shown in Figure 13.

A description on how to use and select the V_{BUS} state encoding is given in Section 10.3.3.
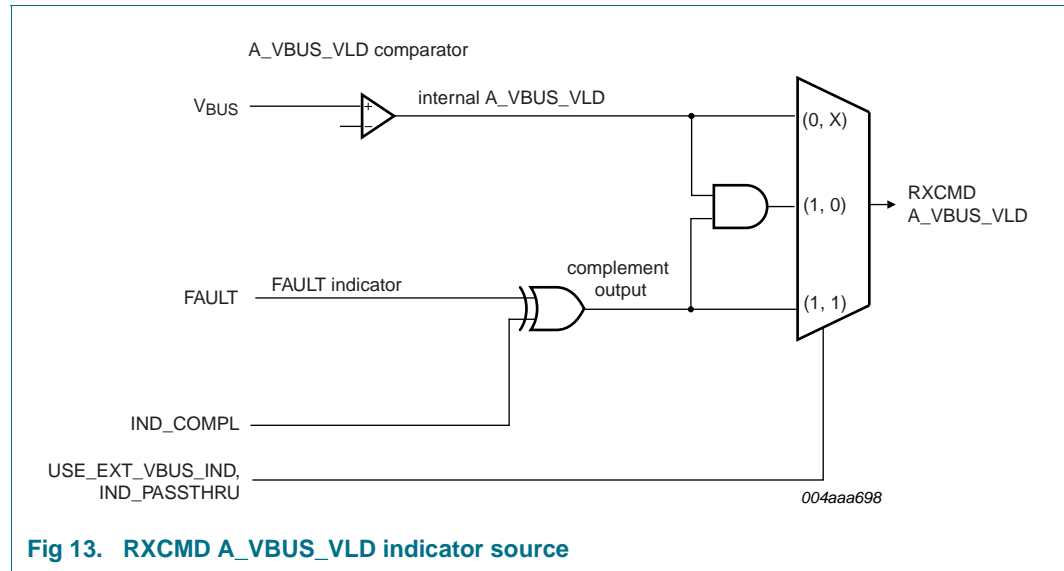
Fig 13.   RXCMD A_VBUS_VLD indicator source

10.3.3   Using and selecting the V_{BUS} state encoding

The V_{BUS} state encoding is shown in Table 20. The ISP1705 will send an RXCMD to the link whenever there is a change in the V_{BUS} state. To receive V_{BUS} state updates, the link must first enable the corresponding interrupts in the USB_INTR_EN_R and USB_INTR_EN_F registers.

The link can use the V_{BUS} state to monitor V_{BUS} and take appropriate actions. Table 21 shows the recommended usage for typical applications.

Table 21. V_{BUS} indicators in RXCMD required for typical applications

Application	A_VBUS_VLD	SESS_VLD	SESS_END
Standard host	yes	no	no
Standard peripheral	no	yes	no
OTG A-device	yes	yes	no
OTG B-device	no	yes	yes

10.3.3.1   Standard USB host controllers

For standard hosts, the system must be able to provide 500 mA on V_{BUS} in the range of 4.75 V to 5.25 V. An external circuit must be used to detect overcurrent conditions. If the external overcurrent detector provides a digital fault signal, then the fault signal must be connected to the ISP1705 FAULT input pin, and the link must do the following:

1. Set the IND_COMPL bit in the INTF_CTRL register (see Section 11.6) to logic 0 or logic 1, depending on the polarity of the external fault signal.

2. Set the USE_EXT_VBUS_IND bit in the OTG_CTRL register (see Section 11.7) to logic 1.

3. If it is not necessary to qualify the fault indicator with the internal A_VBUS_VLD comparator, set the IND_PASSTHRU bit in the INTF_CTRL register (see Section 11.6) to logic 1.

10.3.3.2 Standard USB peripheral controllers

Standard peripherals must be able to detect when V_{BUS} is at a sufficient level for operation. SESS_VLD must be enabled to detect the start and end of USB peripheral operations. Detection of A_VBUS_VLD and SESS_END thresholds is not needed for standard peripherals.

10.3.3.3 OTG devices

When an OTG device is configured as an OTG A-device, it must be able to provide a minimum of 8 mA on V_{BUS}. If the OTG A-device provides less than 100 mA, then there is no need for an overcurrent detection circuit because the internal A_VBUS_VLD comparator is sufficient. If the OTG A-device provides more than 100 mA on V_{BUS}, an overcurrent detector must be used and Section 10.3.3.1 applies. The OTG A-device also uses SESS_VLD to detect when an OTG B-device is initiating V_{BUS} pulsing SRP.

When an OTG device is configured as an OTG B-device, SESS_VLD must be used to detect when V_{BUS} is at a sufficient level for operation. SESS_END must be used to detect when V_{BUS} has dropped to a LOW level, allowing the B-device to safely initiate V_{BUS} pulsing SRP.

10.3.4 RxEvent encoding

The RxEvent field (see Table 22) of the RXCMD informs the link of information related packets received on the USB bus. RxActive and RxError are defined in *USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05*. HostDisconnect is defined in *UTMI+ Specification Rev. 1.0*. A short definition is also given in the following subsections.

Table 22.   Encoded USB event signals

Value	RxActive	RxError	HostDisconnect
00	0	0	0
01	1	0	0
11	1	1	0
10	X	X	1

10.3.4.1 RxActive

When the ISP1705 has detected a SYNC pattern on the USB bus, it signals an RxActive event to the link. An RxActive event can be communicated using two methods. The first method is for the ISP1705 to simultaneously assert DIR and NXT. The second method is for the ISP1705 to send an RXCMD to the link with the RxActive field in the RxEvent bits set to logic 1. The link must be capable of detecting both methods. RxActive frames the receive packet from the first byte to the last byte.

The link must assume that RxActive is set to logic 0 when indicated in an RXCMD or when DIR is deasserted, whichever occurs first.

The link uses RxActive to time high-speed packets and ensure that bus turnaround times are met. For more information on the USB packet timing, see Section 10.6.1.

10.3.4.2 RxError

When the ISP1705 has detected an error while receiving a USB packet, it deasserts NXT and sends an RXCMD with the RxError field set to logic 1. The received packet is no longer valid and must be dropped by the link.

10.3.4.3 HostDisconnect

HostDisconnect is encoded into the RxEvent field of the RXCMD. HostDisconnect is valid only when the ISP1705 is configured as a host (both DP_PULLDOWN and DM_PULLDOWN are set to logic 1), and indicates to the host controller when a peripheral is connected (0b) or disconnected (1b). The host controller must enable HostDisconnect by setting the HOST_DISCON_R and HOST_DISCON_F bits in the USB_INTR_EN_R and USB_INTR_EN_F registers, respectively. Changes in HostDisconnect will cause the PHY to send an RXCMD to the link with the updated value.

10.4 Register read and write operations

Figure 14 shows register read and write sequences. The ISP1705 supports immediate addressing and extended addressing register operations. Extended register addressing is optional for links. Note that register operations will be aborted if the ISP1705 asserts DIR during the operation. When a register operation is aborted, the link must retry until successful. For more information on register operations, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

AD indicates the address byte, and D indicates the data byte.

Fig 14. Example of register write, register read, extended register write and extended register read
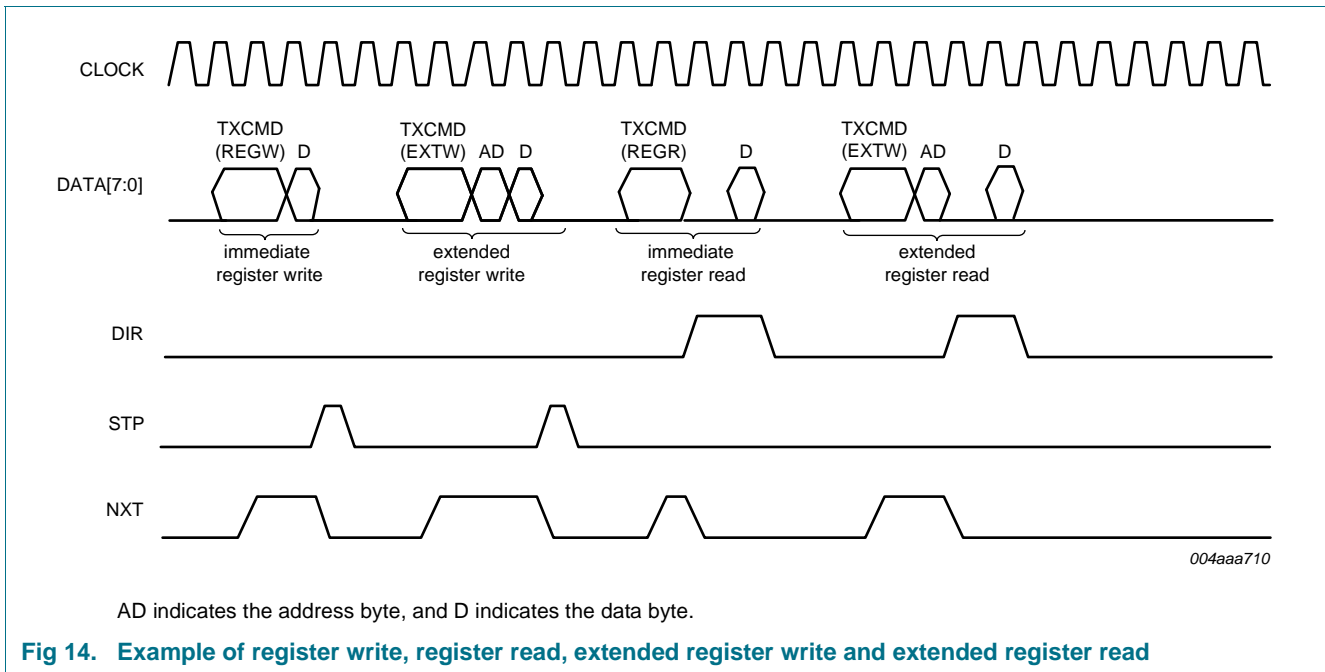
10.5 USB reset and high-speed detection handshake (chirp)

Figure 15 shows the sequence of events for USB reset and high-speed detection handshake (chirp). The sequence is shown for hosts and peripherals. Figure 15 does not show all RXCMD updates, and timing is not to scale. The sequence is as follows:

1. USB reset: The host detects a peripheral attachment as low-speed if DM is HIGH and as full-speed if DP is HIGH. If a host detects a low-speed peripheral, it does not follow the remainder of this protocol. If a host detects a full-speed peripheral, it resets the peripheral by writing to the FUNC_CTRL register (see Section 11.5) and setting XCVRSELECT[1:0] = 00b (high speed) and TERMSELECT = 0b that drives SE0 on the bus (DP and DM connected to ground through 45 Ω). The host also sets OPMODE[1:0] = 10b for correct chirp transmit and receive. The start of SE0 is labeled t0.

   Remark: To receive chirp signaling, the host must also consider the high-speed differential receiver output. The host controller must interpret LINESTATE as shown in Table 19.

2. High-speed detection handshake (chirp)

   a. Peripheral chirp: After detecting SE0 for no less than 2.5 μs, if the peripheral is capable of high speed, it sets XCVRSELECT[1:0] to 00b (high speed) and OPMODE[1:0] to 10b (chirp). The peripheral immediately follows this with a TXCMD (NOPID), transmitting a Chirp K for no less than 1 ms and ending no more than 7 ms after reset time t0. If the peripheral is in low-power mode, it must wake up its clock within 5.6 ms, leaving 200 μs for the link to start transmitting the Chirp K, and 1.2 ms for the Chirp K to complete (worst case with 10 % slow clock).

   b. Host chirp: If the host does not detect the peripheral chirp, it must continue asserting SE0 until the end of reset. If the host detects the peripheral Chirp K for no less than 2.5 μs, then no more than 100 μs after the bus leaves the Chirp K state, the host sends a TXCMD (NOPID) with an alternating sequence of Chirp Ks and Js. Each Chirp K or Chirp J must last no less than 40 μs and no longer than 60 μs.

   c. High speed idle: The peripheral must detect a minimum of Chirp K-J-K-J-K-J. Each Chirp K and Chirp J must be detected for at least 2.5 μs. The peripheral sets TERMSELECT = 0b and OPMODE[1:0] = 00b after seeing the minimum chirp sequence. The peripheral is now in high-speed mode and sees !squelch (01b on LINESTATE). When the peripheral sees squelch (10b on LINESTATE), it knows that the host has completed chirp and waits for Hi-Speed USB traffic to begin. After transmitting the chirp sequence, the host changes OPMODE[1:0] to 00b and begins sending USB packets.

For more information, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Timing is not to scale.
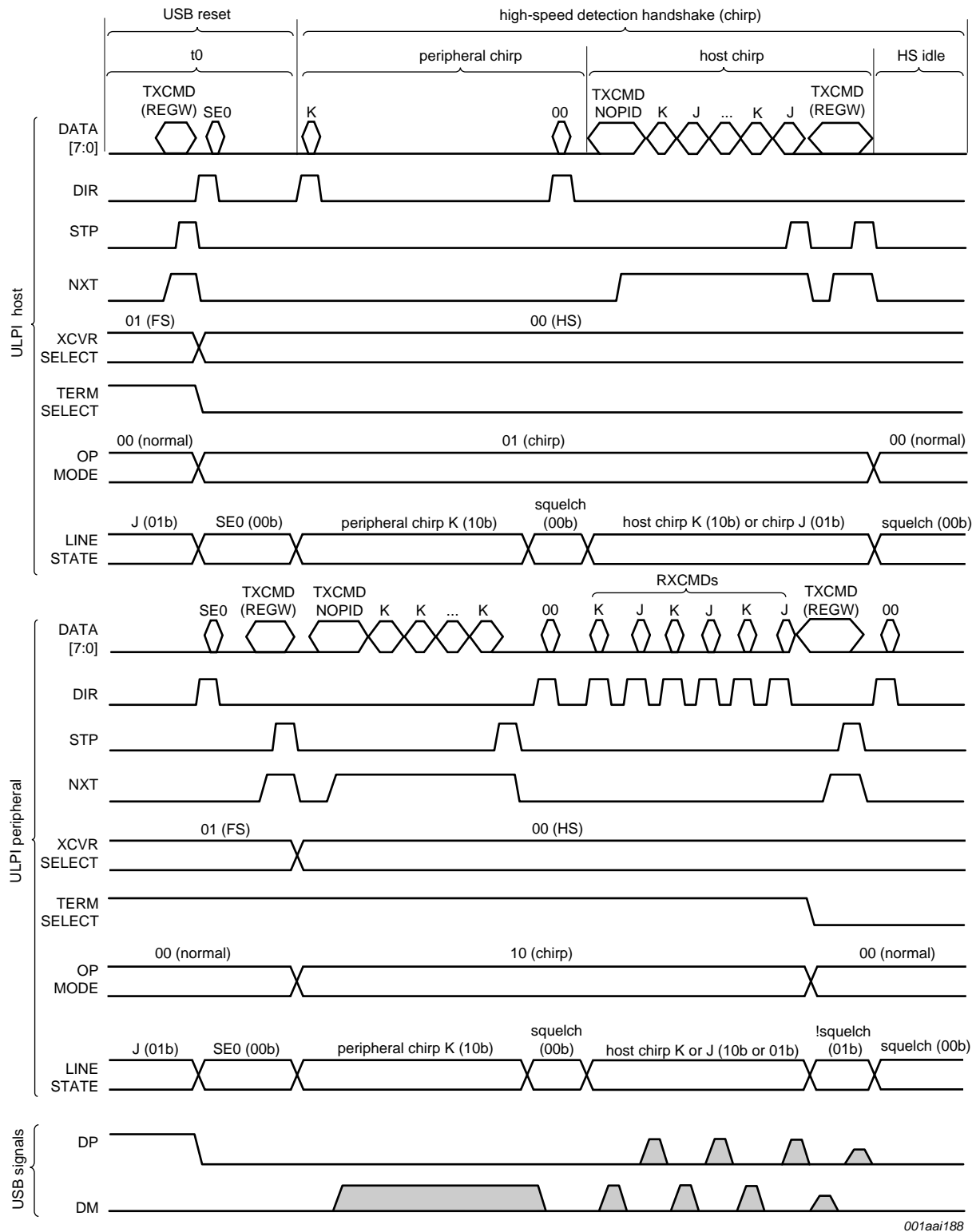
Fig 15. USB reset and high-speed detection handshake (chirp) sequence

10.6 USB packet transmit and receive

An example of a packet transmit and receive is shown in Figure 16. For details on USB packets, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.
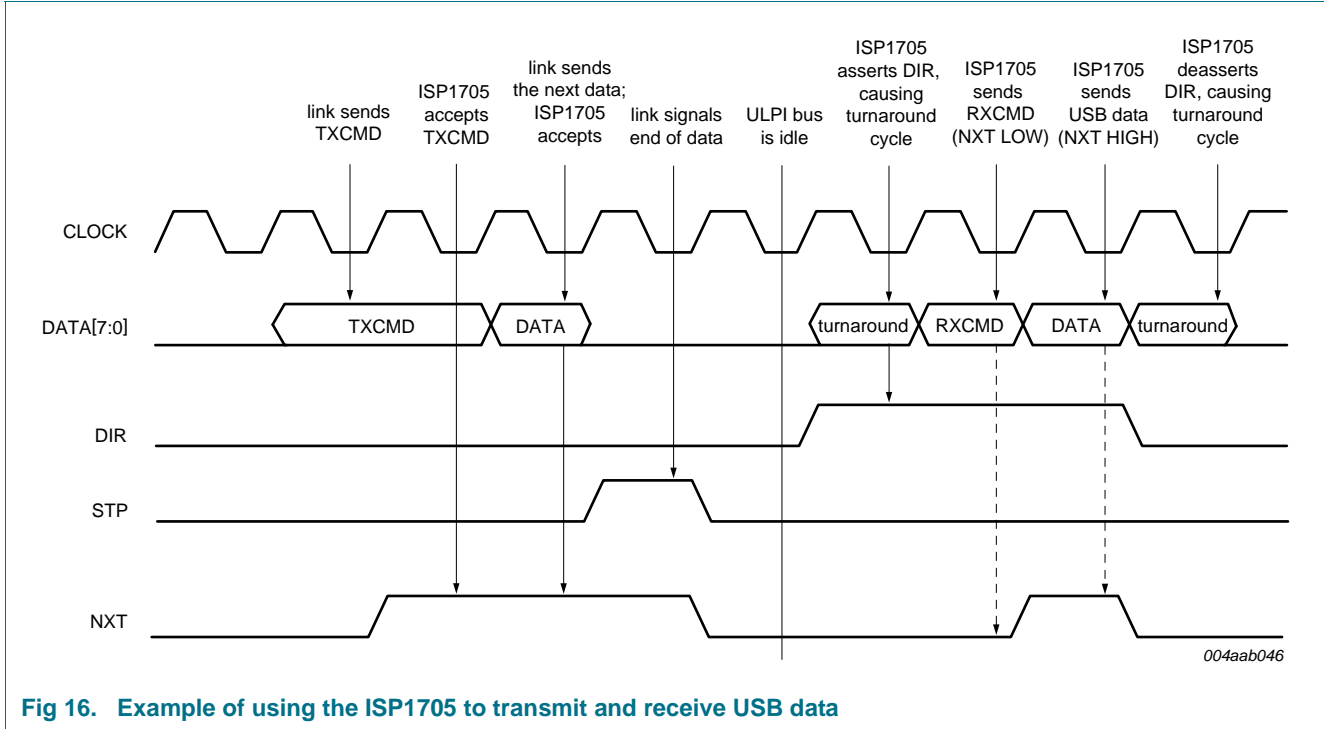
Fig 16.   Example of using the ISP1705 to transmit and receive USB data

10.6.1 USB packet timing

10.6.1.1 ISP1705 pipeline delays

The ISP1705 delays (in clock cycles) are shown in Table 23. For detailed description, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.2*.

Table 23.   PHY pipeline delays

Parameter name	High-speed PHY delay	Full-speed PHY delay	Low-speed PHY delay
RXCMD delay (J and K)	4	4	4
RXCMD delay (SE0)	4	4 to 6	16 to 18
TX start delay	1 to 2	6 to 10	74 to 75
TX end delay (packets)	3 to 4	not applicable	not applicable
TX end delay (SOF)	6 to 9	not applicable	not applicable
RX start delay	5 to 6	not applicable	not applicable
RX end delay	5 to 6	17 to 18	122 to 123

10.6.1.2 Allowed link decision time

The amount of clock cycles allocated to the link to respond to a received packet and correctly receive back-to-back packets is given in Table 24. Link designs must follow the values given in Table 24 for correct USB system operation. Examples of high-speed packet sequences and timing are shown in Figure 17 and Figure 18. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.3*.

Table 24.   Link decision times

Packet sequence	High-speed link delay	Full-speed link delay	Low-speed link delay	Definition
Transmit-Transmit (host only)	15 to 24	7 to 18	77 to 247	Number of clock cycles a host link must wait before driving the TXCMD for the second packet.
				In high speed, the link starts counting from the assertion of STP for the first packet.
				In full speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the first packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Transmit (host or peripheral)	1 to 14	7 to 18	77 to 247	Number of clock cycles the link must wait before driving the TXCMD for the transmit packet.
				In high speed, the link starts counting from the end of the receive packet; deassertion of DIR or an RXCMD indicating RxActive is LOW.
				In full speed or low speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the receive packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Receive (peripheral only)	1	1	1	Minimum number of clock cycles between consecutive receive packets. The link must be capable of receiving both packets.
Transmit-Receive (host or peripheral)	92	80	718	Host or peripheral transmits a packet and will time-out after this number of clock cycles if a response is not received. Any subsequent transmission can occur after this time.

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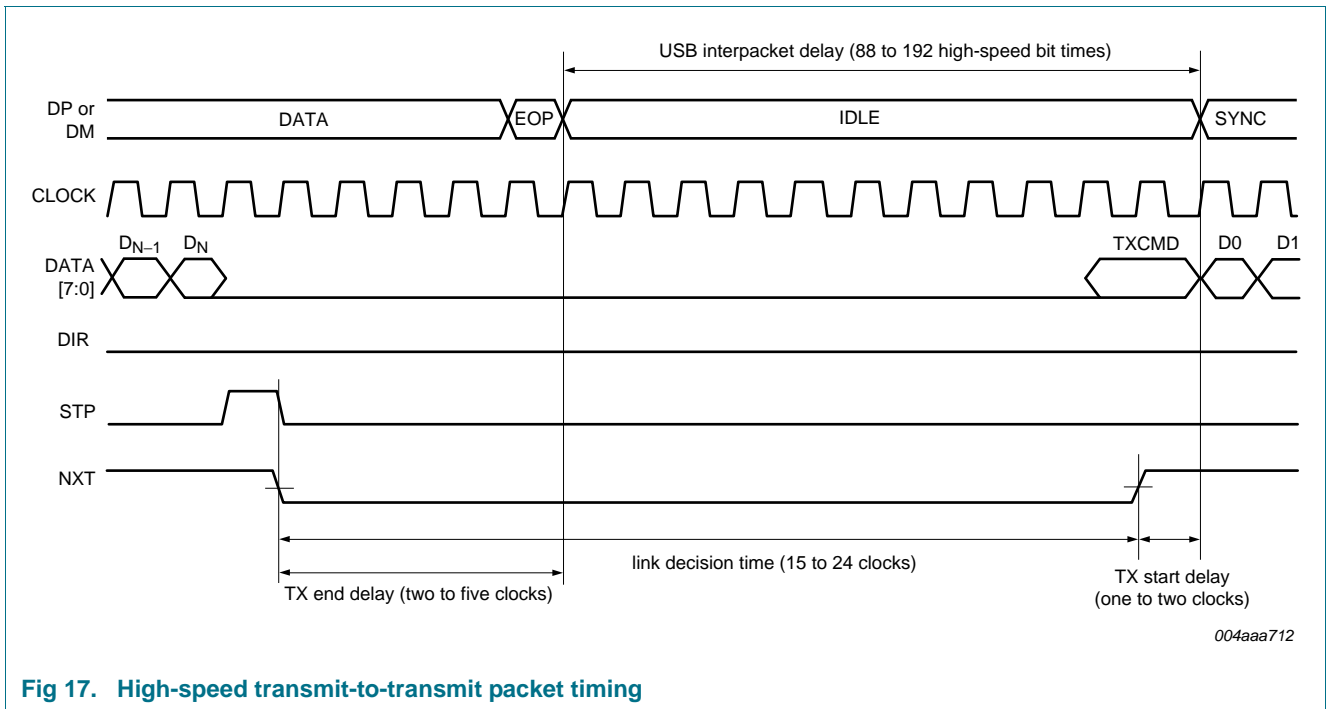
Fig 17.   High-speed transmit-to-transmit packet timing
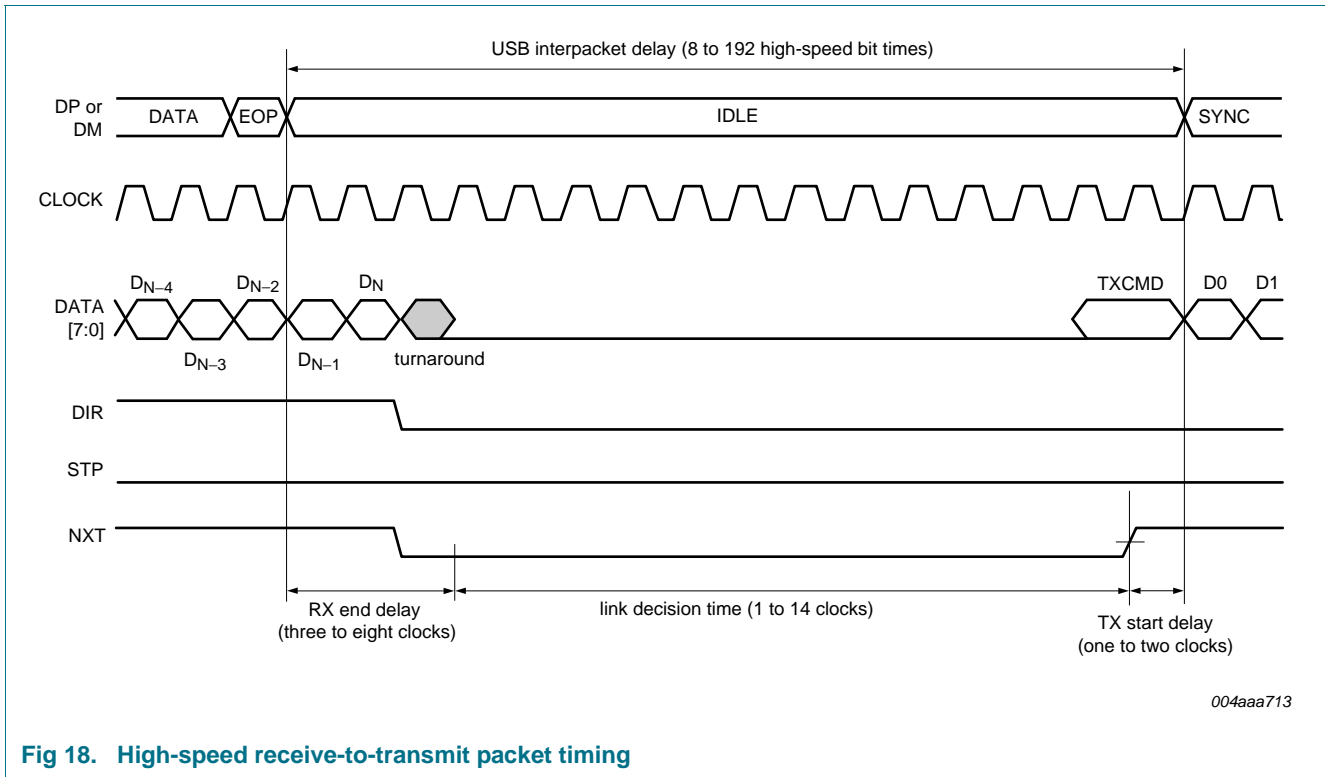
Fig 18.   High-speed receive-to-transmit packet timing

10.7 Preamble

Preamble packets are headers to low-speed packets that must travel over a full-speed bus, between a host and a hub. To enter preamble mode, the link sets XCVRSELECT[1:0] = 11b in the FUNC_CTRL register (see Section 11.5). When in preamble mode, the ISP1705 operates just as in full-speed mode, and sends all data with the full-speed rise time and fall time. Whenever the link transmits a USB packet in preamble mode, the ISP1705 will automatically send a preamble header at full-speed bit rate before sending the link packet at low-speed bit rate. The ISP1705 will ensure a minimum gap of four full-speed bit times between the last bit of the full-speed PRE PID and the first bit of the low-speed packet SYNC. The ISP1705 will drive a J for at least one full-speed bit time after sending the PRE PID, after which the pull-up resistor can hold the J state on the bus. An example transmit packet is shown in Figure 19.

In preamble mode, the ISP1705 can also receive low-speed packets from the full-speed bus.

DP and DM timing is not to scale.

Fig 19.   Preamble sequence
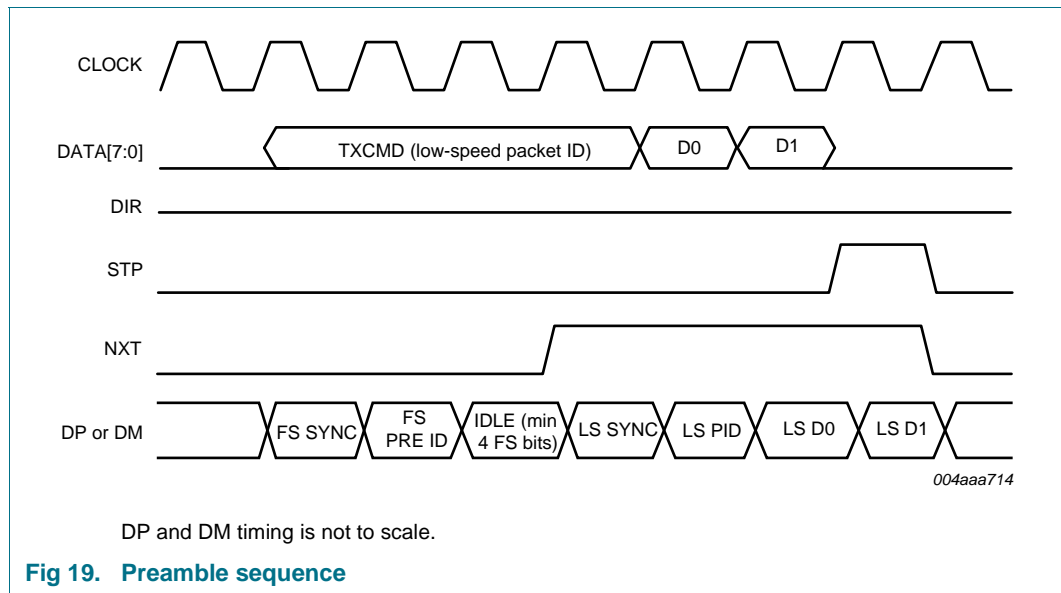
10.8 USB suspend and resume

10.8.1 Full-speed or low-speed host-initiated suspend and resume

Figure 20 illustrates how a host or a hub places a full-speed or low-speed peripheral into suspend and sometime later initiates resume signaling to wake-up the downstream peripheral. Note that Figure 20 timing is not to scale, and does not show all RXCMD LINESTATE updates.

The sequence of events for a host and a peripheral, both with ISP1705, is as follows:

1. Idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations are disabled (TERMSELECT is set to 1b). The peripheral has the 1.5 kΩ pull-up resistor connected to DP for full speed or DM for low speed (TERMSELECT is set to 1b).

2. Suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the PHY into low-power mode by clearing the SUSPENDM bit in the FUNC_CTRL register (see Section 11.5), causing the PHY to draw only suspend current. The host may or may not be powered down.

3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE[1:0] to 10b and transmits a K for at least 20 ms. The peripheral link sees the resume K on LINESTATE, and asserts STP to wake up the PHY.

4. EOP: When STP is asserted, the ISP1705 on the host side automatically appends an EOP of two bits of SE0 at low-speed bit rate, followed by one bit of J. The ISP1705 on the host side knows to add the EOP because DP_PULLDOWN and DM_PULLDOWN are set to 1b for a host. After the EOP is completed, the host link sets OPMODE[1:0] to 00b for normal operation. The peripheral link sees the EOP and also resumes normal operation.

Timing is not to scale.
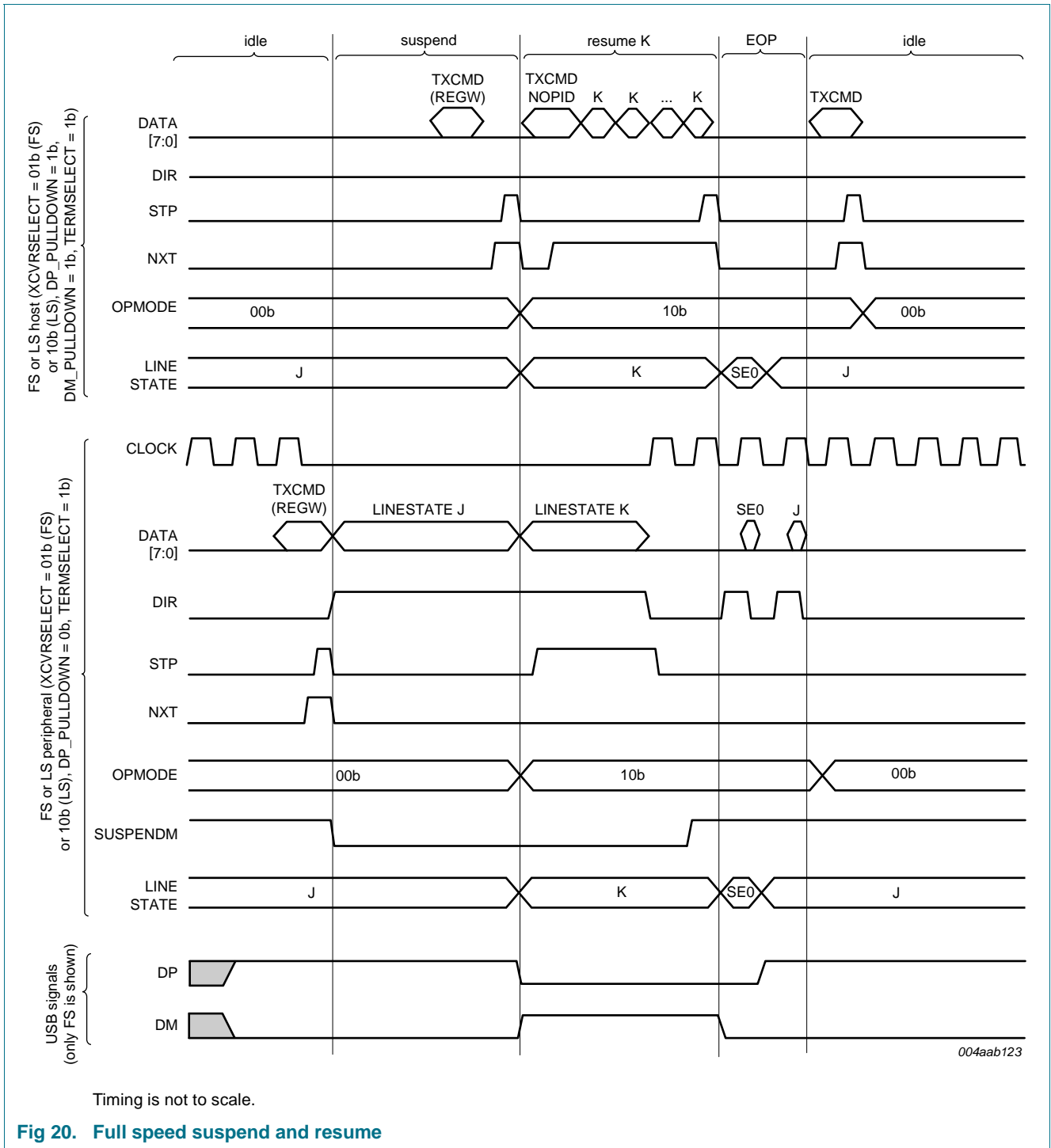
Fig 20. Full speed suspend and resume

10.8.2 High speed suspend and resume

Figure 21 illustrates how a host or a hub places a high-speed enabled peripheral into suspend and then initiates resume signaling. The high-speed peripheral will wake up and return to high-speed operations. Note that Figure 21 timing is not to scale, and does not show all RXCMD LINESTATE updates.

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The sequence of events related to a host and a peripheral, both with ISP1705, is as follows:

1. High speed idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations enabled (TERMSELECT is set to 0b). The peripheral has its 45 Ω terminations enabled (TERMSELECT is set to 0b).

2. Full speed suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the ISP1705 into full-speed mode (XCVRSELECT is set to 01b), removes 45 Ω terminations, and enables the 1.5 kΩ pull-up resistor on DP (TERMSELECT is set to 1b). The peripheral link then places the ISP1705 into low-power mode by clearing SUSPENDM, causing the ISP1705 to draw only suspend current. The host also changes the ISP1705 to full speed, (XCVRSELECT is set to 01b), removes 45 Ω terminations (TERMSELECT is set to 1b), and then may or may not be powered down.

3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE to 10b and transmits a full-speed K for at least 20 ms. The peripheral link sees the resume K (10b) on LINESTATE, and asserts STP to wake up the ISP1705.

4. High-speed traffic: The host link sets high speed (XCVRSELECT is set to 00b), and enables its 45 Ω terminations (TERMSELECT is set to 0b). The peripheral link sees SE0 on LINESTATE and also sets high speed (XCVRSELECT is set to 00b), and enables its 45 Ω terminations (TERMSELECT is set to 0b). The host link sets OPMODE to 00b for normal high-speed operation.

Timing is not to scale.
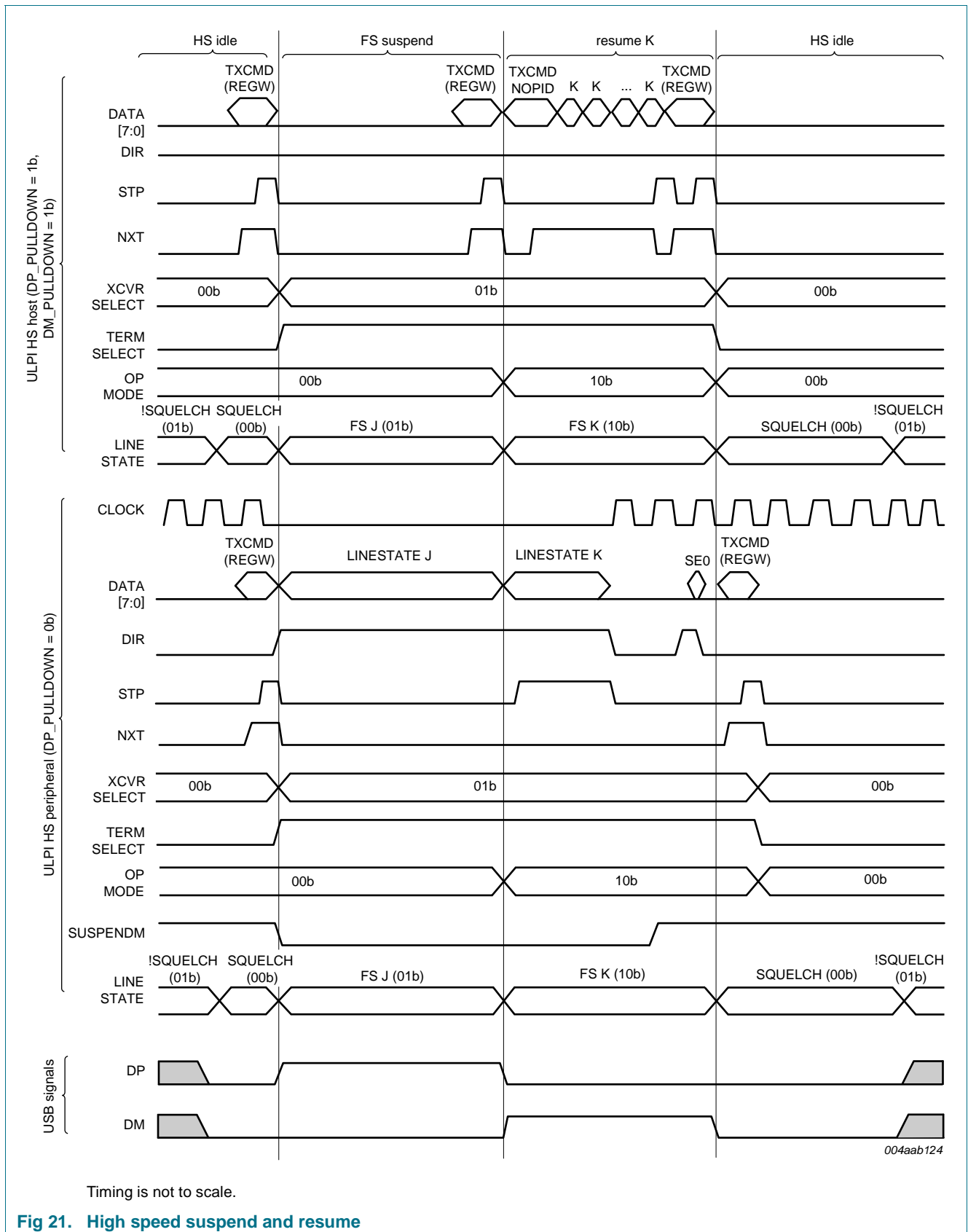
Fig 21. High speed suspend and resume

10.8.3 Remote wake-up

The ISP1705 supports peripherals that initiate remote wake-up resume. When placed into USB suspend, the peripheral link remembers at what speed it was originally operating. Depending on the original speed, the link follows one of the protocols detailed here. In Figure 22, timing is not to scale, and not all RXCMD LINESTATE updates are shown.

The sequence of events related to a host and a peripheral, both with ISP1705, is as follows:

1. Both the host and the peripheral are assumed to be in low-power mode.

2. The peripheral begins remote wake-up by re-enabling its clock and setting its SUSPENDM bit to 1b.

3. The peripheral begins driving K on the bus to signal resume. Note that the peripheral link must assume that LINESTATE is K (01b) while transmitting because it will not receive any RXCMDs.

4. The host recognizes the resume, re-enables its clock and sets its SUSPENDM bit.

5. The host takes over resume driving within 1 ms of detecting the remote wake-up.

6. The peripheral stops driving resume.

7. The peripheral sees the host continuing to drive the resume.

8. The host stops driving resume and the ISP1705 automatically adds the EOP to the end of the resume. The peripheral recognizes the EOP as the end of resume.

9. Both the host and the peripheral revert to normal operation by writing 00b to OPMODE. If the host or the peripheral was previously in high-speed mode, it must revert to high speed before the SE0 of the EOP is completed. This can be achieved by writing XCVRSELECT[1:0] = 00b and TERMSELECT = 0b after LINESTATE indicates SE0.

Timing is not to scale.
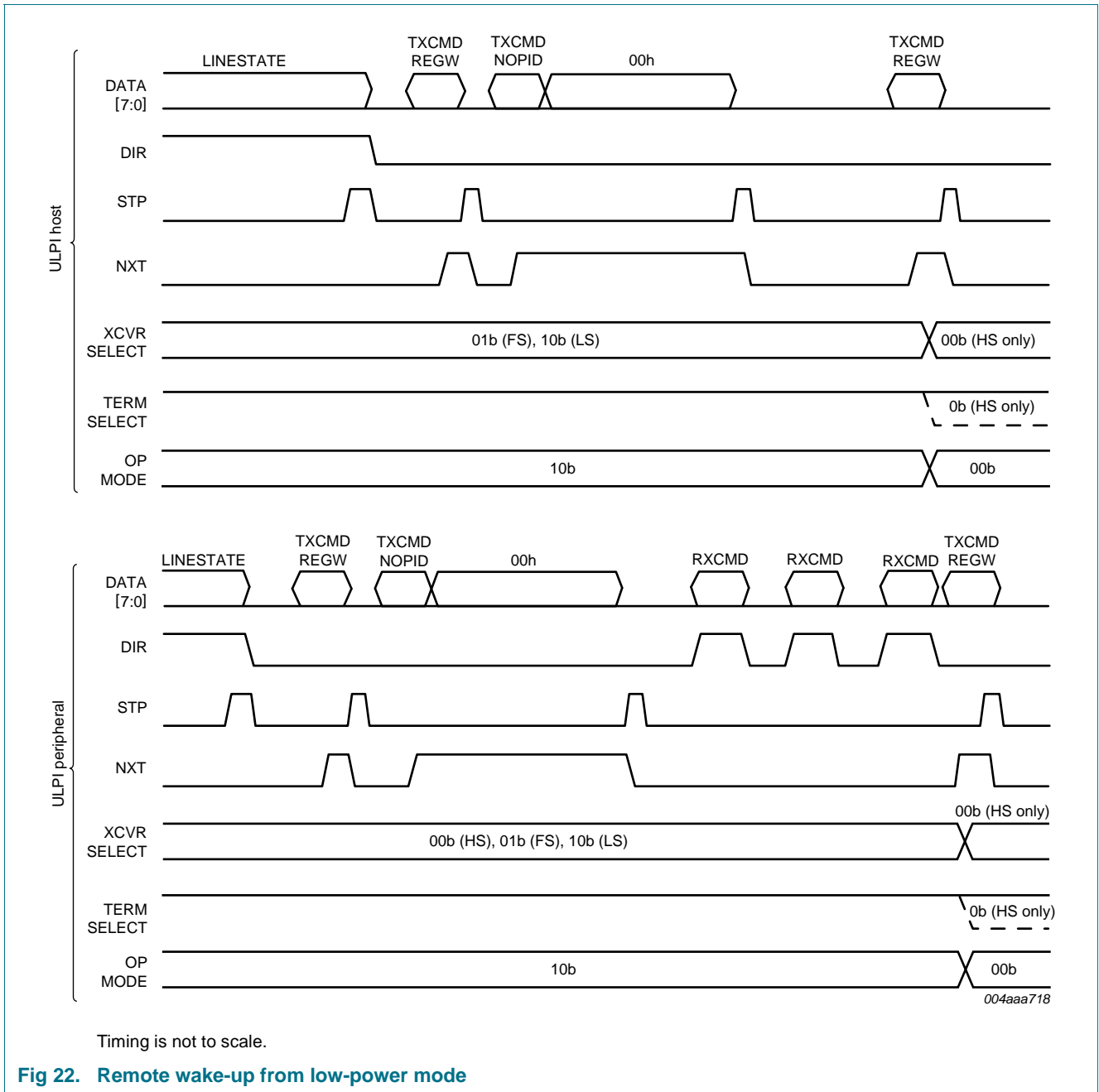
Fig 22.   Remote wake-up from low-power mode

10.9 No automatic SYNC and EOP generation (optional)

This setting allows the link to turn off the automatic SYNC and EOP generation, and must be used for high-speed packets only. It is provided for backwards compatibility with legacy controllers that include SYNC and EOP bytes in the data payload when transmitting packets. The ISP1705 will not automatically generate SYNC and EOP patterns when OPMODE[1:0] is set to 11b. The ISP1705 will still NRZI encode data and perform bit stuffing. An example of a sequence is shown in Figure 23. The link must always send packets using the TXCMD (NOPID) type. The ISP1705 does not provide a mechanism to control bit stuffing in individual bytes, but will automatically turn off bit stuffing for EOP when STP is asserted with data set to FEh. If data is set to 00h when STP is asserted, the

PHY will not transmit any EOP. The ISP1705 will also detect if the PID byte is A5h, indicating an SOF packet, and automatically send a long EOP when STP is asserted. To transmit chirp and resume signaling, the link must set OPMODE to 10b.
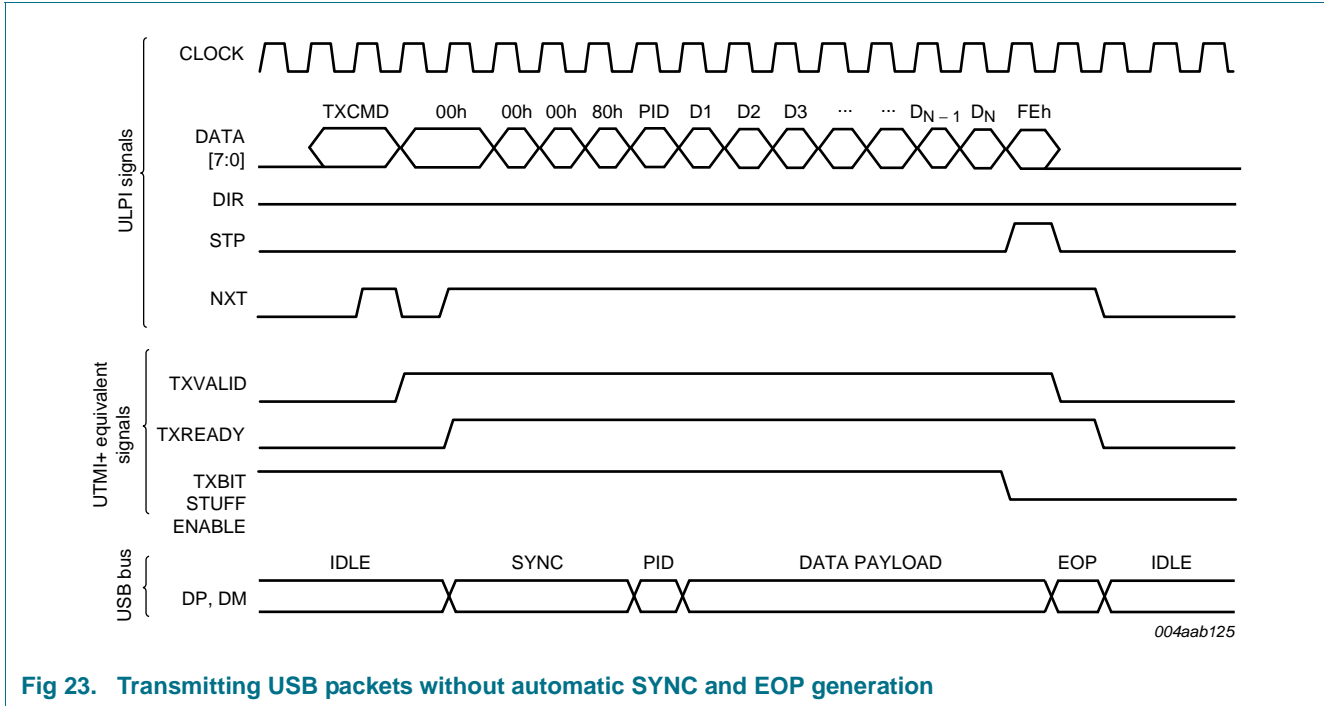
Fig 23. Transmitting USB packets without automatic SYNC and EOP generation

10.10 On-The-Go operations

On-The-Go (OTG) is a supplement to *Universal Serial Bus Specification Rev. 2.0* that allows a portable USB device to assume the role of a limited USB host by defining improvements, such as a small connector and low power. Non-portable devices, such as standard hosts and embedded hosts, can also benefit from OTG features.

The ISP1705 OTG PHY is designed to support all the tasks specified in the OTG supplement. The ISP1705 provides the front end analog support for Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices. The supporting components include:

- Voltage comparators
  - A_VBUS_VLD
  - SESS_VLD (session valid, can be used for both A-session and B-session valid)
  - SESS_END (session end)
- Pull-up and pull-down resistors on DP and DM
- ID detector indicates if micro-A or micro-B plug is inserted
- Charge and discharge resistors on V_{BUS}

The following subsections describe how to use the ISP1705 OTG components.

10.10.1 OTG comparators

The ISP1705 provides comparators that conform to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3* requirements of $V_{A\_VBUS\_VLD}$, $V_{A\_SESS\_VLD}$, $V_{B\_SESS\_VLD}$ and $V_{B\_SESS\_END}$. In this data sheet, $V_{A\_SESS\_VLD}$ and $V_{B\_SESS\_VLD}$ are combined into $V_{A\_SESS\_VLD}$. Comparators are described in Section 8.7.2. Changes in comparator values are communicated to the link by RXCMDs as described in Section 10.3.2. Control over comparators is described in Section 11.8 to Section 11.11.

10.10.2 Pull-up and pull-down resistors

The USB resistors on DP and DM can be used to initiate data-line pulsing SRP. The link must set the required bus state using the mode settings in Table 15.

10.10.3 ID detection

The ISP1705 provides an internal pull-up resistor to sense the state of the ID pin. The pull-up resistor must first be enabled by setting the ID_PULLUP register bit to logic 1. If the state of pin ID has changed, the ISP1705 will send an RXCMD or interrupt to the link by time t_{ID}. If the link does not receive any RXCMD or interrupt by t_{ID}, then the ID state has not changed.

10.10.4 V_{BUS} charge and discharge resistors

A pull-up resistor, $R_{UP(VBUS)}$, is provided to perform V_{BUS} pulsing SRP. A B-device is allowed to charge V_{BUS} above the session valid threshold to request the host to turn on the V_{BUS} voltage.

A pull-down resistor, $R_{DN(VBUS)}$, is provided for a B-device to discharge V_{BUS}. This is done whenever the A-device turns off the V_{BUS} voltage; the B-device can use the pull-down resistor to ensure V_{BUS} is below $V_{B\_SESS\_END}$ before starting a session.

For details, refer to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*.

10.11 Serial modes

The ISP1705 supports both 6-pin serial mode and 3-pin serial mode, controlled by bits 6PIN_FSLS_SERIAL and 3PIN_FSLS_SERIAL of the INTF_CTRL register (see Section 11.6). For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.10*.

Figure 24 and Figure 25 provide examples of 6-pin serial mode and 3-pin serial mode, respectively.
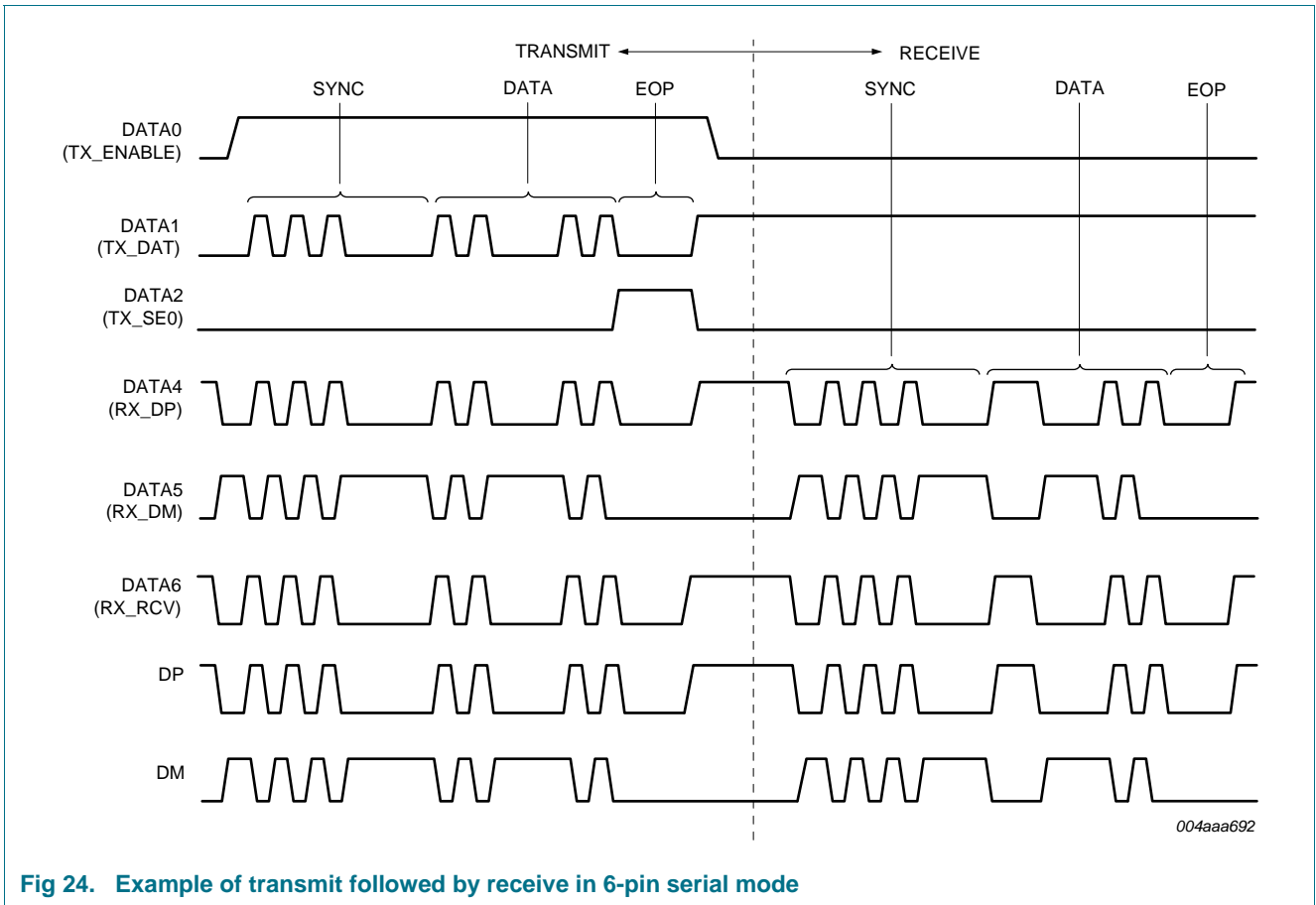
Fig 24. Example of transmit followed by receive in 6-pin serial mode
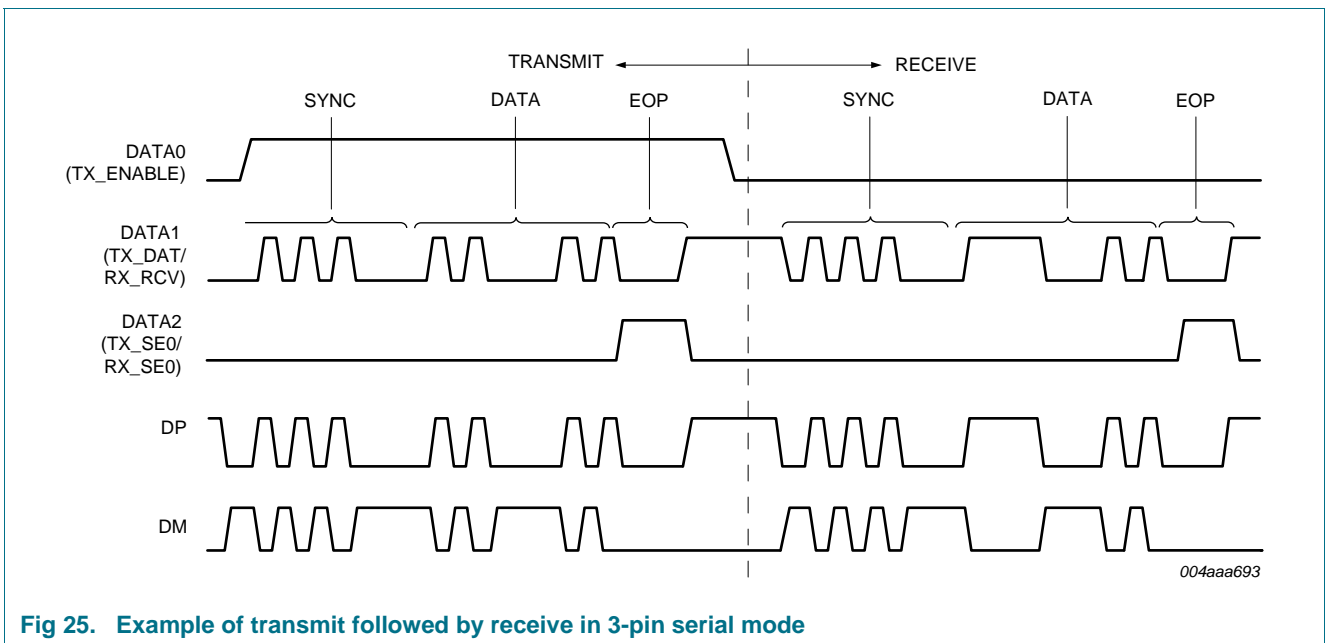
Fig 25. Example of transmit followed by receive in 3-pin serial mode

10.12 Aborting transfers

The ISP1705 supports aborting transfers on the ULPI bus. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.4*.

10.13 Avoiding contention on the ULPI data bus

Because the ULPI data bus is bidirectional, avoid situations in which both the link and the PHY simultaneously drive the data bus.

The following points must be considered while implementing the data bus drive control on the link.

After power-up and clock stabilization, default states are as follows:

- The ISP1705 drives DIR to LOW.
- The data bus is input to the ISP1705.
- The ULPI link data bus is output, with all data bus lines driven to LOW.

When the ISP1705 wants to take control of the data bus to initiate a data transfer, it changes the DIR state from LOW to HIGH.

At this point, the link must disable its output buffers. This must be as fast as possible so the link must use a combinational path from DIR.

The ISP1705 will not immediately enable its output buffers, but will delay the enabling of its buffers until the next clock edge, avoiding bus contention.

When the data transfer is no longer required by the ISP1705, it changes DIR from HIGH to LOW and starts to immediately turn off its output drivers. The link senses the change of DIR from HIGH to LOW, but delays enabling its output buffers for one CLOCK cycle, avoiding data bus contention.

11. Register map

Table 25.   Register map

Field name	Size (bit)	Address (6 bit)				References
		R[1]	W[2]	S[3]	C[4]	
VENDOR_ID_LOW	8	00h	-	-	-	Section 11.1 on page 52
VENDOR_ID_HIGH	8	01h	-	-	-	Section 11.2 on page 52
PRODUCT_ID_LOW	8	02h	-	-	-	Section 11.3 on page 53
PRODUCT_ID_HIGH	8	03h	-	-	-	Section 11.4 on page 53
FUNC_CTRL	8	04h to 06h	04h	05h	06h	Section 11.5 on page 53
INTF_CTRL	8	07h to 09h	07h	08h	09h	Section 11.6 on page 55
OTG_CTRL	8	0Ah to 0Ch	0Ah	0Bh	0Ch	Section 11.7 on page 56
USB_INTR_EN_R	8	0Dh to 0Fh	0Dh	0Eh	0Fh	Section 11.8 on page 58
USB_INTR_EN_F	8	10h to 12h	10h	11h	12h	Section 11.9 on page 58
USB_INTR_STAT	8	13h	-	-	-	Section 11.10 on page 59
USB_INTR_L	8	14h	-	-	-	Section 11.11 on page 59
DEBUG	8	15h	-	-	-	Section 11.12 on page 60
SCRATCH	8	16h to 18h	16h	17h	18h	Section 11.13 on page 61
CARKIT_CTRL	8	19h to 1Bh	19h	1Ah	1Bh	Section 11.14 on page 61
Reserved	8	1Ch to 3Ch	-	-	-	-
PWR_CTRL	8	3Dh to 3Fh	3Dh	3Eh	3Fh	Section 11.15 on page 62

[1]   Read (R): A register can be read. Read-only if this is the only mode given.

[2]   Write (W): The pattern on the data bus will be written over all bits of a register.

[3]   Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4]   Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

11.1   VENDOR_ID_LOW register

Table 26 shows the bit description of the register.

Table 26.   VENDOR_ID_LOW - Vendor ID low register (address R = 00h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ ID_LOW[7:0]	R	CCh*	**Vendor ID low**: Lower byte of the ST-NXP Wireless vendor ID supplied by USB-IF; fixed value of CCh

11.2   VENDOR_ID_HIGH register

Table 27 shows the bit description of the register.

Table 27.   VENDOR_ID_HIGH - Vendor ID high register (address R = 01h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ ID_HIGH[7:0]	R	04h*	**Vendor ID high**: Upper byte of the ST-NXP Wireless vendor ID supplied by USB-IF; fixed value of 04h

11.3 PRODUCT_ID_LOW register

The bit description of the register is given in Table 28.

Table 28.   PRODUCT_ID_LOW - Product ID low register (address R = 02h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_ LOW[7:0]	R	05h*	**Product ID low**: Lower byte of the ST-NXP Wireless product ID number; fixed value of 05h

11.4 PRODUCT_ID_HIGH register

The bit description of the register is given in Table 29.

Table 29.   PRODUCT_ID_HIGH - Product ID high register (address R = 03h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_ HIGH[7:0]	R	17h*	**Product ID high**: Upper byte of the ST-NXP Wireless product ID number; fixed value of 17h

11.5 FUNC_CTRL register

This register controls UTMI function settings of the PHY. The bit allocation of the register is given in Table 30.

Table 30.   FUNC_CTRL - Function control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	SUSPENDM	RESET	OPMODE[1:0]		TERM SELECT	XCVRSELECT[1:0]	
Reset	0	1	0	0	0	0	0	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 31.   FUNC_CTRL - Function control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description

Bit	Symbol	Description
7	-	reserved
6	SUSPENDM	**Suspend**: Active-LOW PHY suspend.
		Places the PHY into low-power mode. The PHY will power down all blocks, except the full-speed receiver, OTG comparators and ULPI interface pins.
		To come out of low-power mode, the link must assert STP. The PHY will automatically clear this bit when it exits low-power mode.
		0b — Low-power mode
		1b — Powered
5	RESET	**Reset**: Active-HIGH transceiver reset.
		After the link sets this bit, the PHY will assert DIR and reset the digital core. This does not reset the ULPI interface or the ULPI register set.
		When the reset is completed, the PHY will deassert DIR and automatically clear this bit, followed by an RXCMD update to the link.
		The link must wait for DIR to be deasserted before using the ULPI bus.
		0b — Do not reset
		1b — Reset

Table 31. **FUNC_CTRL - Function control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description** …*continued*

Bit	Symbol	Description
4 to 3	OPMODE[1:0]	**Operation mode**: Selects the required bit-encoding style during transmit. **00b —** Normal operation **01b —** Non-driving **10b —** Disable bit-stuffing and NRZI encoding **11b —** Do not automatically add SYNC and EOP when transmitting; must be used only for high-speed packets
2	TERMSELECT	**Termination select**: Controls the internal 1.5 kΩ full-speed pull-up resistor and 45 Ω high-speed terminations. Control over bus resistors changes, depending on XCVRSELECT[1:0], OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN, as shown in Table 15.
1 to 0	XCVRSELECT[1:0]	**Transceiver select**: Selects the required transceiver speed. **00b —** Enable the high-speed transceiver **01b —** Enable the full-speed transceiver **10b —** Enable the low-speed transceiver **11b —** Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)

11.6 INTF_CTRL register

The INTF_CTRL register enables alternative interfaces. All of these modes are optional features provided for legacy link cores. Setting more than one of these fields results in undefined behavior. Table 32 provides the bit allocation of the register.

Table 32. **INTF_CTRL - Interface control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	INTF_ PROT_DIS	IND_PASS THRU	IND_ COMPL	reserved	CLOCK_ SUSPENDM	CARKIT_ MODE	3PIN_ FSLS_ SERIAL	6PIN_ FSLS_ SERIAL
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 33. **INTF_CTRL - Interface control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit description**

Bit	Symbol	Description
7	INTF_PROT_DIS	**Interface protect disable**: Controls circuitry built into the ISP1705 to protect the ULPI interface when the link 3-states STP and DATA[7:0]. When this bit is enabled, the ISP1705 will automatically detect when the link stops driving STP.
		0b — Enables the interface protect circuit. The ISP1705 attaches a weak pull-up resistor on STP. If STP is unexpectedly HIGH, the ISP1705 attaches weak pull-down resistors on DATA[7:0], protecting data inputs
		1b — Disables the interface protect circuit, detaches weak pull-down resistors on DATA[7:0], and a weak pull-up resistor on STP
6	IND_PASSTHRU	**Indicator pass-through**: Controls whether the complement output is qualified with the internal A_VBUS_VLD comparator before being used in the V_{BUS} state in RXCMD.
		0b — The complement output signal is qualified with the internal A_VBUS_VLD comparator
		1b — The complement output signal is not qualified with the internal A_VBUS_VLD comparator
5	IND_COMPL	**Indicator complement**: Informs the PHY to invert the FAULT input signal, generating the complement output.
		0b — The ISP1705 will not invert the FAULT signal
		1b — The ISP1705 will invert the FAULT signal
4	-	reserved
3	CLOCK_SUSPENDM	**Clock suspend**: Active-LOW clock suspend.
		Powers down the internal clock circuitry only. By default, the clock will not be powered in 6-pin serial mode or 3-pin serial mode.
		Valid only in 6-pin serial mode and 3-pin serial mode. Valid only when SUSPENDM is set to logic 1, otherwise this bit is ignored.
		0b — Clock will not be powered in 3-pin or 6-pin serial mode or UART mode
		1b — Clock will be powered in 3-pin and 6-pin serial mode or UART mode

Table 33. INTF_CTRL - Interface control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit description *…continued*

Bit	Symbol	Description
2	CARKIT_MODE	**Carkit mode**: Changes the ULPI interface to the carkit interface (UART mode). Bits TXD_EN and RXD_EN in the CARKIT_CTRL register (see Section 11.14) must change as well. The PHY must automatically clear this bit when carkit mode is exited.
		0b — Disable carkit mode
		1b — Enable carkit mode
1	3PIN_FSLS_SERIAL	**3-pin full-speed low-speed serial mode**: Changes the ULPI interface to a 3-bit serial interface. The ISP1705 will automatically clear this bit when 3-pin serial mode is exited.
		0b — Full-speed or low-speed packets are sent using the parallel interface
		1b — Full-speed or low-speed packets are sent using the 3-pin serial interface
0	6PIN_FSLS_SERIAL	**6-pin full-speed low-speed serial mode**: Changes the ULPI interface to a 6-bit serial interface. The ISP1705 will automatically clear this bit when 6-pin serial mode is exited.
		0b — Full-speed or low-speed packets are sent using the parallel interface
		1b — Full-speed or low-speed packets are sent using the 6-pin serial interface

11.7 OTG_CTRL register

This register controls various OTG functions of the ISP1705. The bit allocation of the OTG_CTRL register is given in Table 34.

Table 34. OTG_CTRL - OTG control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USE_EXT_ VBUS_IND	DRV_ VBUS_EXT	reserved	CHRG_ VBUS	DISCHRG_ VBUS	DM_PULL DOWN	DP_PULL DOWN	ID_PULL UP[1]
Reset	0	0	0	0	0	1	1	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

[1] A weak pull-up, which can detect ID correctly, is present when the ID_PULLUP bit is disabled. It is, however, mandatory that the link enables ID_PULLUP.

Table 35. **OTG_CTRL - OTG control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit description**

Bit	Symbol	Description
7	USE_EXT_ VBUS_IND	**Use external V$_{BUS}$ indicator**: Informs the PHY to use an external V$_{BUS}$ overcurrent indicator. **0b —** Use the internal OTG comparator **1b —** Use the external V$_{BUS}$ valid indicator signal input from the FAULT pin
6	DRV_VBUS_EXT	**Drive V$_{BUS}$ external**: Controls the external charge pump or 5 V supply by the PSW_N pin. **0b —** PSW_N is HIGH **1b —** PSW_N to LOW
5	reserved	-
4	CHRG_VBUS	**Charge V$_{BUS}$**: Charges V$_{BUS}$ through a resistor. Used for the V$_{BUS}$ pulsing of SRP. The link must first check that V$_{BUS}$ is discharged (see bit DISCHRG_VBUS), and that both the DP and DM data lines have been LOW (SE0) for 2 ms. **0b —** Do not charge V$_{BUS}$ **1b —** Charge V$_{BUS}$
3	DISCHRG_VBUS	**Discharge V$_{BUS}$**: Discharges V$_{BUS}$ through a resistor. If the link sets this bit to logic 1, it waits for an RXCMD indicating that SESS_END has changed from logic 0 to logic 1, and then resets this bit to logic 0 to stop the discharge. **0b —** Do not discharge V$_{BUS}$ **1b —** Discharge V$_{BUS}$
2	DM_PULLDOWN	**DM pull down**: Enables the 15 kΩ pull-down resistor on DM. **0b —** pull-down resistor is not connected to DM **1b —** pull-down resistor is connected to DM
1	DP_PULLDOWN	**DP pull down**: Enables the 15 kΩ pull-down resistor on DP. **0b —** Pull-down resistor is not connected to DP **1b —** Pull-down resistor is connected to DP
0	ID_PULLUP	**ID pull up**: Connects a pull-up to the ID line and enables sampling of the ID level. Disabling the ID line sampler will reduce the PHY power consumption. **0b —** Disable sampling of the ID line **1b —** Enable sampling of the ID line

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11.8 USB_INTR_EN_R register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB_INTR_STAT register change from logic 0 to logic 1. By default, all transitions are enabled. Table 36 shows the bit allocation of the register.

Table 36.   USB_INTR_EN_R - USB interrupt enable rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol		reserved		ID_GND_R	SESS_ END_R	SESS_ VALID_R	VBUS_ VALID_R	HOST_ DISCON_R
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 37.   USB_INTR_EN_R - USB interrupt enable rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_R	**ID ground rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on ID_GND.
3	SESS_END_R	**Session end rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_END.
2	SESS_VALID_R	**Session valid rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_VLD.
1	VBUS_VALID_R	**V_{BUS} valid rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on A_VBUS_VLD.
0	HOST_DISCON_R	**Host disconnect rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on HOST_DISCON.

11.9 USB_INTR_EN_F register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB_INTR_STAT register change from logic 1 to logic 0. By default, all transitions are enabled. See Table 38.

Table 38.   USB_INTR_EN_F - USB interrupt enable falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol		reserved		ID_GND_F	SESS_ END_F	SESS_ VALID_F	VBUS_ VALID_F	HOST_ DISCON_F
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 39.   USB_INTR_EN_F - USB interrupt enable falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_F	**ID ground fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on ID_GND.
3	SESS_END_F	**Session end fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_END.
2	SESS_VALID_F	**Session valid fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_VLD.
1	VBUS_VALID_F	V_{BUS} **valid fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on A_VBUS_VLD.
0	HOST_DISCON_F	**Host disconnect fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on HOST_DISCON.

11.10   USB_INTR_STAT register

This register (see Table 40) indicates the current value of the interrupt source signal.

Table 40.   USB_INTR_STAT - USB interrupt status register (address R = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND	SESS_ END	SESS_ VALID	VBUS_ VALID	HOST_ DISCON
Reset	X	X	X	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 41.   USB_INTR_STAT - USB interrupt status register (address R = 13h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND	**ID ground**: Reflects the current state of the ID detector circuit.
3	SESS_END	**Session end**: Reflects the current value of the session end voltage comparator.
2	SESS_VALID	**Session valid**: Reflects the current value of the session valid voltage comparator.
1	VBUS_VALID	V_{BUS} **valid**: Reflects the current value of the V_{BUS} valid voltage comparator.
0	HOST_DISCON	**Host disconnect**: Reflects the current value of the host disconnect detector.

11.11   USB_INTR_L register

The bits of the USB_INTR_L register are automatically set by the ISP1705 when an unmasked change occurs on the corresponding interrupt source signal. The ISP1705 will automatically clear all bits when the link reads this register, or when the PHY enters low-power mode.

Remark: It is optional for the link to read this register when the clock is running because all signal information will automatically be sent to the link through the RXCMD byte.

The bit allocation of this register is given in Table 42.

Table 42.   USB_INTR_L - USB interrupt latch register (address R = 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_L	SESS_ END_L	SESS_ VALID_L	VBUS_ VALID_L	HOST_ DISCON_L
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 43.   USB_INTR_L - USB interrupt latch register (address R = 14h) bit description

Bit	Symbol	Description
7 to 5	reserved	-
4	ID_GND_L	**ID ground latch**: Automatically set when an unmasked event occurs on ID_GND. Cleared when this register is read.
3	SESS_END_L	**Session end latch**: Automatically set when an unmasked event occurs on SESS_END. Cleared when this register is read.
2	SESS_VALID_L	**Session valid latch**: Automatically set when an unmasked event occurs on SESS_VLD. Cleared when this register is read.
1	VBUS_VALID_L	V_{BUS} **valid latch**: Automatically set when an unmasked event occurs on A_VBUS_VLD. Cleared when this register is read.
0	HOST_DISCON_L	**Host disconnect latch**: Automatically set when an unmasked event occurs on HOST_DISCON. Cleared when this register is read.

11.12 DEBUG register

The bit allocation of the DEBUG register is given in Table 44. This register indicates the current value of signals useful for debugging.

Table 44.   DEBUG - Debug register (address R = 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						LINE STATE1	LINE STATE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 45.   DEBUG - Debug register (address R = 15h) bit description

Bit	Symbol	Description
7 to 2	-	reserved
1	LINESTATE1	**Line state 1**: Contains the current value of LINESTATE 1
0	LINESTATE0	**Line state 0**: Contains the current value of LINESTATE 0

11.13 SCRATCH register

This is a 1-byte empty register for testing purposes, see Table 46.

Table 46. SCRATCH - Scratch register (address R = 16h to 18h, W = 16h, S = 17h, C = 18h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	SCRATCH[7:0]	R/W/S/C	00h	**Scratch**: This is an empty register byte for testing purposes. Software can read, write, set and clear this register. The functionality of the PHY will not be affected.

11.14 CARKIT_CTRL register

This register controls transparent UART mode. This register is only valid when the CARKIT_MODE bit in the INTF_CTRL register (see Section 11.6) is set. When entering UART mode, set the CARKIT_MODE bit, and then set the TXD_EN and RXD_EN bits. After entering UART mode, the ULPI interface is not available. When exiting UART mode, assert the STP pin or perform a hardware reset using chip select.

For bit allocation, see Table 47.

Table 47. CARKIT_CTRL - Carkit control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				RXD_EN	TXD_EN	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 48. CARKIT_CTRL - Carkit control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit description

Bit	Symbol	Description
7 to 4	-	reserved; the link must never write logic 1 to these bits
3	RXD_EN	**RXD enable**: Routes the UART RXD signal from the DP pin to the DATA1 pin. This bit will automatically be cleared when UART mode is exited.
2	TXD_EN	**TXD enable**: Routes the UART TXD signal from the DATA0 pin to the DM pin. This bit will automatically be cleared when UART mode is exited.
1 to 0	-	reserved; the link must never write logic 1 to these bits

11.15 PWR_CTRL register

This vendor-specific register controls the power feature of the ISP1705. The bit allocation of the register is given in Table 49.

Table 49. **PWR_CTRL - Power control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			DP_WKPU_EN	BVALID_FALL	BVALID_RISE	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 50. **PWR_CTRL - Power control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit description**

Bit	Symbol	Description
7 to 5	-	reserved; the link must never write logic 1 to these bits
4	DP_WKPU_EN	**DP weak pull-up enable**: Enable the weak pull-up resistor on the DP pin ($R_{weakUP(DP)}$) in synchronous mode when V_{BUS} is above the $V_{A\_SESS\_VLD}$ threshold. Note that when the ISP1705 is in UART mode, the DP weak pull-up will be enabled, regardless of the value of this register bit. **0 —** DP weak pull-up is disabled. **1 —** DP weak pull-up is enabled when $V_{BUS} > V_{A\_SESS\_VLD}$.
3	BVALID_FALL	**BVALID fall**: Enables RXCMDs for HIGH-to-LOW transitions on BVALID. When BVALID changes from HIGH to LOW, the ISP1705 will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
2	BVALID_RISE	**BVALID rise**: Enables RXCMDs for LOW-to-HIGH transitions on BVALID. When BVALID changes from LOW to HIGH, the ISP1705 will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
1 to 0	-	reserved; the link must never write logic 1 to these bits

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12. Limiting values

Table 51. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage			−0.5	+4.6	V
V_I	input voltage	on pins PSW_N and FAULT		−0.5	+5.5	V
		on pins CLOCK, STP, DATA[7:0], CFG1, CFG2, RESET_N, CHIP_SEL and CHIP_SEL_N		−0.5	$V_{CC(I/O)}$ + 0.5	V
		on pins ID and CFG0		−0.5	+4.6	V
		on pin XTAL1		−0.5	+2.5	V
		on pins DP and DM	[1]	−0.5	+4.6	V
		on pin V_{BUS}	[2]	−0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	human body model (JESD22-A114D)		−2	+2	kV
		machine model (JESD22-A115-A)		−200	+200	V
		charged device model (JESD22-C101-C)		−500	+500	V
		IEC 61000-4-2 contact on pins DP and DM	[3]	−8	+8	kV
I_{lu}	latch-up current			-	100	mA
T_{stg}	storage temperature			−60	+125	°C

[1] The ISP1705 has been tested according to the additional requirements listed in *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The short circuit withstand test and the AC stress test were performed for 24 hours, and the ISP1705 was found to be fully operational after the test completed.

[2] When an external series resistor is added to the V_{BUS} pin, it can withstand higher voltages for longer periods of time because the resistor limits the current flowing into the V_{BUS} pin. For example, with an external 1 kΩ resistor, V_{BUS} can tolerate 10 V for at least 5 seconds. Actual performance may vary depending on the resistor used and whether other components are connected to V_{BUS}.

[3] The ISP1705 has been tested in-house according to the IEC 61000-4-2 standard on the DP and DM pins. It is recommended that customers perform their own ESD tests, depending on application requirements.

13. Recommended operating conditions

Table 52. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	3.6	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		3.0	3.3	3.6	V
V_I	input voltage	on pins PSW_N, FAULT and V_{BUS}	0	-	5.25	V
		on pins CLOCK, STP, DATA[7:0], CFG1, CFG2, RESET_N, CHIP_SEL and CHIP_SEL_N	0	-	$V_{CC(I/O)}$	V
		on pins DP, DM, ID and CFG0	0	-	3.6	V
		on pin XTAL1	0	-	1.95	V
T_j	junction temperature		−40	-	+125	°C
T_{amb}	ambient temperature		−40	+25	+85	°C

14. Static characteristics

Table 53. Static characteristics: supply pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR(trip)}$	power-on reset trip voltage	on pin REG1V8	0.95	-	1.5	V
I_{CC}	supply current	Power-down mode ($V_{CC(I/O)}$ is lost or chip select is non-active)	-	0.5	10	µA
		full-speed transceiver; bus idle; no USB activity	-	13	-	mA
		high-speed transceiver; bus idle; no USB activity	-	51	-	mA
		full-speed transceiver; 100 % transmission; no inter-packet delay	-	25.65	-	mA
		high-speed transceiver; 100 % transmission; no inter-packet delay	-	55.30	55.30	mA
		low-power mode (bit SUSPENDM = 0b); V_{BUS} valid detector disabled (bits VBUS_VALID_R and VBUS_VALID_F are cleared)				
		for host	-	70	100	µA
		for peripheral	-	240	330	µA
		UART mode; low-speed transceiver; idle	-	750	-	µA
		UART mode; full-speed transceiver; idle	-	600	-	µA
$I_{CC(I/O)(stat)}$	static supply current on pin $V_{CC(I/O)}$	Power-down mode (chip select is non-active)	-	-	10	µA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	ULPI bus idle; 15 pF load on pin CLOCK [1]	-	2	-	mA

[1] The actual value of $I_{CC(I/O)}$ varies depending on the capacitance loading, interface voltage and bus activity. Use the value provided here only as a reference.

Table 54. Static characteristics: full-speed serial

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	with UPLI CLOCK and PLL blocks off (bit CLOCK_SUSPENDM cleared; default); 1.8 m USB cable connected				
		transmitting (maximum toggling)	-	17	-	mA
		receiving	-	5	-	mA
		idle	-	4	-	mA
		with UPLI CLOCK and PLL blocks on (bit CLOCK_SUSPENDM set); 1.8 m USB cable connected				
		transmitting (maximum toggling)	-	26	-	mA
		receiving	-	14	-	mA
		idle	-	13	-	mA

[1] This current consumption is applicable only when the ISP1705 is interfaced to links that can configure and work in serial mode.

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Table 55. Static characteristics: digital pins

Digital pins: CLOCK, DIR, STP, NXT, DATA[7:0], CHIP_SEL_N, CHIP_SEL, CFG1, CFG2 and RESET_N; unless otherwise specified.
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IH}	HIGH-level input voltage		$0.7V_{CC(I/O)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
I_{LI}	input leakage current		−1	-	+1	µA
Output levels						
V_{OH}	HIGH-level output voltage	I_{OL} = +2 mA	$V_{CC(I/O)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OH} = −2 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC(I/O)} - 0.4$ V	8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	8	-	-	mA
Impedance						
Z_L	load impedance		45	-	65	Ω
Pull-up and pull-down						
I_{pu}	pull-up current	interface protect enabled; STP pin only; V_I = 0 V	−30	−50	−80	µA
		UART mode; DATA0 pin only	−30	−50	−80	µA
I_{pd}	pull-down current	interface protect enabled; DATA[7:0] pins only; $V_I = V_{CC(I/O)}$	25	50	95	µA
Capacitance						
C_{in}	input capacitance		-	-	2.9	pF

Table 56. Static characteristics: digital input pin FAULT

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V	−1	-	-	µA
I_{IH}	HIGH-level input current	V_I = 5.25 V	-	-	1	µA

Table 57. Static characteristics: digital output pin PSW_N

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	external pull-up resistor connected	3.0[1]	-	5.25	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	external pull-up resistor connected	-	-	1	µA
I_{OL}	LOW-level output current	V_O = 0.4 V	4.0	-	-	mA

[1] When V_{OH} is less than $V_{O(REG3V3)}$, I_{CC} may increase because of the cross current.

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Table 58. Static characteristics: analog pins (DP, DM)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Original USB transceiver (full speed and low speed)						
Input levels (differential data receiver)						
V_{DI}	differential input sensitivity voltage	$\|V_{DP} - V_{DM}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pull-up on DP; R_L = 1.5 kΩ to 3.6 V	0.0	-	0.3	V
V_{OH}	HIGH-level output voltage	pull-down on pins DP and DM; R_L = 15 kΩ to GND	2.8	-	3.6	V
V_{CRS}	output signal crossover voltage	excluding the first transition from the idle state	1.3	-	2.0	V
Termination						
V_{TERM}	termination voltage for upstream facing port pull-up	for 1.5 kΩ pull-up resistor	3.0	-	3.6	V
Resistance						
$R_{UP(DP)}$	pull-up resistance on pin DP		1425	1500	1575	Ω
$R_{weakUP(DP)}$	weak pull-up resistance on pin DP	bit DP_WKPU_EN = 1b and V_{BUS} > $V_{A\_SESS\_VLD}$	100	125	150	kΩ
Hi-Speed USB transceiver (HS)						
Input levels						
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)		100	-	150	mV
V_{HSDSC}	high-speed disconnect detection threshold voltage (differential signal amplitude)		525	-	625	mV
V_{HSDI}	high-speed differential input sensitivity	$\|V_{DP} - V_{DM}\|$	300	-	-	mV
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)	includes V_{DI} range	−50	-	+500	mV
Output levels						
V_{HSOI}	high-speed idle level voltage		−10	-	+10	mV
V_{HSOL}	high-speed data signaling LOW-level voltage		−10	-	+10	mV
V_{HSOH}	high-speed data signaling HIGH-level voltage		360	-	440	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		−900	-	−500	mV

Table 58.   Static characteristics: analog pins (DP, DM) …continued

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Leakage current						
I_{LZ}	off-state leakage current		−1.0	-	+1.0	μA
Capacitance						
C_{in}	input capacitance	pin to GND	-	-	5	pF
Resistance						
$R_{DN(DP)}$	pull-down resistance on pin DP		14.25	15	15.75	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM		14.25	15	15.75	kΩ
Termination						
$Z_{O(drv)(DP)}$	driver output impedance on pin DP	steady-state drive	40.5	45	49.5	Ω
$Z_{O(drv)(DM)}$	driver output impedance on pin DM	steady-state drive	40.5	45	49.5	Ω
Z_{INP}	input impedance exclusive of pull-up/pull-down (for low-/full-speed)		1	-	-	MΩ
UART mode						
Input levels						
V_{IL}	LOW-level input voltage	pin DP	-	-	0.8	V
V_{IH}	HIGH-level input voltage	pin DP	2.35	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pin DM; I_{OL} = −4 mA	-	-	0.3	V
V_{OH}	HIGH-level output voltage	pin DM; I_{OH} = +4 mA	2.4	-	-	V

Table 59.   Static characteristics: analog pin V_{BUS}

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Comparators						
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	4.75	V
$V_{A\_SESS\_VLD}$	A-device session valid voltage	for A-device and B-device	0.8	1.6	2.0	V
$V_{hys(A\_SESS\_VLD)}$	A-device session valid hysteresis voltage	for A-device and B-device	-	100	-	mV
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to REG3V3 when CHRG_VBUS = 1b	281	680	-	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when DISCHRG_VBUS = 1b	656	1200	-	Ω
$R_{I(idle)(VBUS)}$	idle input resistance on pin V_{BUS}	not in Power-down mode	75	90	100	kΩ
		chip deasserted (Power-down mode)	40	-	100	kΩ
		$V_{CC(I/O)}$ lost (Power-down mode)	140	-	220	kΩ

Table 60.   Static characteristics: analog pin CFG0

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{LI}	input leakage current		−1	-	+1	µA

Table 61.   Static characteristics: ID detection circuit

V_{CC} = 3.0 to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ID}	ID detection time		50	-	-	ms
$V_{th(ID)}$	ID detector threshold voltage		1.0	-	2.0	V
$R_{UP(ID)}$	ID pull-up resistance	bit ID_PULLUP = 1b	40	50	60	kΩ
$R_{weakPU(ID)}$	weak pull-up resistance on pin ID	bit ID_PULLUP = 0b	320	400	480	kΩ
$V_{PU(ID)}$	pull-up voltage on pin ID		3.0	3.3	3.6	V

Table 62.   Static characteristics: resistor reference

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.
SUSPENDM = HIGH.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(RREF)}$	output voltage on pin RREF		-	1.22	-	V

Table 63.   Static characteristics: regulator

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.
SUSPENDM = HIGH.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(REG1V8)}$	output voltage from internal 1.8 V regulator		1.65	1.8	1.95	V
$V_{O(REG3V3)}$	output voltage from internal 3.3 V regulator	not in UART mode	3.0	3.3	3.6	V
		in UART mode	2.5	2.77	2.9	V

Table 64.   Static characteristics: pin XTAL1

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		-	-	0.37	V
V_{IH}	HIGH-level input voltage		1.32	-	-	V

15. Dynamic characteristics

Table 65. Dynamic characteristics: reset and power

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{W(POR)}$	internal power-on reset pulse width		0.2	-	-	µs
$t_{w(REG1V8\_H)}$	REG1V8 HIGH pulse width		-	-	2	µs
$t_{w(REG1V8\_L)}$	REG1V8 LOW pulse width		-	-	11	µs
$t_{W(RESET\_N)}$	external RESET_N pulse width		200	-	-	ns
$t_{startup(PLL)}$	PLL start-up time	measured after $t_{d(det)clk(osc)}$	-	-	640	µs
$t_{d(det)clk(osc)}$	oscillator clock detector delay	measured from regulator start-up time	-	-	640	µs
t_{PWRUP}	regulator start-up time	4.7 µF ± 20 % capacitor each on pins REG1V8 and REG3V3	-	-	1	ms
t_{PWRDN}	regulator power-down time	4.7 µF ± 20 % capacitor each on pins REG1V8 and REG3V3	-	-	100	ms

Table 66. Dynamic characteristics: clock applied to XTAL1

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{i(XTAL1)}$	input frequency on pin XTAL1	see Table 6	-	26.000	-	MHz
		see Table 6	-	24.000	-	MHz
		see Table 6	-	19.300	-	MHz
		see Table 6	-	13.000	-	MHz
$t_{jit(i)(XTAL1)RMS}$	RMS input jitter on pin XTAL1		-	-	200	ps
$\Delta f_{i(XTAL1)}$	input frequency tolerance on pin XTAL1		-	-	200	ppm
$\delta_{i(XTAL1)}$	input duty cycle on pin XTAL1	for the first transaction [1]	-	50	-	%
$t_{r(XTAL1)}$	rise time on pin XTAL1	only for square wave input	-	-	5	ns
$t_{f(XTAL1)}$	fall time on pin XTAL1	only for square wave input	-	-	5	ns

[1] The internal PLL is triggered only on the positive edge from the crystal oscillator. Therefore, the duty cycle is not critical.

Table 67. Dynamic characteristics: CLOCK output

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(AV)(CLOCK)}$	average output frequency on pin CLOCK		59.970	60.000	60.030	MHz
$t_{jit(o)(CLOCK)RMS}$	RMS output jitter on pin CLOCK		-	-	500	ps
$\delta_{o(CLOCK)}$	output clock duty cycle on pin CLOCK		45	50	55	%

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Table 68.   Dynamic characteristics: digital I/O pins (SDR)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified. See Figure 30.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(STP)}$	STP set-up time with respect to the rising edge of pin CLOCK	input-only pin (STP)		6.0	-	-	ns
$t_{su(DATA)}$	DATA set-up time with respect to the rising edge of pin CLOCK	bidirectional pins (DATA[7:0]) as inputs		6.0	-	-	ns
$t_{h(STP)}$	STP hold time with respect to the rising edge of pin CLOCK	input-only pin (STP)		0.0	-	-	ns
$t_{h(DATA)}$	DATA hold time with respect to the rising edge of pin CLOCK	bidirectional pins (DATA[7:0]) as inputs		0.0	-	-	ns
$t_{d(DIR)}$	DIR output delay with respect to the rising edge of pin CLOCK	output-only pin DIR		-	-	9.0	ns
$t_{d(NXT)}$	NXT output delay with respect to the rising edge of pin CLOCK	output-only pin NXT		-	-	9.0	ns
$t_{d(DATA)}$	DATA output delay with respect to the rising edge of pin CLOCK	bidirectional pins as output (DATA[7:0])		-	-	9.0	ns
C_L	load capacitance	pins DATA[7:0], CLOCK, DIR, NXT, STP	[1] -		-	20	pF

[1]   Load capacitance on each ULPI pin.

Table 69.   Dynamic characteristics: digital I/O pins (DDR)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified. See Figure 30.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(STP)}$	STP set-up time with respect to the rising edge of pin CLOCK	input-only pin (STP)		6.0	-	-	ns
$t_{su(DATA)}$	DATA set-up time with respect to the rising edge of pin CLOCK	bidirectional pins (DATA[3:0]) as inputs	[1][2]	4.0	-	-	ns
$t_{h(STP)}$	STP hold time with respect to the rising edge of pin CLOCK	input-only pin (STP)		0.0	-	-	ns
$t_{h(DATA)}$	DATA hold time with respect to the rising edge of pin CLOCK	bidirectional pins (DATA[7:0]) as inputs	[2]	0.0	-	-	ns
$t_{d(DIR)}$	DIR output delay with respect to the rising edge of pin CLOCK	output-only pin DIR		-	-	9.0	ns
$t_{d(NXT)}$	NXT output delay with respect to the rising edge of pin CLOCK	output-only pin NXT		-	-	9.0	ns
$t_{d(DATA)}$	DATA output delay with respect to the rising edge of pin CLOCK	bidirectional pins (DATA[3:0]) as output	[2]	-	-	4.4	ns
C_L	load capacitance	pins DATA[3:0], CLOCK, DIR, NXT, STP	[3]				
		t_d = 4 ns		-	-	10	pF
		t_d = 4.4 ns		-	-	15	pF

[1]   Note that the value exceeds that specified in *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1.*

[2]   Also with respect to the falling edge of pin CLOCK.

[3]   Load capacitance on each ULPI pin.

Table 70.   Dynamic characteristics: analog I/O pins (DP, DM) in USB mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = –40 ℃ to +85 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed driver characteristics; see Figure 26						
t_{HSR}	rise time (10 % to 90 %)	drive 45 Ω to GND on DP and DM	500	-	-	ps
t_{HSF}	fall time (10 % to 90 %)	drive 45 Ω to GND on DP and DM	500	-	-	ps
Full-speed driver characteristics; see Figure 26						
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $|V_{OH} - V_{OL}|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 10 % to 90 % of $|V_{OH} - V_{OL}|$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_{FR} / t_{FF}; excluding the first transition from the idle state	90	-	111.1	%
Low-speed driver characteristics; see Figure 26						
t_{LR}	transition time: rise time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on DM enabled; 10 % to 90 % of $|V_{OH} - V_{OL}|$	75	-	300	ns
t_{LF}	transition time: fall time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on DM enabled; 10 % to 90 % of $|V_{OH} - V_{OL}|$	75	-	300	ns
t_{LRFM}	rise and fall time matching	t_{LR} / t_{LF}; excluding the first transition from the idle state	80	-	125	%

Table 71.   Dynamic characteristics: analog I/O pins (DP, DM) in transparent UART mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = –40 ℃ to +85 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Full-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	25	-	75	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	25	-	75	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	39	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	34	ns
Low-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	100	-	400	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	100	-	400	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
Full-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns
Low-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns

Table 72.　Dynamic characteristics: analog I/O pins (DP, DM) in serial mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 ℃ to +85 ℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver timing (valid only for serial mode)						
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	TX_DAT, TX_SE0 to DP, DM; see Figure 27	-	-	20	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	TX_DAT, TX_SE0 to DP, DM; see Figure 27	-	-	20	ns
t_{PHZ}	driver disable delay from HIGH level	TX_ENABLE to DP, DM; see Figure 28	-	-	12	ns
t_{PLZ}	driver disable delay from LOW level	TX_ENABLE to DP, DM; see Figure 28	-	-	12	ns
t_{PZH}	driver enable delay to HIGH level	TX_ENABLE to DP, DM; see Figure 28	-	-	20	ns
t_{PZL}	driver enable delay to LOW level	TX_ENABLE to DP, DM; see Figure 28	-	-	20	ns
Receiver timing (valid only for serial mode)						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 29	-	-	20	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 29	-	-	20	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 29	-	-	20	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 29	-	-	20	ns
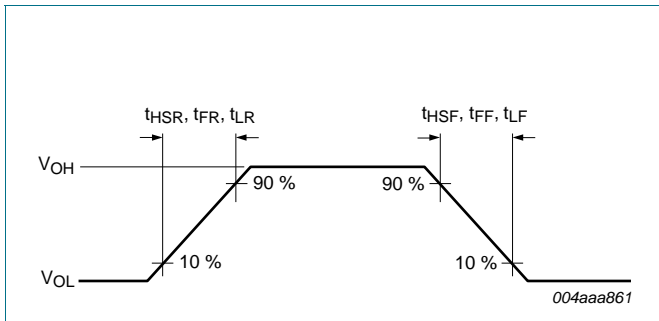
Fig 26.　Rise time and fall time
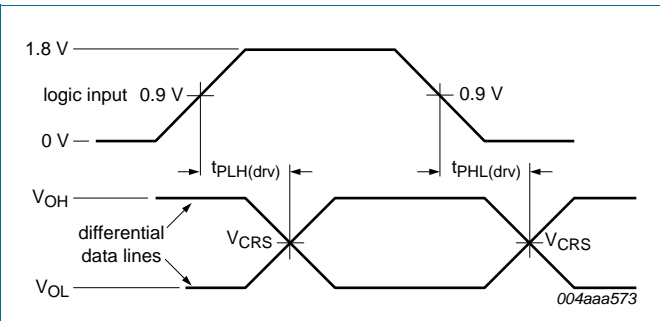
Fig 27.　Timing of TX_DAT and TX_SE0 to DP and DM
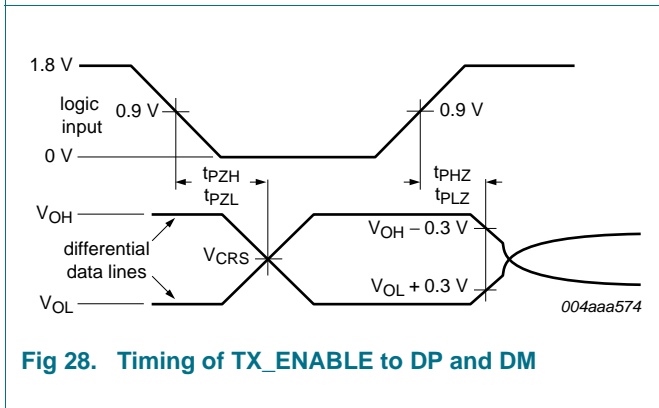
Fig 28.　Timing of TX_ENABLE to DP and DM
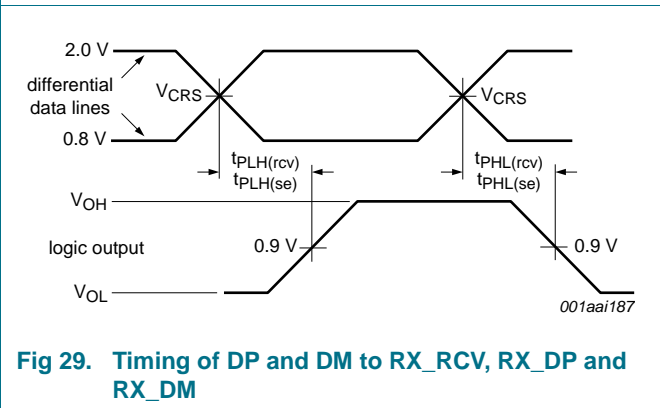
Fig 29.　Timing of DP and DM to RX_RCV, RX_DP and RX_DM
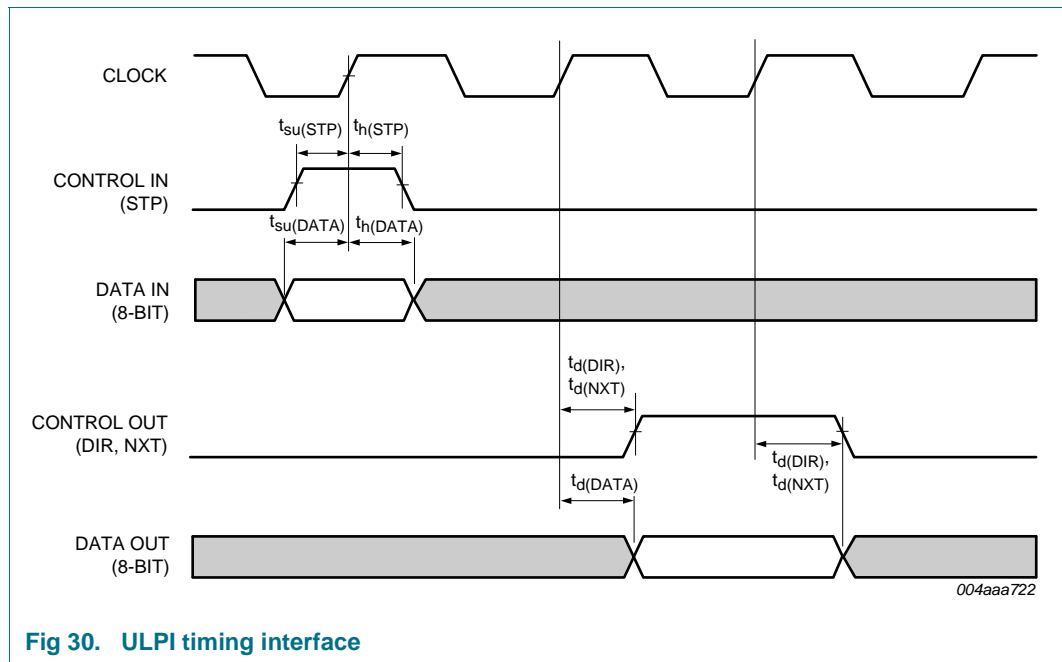
Fig 30. ULPI timing interface

16. Application information

Table 73.   Recommended bill of materials

Designator	Application	Part type	Remark
C_{bypass}	highly recommended for all applications	0.1 µF ± 20 %	-
C_{filter}	highly recommended for all applications	4.7 µF ± 20 %	use a LOW ESR capacitor (0.2 Ω to 2 Ω) for best performance
C_{VBUS}	mandatory for peripherals	1 µF to 10 µF	use low ESR capacitor
	mandatory for host	120 µF (min)	use low ESR capacitor
	mandatory for OTG	1 µF to 6.5 µF	use low ESR capacitor
C_{XTAL}	in all applications	18 pF ± 20 %	-
D_{ESD}	recommended to prevent damages from ESD	-	IP4359CX4/LF; Wafer-Level Chip-Scale Package (WLCSP); ESD IEC 61000-4-2 level 4; ±15 kV contact; ±15 kV air discharge compliant protection.
			Remark: ISP1705 and IP4359CX4/LF together have an IEC 61000-4-2 contact discharge tolerance of ±20 kV.
R_{RREF}	mandatory in all applications	12 kΩ ± 1 %	-
$R_{S(VBUS)}$	recommended for peripherals or external 5 V applications	1 kΩ ± 5 %	-
R_{pullup}	recommended; for applications with an external V_{BUS} supply controlled by PSW_N	10 kΩ	-
xtal	mandatory in all applications	19.2 MHz	C_L = 10 pF; R_S < 220 Ω; C_{XTAL} = 18 pF
		24 MHz	C_L = 10 pF; R_S < 160 Ω; C_{XTAL} = 18 pF
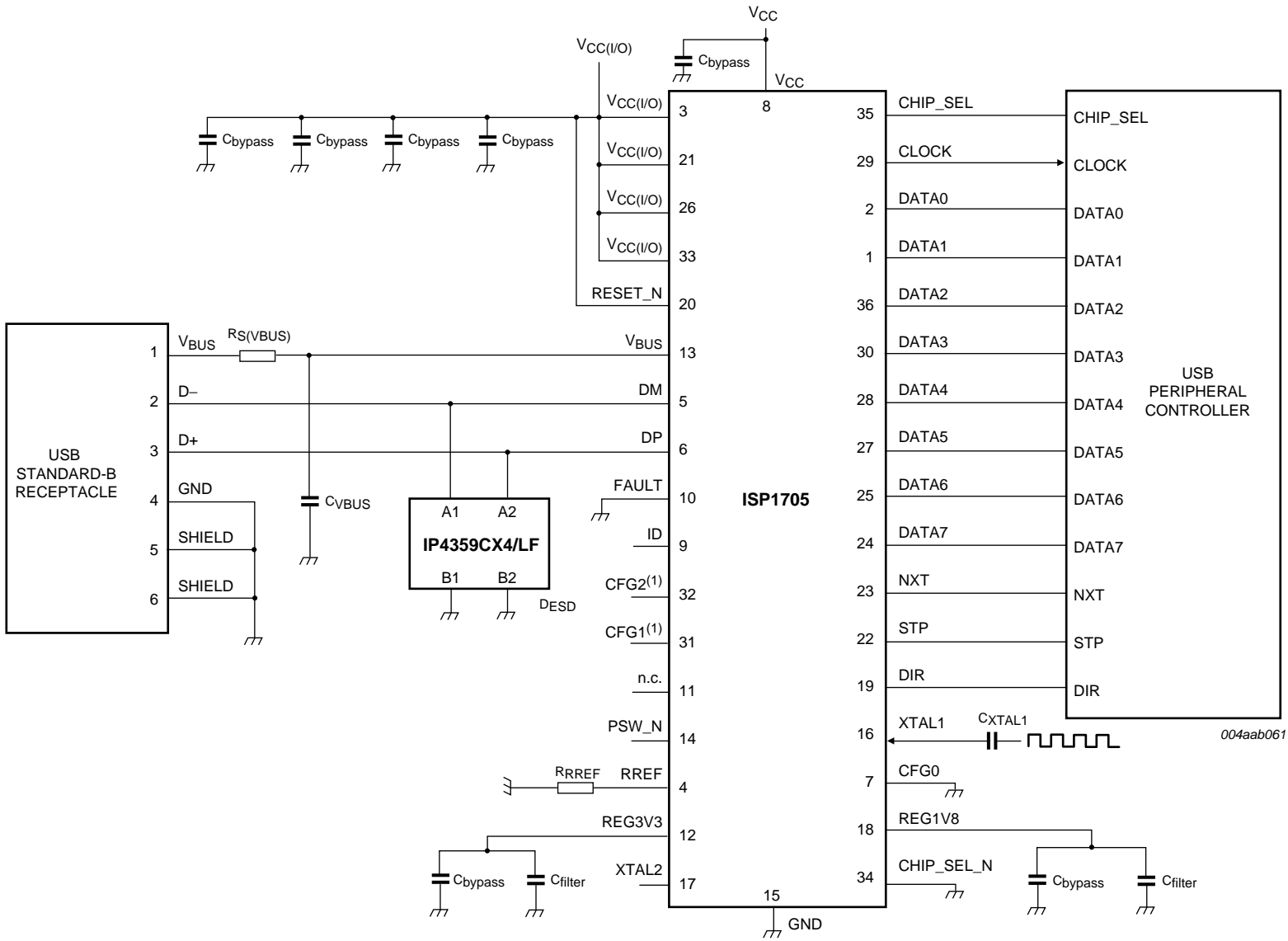
This figure shows the HVQFN pinout. For the TFBGA ballout, see Table 3.

(1) Connect to either GND or $V_{CC(I/O)}$, depending on the clock frequency used. See Table 6.

Fig 31. ISP1705 in peripheral-only application
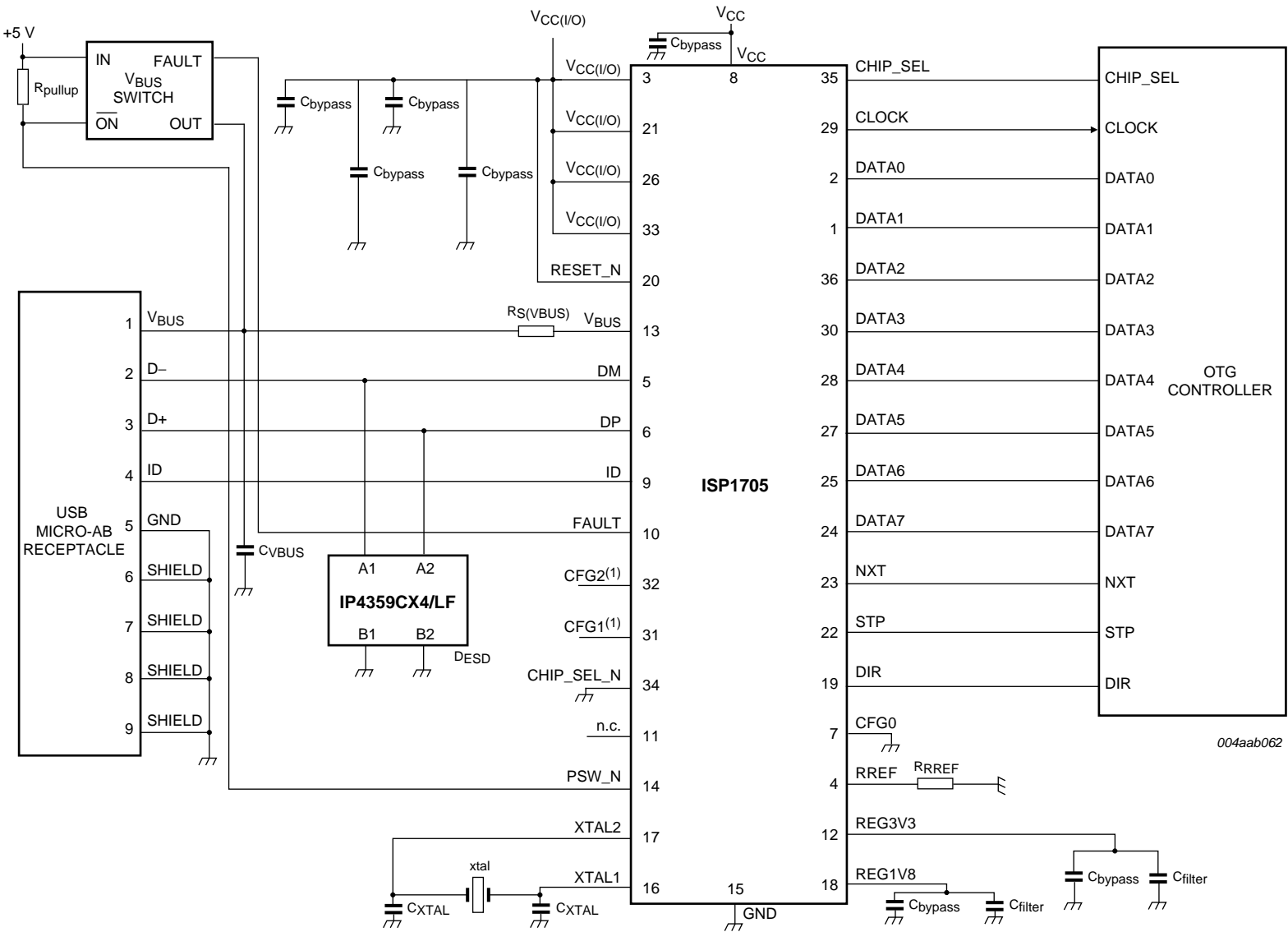
This figure shows the HVQFN pinout. For the TFBGA ballout, see Table 3.

(1) Connect to either GND or $V_{CC(I/O)}$, depending on the crystal frequency used. See Table 6.

Fig 32. ISP1705 in OTG application
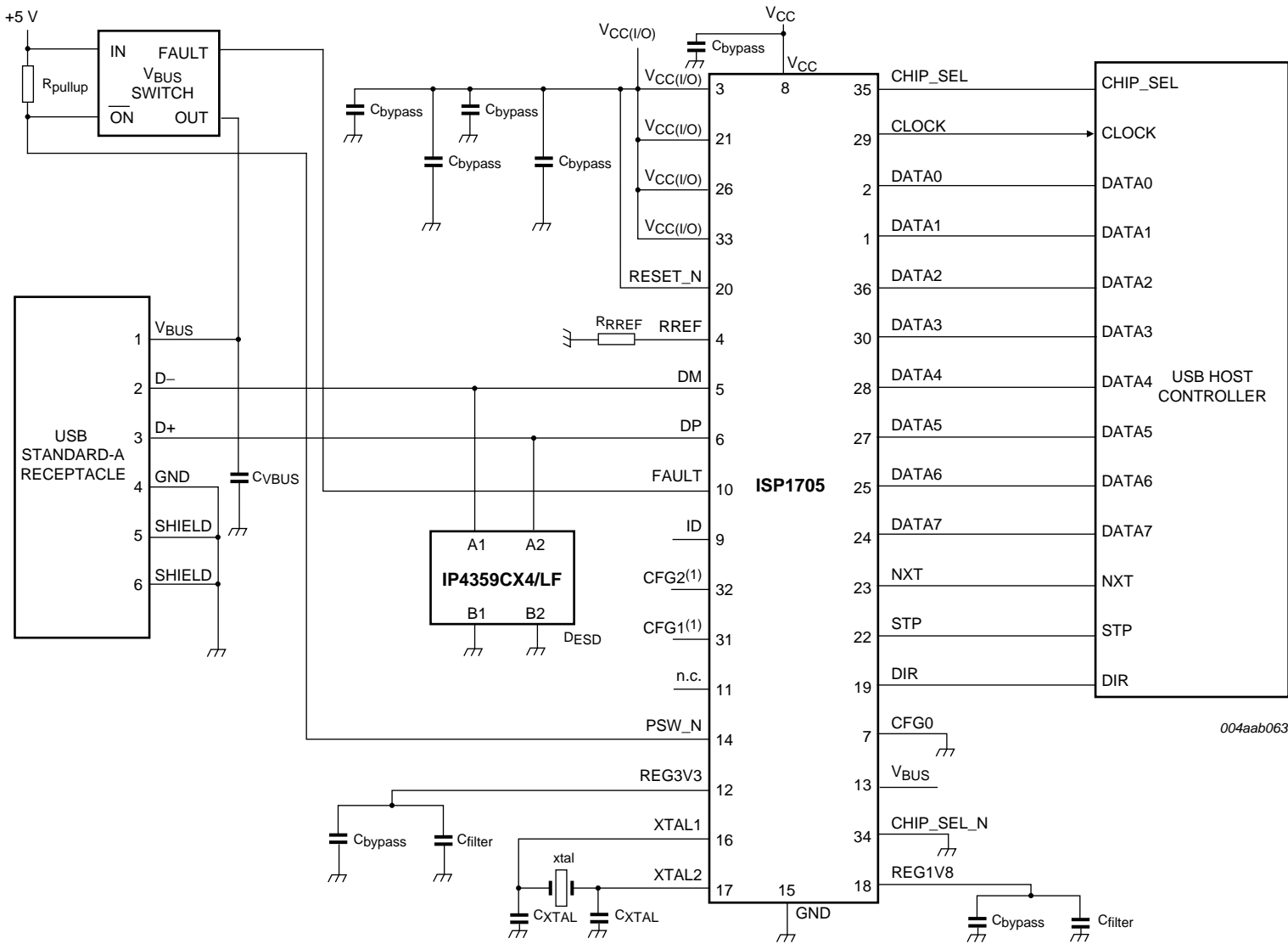
004aab063

This figure shows the HVQFN pinout. For the TFBGA ballout, see Table 3.

(1) Connect to either GND or $V_{CC(I/O)}$, depending on the crystal frequency used. See Table 6.

Fig 33. ISP1705 in host application

17. Package outline

HVQFN36: plastic thermal enhanced very thin quad flat package; no leads;
36 terminals; body 5 x 5 x 0.85 mm

SOT818-1

DIMENSIONS (mm are the original dimensions)

UNIT	A[1] max	A$_1$	b	c	D[1]	D$_h$	E[1]	E$_h$	e	e$_1$	e$_2$	L	v	w	y	y$_1$
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.75 3.45	5.1 4.9	3.75 3.45	0.4	3.2	3.2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT818-1	- - -	MO-220	- - -			03-06-13
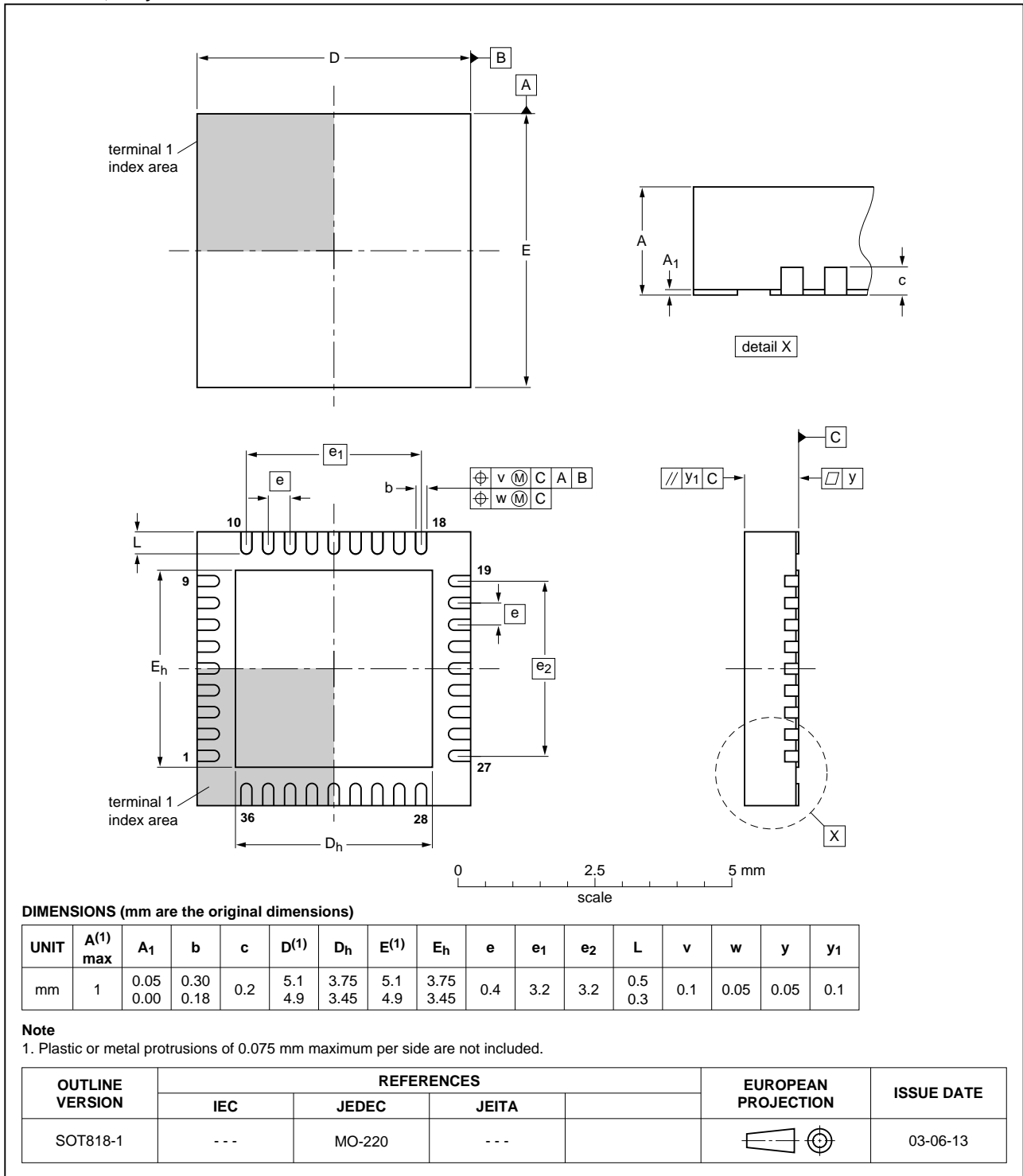
Fig 34. Package outline SOT818-1 (HVQFN36)

TFBGA36: plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 x 3.5 x 0.8 mm   **SOT912-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max	A₁	A₂	b	D	E	e	e₁	e₂	v	w	y	y₁
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	3.6 3.4	3.6 3.4	0.5	2.5	2.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	**JEDEC**	**JEITA**			
SOT912-1	- - -	- - -	- - -			~~05-08-09~~ 05-09-01
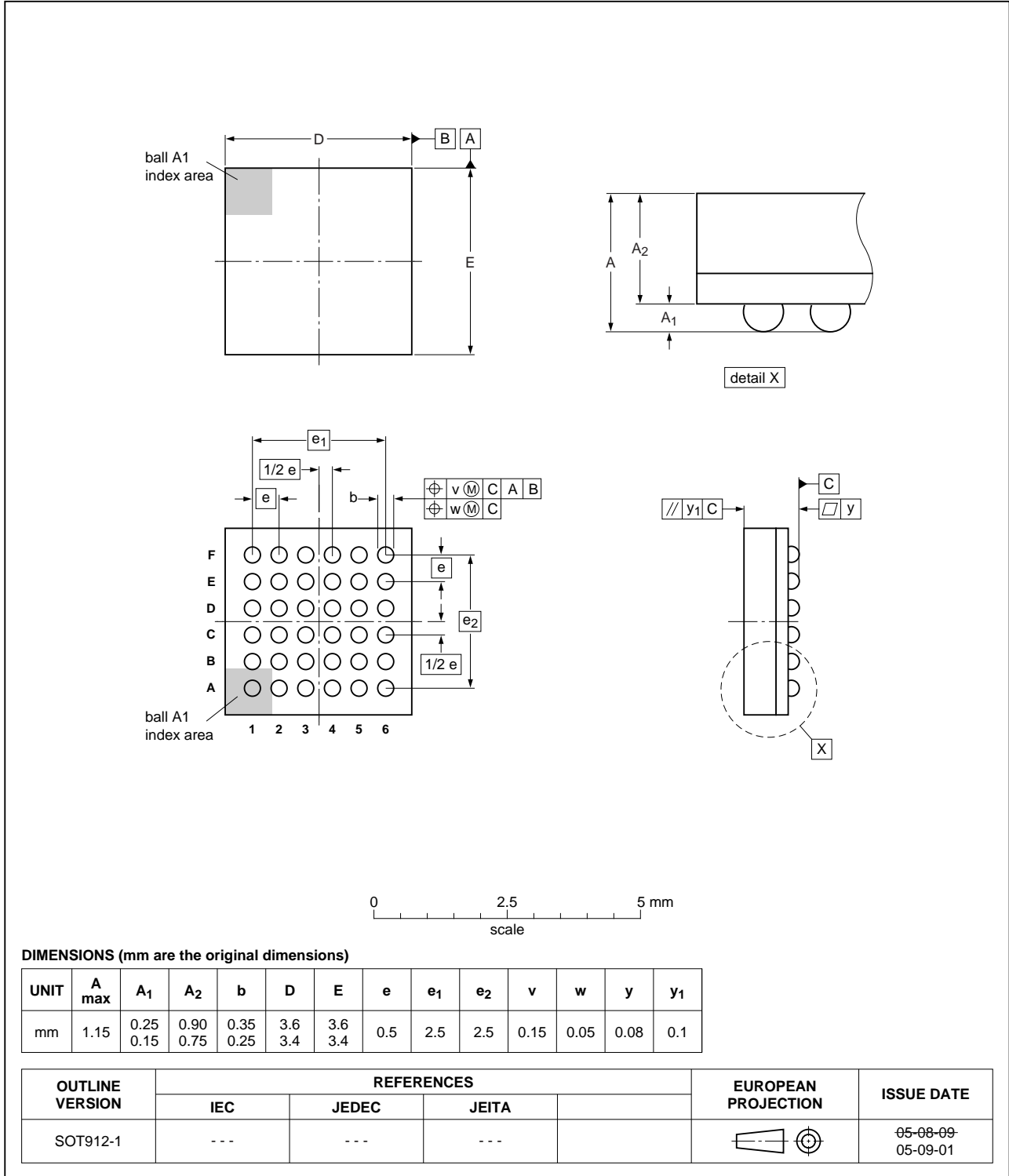
Fig 35.   Package outline SOT912-1 (TFBGA36)

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 36) than a SnPb process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 74 and 75

Table 74.   SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature ($°C$)	
	Volume (mm^3)	
	< 350	$\geq$ 350
< 2.5	235	220
$\geq$ 2.5	220	220

Table 75.   Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature ($°C$)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 36.

MSL: Moisture Sensitivity Level

Fig 36.   Temperature profiles for large and small components
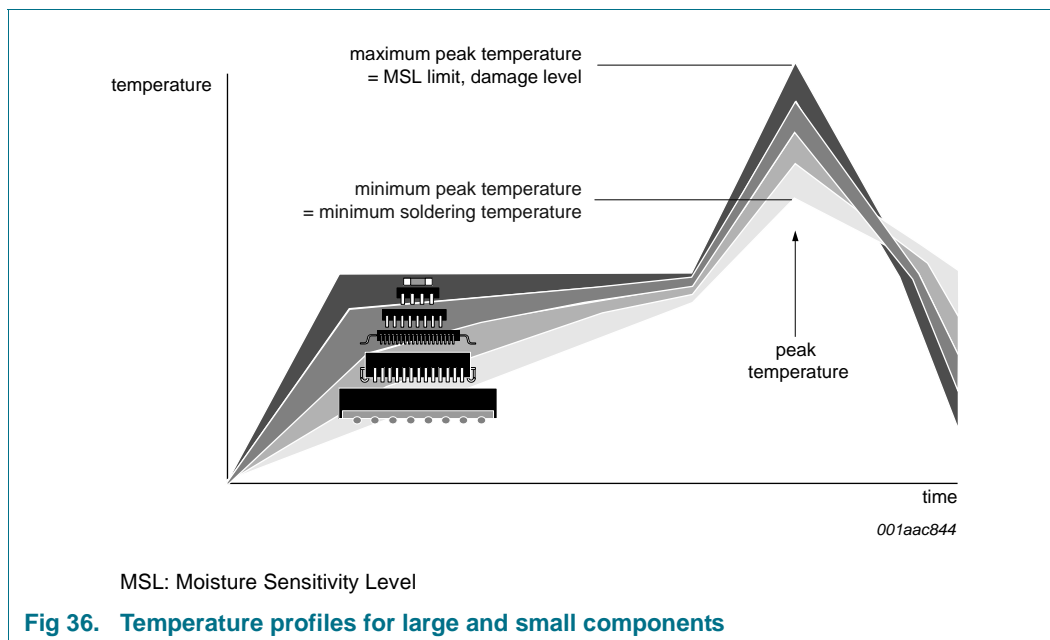
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 76.   Abbreviations

Acronym	Description
ASIC	Application Specific Integrated Circuit
ATX	Analog USB Transceiver
CD-DVD	Compact Disc - Digital Video Disc
CDM	Charged Device Model
CD-ROM	Compact Disc - Read-Only Memory
CD-RW	Compact Disc - ReWritable
DDR	Dual Data Rate
EMI	ElectroMagnetic Interference
EOP	End-Of-Packet
ESD	ElectroStatic Discharge
ESR	Effective Series Resistance
FPGA	Field Programmable Gate-Array
FS	Full Speed
HBM	Human Body Model
HNP	Host Negotiation Protocol
HS	High Speed
ID	Identification
IEC	International Electrotechnical Commission
LS	Low Speed

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Table 76. **Abbreviations** *…continued*

Acronym	Description
MM	Machine Model
NRZI	Non-Return to Zero Inverted
OTG	On-The-Go
PDA	Personal Digital Assistant
PHY	Physical
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
RoHS	Restriction of Hazardous Substances
RXCMD	Receive Command
RXD	Receive Data
SDR	Single Data Rate
SE0	Single-Ended Zero
SOC	System-On-Chip
SOF	Start-Of-Frame
SRP	Session Request Protocol
SYNC	Synchronous
TTL	Transistor-Transistor Logic
TXCMD	Transmit Command
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB-IF	USB Implementers Forum
UTMI	USB Transceiver Macrocell Interface
UTMI+	USB Transceiver Macrocell Interface Plus
WLCSP	Wafer-Level Chip-Scale Package

20. Glossary

A-device — An OTG device with an attached micro-A plug.

B-device — An OTG device with an attached micro-B plug.

Link — ASIC, SOC or FPGA that contains the USB host or peripheral core.

PHY — Physical layer containing the USB transceiver.

21. References

[1]   Universal Serial Bus Specification Rev. 2.0

[2]   On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3]   UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[4]   UTMI+ Specification Rev. 1.0

[5]   USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05

[6]   Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

[7]   Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) (JESD22-A115-A)

[8]   Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components (JESD22-C101-C)

[9]   Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test (IEC 61000-4-2)

22. Revision history

Table 77.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1705_2	20090121	Product data sheet	-	ISP1705_1
Modifications:	• Globally changed NXP Semiconductors and NXP to ST-NXP Wireless. Also updated the legal text.			
	• Table 9 "Pin states in Power-down mode": removed V_{BUS}.			
	• Section 8.11.2 "Interface behavior with respect to RESET_N during normal mode": updated the content.			
	• Table 53 "Static characteristics: supply pins": updated.			
	• Added Table 54 "Static characteristics: full-speed serial".			
	• Table 72 "Dynamic characteristics: analog I/O pins (DP, DM) in serial mode": updated values.			
ISP1705_1	20080613	Product data sheet	-	-

23. Tables

24. Figures

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25. Contents

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