FAIRCHILD SEMICONDUCTOR®

August 2004
Revised April 2005

USB1T1102
Universal Serial Bus Peripheral Transceiver with Voltage Regulator

General Description

This chip provides a USB Transceiver functionality with a voltage regulator that is compliant to USB Specification Rev 2.0. this integrated 5V to 3.3V regulator allows interfacing of USB Application specific devices with supply voltages ranging from 1.65V to 3.6V with the physical layer of Universal Serial Bus. It is capable of operating at 12Mbits/s (full speed) data rates and hence is fully compliant to USB Specification Rev 2.0. The Vbusmon pin allows for monitoring the Vbus line.

The USB1T1102 also provides exceptional ESD protection with 15kV contact HBM on D+, D– pins.

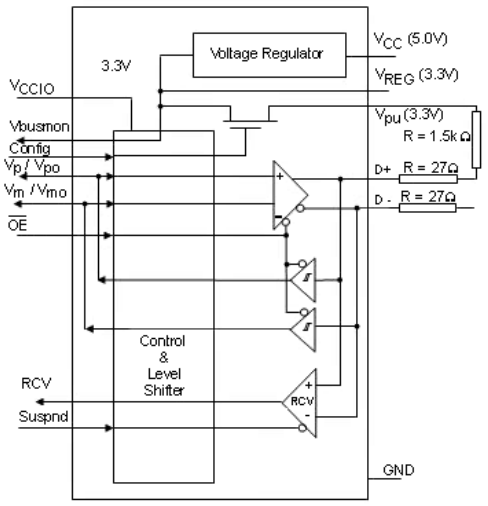
Features

- Complies with Universal Serial Bus Specification 2.0
- Integrated 5V to 3.3V voltage regulator for powering VBus
- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports full speed (12Mbits/s) data rates
- Ideal for portable electronic devices
- MLP technology package (16 pin) with HBCC footprint
- 15kV contact HBM ESD protection on bus pins

Ordering Code:

Order Number	Package Number	Package Description
USB1T1102MPX	MLP14D	Pb-Free 14-Terminal Molded Leadless Package (MLP), 2.5mm Square
USB1T1102MHX	MLP16HB	Pb-Free 16-Terminal Molded Leadless Package (MHBCC), JEDEC MO-217, 3mm Square
USB1T1102RMPX (Preliminary)	MLP14D	Pb-Free 14-Terminal Molded Leadless Package (MLP), 2.5mm Square
USB1T1102RMHX (Preliminary)	MLP16HB	Pb-Free 16-Terminal Molded Leadless Package (MHBCC), JEDEC MO-217, 3mm Square

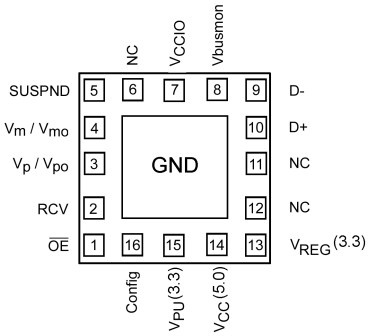
Logic Diagram



Note: On the USB1T1102R (Preliminary) the 1.5k resistor is integrated into the part, and connects V_{PU} and D+ eliminating the need for this external pull-up resistor.

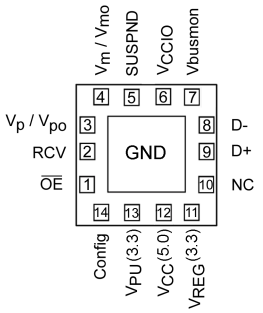
Connection Diagrams

MLP16 GND Exposed Diepad



(Bottom View)

MLP14 GND Exposed Diepad



(Bottom View)

Terminal Descriptions

Terminal Number		Terminal Name	I/O	Terminal Description
MLP14	MLP16			
1	1	$\overline{OE}$	I	Output Enable: Active LOW enables the transceiver to transmit data on the bus. When not active the transceiver is in the receive mode (CMOS level is relative to V_{CCIO})
2	2	RCV	O	Receive Data Output: Non-inverted CMOS level output for USB differential Input (CMOS output level is relative to V_{CCIO}). Driven LOW when SUSPN is HIGH; RCV output is stable and preserved during SE0 condition.
3	3	V_p/V_{po}	I/O	Single-ended D+ receiver output V_P (CMOS level relative to V_{CCIO}): Used for external detection of SE0, error conditions, speed of connected device; Pin also acts as drive data input V_{po} (see Table 1 and Table 2). Output drive is 4 mA buffer.
4	4	V_m/V_{mo}	I/O	Single-ended D– receiver output V_m (CMOS level relative to V_{CCIO}): Used for external detection of SE0, error conditions, speed of connected device; Pin also acts as drive data input V_{mo} (see Table 1 and Table 2). Output drive is 4 mA buffer.
5	5	SUSPND	I	Suspend: Enables a low power state (CMOS level is relative to V_{CCIO}). While the SUSPND pin is active (HIGH) it will drive the RCV pin to logic “0” state.
—	6	NC		No Connect
6	7	V_{CCIO}		Supply Voltage for digital I/O pins (1.65V to 3.6V): When not connected the D+ and D– pins are in 3-STATE. This supply bus is totally independent of V_{CC} (5V) and V_{REG} (3.3V).
7	8	Vbusmon	O	Vbus monitor output (CMOS level relative to V_{CCIO}): When Vbus > 4.1V then Vbusmon = HIGH and when Vbus < 3.6V then Vbusmon = LOW. If SUSPND = HIGH then Vbusmon is pulled HIGH.
9, 8	10, 9	D+, D–	AI/O	Data +, Data –: Differential data bus conforming to the USB standard.
10	11	NC		No Connect
—	12	NC		No Connect
11	13	V_{REG} (3.3V)		Internal Regulator Option: Regulated supply output voltage (3.0V to 3.6V) during 5V operation; decoupling capacitor of at least 0.1 μF is required. Regulator ByPass Option: Used as supply voltage input for 3.3V operation.
12	14	V_{CC} (5.0V)		Internal Regulator Option: Used as supply voltage input (4.0V to 5.5V); can be connected directly to USB line Vbus. Regulator ByPass Option: Connected to V_{REG} (3.3V)

Terminal Descriptions (Continued)

Terminal Number		Terminal Name	I/O	Terminal Description
MLP14	MLP16			
13	15	V_{PU} (3.3V)		Pull-up Supply Voltage (3.3V ± 10%): Connect an external 1.5kΩ resistor on D+ (FS data rate); Pin function is controlled by Config input pin: Config = LOW – V_{PU} (3.3V) is floating (High Impedance) for zero pull-up current. Config = HIGH – V_{PU} (3.3V) = 3.3V; internally connected to V_{REG} (3.3V).
14	16	Config	I	USB connect or disconnect software control input. Configures 3.3V to external 1.5kΩ resistor on D+ when HIGH.
Exposed Diepad	Exposed Diepad	GND	GND	GND supply down bonded to exposed diepad to be connected to the PCB GND.

Functional Description

The USB1T1102 transceiver is designed to convert CMOS data into USB differential bus signal levels and to convert USB differential bus signal to CMOS data.

To minimize EMI and noise the outputs are edge rate controlled with the rise and fall times controlled and defined for full speed data rates only (12Mbits/s). The rise, fall times are balanced between the differential pins to minimize skew.

The USB1T1102 differs from earlier USB Transceiver in that the V_p/V_m and V_{po}/V_{mo} pins are now I/O pins rather than discrete input and output pins. Table 1 describes the specific pin functionality selection. Table 2 and Table 3 describe the specific Truth Tables for Driver and Receiver operating functions.

The USB1T1102 also has the capability of various power supply configurations to support mixed voltage supply applications (see Table 4) and Section 2.1 for detailed descriptions.

Functional Tables

TABLE 1. Function Select

SUSPND	$\overline{OE}$	D+, D–	RCV	V_p/V_{po}	V_m/V_{mo}	Function
L	L	Driving & Receiving	Active	V_{po} Input	V_{mo} Input	Normal Driving (Differential Receiver Active)
L	H	Receiving (Note 1)	Active	V_p Output	V_m Output	Receiving
H	L	Driving	Inactive (Note 2)	V_{po} Input	V_{mo} Input	Driving during Suspend (Differential Receiver Inactive)
H	H	3-STATE (Note 1)	Inactive (Note 2)	V_p Output	V_m Output	Low Power State

Note 1: Signal levels is function of connection and/or pull-up/pull-down resistors.

Note 2: For SUSPND = HIGH mode the differential receiver is inactive and the output RCV is forced LOW. The out-of-suspend signaling (K) is detected via the single-ended receivers of the V_p/V_{po} and V_m/V_{mo} pins.

TABLE 2. Driver Function ($\overline{OE}$ = L) using Differential Input Interface

V_m/V_{mo}	V_p/V_{po}	Data
L	L	SE0 (Note 3)
L	H	Differential Logic 1
H	L	Differential Logic 0
H	H	Illegal State

Note 3: SE0 = Single Ended Zero

TABLE 3. Receiver Function ($\overline{OE}$ = H)

D+, D–	RCV	V_p/V_{po}	V_m/V_{mo}
Differential Logic 1	H	H	L
Differential Logic 0	L	L	H
SE0	X	L	L

X = Don't Care

Power Supply Configurations and Options

The USB1T1102 may be operated in two power supply modes.

1. Normal (Regulator) Mode: For 5V operation V_{CC} is connected to 5V source (4.0V to 5.5V) and the internal voltage regulator then produces 3.3V for the USB connections.
2. Bypass Mode: For 3.3V operation both V_{CC} and V_{REG} are connected to a 3.3V source (3.0V to 3.6V)

In both cases for normal mode the V_{CCIO} is an independent voltage source (1.65V to 3.6V) that is a function of the external circuit configuration.

A summary of the Supply Configurations is described in Table 4.

TABLE 4. Power Supply Configuration Options

Pins	Power Supply Mode Configuration	
	Normal (Regulated Output)	**Normal (Regulator Bypass)**
V_{CC} (5V)	Connected to 5V Source	Connected to V_{REG} (3.3V) [Max Drop of 0.3V] (2.7V to 3.6V0
V_{REG} (3.3V)	3.3V, 300µA Regulated Output	Connected to 3.3V Source
V_{CCIO}	1.65V to 3.6V Source	1.65V to 3.6v Source
V_{PU}	3.3V Available if Config = HIGH	3.3V Available if Config = HIGH
D+, D–	Function of Mode Set Up	Function of Mode Set Up
V_p/V_{po}, V_m/V_{mo}	Function of Mode Set Up	Function of Mode Set Up
RCV	Function of Mode Set Up	Function of Mode Set Up
Vbusmon	Function of Mode Set Up	Function of Mode Set Up
OE, SUSPND Config	Function of Mode Set Up	Function of Mode Set Up

ESD Protection

ESD Performance of the USB1T1102

HBM D+/D–: 15.0kV

HBM, all other pins (Mil-Std 883E): 6.5kV

ESD Protection: D+/D– Pins

Since the differential pins of a USB transceiver may be subjected to extreme ESD voltages, additional immunity has been included in the D+ and D– pins without compromising performance. The USB1T1102 differential pins have ESD protection to the following limits:

- 15kV using the contact Human Body Model
- 8kV using the Contact Discharge method as specified in IEC 61000-4-2

Human Body Model

Figure 1 shows the schematic representation of the Human Body Model ESD event. Figure 2 is the ideal waveform representation of the Human Body Model.

IEC 61000-4-2, IEC 60749-26 and IEC 60749-27

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment, and as such evaluates the equipment in its entirety for ESD immunity. Fairchild Semiconductor has evaluated this device using the IEC 6100-4-2 representative system model depicted in Figure 3. Under the additional standards set forth by the IEC, this device is also compliant with IEC 60749-26 (HBM) and IEC 60749-27 (MM).

Additional ESD Test Conditions

For additional information regarding our product test methodologies and performance levels, please contact Fairchild Semiconductor.

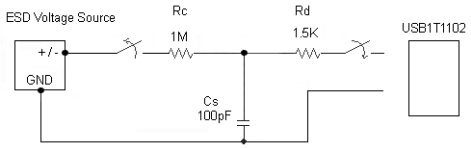


FIGURE 1. Human Body ESD Test Model

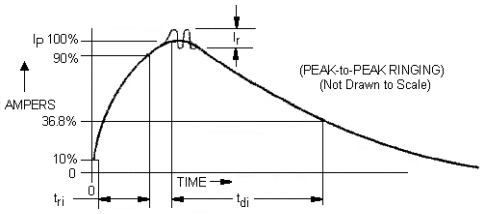


FIGURE 2. HBM Current Waveform

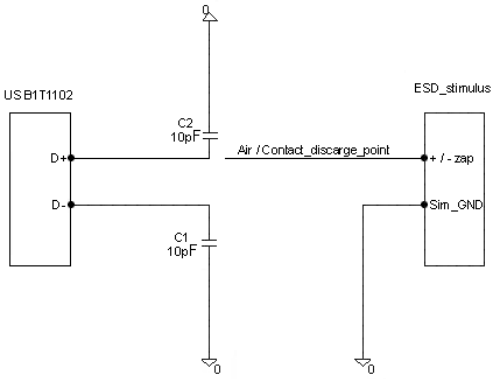


FIGURE 3. IEC 61000-4-2 ESD Test Model

Absolute Maximum Ratings (Note 4)

Supply Voltage (V_{CC})(5V)	−0.5V to +6.0V
I/O Supply Voltage (V_{CCIO})	−0.5V to +4.6V
Latch-up Current (I_{LU})	
V_I = −1.8V to +5.4V	150 mA
DC Input Current (I_{IK})	
V_I < 0	−50 mA
DC Input Voltage (V_I)	
(Note 5)	−0.5V to V_{CCIO} +5.5V
DC Output Diode Current (I_{OK})	
V_O > V_{CC} or V_O < 0	±50 mA
DC Output Voltage (V_O)	
(Note 5)	−0.5V to V_{CCIO} + 0.5V
Output Source or Sink Current (I_O)	
V_O = 0 to V_{CC}	
Current for D+, D− Pins	±50 mA
Current for RCV, V_m/V_p	±15 mA
DC V_{CC} or GND Current	
(I_{CC}, I_{GND})	±100 mA
ESD Immunity Voltage (V_{ESD});	
Contact HBM	
Pins D+, D−, V_{CC} (5.5V) and GND	15kV
All Other Pins	6.5kV
Storage Temperature (T_{STO})	−40°C to + 125°C
Power Dissipation (P_{TOT})	
I_{CC} (5V)	48 mW
I_{CCIO}	9 mW

Recommended Operating Conditions

DC Supply Voltage V_{CC} (5V)	4.0V to 5.5V
I/O DC Voltage V_{CCIO}	1.65V to 3.6V
DC Input Voltage Range (V_I)	0V to V_{CCIO} +5.5V
DC Input Range for AI/O ($V_{AI/O}$)	0V to V_{CC}
Pins D+ and D−	0V to 3.6V
Operating Ambient Temperature	
(T_{AMB})	−40°C to +85°C

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristic tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: IO Absolute Maximum Rating must be observed.

DC Electrical Characteristics (Supply Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} (5V) = 4.0V to 5.5V or V_{REG} (3.3V) = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V

Symbol	Parameter	Conditions	Limits −40°C to +85°C			Units
			Min	Typ	Max	
V_{REG} (3.3V)	Regulated Supply Output	Internal Regulator Option; I_{LOAD} ≤ 300 µA	3.0 (Note 6)(Note 7)	3.3	3.6	V
I_{CC}	Operating Supply Current (V_{CC}5.0)	Transmitting and Receiving at 12 Mbits/s; C_{LOAD} = 50 pF (D+, D−)		4.0 (Note 8)	8.0	mA
I_{CCIO}	I/O Operating Supply Current	Transmitting and Receiving at 12 Mbits/s		1.0 (Note 8)	2.0	mA
$I_{CC\ (IDLE)}$	Supply Current during FS IDLE and SE0 (V_{CC}5.0)	IDLE: V_{D+} ≥ 2.7V, V_{D-} ≤ 0.3V; SE0: V_{D+} ≤ 0.3V, V_{D-} ≤ 0.3V			300 (Note 9)	µA
$I_{CCIO\ (STATIC)}$	I/O Static Supply Current	IDLE, SUSPND or SE0			20.0	µA
$I_{CC(SUSPND)}$	Suspend Supply Current USB1T1102	SUSPND = HIGH $\overline{OE}$ = HIGH V_m = V_p = OPEN			25.0 (Note 9)	µA
	Suspend Supply Current USB1T1102R	SUSPND = HIGH $\overline{OE}$ = HIGH V_p = V_m = OPEN			40.0 (Note 10)	
V_{CCTH}	V_{CC} Threshold Detection Voltage	1.65V ≤ V_{CCIO} ≤ 3.6V				V
		Supply Lost			3.6	
		Supply Present	4.1			
V_{CCHYS}	V_{CC} Threshold Detection Hysteresis Voltage	V_{CCIO} = 1.8V		70.0		mV

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Limits			Units
			–40°C to +85°C			
			Min	Typ	Max	
V_{CCIOTH}	V_{CCIO} Threshold Detection Voltage	2.7V ≤ V_{REG} ≤ 3.6V				V
		Supply Lost			0.5	
		Supply Present	1.4			
$V_{CCIOHYS}$	V_{CCIO} Threshold Detection Hysteresis Voltage	V_{REG} = 3.3V		450		mV
V_{REGTH}	Regulated Supply Threshold Detection Voltage	1.65V ≤ V_{CCIO} ≤ V_{REG} 2.7V ≤ V_{REG} ≤ 3.6V				V
		Supply Lost		0.8		
		Supply Present	2.4 (Note 11)			
V_{REGHYS}	Regulated Supply Threshold Detection Hysteresis Voltage	V_{CCIO} = 1.8V		450		mV

Note 6: I_{LOAD} includes the pull-up resistor current via pin V_{PU}

Note 7: The minimum voltage in Suspend mode is 2.7V.

Note 8: Not tested in production, value based on characterization.

Note 9: Excludes any current from load and V_{PU} current to the 1.5kΩ resistor.

Note 10: Includes current between V_{pu} and the 1.5k internal pull-up resistor.

Note 11: When V_{CCIO} < 2.7V, minimum value for V_{REGTH} = 2.0V for supply present condition.

DC Electrical Characteristics (Digital Pins – excludes D+, D– Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CCIO} = 1.6V to 3.6V

Symbol	Parameter	Test Conditions	Limits		Units
			–40°C to +85°C		
			Min	Max	
Input Levels					
V_{IL}	LOW Level Input Voltage			0.3	V
V_{IH}	HIGH Level Input Voltage		0.6*V_{CCIO}		V
	OUTPUT LEVELS:				
V_{OL}	LOW Level Output Voltage	I_{OL} = 2 mA		0.4	V
		I_{OL} = 100 μA		0.15	
V_{OH}	HIGH Level Output Voltage	I_{OH} = 2 mA	V_{CCIO} - 0.4		V
		I_{OH} = 100 μA	V_{CCIO}- 0.15		
Leakage Current					
I_{LI}	Input Leakage Current	V_{CCIO} = 1.65V to 3.6V		±1.0 (Note 12)	μA
Capacitance					
C_{IN}, $C_{I/O}$	Input Capacitance	Pin to GND		10.0	pF

Note 12: If $V_{CCIO} \geq V_{REG}$ then leakage current will be higher than specified.

DC Electrical Characteristics (Analog I/O Pins – D+, D– Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 4.0V to 5.5V or V_{REG} = 3.0V to 3.6V

Symbol	Parameter	Test Condition	Limits			Units
			–40°C to +85°C			
			Min	Typ	Max	
Input Levels – Differential Receiver						
V_{DI}	Differential Input Sensitivity	$\lvert V_{I(D+)} - V_{I(D-)} \rvert$	0.2			V
V_{CM}	Differential Common Mode Voltage		0.8		2.5	V
INPUT LEVELS – Single-ended Receiver						
V_{IL}	LOW Level Input Voltage				0.8	V
V_{IH}	HIGH Level Input Voltage		2.0			V
V_{HYS}	Hysteresis Voltage		0.30		0.7	V
Output Levels						
V_{OL}	LOW Level Output Voltage	R_L = 1.5kΩ to 3.6V			0.3	V
V_{OH}	HIGH Level Output Voltage	R_L = 15kΩ to GND	2.8 (Note 13)		3.6	V
Leakage Current						
I_{OFF}	Input Leakage Current Off State				±1.0	µA
	CAPACITANCE					
$C_{I/O}$	I/O Capacitance	Pin to GND			20.0	pF
Resistance						
Z_{DRV}	Driver Output Impedance			41.0 (Note 14)		Ω
Z_{IN}	Driver Input Impedance		10.0			MΩ
R_{SW}	Switch Resistance				10.0	Ω
V_{TERM}	Termination Voltage	R_{PU} Upstream Port	3.0 (Note 15) (Note 16)		3.6	V

Note 13: If V_{OH} min. = V_{REG} - 0.2V.

Note 14: Includes external resistors of 29Ω on both D+ and D– pins.

Note 15: This voltage is available at pin V_{PU} and V_{REG}.

Note 16: Minimum voltage is 2.7V in the suspend mode.

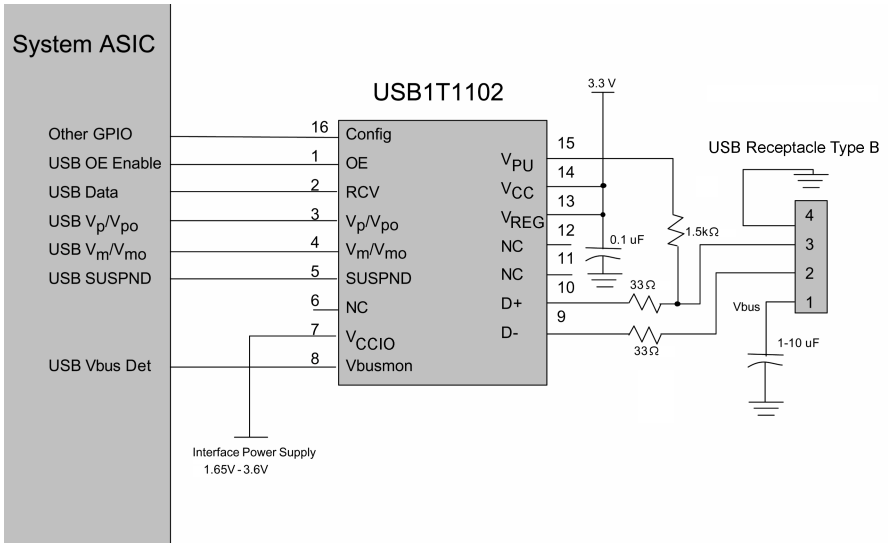
AC Electrical Characteristics (A I/O Pins Full Speed)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 4.0V to 5.5V or V_{REG} = 3.0V to 3.6V, V_{CCIO} = 1.65V to 3.6V, C_L = 50 pF; R_L = 1.5K on D+ to V_{PU}

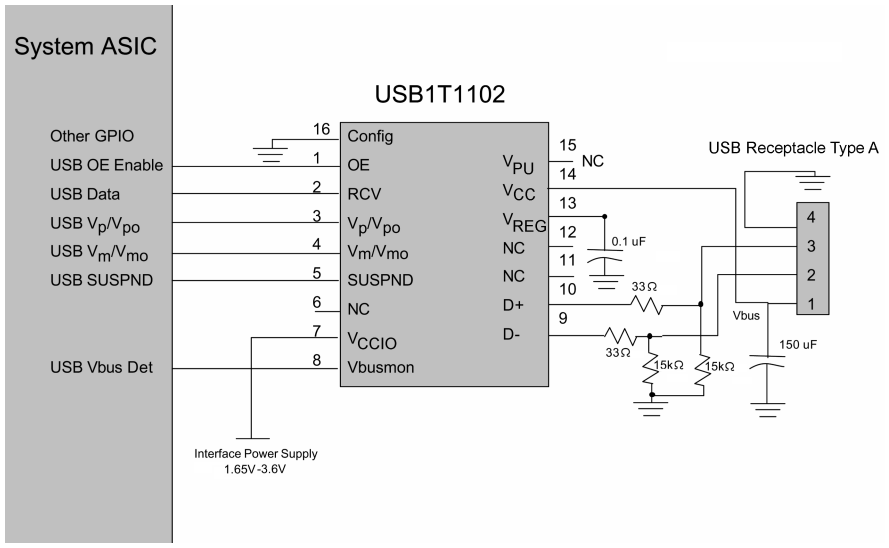
Symbol	Parameter	Test Conditions	Limits			Unit
			−40°C to +85°C			
			Min	Typ	Max	
Driver Characteristics						
t_R	Output Rise Time	C_L = 50 – 125 pF	4.0		20.0	ns
		10% to 90%				
t_F	Output Fall Time	Figures 4, 8	4.0		20.0	
t_{RFM}	Rise/Fall Time Match	t_F/ t_R Excludes First Transition from Idle State	90.0		111.1	%
V_{CRS} (Note 17)	Output Signal Crossover Voltage	Excludes First Transition from Idle State see Waveform	1.3		2.0	V
Driver Timing						
t_{PLH} t_{PHL}	Propagation Delay (V_p/V_{po}, V_m/V_{mo} to D+/D–)	Figures 5, 8			18.0	ns
t_{PHZ} t_{PLZ}	Driver Disable Delay ($\overline{OE}$ to D+/D–)	Figures 7, 9			15.0	ns
t_{PZH} t_{PZL}	Driver Enable Delay ($\overline{OE}$ to D+/D–)	Figures 7, 9			15.0	ns
Receiver Timing						
t_{PLH} t_{PHL}	Propagation Delay (Diff) (D+/D– to Rev)	Figures 6, 10			15.0	ns
t_{PLH} t_{PHL}	Single Ended Receiver Propagation Delay (D+/D– to V_p/ V_{po}, V_m/V_{mo})	Figures 6, 10			18.0	ns

Note 17: Not production tested, guaranteed by characterization.

Typical Application Configurations



Upstream Connection in Bypass Mode with Differential Outputs



Downstream Connection in Normal Mode with Differential Outputs

AC Waveforms

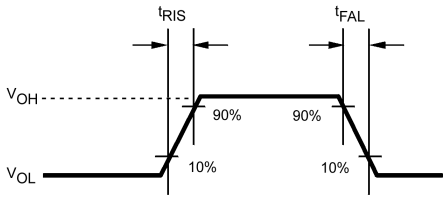


FIGURE 4. Rise and Fall Times

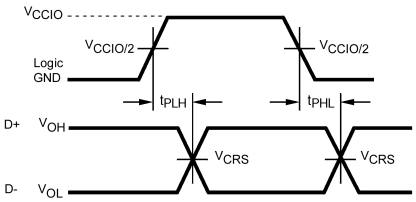


FIGURE 5. V_{po}, V_{mo} to D+/D–

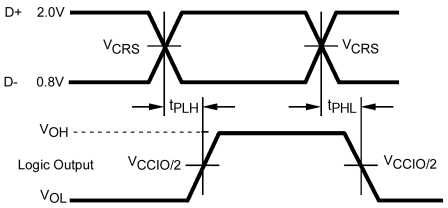


FIGURE 6. D+/D– to R_{CV}, V_{po}/V_p and V_{mo}/V_m

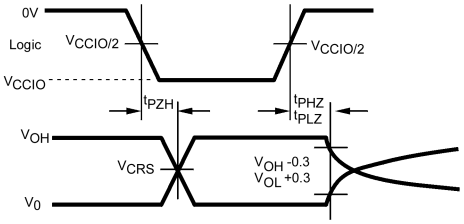
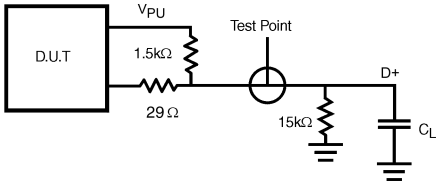


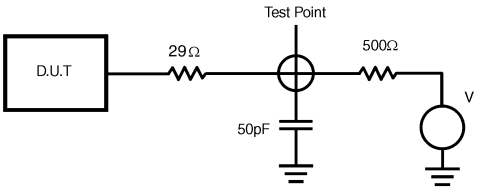
FIGURE 7. $\overline{OE}$ to D+/D–

Test Circuits and Waveforms



C_L = 50 pF Full Speed Propagation Delays
C_L = –125 pF Edge Rates only

FIGURE 8. Load for D+/D–



V = 0 for t_{PZH}, t_{PHZ}
V = V_{REG} for t_{PZL}

FIGURE 9. Load for Enable and Disable Times

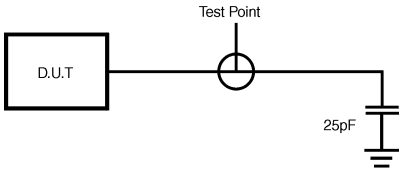


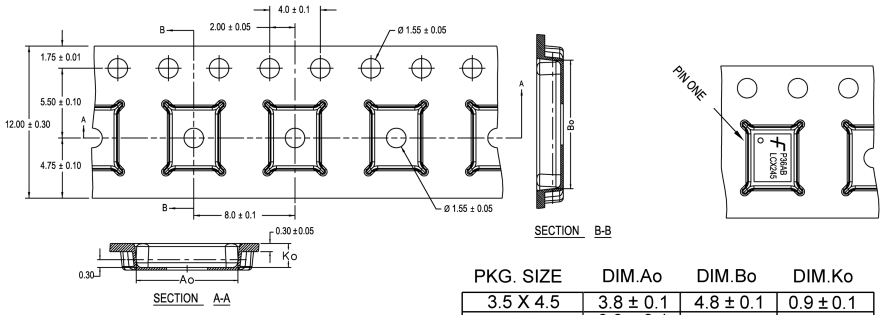
FIGURE 10. Load for V_m/V_{mo}, V_{p}/V_{po} and RCV

Tape and Reel Specification

Tape Format for MLP

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
MPX/MHX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



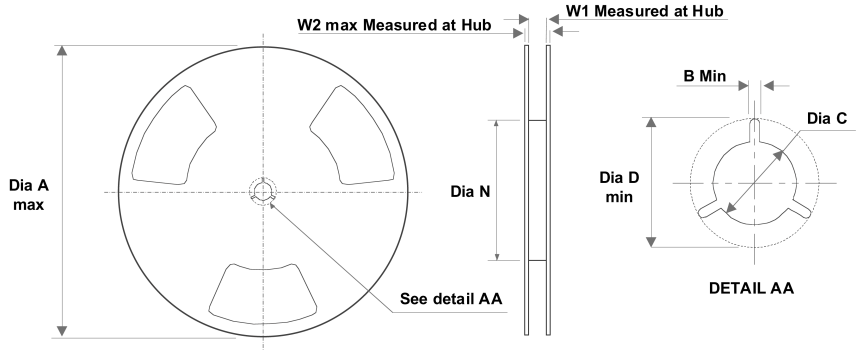
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

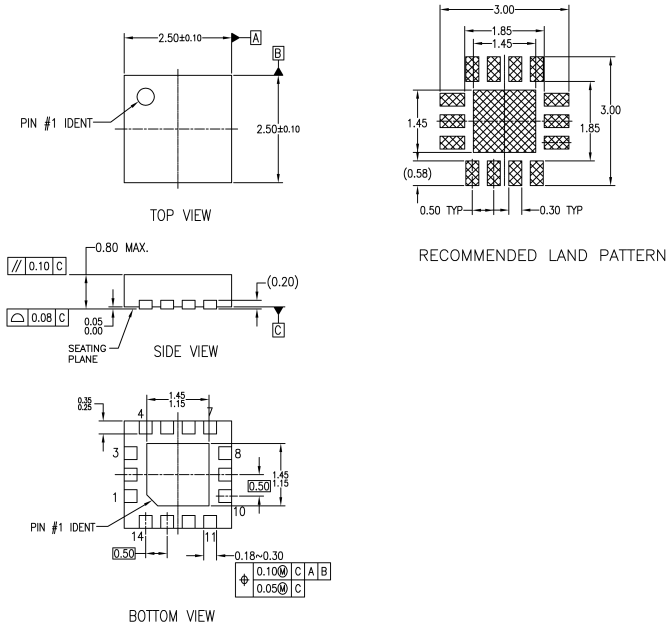
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0	0.059	0.512	0.795	7.008	0.488	0.724
	330	(1.50)	(13.00)	(20.20)	(178)	(12.4)	(18.4)

Physical Dimensions inches (millimeters) unless otherwise noted



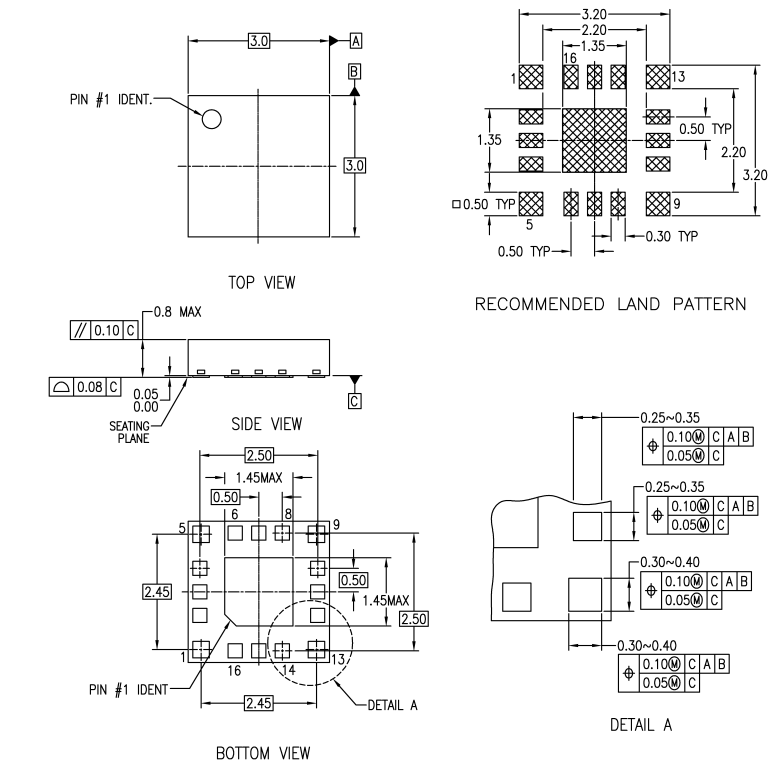
NOTES:

A. NO JEDEC REGISTRATION
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14DrevA

Pb-Free 14-Terminal Molded Leadless Package (MLP), 2.5mm Square
MLP14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. SIMILAR TO JEDEC REGISTRATION MO−217, DATED 11/2001
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP16HBrevA

Pb-Free 16-Terminal Molded Leadless Package (MHBCC), JEDEC MO-217, 3mm Square
Package Number MLP16HB

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