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2.5 Gbit/s Clock and Data Recovery Circuit GD16543

Preliminary

General Description

The GD16543 is a high performance monolithic integrated *Clock and Data Recovery* (CDR) device applicable for optical communication systems including:

- ◆ SDH STM-16
- ◆ SONET OC-48

The CDR contains all circuits needed for reliable acquisition and lock of the VCO phase to the incoming data-stream.

The electrical input sensitivity is better than 20 mV. Optical receivers with sensitivity better than -34 dBm have been obtained without optical pre-amplifiers.

The device meets all ITU-T jitter requirements when used with the recommended loop filter (jitter tolerance, -transfer and -generation).

The integrated 1:4 demultiplexer with differential ECL outputs ensures a simple and universal interface to the system CMOS ASICs.

The 622 MHz output clock is maintained within 500 ppm tolerance even in absence of data.

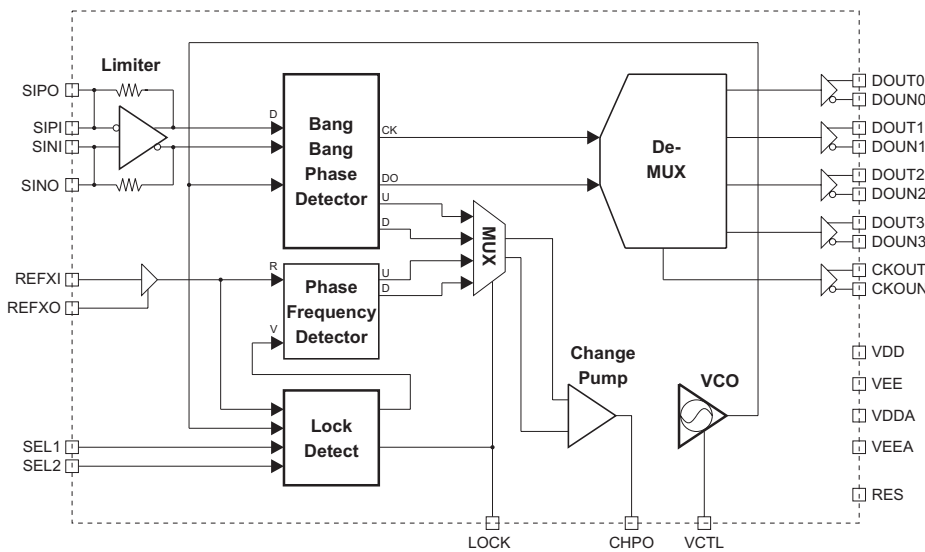
The GD16543 is available in a 40 lead ceramic LCC and in a 48 lead 7x7 mm TQFP power enhanced plastic package.

Features

- Clock and Data Recovery covering 2.3 Gbit/s to 2.7 Gbit/s.
- SDH STM-16, SONET OC-48 compatible.
- Differential Data inputs with 20 mV sensitivity.
- Differential ECL Data and Clock outputs.
- Acquisition time: < 500 μ s
- Few external passive components needed.
- 50 Ω Loop-Through data inputs for higher sensitivity.
- Single supply operation.
- Power dissipation: 1 W.
- Available in:
 - a 48 lead 7x7 mm TQFP plastic package
 - a 40 lead ceramic LCC.

Applications

- Clock and Data Recovery for optical communication systems including:
 - SDH STM-16
 - SONET OC-48



Functional Details

The main application of the GD16543 is as a receiver for:

- ◆ SDH STM-16
- ◆ SONET OC-48 optical communication systems.

It integrates:

- ◆ a Voltage Controlled Oscillator (VCO)
 - ◆ a Lock Detect Circuit
 - ◆ a Frequency Detector (PFD)
 - ◆ a Bang-Bang Phase Detector
- into a *Phase Locked Loop* (PLL) - based clock and data recovery circuit followed by a 1:4 demultiplexer with differential ECL data and clock outputs.

VCO

The VCO is a low noise LC-type differential oscillator with a tuning range from 2.2 to 2.7 GHz. Tuning is done by applying a voltage to the VCTL pin.

Lock Detect Circuit

The lock detect circuit continuously monitors the difference between the reference clock and the divided VCO clock. If the reference clock and the divided VCO frequency differs by more than 500 ppm (or 2000 ppm, selectable), it switches the PFD into the PLL in order to pull the VCO back inside the lock-in range. This mode is called **the acquisition mode**.

The PFD is used to ensure predictable lock up conditions for the GD16543 by locking the VCO to an external reference clock source. It is only used during acquisition and pulls the VCO into the lock range where the Bang-Bang phase detector is capable of acquiring lock. The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic.

Once the VCO is inside the lock-range the lock-detection circuit switches the Bang-Bang phase detector into the PLL in order to lock to the data signal. This mode is called **CDR mode**.

For the purpose of stand alone applications the GD16543 has been equipped with a crystal oscillator for a series resonance, fundamental mode crystal. A crystal for use at 2.488 GHz is also available. When not used with a crystal, the REF_{XI} input can be used as a standard ECL input.

The reference clock input, REF_{XI}, to the PFD is at 1/64 of the data rate.

Bang-Bang Phase Detector

The Bang-Bang phase detector is used in **CDR mode** as a true digital type detector, producing a binary output. It samples the incoming data twice each bit period: once in the transition of the (previous) bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits will show whether the VCO clock leads or lags the data. Hence the PLL is controlled by the bit transition point, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode. The external loop filter components control the characteristics of the PLL.

The binary output of either the PFD or the Bang-Bang phase detector (depending of the mode of the lock-detection circuit) is fed to a charge pump capable of sinking or sourcing current or tristating. The output of the charge pump is filtered through the loop filter and controls the tune-voltage of the VCO.

As a result of the continuous monitoring lock-detect circuit the VCO frequency never deviates more than 500 ppm (2000 ppm) from the reference clock before the PLL is considered to be 'Out of Lock'. Hence the acquisition time is predictable and short and the output clock CKOUT is always kept within the 500 ppm (2000 ppm) limits, ensuring safe clocking of down stream circuitry.

The LOCK Signal

The status of the lock-detection circuit is given by the LOCK signal. In CDR mode LOCK is steady high. In acquisition mode LOCK is alternating indicating the continuous shifts between the Bang-Bang Detector (high) and the PFD (low).

The LOCK output may be used to generate *Loss Of Signal* (LOS). The time for LOCK to assert is predictable and short, equal to the time to go into lock, but the time for LOCK to de-assert must be considered. When the line is down (i.e. no information received) the optical receiver circuit may produce random noise. It is possible that this random noise will keep the GD16543 within the 500 ppm (2000 ppm) range of the line frequency, hence LOCK will remain asserted for a non-deterministic time. This may be prevented by injecting a small current at the loop filter node, which actively pulls the PLL out of the lock range when the output of the phase detector acts randomly.

The negligible penalty paid is a static phase error on the sampling time in the decision gate. However, due to the nature of the phase detector the error will be small (few degrees), forcing the loop to be at one edge of the error-function shaped transfer characteristic of the detector.

Inputs

The input amplifier (pin SIPI / SINI) is designed as a limiting amplifier with a sensitivity better than 20 mV (differential).

The inputs may be either AC or DC coupled. In both cases input termination is made through pins SIPO / SINO. If the inputs are AC coupled the amplifier features an internal offset cancelling DC feedback. Notice that the offset cancellation will only work when the input is differential and AC-coupled as shown in the Figures at page 3.

Following the CDR block the data is 1:4 demultiplexed and output together with a 622 MHz clock. The data and clock outputs are differential ECL outputs that should be terminated via 50 Ω to -2 V.

Package

The GD16543 is provided in either a 48 lead power enhanced TQFP or in a 40 pin Multi Layer Ceramic package with internal 50 Ω transmission lines.

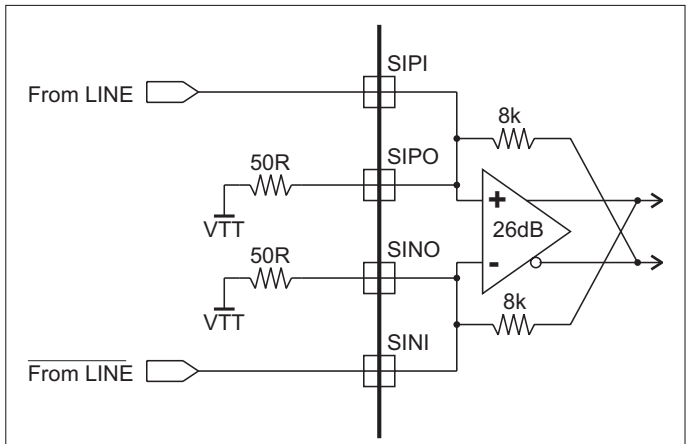


Figure 1. DC Coupled Input (Ignoring internal offset compensation)

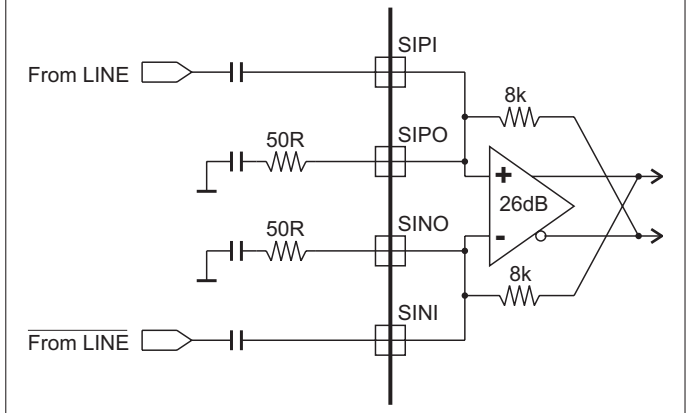


Figure 2. AC Coupled Input (Using internal offset compensation)

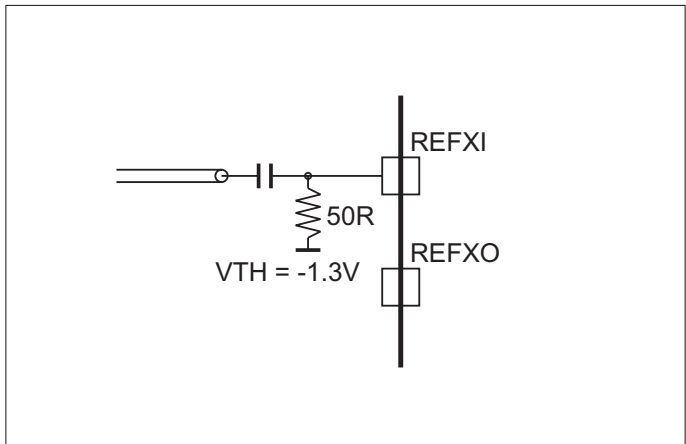


Figure 4. External Reference Clock

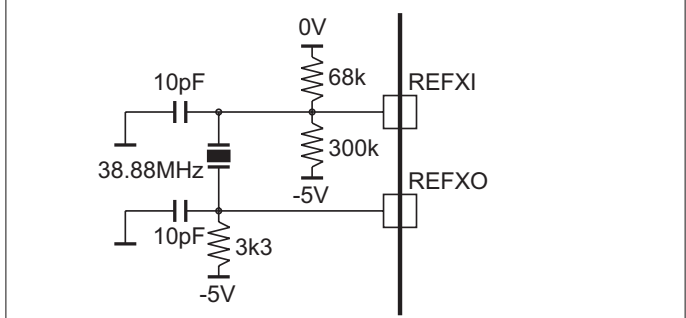


Figure 5. Crystal Oscillator

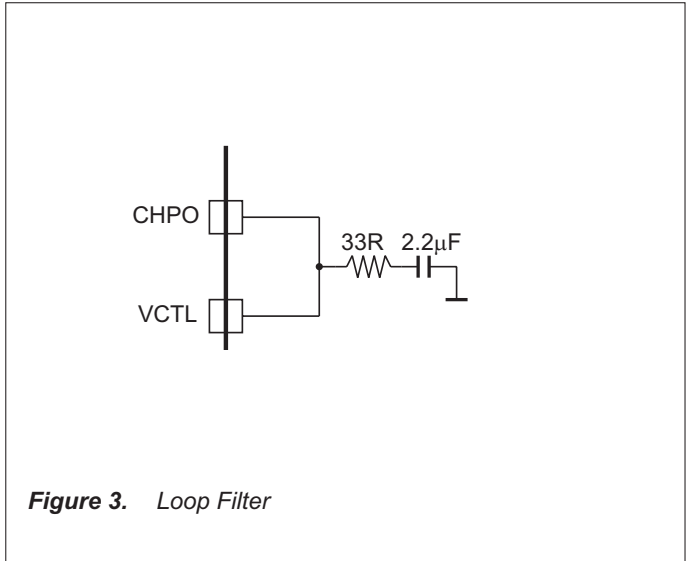


Figure 3. Loop Filter

Pin List

Mnemonic:	Pin No.:		Pin Type:	Description:
	40 LCC	48 TQFP		
SIPI, SIPO	22, 21	6, 7	Anl. IN	Loop-through terminated serial positive differential input. May be used as ECL compatible input.
SINI, SINO	24, 25	5, 4	Anl. IN	Loop-through terminated serial negative differential input. May be used as ECL compatible input.
DOUT0, DOUN0 DOUT1, DOUN1 DOUT2, DOUN2 DOUT3, DOUN3	11, 10 9, 8 19,18 17,16	19, 20 21, 22 10, 11 12, 13	ECL OUT	Re-timed differential data outputs. DOUT0 is the first bit received.
CKOUT, CKOUN	14, 13	16, 17	ECL OUT	Regenerated differential output clock, 622 MHz.
REFXI	35	38	ECL IN	38.88 MHz Reference clock input or X-tal input for Phase/ Freq. detect and Lock-detect.
REFXO	36	37	ECL OUT	38.88 MHz Reference clock output.
SEL1, SEL2	38, 39	34, 33	ECL IN	Single ended inputs, PLL set-up of Internal/ External switch mode and LOCK: SEL1 SEL2 0 0 Auto lock, 500 ppm. 0 1 Auto Lock, 2000 ppm. 1 0 Manual, Phase/Freq. Detector, 500 ppm. 1 1 Manual, Phase Detector, 2000 ppm.
LOCK	4	26	ECL OUT	Single ended CDR Lock alarm output. When low, the divided VCO freq. deviates more than 500/2000 ppm from REFXI.
RES	2	29	ECL IN	Global reset when high. For test purposes only. Connect to VEE for normal operation.
VCTL	29	45	Anl. IN	VCO control voltage input.
CHPO	33	41	Anl. OUT	Charge pump current output.
VDD	1, 3, 6, 12, 23	3, 9, 15, 18, 24, 25, 27, 31, 32, 36, 40, 48	PWR	0 V power for core and ECL I/O.
VEE	5, 7, 15, 20, 26, 27, 30, 34, 37, 40	1, 2, 8, 14, 23, 28, 30, 35, 39, 42, 47	PWR	-5 V power for core and ECL I/O.
VDDA	28	43, 46	PWR	0 V power for VCO.
VEEA		44	PWR	-5 V power for VCO.
NC	31, 32		NC	Not Connected
Heat sink				Connected to VDD

Pin Outline

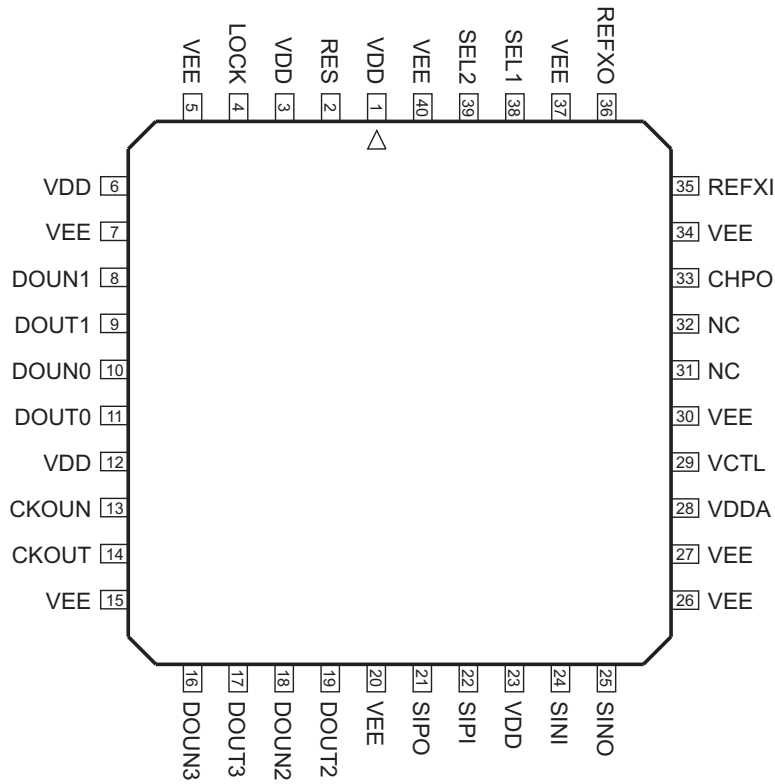


Figure 6. 40 Lead LCC, Top View

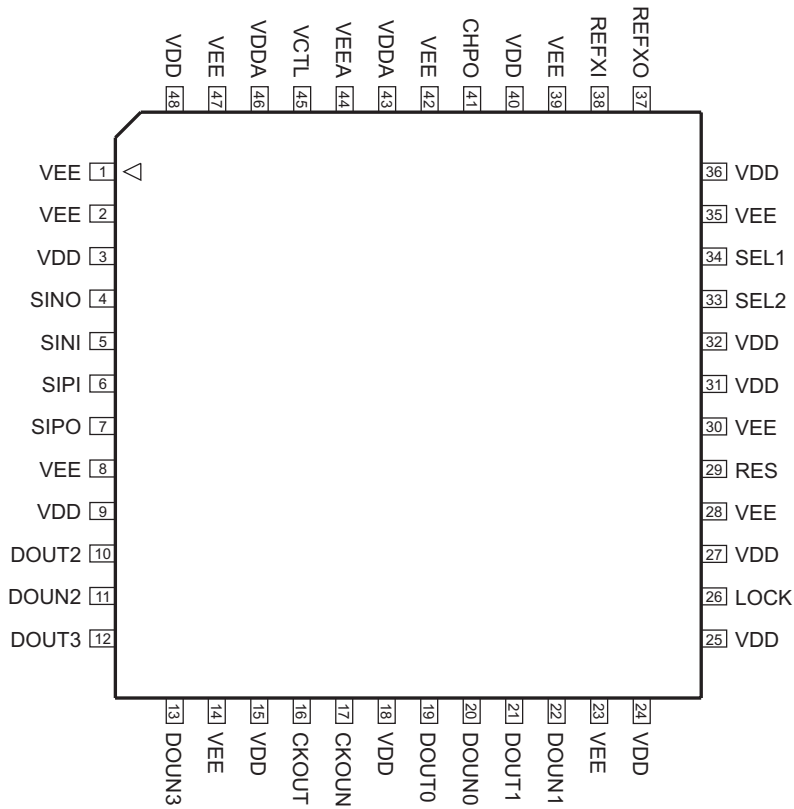


Figure 7. 48 Lead TQFP, Top View

Maximum Ratings

These are the limits beyond which the component may be damaged.

All voltages in the table are referred to VDD.

All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{EE}, V_{EEA}	Supply voltage		-6		0	V
V_o MAX	Output voltage		$V_{EE} - 0.5$		0.5	V
I_o MAX, ECL	Output current				30	mA
I_o MAX, CHPO	Output current				1	mA
V_i MAX	Input voltage		$V_{EE} - 0.5$		0.5	V
I_i MAX	Input current		-1.0		1.0	mA
T_o	Operating temperature	Junction	-55		125	°C
T_s	Storage temperature		-65		150	°C

DC Characteristics

$T_{CASE} = 0\text{ °C to }85\text{ °C}$, $V_{EE} = -5.0\text{ V}$

All voltages in the table are referred to VDD.

All input signal and power currents in the table are defined positive into the pin.

All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{EE}	Supply voltage		-5.40	-5.0	-4.5	V
I_{EE}	Supply current	Note 1		180		mA
V_i SINX/SIPX	Data input sensitivity, differential/single-ended	Note 2		20	25	mV
V_i MAX SINX/SIPX	Maximum input voltage swing, differential	Note 6			500	mV
V_{ICM} SINX/SIPX	Data common mode		-2	-1.3	-1	V
V_{IH} ECL	ECL input high voltage	Note 1	-1.1		0	V
V_{IL} ECL	ECL input low voltage	Note 1	V_{EE}		-1.5	V
I_{IH} ECL	ECL input high current				100	μA
I_{IL} ECL	ECL input low current				100	μA
V_i VCTL	VCO control voltage	$I_{VCTL} < 30\text{ μA}$	V_{EE}		-1	V
V_{OH} ECL	ECL output high voltage	Note 3, 4	-1.0		-0.5	V
V_{OL} ECL	ECL output low voltage	Note 3, 4	V_{TT}		-1.6	V
I_{OH} CHPO	CHPO source current	Note 5		400		μA
I_{OL} CHPO	CHPO sink current	Note 5		400		μA

Note 1: $V_{EE} = -5.0\text{ V}$

Note 2: AC-coupled, p-p voltage for differential coupling, BER 10^{-12} . Data eye diagram in accordance with ITU G.957, $2^{23} - 1$ PRBS, terminated via loop through 50 Ω .

Note 3: $V_{TT} = -2.0\text{ V} \pm 5\%$

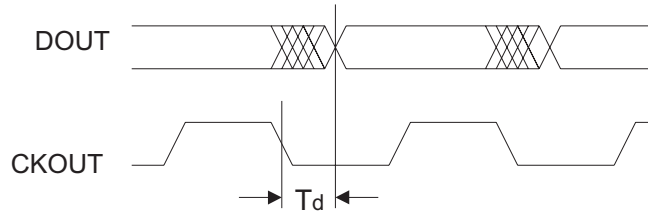
Note 4: $R_L = 50\text{ Ω to }V_{TT}$

Note 5: Output terminated to -2.5 V during test.

Note 6: AC coupled input, p-p voltage.

AC Characteristics

$T_{CASE} = 0\text{ }^{\circ}\text{C to } 85\text{ }^{\circ}\text{C}$, $V_{EE} = -5.0\text{ V}$



Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
J_{TOL}	Jitter tolerance Note 1. See Figure 8.	$2\text{ Hz} < f < 100\text{ kHz}$ $1\text{ MHz} < f < 5\text{ MHz}$	1.5 0.15	>2 >0.35		UI _{16, p-p} Note 2
J_{TRF}	Jitter transfer Note 1. See Figure 9.	$12\text{ kHz} < f < 2\text{ MHz}$		0.08	0.1	dB
J_{OUT}	Output clock intrinsic jitter Note 1	$5\text{ kHz} < f < 1\text{ MHz}$ $1\text{ MHz} < f < 20\text{ MHz}$			0.125 0.05	UI _{4, p-p} UI _{4, p-p} Note 2
T_A	Acquisition time	$2^{23} - 1$ PRBS		50	500	μs
L_{CID}	Consecutive identical bits	# of bits with no transition	400	1000		bits
D_C	Input data / REFXXI frequency deviation	Note 3	-200		200	ppm
$C_{DUTY, REFXXI}$	REFXXI clock duty cycle	$V_{thr} = -1.3\text{ V}$	40		60	%
F_{VCO}	VCO centre frequency			2.5		GHz
$C_{DUTY, CKOUT}$	Output clock duty cycle	$V_{thr} = -1.3\text{ V}$, $50\ \Omega$ to -2.0 V	45		55	%
$T_{RISE, ECL}$	ECL output rise time	20 - 80%, $50\ \Omega$ to -2.0 V		350	700	ps
$T_{FALL, ECL}$	ECL output fall time	80 - 20%, $50\ \Omega$ to -2.0 V		350	700	ps
$T_D, DOUXX$	Data output from CKOUT	See figure above		275		ps

Note 1: Jitter parameters acquired at $V_{EE} = 5.0\text{ V} \pm 5\%$, $R = 33\ \Omega$, and $C = 2.2\ \mu\text{F}$. When shifting the V_{EE} range and tolerance, R and C values should be changed to accommodate changed loop gain parameters.

Note 2: $1\text{ UI}_{16, p-p} = 402\text{ ps}$. $1\text{ UI}_{4, p-p} = 1.608\text{ ns}$.

Note 3: Maximum allowable deviation between reference clock and divided VCO clock when locked to data.

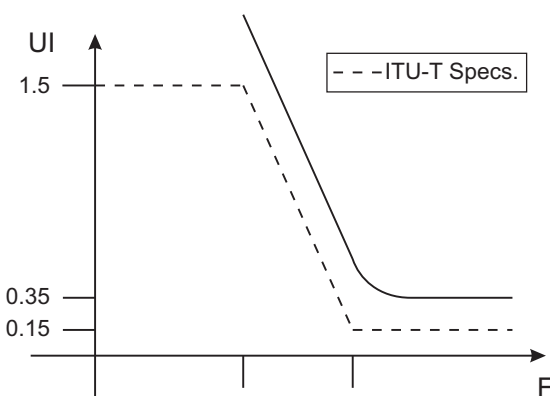


Figure 8. Jitter Tolerance, Typical

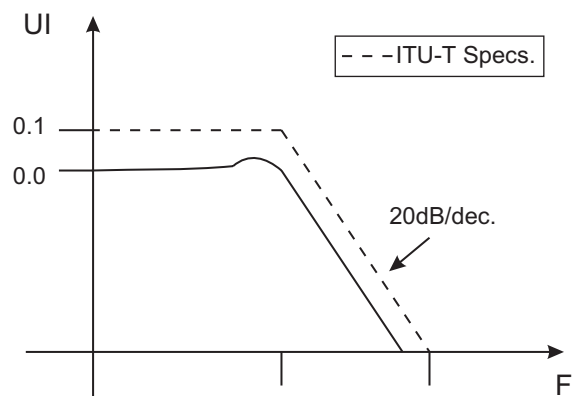


Figure 9. Jitter Transfer, Transfer

Package Outline

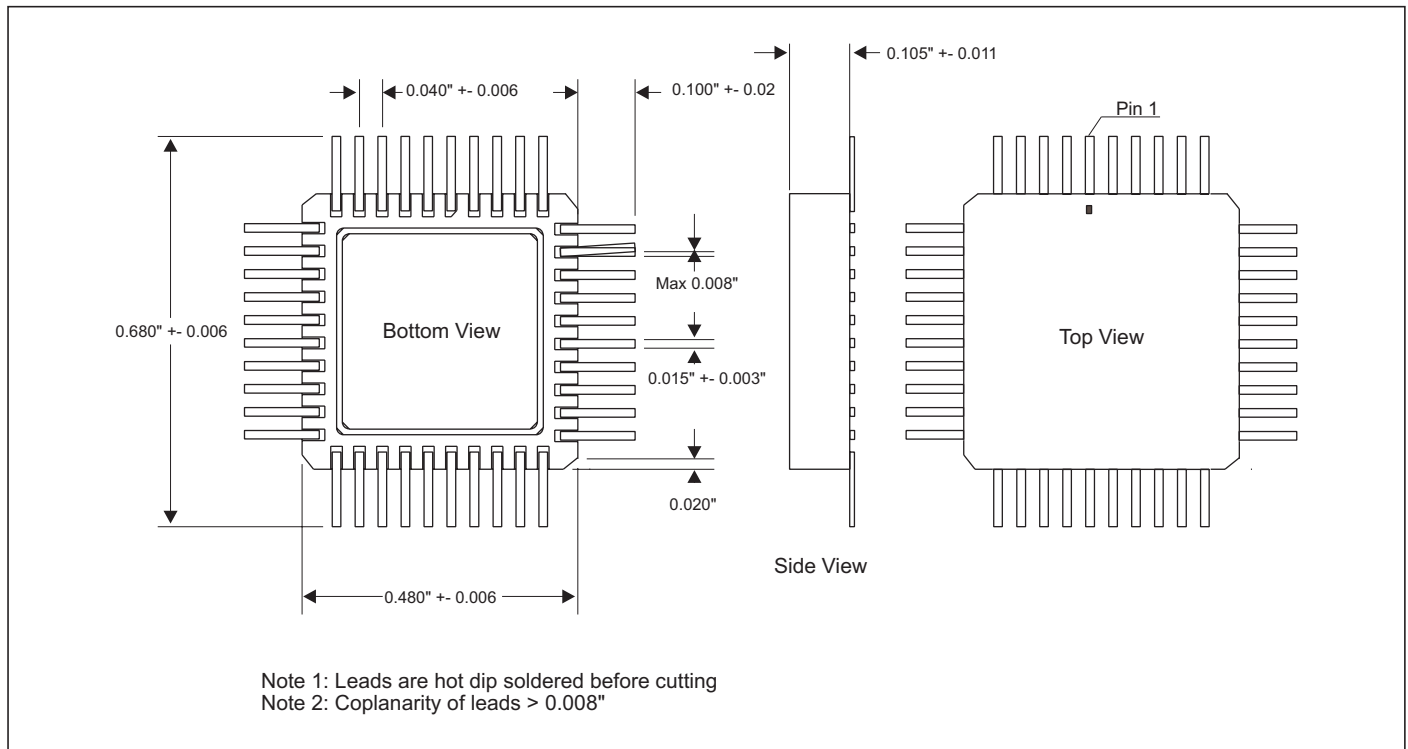


Figure 10. 40 Lead LCC, Leaded (All Dimensions are in inch)

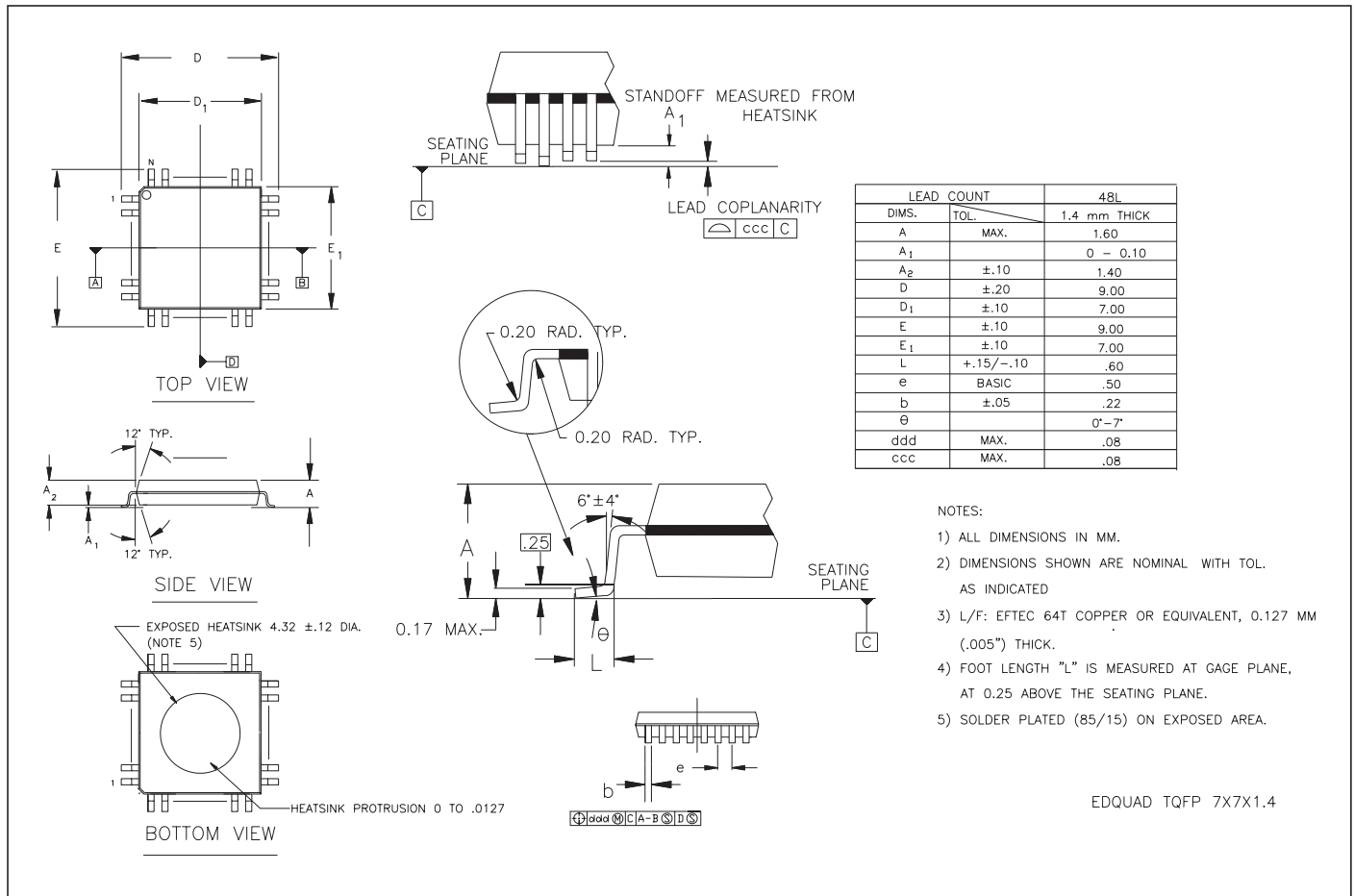


Figure 11. 48 Lead TQFP, Power Enhanced (All Dimensions are in mm)

External References

ITU-T G.825 (03/93) Control of Jitter and Wander within digital networks based on SDH
ITU-T G.957 (07/95) Optical interfaces for equip. and systems relating to SDH
ITU-T G.958 (11/94) Digital line systems based on SDH for use on optical fibre cables

Device Marking



Figure 12. Device Marking, (Top - 48 pin and Bottom - 40 pin)

Ordering Information

To order, please specify as shown below:

Product Name:	Intel Order Number:	Package Type:	Case Temperature Range:
GD16543-40AC		40 lead Ceramic LCC	0..85 °C
GD16543-40AB		40 lead Ceramic LCC, leaded	0..85 °C
GD16543-48BA	FAGD1654348BA MM#: 836065	48 lead TQFP, EDQUAD	0..85 °C



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