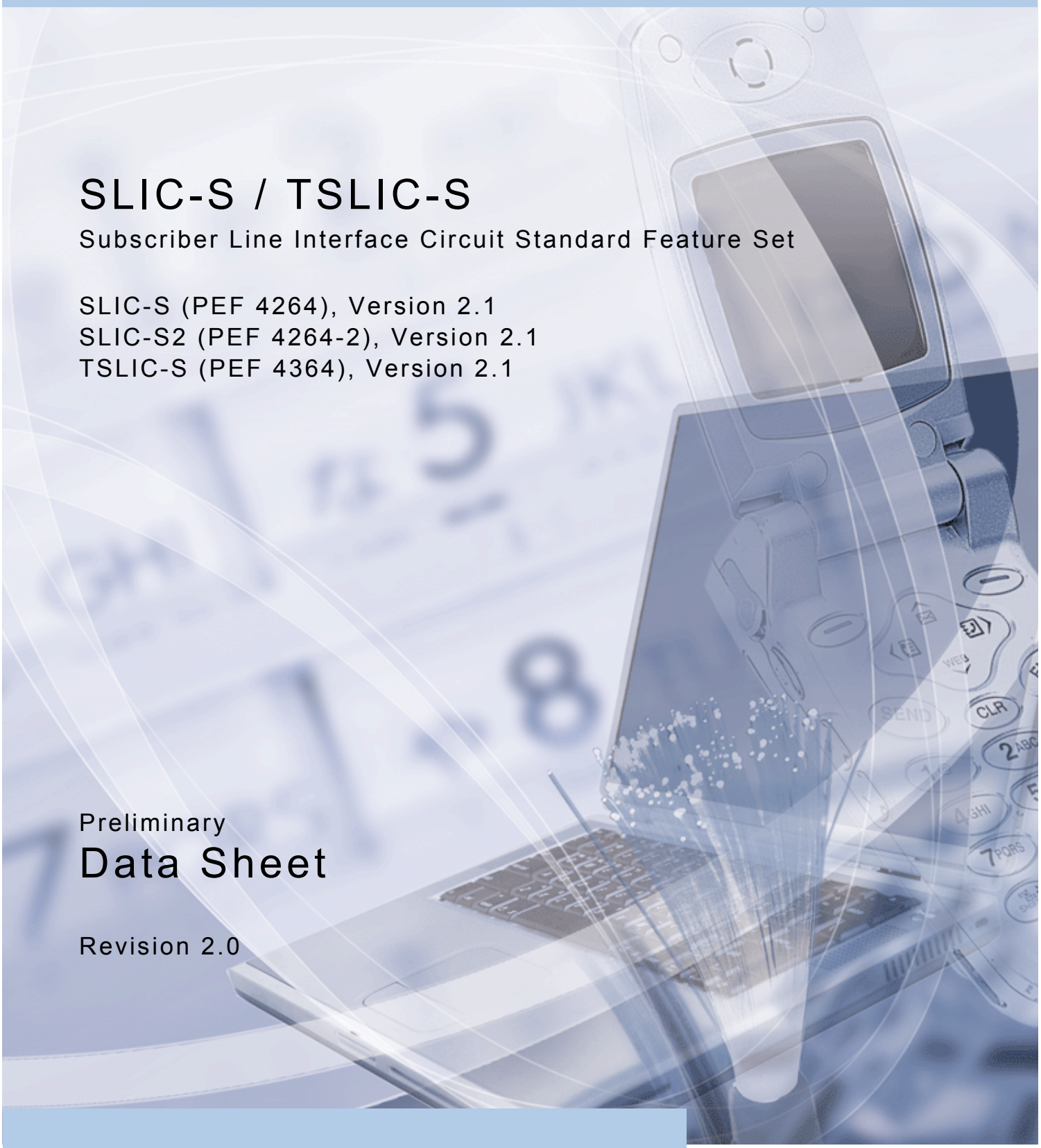
October 2006

SLIC-S / TSLIC-S

Subscriber Line Interface Circuit Standard Feature Set

SLIC-S (PEF 4264), Version 2.1
SLIC-S2 (PEF 4264-2), Version 2.1
TSLIC-S (PEF 4364), Version 2.1



Preliminary

Data Sheet

Revision 2.0

Communication Solutions

Never stop thinking

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SLIC-S / TSLIC-S Subscriber Line Interface Circuit Standard Feature Set

Revision History: 2006-10-10, Revision 2.0

Previous Version: Revision 1.0

Page	Subjects (major changes since last revision)
Page 38	"Recommended PCB Foot Print Pattern for PG-DSO-36-15 Package" on Page 38 modified.

Trademarks

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1 General Description

Infineon Technologies' high voltage ringing Subscriber Line Interface Circuit SLIC-S (PEF 4264) Version 2.1 (V2.1) is the latest out of the well-known and broadly used SLIC-S family. It has been designed not only to cover all previous SLIC-S applications, but also to extend the supply voltage range to 120 V to enable balanced sinusoidal ring signals up to 65 V_{rms}.

As SLIC-S V2.1 is pin compatible with its previous versions, it can be operated with all codec devices of the DuSLIC® or VINETIC® chip sets. The highly flexible device offers 3.3 V and 5 V compatibility. Integrated supply switches allow the choice between two negative battery voltages for voice transmission, whereas in the ring mode an additional positive supply voltage is used.

To minimize the average system power dissipation, a power-down mode can be utilized; the transmission part is switched off completely and off-hook supervision is provided by activating a simple line current sensor with negligible power consumption.

SLIC-S V2.1 is available in a single (PEF 4264) channel version in either PG-DSO-20-24 or PG-VQFN-48-15 power packages, or in a dual channel version (PEF 4364), packaged in PG-DSO-36-15.

1.1 Version 2.1: Summary of Changes

Compared with the previous version of SLIC-S (PEB 4264 V1.2), the new version V2.1 is characterized by the following changes:

- Increased supply voltage range VHR - VBATH of up to 120 V
- Sinusoidal ring voltage up to 65 V_{rms}
- High impedance DC inputs
- Fully differential receive path - VCMS pin not required
- Fast current limitation for improved overvoltage behaviour
- Electrical Parameters (**Chapter 4.5**):
  - Supply currents
  - Open loop resistances RTG, RRB
  - Power down open loop line voltage
  - Off-hook output current on IT
  - IT output current reverse polarity (limitation with VDD = 3.3 V)
- Application circuit:
  - 100 nF / 50 V capacitor at CEXT
  - Per channel series diode in VBATL supply mandatory (no shared diodes)

1.2 Features

- High voltage SLIC with integrated ringing
- Compatible with both 3.3 and 5 V systems
- Available in single and dual-channel versions
- High-voltage line feed (long loop driving capability)
- Sensing of transversal and longitudinal line currents
- Two Battery voltages (–15 V … –70 V)
- Positive ring supply voltage up to +70 V
- Total supply voltage up to 120 V
- Integrated balanced ringing up to 65 V_{rms}
- High longitudinal balance performance with SLIC-S2 (PEF 4264-2)
- Power-saving active mode (ACTL) with reduced battery voltage
- Power Down mode with negligible power consumption
- Package options:
  - PG-DSO-20-24
  - PG-VQFN-48-15
  - PG-DSO-36-15 (dual channel)
- Reliable Smart Power Technology

PG-DSO-20-24

PG-VQFN-48-15

PG-DSO-36-15

Product Name	Product Type	Package
SLIC-S / SLIC-S2	PEF 4264T / PEF 4264-2T	PG-DSO-20-24
SLIC-S / SLIC-S2	PEF 4264V / PEF 4264-2V	PG-VQFN-48-15
TSLIC-S	PEF 4364T	PG-DSO-36-15

1.3 Logic Symbol

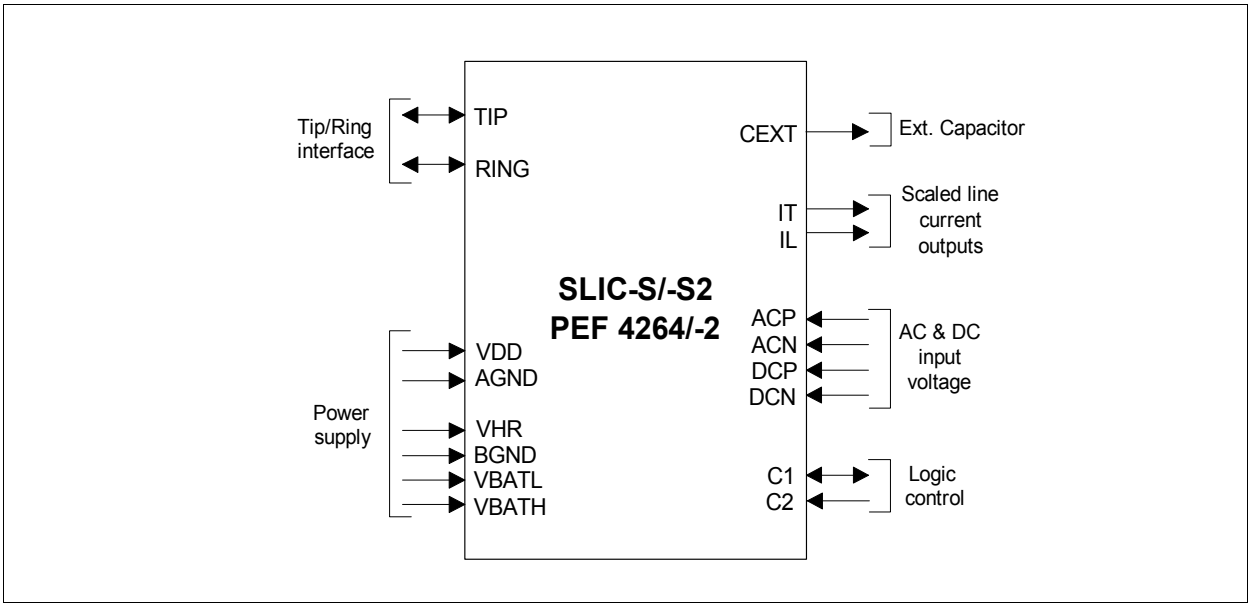


Figure 1 Logic Symbol SLIC-S/-S2 (PEF 4264/-2)

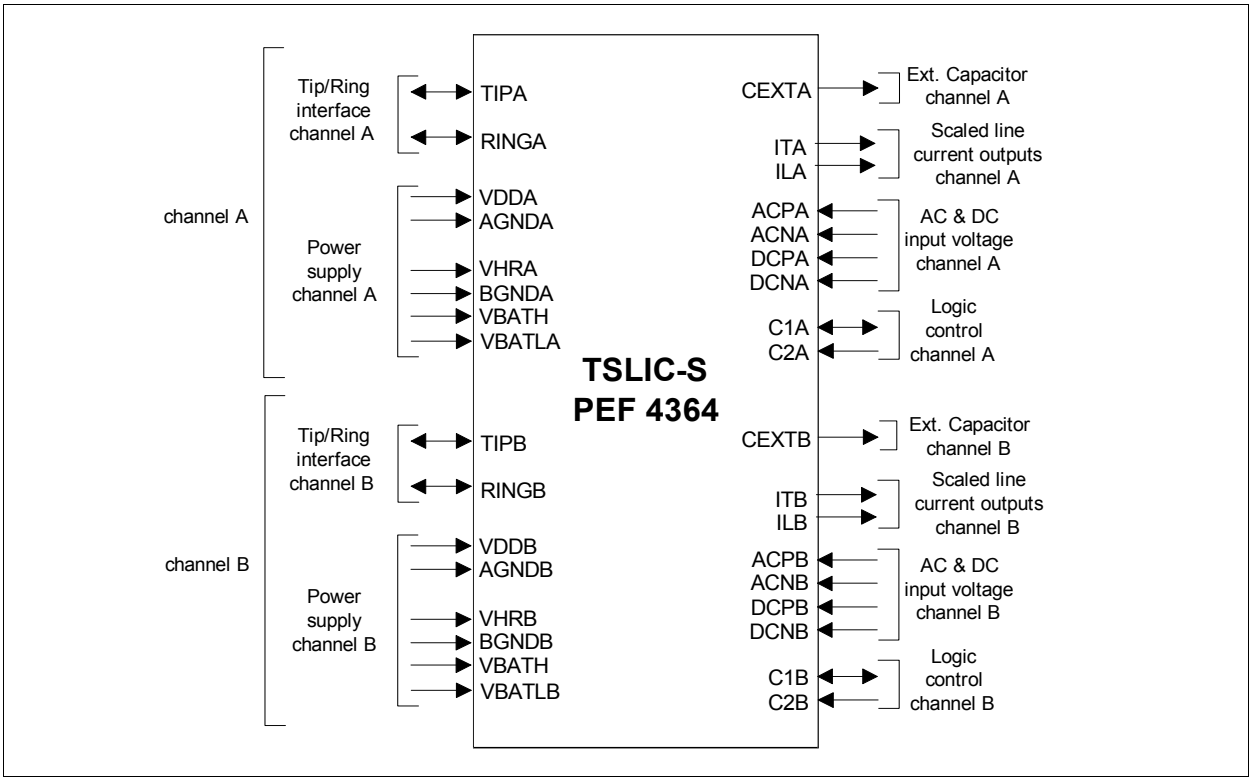


Figure 2 Logic Symbol TSLIC-S (PEF 4364)

1.4 Pin Configuration

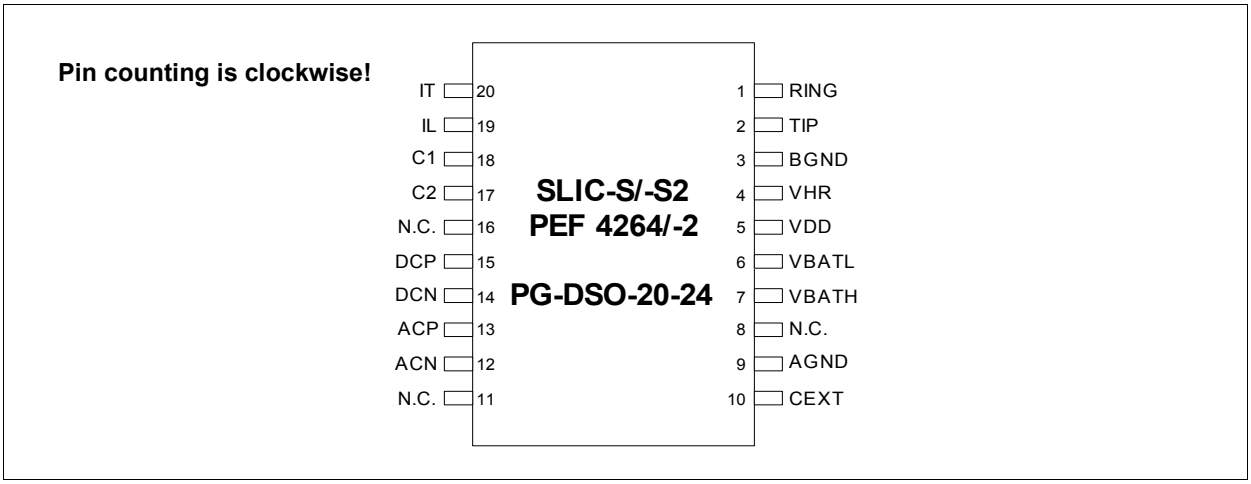


Figure 3 Pin Configuration PG-DSO-20-24 Package (top view)

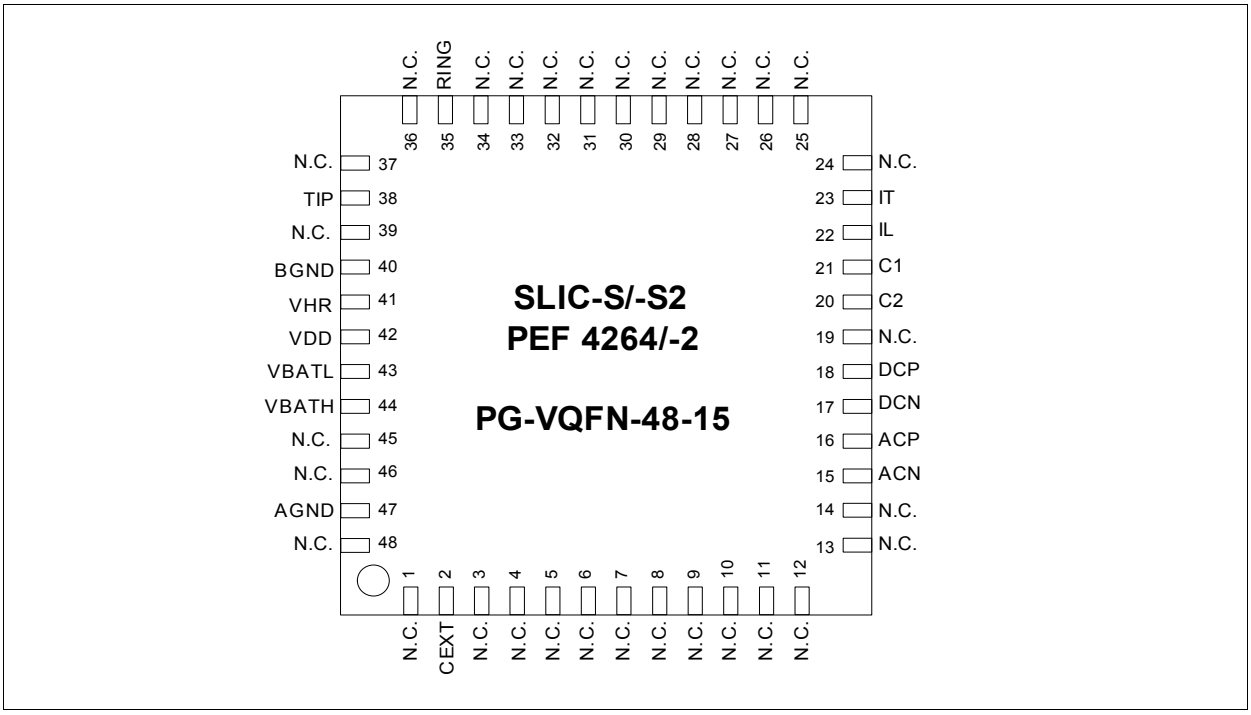


Figure 4 Pin Configuration PG-VQFN-48-15 Package (top view)

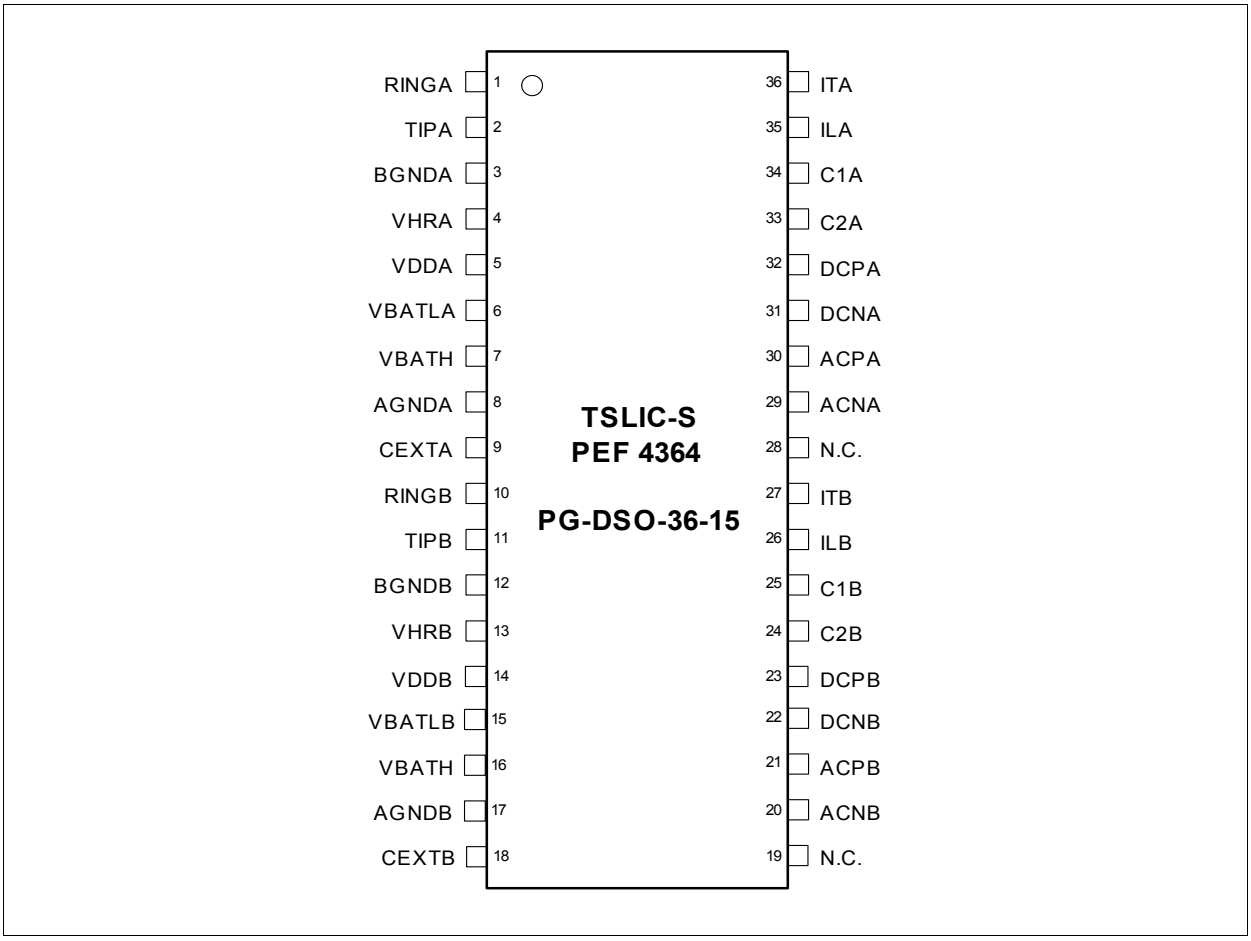


Figure 5 Pin Configuration PG-DSO-36-15 Package (dual channel) (top view)

1.5 Pin Definitions and Functions

Table 1 Pin Definitions and Functions PG-DSO-20-24 and PG-VQFN-48-15

Pin No. PG-DSO-20-24	Pin No. PG-VQFN-48-15	Name	Pin Type	Function
1	35	RING	I/O	Subscriber loop connection RING
2	38	TIP	I/O	Subscriber loop connection TIP
3	40	BGND	GND	Battery ground: reference for TIP, RING, VBATH, VBATL and VHR
4	41	VHR	PWR	Auxiliary positive battery supply voltage used in ringing mode (5 V ≤ V_{HR} ≤ 70 V)
5	42	VDD	PWR	Positive supply voltage (+3.3 or +5 V), referred to AGND
6	43	VBATL	PWR	Second negative battery supply voltage (-15 V ≥ V_{BATL} ≥ V_{BATH})
7	44	VBATH	PWR	Most negative battery supply voltage; chip substrate potential (–20 V ≥ V_{BATH} ≥ –70 V)
9	47	AGND	GND	Analog ground: reference for VDD and all signal and control pins except TIP and RING
10	2	CEXT	O	Common mode line potential with high output resistance (160 kΩ); an external capacitance allows supply voltage filtering
12 13	15 16	ACN ACP	I	ACP - ACN: differential two-wire AC input voltage; at TIP/RING amplified by -6
14 15	17 18	DCN DCP	I	DCP - DCN: differential DC or ring input voltage; at TIP/RING amplified by -30 (ACTL, ACTH) and -60 (ACTR mode), respectively
17	20	C2	I	Ternary logic input, controlling the operation mode
18	21	C1	I/O	Ternary logic input, controlling the operation mode in case of thermal overload (chip temperature exceeding 165 °C) this pin sinks a current of typically 150 µA.
19	22	IL	O	Current output: longitudinal line current scaled down by a factor of 100
20	23	IT	O	Current output: transversal line current scaled down by a factor of 50
8, 11, 16	1)	N.C.		Not connected

1) For the PG-VQFN-48-15 package the following pins are not connected:
1,3,4,5,6,7,8,9,10,11,12,13,14,24,25,26,27,28,29,30,31,32,33,34,36,37,39,45,46,48

Table 2 Pin Definitions and Functions PG-DSO-36-15

Pin No.	Name	Pin Type	Function
1 10	RINGA RINGB	I/O	Subscriber loop connection RING (Channel A) Subscriber loop connection RING (Channel B)
2 11	TIPA TIPB	I/O	Subscriber loop connection TIP
3 12	BGNDA BGNDB	GND	Battery ground: reference for TIP, RING, VBATH, VBATL and VHR
4 13	VHRA VHRB	PWR	Auxiliary positive battery supply voltage used in ringing mode (5 V ≤ V_{HR} ≤ 70 V)
5 14	VDDA VDDB	PWR	Positive supply voltage (+3.3 or +5 V), referred to AGND
6 15	VBATLA VBATLB	PWR	Second negative battery supply voltage (–15 V ≥ V_{BATL} ≥ V_{BATH})
7, 16	VBATH	PWR	Most negative battery supply voltage; chip substrate potential (–20 V ≥ V_{BATH} ≥ –70 V)
8 17	AGNDA AGNDB	GND	Analog ground: reference for VDD and all signal and control pins except TIP and RING
9 18	CEXTA CEXTB	O	Common mode line potential with high output resistance (160 kΩ); an external capacitance allows supply voltage filtering
29, 30 20, 21	ACNA, ACPA ACNB, ACPB	I	ACP - ACN: differential two-wire AC input voltage; at TIP/RING amplified by -6
31, 32 22, 23	DCNA, DCPA DCNB, DCPB	I	DCP - DCN: differential DC or ring input voltage; at TIP/RING amplified by -30 (ACTL, ACTH) and -60 (ACTR mode), respectively
33 24	C2A C2B	I	Ternary logic input, controlling the operation mode
34 25	C1A C1B	I/O	Ternary logic input, controlling the operation mode in case of thermal overload (chip temperature exceeding 165 °C) this pin sinks a current of typically 150 µA.
35 26	ILA ILB	O	Current output: longitudinal line current scaled down by a factor of 100
36 27	ITA ITB	O	Current output: transversal line current scaled down by a factor of 50
19, 28	N.C.		Not connected

1.6 Functional Block Diagram

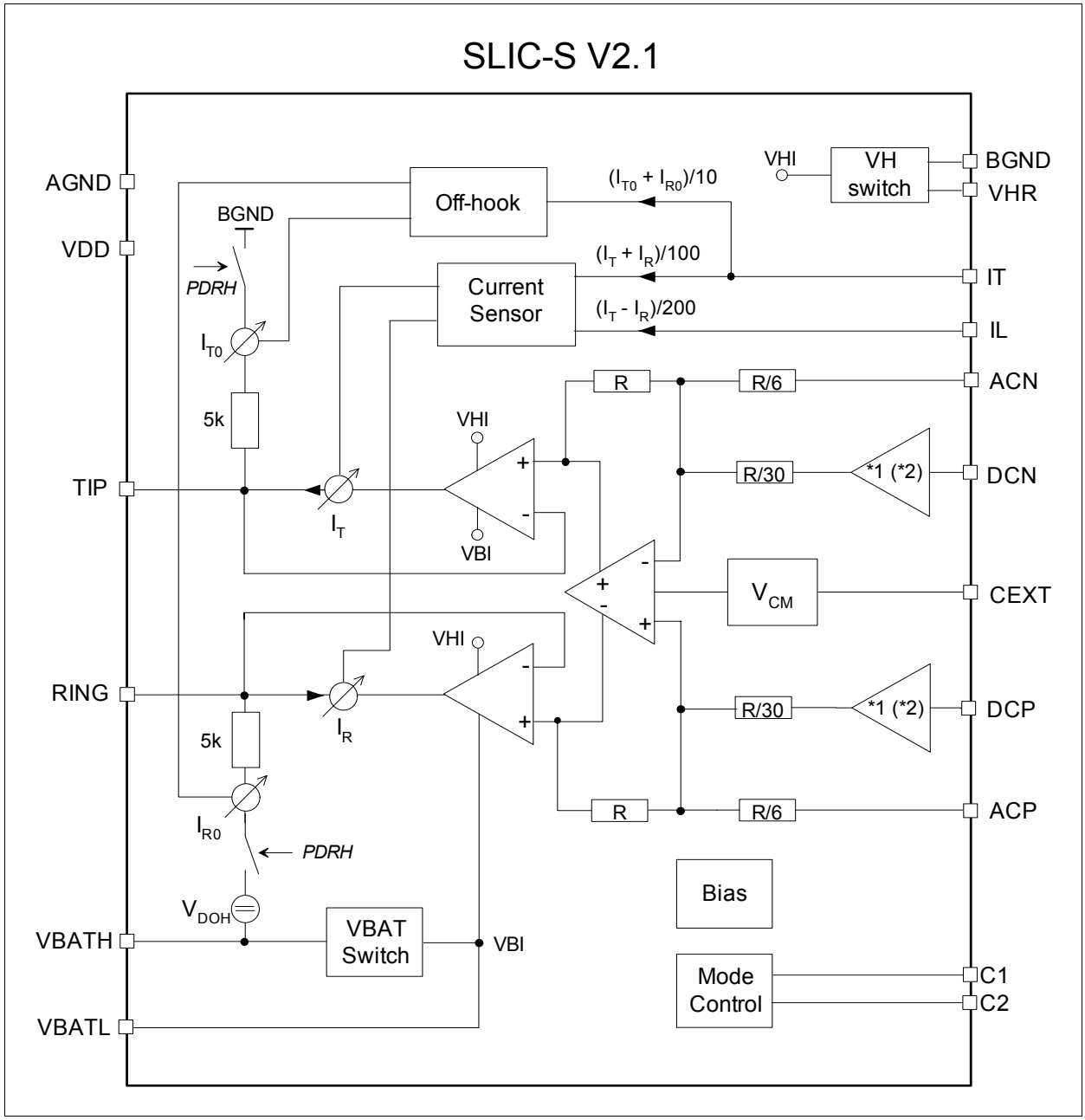


Figure 6 Block Diagram

*Note: As in the dual channel version both channels "A" and "B" are identical, channel independent pin names (e.g. "TIP" instead of "TIPA / TIPB") are used throughout this document (with the exception of **Table 2**)*

2 Functional Description

A functional block diagram is shown in **Figure 6**.

SLIC-S V2.1 supports AC and DC control loops based on feeding a voltage V_{TR} to the line and sensing the transversal line current I_{Trans} and the longitudinal current I_{Long}.

In receive direction, DC and AC voltages are handled separately with different gains. Both are applied differentially via the codec interface pins DCP / DCN and ACP / ACN, respectively, defining the transversal line voltage V_{TR} through

$V_{TR} = V_{TIP} - V_{RING} = V_{ab} =$

$= 30 * (V_{DCP} - V_{DCN}) + 6 * (V_{ACP} - V_{ACN})$ for modes ACTH, ACTL

$= 60 * (V_{DCP} - V_{DCN}) + 6 * (V_{ACP} - V_{ACN})$ for mode ACTR

As the ring signal is processed in the DC path, the DC gain is doubled in the ring mode ACTR to enable the full output voltage swing.

The common mode line voltage is always equal to the mean supply voltage, $V_{CM} = (V_{HI} + V_{BI}) / 2$, leading to symmetrical line potentials with respect to the supplies. Depending on the operation mode, V_{HI} is switched either to V_{HR} or to BGND via the VH switch, whereas V_{BI} is connected either to V_{BATH} via the VBAT switch or to V_{BATL} via an external diode.

A reversed polarity of V_{TR} is easily obtained by changing the polarity of $(V_{DCP} - V_{DCN})$.

In transmit direction, the transversal and longitudinal line currents I_{Trans} and I_{Long} (**Figure 7**) are measured, and scaled images are provided at the IT and IL pins, respectively:

$I_{IT} = (I_T + I_R) / 100 = I_{Trans} / 50$

$I_{Trans} = (I_T + I_R) / 2$

$I_{IL} = (I_T - I_R) / 200 = I_{Long} / 100$

$I_{Long} = (I_T - I_R) / 2$

For off-hook detection in PDRH mode, 5 kΩ resistors are connected from TIP to BGND and from RING to VBATH, respectively. The currents through these resistors, I_{T0} and I_{R0}, are sensed, scaled and provided at IT:

$I_{IT0} = (I_{T0} + I_{R0}) / 10 = I_{TRANS0} / 5$

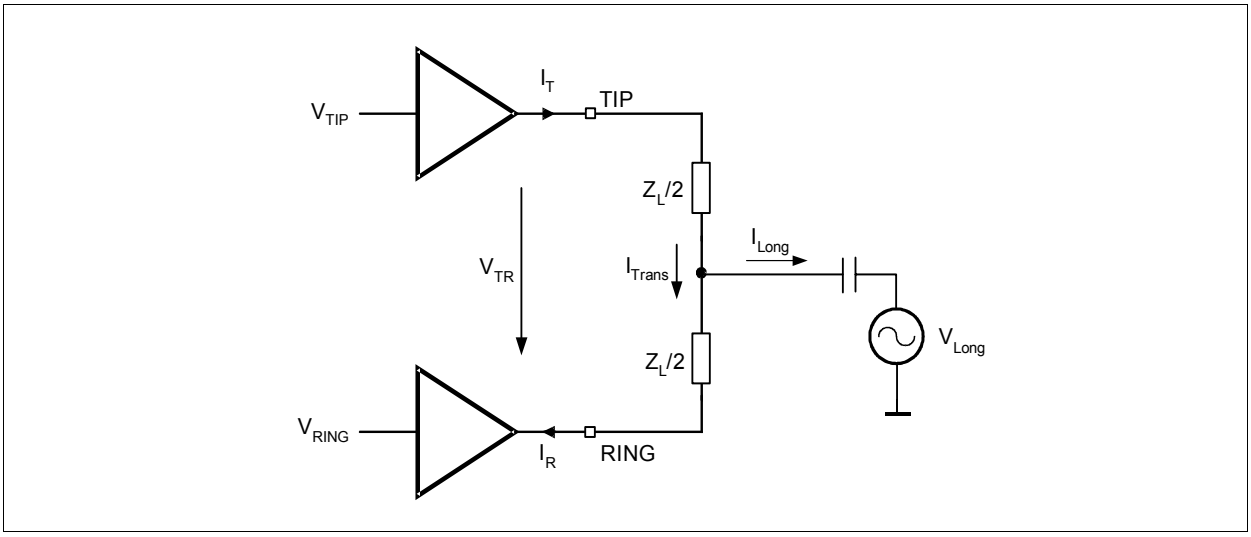


Figure 7 Transversal and Longitudinal Line Currents

2.1 Operating Modes

SLIC-S V2.1 operates in the following modes controlled by ternary logic signals at C1 and C2:

Table 3 SLIC-S Mode Table

		C2		
		L	**M**	**H**
C1	**L**[1)]	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

1) No ‘Overtemp’ signaling possible via pin C1, if C1 is low.

Table 4 SLIC-S Modes and Supplies

Mode	Mode Description	Internal Supply Voltages V_{BI}, V_{HI}
PDH	Power Down High Impedance	VBATH, VH switch open
PDRH	Power Down Resistive High	VBATH, VH switch open
PDRHL	Power Down Resistive High Load	VBATH, VH switch open
ACTL	Active Low	VBATL, BGND
ACTH	Active High	VBATH, BGND
ACTR	Active Ring	VBATH, VHR
HIRT	High Impedance on RING and TIP	VBATH, VHR
HIT	High Impedance on TIP	VBATH, VHR
HIR	High Impedance on RING	VBATH, VHR

Power Down High Impedance (PDH)

PDH offers high impedance at TIP and RING; it can be used for testing purposes or when an error condition occurs. In PDH mode all functions are switched off. Off-hook detection is not available.

Power Down Resistive High (PDRH)

Power consumption is reduced to a minimum by switching completely off all voice transmission functions. To allow off-hook detection, PDRH provides a connection of 5 kΩ each from TIP to BGND and RING to VBATH, respectively, while the output buffers show high impedance (see **Figure 6**). The current through these resistors is sensed, scaled by 1/5 and transferred to the IT pin for off-hook supervision.

Power Down Resistive High Load (PDRHL)

PDRHL is used as a transition state from Power Down to Active modes (automatically initiated during a mode change). It causes fast preloading of CEXT in order to suppress line voltage transients.

Active Low (ACTL), Active High (ACTH)

These are the regular transmission modes for voiceband. The line-driving section is operated between BGND and VBATL (ACTL) or VBATH (ACTH).

Active Ring (ACTR)

Utilizing an additional positive battery voltage V_{HR}, this mode allows balanced ringing of up to 65 Vrms or feeding of very long telephone lines. In ACTR mode the DC voltage gain is doubled to 60.

High Impedance (HIR, HIT, HIRT)

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer is still sensed. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes).

2.2 Current Limitation / Overtemperature Protection

In any operating mode the total current delivered by the output drivers is limited to typically 85 mA.

If, however, the junction temperature exceeds 165 °C, the current limit is further reduced to keep the junction temperature constant.

Simultaneously, pin C1 sinks a signalling current I_{therm}.

3 Typical Application Circuit for DuSLIC® and VINETIC®

Figure 8 to **Figure 9** show one channel of application circuits including SLIC-S / TSLIC-S V2.1 and SLICOFI®-2/-2S or VINETIC® codec (please refer to the latest DuSLIC® or VINETIC® Data Sheet).

In **Table 5** the recommended external components for a dual channel DuSLIC® or VINETIC® system and their typical values are listed.

Table 5 External Components DuSLIC® / VINETIC® for 2 Channels

No.	Symbol	Value	Unit	Relat. Tol.	Rating	DuSLIC® Systems	VINETIC® Systems
2	R_{IT1}	470	Ω	1 %	–	x	–
2	R_{IT1}	510	Ω	1 %	–	–	x
2	R_{IT2}	680	Ω	1 %	–	x	x
2	R_{IL}	1.6	kΩ	1 %	–	x	x
4	R_{STAB}	30	Ω	1 %[1)]	–	x	x
4	C_{STAB}	15			100 V	x	x
2	C_{DC}	120	nF	10 %	10 V	x	–
2	C_{DC}	220	nF	10 %	10 V	–	x[2)]
2	C_{ITAC}	680	nF	10 %	10 V	x	–
2	C_{ITAC}	1	µF	10 %	10 V	–	x
1	C_{PRE}	18	nF	5 %	10 V	–	x
2	C_{VCMIT}	680	nF	10 %	10 V	x	–
1	C_{REF}	68	nF	20 %	10 V	x	x
2	C_{EXT}	100	nF	20 %	50 V	x	x
6	C_1	100	nF	10 %	10 V	x	–
13	C_1	100	nF	10 %	10 V	–	x
6	C_2	100	nF	10 %	100 V	x	x
1	C_3	4.7	µF	20 %	10 V, Tantal	x	–
4	D_1, D_2	BAS 21	–	–	–	x	x
2	D_3[3)]	BAS 21	–	–	–	x	x
2	OVP[4)]	Overvoltage Protection (e.g. thyristor)	–	–	–	x	x
4	OCP[4)]	Overcurrent Protection (e.g. LFR, fuse, PTC)	–	–	–	x	x

1) Matching tolerance depends on longitudinal balance requirements (for details see **[2]**).

2) With VINETIC®-2CPE this capacitance is substituted by 100 nF between DCN and DCP.

3) Due to the changed battery switch concept (see **Figure 6**), the VBATL series diode must not be shared between different channels; one diode per channel is mandatory (also for applications with TSLIC-S).

4) See **[1]**

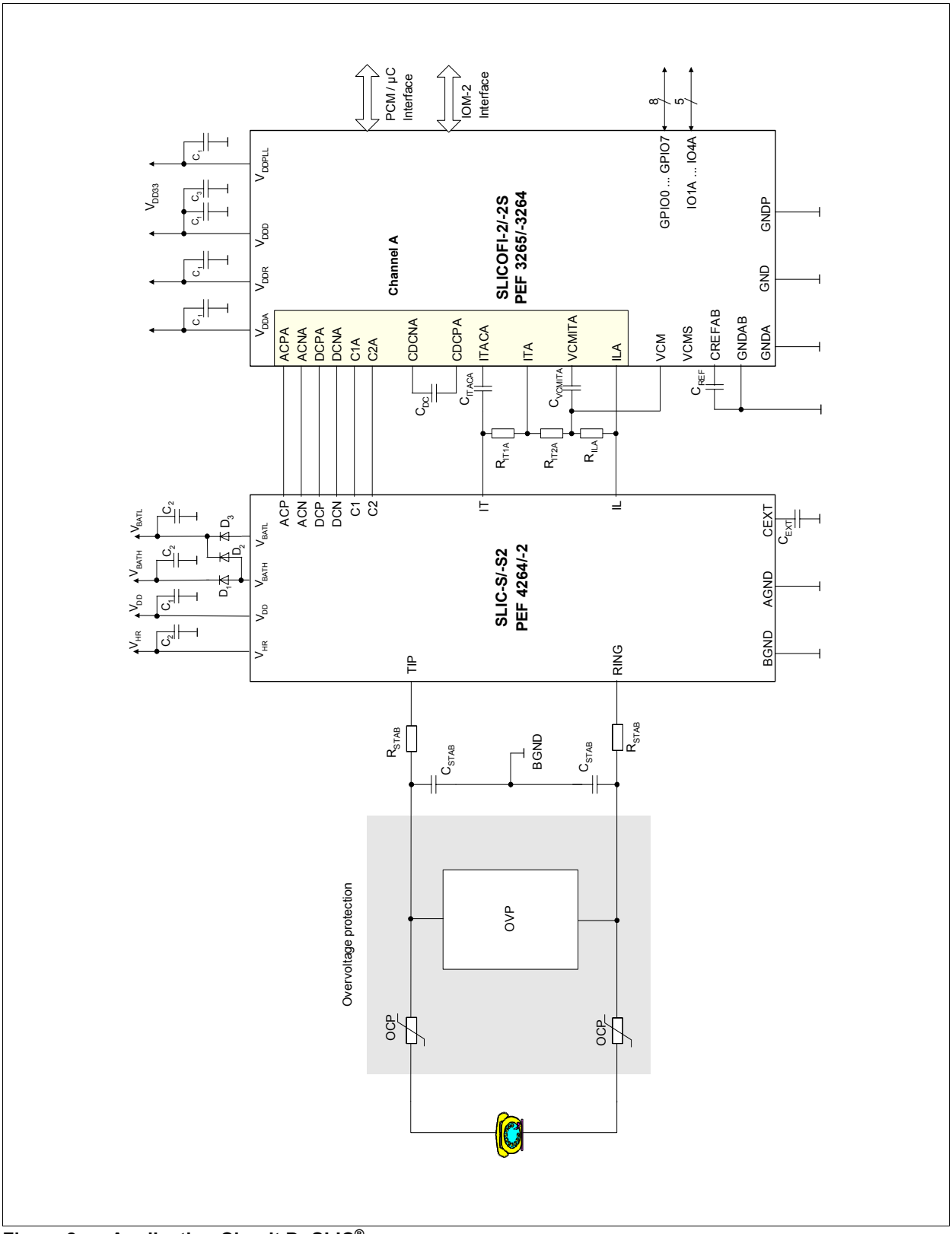


Figure 8 Application Circuit DuSLIC®

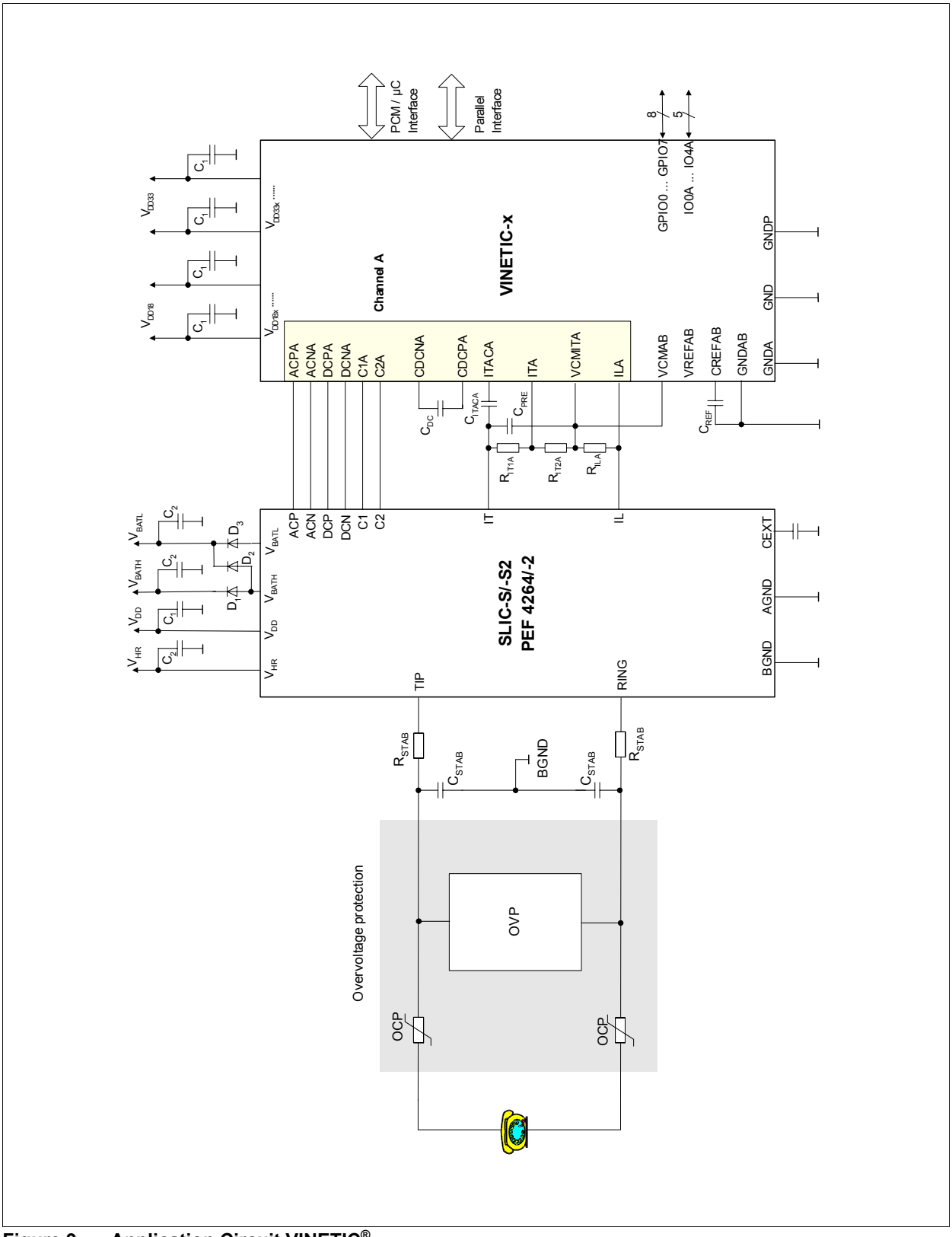


Figure 9 Application Circuit VINETIC®

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Battery voltage low	V_{BATL}	–70	–	0.4	V	Referred to BGND
Battery voltage high	V_{BATH}	–75	–	0.4	V	Referred to BGND
Battery voltage difference	$V_{BATL} - V_{BATH}$	–0.4	–	–	V	–
Auxiliary supply voltage	V_{HR}	–0.4	–	75	V	Referred to BGND
Total battery supply voltage, continuous	$V_{HR} - V_{BATH}$	–0.4	–	125	V	–
V_{DD} supply voltage	V_{DD}	–0.4	–	7	V	Referred to AGND
Ground voltage difference	$V_{BGND} - V_{AGND}$	–0.4	–	0.4	V	–
Input voltages	V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{C1}, V_{C2}, V_{C3}	–0.4	–	V_{DD} + 0.4	V	Referred to AGND
Junction temperature	T_j	–	–	150	°C	–
ESD voltage, all pins	–	–	–	1	kV	SDM (Socketed Device Model)[1)]
	–	–	–	1	kV	HBM (Human Body Model)[1)]

1) EOS/ESD Assn. Standard DS5.3-1993.

Attention: Stresses exceeding the max. values listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Foreign Line Voltages

External voltages applied at the line outputs may cause large currents in the SLIC. The resulting on-chip power dissipation has to be limited to avoid thermal destruction, if the overtemperature protection cannot react sufficiently fast due to high local power density. The safe power dissipation values are strongly dependent on duration. They can be expressed in terms of voltage and current limits directly at the TIP and RING pins (see **Table 7** and **Table 8**).

Table 7 Voltage Limits on Output Pins

Voltage Duration	Pins	Min. Voltage [V]	Max. Voltage [V]
Continuous	TIP, RING	V_{BATH} – 0.4	V_{HR} + 5
< 10 ms	TIP, RING	V_{BATH} – 5	V_{HR} + 10
< 100 µs	TIP, RING	V_{BATH} – 10	V_{HR} + 20
< 1 µs	TIP, RING	V_{BATH} – 15	V_{HR} + 20

Table 8 Current Limits on Output Pins

Current Duration	Pins	Min. current [A]	Max. current [A]
Continuous	TIP, RING	– 0.1	0.1
< 10 ms	TIP, RING	– 0.5	0.5
< 100 µs	TIP, RING	– 1.0	1.0
< 1 µs	TIP, RING	– 1.5	1.5

The above limitations have to be regarded as typical. They are valid simultaneously. Together with external circuitry they determine protection requirements (see **[1]**).

4.3 Operating Range

Table 9 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Battery voltage L[1)]	V_{BATL}	–65	–	–15	V	Referred to BGND
Battery voltage H [1)]	V_{BATH}	–70	–	–20	V	Referred to BGND
Auxiliary supply voltage	V_{HR}	V_{DD}	–	70	V	Referred to BGND
Total battery supply voltage	$V_{HR} - V_{BATH}$	–	–	120	V	–
V_{DD} supply voltage	V_{DD}	3.15	–	5.5	V	Referred to AGND
Ground voltage difference	$V_{BGND} - V_{AGND}$	–0.4	–	0.4	V	–
Voltage at pins IT, IL	V_{IT}, V_{IL}	–0.4	–	V_{DD} - 0.6	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}		0	–	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	–40	–	85	°C	–
Junction temperature	T_J	–	–	125[2)]	°C	–

1) If the battery switch is not used, VBATL has to be connected with VBATH

2) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

4.4 Thermal Resistances

Table 10 Thermal Resistances

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction to case	$R_{th, jC}$	–	2	–	K/W	All packages
Junction to ambient	$R_{th, jA}$	–	50	–	K/W	PG-DSO-20-24 without heatsink
		–	20	–	K/W	PG-DSO-20-24 with heatsink PG-DSO-36-15, 4-layer JEDEC PCB with vias, die pad soldered to PCB (footprint see **Chapter 6.3.1**)
		–	25	–	K/W	PG-VQFN-48-15, 4-layer JEDEC PCB with vias, die pad soldered to PCB (footprint see **Chapter 6.2.1**)

4.5 Electrical Parameters

Unless otherwise stated, minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at V_{BATH} = –48 V, V_{BATL} = –24 V, V_{HR} = +32 V and V_{DD} = +3.3 V.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extended temperature range operation at –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

4.5.1 Supply Currents and Power Dissipation

Table 11 Supply Currents, Power Dissipation (I_R = I_T = 0; V_{TR} = 0; one channel)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Power Down High Impedance, Power Down Resistive High							
V_{DD} current	I_{DD}	–	250	350	µA	–	1
V_{BATH} current	I_{BATH}	–	40	80	µA	–	2
V_{BATL} current	I_{BATL}	–	0	10	µA	–	3
V_{HR} current	I_{HR}	–	0	10	µA	–	4
Active Low							
V_{DD} current	I_{DD}	–	2.2	2.8	mA	–	5
V_{BATH} current	I_{BATH}	–	40	80	µA	–	6
V_{BATL} current[1)]	I_{BATL}	–	3.3	4	mA	–	7
V_{HR} current	I_{HR}	–	0	10	µA	–	8
Active High							
V_{DD} current	I_{DD}	–	2.6	3.2	mA	–	9
V_{BATH} current[2)]	I_{BATH}	–	3.8	4.5	mA	–	10
V_{BATL} current	I_{BATL}	–	0	10	µA	–	11
V_{HR} current	I_{HR}	–	0	10	µA	–	12
Active Ring							
V_{DD} current	I_{DD}	–	1.5	2	mA	–	13
V_{BATH} current[3)]	I_{BATH}	–	3.5	4.3	mA	–	14
V_{BATL} current	I_{BATL}	–	0	10	µA	–	15
V_{HR} current[4)]	I_{HR}	–	1.8	2.3	mA	–	16
High Impedance on TIP or RING (HIR, HIT)							
V_{DD} current	I_{DD}	–	1.5	2	mA	–	17
V_{BATH} current	I_{BATH}	–	2.9	3.6	mA	–	18
V_{BATL} current	I_{BATL}	–	0	10	µA	–	19
V_{HR} current	I_{HR}	–	1.3	1.7	mA	–	20
High Impedance on TIP and RING (HIRT)							
V_{DD} current	I_{DD}	–	1.4	1.8	mA	–	21
V_{BATH} current	I_{BATH}		2.2	2.8	mA	–	22

Table 11 Supply Currents, Power Dissipation (I_R = I_T = 0; V_{TR} = 0; one channel) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
V_{BATL} current	I_{BATL}	–	0	10	µA	–	23
V_{HR} current	I_{HR}	–	0.8	1.1	mA	–	24

1) Current depending on supply voltage: I_{BATL} (V_{BATL}) = I_{BATL} (-24 V) + (-V_{BATL} - 24) / 40 kΩ
2) Current depending on supply voltage: I_{BATH} (V_{BATH}) = I_{BATH} (-48 V) + (-V_{BATH} - 48) / 40 kΩ
3) Current depending on line voltage: I_{BATH} (V_{TR}) = I_{BATH} (0) + |V_{TR}| / 40 kΩ
4) Current depending on line voltage: I_{HR} (V_{TR}) = I_{HR} (0) + |V_{TR}| / 60 kΩ

The total power dissipated in the SLIC consists of the quiescent power P_Q due to the supply currents and the output stage power P_O caused by any line current I_{Trans} (see **Table 12**).

$P_{tot} = P_Q + P_O$

with $P_Q = V_{DD} * I_{DD} + |V_{BATH}| * I_{BATH} + |V_{BATL}| * I_{BATL} + V_{HR} * I_{HR}$

Table 12 Output Stage Power Dissipation

Operating Mode	Equation for P_O Calculation	Comment
ACTL	$P_O = (1.05 * \|V_{BATL}\| - V_{TR}) * I_{Trans}$	–
ACTH	$P_O = (1.05 * \|V_{BATH}\| - V_{TR}) * I_{Trans}$	–
ACTR	$P_O = (1.02 * V_{HR} + 1.05 * \|V_{BATH}\| - V_{TR}) * I_{Trans}$ $P_O = [4 * (V_H + \|V_{BATH}\|) - \pi * V_P * \cos\varphi] * V_P / (2 * \pi * Z_L)$	Ohmic load complex load $Z = Z_L e^{i\varphi}$, V_P ... peak ring voltage

For the dual channel version, the power values of each channel have to be added to yield the total power dissipation.

4.5.2 DC Characteristics

Table 13 DC Characteristics (V_{ACP} = V_{ACN} = 1.5 V)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Line Termination TIP, RING							
Differential DC line voltage	$V_{TR, DC}$	–0.4	0	0.4	V	V_{DCP} = V_{DCN} = 1.5 V Modes: ACTx	25
		23.5	24	24.5	V	V_{DCP} – V_{DCN} = 0.8 V Mode: ACTH	26
		–24.5	–24	–23.5	V	V_{DCP} – V_{DCN} = –0.8 V Mode: ACTH	27
Common mode DC line voltage	$V_{TIP, DC}$ = = $V_{RING, DC}$	–13	–12	–11	V	Mode: ACTL	28
		–25	–24	–23	V	Mode: ACTH	29
		–10	–9	–8	V	Mode: ACTR	30
DC line voltage drop (see **Figure 10**)	– V_{BATH} – $V_{TR, max}$	–	2.5	3	V	$I_{Trans,DC}$ = 20 mA V_{DCP} – V_{DCN} = 2.5 V Temp = 25°C[1)] Mode: ACTH	31
Output current limit (see **Figure 15**)	$\|I_{R, max}\|$, $\|I_{T, max}\|$	70 80	85 100	100 120	mA mA	V_T,V_R = 0 (sinking) V_T,V_R = V_{BATx} (sourcing) Temp = 25°C[2)]	32 33
Open loop resistance TIP to V_{BGND} (see **Figure 16**)	R_{TG}	4.2	5	5.8	kΩ	Temp = 25°C[3)] Mode: PDRH	34
Open loop resistance RING to V_{BATH} (see **Figure 16**)	R_{RB}	4.2	5	5.8	kΩ	Temp = 25°C[3)] Mode: PDRH	35
Power down open loop line voltage	$V_{TR,PD}$ = = – V_{BATH} – V_{DOH}	42	44	47	V	Mode: PDRH	36
Power down output leakage current	$I_{Leak,R}$	–10	–	10	µA	V_{BATH} < $V_{T/R}$ < 0	37
	$I_{Leak,T}$	–10	–	10	µA	Mode: PDH	38
High impedance output leakage current	$I_{Leak,R}$	–10	–	10	µA	V_{BATH} < V_R < V_{HR} Mode: HIR, HIRT	39
	$I_{Leak,T}$	–10	–	10	µA	V_{BATH} < V_T < V_{HR} Mode: HIT, HIRT	40
Inputs DCP, DCN, ACP, ACN, Output C_{EXT}							
Input current DCP, DCN	I_{DC}	–	0.1	–	µA	–	41
Differential AC input resistance ACP, ACN	R_{AC}	–	20	–	kΩ	–	42
Output resistance on C_{EXT}	–	–	100	–	kΩ	–	43
Current Outputs IT, IL							
IT output current	I_{IT}	–15	0	15	µA	I_R = I_T = 0 mA	44

Table 13 DC Characteristics (V_{ACP} = V_{ACN} = 1.5 V) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
IT output current normal polarity	I_{IT}	380	400	420	µA	I_R = I_T = 20 mA	45
IT output current reverse polarity[4]	I_{IT}	–420	–400	–380	µA	I_R = I_T = –20 mA	46
Transversal current ratio (see Figure 18)[5]	$1/G_{IT,DC}$	49.5	50	50.5	–	I_R = I_T = 20 mA, I_R = I_T = –20 mA	47
Off-hook output current on IT	–	800	950	1100	µA	TIP/RING shorted, Temp = 25 °C[6] Mode: PDRH	48
IL output current (see Figure 18)	I_{IL}	–20	0	20	µA	I_R = I_T = 20 mA	49
		30	50	70	µA	I_R = 15 mA, I_T = 25 mA	50
		–160	–125	–90	µA	I_R = 50mA, I_T = 25mA	51
Control Inputs C1, C2							
H-input voltage	V_{IH}	2.7	–	V_{DD} + 0.3	V	–	52
M-input voltage	V_{IM}	1.2	–	2.1	V	–	53
L-input voltage	V_{IL}	–0.3	–	0.6	V	–	54
Input pull down current	I_{in}	0	2	10	µA	–	55
Thermal overload current C1	I_{therm}	120	150	250	µA	V_{C1} = 1.20 V	56
Thermal overload threshold temperature	T_{jLIM}	–	165	–	°C	Mode: ACTx, HIx	57

1) The systematic temperature dependence is appr. + 7 mV / °C
2) The systematic temperature dependence is appr. -0.3 % / °C
3) The systematic temperature dependence is appr. +0.1 %/ °C
4) With **VDD = 3.3 V**, the IT output current **in reverse polarity** is limited to typically 700 µA; thus, the DC current regulation loop operates correctly only up to the corresponding line current value of 35 mA. In all other cases, IT is linear within the full line current range
5) The offset (I_R = I_T = 0 mA) has to be taken into account.
6) The systematic temperature dependence is appr. -0.1 %/ °C

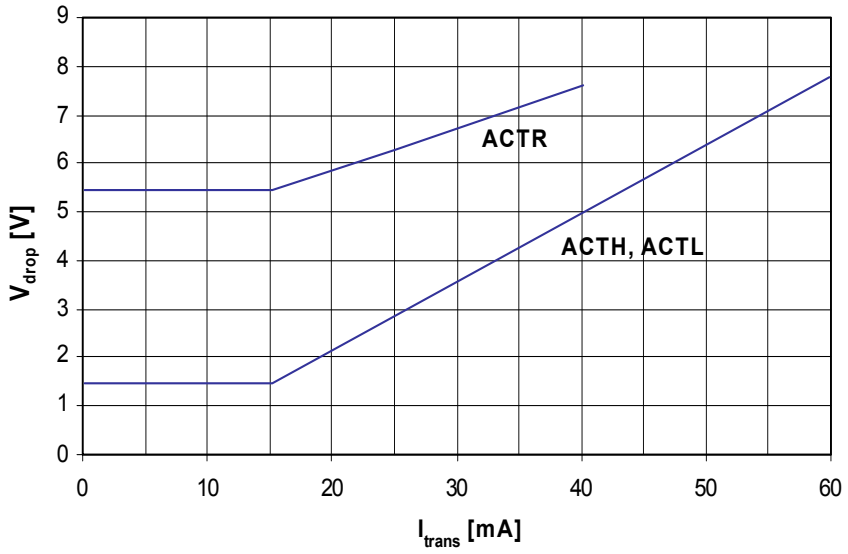


Figure 10 Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR

4.5.3 AC Characteristics

If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA and –25 mA, respectively; they are valid in all active modes.

Table 14 AC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Line Termination TIP, RING							
Receive gain (see **Figure 18**)	G_r	5.925	6.0	6.075	–	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz	58
Total harmonic distortion V_{TR} (see **Figure 18**)	THD	–	0.01	0.3	%	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz	59
Teletax distortion	$THDTTX$	–	0.1	1	%	$V_{TR,AC}$ = 5 V_{rms}, f = 16 kHz, R_L = 200 Ω	60
		–	0.2	3	%	$V_{TR,AC}$ = 5 V_{rms}, f = 16 kHz, R_L = 200 Ω, $I_{Trans,DC}$ = 0 mA	61
Psophometric noise (see **Figure 18**)	N_{pVTR}	–	–82	–76	dBmp	–	62
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (see **Figure 19**)	$LTRR$	–	80	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 3.4 kHz	63
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop) PEF 4264, PEF 4364 (see **Figure 19**)	$LTRR_{loop}$	54 52	58 56	– –	dB dB	V_{long} = 3 V_{rms} 300 Hz < f < 1 kHz f = 3.4 kHz	64 65

Table 14 AC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop) PEF 4264-2 (see **Figure 19**)	$LTRR\text{-}2_{loop}$					V_{long} = 3 V_{rms}	
		61	65	–	dB	300 Hz < f < 1 kHz	66
		56	60	–	dB	f = 3.4 kHz	67
Transversal to longitudinal rejection ratio V_{TR}/V_{long}(see **Figure 21**)	$TLRR$	48	60	–	dB	$V_{ACP} - V_{ACN}$ = 1920 mV_{rms}, 300 Hz < f < 3.4 kHz	68
Power supply rejection ratio (see **Figure 11**, **Figure 12**, **Figure 14**, **Figure 14**)	$PSRR$					$V_{SupplyAC}$ = 100 mV_p, 300 Hz < f < 3.4 kHz	
V_{BATL}/V_{TR}		40	60	–	dB		69
V_{BATH}/V_{TR}		40	60	–	dB		70
V_{HR}/V_{TR}		33	50	–	dB		71
V_{DD}/V_{TR}		33	50	–	dB		72
Interchannel crosstalk[1]			-80		dB	300 Hz < f < 3.4 kHz both channels active	73
			-80		dB	One channel active, one channel power down	74
Ringing amplitude TIP/RING	V_{RNG0}	–	65	–	Vrms	$V_{DCP} - V_{DCN}$ = 0.15 V (DC) + 1.42 V_{rms} (sine wave, 20 Hz) R_R = 450 Ω, C_R = 3.4 µF, Mode: ACTR	75
Ringing distortion (see **Figure 22**)	RD	–	0.1	2	%		76
Transversal Current IT[2]							
Transversal current ratio (see **Figure 18**)	$1/G_{it}$					$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz	
		49.5	50	50.5		$I_{Trans,DC}$ = 25 mA	77
		49	50	51		$I_{Trans,DC}$ = –25 mA	78
Total harmonic distortion V_{IT}	THD_{IT}	–	0.02	0.3	%	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz	79
Psophometric noise (see **Figure 18**)	N_{pVIT}	–	–110	–105	dBmp	–	80
Longitudinal to transversal current output rejection ratio V_{long}/V_{IT} (see **Figure 19**)	$LITRR$	–	85	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 3.4 kHz	81
Power supply rejection ratio	$PSRR$					$V_{SupplyAC}$ = 100 mV_p, 300 Hz < f < 3.4 kHz	
V_{BATL}/V_{IT}		50	70	–	dB		82
V_{BATH}/V_{IT}		50	70	–	dB		83
V_{HR}/V_{IT}		50	70	–	dB		84
V_{DD}/V_{IT}		50	70	–	dB		85

1) Dual channel version PEF 4364 only

2) Unless otherwise specified, characteristics are valid for both DC line current directions (normal and reverse polarity)

4.5.3.1 Frequency Dependence of PSRR

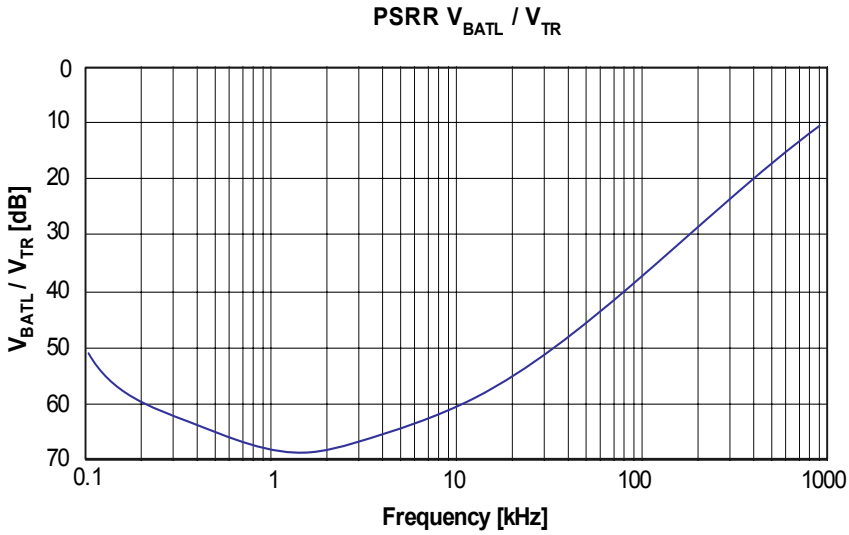


Figure 11 Typical Frequency Dependence of PSRR V_{BATL}/V_{TR}

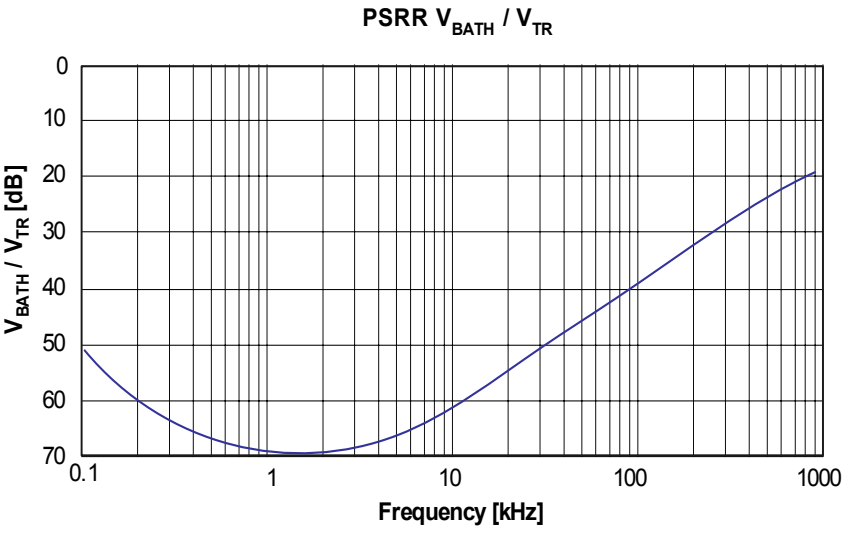


Figure 12 Typical Frequency Dependence of PSRR V_{BATH}/V_{TR}

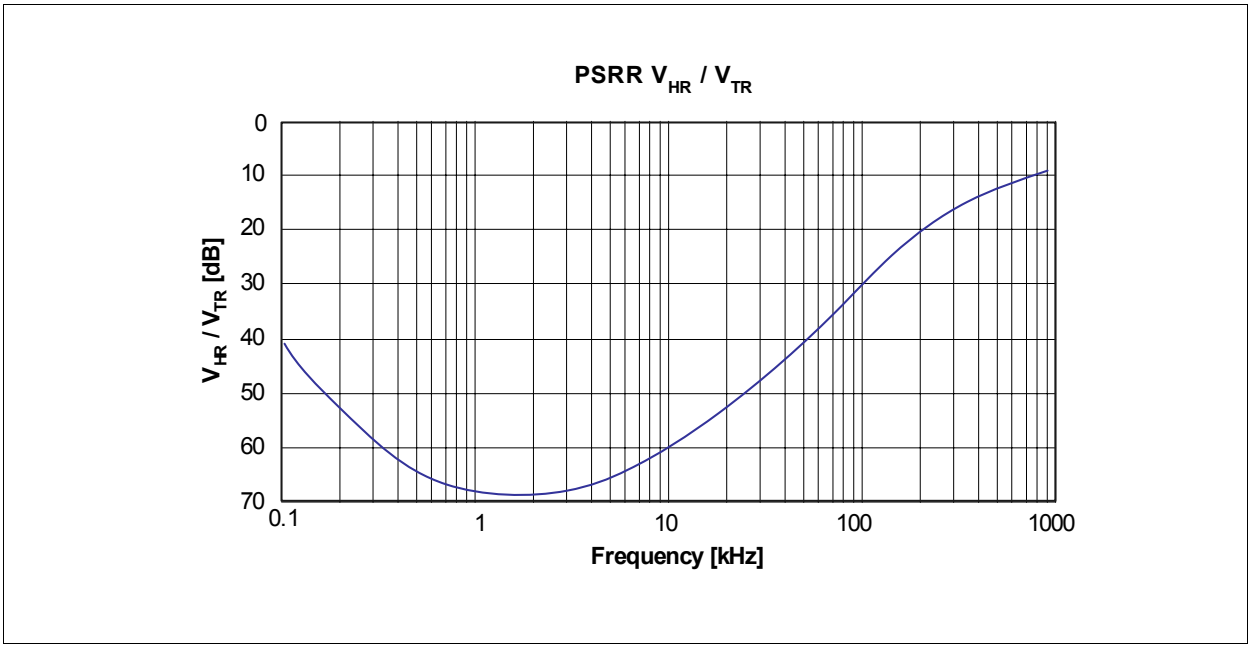


Figure 13 Typical Frequency Dependence of PSRR V_{HR}/V_{TR}

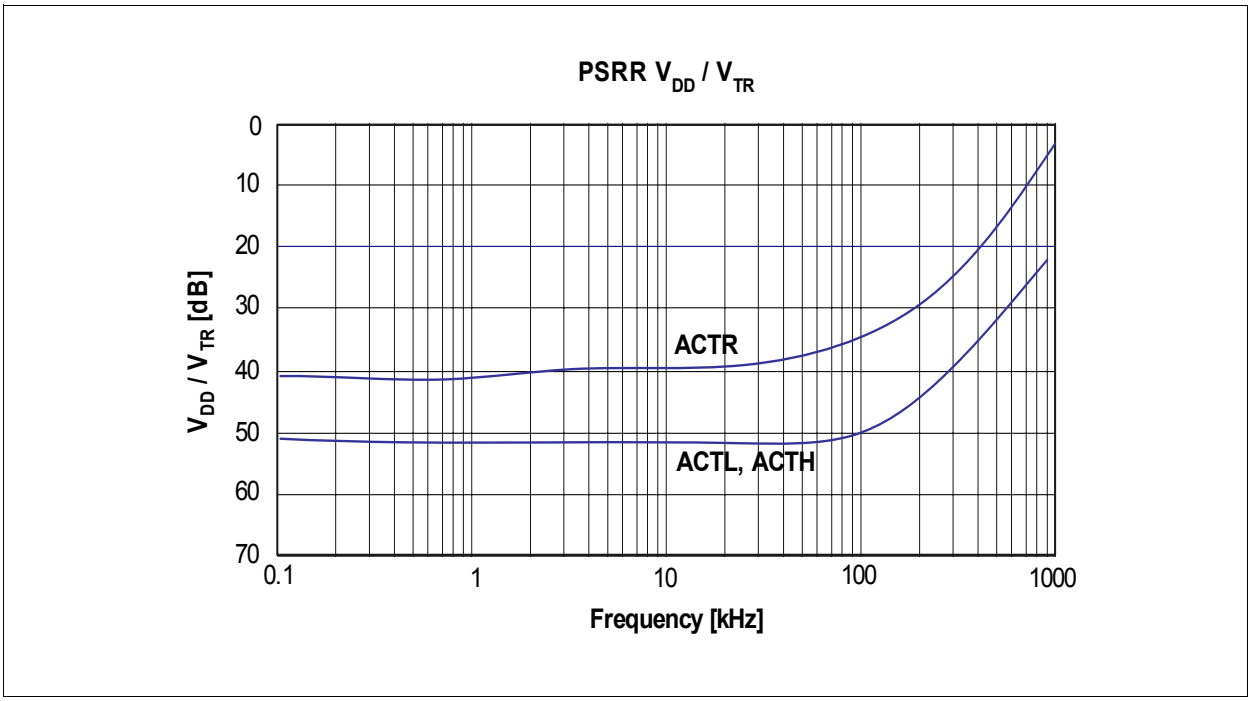


Figure 14 Typical Frequency Dependence of PSRR V_{DD}/V_{TR}

5 Test Figures

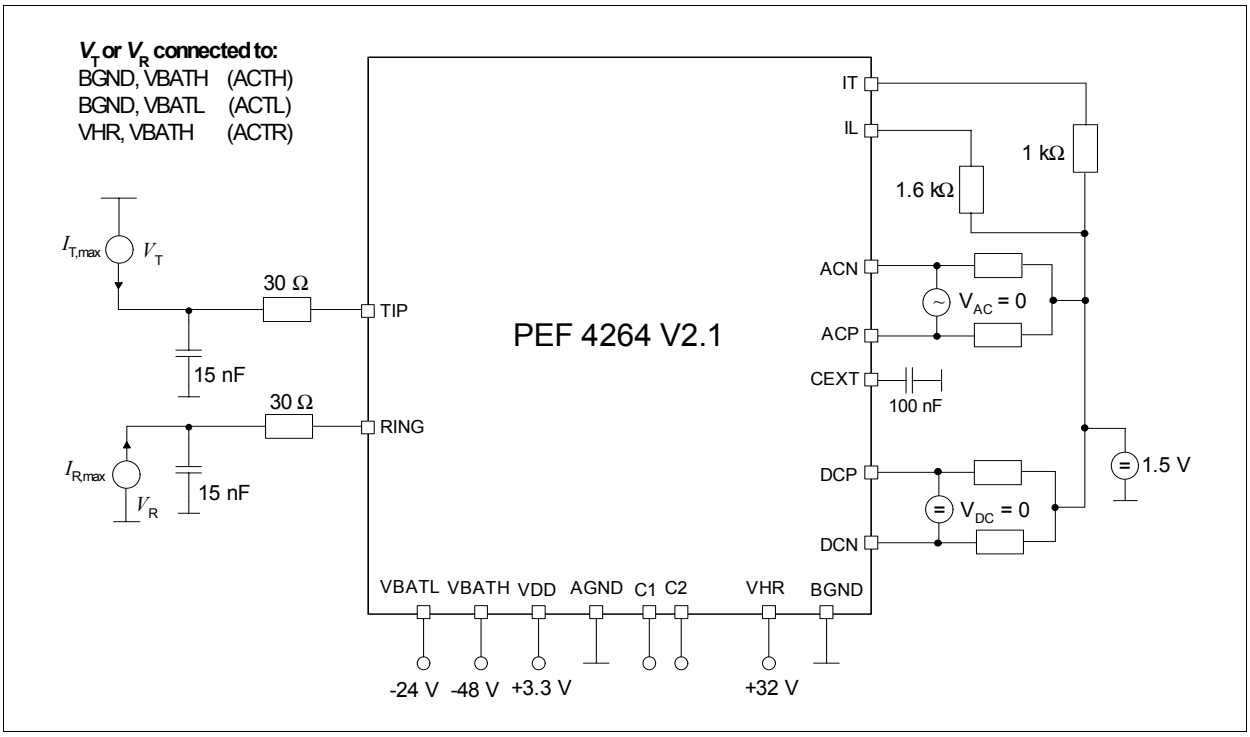


Figure 15 Output Current Limit

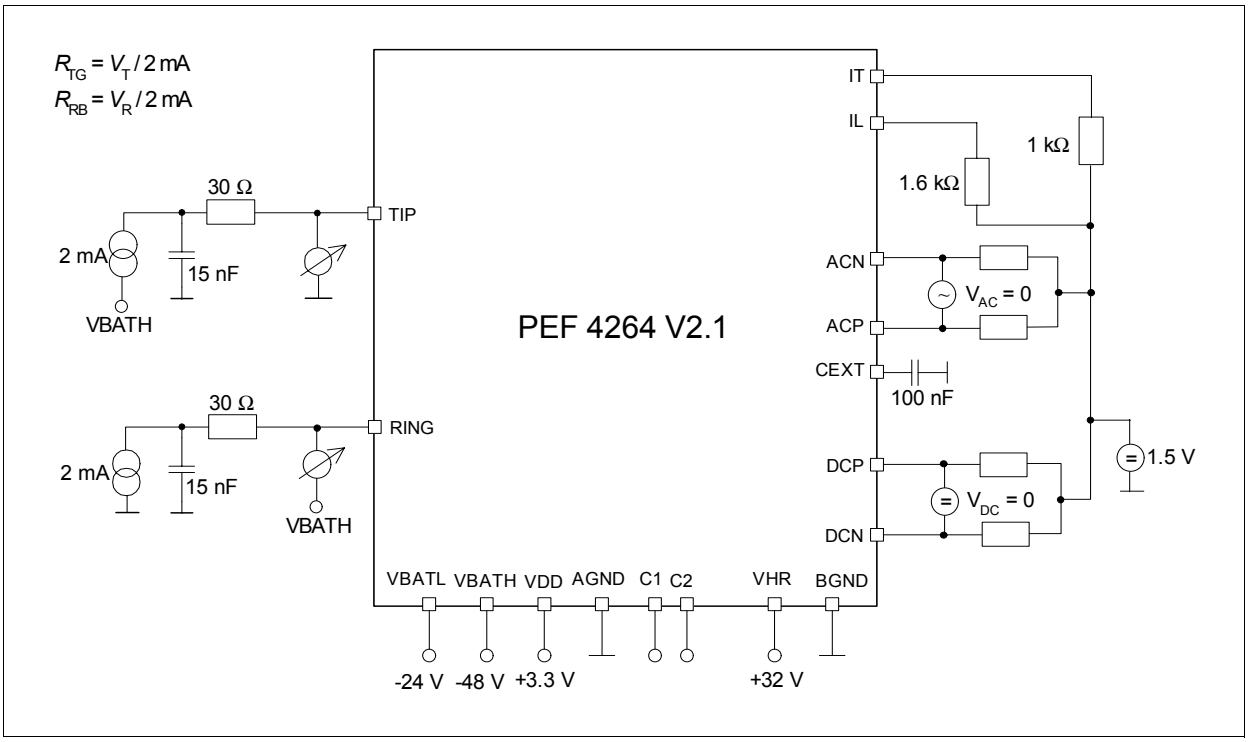


Figure 16 Output Resistance PDRH, PDRHL

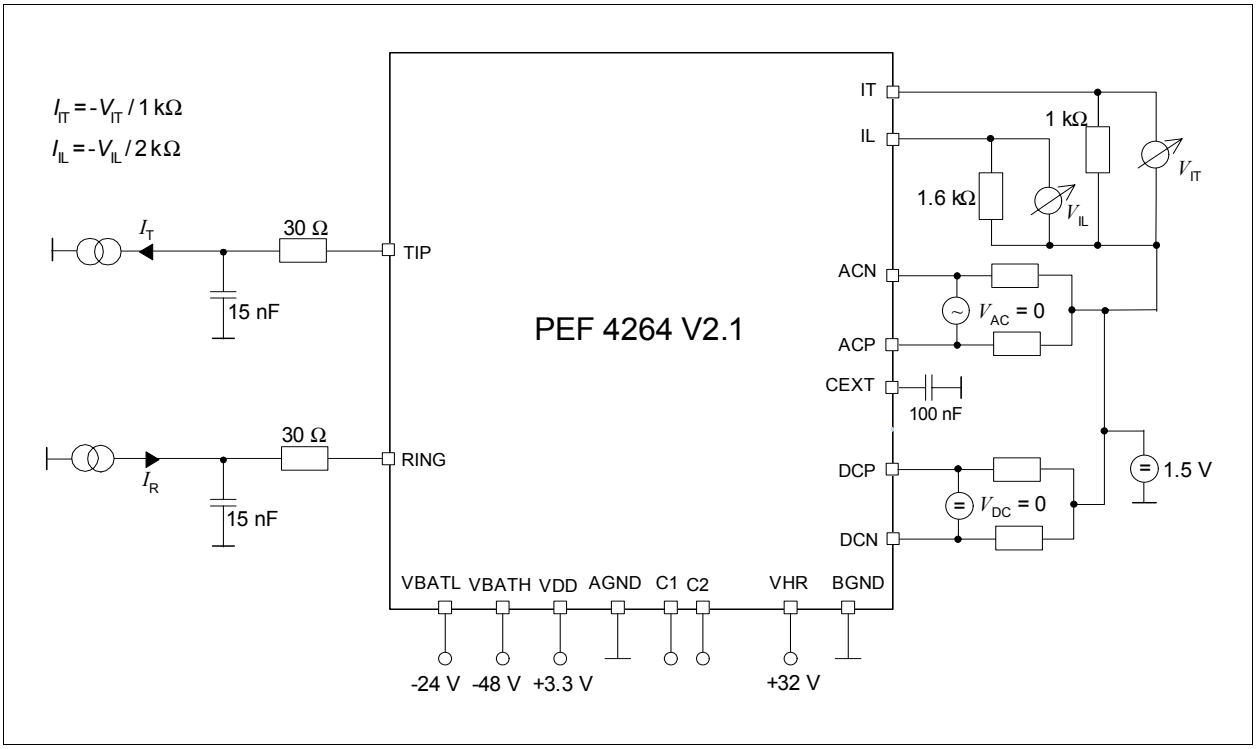


Figure 17 Current Outputs IT, IL

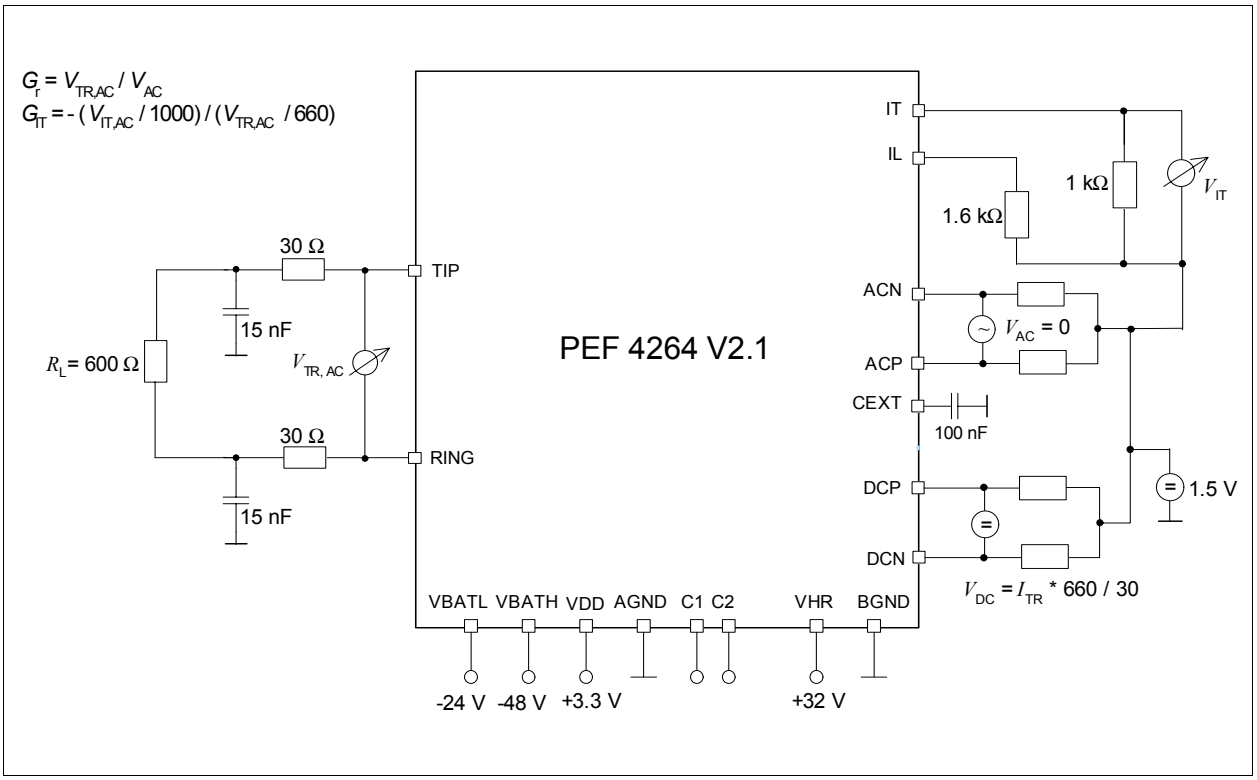


Figure 18 Transmission Characteristics

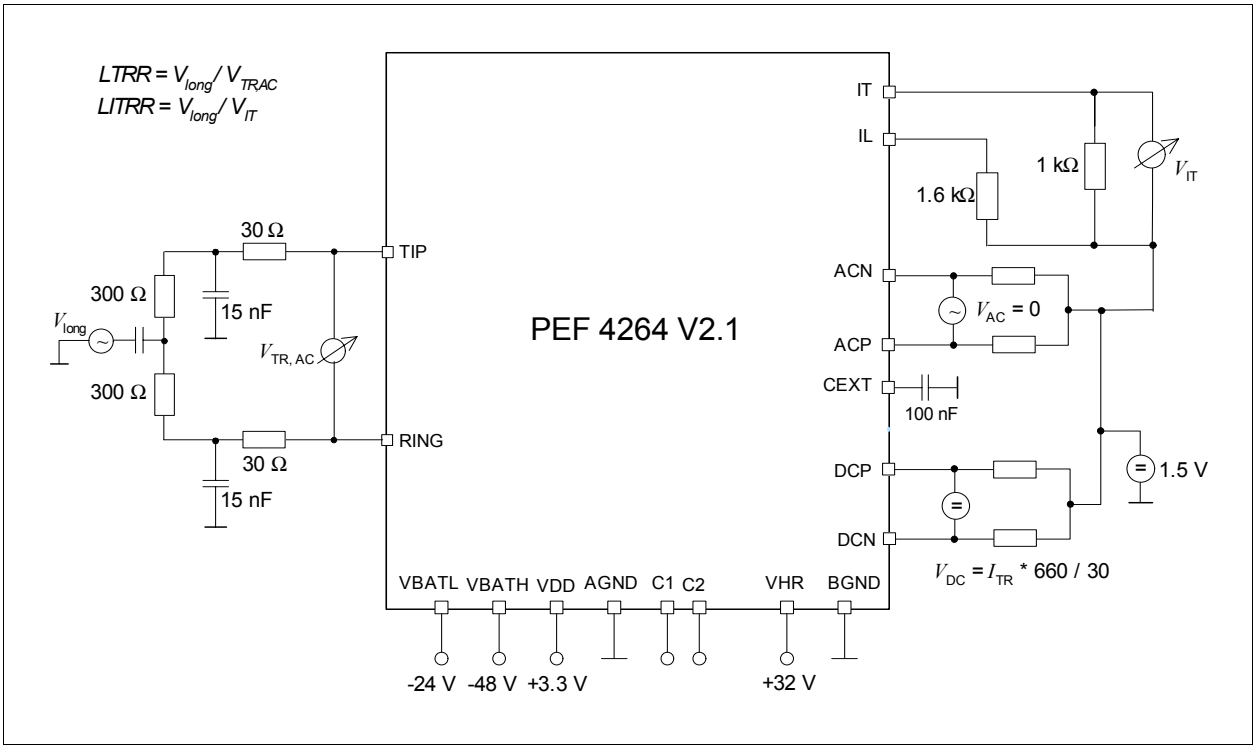


Figure 19 Longitudinal to Transversal Rejection

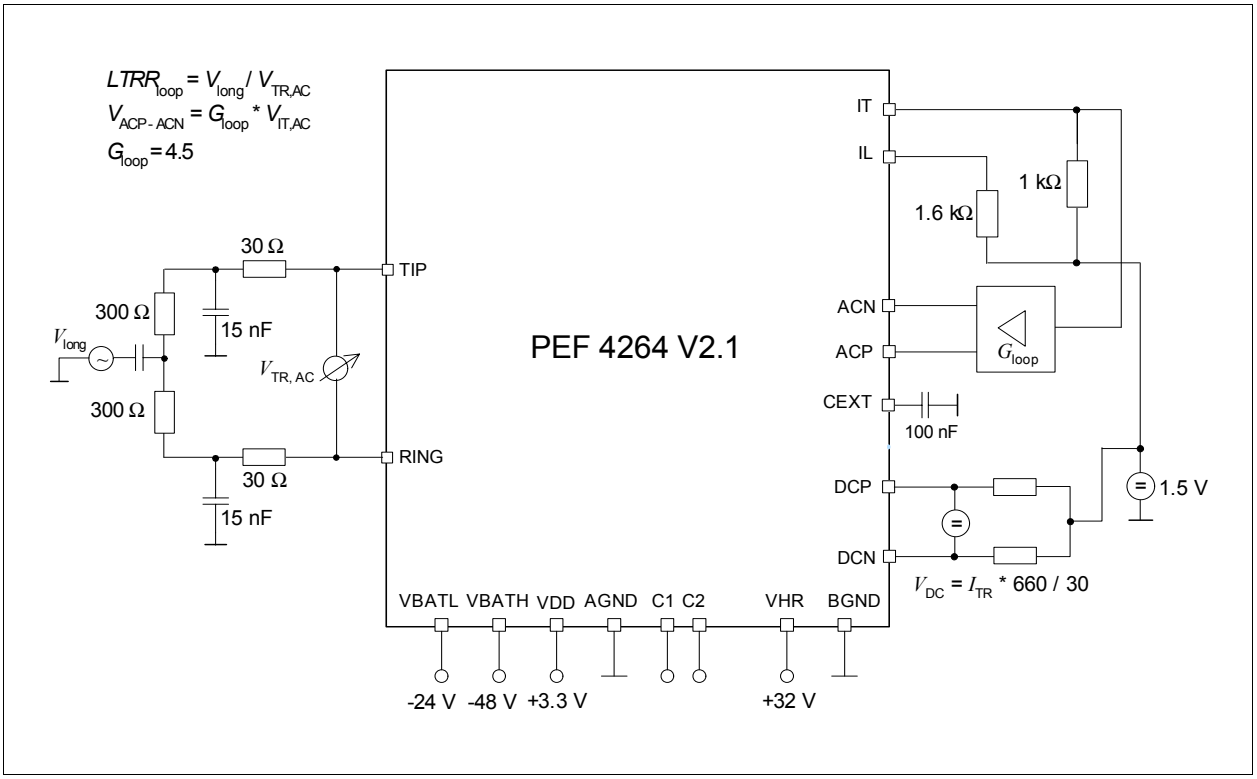


Figure 20 Longitudinal to Transversal Rejection Loop

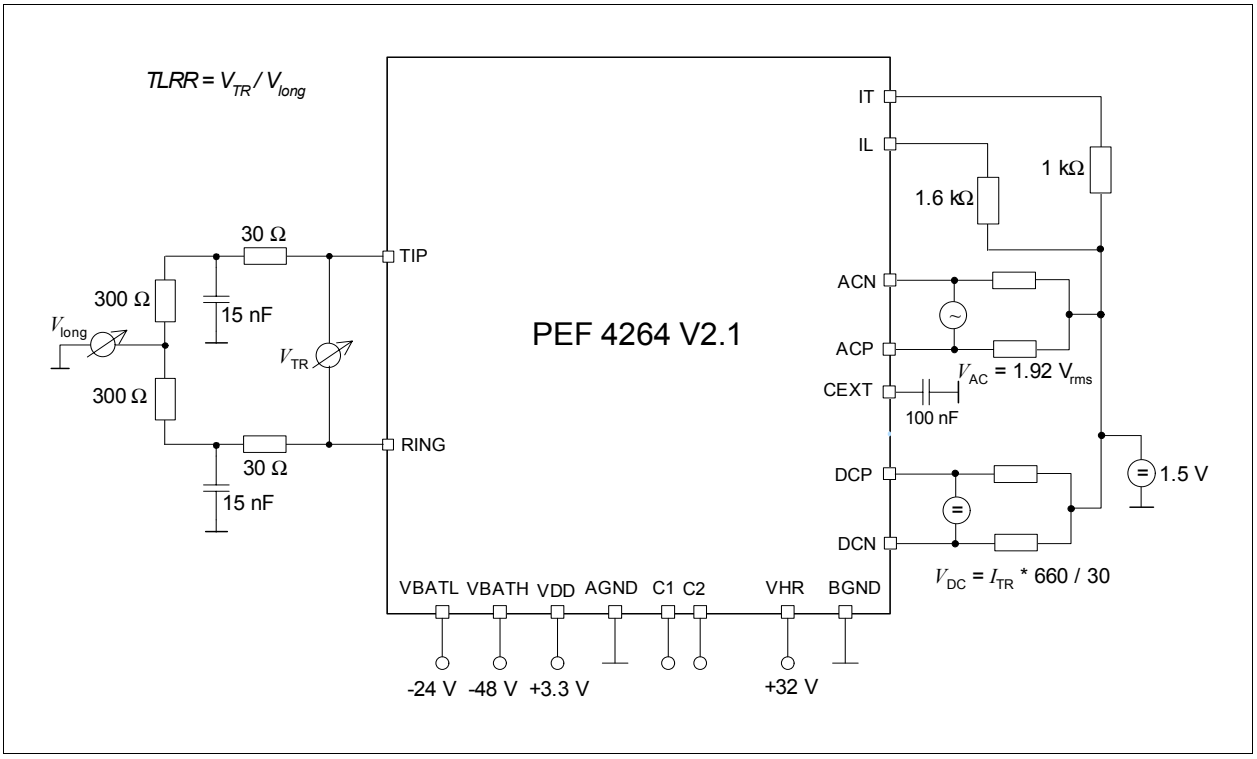


Figure 21 Transversal to Longitudinal Rejection

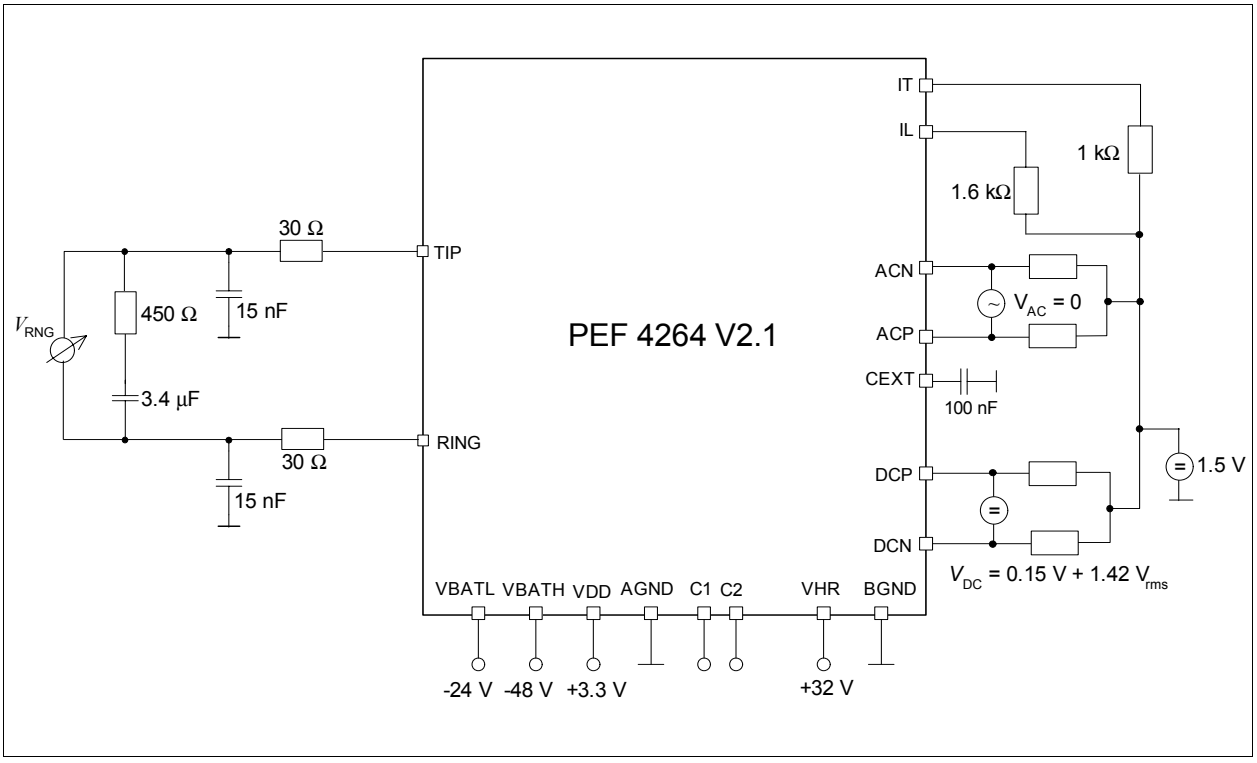


Figure 22 Ring Amplitude

6 Package Outlines

6.1 PG-DSO-20-24 Package

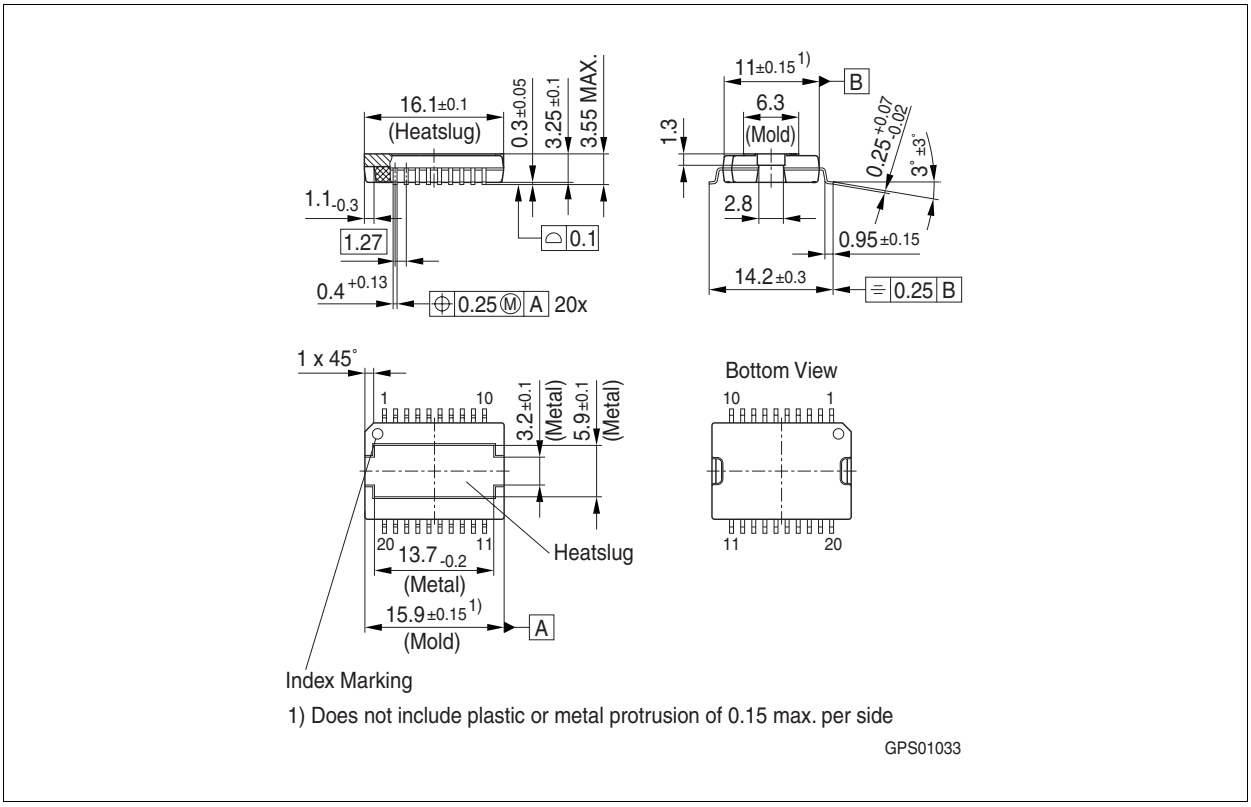


Figure 23 Package Outline for PG-DSO-20-24 (Plastic Green Dual Small Outline)

Notes

1. *Heatsink on top - pin counting clockwise (top view)*
2. *Dimensions in mm*

Attention: The heatsink is connected to VBATH via the chip substrate. Due to the high voltage of up to 125 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.

6.2 PG-VQFN-48-15 Package

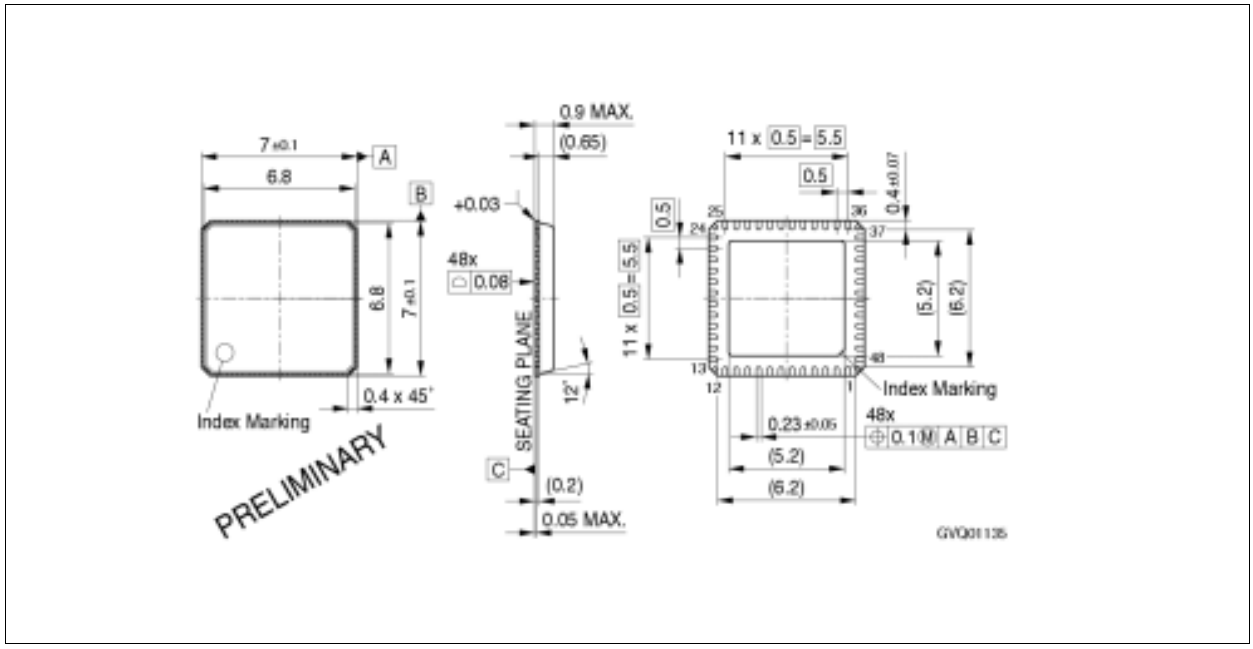


Figure 24 Package Outline for PG-VQFN-48-15 (Plastic Green Very thin Profile Quad Flatpack No-lead)

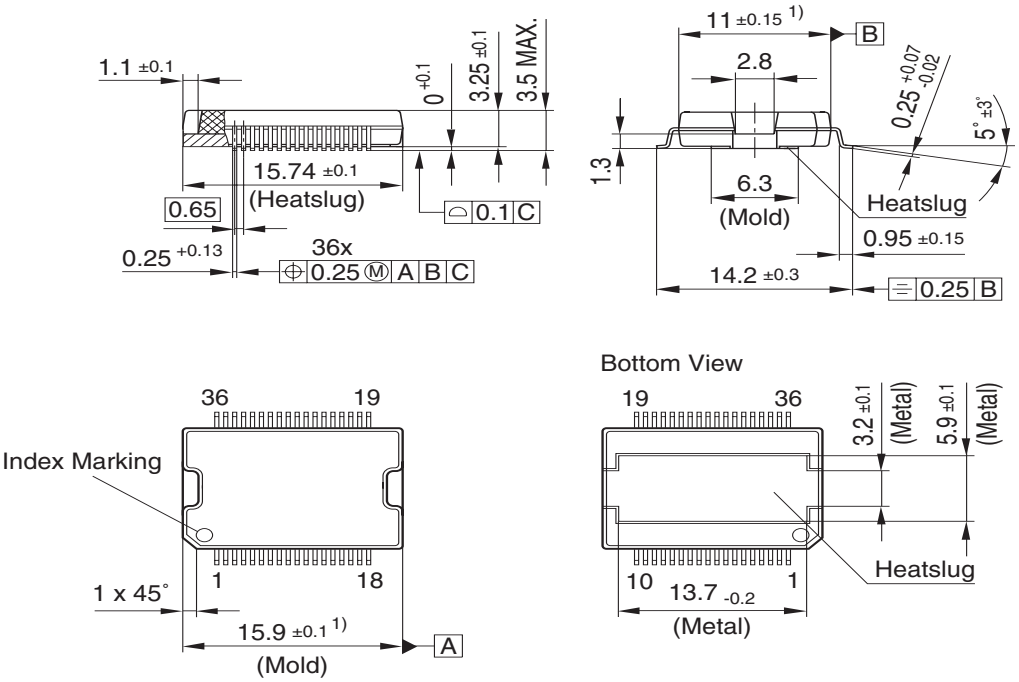
Note: Dimensions in mm

Attention: The exposed die pad and the die pad edges are connected to VBATH via the chip substrate. Due to the high voltage of up to 125 V between VHR and VBATH, touching of the die pad or any attached conducting part can be hazardous.

6.2.1 Recommended PCB Foot Print Pattern for PG-VQFN-48-15 Package

For detailed information on PCB related thermal and soldering issues of the PG-VQFN-48-15 package see **[4]**, chapter 3 and 4.

6.3 PG-DSO-36-15 Package



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 25 Package Outline for PG-DSO-36-15 (Plastic Green Dual Small Outline)

Notes

1. *Heatslug down version - pin counting counterclockwise (top view)*
2. *Dimensions in mm*

Attention: The heatslug is connected to VBATH via the chip substrate. Due to the high voltage of up to 125 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.

6.3.1 Recommended PCB Foot Print Pattern for PG-DSO-36-15 Package

The heatslug is soldered to the PCB according to **Figure 25**. For improved thermal behaviour the utilization of another PCB metal layer as an additional cooling area is recommended. These copper areas should be both electrically separated from each other and floating, i. e. they must not be connected with any other metallic part on the PCB.

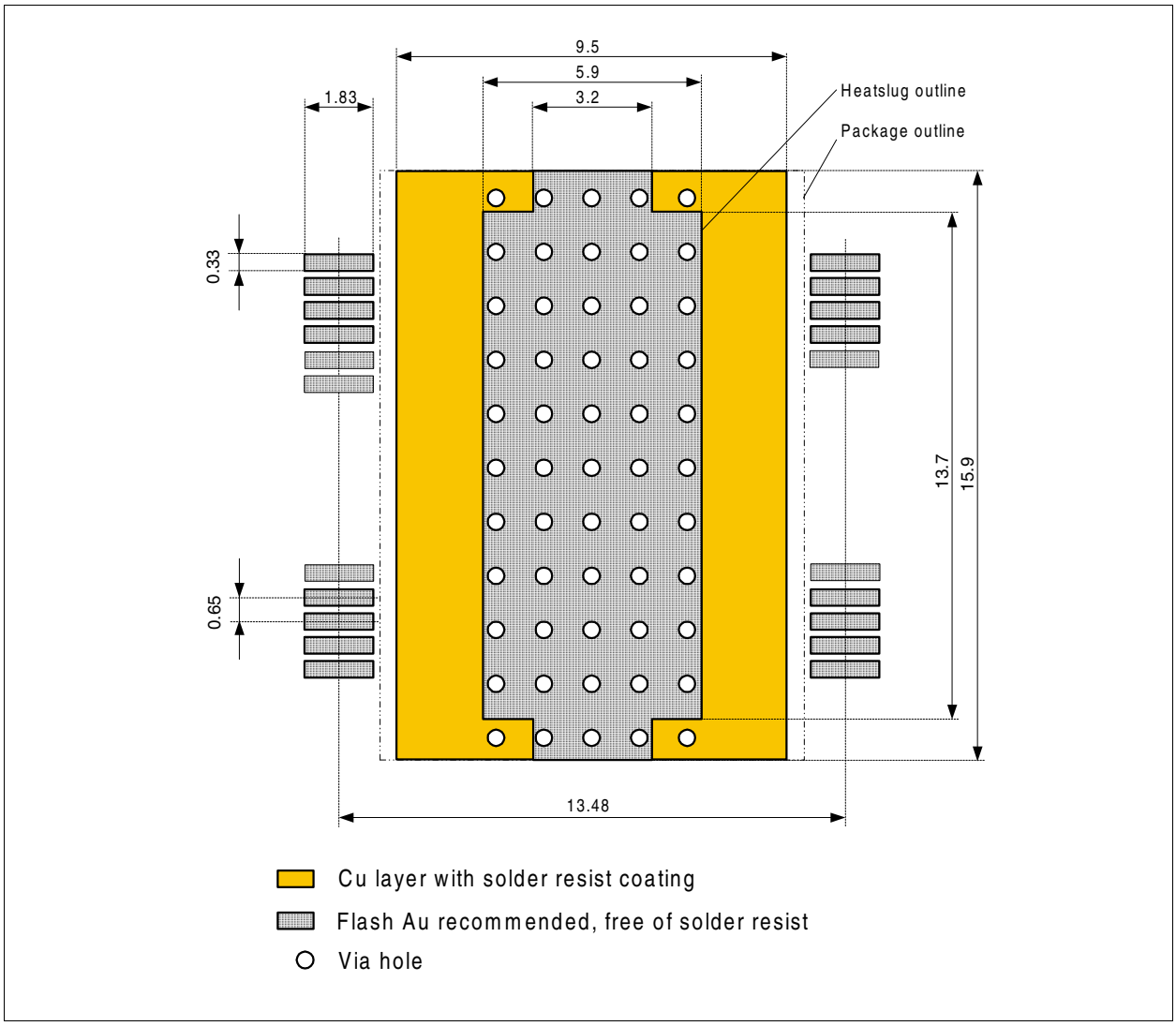


Figure 26 Footprint for PG-DSO-36-15

References

[1] SLIC-S/-S2 / TSLIC-S (PEF 4264/-2 / PEF 4364) Application Note “Protection for SLIC-S/-S2 against Overvoltages and Overcurrents according to ITU-T K. 20/K.21/K.45” Rev. 1.0, 2003-07-18

[2] VINETIC® Version 1.4 Prel. Application Note External Components Rev. 2.0, 2005-09-06

[3] VINETIC® Version 2.1/2.2 Preliminary Hardware Design Guide Rev. 2.0, 2005-05-19

[4] Recommendations for Printed Circuit Board Assembly of Infineon P(G)-VQFN Packages, Application Support, DS3, 2006-03-03

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