FINAL

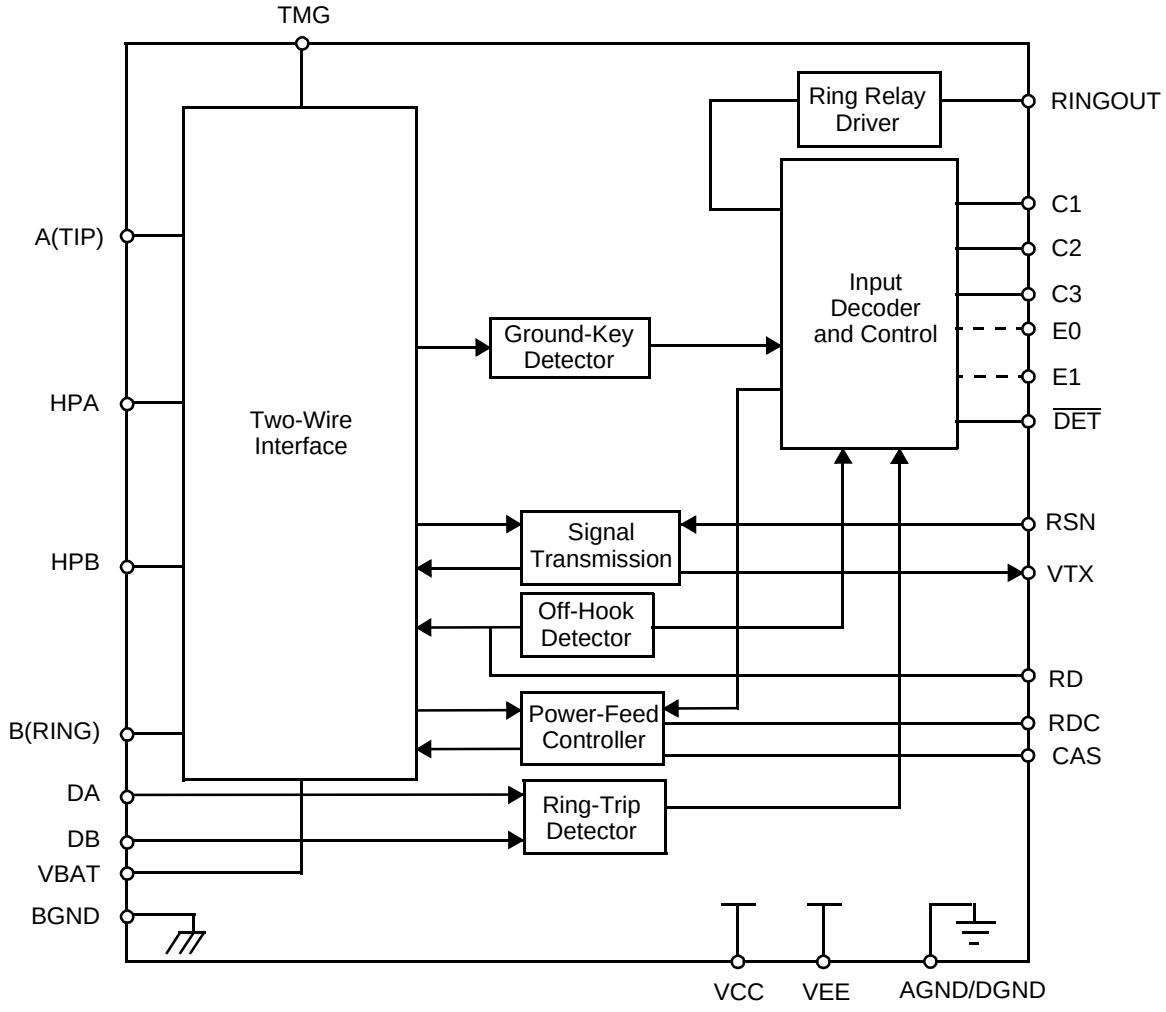
# Am7943

## Subscriber Line Interface Circuit

## DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Current gain = 200
- Programmable loop-detect threshold
- Low power Standby state
- Performs polarity reversal
- Ground-key detector
- Tip Open state for ground-start lines
- –19 V to –58 V battery operation
- Two-wire impedance set by single external impedance
- On-hook transmission
- On-chip ring relay driver and relay snubber circuit
- On-chip Thermal Management (TMG) feature
- Ideal for DLC and PABX applications

## BLOCK DIAGRAM

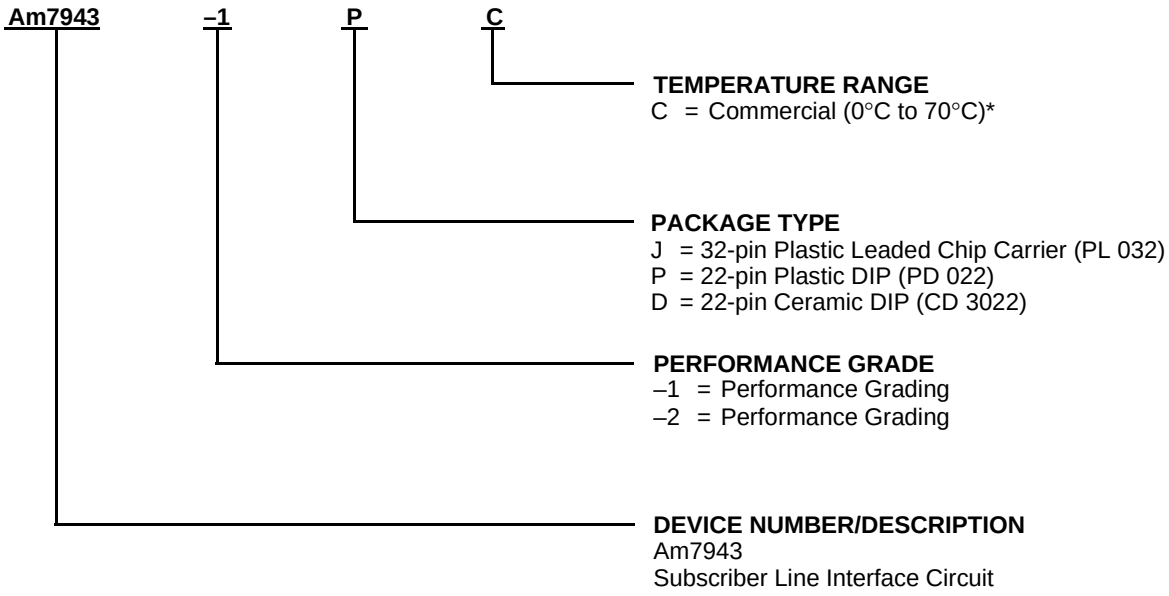



Publication# **18406** Rev: **C** Amendment: **/0**
Issue Date: **July 1998**

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.




| Valid Combinations | | |
|---|---|---|
| Am7943 | –1<br>–2 | DC<br>JC<br>PC |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

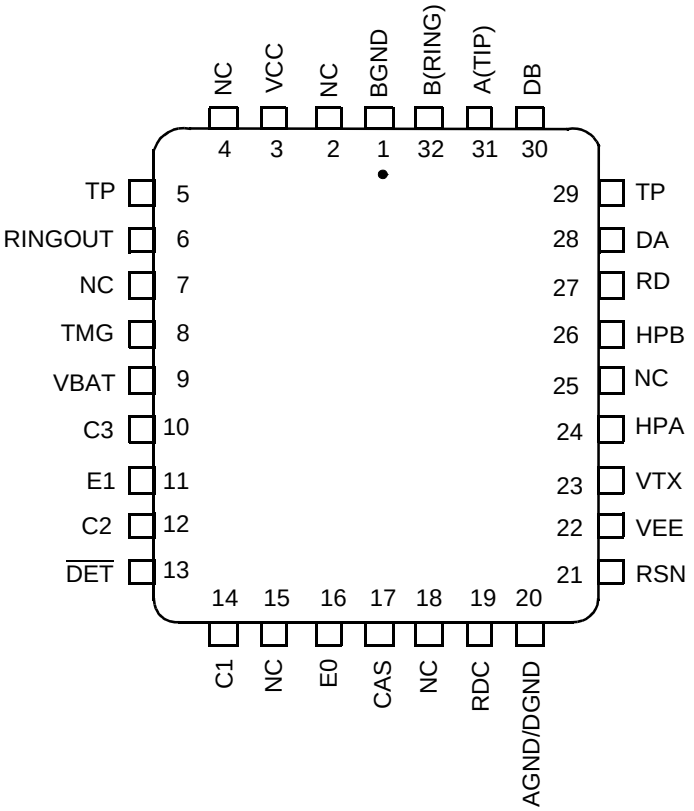
***Note:***

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

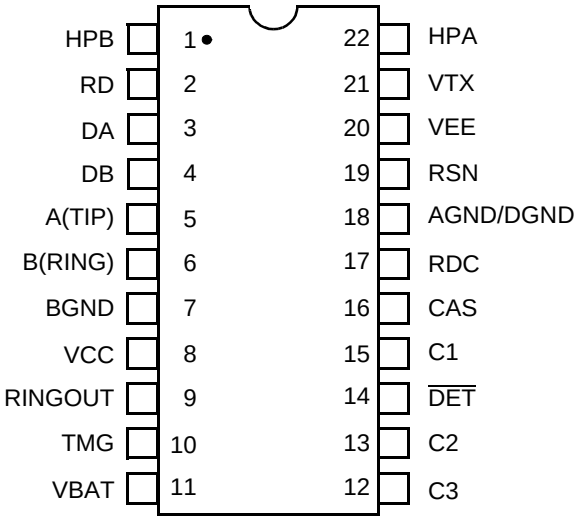
## CONNECTION DIAGRAMS

### Top View

**32-Pin PLCC**




**22-Pin Plastic DIP**
**or**
**22-Pin Ceramic DIP**




***Notes:***

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*
3. *NC = No Connect*

## PIN DESCRIPTIONS

| Pin Names | Type | Description |
|---|---|---|
| AGND/DGND | Gnd | Analog and Digital ground. |
| A(TIP) | Output | Output of A(TIP) power amplifier. |
| BGND | Gnd | Battery (power) ground. |
| B(RING) | Output | Output of B(RING) power amplifier. |
| C3–C1 | Input | Decoder. TTL compatible. C3 is MSB and C1 is LSB. |
| CAS | Capacitor | Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region. |
| DA | Input | Ring-trip negative. Negative input to ring-trip comparator. |
| DB | Input | Ring-trip positive. Positive input to ring-trip comparator. |
| $\overline{\text{DET}}$ | Output | Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1–E0). The output is open-collector with a built-in 15 kΩ pull-up resistor. |
| E0 | Input | $\overline{\text{DET}}$ Enable. A logic High enables $\overline{\text{DET}}$. A logic Low disables $\overline{\text{DET}}$. ($\overline{\text{DET}}$ = Logic High). (PLCC only) |
| E1 | Input | Ground-Key Enable. E1 = High connects the ground-key detector to $\overline{\text{DET}}$. E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$. (PLCC only) |
| HPA | Capacitor | High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor. |
| HPB | Capacitor | High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor. |
| RD | Resistor | Detector resistor. Detector threshold set and filter pin. |
| RDC | Resistor | DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of $V_{RDC}$ is negative for normal polarity and positive for reverse polarity. |
| RINGOUT | Output | Ring Relay Driver. Open-collector driver with emitter internally connected to BGND. |
| RSN | Input | Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. |
| TMG | — | Thermal management. A resistor connected from this pin to VBAT reduces the on-chip power dissipation in the normal polarity, Active state only. Refer to Table 2. |
| TP | Thermal | Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation |
| VBAT | Battery | Battery supply. |
| VCC | Power | +5 V power supply. |
| VEE | Power | –5 V power supply. |
| VTX | Output | Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network. |

## ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

$V_{CC}$ with respect to AGND/DGND . . .–0.4 V to +7.0 V

$V_{EE}$ with respect to AGND/DGND . . .+0.4 V to –7.0 V

$V_{BAT}$ with respect to AGND/DGND:
- Continuous . . . . . +0.4 V to –70 V
- 10 ms . . . . . +0.4 V to –75 V

BGND with respect to AGND/DGND . . . .+3 V to –3 V

A(TIP) or B(RING) to BGND:
- Continuous . . . . . .–70 V to +1 V
- 10 ms (f = 0.1 Hz) . . . . . .–70 V to +5 V
- 1 ms (f = 0.1 Hz) . . . . . .–80 V to +8 V
- 10 µs (f = 0.1 Hz) . . . . . .–90 V to +12 V

Current from A(TIP) or B(RING). . . . . .±150 mA

Current from TMG . . . . . 100 mA

Voltage on RINGOUT:
- During transient . . . . . BGND to +10 V
- During steady state. . . . . BGND to +7 V

Current through relay drivers . . . . . 60 mA

DA and DB inputs
- Voltage on ring-trip inputs . . . . . .$V_{BAT}$ to 0 V
- Current into ring-trip inputs . . . . . .±10 mA

C3–C1, E0, E1
- to AGND/DGND . . . . . .–0.4 V to $V_{CC}$ +0.4 V

Maximum power dissipation, $T_A$ = 85°C

No heat sink (see note):
- In 22-pin ceramic DIP package. . . . . 1.2 W
- In 22-pin plastic DIP package . . . . . 1.0 W
- In 32-pin PLCC package. . . . . 1.4 W

Thermal data . . . . . .$\theta_{JA}$
- In 22-pin ceramic package . . . . . .50°C/W typ
- In 22-pin plastic package . . . . . .56°C/W typ
- In 32-pin PLCC package. . . . . .43°C/W typ

***Note:*** *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

$V_{CC}$ . . . . . 4.75 V to 5.25 V

$V_{EE}$ . . . . . –4.75 V to –5.25 V

$V_{BAT}$ . . . . . .–19 V to –56.5 V

AGND/DGND . . . . . 0 V

BGND with respect to
- AGND/DGND. . . . . –100 mV to +100 mV

Load resistance on VTX to ground . . . . . 10 kΩ min

*Operating Ranges define those limits between which device functionality is guaranteed.*

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

## ELECTRICAL CHARACTERISTICS

| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Analog ($V_{TX}$) output impedance | | | 3 | | Ω | |
| Analog ($V_{TX}$) output offset | <br>–40°C to +85°C | –35<br>–40 | | +35<br>+40 | mV | —<br>4 |
| Analog (RSN) input impedance | 300 Hz to 3.4 kHz | | 1 | 20 | Ω | 4 |
| Longitudinal impedance at A or B | | | | 35 | | |
| Overload level | 4-wire and 2-wire Active state | –2.5 | | +2.5 | Vpk | 2a |
| | On-hook, $R_{LAC}$ = 900 Ω, Active or OHT state | 0.95 | | | Vrms | 2b |
| **Transmission Performance** | | | | | | |
| 2-wire return loss (See Test Circuit D) | 200 to 3400 Hz | 26 | | | dB | 4, 8 |
| **Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); $R_L$ = 740 Ω at $V_{BAT}$ = 48 V** | | | | | | |
| Longitudinal to metallic L-T, L-4 | 200 Hz to 1 kHz –1*<br>normal polarity 0°C to +70°C –2<br>normal polarity –40°C to +85°C –2<br>reverse polarity –2 | 52<br>63<br>58<br>58 | | | dB | —<br>—<br>4<br>— |
| | 1 kHz to 3.4 kHz –1*<br>normal polarity 0°C to +70°C –2<br>normal polarity –40°C to +85°C –2<br>reverse polarity –2 | 52<br>58<br>54<br>54 | | | dB | —<br>—<br>4<br>— |
| Longitudinal signal generation 4-L | 300 Hz to 800 Hz normal polarity | 42 | | | | |
| Longitudinal current per pin | Active state and OHT state | 27 | 35 | | mArms | |
| **Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B) BAT = –48 V, $R_L$ = 900 Ω** | | | | | | |
| Gain accuracy | 0 dBm, 1 kHz<br>0°C to +70°C<br>–40°C to +85°C | <br>–0.15<br>–0.20 | | <br>+0.15<br>+0.20 | dB | —<br>—<br>4 |
| Gain accuracy, OHT state | –10 dBm, on-hook, $R_{LAC}$ = 900 Ω | –0.5 | | +0.5 | dB | 4 |
| Variation with frequency | 300 to 3400 Hz<br>relative to 1 kHz 0°C to +70°C<br>–40°C to +85°C | <br>–0.10<br>–0.15 | | <br>+0.10<br>+0.15 | dB | —<br>—<br>4 |
| Gain tracking | +7 dBm to –55 dBm<br>Reference: 0 dBm | –0.1 | | +0.1 | dB | 4<br>— |
| **Balance Return Signal (4- to 4-Wire, See Test Circuit B) BAT = –48 V, $R_L$ = 900 Ω** | | | | | | |
| Gain accuracy | 0 dBm, 1 kHz<br>0°C to +70°C<br>–40°C to +85°C | <br>–0.15<br>–0.20 | | <br>+0.15<br>+0.20 | dB | —<br>3<br>4 |
| Variation with frequency | 300 to 3400 Hz<br>relative to 1 kHz 0°C to +70°C<br>–40°C to +85°C | <br>–0.1<br>–0.15 | | <br>+0.1<br>+0.15 | dB | —<br>3<br>4 |
| Gain tracking | +3 dBm to –55 dBm<br>Reference: 0 dBm<br>0°C to +70°C<br>–40°C to +85°C | <br><br>–0.1<br>–0.15 | | <br><br>+0.1<br>+0.15 | dB | —<br>—<br>3, 4<br>4 |
| Group delay | f = 1 kHz | | 4 | | µs | 4, 8 |

***Note:***
** P.G. = Performance Grade*

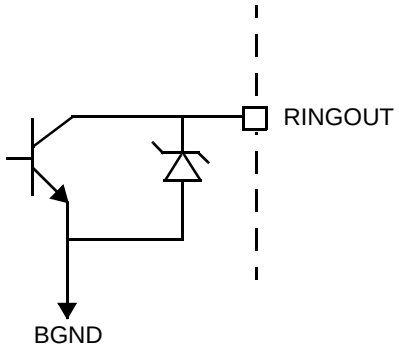
## ELECTRICAL CHARACTERISTICS (continued)

| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| **Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire) (See Test Circuits A and B)**<br>**BAT = –48 V, $R_L$ = 900 Ω** | | | | | | |
| Harmonic distortion<br>300 Hz to 3400 Hz | 2-wire level = 0 dBm<br>2-wire level = +7 dBm | | –64<br>–55 | –50<br>–40 | dB | |
| **Idle Channel Noise (2-wire and 4-wire)** | | | | | | |
| C-message weighted noise | 0°C to +85°C<br>–40°C to 0°C | | +7<br>+7 | +10<br>+12 | dBrnC | —<br>4 |
| Psophometric weighted noise | 0°C to +85°C<br>–40°C to 0°C | | –83 | –80<br>–78 | dBmp | —<br>4 |
| **Line Characteristics, Active State (See Figure 1)** | | | | | | |
| Short loops, Active state | BAT = –43 V, $R_{LDC}$ = 600 Ω<br>BAT = –48 V, $R_{LDC}$ = 600 Ω | 25.0 | 27.0 | 29.0 | | |
| Long loops, Active state | BAT = –43 V, $R_{LDC}$ = 1.4 kΩ<br>BAT = –48 V, $R_{LDC}$ = 1.9 kΩ | 20.0<br>18.0 | 23.8<br>20.4 | | | |
| OHT state | BAT = –48 V, $R_{LDC}$ = 600 Ω | 16.0 | 18.0 | 20.0 | mA | |
| Standby state | $I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 1800}$ $T_A$ = 25°C | 0.7$I_L$ | $I_L$ | 1.3$I_L$ | | |
| | $R_L$ = 600 Ω, BAT = –48 V<br>$T_A$ = 70°C | 15.0 | 17.4 | | | |
| Loop current | Tip Open, $R_L$ = 0<br>Disconnect, $R_L$ = 0<br>Tip Open, Bwire to GND<br>Tip Open, Bwire = $V_{BAT}$ + 6 V | | —<br>—<br>30<br>30 | 100<br>100<br>—<br>— | µA<br>µA<br>mA<br>mA | |
| $I_L$LIM (Itip + Iring) | Tip and ring shorted to GND | | 100 | 130 | mA | |
| Ground-start signaling (tip voltage) | Active state<br>$R_{TIP}$ to –48 V = 7.0 kΩ<br>$R_{RING}$ to GND = 100 Ω | –7.5 | –5.0 | | V | 4<br>—<br>— |
| Open circuit voltage | Active and OHT<br>BAT = –48 V | 40.5 | 42.0 | | | |
| **Power Dissipation, Normal Loop Polarity, BAT = –48 V** | | | | | | |
| On hook, Open Circuit state | | | 25 | 70 | | |
| On hook, OHT state | | | 120 | 210 | | |
| On hook, Active state | $R_{TMG}$ = Open<br>$R_{TMG}$ = 1700 Ω | | 160<br>195 | 260<br>280 | mW | |
| On hook, Standby state | | | 35 | 85 | | |
| Off hook, OHT state | $R_L$ = 300 Ω, $R_{TMG}$ = ∞<br>BAT = –48 V | | 735 | 1050 | | |
| Off hook, Active state | $R_L$ = 300 Ω, $R_{TMG}$ = ∞<br>BAT = –48 V | | 1.25 | 1.45 | W | |
| | $R_L$ = 300 Ω, $R_{TMG}$ = ∞ | | 0.57 | 0.85 | | |
| Off hook, Standby state | $R_L$ = 600 Ω, $T_A$ = 25°C | | 0.68 | 1.0 | | |

## ELECTRICAL CHARACTERISTICS (continued)

| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| **Supply Currents, BAT = –48 V** | | | | | | |
| $V_{CC}$ on-hook supply current | Open Circuit state<br>OHT state<br>Standby state<br>Active state | | 1.7<br>4.9<br>2.2<br>6.3 | 2.5<br>7.5<br>3.0<br>8.5 | mA | |
| $V_{EE}$ on-hook supply current | Open Circuit state<br>OHT state<br>Standby state<br>Active state | | 0.7<br>2.0<br>0.77<br>2.1 | 2.0<br>3.5<br>2.0<br>5.0 | | |
| $V_{BAT}$ on-hook supply current | Open Circuit state<br>OHT state<br>Standby state<br>Active state | | 0.18<br>1.9<br>0.45<br>4.2 | 1.0<br>4.7<br>1.5<br>5.7 | | |
| **Power Supply Rejection Ratio ($V_{RIPPLE}$ = 50 mVrms), Active Normal State** | | | | | | |
| $V_{CC}$ | 50 Hz to 3400 Hz | 33 | 40 | | dB | 5 |
| $V_{EE}$ | 50 Hz to 3400 Hz | 29 | 35 | | | |
| $V_{BAT}$ | 50 Hz to 3400 Hz | 30 | 50 | | | |
| Effective internal resistance | CAS pin to GND | 85 | 170 | 255 | kΩ | 4 |
| RFI rejection | 100 kHz to 30 MHz<br>(See Figure E) | | | 1.0 | mVrms | 4 |
| **Off-Hook Detector** | | | | | | |
| Current threshold | $I_{DET} = \frac{375}{R_D}$ | –10 | | +10 | % | |
| **Ground-Key Detector Thresholds, Active State, BAT = –48 V** | | | | | | |
| Ground-key resistance threshold | B(RING) to GND | 2.0 | 5.0 | 10.0 | kΩ | |
| Ground-key current threshold | B(RING) to GND | | 9 | | mA | |
| **Ring-Trip Detector Input** | | | | | | |
| Bias current | | –0.5 | –0.05 | | µA | |
| Offset voltage | Source resistance = 2 MΩ | –50 | 0 | +50 | mV | 6 |
| **Logic Inputs (C3–C1, E0, E1)** | | | | | | |
| Input High voltage | | 2.0 | | | V | |
| Input Low voltage | | | | 0.8 | | |
| Input High current | All inputs except C3 and E1<br>Input C3<br>Input E1 | –75<br>–75<br>–75 | | 40<br>200<br>45 | µA | |
| Input Low current | | –0.4 | | | mA | |
| **Logic Output ($\overline{DET}$)** | | | | | | |
| Output Low voltage | $I_{OUT}$ = 0.8 mA | | | 0.4 | V | |
| Output High voltage | $I_{OUT}$ = –0.1 mA | 2.4 | | | | |
| **Relay Driver Output (RINGOUT)** | | | | | | |
| On voltage | 35 mA sink | | +0.25 | +0.4 | V | |
| Off leakage | $V_{OH}$ = +5 V | | | 100 | µA | |
| Zener breakover | 100 µA | 6 | 7.2 | | V | |
| Zener on voltage | 30 mA | | 10 | | | |

## RELAY DRIVER SCHEMATIC

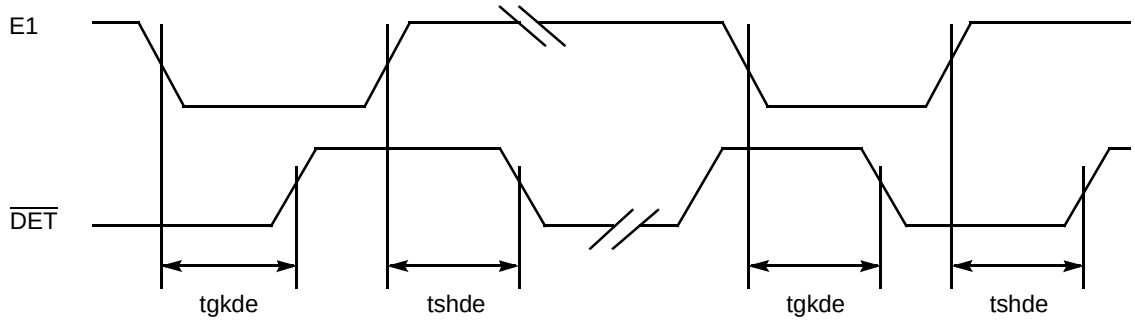



## SWITCHING CHARACTERISTICS
## (32-pin PLCC only)

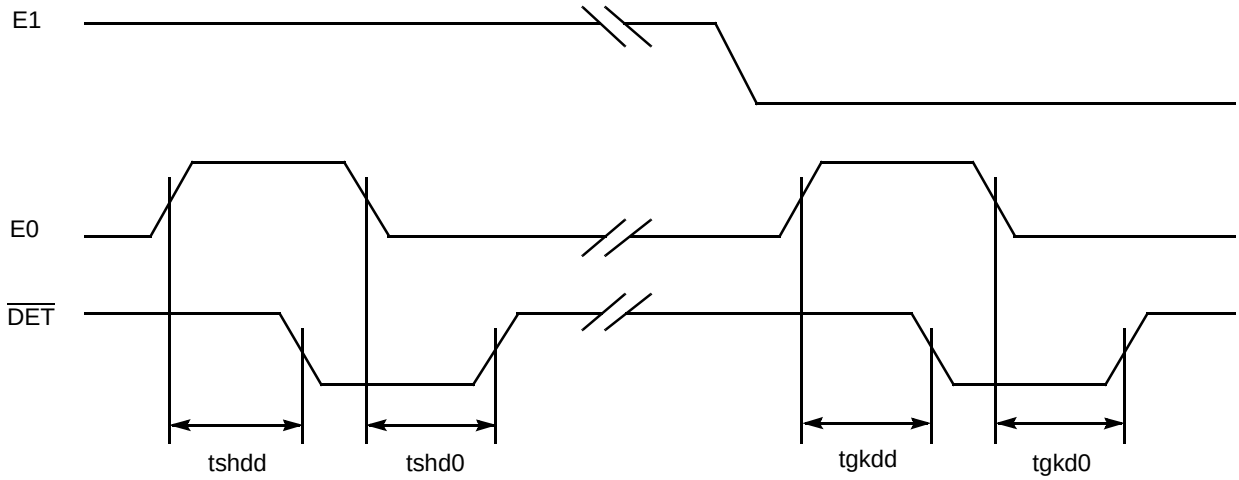
| Symbol | Parameter | Test Conditions | Temperature Range | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| tgkde | E1 Low to $\overline{DET}$ High (E0 = 1) | Ground-Key Detect state $R_L$ open, $R_G$ connected (See Figure G) | 0°C to 70°C<br>–40° to +85°C | | | 3.8<br>4.0 | µs | 4 |
| | E1 Low to $\overline{DET}$ Low (E0 = 1) | | 0°C to 70°C<br>–40° to +85°C | | | 1.1<br>1.6 | | |
| tgkdd | E0 High to $\overline{DET}$ Low (E1 = 0) | | 0°C to 70°C<br>–40° to +85°C | | | 1.1<br>1.6 | | |
| tgkd0 | E0 Low to $\overline{DET}$ High (E1 = 0) | | 0°C to 70°C<br>–40° to +85°C | | | 3.8<br>4.0 | | |
| tshde | E1 High to $\overline{DET}$ Low (E0 = 1) | Switchhook Detect state $R_L$ = 600 Ω, $R_G$ open (See Figure F) | 0°C to 70°C<br>–40° to +85°C | | | 1.2<br>1.7 | | |
| | E1 High to $\overline{DET}$ High (E0 = 1) | | 0°C to 70°C<br>–40° to +85°C | | | 3.8<br>4.0 | | |
| tshdd | E0 High to $\overline{DET}$ Low (E1 = 1) | | 0°C to 70°C<br>–40° to +85°C | | | 1.1<br>1.6 | | |
| tshd0 | E0 Low to $\overline{DET}$ High (E1 = 1) | | 0°C to 70°C<br>–40° to +85°C | | | 3.8<br>4.0 | | |

## SWITCHING WAVEFORMS

**E1 to $\overline{\text{DET}}$**




**E0 to $\overline{\text{DET}}$**

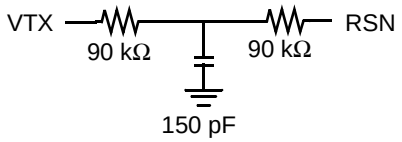



***Note:***
*All delays measured at 1.4 V level.*

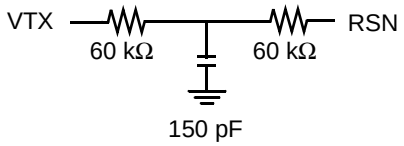
***Notes:***

1. *Unless otherwise noted, test conditions are $V_{CC}$ = +5 V, $V_{EE}$ = –5 V, $C_{HP}$ = 0.33 µF, $R_{DC1}$ = $R_{DC2}$ = 9.26 kΩ, $C_{DC}$ = 0.33 µF, $R_d$ = 35.4 kΩ, $C_{CAS}$ = 0.33 µF, no fuse resistors, BAT = –48 V, $R_L$ = 900 Ω, and $R_{TMG}$ = 1700 Ω.*
2. *a. Overload level is defined when THD = 1%.*
   *b. Overload level is defined when THD = 1.5%.*
3. *Balance return signal is the signal generated at $V_{TX}$ by $V_{RX}$. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz with a termination impedance of 900 Ω and an $R_L$ of 600 Ω in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Assumes the following $Z_T$ networks:*

(900 Ω):




(600 Ω):




8. *Group delay can be considerably reduced by using a $Z_T$ network such as that shown in Note 7 above. The network reduces the group delay to less than 2 µs. The effect of group delay on the linecard performance may be compensated for by using the QSLAC™ or DSLAC™ device.*

**Table 1. SLIC Decoding**

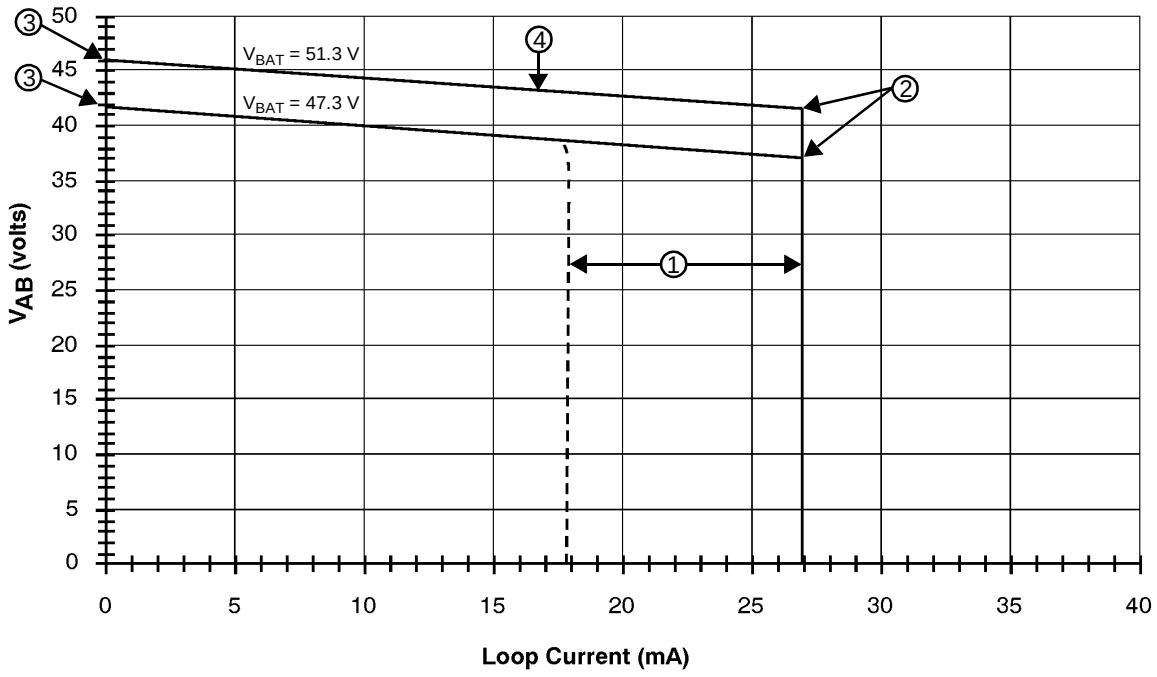
| | | | | $\overline{\text{DET}}$ Output | |
|---|---|---|---|---|---|
| **State** | **C3** | **C2** | **C1** | **Two-wire Status** | **E1 = 1** | **E1 = 0** |
| 0 | 0 | 0 | 0 | Open Circuit | Ring trip | Ring trip |
| 1 | 0 | 0 | 1 | Ringing | Ring trip | Ring trip |
| 2 | 0 | 1 | 0 | Active | Loop detector | Ground key |
| 3 | 0 | 1 | 1 | On-hook TX (OHT) | Loop detector | Ground key |
| 4 | 1 | 0 | 0 | Tip Open | Loop detector | Ground key |
| 5 | 1 | 0 | 1 | Standby | Loop detector | Ground key |
| 6 | 1 | 1 | 0 | Active Polarity Reversal | Loop detector | Ground key |
| 7 | 1 | 1 | 1 | OHT Polarity Reversal | Loop detector | Ground key |

***Note:***
*E0 and E1 are internally pulled High in the 22-pin DIP package option. E0 High enables the $\overline{DET}$ pin.*

**Table 2. User-Programmable Components**

| | |
|---|---|
| $Z_T = 200(Z_{2WIN} - 2R_F)$ | $Z_T$ is connected between the VTX and RSN pins. The fuse resistors are $R_F$ and $Z_{2WIN}$ is the desired 2-wire AC input impedance. When computing $Z_T$, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account. |
| $Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{200 \bullet Z_T}{Z_T + 200(Z_L + 2R_F)}$ | $Z_{RX}$ is connected from $V_{RX}$ to RSN. $Z_T$ is defined above and $G_{42L}$ is the desired receive gain. |
| $R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$<br>$C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$ | $R_{DC1}$, $R_{DC2}$, and $C_{DC}$ form the network connected to the RDC pin. $R_{DC1}$ and $R_{DC2}$ are approximately equal. $I_{LOOP}$ is the desired loop current in the constant-current region. |
| $R_D = \frac{375}{I_T}$, $C_D = \frac{0.5\ ms}{R_D}$ | $R_D$ and $C_D$ form the network connected from RD to –5 V and $I_T$ is the threshold current between on hook and off hook. |
| $I_{OHT} = \frac{500\ V \bullet 0.66}{R_{DC1} + R_{DC2}}$ | OHT loop current (constant-current region) |
| $C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$ | $C_{CAS}$ is the regulator filter capacitor and $f_c$ is the desired filter cut-off frequency. |
| **Thermal Management Equations (Normal Active and Tip Open states)** | |
| $R_{TMG} = \frac{V_{BAT} - 6\ V}{I_{LOOP}}$ | $R_{TMG}$ is connected from TMG to $V_{BAT}$ and is used to limit power dissipation within the SLIC in Normal Active and Tip Open states only. |
| $P_{RTMG} = \frac{(V_{BAT} - 6\ V - (I_L \bullet R_L))^2}{R_{TMG}}$ | Power dissipated in the thermal management resistor, $R_{TMG}$, during Active and Tip Open states |
| $P_{SLIC} = V_{BAT} \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12\ W$ | Power dissipated in the SLIC while in Active and Tip Open states |
| **Thermal Management Equations (Polarity Reverse State)**<br>**Note: SLIC die temperature should not exceed 140°C.** | |
| $P_{SLIC} = V_{BAT} \bullet I_L - R_L(I_L)^2 + 0.12\ W$ | Power dissipated in the SLIC while in the Polarity Reverse state |
| $T_{SLIC} = P_{SLIC} \bullet \theta_{JA} + T_{Ambient}$ | Total die temperature |
| Theta JA ($\theta_{JA}$) PDIP = 60°C/watt | Thermal impedance of the 22-pin plastic dip package |
| Theta JA ($\theta_{JA}$) CDIP = 55°C/watt | Thermal impedance of the 22-pin ceramic dip package |
| Theta JA ($\theta_{JA}$) PLCC = 43°C/watt | Thermal impedance of the 32-pin plastic leaded chip carrier package |

## DC FEED CHARACTERISTICS




$R_{DC1} + R_{DC2} = R_{DC} = 18.52\ k\Omega$

***Notes:***

1. *Constant-current region:*

   *Active state,* $I_L = \frac{500}{R_{DC}}$

   *OHT state,* $I_L = \frac{2}{3} \bullet \frac{500}{R_{DC}}$

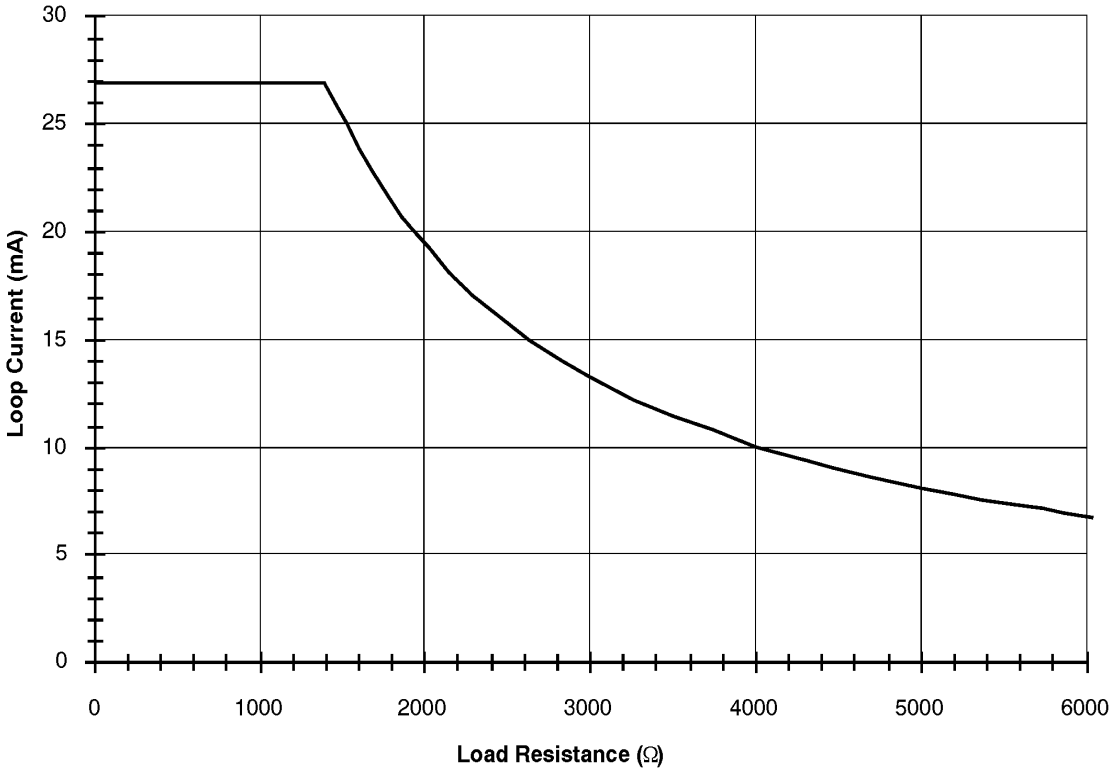
2. *Anti-sat (battery tracking) turn-on:* $V_{AB} = 1.017|V_{BAT}| - 10.7$

3. *Open circuit voltage:* $V_{AB} = 1.017|V_{BAT}| - 6.3$

4. *Anti-sat (battery tracking) region:* $V_{AB} = 1.017|V_{BAT}| - 6.3 - I_L \frac{R_{DC}}{120}$

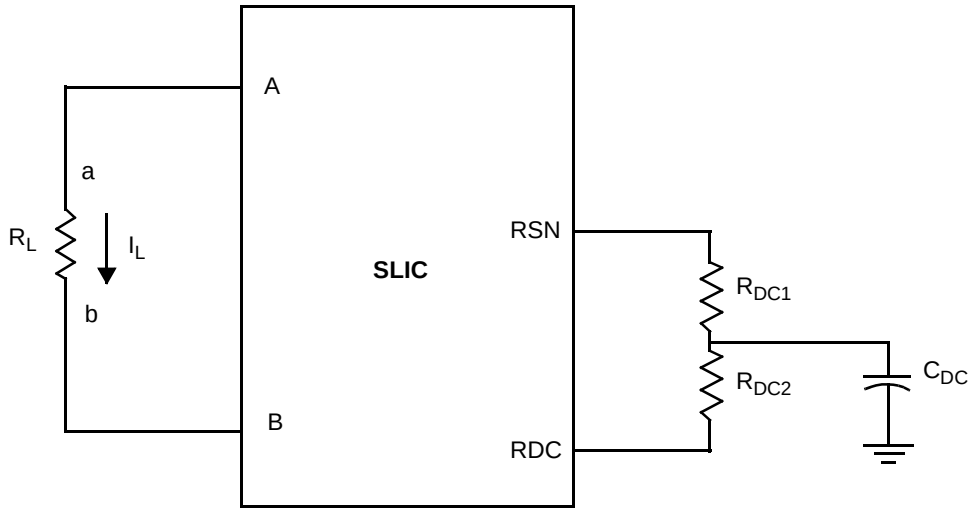
**a. $V_A$–$V_B$ ($V_{AB}$) Voltage vs. Loop Current (Typical)**

## DC FEED CHARACTERISTICS (continued)




$R_{DC1} + R_{DC2} = R_{DC} = 18.52\ k\Omega$
$V_{BAT} = 47.3\ V$

**b. Loop Current vs. Load Resistance (Typical)**

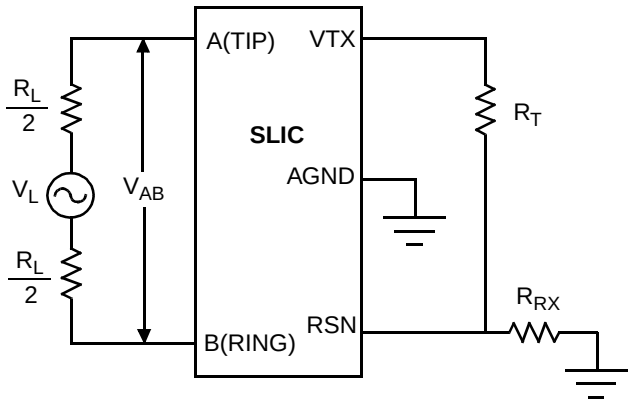



Feed current programmed by $R_{DC1}$ and $R_{DC2}$

**c. Feed Programming**

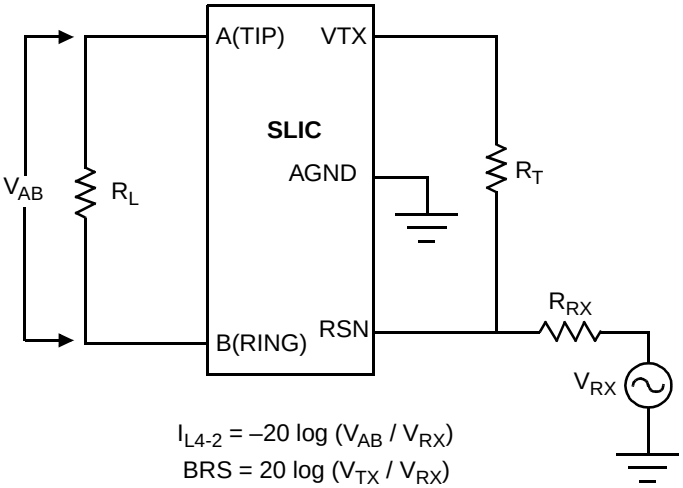
**Figure 1. DC Feed Characteristics**

## TEST CIRCUITS




$I_{L2\text{-}4} = -20 \log (V_{TX} / V_{AB})$

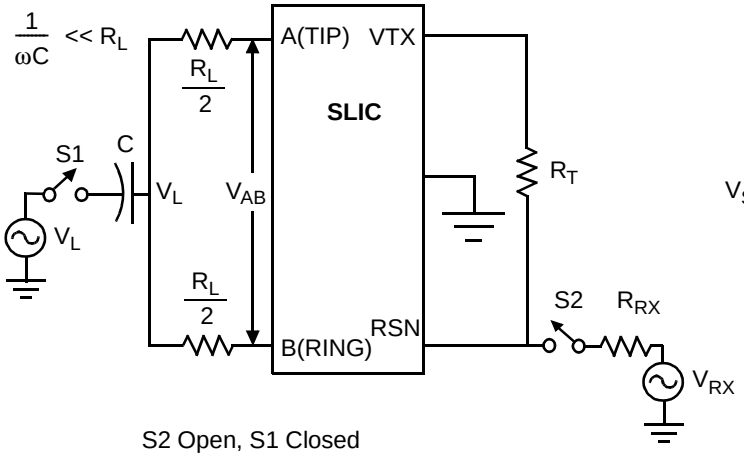
**A. Two- to Four-Wire Insertion Loss**




$I_{L4\text{-}2} = -20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

**B. Four- to Two-Wire Insertion Loss and Balance Return Signal**




S2 Open, S1 Closed

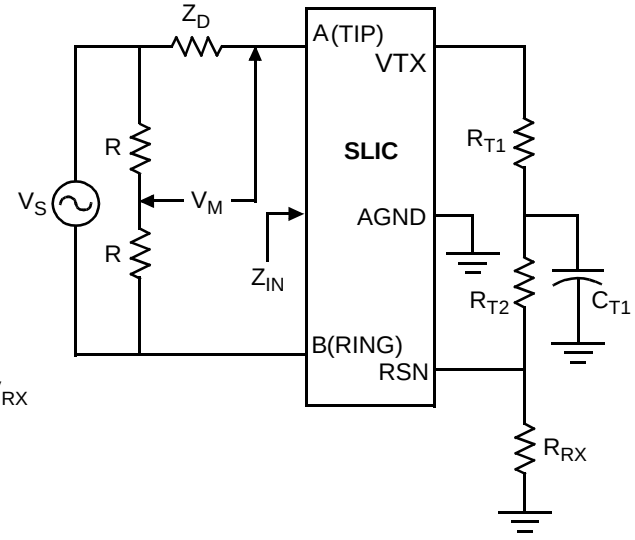
L-T Long. Bal. = 20 log ($V_{AB}$ / $V_L$)

L-4 Long. Bal. = 20 log ($V_{TX}$ / $V_L$)

S2 Closed, S1 Open

4-L Long. Sig. Gen. = 20 log ($V_L$ / $V_{RX}$)

**C. Longitudinal Balance**



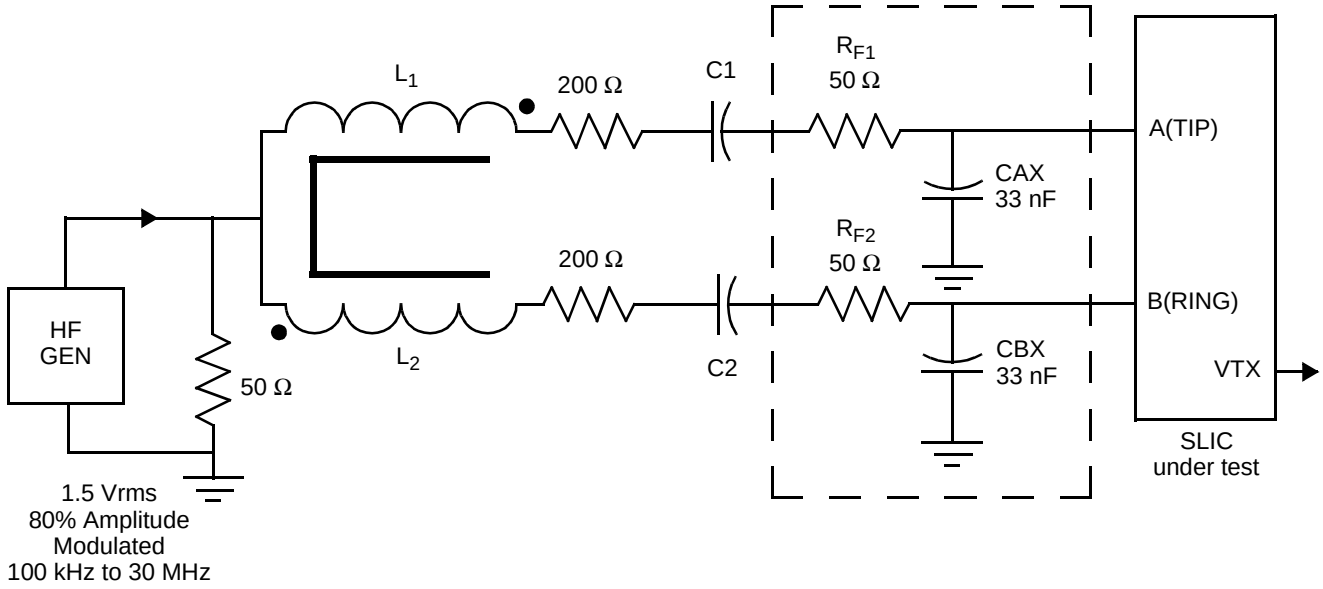

***Note:***

*$Z_D$ is the desired impedance (e.g., the characteristic impedance of the line).*

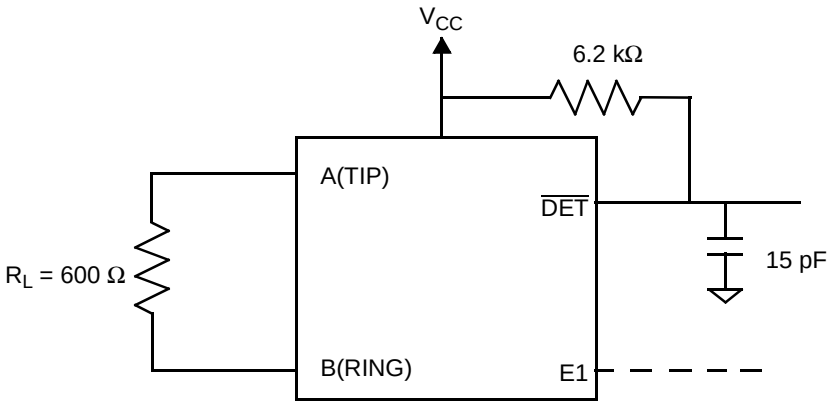
$R_L = -20 \log (2 V_M / V_S)$

**D. Two-Wire Return Loss Test Circuit**

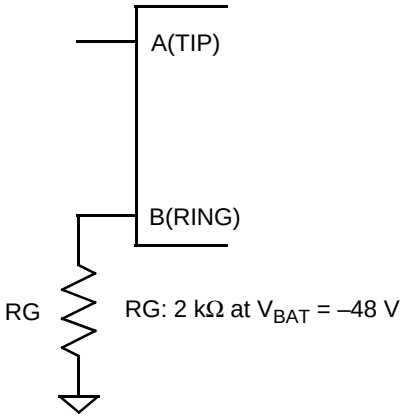
## TEST CIRCUITS (continued)




**E. RFI Test Circuit**

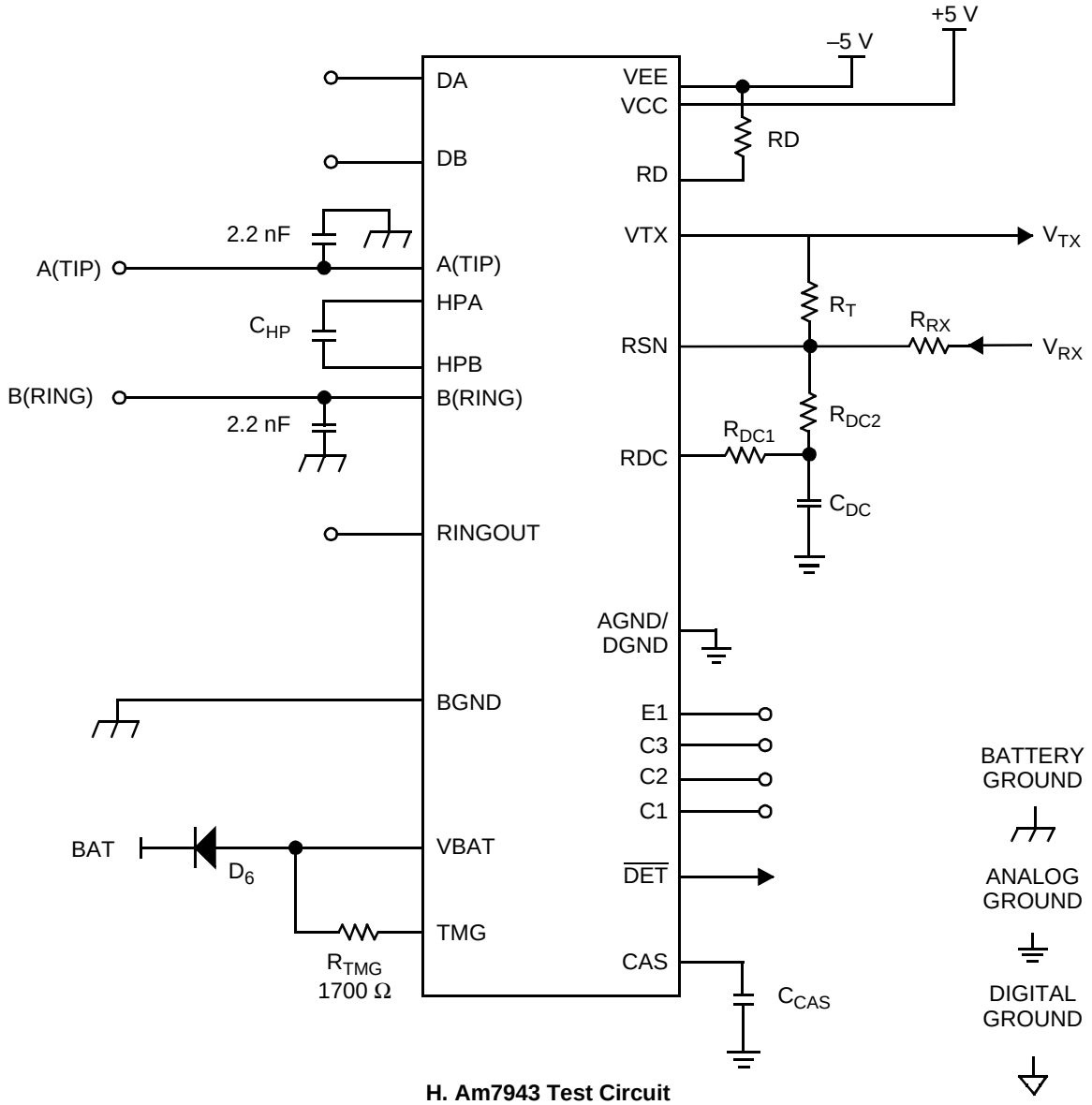



**F. Loop-Detector Switching**




**G. Ground-Key Switching**

## TEST CIRCUITS (continued)




**H. Am7943 Test Circuit**

## REVISION SUMMARY

### Revision A to B

- Minor changes were made to the data sheet style and format to conform to AMD standards.

### Revision B to Revision C

- In Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”
- Minor changes were made to the data sheet style and format to conform to AMD standards.