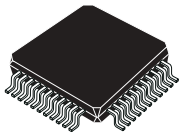
STLC3065

WLL SUBSCRIBER LINE INTERFACE CIRCUIT

- MONOCHIP SLIC OPTIMISED FOR WLL APPLICATIONS
- IMPLEMENT ALL KEY FEATURES OF THE BORSHT FUNCTION
- SINGLE SUPPLY (5.5 TO 15.8V)
- BUILT IN DC/DC CONVERTER CONTROLLER.
- SOFT BATTERY REVERSAL WITH PROGRAMMABLE TRANSITION TIME.
- ON-HOOK TRANSMISSION.
- PROGRAMMABLE OFF-HOOK DETECTOR THRESHOLD
- METERING PULSE GENERATION AND FILTER
- INTEGRATED RINGING
- INTEGRATED RING TRIP
- DUAL 2W PORT FOR DATA/VOICE OPERATION
- PARALLEL CONTROL INTERFACE (3.3V LOGIC LEVEL)
- PROGRAMMABLE CONSTANT CURRENT FEEDER
- SURFACE MOUNT PACKAGE



TQFP44

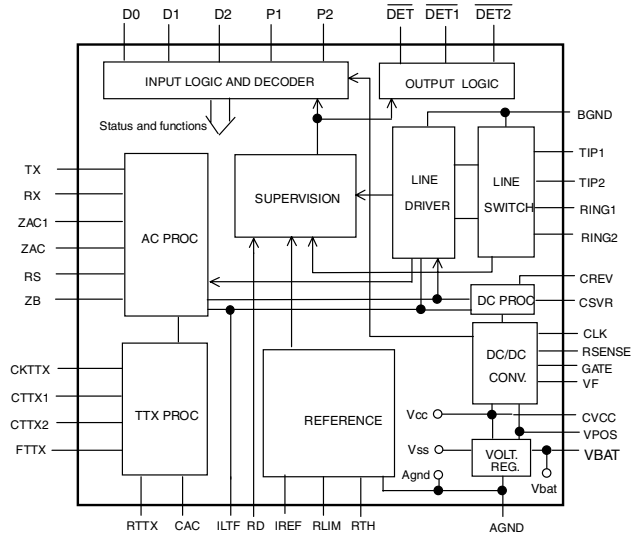
ORDERING NUMBERS: STLC3065Q
STLC3065QTR

- INTEGRATED THERMAL PROTECTION
- -40 TO +85°C OPERATING RANGE

DESCRIPTION

The STLC3065 is a SLIC device specifically designed for WLL (Wireless Local Loop) application. One of the distinctive characteristics of this device is the ability to operate with a single supply voltage (from +5.5V to +15.8V) and self generate the negative battery by means of an on chip DC/DC converter controller that drives an external

BLOCK DIAGRAM



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DESCRIPTION (continued)

MOS switch.

The self generated battery voltage tracks the line resistance. In this way the power dissipation inside the device is low enough to allow the use of small SMD package (TQFP44).

Other useful characteristics for application in the WLL environment are the integrated ringing generator and the dual two wire port that allows to drive two different terminal equipment whether the transmission is voice or data. When one port is transmitting the other one is idle.

The control interface is a parallel type with open drain output and 3.3V logic levels.

The metering pulses are generated on chip starting from two logic signals (0, 3.3V) one defines the metering pulse frequency and the other the metering pulse duration. An on chip circuit then provides the proper shaping and filtering.

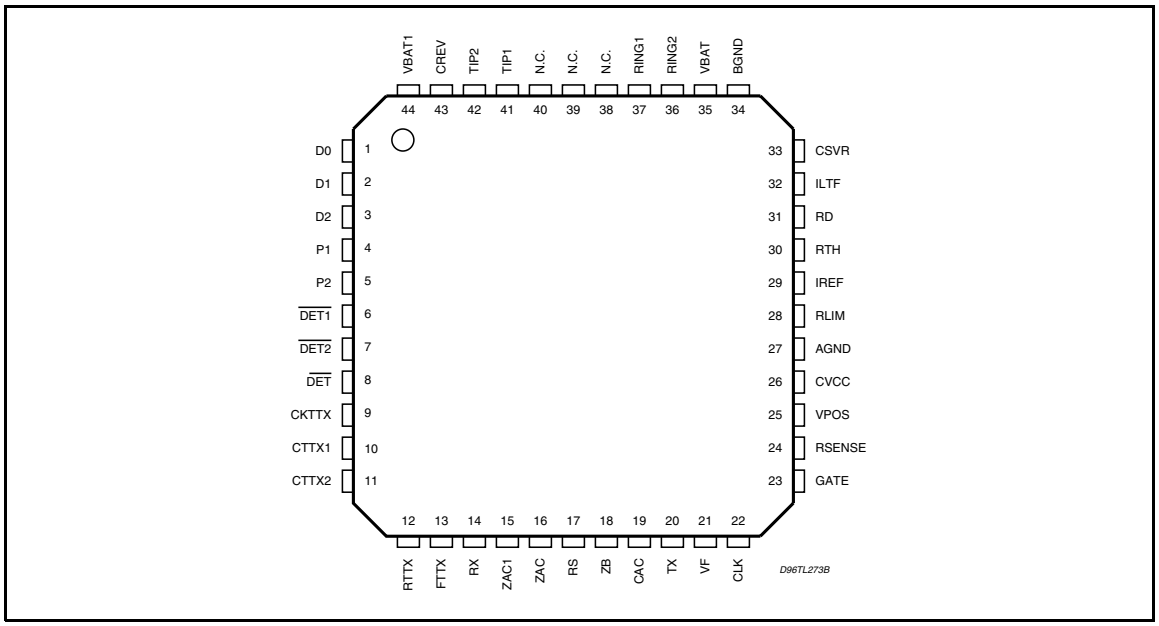
Metering pulse amplitude and shaping (rising and decay time) can be programmed by external components. A dedicated cancellation circuit avoid possible CODEC input saturation due to Metering pulse echo.

Constant current feed can be set from 20mA to 40mA.

Off-hook detection threshold is programmable from 5mA to 9mA.

The device, developed in BCD100II technology (100V process), operates in the extended temperature range and integrates a thermal protection that set the device in power down when Tj exceeds 140°C.

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{pos}	Positive Supply Voltage	-0.4 to +17	V
A/BGND	AGND to BGND	-1 to +1	V
V_{dig}	Pin D0, D1, D2, P1, P2, $\overline{DET}$, $\overline{DET1}$, $\overline{DET2}$ CKTTX	-0.4 to 5.5	V
T_j	Max. junction Temperature	150	°C
V_{btot} (1)	Vbtot=|Vpos|+|Vbat|. (Total voltage applied to the device supply pins).	100	V

(1) Vbat is self generated by the on chip DC/DC converter and can be programmed via RF1 and RF2. RF1 and RF2 shall be selected in order to fulfil the a.m limits (see External Components Table page 13)

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OPERATING RANGE

Symbol	Parameter	Value	Unit
V_{pos}	Positive Supply Voltage	5.5 to +15.8	V
A/BGND	AGND to BGND	-100 to +100	V
V_{dig}	Pin D0, D1, D2, $\overline{DET}$, $\overline{DET1}$, $\overline{DET2}$, CKTTX, P_1, P_2	-0.25 to 5.25	V
T_{op}	Ambient Operating Temperature Range	-40 to +85	°C
V_{bat} (1)	Self Generated Battery Voltage	-74 max.	V

(1) Vbat is self generated by the on chip DC/DC converter and can be programmed via RF1 and RF2.
RF1 and RF2 shall be selected in order to fulfil the a.m limits (see External Components Table page 10)

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Typ.	60	°C/W

PIN DESCRIPTION

N.	Name	Function
25	VPOS	Positive supply input ranging from 5.5V to 15.8V.
34	BGND	Battery Ground, must be shorted with AGND.
27	AGND	Analog Ground, must be shorted with BGND.
16	ZAC	AC impedance synthesis.
15	ZAC1	RX buffer output, the AC impedance is connected from this node to ZAC.
17	RS	Protection resistors image (the image resistor is connected from this node to ZAC).
18	ZB	Balance Network for 2 to 4 wire conversion (the balance impedance ZB is connected from this node to AGND. ZA impedance is connected from this node to ZAC1).
20	TX	4 wire output port (TX output). The signal is referred to AGND. If connected to single supply CODEC input it must be DC decoupled with proper capacitor.
14	RX	4 wire input port (RX input); 300KΩ input impedance. This signal is referred to AGND. If connected to single supply CODEC output it must be DC decoupled with proper capacitor.
19	CAC	AC feedback input, AC/DC split capacitor (CAC).
32	ILTF	Transversal line current image output.
41	TIP1	2 wire port #1; TIP wire (Ia is the current sourced from this pin).
37	RING1	2 wire port #1; RING wire (Ib is the current sunk into this pin).
42	TIP2	2 wire port #2; TIP wire (Ia is the current sourced from this pin)
36	RING2	2 wire port #2; RING wire (Ib is the current sunk into this pin)
28	RLIM	Constant current feed programming pin (via RLIM). RLIM should be connected close to this pin and PCB layout should avoid noise injection on this pin.
30	RTH	Off-hook threshold programming pin (via RTH). RTH should be connected close to this pin and PCB layout should avoid noise injection on this pin.
29	IREF	Internal bias current setting pin. RREF should be connected close to this pin and PCB layout should avoid noise injection on this pin.
43	CREV	Reverse polarity transition time control. One proper capacitor connected between this pin and AGND is setting the reverse polarity transition time. This is the same transition time used to shape the "trapezoidal ringing" during ringing injection.
26	CVCC	Internal positive voltage supply filter.

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PIN DESCRIPTION (continued)

N.	Name	Function
35	VBAT	Regulated battery voltage self generated by the device via DC/DC converter. Must be shorted to VBAT1.
23	GATE	Driver for external Power MOS transistor.
21	VF	Feedback input for DC/DC converter controller.
22	CLK	Power Switch Controller Clock (typ. 125KHz). From version marked STLC3065 A5, this pin can also be connected to CVCC or AGND. When the CLK pin is connected to CVCC an internal auto-oscillation is internally generated and it is used instead of the external clock. When the CLK pin is connected to AGND, the GATE output is disabled.
24	RSENSE	Voltage input for current sensing. RSENSE should be connected close to this pin and VPOS pin. The PCB layout should minimize the extra resistance introduced by the copper tracks.
1	D0	Control Interface: input bit 0.
2	D1	Control Interface: input bit 1.
3	D2	Control interface: input bit 2.
4	P1	Control Interface: port 1 selection bit
5	P2	Control Interface: port 2 selection bit
8	$\overline{DET}$	Logic interface output of the supervision detector (active low).
6	$\overline{DET1}$	Logic interface output of thr linr port 1 detector (active low)
7	$\overline{DET2}$	Logic interface output of thr linr port 2 detector (active low)
33	CSVR	Battery supply filter capacitor.
12	RTTX	Metering pulse cancellation buffer output. TTX filter network should be connected to this point. If not used should be left open.
13	FTTX	Metering pulse buffer input this signal is sent to the line and used to perform TTX filtering.
10	CTTX1	Metering burst shaping external capacitor.
11	CTTX2	Metering burst shaping external capacitor.
9	CKTTX	Metering pulse clock input (12 KHz or 16KHz square wave).
44	VBAT1	Frame connection. Must be shorted to VBAT.
38,39, 40	NC	Not connected.

FUNCTIONAL DESCRIPTION

The STLC3065 is a device specifically developed for WLL application.

It is based on a SLIC core, on purpose optimised for this application, with the addition of a DC/DC converter controller and a dual port in order to fulfil the WLL requirements.

The SLIC core performs the standard feeding, signalling and transmission functions.

It can be set in three different operating modes via the D0, D1, D2 pins of the control logic interface (0 to 3.3V logic levels). The loop status is carried out on the $\overline{DET}$ pin (active low).The $\overline{DET}$ pin is an open drain output to allow easy interfacing with both 3.3V and 5V logic levels.

The three possible SLIC core operating modes are:

- Power Down (PWD)
- Active
- Ringing

Table 1 shows how to set the different SLIC core operating modes.

Table 1. SLIC core operating modes.

D0	D1	D2	Operating Mode
0	0	X	Power Down
0	1	0	Active Normal Polarity
0	1	1	Active Reverse Polarity
1	1	0	Active TTX injection (N.P.)
1	1	1	Active TTX injection (R.P.)
1	0	0/1	Ring (D2 bit toggles @ fring)

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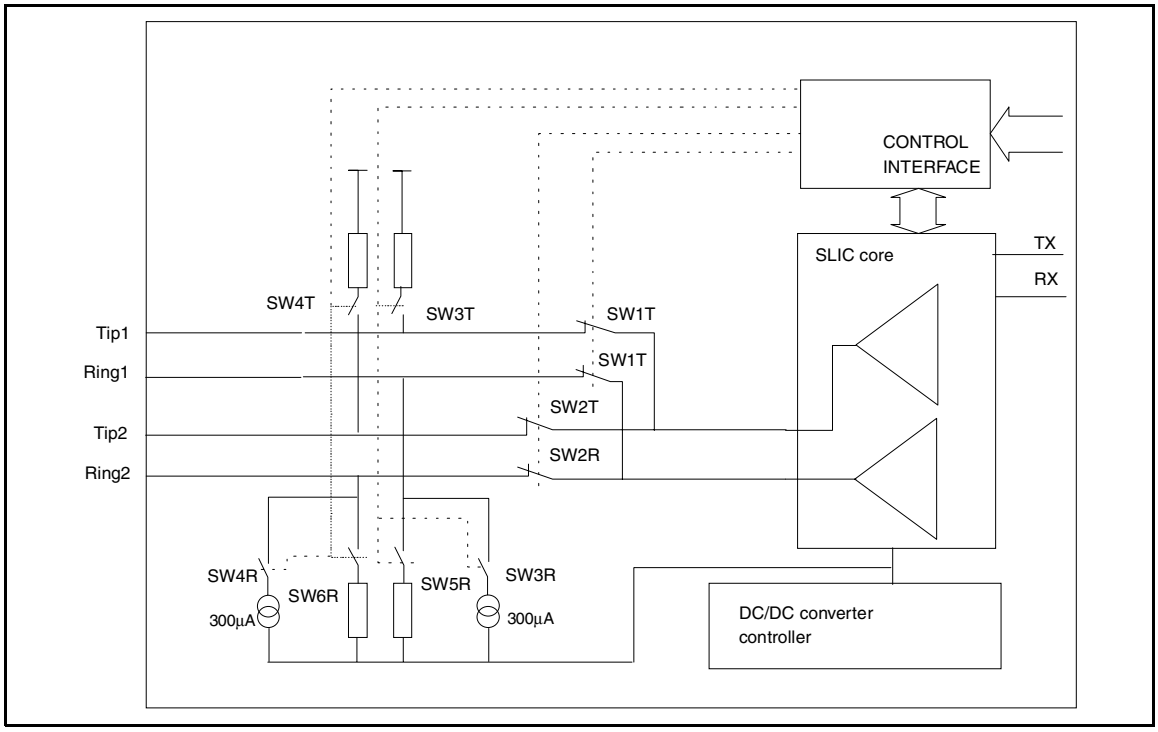
FUNCTIONAL DIAGRAM



The STLC3065 operating modes will be obtained as combination of the SLIC core status and the dual port configuration.

The DC/DC converter controller is driving an external power MOS transistor (P-Channel) in order to generate the negative battery voltage needed for device operation.

The DC/DC converter controller is synchronised with an external CLK (125KHz typ.).
From version marked STLC3065 A5, it can be synchronised to an internal clock generated when the pin CLK is connected to CVCC. One sensing resistor in series to Vpos supply allows to fix the maximum allowed input peak current. This feature is implemented in order to avoid overload on Vpos supply in case of line transient (ex. ring trip detection).

The typical value is obtained for a sensing resistor equal to 110mΩ that will guarantee an average current consumption from Vpos < 700mA.

In on-hook condition the self generated battery voltage is set to a predefined value.

This value can be adjusted via one external resistor (RF1) and it is typical -50V. When RING mode is selected this value is increased up to -70V typ.

Once the line goes in off-hook condition the DC/DC converter automatically adjust the generated battery voltage in order to feed the line with a fixed DC current (programmable via RLIM) optimising in this way the power dissipation.

The Dual Port allows to connect the SLIC core to one of the two possible 2W ports (TIP1/RING1, TIP2/RING2).

Dual port concept

One switches array integrated in STLC3065 allows to connect the TIP and RING output of the SLIC core to one of the two 2W ports (TIP1/RING1 or TIP2/RING2). For special conditions it is also possible to connect both ports to the SLIC core.The structure of the switches array is shown in fig.1 and it is controlled via the two logic inputs P1 and P2.

Depending on the switches configurations each 2W port (TIP1/RING1 or TIP2/RING2) can be set in four possible conditions:

- Open
- Connected to BGND and Battery via two integrated 1.5KΩ resistors.
- Connected to the SLIC core
- Connected to an internal 300µA (min.) current source.

Depending on the SLIC core operating modes (defined by D0,D1 and D2) only a subset of these conditions can be programmed.

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Figure 1. Dual Port Concept.

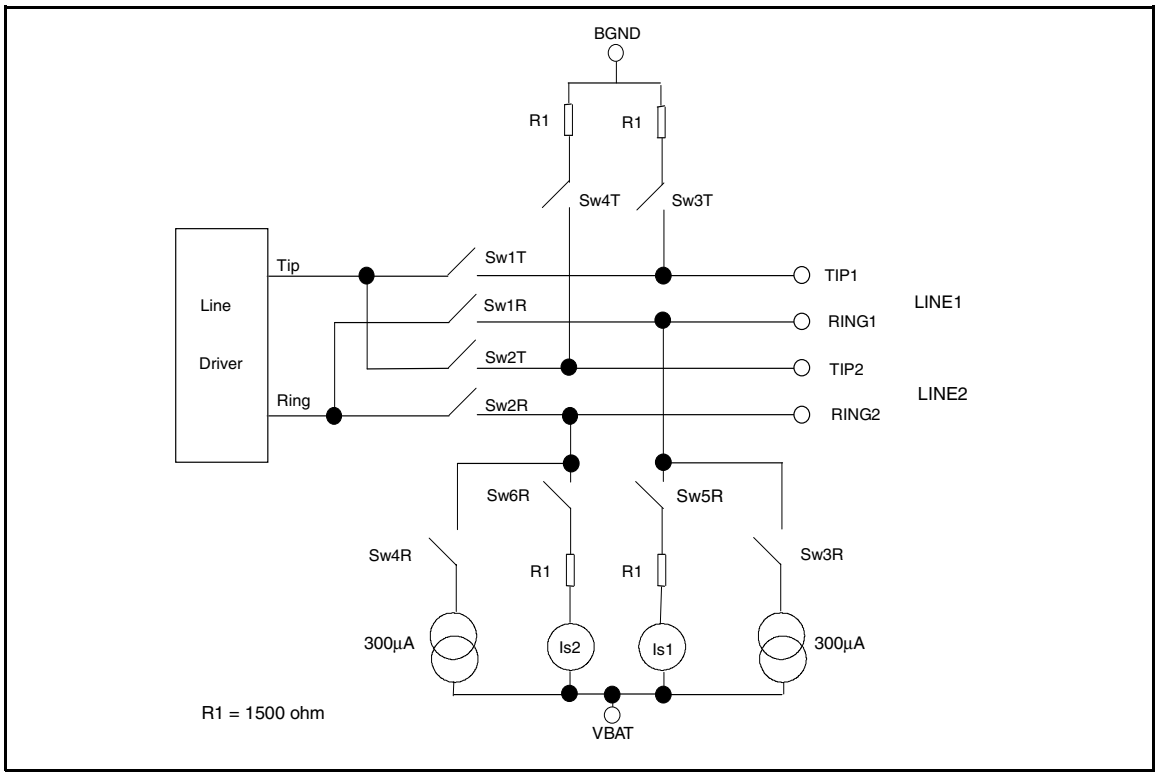

Table 2. Dual Port control.

D0	D1	D2	P1	P2	OPER. MODE	LINE 1	LINE 2	$\overline{DET}$	$\overline{DET1}$	$\overline{DET2}$
0	0	X	0	0	Power Down	Open	Open	-	-	-
0	0	X	1	1	High Z feed.	To P.S. via Res.	To P.S. via Res.	off-hook line 1+2	off-hook line 1	off-hook line 2
0	0	X	0	1	Power Down/ High Z feed.	Open	To P.S. via Res.	off-hook line 2	-	off-hook line 2
0	0	X	1	0	High Z feed. Power Down	To P.S. via Res.	Open	off-hook line 1	off-hook line 1	-
X	1	X	0	0	ACTIVE	300µA bias	300µA bias	-	-	-
X	1	X	1	1	ACTIVE	To Buffer	To Buffer	off-hook line 1+2	-	-
X	1	X	0	1	ACTIVE	300µA bias	To Buffer	off-hook line 2	-	-
X	1	X	1	0	ACTIVE	To Buffer	300µA bias	off-hook line 1	-	-
1	0	X	0	0	RING	300µA bias	300µA bias	-	-	-
1	0	X	1	1	RING	To Buffer	To Buffer	Ring-trip line 1+2	-	-
1	0	X	0	1	RING	300µA bias	To Buffer	Ring-trip line 2	-	-
1	0	X	1	0	RING	To Buffer	300µA bias	Ring-trip line 1	-	-

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Where:

"Open":	the line port termination is in high impedance.
"To P.S. via Res":	the TIP(n) wire is connected to BGND through a 1500Ω resistor , the RING(n) wire is connected to VBAT by a 1500Ω resistor. The current flowing in the second resistor is used to detect the off-hook .
"To Buffer":	the TIP(n) wire and RING(n) wire are connected to the SLIC core line driver and the off-hook detection is performed using the SLIC core supervision circuit that drives the $\overline{DET}$ output.
"300μA bias":	the TIP(n) wire is connected to BGND through a 1500Ω resistor , the RING(n) wire is biased by a 300μA current generator to negative battery (Vbat)

Note: see also Appendix C

Table 2 shows all the possible combinations between switches configurations and operating modes.

A detailed description of each configuration can be found in the "OPERATING MODES" description section.

OPERATING MODES

Power Down (PWD)

D0	D1	D2	P1	P2	$\overline{DET}$	$\overline{DET1}$	$\overline{DET2}$
0	0	X	0	0	disable	disable	disable

DC CHARACTERISTIC & SUPERVISION

When this mode is selected both 2W ports (TIP1/RING1 and TIP2/RING2) are in high impedance; all switches Sw1 to Sw6 are open (see fig.1)

The SLIC core is switched off and the line detectors are disabled therefore the off-hook condition cannot be detected.

This mode can be selected in emergency condition when it is necessary to cut any current delivered to the line.

This mode is also forced by STLC3065 in case of thermal overload (Tj > 140°C).

In this case the device goes back to the previous status as soon as the junction temperature decrease under the hysteresis threshold.

AC CHARACTERISTICS

Both the 2W ports (TIP1/RING1 and TIP2/RING2) are set in high impedance, the TX output buffer is a low impedance output, no AC transmission is possible.

High Impedance Feeding (HI-Z)

D0	D1	D2	P1	P2	$\overline{DET}$	$\overline{DET1}$	$\overline{DET2}$
0	0	X	1	1	off/hk line 1+2	off/hk line 1	off/hk line 2
0	0	X	0	1	off/hk line 2	disable	off/hk line 1
0	0	X	1	0	off/hk line 1	off/hk line 1	disable

DC CHARACTERISTIC & SUPERVISION

This operating mode is normally selected when the telephone is in on-hook in order to monitor the line status keeping the power consumption at the minimum.

The SLIC core of STLC3065 is in PWD mode (see fig.1 or FUNCTIONAL DIAGRAM); the two line series switches (Sw1; Sw2) are open. Depending on P1, P2 the 2W ports (TIP1/RING1 and TIP2/RING2) can be in high impedance or connected to the built in feeding resistors (2x1500Ω) via SW3T and SW5R or SW4T and SW6R.

P1 controls TIP1/RING1 and P2 controls TIP2/RING2 (see Fig.1 and Table 2).

When this mode is selected normally both P1, P2 bits should be set to one.

The output voltage in on-hook condition is equal to the self generated battery voltage (-50V typ).

When off-hook occurs on 2W port 1 (2) the current flowing through the RING1(2) wire activates the DET1 (2_) detector indicating the line status change. When DET1 or DET2 are activated also the $\overline{DET}$ become active (low logic level).

The off-hook threshold in HI-Z mode is the same value programmed in ACTIVE mode.

The DC characteristic in HI-Z mode is just equal to the self generated battery with 2x(1500W+Rp)

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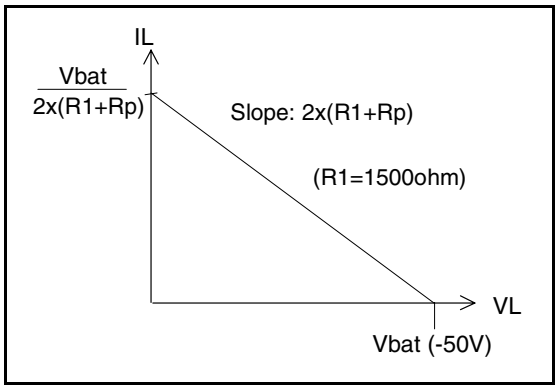
in series (see fig.2), where Rp is the external protection resistance.

It should be noted that in case of both ports in HI-Z mode and both of them in off-hook condition the power dissipated inside the chip could drive the device in thermal protection. This can be prevented via a proper software control that should avoid to keep as a steady condition both lines in off-hook and HI-Z mode. Typical operation is to set the SLIC core in active mode as soon as off-hook is detected.

Figure 2. DC characteristic in HI-Z mode.



AC CHARACTERISTICS

The AC impedance shown at the 2W ports (TIP1/RING1 and TIP2/RING2) is the same as the DC one. Depending on the P1, P2 bits the TIP1/RING1 and TIP2/RING2 AC impedance will be 2x(1500Ω + Rp) or high impedance.

Active

D0	D1	D2	P1	P2	$\overline{DET}$	$\overline{DET1}$	$\overline{DET2}$
X	1	X	0	0	disable	disable	disable
X	1	X	1	1	off/hk line 1+2	disable	disable
X	1	X	0	1	off/hk line 2	disable	disable
X	1	X	1	0	off/hk line 1	disable	disable

DC CHARACTERISTICS & SUPERVISION

When this mode is selected it is because one connected telephone goes off-hook and the STLC3065 is providing both DC feeding and AC transmission.

The SLIC core is in ACTIVE mode and normally only one of the two port should be connected to it: P1,P2 = (1,0) or (0,1). (see Fig.1 and Table 2).

The unselected port is anyway DC biased being TIP wire connected to BGND via a 1600W resistor and the RING wire connected to a 300mA (min.) current source connected to Vbat.

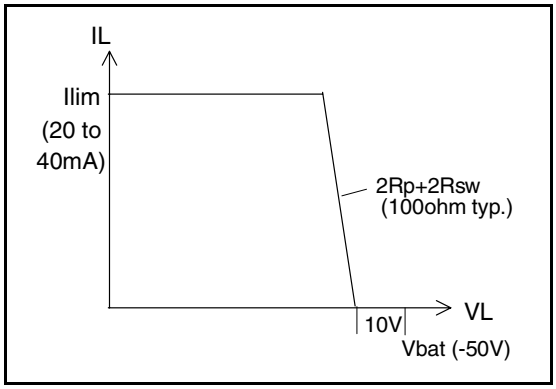
It should be noted that since Vbat is self generated by the STLC3065 and it is tracking the line voltage depending on the loop resistance connected to the selected port its voltage can range typically from -12V to -50V. The unselected port status (on/off hook) cannot be detected. For special configurations it is also possible to set ACTIVE mode with both port selected (P1,P2=1,1) or both unselected (P1,P2=0,0).

Considering now the selected port, this is connected to the SLIC core. The STLC3065 feeds the line with a constant current fixed by RLIM (20mA to 40mA range). The on-hook voltage is typically 40V allowing on-hook transmission; the self generated Vbat is -52V typ.

If the loop resistance is very high and the line current cannot reach the programmed constant current feed value, the STLC3065 behaves like a 40V voltage source with a series impedance equal to the protection resistors 2xRp(typ. 2x41Ω) plus the line series switches (Sw1 or Sw2) on resistance 2xRsw (typ. 2x9Ω).

Fig.3 shows the typical DC characteristic in ACTIVE mode.

Figure 3. DC characteristic in ACTIVE mode



The line status (on/off hook) is monitored by the SLIC core Supervision circuit. The off-hook threshold can be programmed via the external resistor RTH in the range from 5mA to 9mA.

When the line goes in off-hook condition the built in DC/DC converter controller set properly the Vbat supply in order to keep the loop current fixed to the programmed value.

Independently on the programmed constant current value, the TIP and RING buffers have a current source capability limited to 70mA typ.

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Moreover the power available at Vbat is controlled by the DC/DC converter that limits the peak current drawn from the Vpos supply. The maximum allowed current peak is set by the RSENSE resistor and it is typically 900mApk.

AC CHARACTERISTICS

The SLIC core provides the standard SLIC transmission functions:

- **Input impedance synthesis:** can be real or complex and is set by a scaled (x50) external ZAC impedance.
- **Transmit and receive:** The AC signal present on the 2W port (TIP/RING) is transferred to the TX output with a -6dB gain and from the RX input to the 2W port with a 0dB gain.
- **2 to 4 wire conversion:** The balance impedance can be real or complex, the proper cancellation is obtained by means of two external impedance ZA and ZB.

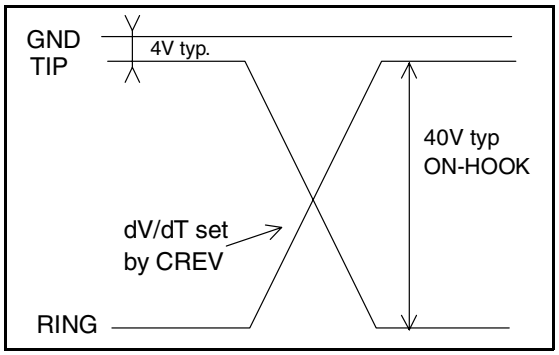
Once in Active mode (D1=1) the SLIC core can operate in different states setting properly D0 and D2 control bits (see also Table3).

D0	D1	D2	Operating state
0	1	0	Active Normal Polarity
0	1	1	Active Reverse Polarity
1	1	0	Active TTX injection (N.P.)
1	1	1	Active TTX injection (R.P.)

POLARITY REVERSAL

The D2 bit controls the line polarity, the transition between the two polarities is performed in a "soft" way. This means that the TIP and RING wire exchange their polarities following a ramp transition (see fig.4). The transition time is controlled by an external capacitor CREV. This capacitor is also setting the shape of the ringing trapezoidal waveform.

Figure 4. TIP/RING typical transition from Direct to Reverse Polarity



When the control pins set battery reversal the line polarity is reversed with a proper transition time set via an external capacitor (CREV).

METERING PULSE INJECTION (TTX)

The metering pulses circuit consist of a burst shaping generator that gives a square wave shaped and a low pass filter to reduce the harmonic distortion of the output signal.

The metering pulse is obtained starting from two logic signals:

- CKTTX: is a square wave at the TTX frequency (12 or 16KHz) and should be permanently applied to the CKTTX pin or at least for all the duration of the TTX pulse (including rising and decay phases).
- D0: enable the TTX generation circuit and define the TTX pulse duration.

This two signals are then processed by a dedicated circuitry integrated on chip that generate the metering pulse as an amplitude modulated shaped squarewave (SQTTX) (see fig.5).

Both the amplitude and the envelope of the squarewave (SQTTX) can be programmed by means of external components. In particular the amplitude is set by the two resistors RLV and the shaping by the capacitor CS.

The waveform so generated is then filtered and injected on the line. The low pass filter can be obtained using the integrated buffer OP1 connected between pin FTTX (OP1 non inverting input) and RTTX (OP1 output) (see fig.5) and implementing a "Sallen and Key" configuration.

Depending on the external components count it is possible to build an optimised application depending on the distortion level required. In particular harmonic distortion levels equal to 13%, 6% and 3% can be obtained respectively with first, second and third order filters (see fig.5).

The circuit shown in the "Application diagram" is related to the simple first order filter.

Once the shaped and filtered signal is obtained at RTTX buffer output it is injected on the TIP/RING pins with a +6dB gain.

It should be noted that this is the nominal condition obtained in presence of ideal TTX echo cancellation (obtained via proper setting of RTTX and CTTX). In addition the effective level obtained on the line will depend on the line impedance, the protection resistor value and the series switch (SW1 or SW2) on resistance.

In the typical application (TTX line impedance =200Ω , RP=41Ω, SW1,2 on resistance = 9Ω and ideal TTX echo cancellation) the metering pulse level on the line will be 1.33 times the level applied to the RTTX pin.

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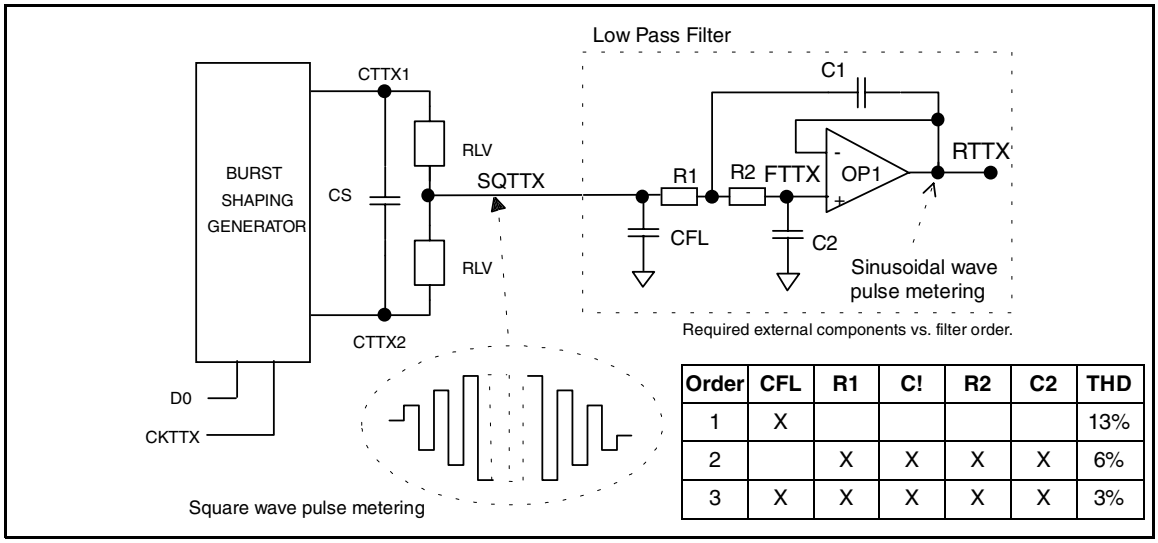
Figure 5. Metering pulse generation circuit.



Required external components vs. filter order.

Order	CFL	R1	C!	R2	C2	THD
1	X					13%
2		X	X	X	X	6%
3	X	X	X	X	X	3%

As already mentioned the metering pulse echo cancellation is obtained by means of two external components (RTTX and CTTX) that should match the line impedance at the TTX frequency. This simple network has a double effect:

- Synthesise a low output impedance at the TIP/RING pins at the TTX frequency.
- Cut the eventual TTX echo that will be transferred from the line to the TX output.

Ringing

D0	D1	D2	P1	P2	$\overline{DET}$	$\overline{DET1}$	$\overline{DET2}$
1	0	0/1 @fr	1	1	RTrip line 1+2	disable	disable
1	0	0/1 @fr	0	1	RTrip line 2	disable	disable
1	0	0/1 @fr	1	0	RTrip line 1	disable	disable

When this mode is selected STLC3065 self generate an higher negative battery (-70V typ.) in order to allow a balanced ringing signal of typically 62Vpeak.

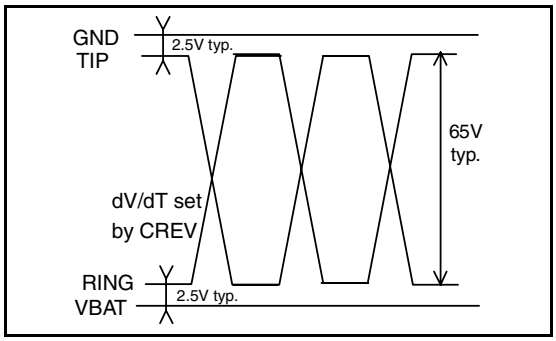
The SLIC core is set in ring mode via the control inputs D0 and D1 set respectively to 0 and 1.

In this condition both the DC and AC feedback loop are disabled and the SLIC core line drivers operate as voltage buffers.

The ring waveform is obtained toggling the D2 control bit at the desired ring frequency. This bit in fact controls the line polarity (0=direct; 1=reverse).

As in the ACTIVE mode the line voltage transition is performed with a ramp transition, obtaining in this way a trapezoidal balanced ring waveform (see fig.6).

Figure 6. TIP/RING typical ringing waveform



The shaping is defined by the CREV external capacitor.

Selecting the proper capacitor value it is possible to get different crest fattor values. The following table shows the crest factor values obtained with a 20Hz and 25Hz ring frequency and with 1REN. This value are valid either with European or USA specification:

CREV	CREST FACTOR @20Hz	CREST FACTOR @25Hz
22nF	1.2	1.26
27nF	1.25	1.32
33nF	1.33	Not significant (*)

(*)Distorsion already less than 10%.

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Depending on the P1,P2 control bits the ring waveform can be applied to both 2W ports (TIP1/RING1 and TIP2/RING2) or to one of the two (see also table2).

The ring trip detection is performed sensing the variation of the AC line impedance from on hook (relatively high) to off-hook (low). This particular ring trip method allows to operate without DC offset superimposed on the ring signal and therefore obtaining the maximum possible ring level on the load starting from a given negative battery.

It should be noted that such a method is optimised for operation on short loop applications and may not operate properly in presence of long loop applications (>500Ω).

Once ring trip is detected, the $\overline{DET}$ output is activated (logic level low), at this point the card controller or a simple logic circuit should stop the D2 toggling in order to effectively disconnect the ring signal and then set the STLC3065 in the proper operating mode (Normally ACTIVE).

RING LEVEL IN PRESENCE OF MORE TELEPHONE IN PARALLEL.

As already mentioned above the maximum current that can be drawn from the Vpos supply is controlled and limited via the external RSENSE.

This will limit also the power available at the self generated negative battery.

If for any reason the ringer load will be too high the self generated battery will drop in order to keep the power consumption to the fixed limit and therefore also the ring voltage level will be reduced.

In the typical application with RSENSE = 110mW the peak current from Vpos is limited to about 900mA, which correspond to an average current of 700mA max. In this condition the STLC3065 can drive up to 3REN with a ring frequency fr=25Hz (1REN = 1800Ω + 1.0μF, European standard).

In order to drive up to 5REN (1REN= 6930Ω + 8mF, US standard) it is necessary to modify the external components as follows:

CREV = 15nF

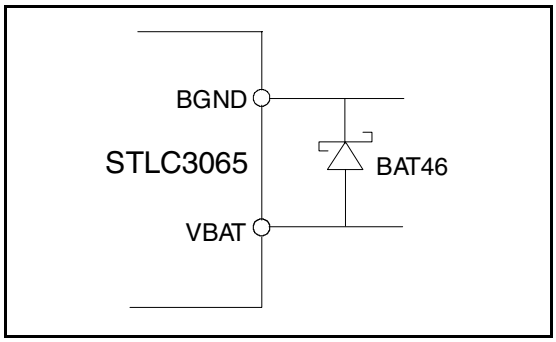
RD = 2.2 KΩ

Power On Requirements

In order to avoid damage to the device when Vpos is first applied it is recommended to keep all the logic inputs to a low logic level (0V) until Vpos is > 5.5V.

In case this power up sequence cannot be guaranteed, it's recommended to connect a shottky diode (BAT46 or equivalent) between VBAT and BGND (see figure 7).

Figure 7. Shottky diode connection



Layout Recommendation

A properly designed PCB layout is a basic issue to guarantee a correct behaviour and good noise performances.

Particular care must be taken on the ground connection and in this case the star configuration allows surely to avoid possible problems (see Application Diagram Fig. 8).

The ground of the power supply (VPOS) has to be connected to the center of the star, let's call this point PGND. This point should show a resistance as low as possible, that means it should be a ground plane.

Noise sources can be identified in not enough good grounds, not enough low impedance supplies and parasitic coupling between PCB tracks and high impedance pins of the device.

In particular, to avoid noise problems, layout should prevent any coupling between the DC/DC converter components and analog pins that are referred to AGND (ex: RD, IREF, RTH, RLIM, VF). As a first reccomendation the components CV, L, D1, CVPOS, RSENSE should be kept as close as possible to each other and isolated from the other components.

Additional improvements can be obtained:

decoupling the center of the star from the analog ground of STLC3065 using small chokes.

adding a capacitor in the range of 100nF between VPOS and AGND in order to filter the switch frequency on VPOS.

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External Components List

In order to properly define the external components value the following system parameters have to be defined:

- The AC input impedance shown by the SLIC at the line terminals "Zs" to which the return loss measurement is referred. It can be real (typ. 600Ω) or complex.
- The AC balance impedance, it is the equivalent impedance of the line "Zl" used for evaluation of the trans-hybrid loss performances (2/4 wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The line impedance at the TTX frequency "Zlttx".
- The metering pulse level amplitude measured at line termination "V_{LOTTX}". In case of low order filtering, V_{LOTTX} represents the amplitude (Vrms) of the fundamental frequency component. (typ 12 or 16KHz).
- Pulse metering envelope rise and decay time constant "t".
- The slope of the ringing waveform "$\Delta V_{TR/\Delta T}$".
- The value of the constant current limit current "Ilim".
- The value of the off-hook current threshold "I_{TH}".
- The value of the ring trip rectified average threshold current "I_{RTH}".
- The value of the required self generated negative battery "V_{BATR}" in ring mode (max value is 70V). This value can be obtained from the desired ring peak level +5V.
- The value of the maximum current peak sunk from Vpos "IPK".

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EXTERNAL COMPONENTS

Name	Function	Formula	Typ. Value
RREF	Bias setting current	RREF = 1.3/Ibias Ibias = 50µA	26kΩ 1%
CSVR	Negative Battery Filter	CSVR = 1/(2π · fp · 1.8MΩ) fp = 50Hz	1.5nF 10% 100VL
RD	Ring Trip threshold setting resistor	RD = 100/I_{RTH} 2KΩ < RD < 5KΩ	4.12kΩ 1% @ IRTH = 24mA
CAC	AC/DC split capacitance		22µF 20% 15VL @ RD = 4.12kΩ
RP	Line protection resistor	Rp > 30Ω	41Ω 1%
RS	Protection and series switches resistance image	RS = 100 · (Rp + 9Ω)	5kΩ @ Rp = 41Ω
ZAC	Two wire AC impedance	ZAC = 50 · (Zs - 2Rp - 18Ω)	25kΩ 1% @ Zs = 600Ω
ZA (1)	SLIC impedance balancing network	ZA = 50 · Zs	30kΩ 1% @ Zs = 600Ω
ZB (1)	Line impedance balancing network	ZB = 50 · Zl	30kΩ 1% @ Zl = 600Ω
CCOMP	AC feedback loop compensation	CCOMP = 1/(2π·fo·100·(RP+9Ω)) fo = 250kHz	120pF 10% 10VL @ Rp = 41Ω
CH	Trans-Hybrid Loss frequency compensation	CH = CCOMP	120pF 10% 10VL
RLIM	Current limiting programming	RLIM = 1300/Ilim 32.5kΩ < RLIM < 65kΩ	52.3kΩ 1% @ Ilim = 25mA
RTH	Off-hook threshold programming (ACTIVE mode)	RTH = 260/I_{TH} 27kΩ < RTH < 52kΩ	28.7kΩ 1% @I_{TH} = 9mA
CREV	Reverse polarity transition time programming	CREV = (1/3750) · $\Delta T/\Delta V_{TR}$)	22nF 10% 10V @ 12V/ms
RTTX (3)	Pulse metering cancellation resistor	RTTX = 50Re[(Zlttx+2Rp+18Ω)]	15kΩ @Zlttx = 200Ω real
CTTX (3)	Pulse metering cancellation capacitor	CTTX = 1/{50·2π·fttx[-Im(Zlttx)]}	100nF 10% 10V (2) @ Zlttx = 200Ω real
RLV	Pulse metering level resistor	RLV = $63.3 \cdot 10^3 \cdot \alpha \cdot V_{LOTTX}$ α = (|Zlttx + 2Rp + 18Ω|/|Zlttx|)	27kΩ 1% @ V_{LOTTX} = 275mVrms
CS	Pulse metering shaping capacitor	CS = τ/(2·RLV)	100nF 10% 10V @ τ = 6ms, RLV = 27.1kΩ
CFL	Pulse metering filter capacitor	CFL = 2/(2π·fttx·RLV)	1nF 10% 10V @fttx = 12kHz RLV = 27kΩ
RDD	Pull up resistors		100kΩ
CVCC	Internally supply filter capacitor		100nF 20% 10V
CVpos	Positive supply filter capacitor with low impedance for switch mode power supply		100µF(4)
CV	Battery supply filter capacitor with low impedance for switch mode power supply		100µF 20% 100V (5)
CVB	High frequency noise filter		470nF 20% 100VL

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EXTERNAL COMPONENTS (continued)

Name	Function	Formula	Typ. Value
CRD (6)	High frequency noise filter		100nF 10% 15VL
Q1	DC/DC converter switch P ch. MOS transistor	RDS(ON)≤1.2Ω,VDS = -100V Total gate charge=20nC max. with VGS=4.5V and VDS=1V ID>500mA	Possible choiches: IRF9510 or IRF9520 or IRF9120 or equivalent
D1	DC/DC converter series diode	Vr > 100V, $t_{RR} \leq 50ns$	SMBYW01-200 or equivalent
RSENSE	DC/DC converter peak current limiting	RSENSE = 100mV/I_{PK}	110mΩ @I_{PK} = 900mA
L (8)	DC/DC converter inductor	DC Resistance ≤ 0.1Ω (9)	L=125µH RFP1304PV (Manuf.: All Inductive) or SUMIDA CDRH125 or equivalent
CF1	DC/DC converter feedback loop stability		220pF to 470pF (10)
RF1	Negative battery programming level	250KΩ<RF1<300KΩ (7)	300kW 1% @ V_{BATR} = -70V
RF2	Negative battery programming level		9.1kΩ 1%

(1) In case Zs=Zl, ZA and ZB can be replaced by two resistors of same value: RA=RB=|Zs|.
(2) In this case CTTX is just operating as a DC decoupling capacitor (fp=100Hz).
(3) Defining ZTTX as the impedance of RTTX in series with CTTX, RTTX and CTTX can also be calculated from the following formula: ZTTX=50*(Zlttx+2Rp+18Ω).
(4) CVpos should be defined depending on the power supply current capability and maximum allowable ripple.
(5) For low ripple application use 2x47µF in parallel.
(6) Can be saved if proper PCB layout avoid noise coupling on RD pin (high impedance input).
(7) RF1 sets the self generated battery voltage in RING and ACTIVE(Il=0) mode as follows:

	267kΩ	280kΩ	294kW	300kΩ
$V_{BAT(ACTIVE)}$	-46V	-48V	-49V	-50V
$V_{BATR(RING)}$	-62V	-65V	-68V	-70V

VBATR should be defined considering the ring peak level required (Vringpeak=VBATR-6V typ.).
The above relation is valid provided that the Vpos power supply current capability and the RSENSE programming allow to source all the current requested by the particular ringer load configuration.
(8) Core: MICROMETALS T50-26C IRON POWDER, AL-VALUE 61nH/N2
Current rating: 2A (50/60Hz)
Operating Temperature -25° to +60° Centigrades
Inductance: 14µH +/-15% at 1KHz, 1mA
DC resistance of winding: MAX.100 mOhm
Code: RFY1303
Wire: UEW2, 0,60 mm
Turns: 50
Inductance (f=1KHz): >125µH
(9) For high efficiency in HI-Z mode coil resistance @125kHz must be <3ohm
(10) Function of this capacitor is to introduce a zero at the resonance frequency for loop stability. In case some parasitic resistance are already present in the loop (Coil, CVBAT, PCB layout), the presence of this capacitor can degrade the device noise performances; in this case CF1 should be removed being the loop stability already guaranteed by the parasitic resistance.

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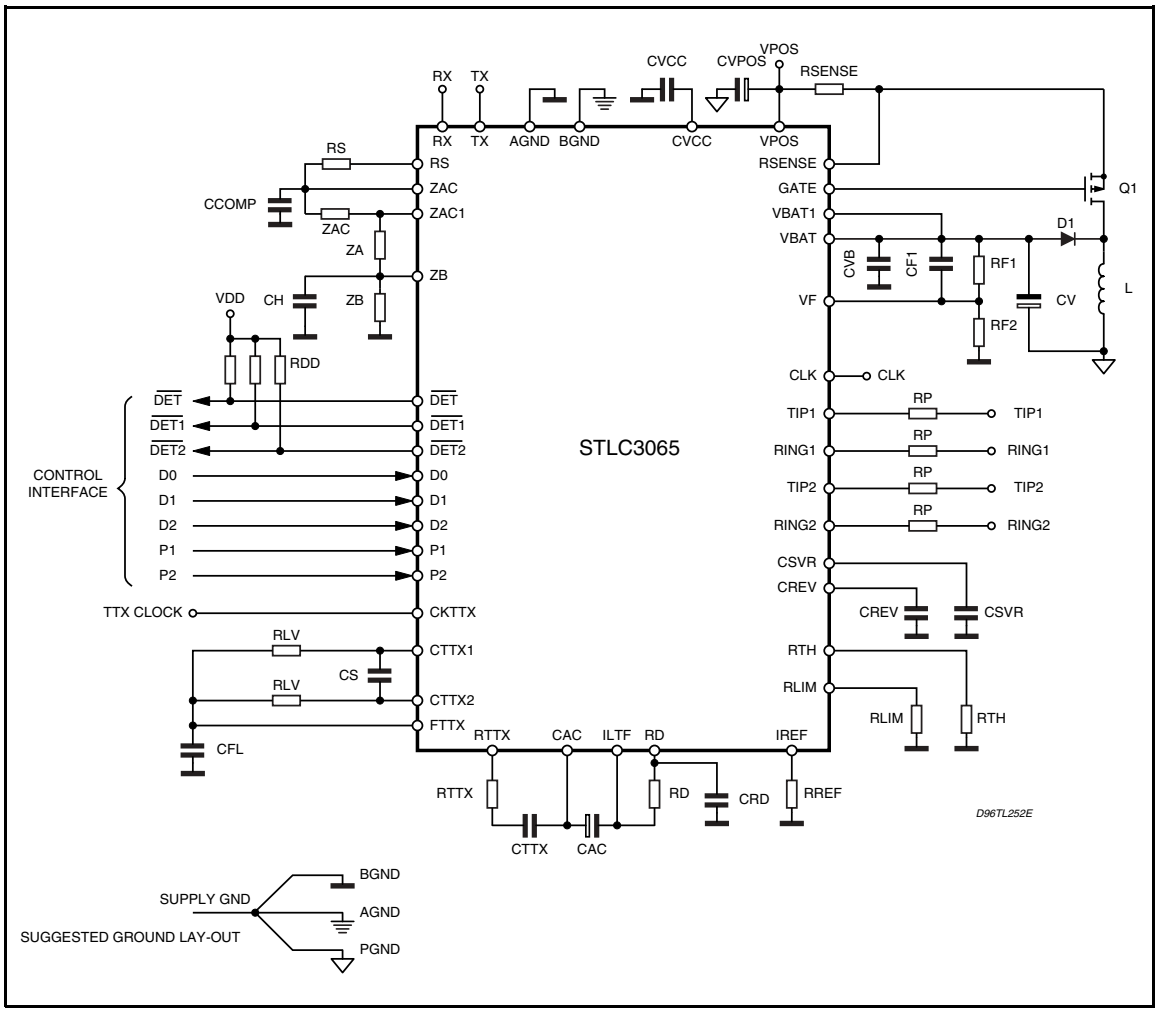
Figure 8. Application diagram.



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ELECTRICAL CHARACTERISTICS

Test conditions: V_{pos} = 6.0V, AGND = BGND, Normal Polarity, T_{amb} = 25°C.

External components as listed in the "Typical Values" column of EXTERNAL COMPONENTS Table.

Note: Testing of all parameter is performed at 25°C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85°C.

DC CHARACTERISTICS						
Symbol	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{lohi}	Line voltage	Il = 0, HI-Z (High impedance feeding) T_{amb} = 0 to 85°C	44	50		V
V_{lohi}	Line voltage	Il = 0, HI-Z (High impedance feeding) T_{amb} = -40 to 85°C	42	48		V
V_{loa}	Line voltage	Il = 0, ACTIVE T_{amb} = 0 to 85°C	33	40		V
V_{loa}	Line voltage	Il = 0, ACTIVE T_{amb} = -40 to 85°C	31	37		V
Ilim	Lim. current programming range	ACTIVE mode	20		40	mA
Ilima	Lim. current accuracy	ACTIVE mode. Rel. to programmed value 20mA to 40mA	-10		10	mA
Rfeed HI	Feeding resistance	HI-Z (High Impedance feeding)	2.4		3.6	kΩ
Zrx	RX port input impedance		280			kΩ
AC CHARACTERISTICS						
L/T	Long. to transv. (see Appendix for test circuit)	Rp = 41Ω, 1% tol., ACTIVE N. P., R_L = 600Ω (*) f = 300 to 3400Hz	48	50		dB
T/L	Transv. to long. (see Appendix for test circuit)	Rp = 41Ω, 1% tol., ACTIVE N. P., R_L = 600Ω (*) f = 300 to 3400Hz	40	45		dB
T/L	Transv. to long. (see Appendix for test circuit)	Rp = 41Ω, 1% tol., ACTIVE N. P., R_L = 600Ω (*) f = 1kHz	48	53		dB
2WRL	2W return loss	300 to 3400Hz, ACTIVE N. P., R_L = 600Ω (*)	22	26		dB
THL	Trans-hybrid loss	300 to 3400Hz, 20LogIVRX/VTXI, ACTIVE N. P., R_L = 600Ω (*)	30			dB
Ovl	2W overload level	at line terminals on ref. imped. ACTIVE N. P., R_L = 600Ω (*)	10			dBm
TXoff	TX output offset	ACTIVE N. P., R_L = 600Ω (*)	-150		150	mV
G24	Transmit gain abs.	0dBm @ 1020Hz, ACTIVE N. P., R_L = 600Ω (*)	-6.4		-5.6	dB
G42	Receive gain abs.	0dBm @ 1020Hz, ACTIVE N. P., R_L = 600Ω (*)	-0.4		0.4	dB
G24f	TX gain variation vs. freq.	rel. 1020Hz; 0dBm, 300 to 3400Hz, ACTIVE N. P., R_L = 600Ω (*)	-0.12		0.12	dB

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ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G42f	RX gain variation vs. freq.	rel. 1020Hz; 0dBm, 300 to 3400Hz, ACTIVE N. P., R_L = 600Ω (*)	-0.12		0.12	dB
V2Wp	Idle channel noise at line	psophometric filtered ACTIVE N. P., R_L = 600Ω (*) T_{amb} = 0 to +85°C		-73	-68	dBmp
V2Wp	Idle channel noise at line	psophometric filtered ACTIVE N. P., R_L = 600Ω (*) T_{amb} = -40 to +85°C		-68		dBmp
V4Wp	Idle channel noise at line	psophometric filtered ACTIVE N. P., R_L = 600Ω (*) T_{amb} = 0 to +85°C		-75	-70	dBmp
V4Wp	Idle channel noise at line	psophometric filtered ACTIVE N. P., R_L = 600Ω (*) T_{amb} = -40 to +85°C		-75		dBmp
Thd	Total Harmonic Distortion	ACTIVE N. P., R_L = 600Ω (*)			-46	dB
VTTX	Metering pulse level on line	ACTITIVE - TTX Zl = 200Ω fttx = 12kHz	200	250		mVrms
CLKfreq	CLK operating range		-10%	125	10%	kHz
AIS	Insolation between 2-wire ports	ACTIVE, odBm0 @ 1020Hz, R_L = 600Ω		-20		dB

(*) R_L: Line Resistance

RING						
Vring	Line voltage	RING D2 toggling @ fr = 25Hz Load = 3REN; Crest Factor = 1.25 1REN = 1800Ω + 1.0µF T_{amb} = 0 to +85°C	45	49		Vrms
Vring	Line voltage	RING D2 toggling @ fr = 25Hz Load = 3REN; Crest Factor = 1.25 1REN = 1800Ω + 1.0µF T_{amb} = -40 to +85°C	44	48		Vrms
LIS	Insolation between 2-wire ports	RING Mode on Port1			-50	dBmp
DETECTORS						
IOFFTHA	Off/hook current threshold	ACT. mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFTHA	Off/hook loop resistance threshold	ACT. mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)			3.4	kΩ
IONTHA	On/hook current threshold	ACT. mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHA	On/hook loop resistance threshold	ACT. mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)	8			kΩ
IOFFTHI	Off/hook current threshold	Hi Z mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFFTHI	Off/hook loop resistance threshold	Hi Z mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)			800	Ω

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ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IONTHI	On/hook current threshold	Hi Z mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHI	On/hook loop resistance threshold	Hi Z mode, RTH = 28.7kΩ 1% (Prog. ITH = 9mA)	8			kΩ
Irt	Ring Trip detector threshold range	RING	20		50	mA
Irta	Ring Trip detector threshold accuracy	RING	-15		15	%
Trtd	Ring trip detection time	RING		TBD		ms
Td	Dialling distortion	ACTIVE	-1		1	ms
Rlrt (1)	Loop resistance				500	Ω
ThAl	Tj for th. alarm activation			160		°C

(1) Rlrt = Maximum loop resistance (incl. telephone) for correct ring trip detection.

DIGITAL INTERFACE INPUTS: D0, D1, D2, P1, P2,CLK OUTPUTS: DET, DET1, DET2						
Vih	In put high voltage		2			V
Vil	Input low voltage				0.8	V
Iih	Input high current		-10		10	µA
Iil	Input low current		-10		10	µA
Vol	Output low voltage	Iol = 1mA			0.45	V
PSRR AND POWER CONSUMPTION						
PSRRC	Power supply rejection Vpos to 2W port	Vripple = 100mVrms 50 to 4000Hz	26	36		dB
Ivpos	Vpos supply current @ ii = 0	HI-Z On-Hook ACTIVE On-Hook, RING (line open)		52 93 120	60 115 140	mA mA mA
Ipk	Peak current limiting accuracy	RING Off-Hook RSENSE = 110mΩ	-20%	950	+20%	mApk

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APPENDIX A

STLC3065 Test Circuits

Referring to the application diagram shown in fig. 8 of the STLC3065 datasheet and using as external components the Typ. Values specified in the "External Components" Table (page 16) find below the proper configuration for each measurement.

All measurements requiring DC current termination should be performed using "Wandel & Goltermann DC Loop Holding Circuit GH-1" or equivalent.

Figure A1. 2W Return Loss
2WRL = 20Log(\|Zref + Zs\|/\|Zref-Zs\|) = 20Log(E/2Vs)

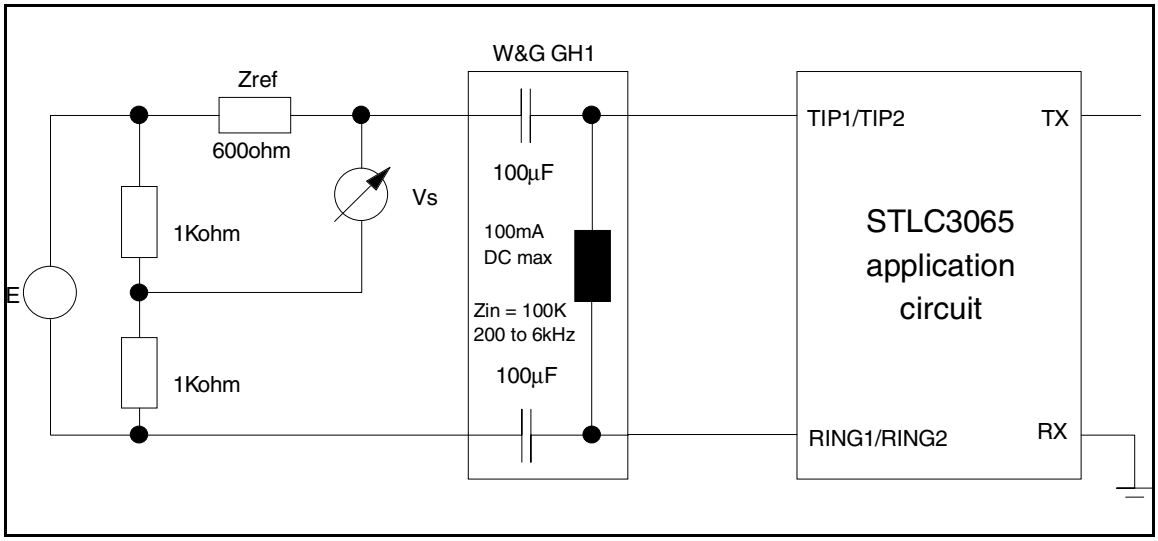

Figure A2. THL Trans Hybrid Loss
THL = 20Log\|Vrx/Vtx\|

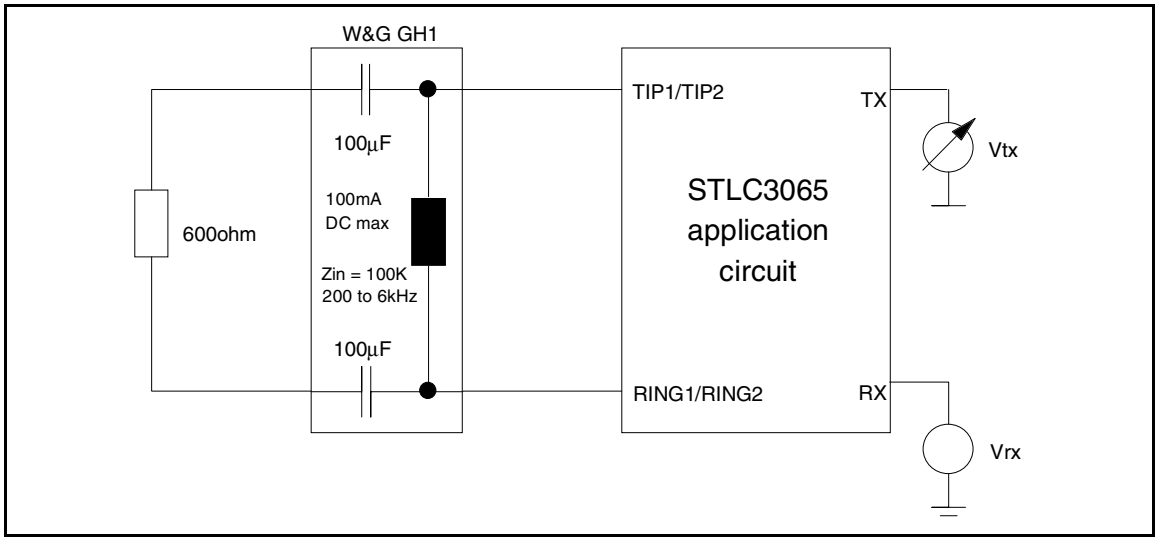

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Figure A3. G24 Transmit Gain
G24 = 20Log\|2Vtx/E\|

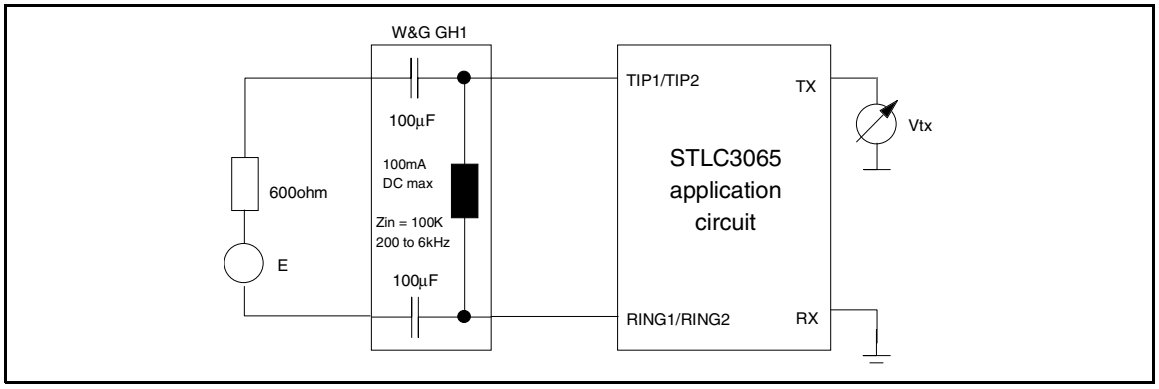

Figure A4. G42 Receive Gain
G42 = 20Log\|Vl/Vrx\|

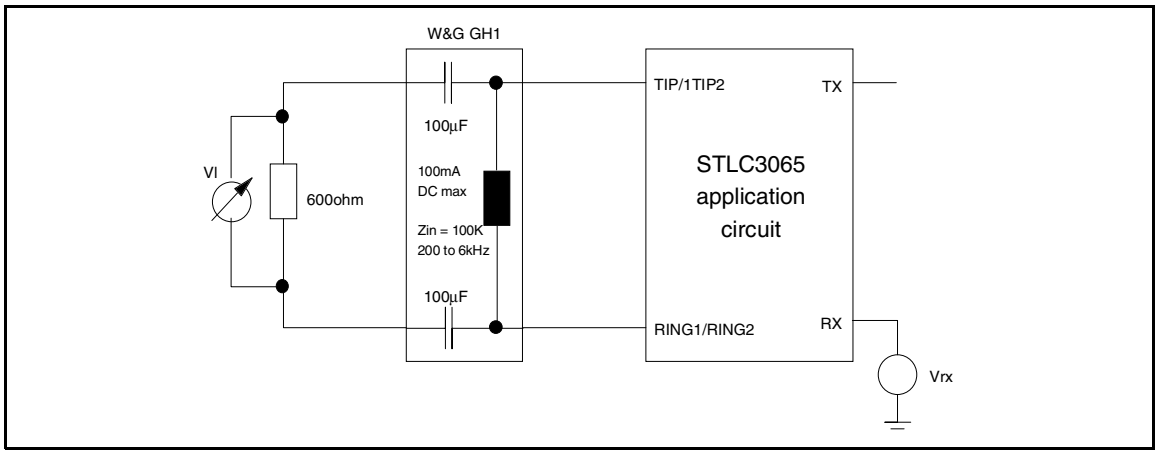

Figure A5. PSRRC Power supply rejection Vpos to 2W port
PSSRC = 20Log\|Vn/Vl\|

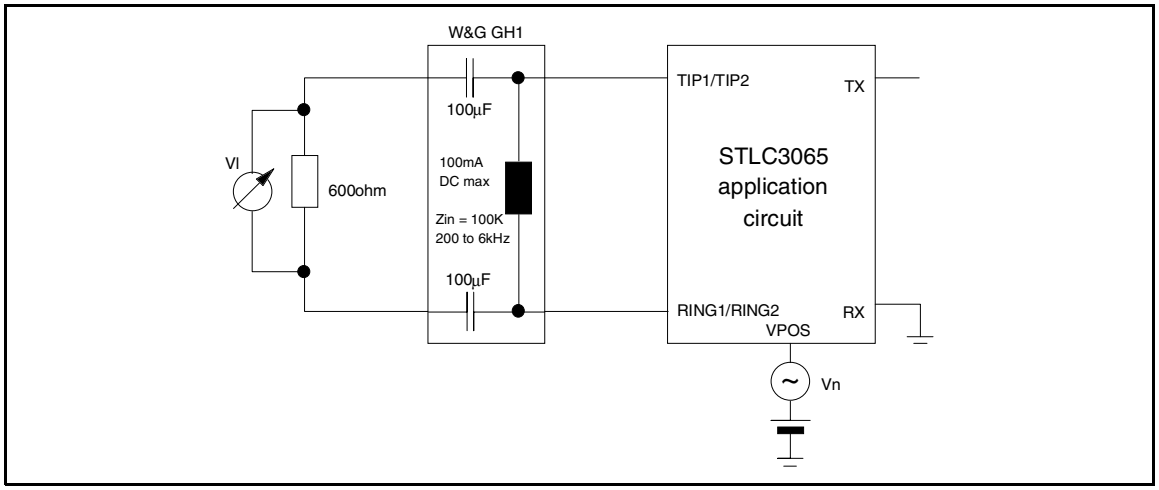

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Figure A6. L/T Longitudinal to Transversal Conversion
L/T = 20Log\|Vcm/Vl\|

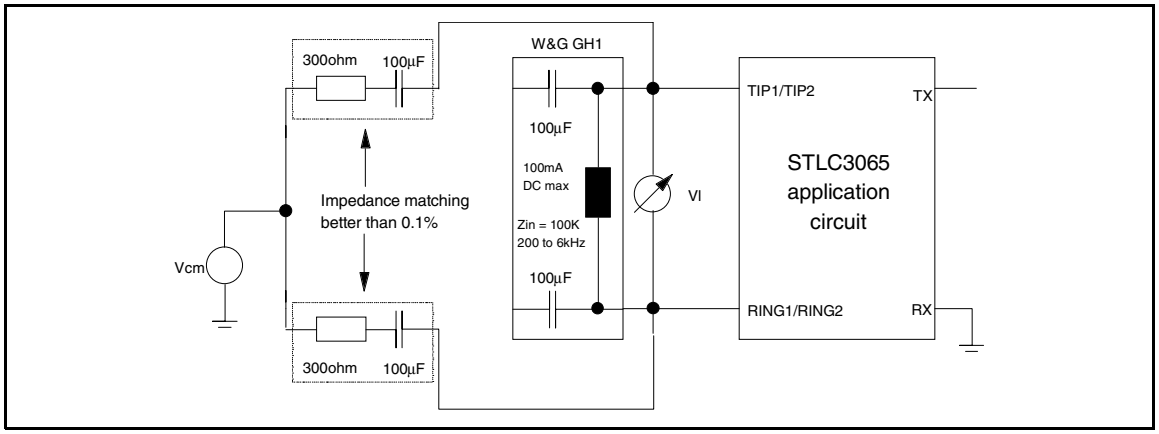

Figure A7. T/L Transversal to Longitudinal Conversion
T/L = 20Log\|Vrx/Vcm\|

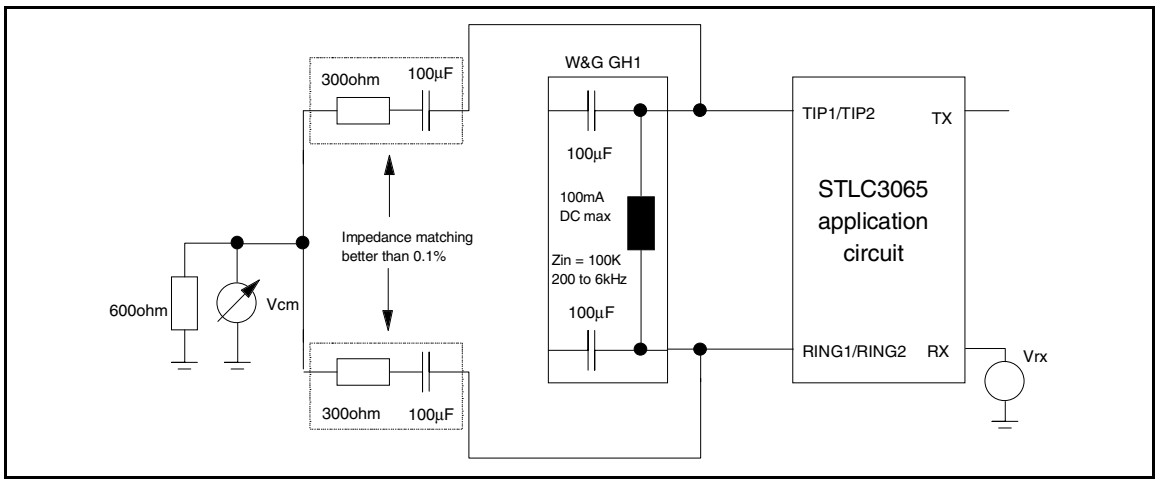

Figure A8. VTTX Metering Pulse level on line

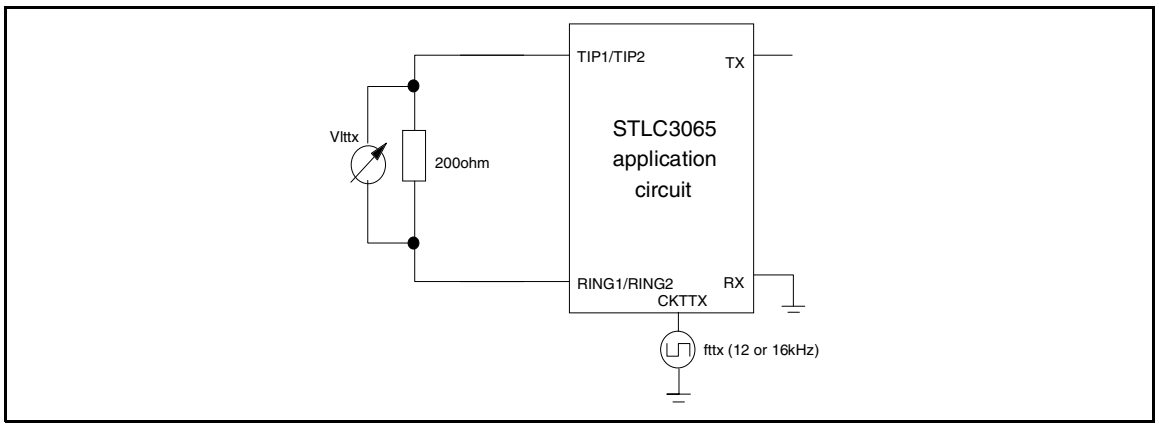

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Figure A9. V2Wp and W4Wp: Idle channel psophometric noise at line and TX.
V2Wp = 20Log\|Vl/0.774l\|; V4Wp = 20Log\|Vtx/0.774l\|

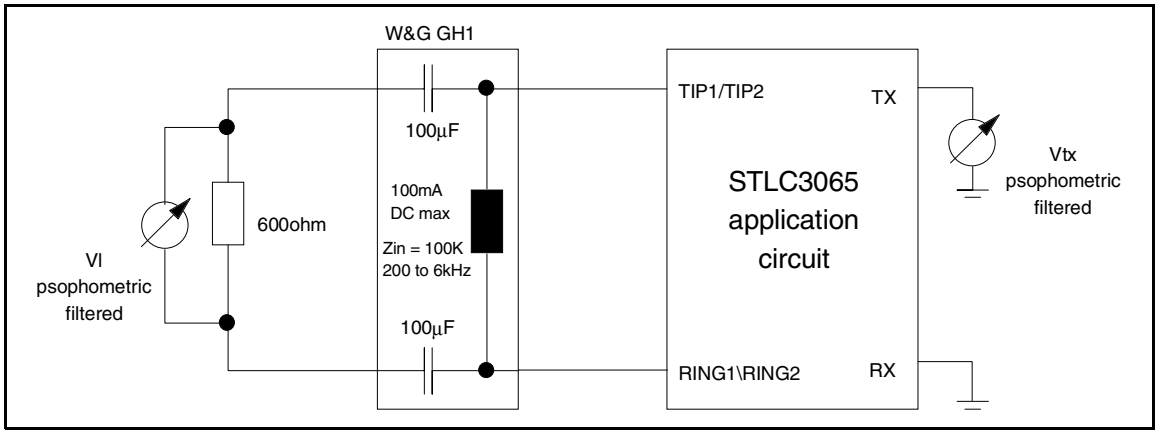

Figure A10. AIS Isolation between 2 wire ports
AIS = 20Log\|Vais/Vl\|

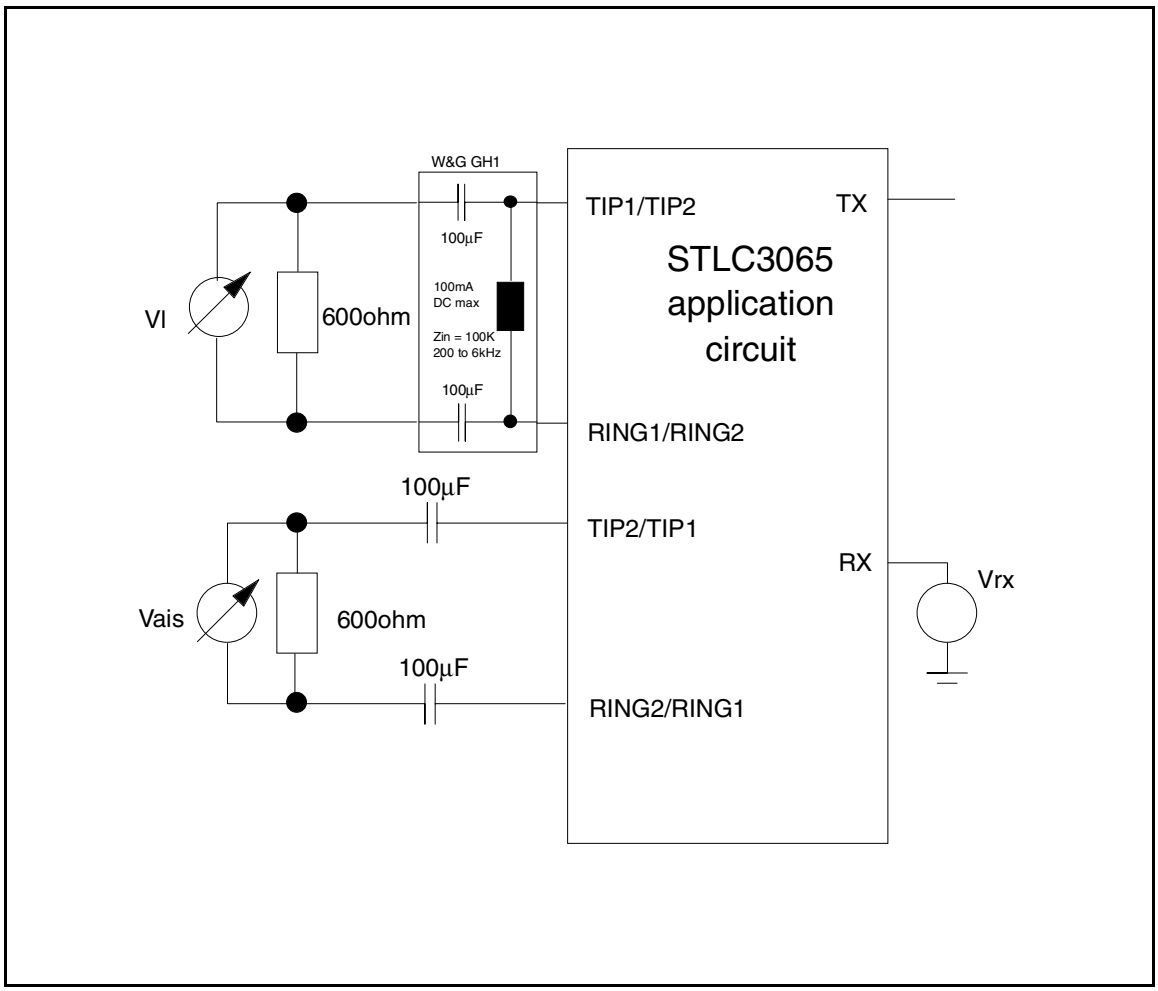

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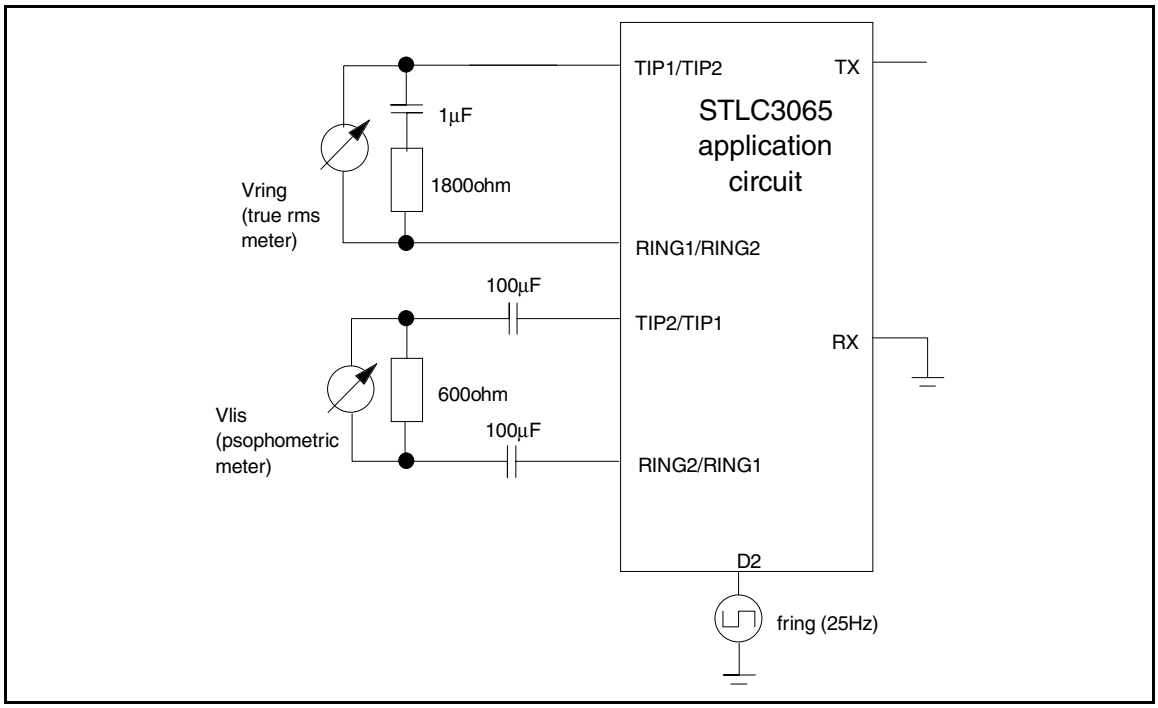
Figure A11. Vring, Vlis: Ring Voltage and port isolation



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APPENDIX B

STLC3065 OVERVOLTAGE PROTECTION

Figure B1. Simplified configuration for indoor overvoltage protection

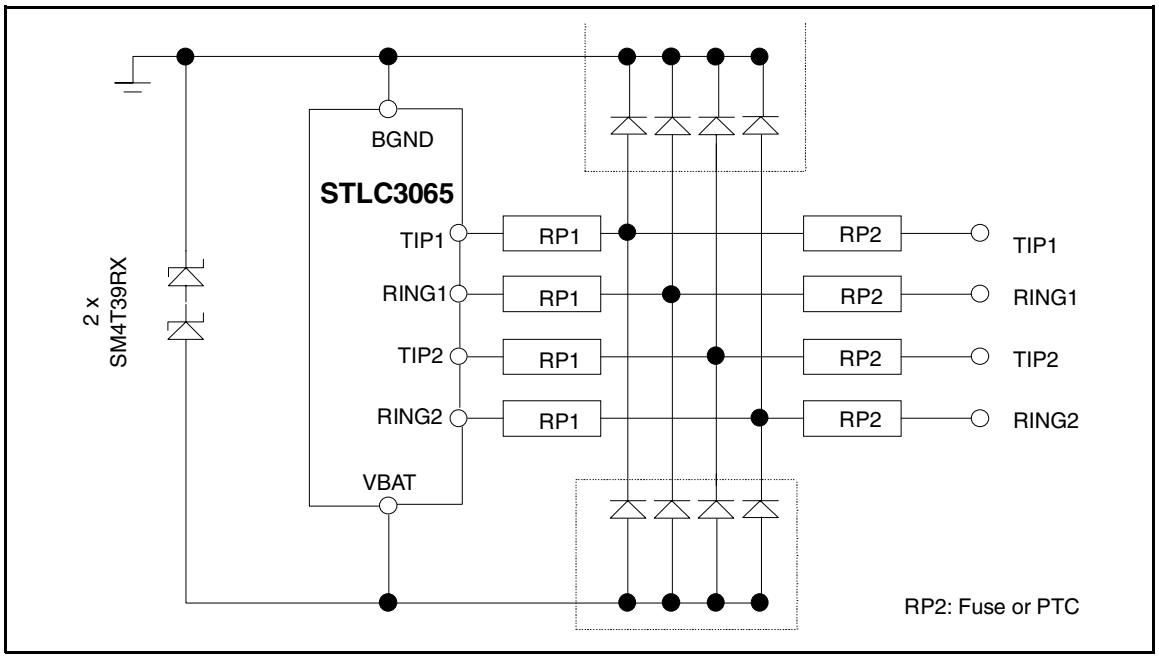
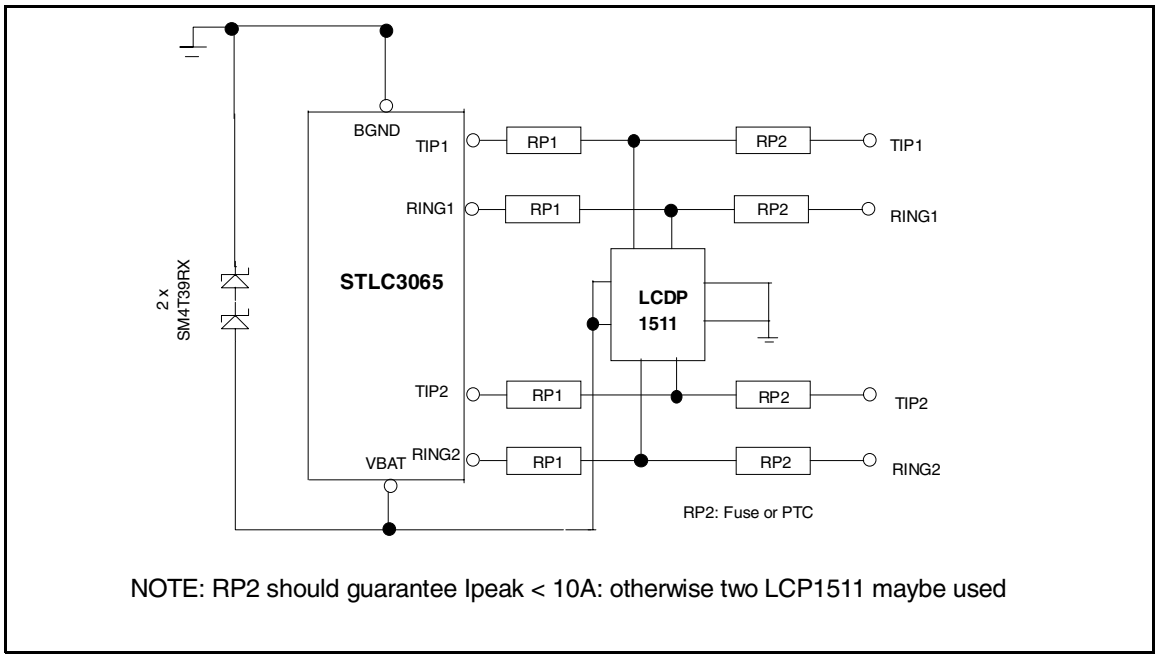


Figure B2. Standard overloltage protection configuration for k20 compliance



NOTE: RP2 should guarantee Ipeak < 10A: otherwise two LCP1511 maybe used

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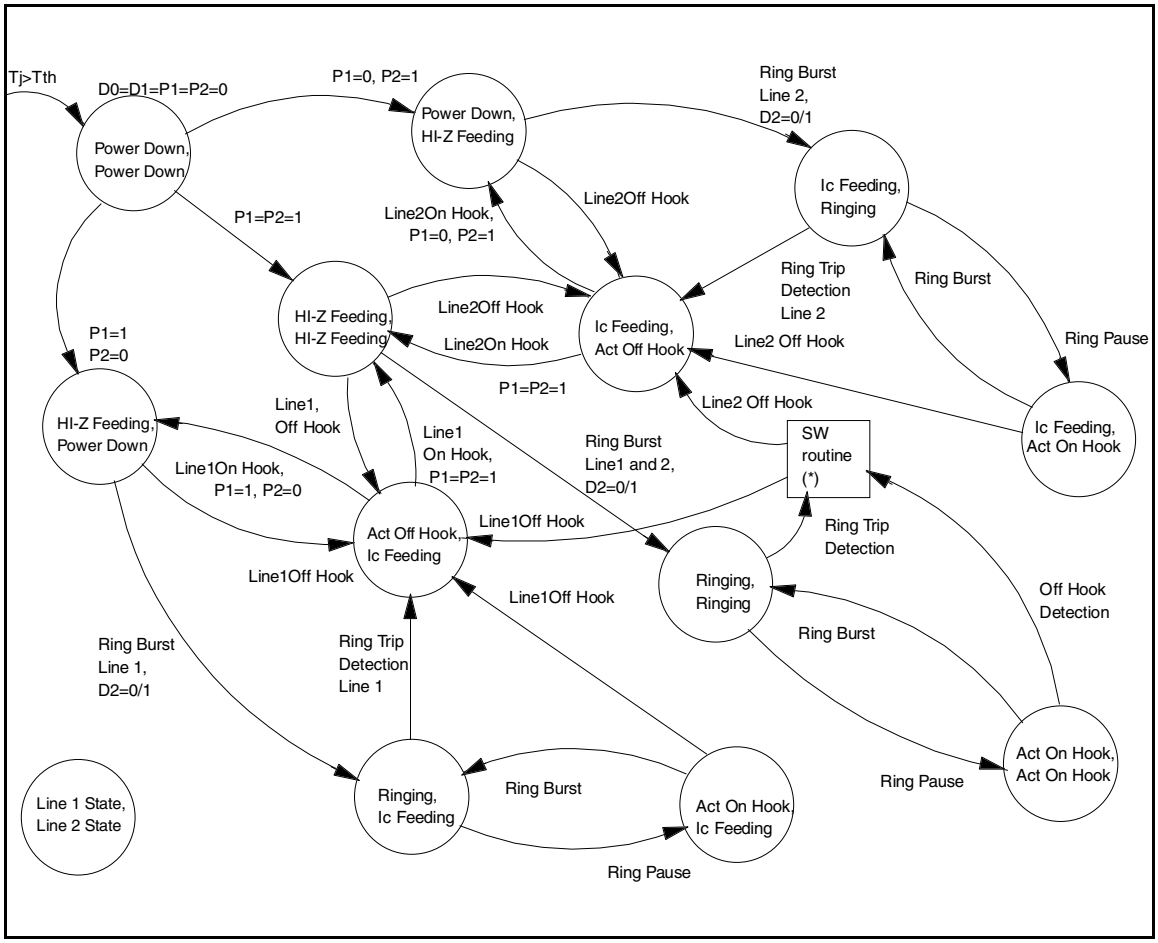
APPENDIX C

Figure C1. Typical state diagram for the STLC3065 operation



Note: all state transitions are under the microprocessor control.

(*) = When the ringing signal is sent to both lines, the STLC3065 is not able to detect the answering line. To detect the answering line, a SW routine is needed that disables first the line 1 (forcing P1=0) and then the line 2 (forcing P2=0) so as to detect which line is in Off Hook condition.

The On Hook condition is declared when it persists for T>Tref.

Ic Feeding state is referred to a constant feeding current applied to the local loop and equal to 300µA.

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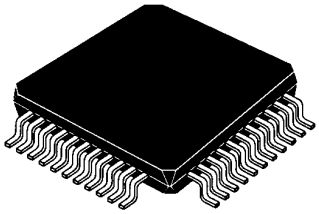
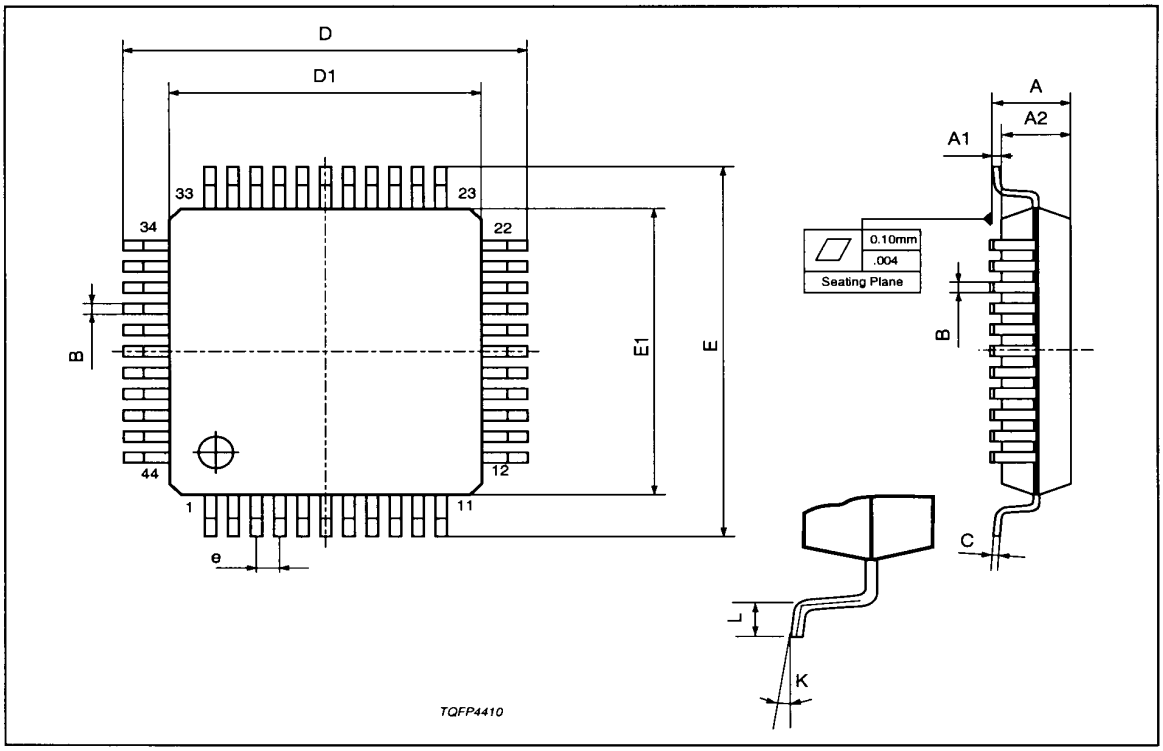
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10)



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