Data Sheet, DS2, July 2000

DuSLIC

Dual Channel Subscriber Line Interface Circuit

PEB 3264/-2 Version 1.2
PEB 4264/-2 Version 1.1
PEB 3265 Version 1.2
PEB 4265/-2 Version 1.1
PEB 4266 Version 1.1

Wired
Communications

Never stop thinking.

Edition 2000-07-14

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DuSLIC
Preliminary
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Page	Subjects (major changes since last revision)
Page 15	Usage of the term *SLICOFI-2x* as synonym used for all codec versions SLICOFI-2/-2S/-2S2.
Page 33	**Chapter 3.1** "Functional Overview" completely updated.
Page 94	**Chapter 4.7.2** "Power Dissipation of SLICOFI-2": Power dissipation tables were replaced by cross-references to **Chapter 7**.
Page 107	**Chapter 4.8** "Integrated Test and Diagnosis Functions" replaces the former chapter "Test Modes".
Page 132	**Chapter 4.9** "Signal Path and Test Loops": updated figures.
Page 137	**Chapter 4.10** "Caller ID Buffer Handling of SLICOFI-2" added.
Page 162	**Figure 70** "Interface SLICOFI-2 and SLIC-P": Pin IO1A on PEB 3265 was replaced by pin IO2A.
Page 174	Register XCR: Bit PLL-LOOP removed.
Page 204	Register LMCR2: Description for bit LM-NOTCH changed.
Page 228	**Chapter 6.2.3** "POP Commands": General update and partially renaming of POP commands.
Page 317	**Chapter 7**: Electrical characteristics and AC transmission performance completely updated.
Page 342	**Chapter 7.4.6** "Digital Interface": Test condition current I_0 for Low-output voltage V_{OLDU} for PEB 3264/-2 was lowered to $I_0 = -30$ mA.
Page 367	**Chapter 8** "Application Circuits" completely overworked.

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Preliminary

Preface

This document describes the DuSLIC chip set comprising a programmable dual channel *SLICOFI-2x* codec and two single channel high-voltage SLIC chips. For more DuSLIC related documents please see our webpage at http://www.infineon.com/duslic.

To simplify matters, the following synonyms are used:

SLICOFI-2x:	Synonym used for all codec versions SLICOFI-2/-2S/-2S2
SLIC:	Synonym used for all SLIC versions SLIC-S/-S2, SLIC-E/-E2 and SLIC-P

Organization of this Document

This Data Sheet is divided into eleven chapters. It is organized as follows:

- Chapter 1, Overview
  A general description of the product, its key features, and some typical applications.
- Chapter 2, Pin Descriptions
- Chapter 3, Functional Description
  The main functions are presented following a functional block diagram.
- Chapter 4, Operational Description
  A brief description of the three operating modes: power down, active and ringing (plus signal monitoring techniques).
- Chapter 5, Interfaces
  Connection information including standard IOM-2 and PCM interface timing frames and pins.
- Chapter 6, *SLICOFI-2x* command structure
  A general brief about the *SLICOFI-2x* command structure.
- Chapter 7, Electrical Characteristics
  Parameters, symbols and limit values.
- Chapter 8, Application Circuits
  External components and layout recommendations. Illustrations of balanced ringing, unbalanced ringing and protection circuits.
- Chapter 9, Package Outlines
  Illustrations and dimensions of the package outlines.
- Chapter 10, Glossary
  List of abbreviations and description of symbols.
- Chapter 11, Index

1 Overview

DuSLIC is a chip set, comprising one dual channel *SLICOFI-2x* codec and two single channel SLIC chips. It is a highly flexible codec/SLIC solution for an analog line circuit and is widely programmable via software. Users can now serve different markets with a single hardware design that meets all different standards worldwide.

The interconnections between the single channel high-voltage SLIC and the dual channel *SLICOFI-2x* codec (advanced CMOS process) ensure a seamless fit. This guarantees maximum transmission performance with minimum line circuit component count.

DuSLIC family chip sets:

Table 1 DuSLIC Chip Sets

Chip Set	**DuSLIC-S**	**DuSLIC-S2**	**DuSLIC-E**	**DuSLIC-E2**	**DuSLIC-P**
Marketing Name	SLICOFI-2S/ SLIC-S	SLICOFI-2S2/ SLIC-S2	SLICOFI-2/ SLIC-E	SLICOFI-2/ SLIC-E2	SLICOFI-2/ SLIC-P
Product ID	PEB 3264/ PEB 4264	PEB 3264-2/ PEB 4264-2(1)	PEB 3265/ PEB 4265	PEB 3265/ PEB 4265-2(2)	PEB 3265/ PEB 4266
Longitudinal Balance	53 dB	60 dB	53 dB	60 dB	53 dB
Maximum DC feeding	32 mA	50 mA	32 mA	50 mA	32 mA
Neg. Battery Voltages	2	2	2	2	2/3
Add. positive Voltages	1	1	1	1	0
Internal Ringing	45 Vrms	no	85 Vrms	85 Vrms	85 Vrms bal., 50 Vrms unbal.
ITDF(3)	no	no	yes	yes	yes
TTX	1.2 Vrms	no	2.5 Vrms	2.5 Vrms	2.5 Vrms
Add-Ons(4)	no	no	yes	yes	yes

(1) Nevertheless marked on the chip as PEB 4264

(2) Nevertheless marked on the chip as PEB 4265

(3) Integrated Test and Diagnosis Functions

(4) The add-on functions are DTMF detection, Caller ID generation, Message Waiting lamp support, Three Party Conferencing, Universal Tone Detection (UTD), Line Echo Cancellation (LEC) and Sleep Mode.

The DuSLIC family comprises five different chip sets (see **Table 1**):

- Three basic DuSLIC chip sets optimized for different applications:
  DuSLIC-S (Standard),
  DuSLIC-E (Enhanced),
  DuSLIC-P (Power Management).
- Two different performance versions of the basic DuSLIC-E and DuSLIC-S chip sets:
  DuSLIC-E2 (using SLIC-E2 PEB 4265-2 compared to DuSLIC-E)
  DuSLIC-S2 (using SLIC-S2 PEB 4264-2 and codec PEB 3264-2)

The codec devices SLICOFI-2, SLICOFI-2S and SLICOFI-2S2 are manufactured in an advanced 0.35 µm 3.3 V CMOS process.

The SLIC-E, SLIC-E2 and SLIC-P devices are manufactured in Infineon Technologies robust and well proven 170 V Smart Power technology.

The SLIC-S and SLIC-S2 devices are manufactured in Infineon Technologies 90 V Smart Power technology and offer further cost reduction.

Usage of Codec´s and SLIC´s:

DuSLIC-E, DuSLIC-E2 and DuSLIC-P comprise the same SLICOFI-2 codec with full EDSP (Enhanced Digital Signal Processor) features like DTMF detection, Caller ID generation, Universal Tone Detection (UTD) and Line Echo Cancellation.

DuSLIC-S comprises the SLICOFI-2S codec without EDSP features.

DuSLIC-S2 comprises the SLICOFI-2S2 codec based on the SLICOFI-2S but without Teletax metering (TTX) and internal ringing capability.

The respective SLIC variant for each chip set featured in **Table 1** has been selected according to performance and application requirements:

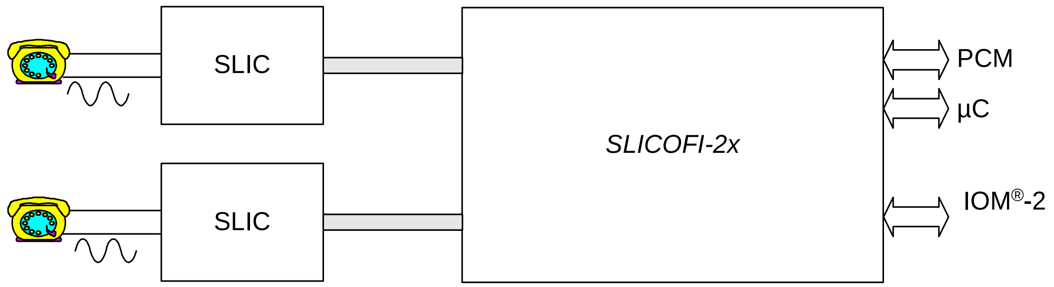
SLIC-S/-S2 (PEB 4264 / PEB 4264-2) and SLIC-E/-E2 (PEB 4265 / PEB 4265-2) are optimized for access network requirements, while the power management SLIC-P (PEB 4266) is an enhanced version for extremely power-sensitive applications or for applications where internal unbalanced ringing is required.

DuSLIC Architecture

Unlike traditional designs, DuSLIC splits the SLIC function into high-voltage SLIC functions and low-voltage SLIC functions.

The low-voltage functions are handled in the *SLICOFI-2x* device. The partitioning of the functions is shown in **Figure 1**.

For further information see **Chapter 3.1**.



HV SLIC Functions

- Voltage feeding
- Transversal current sensing
- Longitudinal current sensing
- Overload protection
- Battery switching
- Ring amplification
- On-hook transmission
- Polarity reversal

LV SLIC Functions

- Programmable DC feeding
- Ring generation
- Supervision
- Teletax generation
- Teletax notch filter
- Ring trip detection
- Ground key detection
- Hook switch detection

Codec Filter Functions

- Filtering
- PCM compression/expansion
- Programmable gain
- Programmable frequency
- Impedance matching
- Hybrid balance
- DTMF generation
- DTMF detection
- FSK generation (Caller ID)
- Linear mode support (16-bit uncompressed voice data)
- IOM-2 and PCM/µC interface
- Integrated Test and Diagnosis Functions (IDTF)
- Line Echo Cancelling (LEC)
- Universal Tone Detection (UTD)
- Three-party conferencing
- Message waiting lamp support

ezm14034.wmf

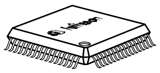
Figure 1 DuSLIC Chip Set

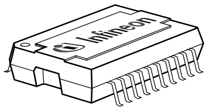
Dual Channel Subscriber Line Interface Circuit
DuSLIC

PEB 3264/-2
PEB 3265
PEB 4264/-2
PEB 4265/-2
PEB 4266

Version 1.2

1.1 Features


P-MQFP-64-1,-2


P-DSO-20-5

- Internal unbalanced/balanced ringing capability up to 85 Vrms
- Programmable Teletax (TTX) generation
- Programmable battery feeding with capability for driving longer loops
- Fully programmable dual-channel codec
- Ground/loop start signaling
- Polarity reversal
- Integrated Test and Diagnosis Functions (IDTF)
- On-hook transmission
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID (FSK) generator
- Integrated fax/modem detection (Universal Tone Detection (UTD))
- Integrated Line Echo Cancellation unit (LEC)
- Optimized filter structure for modem transmission
- Three-party conferencing (in PCM/µC mode)
- Message waiting lamp support (PBX)
- Power optimized architecture
- Power management capability (integrated battery switches)
- 8 and 16 kHz PCM Transmission
- Specification in accordance with
  ITU-T Recommendation Q.552 for interface Z and applicable LSSGR

Type	Package
PEB 3264/-2	P-MQFP-64-1
PEB 4264/-2	P-DSO-20-5
PEB 3265	P-MQFP-64-1
PEB 4265/-2	P-DSO-20-5
PEB 4266	P-DSO-20-5

1.2 Logic Symbols

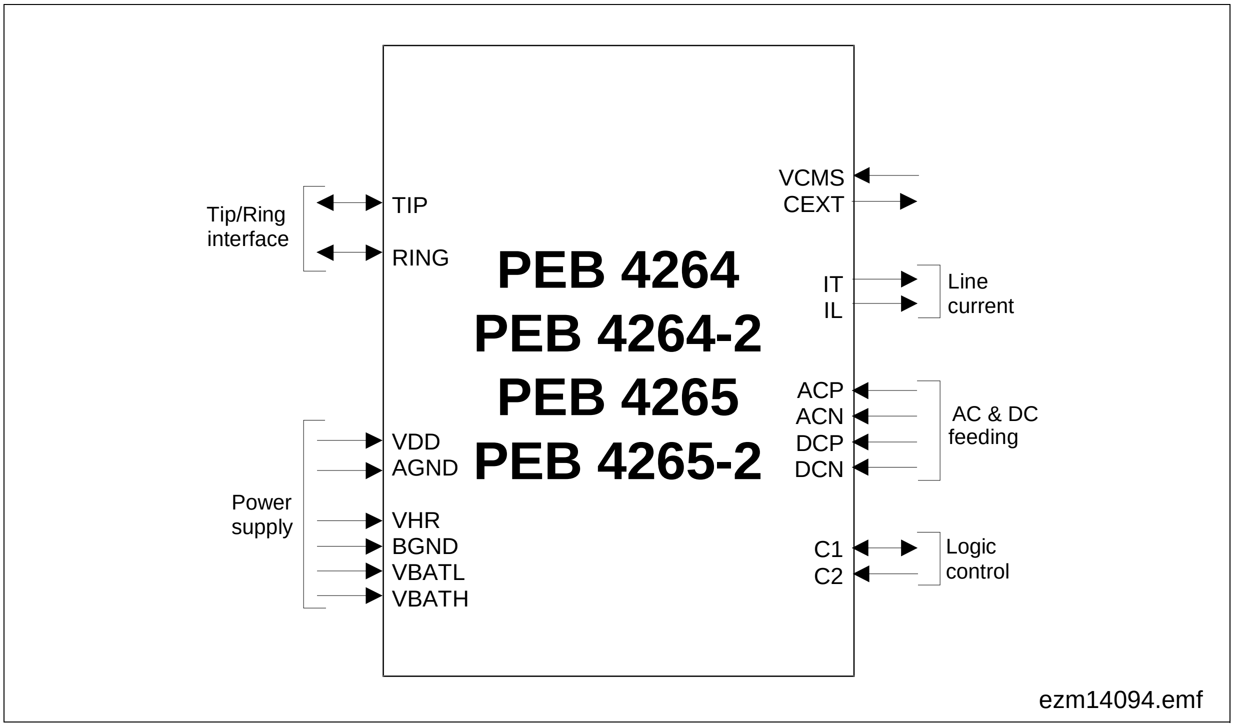

PEB 4264
PEB 4264-2
PEB 4265
PEB 4265-2
Tip/Ring interface
TIP
RING
Power supply
VDD
AGND
VHR
BGND
VBATL
VBATH
VCMS
CEXT
IT
IL
Line current
ACP
ACN
DCP
DCN
AC & DC feeding
C1
C2
Logic control
ezm14094.emf

Figure 2 Logic Symbol SLIC-S / SLIC-S2 / SLIC-E / SLIC-E2

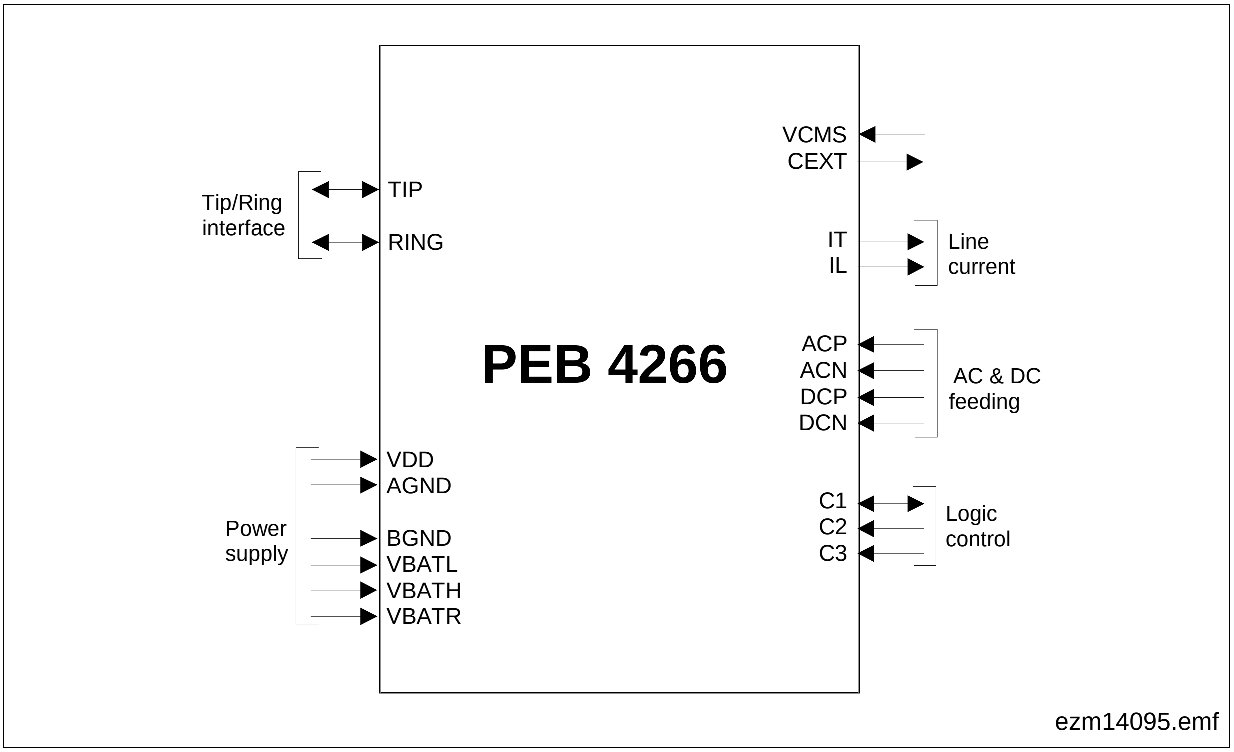

PEB 4266
Tip/Ring interface
TIP
RING
Power supply
VDD
AGND
BGND
VBATL
VBATH
VBATR
VCMS
CEXT
IT
IL
Line current
ACP
ACN
DCP
DCN
AC & DC feeding
C1
C2
C3
Logic control
ezm14095.emf

Figure 3 Logic Symbol SLIC-P

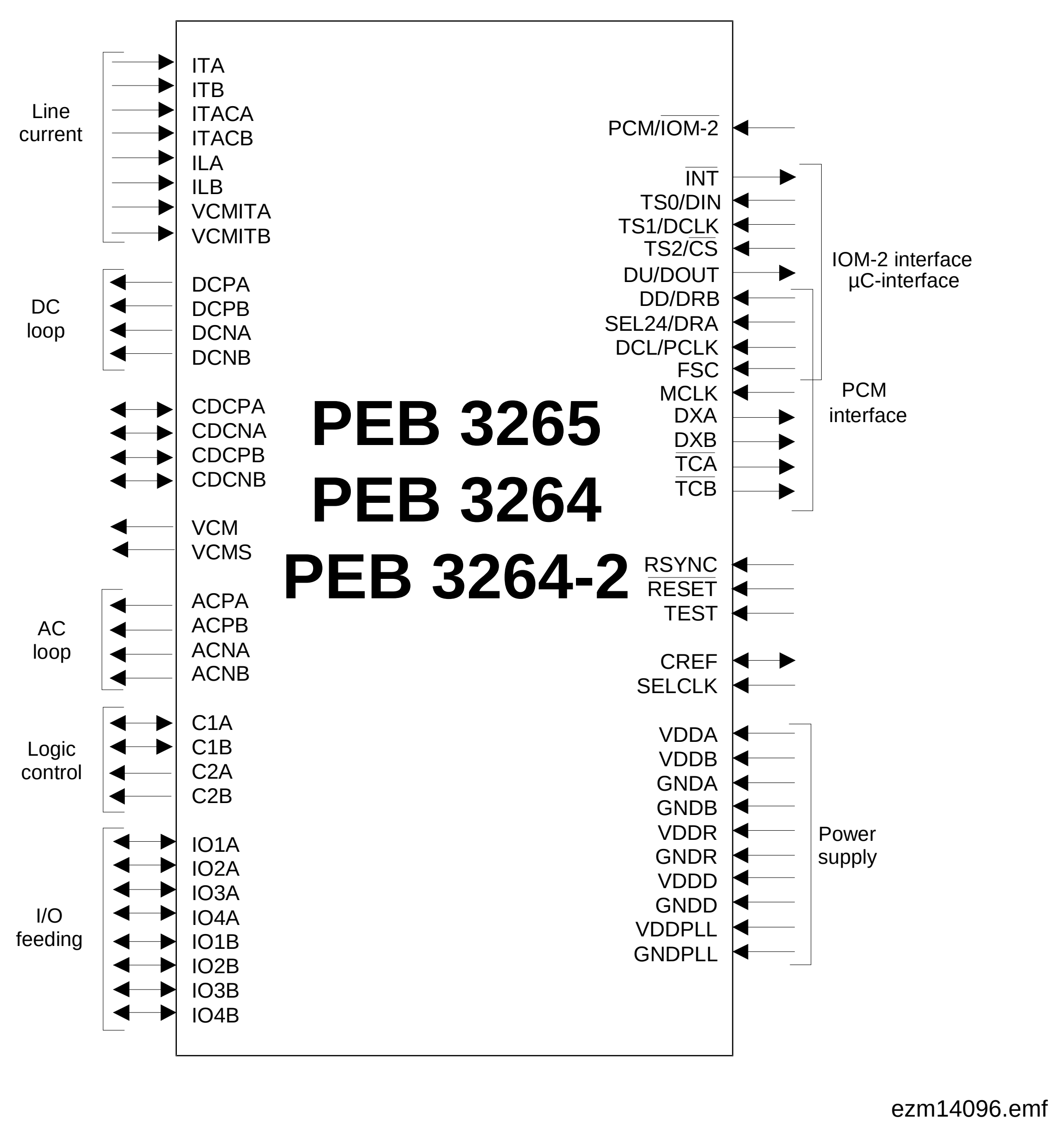

Line
current
ITA
ITB
ITACA
ITACB
ILA
ILB
VCMITA
VCMITB
DC
loop
DCPA
DCPB
DCNA
DCNB
CDCPA
CDCNA
CDCPB
CDCNB
VCM
VCMS
AC
loop
ACPA
ACPB
ACNA
ACNB
Logic
control
C1A
C1B
C2A
C2B
I/O
feeding
IO1A
IO2A
IO3A
IO4A
IO1B
IO2B
IO3B
IO4B
PEB 3265
PEB 3264
PEB 3264-2
PCM/IOM-2
INT
TS0/DIN
TS1/DCLK
TS2/CS
DU/DOUT
DD/DRB
SEL24/DRA
DCL/PCLK
FSC
MCLK
DXA
DXB
TCA
TCB
IOM-2 interface
µC-interface
PCM
interface
RSYNC
RESET
TEST
CREF
SELCLK
VDDA
VDDB
GNDA
GNDB
VDDR
GNDR
VDDD
GNDD
VDDPLL
GNDPLL
Power
supply
ezm14096.emf

Figure 4 Logic Symbol SLICOFI-2/-2S/-2S2

1.3 Typical Applications

- Digital Loop Carrier (DLC)
- Wireless Local Loop
- Fiber in the Loop
- Private Branch Exchange
- Intelligent NT (Network Termination) for ISDN
- ISDN Terminal Adapter
- Central Office
- Cable Modem
- XDSL NT
- Router

2 Pin Descriptions

2.1 Pin Diagram SLIC

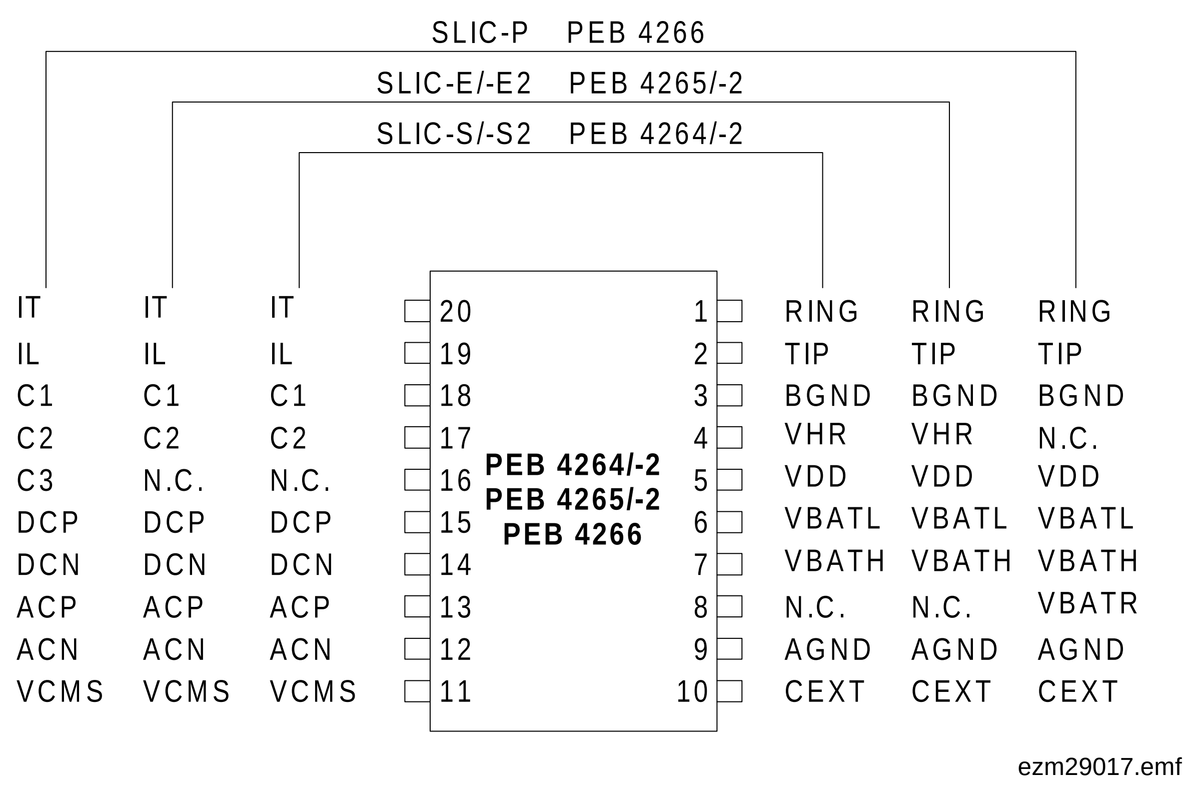

SLIC-P PEB 4266
SLIC-E/-E2 PEB 4265/-2
SLIC-S/-S2 PEB 4264/-2
IT
IL
C1
C2
C3
N.C.
DCP
DCN
ACP
ACN
VCMS
20
19
18
17
16
15
14
13
12
11
PEB 4264/-2
PEB 4265/-2
PEB 4266
1
2
3
4
5
6
7
8
9
10
RING
TIP
BGND
VHR
N.C.
VDD
VBATL
VBATH
VBATR
AGND
CEXT
ezm29017.emf

Figure 5 **Pin Configuration SLIC-S/-S2, SLIC-E/-E2, SLIC-P** (top view)

Note: The SLIC is only available in a P-DSO-20-5 package with heatsink on top. Please note that the pin counting for the P-DSO-20-5 package is clockwise (top view) in contrast to similar type packages which mostly count counterclockwise.

Table 2 Pin Definitions and Functions SLIC-S/-S2 and SLIC-E/-E2

Pin No.	Symbol	Input (I) Output (O)	Function
1	RING	I/O	Subscriber loop connection RING
2	TIP	I/O	Subscriber loop connection TIP
3	BGND	Power	Battery ground: TIP, RING, V_{BATH}, V_{BATL} and V_{HR} refer to this pin
4	VHR	Power	Auxiliary positive battery supply voltage used in ringing mode
5	VDD	Power	Positive supply voltage (+ 5 V), referred to AGND
6	VBATL	Power	Negative battery supply voltage ($-15\ V \geq V_{BATL} \geq V_{BATH}$)
7	VBATH	Power	Negative battery supply voltage: SLIC-S / SLIC-S2: $-20\ V \geq V_{BATH} \geq -65\ V$ SLIC-E / SLIC-E2: $-20\ V \geq V_{BATH} \geq -85\ V$
8	N.C.	–	Not connected
9	AGND	Power	Analog ground: V_{DD}, and all signal and control pins with the exception of TIP and RING refer to AGND
10	CEXT	O	Output of voltage divider defining DC line potentials; an external capacitance allows supply voltage filtering (output resistance about 30 kΩ)
11	VCMS	I	Reference voltage for differential two-wire interface, typical 1.5 V
12, 13	ACN, ACP	I	Differential two-wire AC input voltage; multiplied by – 6 and related to $(V_{HI} + V_{BI})/2$, ACN appears at TIP and ACP at RING output, respectively (V_{HI} & V_{BI} are internal voltages)
14, 15	DCN DCP	I	Differential two-wire DC input voltage; multiplied by a factor (– 30 in ACTH and ACTL mode, – 60 in ACTR mode) and related to $(V_{HI} + V_{BI})/2$, DCN appears at TIP and DCP at RING output, respectively
16	N.C.	–	Not connected
17	C2	I	Ternary logic input, controlling the operation mode
18	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding 165 °C) this pin sinks a current of typically 150 µA

Table 2 Pin Definitions and Functions SLIC-S/-S2 and SLIC-E/-E2 (cont'd)

Pin No.	**Symbol**	**Input (I) Output (O)**	**Function**
19	IL	O	Current output: longitudinal line current scaled down by a factor of 100
20	IT	O	Current output representing the transversal current scaled down by a factor of 50

Note: The SLIC is only available in a P-DSO-20-5 package with heatsink on top. Please note that the pin counting for the P-DSO-20-5 package is clockwise (top view) in contrast to similar type packages which mostly count counterclockwise.

Table 3 Pin Definitions and Functions SLIC-P

Pin No.	Symbol	Input (I) Output (O)	Function
1	RING	I/O	Subscriber loop connection RING
2	TIP	I/O	Subscriber loop connection TIP
3	BGND	Power	Battery ground: TIP, RING, V_{BATH}, V_{BATL} and V_{BATR} refer to this pin
4	N.C.	–	Not connected
5	VDD	Power	Positive supply voltage (3.1 V $\leq V_{DD} \leq$ 5.5 V), referred to AGND
6	VBATL	Power	Negative battery supply voltage (– 15 V $\geq V_{BATL} \geq$ – 140 V)
7	VBATH	Power	Negative battery supply voltage (– 20 V $\geq V_{BATH} \geq$ – 145 V, $V_{BATL} \geq V_{BATH}$)
8	VBATR	Power	Negative battery supply voltage used as on-hook voltage in power sensitive applications with external ringing or for the extended battery feeding option. (– 25 V $\geq V_{BATR} \geq$ – 150 V, $V_{BATL} \geq V_{BATH} \geq V_{BATR}$)
9	AGND	Power	Analog ground: V_{DD}, and all signal and control pins with the exception of TIP and RING refer to AGND
10	CEXT	O	Output of voltage divider defining DC line potentials; an external capacitance allows supply voltage filtering (output resistance about 30 kΩ)
11	VCMS	I	Reference voltage for differential two-wire interface, typical 1.5 V
12, 13	ACN, ACP	I	Differential two-wire AC input voltage; multiplied by – 6 and related to V_{BI}/2, ACN appears at TIP and ACP at RING output, respectively (V_{BI} is an internal voltage)
14, 15	DCN, DCP	I	Differential two-wire DC input voltage; multiplied by a factor (– 30 in ACTH & ACTL mode, – 60 in ACTR mode) and related to V_{BI}/2, DCN appears at TIP and DCP at RING output, respectively
16	C3	I	Binary logic input, controlling the operation mode
17	C2	I	Ternary logic input, controlling the operation mode
18	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding 165 °C) this pin sinks a current of typically 150 µA

Table 3 Pin Definitions and Functions SLIC-P (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
19	IL	O	Current output: longitudinal line current scaled down by a factor of 100
20	IT	O	Current output representing the transversal current scaled down by a factor of 50

Note: The SLIC is only available in a P-DSO-20-5 package with heatsink on top. Please note that the pin counting for the P-DSO-20-5 package is clockwise (top view) in contrast to similar type packages which mostly count counterclockwise.

2.2 Pin Diagram SLICOFI-2/-2S/-2S2

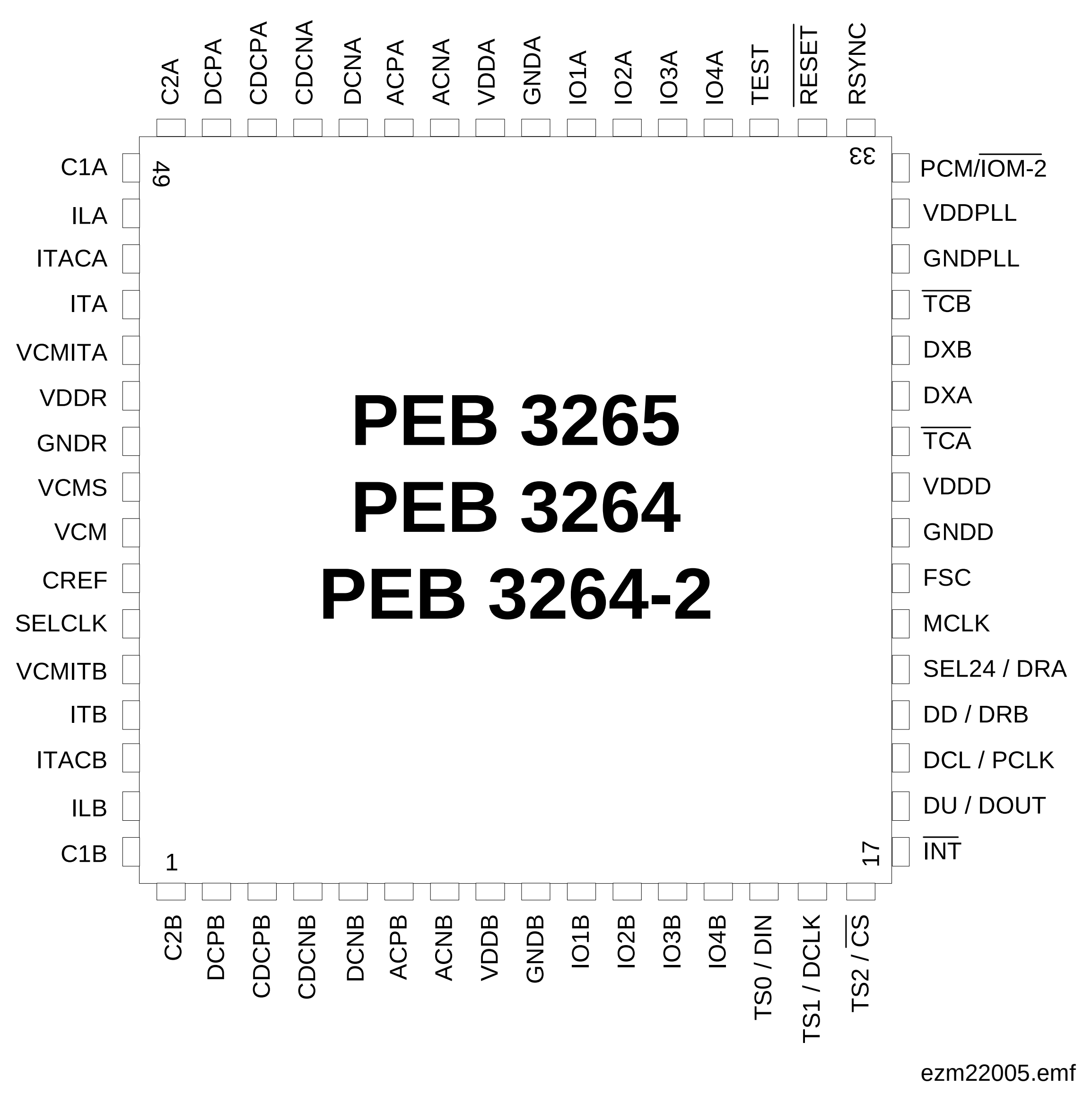

C2A
DCPA
CDCPA
CDCNA
DCNA
ACPA
ACNA
VDDA
GNDA
IO1A
IO2A
IO3A
IO4A
TEST
RESET
RSYNC
C1A
ILA
ITACA
ITA
VCMITA
VDDR
GNDR
VCMS
VCM
CREF
SELCLK
VCMITB
ITB
ITACB
ILB
C1B
49
33
1
17
PCM/IOM-2
VDDPLL
GNDPLL
TCB
DXB
DXA
TCA
VDDD
GNDD
FSC
MCLK
SEL24 / DRA
DD / DRB
DCL / PCLK
DU / DOUT
INT
C2B
DCPB
CDCPB
CDCNB
DCNB
ACPB
ACNB
VDDB
GNDB
IO1B
IO2B
IO3B
IO4B
TS0 / DIN
TS1 / DCLK
TS2 / CS
PEB 3265
PEB 3264
PEB 3264-2
ezm22005.emf

Figure 6 **Pin Configuration SLICOFI-2/-2S/-2S2** (top view)

Table 4 **Pin Definitions and Functions SLICOFI-2/-2S/-2S2**

Pin No.	Symbol	Input (I) Output (O)	Function
1	C2B	O	Ternary logic output for controlling the SLIC operation mode (channel B)
2	DCPB	O	Two-wire output voltage (DCP) (channel B)
3	CDCPB	I/O	External capacitance for filtering (channel B)
4	CDCNB	I/O	External capacitance for filtering (channel B)
5	DCNB	O	Two-wire output voltage (DCN) (channel B)
6	ACPB	O	Differential two-wire AC output voltage controlling the RING pin (channel B)
7	ACNB	O	Differential two-wire AC output voltage controlling the TIP pin (channel B)
8	VDDB	Power	+ 3.3 V analog supply voltage (channel B)
9	GNDB	Power	Analog ground (channel B)
10	IO1B	I/O	User-programmable I/O pin (channel B) with relay-driving capability. In external ringing mode IO1 is used to automatically control and drive the ring relay.
11	IO2B	I/O	User-programmable I/O pin (channel B) with relay-driving capability. SLICOFI-2 and SLIC-P: connected to pin C3 of SLIC-P, when two supply voltages for voice transmission and internal ringing are used.1)
12	IO3B	I/O	User-programmable I/O pin (channel B) with analog input functionality
13	IO4B	I/O	User-programmable I/O pin (channel B) with analog input functionality
14	TS0 DIN	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Time slot selection pin 0 PCM/$\overline{\text{IOM-2}}$ = 1 (μC interface): Data in
15	TS1 DCLK	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Time slot selection pin 1 PCM/$\overline{\text{IOM-2}}$ = 1 (μC interface): Data clock
16	TS2 $\overline{\text{CS}}$	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Time slot selection Pin 2 PCM/$\overline{\text{IOM-2}}$ = 1 (μC interface): Chip select, low active
17	$\overline{\text{INT}}$	O	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): not connected PCM/$\overline{\text{IOM-2}}$ = 1 (μC interface): Interrupt pin, low active

Table 4 **Pin Definitions and Functions SLICOFI-2/-2S/-2S2** (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
18	DU DOUT	O O	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Data upstream, open drain PCM/$\overline{\text{IOM-2}}$ = 1 (µC interface): Data out, push/pull
19	DCL PCLK	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Data clock PCM/$\overline{\text{IOM-2}}$ = 1 (PCM interface): 128 kHz to 8192 kHz PCM clock
20	DD DRB	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Data downstream PCM/$\overline{\text{IOM-2}}$ = 1 (PCM interface): Receive data input for PCM highway B
21	SEL24 DRA	I I	PCM/$\overline{\text{IOM-2}}$ =0 (IOM-2 interface): SEL24 = 0: DCL = 2048 kHz selected SEL24 = 1: DCL = 4096 kHz selected PCM/$\overline{\text{IOM-2}}$ =1 (PCM-interface): Receive Data input for PCM-highway A
22	MCLK	I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): not connected PCM/$\overline{\text{IOM-2}}$ = 1 (PCM interface): master clock when PCM/µC interface is used, clock rates are 512 kHz, 1536 kHz, 2048 kHz, 4096 kHz, 7168 kHz, 8192 kHz
23	FSC	I	Frame synchronization clock for PCM/µC or IOM-2 interface, 8 kHz, identifies the beginning of the frame, individual time slots are referenced to this input signal.
24	GNDD	Power	Digital ground
25	VDDD	Power	+ 3.3 V digital supply voltage
26	$\overline{\text{TCA}}$	O	Transmit control output for PCM highway A, active low during transmission, open drain
27	DXA	O	Transmit data output for PCM highway A (goes tristate when inactive)
28	DXB	O	Transmit data output for PCM highway B (goes tristate when inactive)
29	$\overline{\text{TCB}}$	O	Transmit control output for PCM highway B, active low during transmission, open drain
30	GNDPLL	Power	Digital ground PLL
31	VDDPLL	Power	+ 3.3 V supply voltage PLL

Table 4 Pin Definitions and Functions SLICOFI-2/-2S/-2S2 (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
32	PCM/ $\overline{\text{IOM-2}}$	I	PCM/$\overline{\text{IOM-2}}$ = 1: PCM/µC interface selected PCM/$\overline{\text{IOM-2}}$ = 0: IOM-2 interface selected
33	RSYNC	I	External ringing synchronization pin
34	$\overline{\text{RESET}}$	I	Reset pin, low active
35	TEST	I	Testpin for production test, has to be connected to GNDD
36	IO4A	I/O	User-programmable I/O Pin (channel A) with analog input functionality
37	IO3A	I/O	User-programmable I/O Pin (channel A) with analog input functionality
38	IO2A	I/O	User-programmable I/O Pin (channel A) with relay-driving capability. SLICOFI-2 and SLIC-P: connected to pin C3 of SLIC-P, when two supply voltages for voice transmission and internal ringing are used.1)
39	IO1A	I/O	User-programmable I/O Pin (channel A) with relay-driving capability. In external ringing mode IO1 is used to automatically control and drive the ring relay.
40	GNDA	Power	Analog ground (channel A)
41	VDDA	Power	+ 3.3 V analog supply voltage (channel A)
42	ACNA	O	Differential two-wire AC output voltage controlling the TIP pin (channel A)
43	ACPA	O	Differential two-wire AC output voltage controlling the RING pin (channel A)
44	DCNA	O	Two-wire output voltage (DCN) (channel A)
45	CDCNA	I/O	External capacitance for filtering (channel A)
46	CDCPA	I/O	External capacitance for filtering (channel A)
47	DCPA	O	Two-wire output voltage (DCP) (channel A)
48	C2A	O	Ternary logic output for controlling the SLIC operation mode (channel A)
49	C1A	I/O	Ternary logic output, controlling the SLIC operation mode (channel A); indicating thermal overload of SLIC if a current of typically 150 µA is drawn out
50	ILA	I	Longitudinal current input (channel A)
51	ITACA	I	Transversal current input (AC) (channel A)

Table 4 Pin Definitions and Functions SLICOFI-2/-2S/-2S2 (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
52	ITA	I	Transversal current input (AC + DC) (channel A)
53	VCMITA	I	Reference pin for trans./long. current sensing (channel A)
54	VDDR	Power	+ 3.3 V analog supply voltage (bias)
55	GNDR	Power	Analog ground (bias)
56	VCMS	O	Reference voltage for differential two-wire interface, typical 1.5 V
57	VCM	O	Reference voltage for input pins IT, IL, ITAC
58	CREF	I/O	An external capacitor of 68 nF has to be connected to GNDR
59	SELCLK	I	Master clock select. Should be set to GND (internal master clock generation). For test purposes, external master clock generation can be selected (SELCLK = 1). In this case a clock of nominal 32.768 Mhz with a jitter time of less than 1 ns has to be applied to the MCLK pin.
60	VCMITB	I	Reference pin for transversal/longitudinal current sensing (channel B)
61	ITB	I	Transversal current input (AC + DC) (channel B)
62	ITACB	I	Transversal current input (AC) (channel B)
63	ILB	I	Longitudinal current input (channel B)
64	C1B	I/O	Ternary logic output, controlling the SLIC operation mode (channel B); indicating thermal overload of SLIC if a current of typically 150 µA is drawn out

---

[1] If SLIC-P is selected, IO2 cannot be controlled by the user, but is utilized by the SLICOFI-2 to control the C3 pin of SLIC-P.

3 Functional Description

3.1 Functional Overview

3.1.1 Basic Functions available for all DuSLIC Chip Sets

The functions described in this chapter are integrated in all DuSLIC chip sets (see **Figure 7** for DuSLIC-S/-S2 and **Figure 8** for DuSLIC-E/-E2/-P).

All BORSCHT functions are integrated:

- Battery feed
- Overvoltage protection
  (realized by the robust high-voltage SLIC technology and additional circuitry)
- Ringing¹⁾
- Signaling (supervision)
- Coding
- Hybrid for 2/4-wire conversion
- Testing

An important feature of the DuSLIC design is the fact that all the SLIC and codec functions are programmable via the IOM-2 or PCM/µC-interface of the dual channel *SLICOFI-2x* device:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude¹⁾
- Hook thresholds
- TTX modes²⁾

Because signal processing within the *SLICOFI-2x* is completely digital, it is possible to adapt to the requirements listed above by simply updating the coefficients that control DSP processing of all data. This means, for example, that changing impedance matching or hybrid balance requires no hardware modifications. A single hardware is now capable of meeting the requirements for different markets. The digital nature of the filters and gain stages also assures high reliability, no drifts (over temperature or time) and minimal variations between different lines.

---

1) For DuSLIC-S2 chip set external ringing is supported
2) Not available with DuSLIC-S2 chip set

The characteristics for the two voice channels within *SLICOFI-2x* can be programmed independently of each other. The DuSLICOS software is provided to automate calculation of coefficients to match different requirements. DuSLICOS also verifies the calculated coefficients.

3.1.2 Additional Functions available for DuSLIC-E/-E2/-P Chip Sets

The following line circuit functions are integrated only in the DuSLIC-E/-E2/-P chip sets (see **Figure 8**):

- Teletax metering

For pulse metering, a 12/16 kHz sinusoidal metering burst has to be transmitted. The DuSLIC chip set generates the metering signal internally and has an integrated notch filter.

- DTMF

DuSLIC has an integrated DTMF generator comprising two tone generators and a DTMF decoder. The decoder is able to monitor the transmit or receive path for valid tone pairs and outputs the corresponding digital code for each DTMF tone pair.

- Caller ID Frequency Shift Keying (FSK) Modulator

DuSLIC has an integrated FSK modulator capable of sending Caller ID information. The Caller ID modulator complies with all requirements of ITU-T recommendation V.23 and Bell 202.

- LEC (Line Echo Cancellation)

DuSLIC contains an adaptive line echo cancellation unit for the cancellation of near end echos (up to 8 ms cancelable echo delay time).

- UTD (Universal Tone Detection)

DuSLIC has an integrated Universal Tone Detection unit to detect special tones in the receive or transmit path (e.g. fax or modem tones).

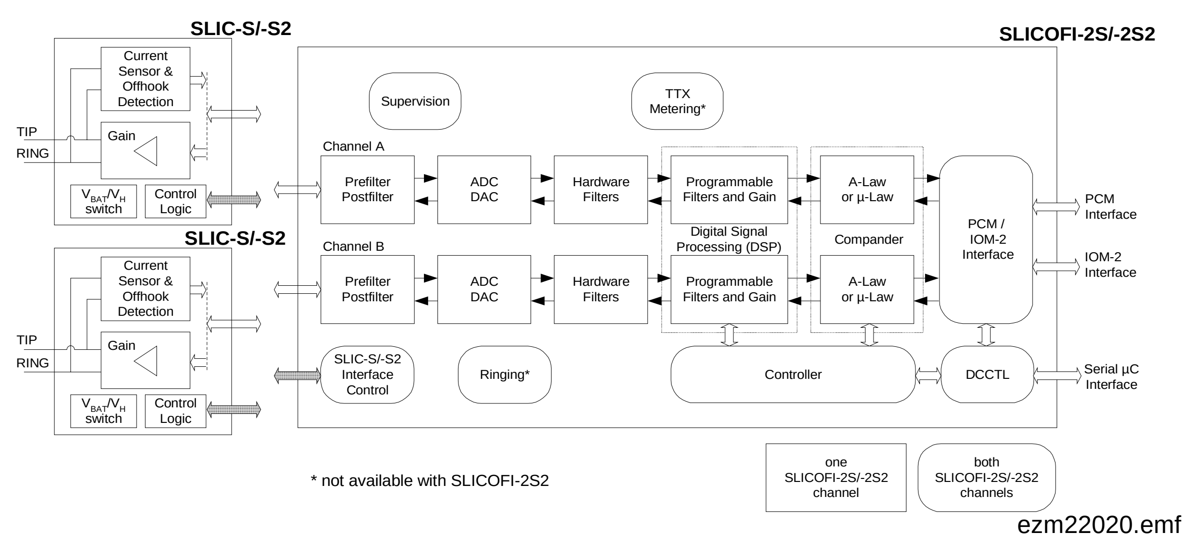

SLIC-S/-S2
SLICOFI-2S/-2S2
Current Sensor & Offhook Detection
TIP
RING
Gain
V_{BAT}/V_H switch
Control Logic
SLIC-S/-S2
Current Sensor & Offhook Detection
TIP
RING
Gain
V_{BAT}/V_H switch
Control Logic
Supervision
TTX Metering*
Channel A
Prefilter Postfilter
ADC DAC
Hardware Filters
Programmable Filters and Gain
A-Law or µ-Law
PCM / IOM-2 Interface
Digital Signal Processing (DSP)
Compander
Channel B
Prefilter Postfilter
ADC DAC
Hardware Filters
Programmable Filters and Gain
A-Law or µ-Law
PCM Interface
IOM-2 Interface
SLIC-S/-S2 Interface Control
Ringing*
Controller
DCCTL
Serial µC Interface
one SLICOFI-2S/-2S2 channel
both SLICOFI-2S/-2S2 channels
* not available with SLICOFI-2S2
ezm22020.emf

Figure 7 Line Circuit Functions included in the DuSLIC-S/-S2

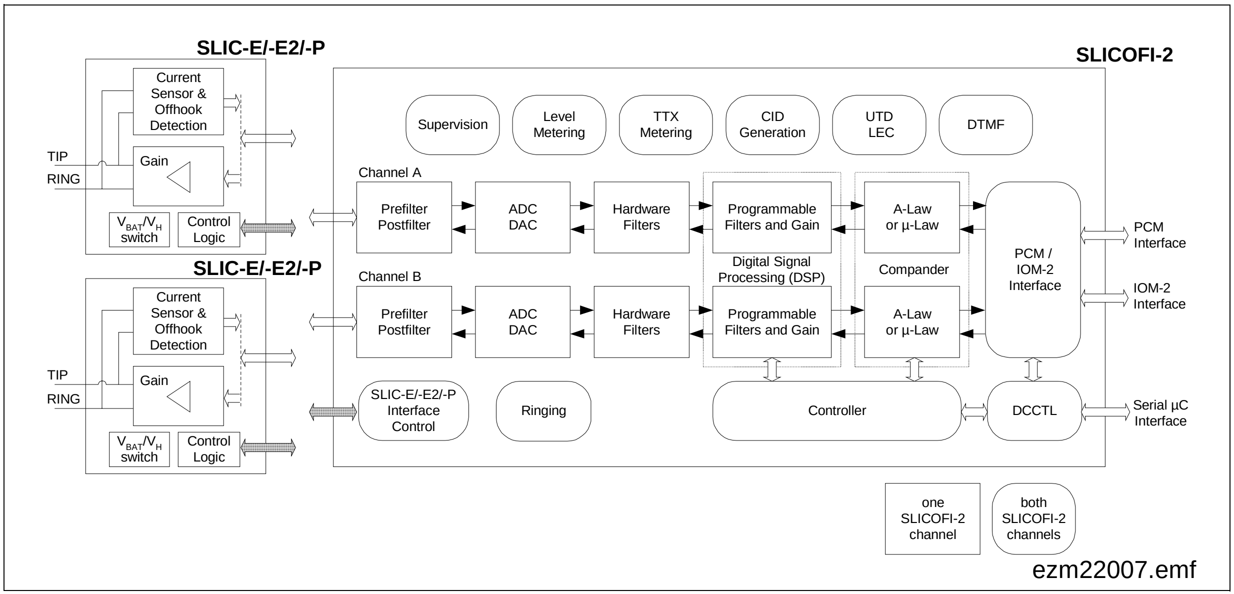

SLIC-E/-E2/-P
SLICOFI-2
Current Sensor & Offhook Detection
TIP
RING
Gain
V_{BAT}/V_H switch
Control Logic
SLIC-E/-E2/-P
Current Sensor & Offhook Detection
TIP
RING
Gain
V_{BAT}/V_H switch
Control Logic
Supervision
Level Metering
TTX Metering
CID Generation
UTD LEC
DTMF
Channel A
Prefilter Postfilter
ADC DAC
Hardware Filters
Programmable Filters and Gain
A-Law or µ-Law
PCM / IOM-2 Interface
Digital Signal Processing (DSP)
Compander
Channel B
Prefilter Postfilter
ADC DAC
Hardware Filters
Programmable Filters and Gain
A-Law or µ-Law
PCM Interface
IOM-2 Interface
SLIC-E/-E2/-P Interface Control
Ringing
Controller
DCCTL
Serial µC Interface
one SLICOFI-2 channel
both SLICOFI-2 channels
ezm22007.emf

Figure 8 Line Circuit Functions included in the DuSLIC-E/-E2/-P

3.2 Block Diagrams

Figure 9, **Figure 10** and **Figure 11** show the basic functional blocks and circuits for all SLIC versions of the DuSLIC chip set.

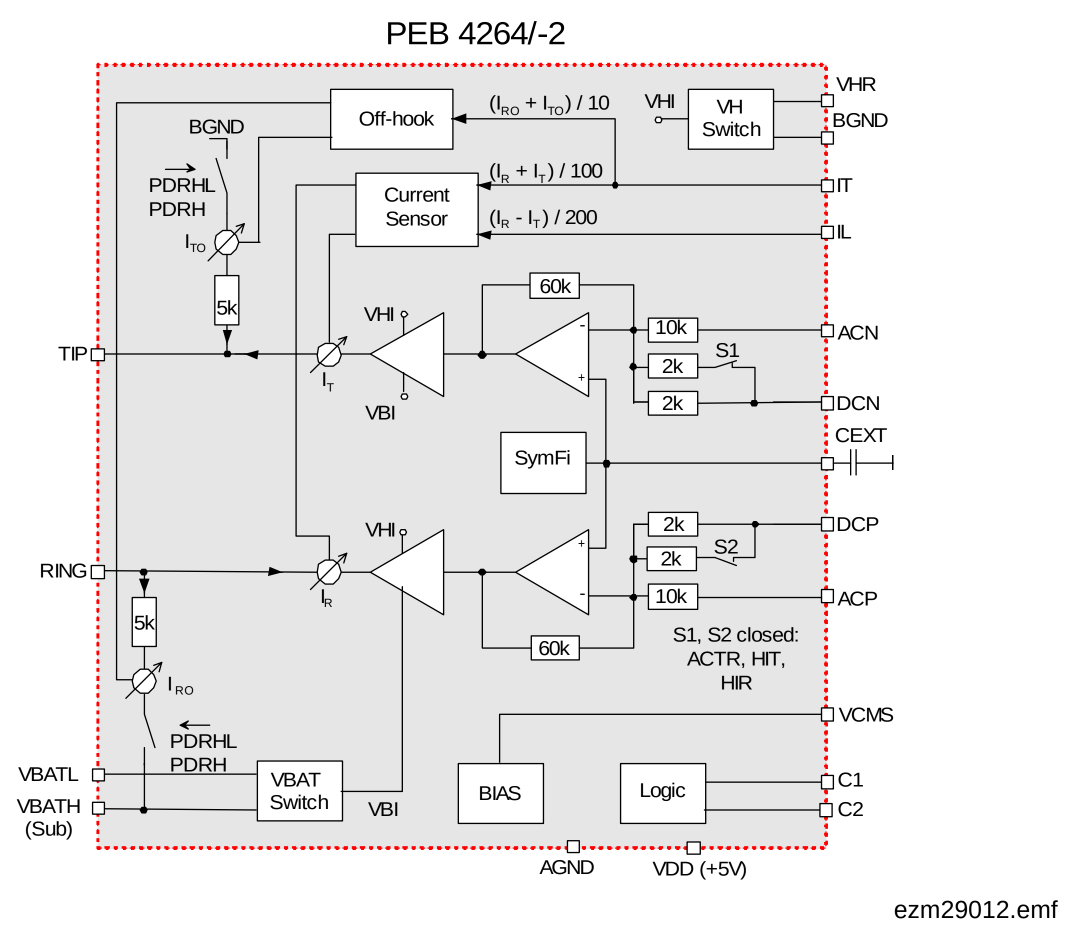

PEB 4264/-2
Off-hook
$(I_{RO} + I_{TO}) / 10$
VHI
VH Switch
VHR
BGND
BGND
PDRHL
PDRH
I_{TO}
Current Sensor
$(I_R + I_T) / 100$
IT
$(I_R - I_T) / 200$
IL
5k
60k
VHI
10k
ACN
TIP
I_T
2k
S1
2k
DCN
VBI
SymFi
CEXT
VHI
2k
DCP
RING
I_R
2k
S2
5k
10k
ACP
60k
S1, S2 closed:
ACTR, HIT,
HIR
I_{RO}
VCMS
PDRHL
PDRH
VBATL
VBAT Switch
BIAS
Logic
C1
VBATH
(Sub)
VBI
C2
AGND
VDD (+5V)
ezm29012.emf

Figure 9 Block Diagram SLIC-S/-S2 (PEB 4264/-2)

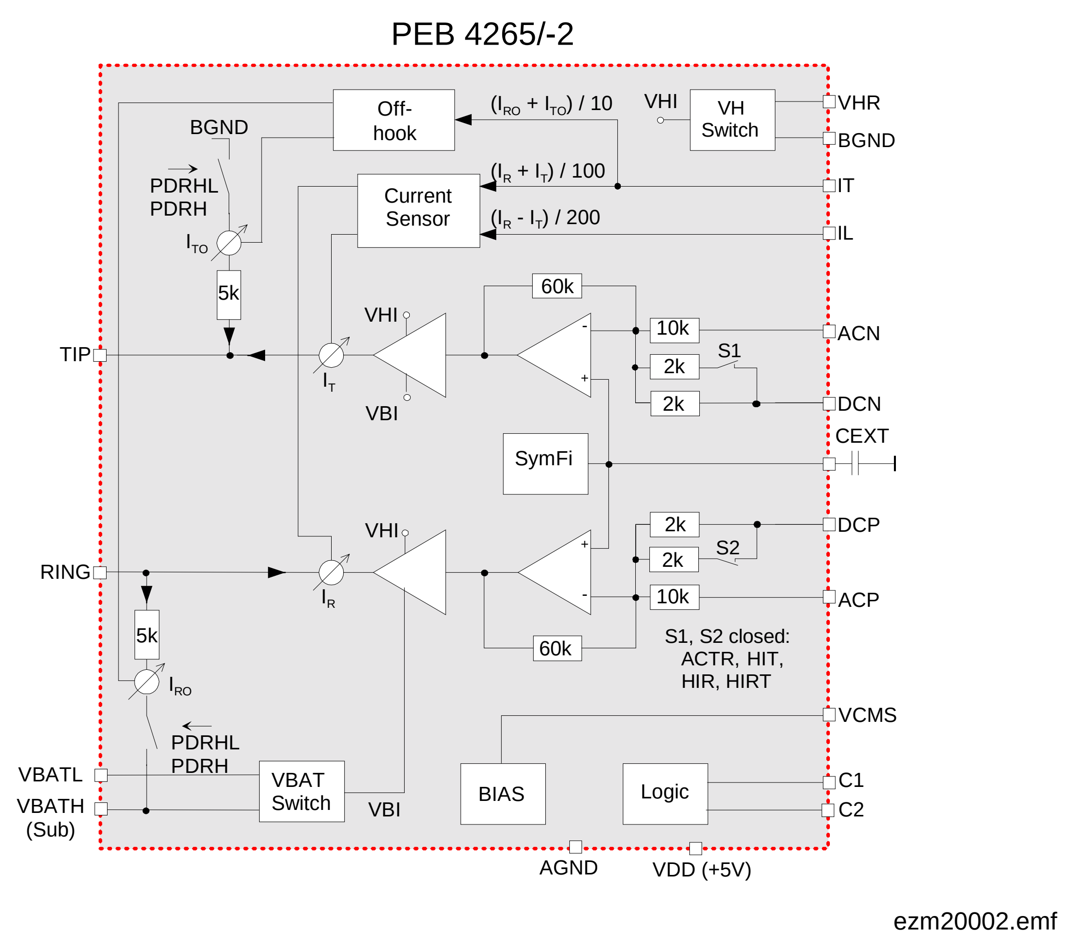

PEB 4265/-2
Off-hook
$(I_{RO} + I_{TO}) / 10$
VHI
VH Switch
VHR
BGND
BGND
PDRHL
PDRH
I_{TO}
Current Sensor
$(I_R + I_T) / 100$
$(I_R - I_T) / 200$
IT
IL
5k
60k
VHI
10k
ACN
2k
S1
TIP
I_T
2k
DCN
VBI
CEXT
SymFi
VHI
2k
DCP
2k
S2
RING
I_R
10k
ACP
5k
60k
S1, S2 closed:
ACTR, HIT,
HIR, HIRT
I_{RO}
VCMS
PDRHL
PDRH
VBATL
VBAT Switch
BIAS
Logic
C1
VBATH
(Sub)
VBI
C2
AGND
VDD (+5V)
ezm20002.emf

Figure 10 Block Diagram SLIC-E/-E2 (PEB 4265/-2)

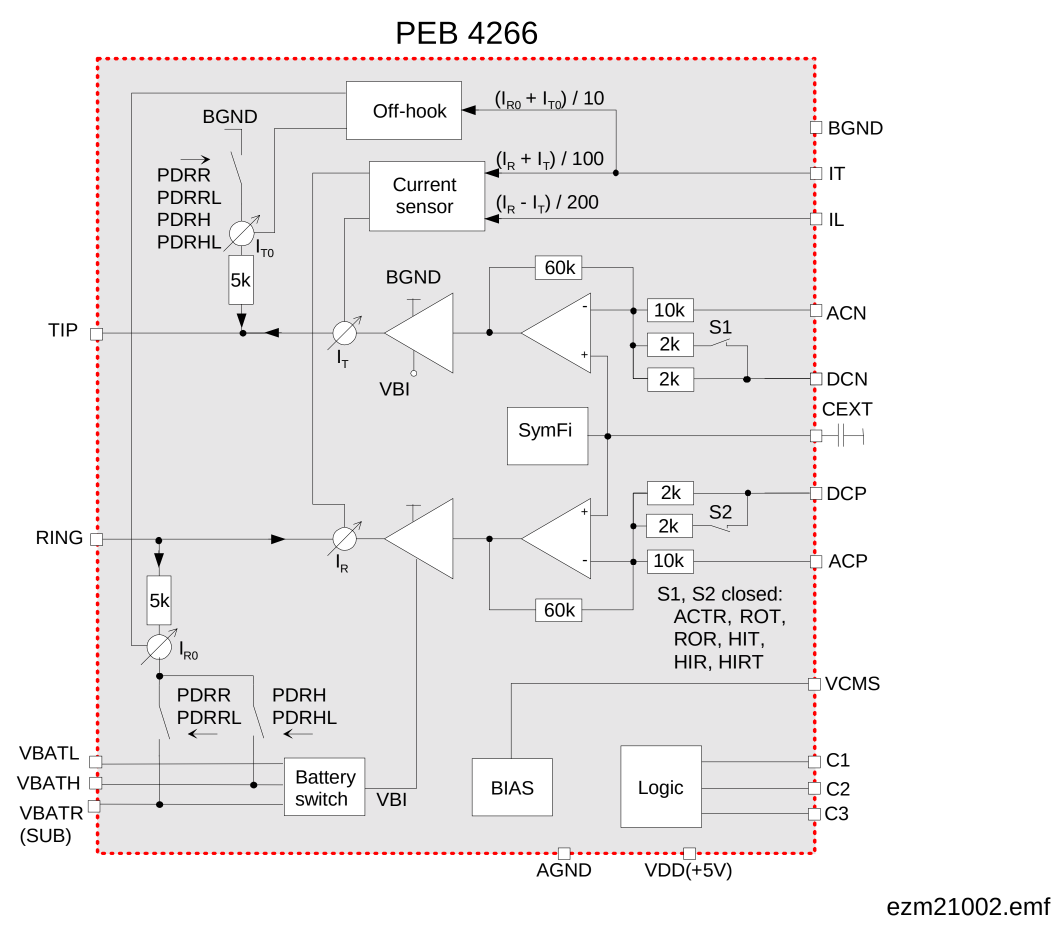

PEB 4266
Off-hook
$(I_{R0} + I_{T0}) / 10$
BGND
Current sensor
$(I_R + I_T) / 100$
$(I_R - I_T) / 200$
IT
IL
PDRR
PDRRL
PDRH
PDRHL
I_{T0}
5k
BGND
60k
10k
ACN
TIP
S1
2k
2k
DCN
I_T
VBI
CEXT
SymFi
2k
DCP
S2
RING
2k
10k
ACP
I_R
60k
5k
I_{R0}
S1, S2 closed:
ACTR, ROT,
ROR, HIT,
HIR, HIRT
VCMS
PDRR
PDRRL
PDRH
PDRHL
VBATL
VBATH
VBATR
(SUB)
Battery switch
VBI
BIAS
Logic
C1
C2
C3
AGND
VDD(+5V)
ezm21002.emf

Figure 11 **Block Diagram SLIC-P (PEB 4266)**

Figure 12 shows the internal block structure of all *SLICOFI-2x* codec versions available. The Enhanced Digital Signal Processor (EDSP) realizing the add-on funtions[1] is only integrated in the SLICOFI-2 (PEB 3265) device.

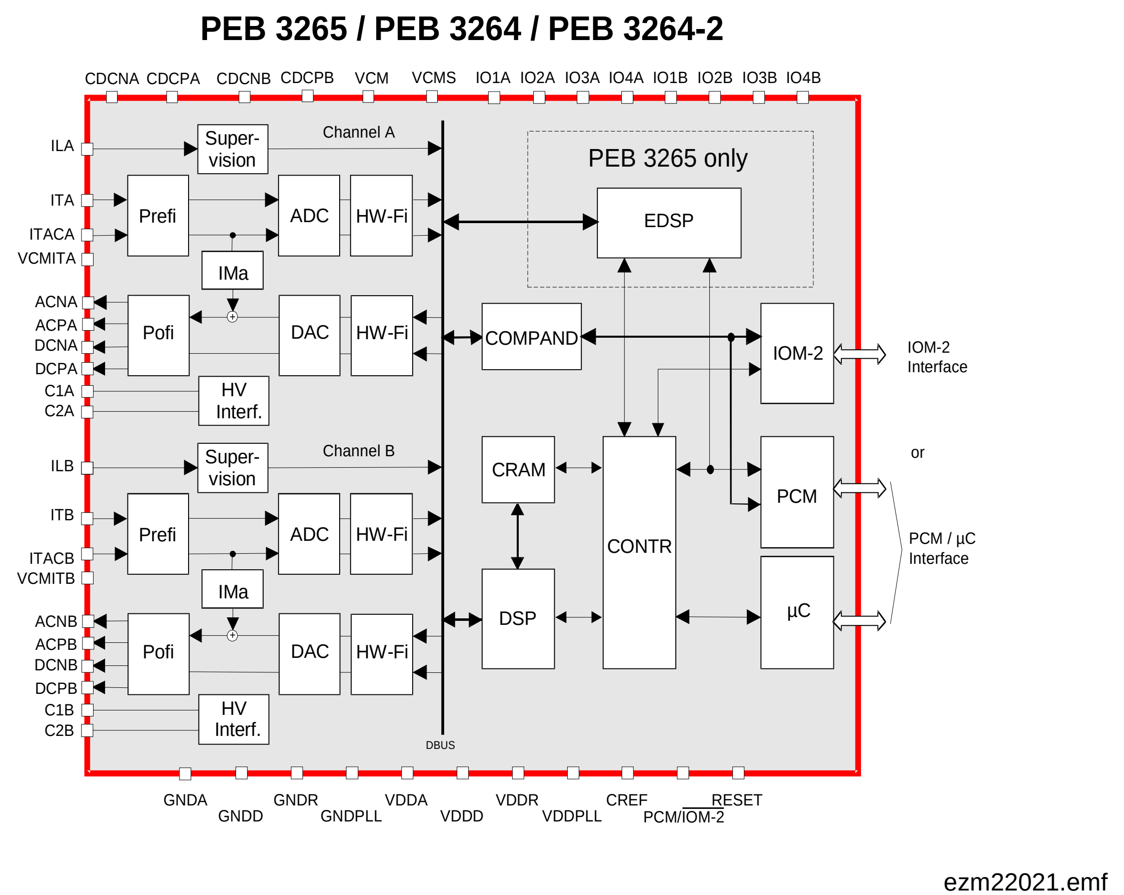

PEB 3265 / PEB 3264 / PEB 3264-2
CDCNA
CDCPA
CDCNB
CDCPB
VCM
VCMS
IO1A
IO2A
IO3A
IO4A
IO1B
IO2B
IO3B
IO4B
ILA
ITA
ITACA
VCMITA
ACNA
ACPA
DCNA
DCPA
C1A
C2A
Super-vision
Channel A
Prefi
ADC
HW-Fi
IMa
Pofi
DAC
HW-Fi
HV Interf.
PEB 3265 only
EDSP
COMPAND
IOM-2
IOM-2 Interface
or
CRAM
CONTR
PCM
DSP
µC
PCM / µC Interface
ILB
ITB
ITACB
VCMITB
ACNB
ACPB
DCNB
DCPB
C1B
C2B
Super-vision
Channel B
Prefi
ADC
HW-Fi
IMa
Pofi
DAC
HW-Fi
HV Interf.
DBUS
GNDA
GNDD
GNDR
GNDPLL
VDDA
VDDD
VDDR
VDDPLL
CREF
RESET
PCM/IOM-2
ezm22021.emf

Figure 12 Block Diagram SLICOFI-2/-2S/-2S2 (PEB 3265, PEB 3264/-2)

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[1] The add-on functions are DTMF detection, Caller ID generation, Message Waiting lamp support, Three Party Conferencing, Universal Tone Detection (UTD), Line Echo Cancellation (LEC) and Sleep Mode.

3.3 DC Feeding

DC feeding with the DuSLIC is fully programmable by using the software coefficients depicted in **Table 5** on **Page 45**.

Figure 13 shows the signal paths for DC feeding between the SLIC and *SLICOFI-2x*:

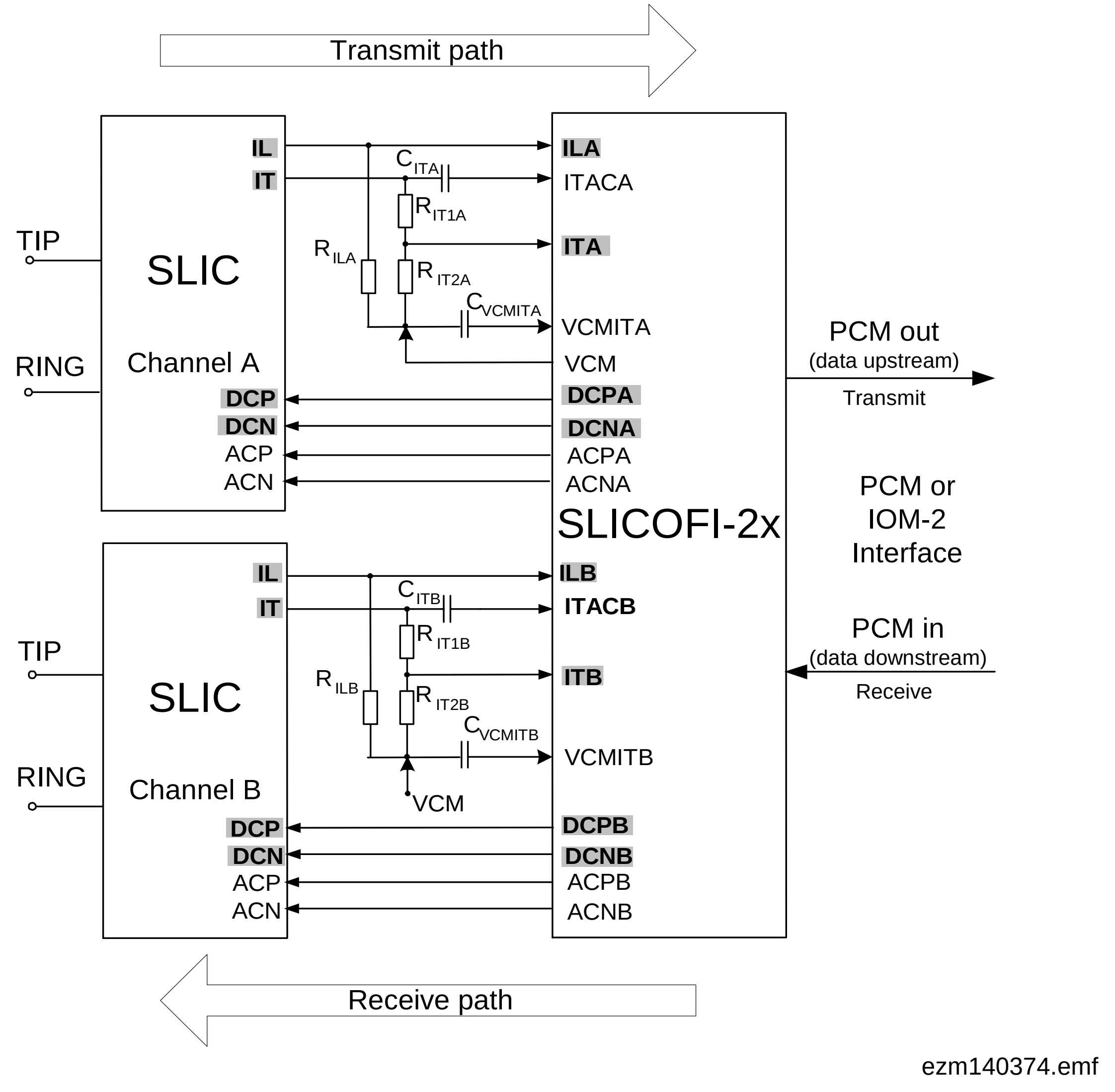

Transmit path
TIP
RING
SLIC
Channel A
IL
IT
DCP
DCN
ACP
ACN
C_{ITA}
R_{IT1A}
R_{ILA}
R_{IT2A}
C_{VCMITA}
ILA
ITACA
ITA
VCMITA
VCM
DCPA
DCNA
ACPA
ACNA
SLICOFI-2x
PCM out
(data upstream)
Transmit
PCM or
IOM-2
Interface
PCM in
(data downstream)
Receive
TIP
RING
SLIC
Channel B
IL
IT
DCP
DCN
ACP
ACN
C_{ITB}
R_{IT1B}
R_{ILB}
R_{IT2B}
C_{VCMITB}
VCM
ILB
ITACB
ITB
VCMITB
DCPB
DCNB
ACPB
ACNB
Receive path
ezm140374.emf

Figure 13 Signal Paths – DC Feeding

3.3.1 DC Characteristic Feeding Zones

The DuSLIC DC feeding characteristic has three different zones: the constant current zone, the resistive zone and the constant voltage zone. A voltage reserve V_{RES} (see **Chapter 3.3.7**) can be selected to avoid clipping the high level AC signals (e.g. TTX) and to take into account the voltage drop of the SLIC. The DC feeding characteristic is shown in **Figure 14**.

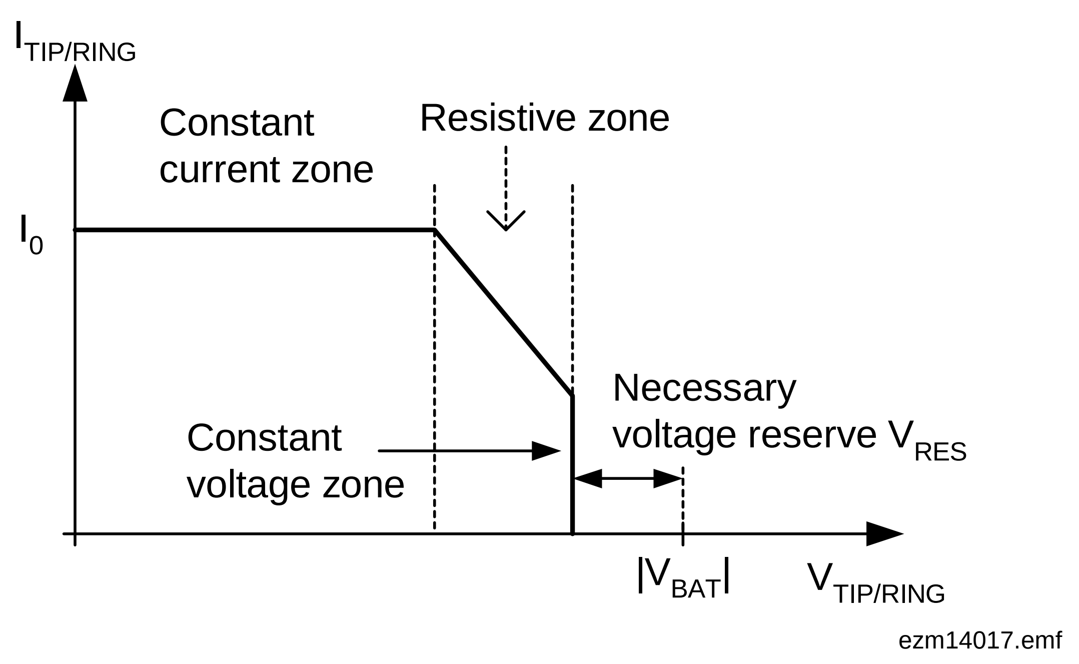
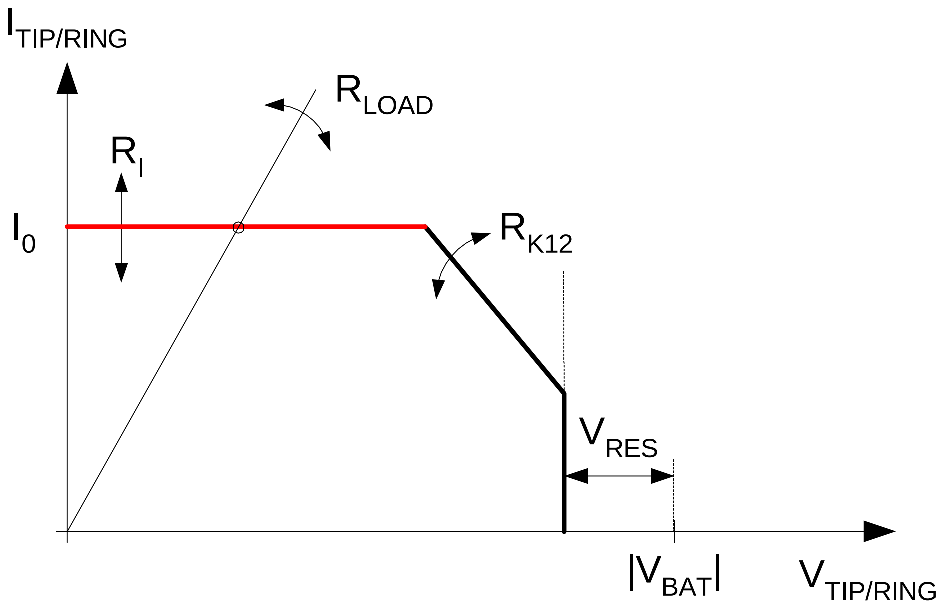

I_{TIP/RING}
Constant current zone
Resistive zone
I0
Necessary voltage reserve VRES
Constant voltage zone
|VBAT|
VTIP/RING
ezm14017.emf

Figure 14 DC Feeding Characteristic

The simplified diagram shows the constant current zone as an ideal current source with an infinite internal resistance, while the constant voltage zone is shown as an ideal voltage source with an internal resistance of 0 Ω. For the specification of the internal resistances see **Chapter 3.3.5**.

3.3.2 Constant Current Zone

In the off-hook state, the feed current must usually be kept at a constant value independent of load (see **Figure 15**). The SLIC senses the DC current and supplies this information to *SLICOFI-2x* via the IT pin (input pin for DC control). *SLICOFI-2x* compares the actual current with the programmed value and adjusts the SLIC drivers as necessary. $I_{\text{TIP/RING}}$ in the constant current zone is programmable from 0 to 32 mA or 0 to 50 mA depending on the used SLIC version.



ezm14016.emf

Figure 15 Constant Current Zone

Depending on the load, the operating point is determined by the voltage $V_{\text{TIP/RING}}$ between the Tip and Ring pins.

The operating point is calculated from:

$V_{\text{TIP/RING}} = R_{\text{LOAD}} \times I_{\text{TIP/RING}}$

where

$R_{\text{LOAD}} = R_{\text{PRE}} + R_{\text{LINE}} + R_{\text{PHONE,OFF-HOOK}}$

$R_{\text{PRE}} = R_{\text{PROT}} + R_{\text{STAB}}$ (see **Figure 99** on **Page 370**).

The lower the load resistance R_{LOAD}, the lower the voltage between the Tip and Ring pins. A typical value for the programmable feeding resistance in the constant current zone is about $R_{\text{I}} = 10\ \text{k}\Omega$ (see **Table 5**).

3.3.3 Resistive Zone

The programmable resistive zone R_{K12} of DuSLIC provides extra flexibility over a wide range of applications. The resistive zone is used for very long lines where the battery is incapable of feeding a constant current into the line.

The operating point in this case crosses from the constant current zone for low and medium impedance loops to the resistive zone for high impedance loops (see **Figure 16**). The resistance of the zone R_{K12} is programmable from R_V to 1000 Ω.

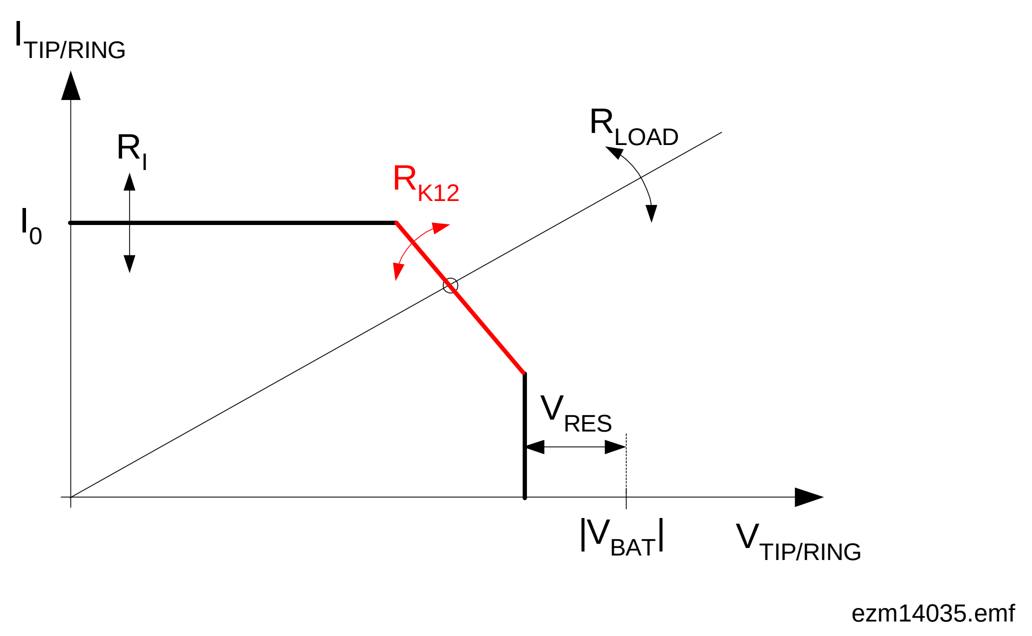
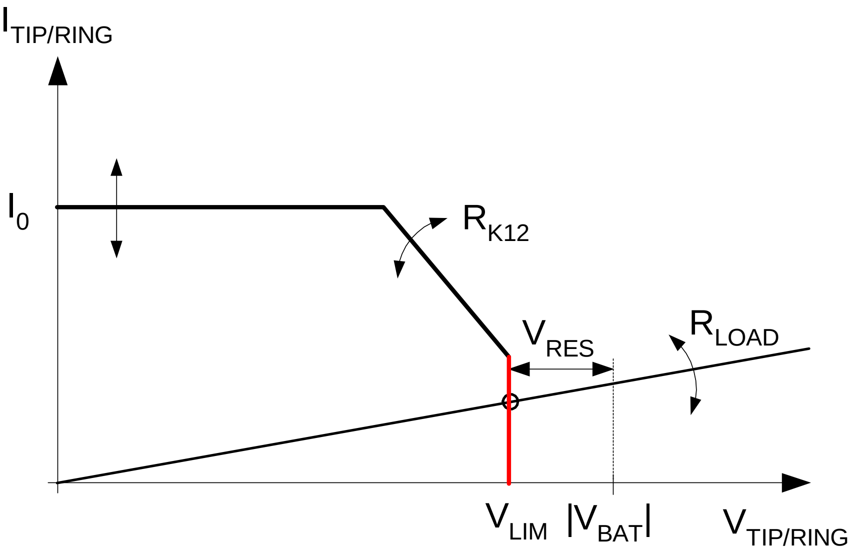


Figure 16 Resistive Zone

3.3.4 Constant Voltage Zone

The constant voltage zone (see **Figure 17**) is used in some applications to supply a constant voltage to the line. In this case $V_{\mathrm{TIP/RING}}$ is constant and the current depends on the load between the Tip and Ring pin.

In the constant voltage zone the external resistors $R_{\mathrm{PRE}} = R_{\mathrm{Stab}} + R_{\mathrm{Prot}}$ necessary for stability and protection define the resistance R_{V} seen at the RING and TIP wires of the application.
The programmable range of the parameters R_{I}, I_0, I_{K1}, V_{K1}, R_{K12} and V_{LIM} is given in **Table 5**.



ezm14036.emf

Figure 17 Constant Voltage Zone

3.3.5 Programmable Voltage and Current Range of DC Characteristic

The DC characteristic and all symbols are shown in **Figure 18**.

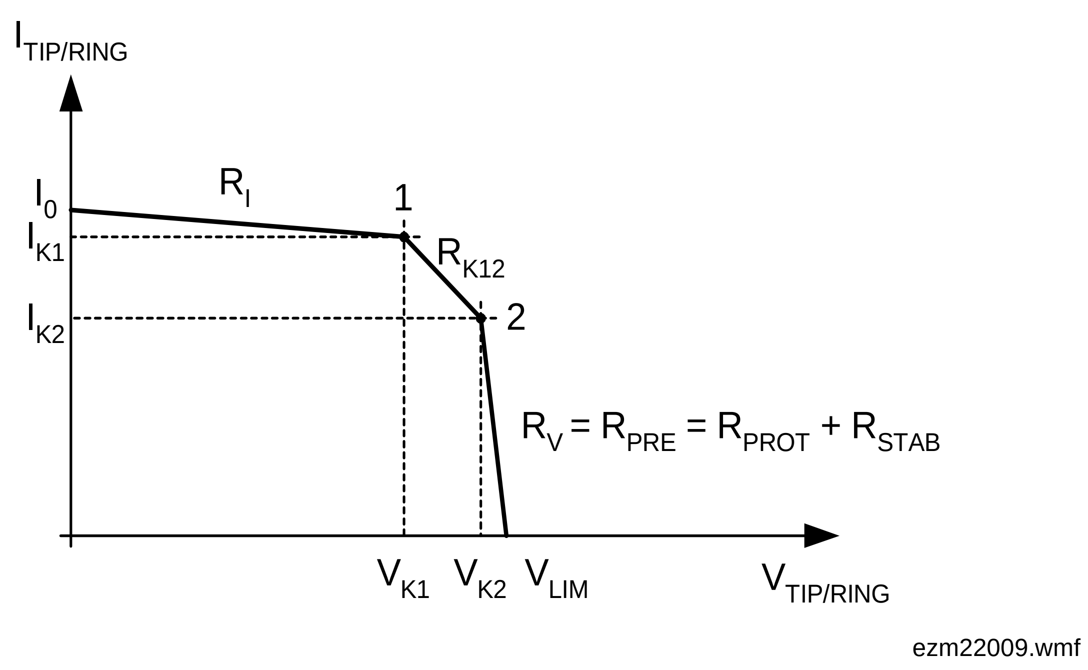


Figure 18 DC Characteristic

Table 5 DC Characteristic

Symbol	Programmable Range	Condition
R_I	1.8 kΩ … 40 kΩ	–
I_0	0 … 32 mA	only for DuSLIC-S, DuSLIC-E, DuSLIC-P
	0 … 50 mA	only for DuSLIC-S2, DuSLIC-E2
I_{K1}	0 … 32 mA	only for DuSLIC-S, DuSLIC-E, DuSLIC-P
	0 … 50 mA	only for DuSLIC-S2, DuSLIC-E2
V_{K1}	0 … 50 V	–
	$V_{K1} < V_{LIM} - I_{K1} \times R_{K12}$	only (V_{K1}, I_{K1})
	$V_{K1} < V_{LIM} - I_{K1} \times R_V$ $V_{K1} > V_{LIM} - I_{K1} \times R_{K12}$	(V_{K1}, I_{K1}) and (V_{K2}, I_{K2})
R_{K12}	R_V … 1000 Ω	–
V_{LIM}	0 … 50 V	–
	$V_{LIM} > V_{K1} + I_{K1} \times R_{K12}$	only (V_{K1}, I_{K1})

3.3.6 SLIC Power Dissipation

The major portion of the power dissipation in the SLIC can be estimated by the power dissipation in the output stages. The power dissipation can be calculated from:

$$P_{\mathrm{SLIC}} \approx (V_{\mathrm{BAT}} - V_{\mathrm{TIP/RING}}) \times I_{\mathrm{TIP/RING}}$$

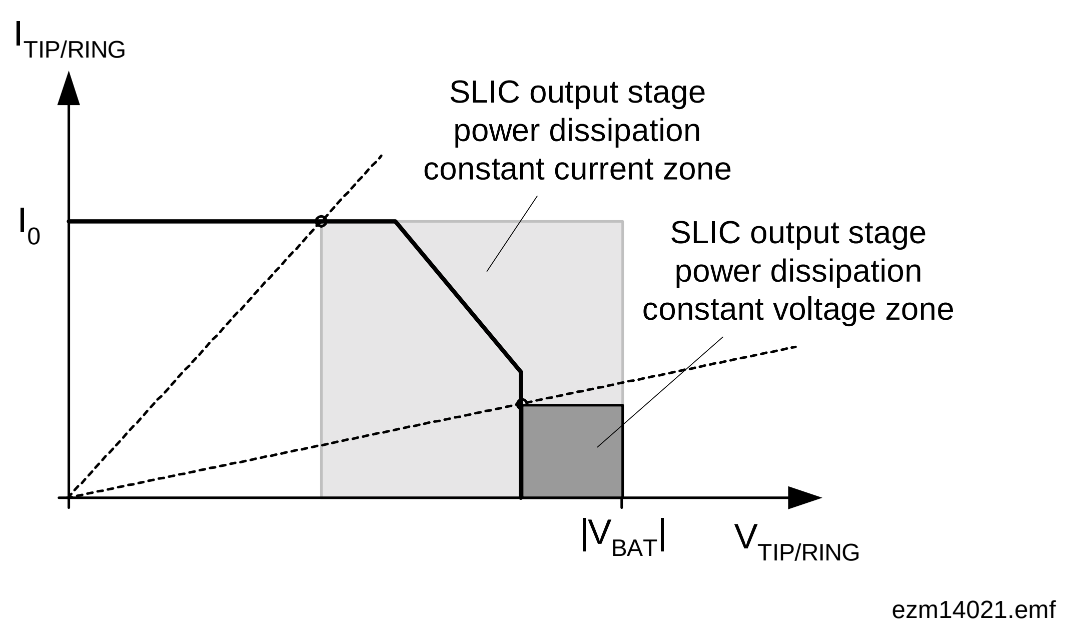

$I_{TIP/RING}$
SLIC output stage power dissipation constant current zone
I_0
SLIC output stage power dissipation constant voltage zone
$|V_{BAT}|$
$V_{TIP/RING}$
ezm14021.emf

Figure 19 Power Dissipation

For further information see **Chapter 4.7.3** on **Page 95**.

3.3.7 Necessary Voltage Reserve

To avoid clipping AC speech signals as well as AC metering pulses, a voltage reserve V_{RES} (see **Figure 14**) has to be provided.

$$V_{RES} = |V_{BAT}| - V_{LIM}$$

V_{BAT} is the selected battery voltage, which can be depending on the mode either V_{BATH}, V_{BATL}, ($V_{HR} - V_{BATH}$) for SLIC-S/-S2/-E/-E2 or V_{BATH}, V_{BATL}, $-V_{BATR}$ for SLIC-P.

V_{RES} consists of:

- Voltage reserve of the SLIC output buffers: this voltage drop depends on the output current through the Tip and Ring pins. For a standard output current of 25 mA, this voltage reserve is a few volts (see **Table 17** on **Page 95**).
- Voltage reserve for AC speech signals: max. signal amplitude (example 2 V)
- Voltage reserve for AC metering pulses: The TTX signal amplitude V_{TTX} depends on local specifications and varies from 0.1 Vrms to several Vrms at a load of 200 Ω. To obtain V_{TTX} = 2 Vrms at a load of 200 Ω and R_{PRE} = 50 Ω ($R_{PRE} = R_{PROT} + R_{STAB}$, see **Figure 99** on **Page 370**), 3 Vrms = 4.24 Vpeak are needed at the SLIC output.

Therefore a V_{RES} value of 10.24 V must be selected (= 4 V (SLIC drop for peak current of DC and speech and TTX) + 2 V (AC speech signals) + 4.24 V (TTX-signal)).

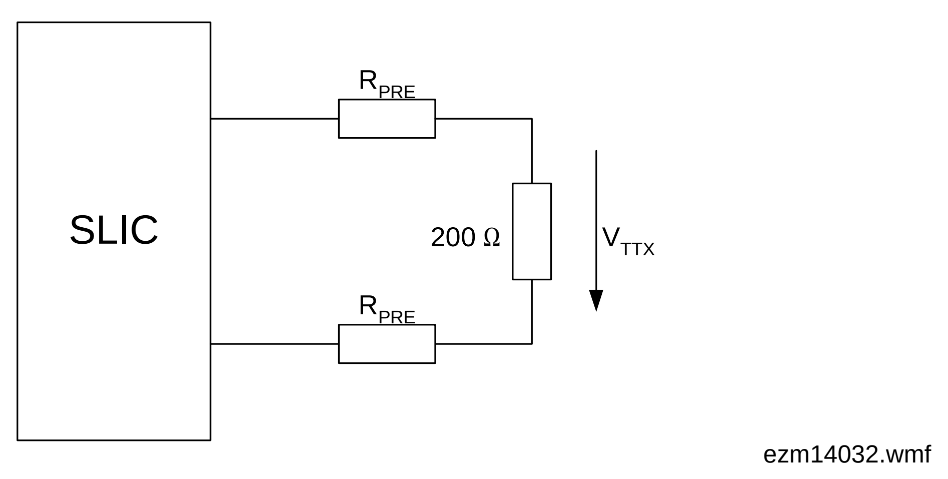


Figure 20 TTX Voltage Reserve Schematic

3.3.8 Extended Battery Feeding

If the battery voltage is not sufficient to supply the minimum required current through the line even in the resistive zone, the auxiliary positive battery voltage can be used to expand the voltage swing between Tip and Ring. With this extended supply voltage V_{HR} (DuSLIC-S/E) respectively V_{BATR} (DuSLIC-P), it is possible to supply the constant current for long lines. **Figure 21** shows the DC feeding impedances $R_{\mathrm{MAX,ACTH}}$ in ACTH mode and $R_{\mathrm{MAX,ACTR}}$ in ACTR mode (for ACTH and ACTR modes see **Chapter 4.1**).

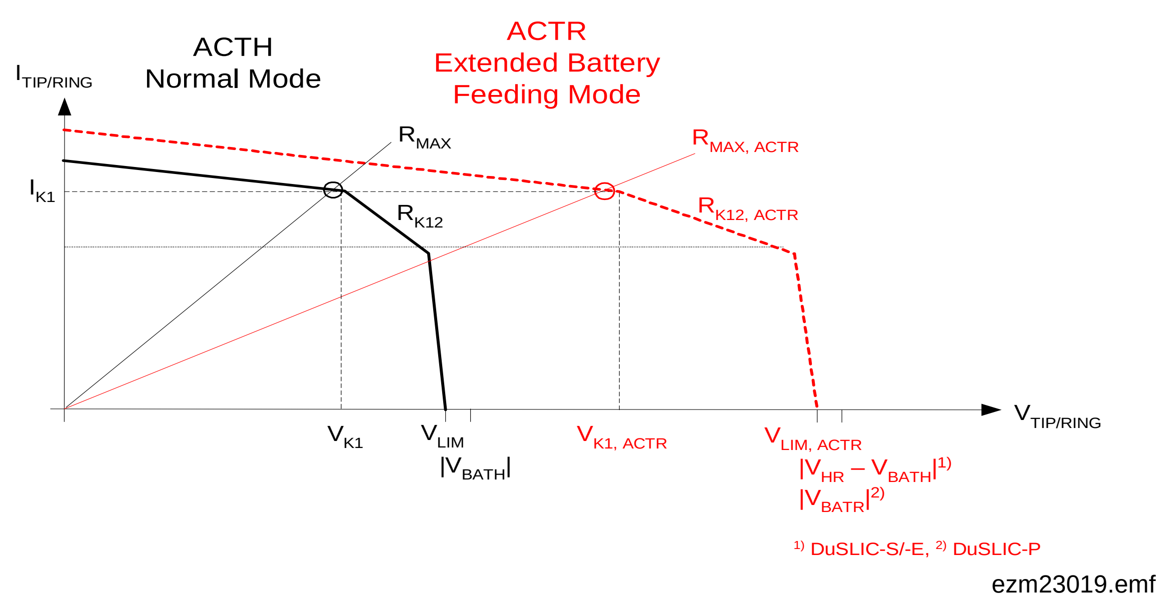


Figure 21 DC Feeding Characteristics (ACTH, ACTR)

The extended feeding characteristic is determined by the feeding characteristic in normal mode (ACTH) and an additional gain factor $\mathrm{K_B}$ (DuSLICOS DC Control Parameter 1/3: Additional Gain in active Ring):

$$V_{\mathrm{LIM,ACTR}} = V_{\mathrm{LIM}} \times \mathrm{K_B}$$

$$V_{\mathrm{K1,ACTR}} = V_{\mathrm{K1}} \times \mathrm{K_B} + R_{\mathrm{V}} \times I_{\mathrm{K1}} \times (\mathrm{K_B} - 1) \approx V_{\mathrm{K1}} \times \mathrm{K_B}$$

$$R_{\mathrm{K12,ACTR}} = \mathrm{K_B} \times (R_{\mathrm{K12}} - R_{\mathrm{V}}) + R_{\mathrm{V}} \approx R_{\mathrm{K12}} \times \mathrm{K_B}$$

$$R_{\mathrm{I,ACTR}} = R_{\mathrm{I}} \times \mathrm{K_B}/2$$

$$I_{\mathrm{K2,ACTR}} = I_{\mathrm{K2}} \times \mathrm{K_B} \times (R_{\mathrm{K12}} - R_{\mathrm{V}})/(\mathrm{K_B} \times R_{\mathrm{K12}} - R_{\mathrm{V}})$$

$$V_{\mathrm{K2,ACTR}} = V_{\mathrm{LIM,ACTR}} - I_{\mathrm{K2,ACTR}} \times R_{\mathrm{V}}$$

3.4 AC Transmission Characteristics

SLICOFI-2x uses either an IOM-2 or a PCM digital interface. In receive direction, *SLICOFI-2x* converts PCM data from the network and outputs a differential analog signal (ACP and ACN) to the SLIC, that amplifies the signal and applies it to the subscriber line. In transmit direction, the transversal (IT) and longitudinal (IL) currents on the line are sensed by the SLIC and fed to the *SLICOFI-2x*. A capacitor separates the transversal line current into DC (IT) and AC (ITAC) components. As ITAC is the sensed transversal (also called metallic) current on the line, it includes both the receive and transmit components. *SLICOFI-2x* separates the receive and transmit components digitally, via a transhybrid circuit. **Figure 22** shows the signal paths for AC transmission between the SLICs and *SLICOFI-2x*:

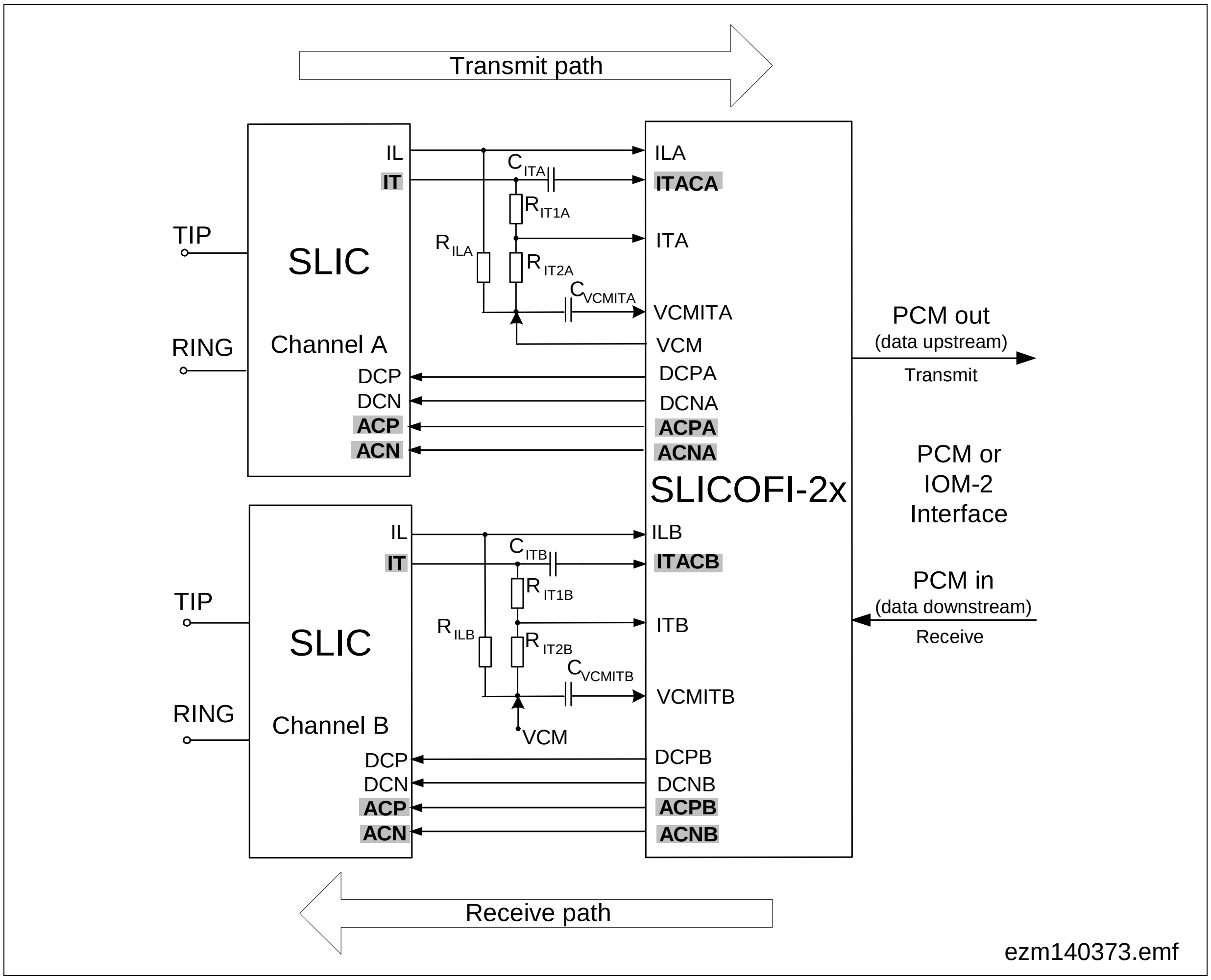
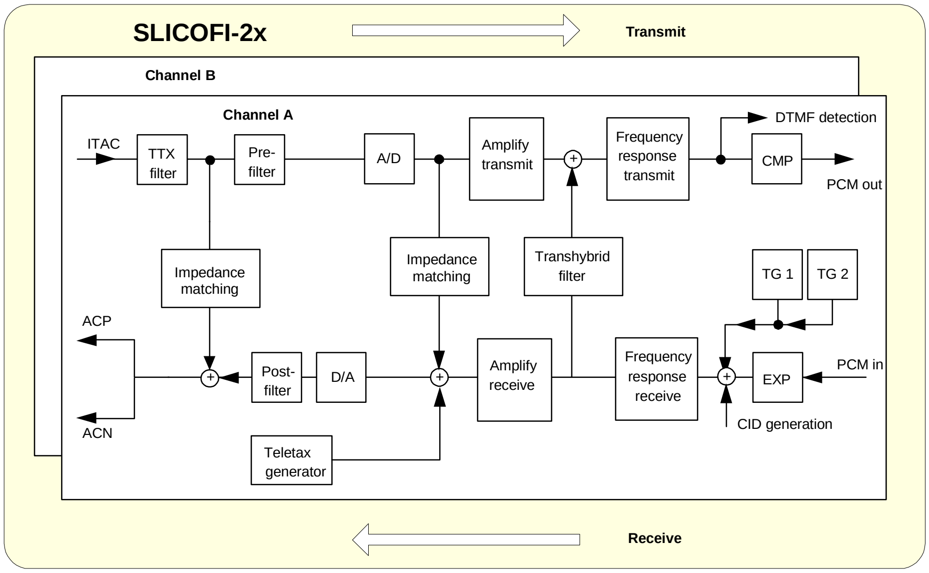

Transmit path
TIP
RING
SLIC
Channel A
IL
IT
DCP
DCN
ACP
ACN
C_{ITA}
R_{IT1A}
R_{ILA}
R_{IT2A}
C_{VCMITA}
ILA
ITACA
ITA
VCMITA
VCM
DCPA
DCNA
ACPA
ACNA
SLICOFI-2x
PCM out
(data upstream)
Transmit
PCM or
IOM-2
Interface
PCM in
(data downstream)
Receive
TIP
RING
SLIC
Channel B
IL
IT
DCP
DCN
ACP
ACN
C_{ITB}
R_{IT1B}
R_{ILB}
R_{IT2B}
C_{VCMITB}
VCM
ILB
ITACB
ITB
VCMITB
DCPB
DCNB
ACPB
ACNB
Receive path
ezm140373.emf

Figure 22 Signal Paths - AC Transmission

The signal flow within the *SLICOFI-2x* for one voice channel is shown in **Figure 23** by the following schematic circuitry. With the exception of a few analog filter functions, signal processing is performed digitally in the *SLICOFI-2x*.


SLICOFI-2x
Transmit
Channel B
Channel A
ITAC
TTX filter
Pre-filter
A/D
Amplify transmit
Frequency response transmit
DTMF detection
CMP
PCM out
Impedance matching
Impedance matching
Transhybrid filter
TG 1
TG 2
ACP
Post-filter
D/A
Amplify receive
Frequency response receive
EXP
PCM in
ACN
CID generation
Teletax generator
Receive

ezm14026.emf

Figure 23 Signal Flow in Voice Channel (A)

3.4.1 Transmit Path

The current sense signal (ITAC) is converted to a voltage by an external resistor. This voltage is first filtered by an anti-aliasing filter (pre-filter), that stops producing noise in the voiceband from signals near the A/D sampling frequency. A/D conversion is done by a 1-bit sigma-delta converter. The digital signal is down-sampled further and routed through programmable gain and filter stages. The coefficients for the filter and gain stages can be programmed to meet specific requirements. The processed digital signal goes through a compander (CMP) that converts the voice data into A-law or µ-law codes. A time slot assignment unit outputs the voice data to the programmed time slot. *SLICOFI-2x* can also operate in 16-bit linear mode for processing uncompressed voice data. In this case, two time slots are used for one voice channel.

3.4.2 Receive Path

The digital input signal is received via the IOM-2 or PCM interface. Expansion (EXP), PCM low-pass filtering, frequency response correction and gain correction are performed by the DSP. The digital data stream is up-sampled and converted to a corresponding analog signal. After smoothing by post-filters in the *SLICOFI-2x*, the AC signal is fed to the SLIC, where it is superimposed on the DC signal. The DC signal has been processed in a separate DC path. A TTX signal, generated digitally within *SLICOFI-2x*, can also be added.

3.4.3 Impedance Matching

The SLIC outputs the voice signal to the line (receive direction) and also senses the voice signal coming from the subscriber. The AC impedance of the SLIC and the load impedance need to be matched in order to maximize power transfer and minimize two-wire return loss. The two-wire return loss is a measure of the impedance matching between a transmission line and the AC termination of DuSLIC.

Impedance matching is done digitally within *SLICOFI-2x* by providing three impedance matching feedback loops. The loops feed the transmit signal back to the receive signal simulating the programmed impedance through the SLIC. When calculating the feedback filter coefficients, the external resistors between the protection network and SLIC ($R_{\mathrm{PRE}} = R_{\mathrm{PROT}} + R_{\mathrm{STAB}}$, see **Figure 100**, **Page 372**) have to be taken into account. The impedance can be programmed to any appropriate real and complex values shown in the Nyquist diagram **Figure 24**. This means that the device can be adapted to requirements anywhere in the world without requiring the hardware changes that are necessary with conventional line card designs.

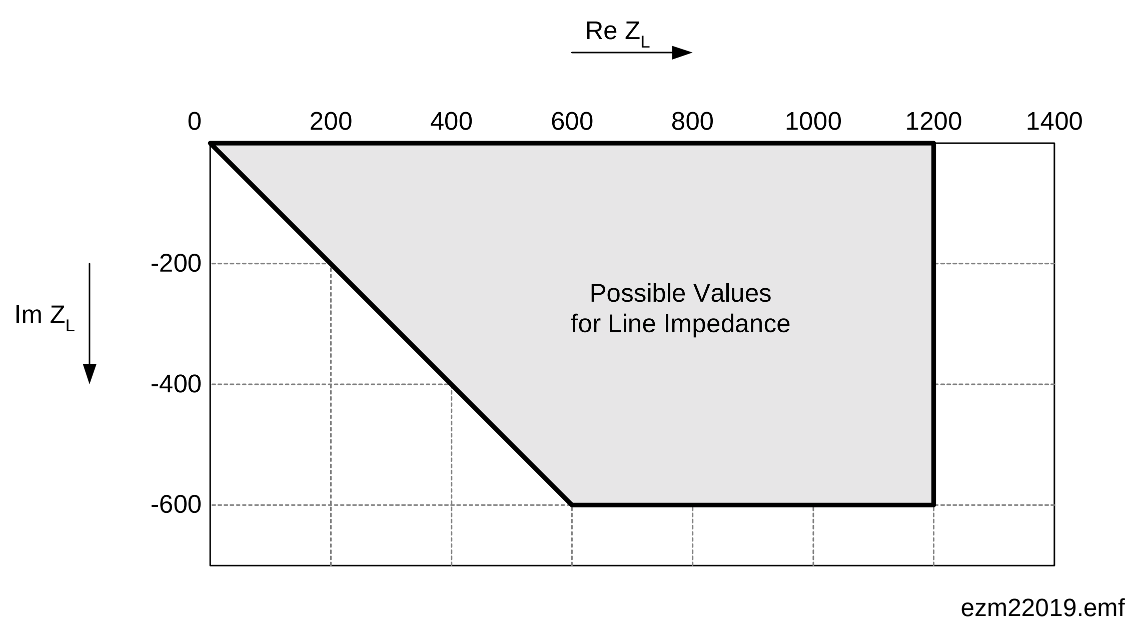


Figure 24 **Nyquist Diagram**

3.5 Ringing

With the 170 V technology used for the SLIC, a ringing voltage of up to 85 Vrms can be generated on-chip without the need for an external ringing generator. The *SLICOFI-2x* generates a sinusoidal ringing signal that causes less noise and cross-talk in neighboring lines than a trapezoidal ringing signal. The ringing frequency is programmable from 3 to 300 Hz.

SLIC-E/-E2, SLIC-S/-S2 and SLIC-P support different ringing methods (see **Chapter 3.5.3**).

3.5.1 Ringer Load

A typical ringer load can be thought of as a resistor in series with a capacitor. Ringer loads are usually described as a REN (Ringer Equivalence Number) value. REN is used to describe the on-hook impedance of the terminal equipment, and is actually a dimensionless ratio that reflects a certain load. REN definitions vary from country to country. A commonly used REN is described in FCC part 68 that defines a single REN as either 5 kΩ, 7 kΩ or 8 kΩ of AC impedance at 20 Hz. The impedance of an n-multiple REN is equivalent to parallel connection of n single RENs. In this manual, all references to REN assume the 7 kΩ model.

For example, a 1 REN and 5 REN load would be:

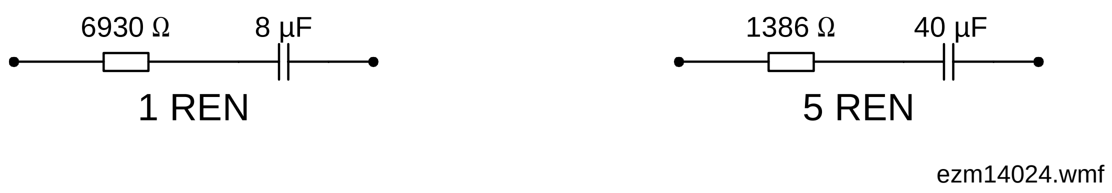


Figure 25 Typical Ringer Loads of 1 and 5 REN Used in US

3.5.2 Ring Trip

Once the subscriber has gone off-hook, the ringing signal must be removed within a specified time, and power must start feeding to the subscriber's phone. There are two ring trip methods:

DC Ring Trip Detection

Most applications with DuSLIC are using DC ring trip detection. By applying a DC offset together with the ringing signal, a transversal DC loop current starts to flow when the subscriber goes off-hook. This DC current is sensed by the SLIC and in this way used as an off-hook criterion. The SLIC supplies this information to the *SLICOFI-2x* at the IT pin. The *SLICOFI-2x* continuously integrates the sensed line current I_{TRANS} over one ringer period. This causes the integration result to represent the DC component of the ring current. If the DC current exceeds the programmed ring trip threshold, *SLICOFI-2x* generates an interrupt. Ring trip is reliably detected and reported within two ring signal periods. The ringing signal is switched off automatically at zero crossing by the *SLICOFI-2x*. The threshold for the ring trip DC current is set internally in *SLICOFI-2x*, programmed via the digital interface. The DC offset for ring trip detection can be generated by the DuSLIC chip set and the internal ring trip function can be used, even if an external ringing generator is used.

AC Ring Trip Detection

For short lines (< 1 kΩ loop length) and for low-power applications, the DC offset can be avoided to reduce the battery voltage for a given ring amplitude. Ring trip detection is done by rectifying the ring current I_{TRANS}, integrating it over one ringer period and comparing it to a programmable AC ring trip threshold. If the ring current exceeds the programmed threshold the HOOK bit in register INTREG1 is set accordingly.

Most applications with DuSLIC are using DC ring trip detection, which is more reliable than AC ring trip detection.

3.5.3 Ringing Methods

There are two methods of ringing:

- Balanced ringing (bridged ringing)
- Unbalanced ringing (divided ringing)

Internal balanced ringing generally offers more benefits compared to unbalanced ringing:

- Balanced ringing produces much less longitudinal voltage, which results in a lower amount of noise coupled into adjacent cable pairs
- By using a differential ringing signal, lower supply voltages become possible

The phone itself cannot distinguish between balanced and unbalanced ringing. Where unbalanced ringing is still used, it is often simply a historical leftover. For a comparison between balanced and unbalanced ringing see also ANSI document T1.401-1993.

Additionally, integrated ringing with the DuSLIC offers the following advantages:

- Internal ringing (no need for external ringing generator and relays)
- Reduction of board space because of much higher integration and fewer external components
- Programmable ringing amplitude, frequency and ringing DC offset without hardware changes
- Programmable ring trip thresholds
- Switching off the ringing signal at zero-crossing

3.5.4 DuSLIC Ringing Options

Application requirements differ with regard to ringing amplitudes, power requirements, loop length and loads. The DuSLIC options include three different SLICs to select the most appropriate ringing methods (see **Table 6**):

Table 6 Ringing Options with SLIC-S, SLIC-E/-E2 and SLIC-P

SLIC Version/ Ringing Facility, Battery Voltages	**SLIC-S PEB 4264**	**SLIC-E/-E2 PEB 4265 PEB 4265-2**	**SLIC-P PEB 4266**
Internal balanced ringing max. voltage in Vrms (sinusoidal) with 20 V_{DC} used for ring trip detection	45 Vrms	85 Vrms	85 Vrms
DC voltage for balanced ringing[1]	programmable typ. 0 … 50 V	programmable typ. 0 … 50 V	programmable typ. 0 … 50 V
Internal unbalanced ringing max. voltage in Vrms (sinusoidal)	NO	NO	50 Vrms
DC voltage for unbalanced ringing	NO	NO	$V_{BATR}/2$
Required SLIC supply voltages for maximum ringing amplitude (typically)	V_{DD} = 5 V, V_{BATH} = – 54 V, V_{HR} = 36 V	V_{DD} = 5 V, V_{BATH} = – 70 V, V_{HR} = 80 V	V_{DD} = 5 V or 3.3 V, V_{BATH} = – 70 V, V_{BATR} = – 150 V
Number of battery voltages for power saving	2 (V_{BATL} & V_{BATH})	2 (V_{BATL} & V_{BATH})	2 (when internal ringing is used) 3 (when external ringing is used)

[1] In most applications 20 V_{DC} are sufficient for reliable ring trip detection. A higher DC voltage will reduce the achievable maximum ringing voltage. For short loops 10 V_{DC} may be sufficient.

SLIC-S allows balanced ringing up to 45 Vrms and is dedicated for short loop or PBX applications.

For SLIC-S2 only external ringing is provided.

SLIC-E/-E2 allows balanced ringing up to 85 Vrms and can therefore be used in systems with higher loop impedance.

The low-power SLIC-P is optimized for power-critical applications (e.g. intelligent ISDN network termination). Internal ringing can be used up to 85 Vrms balanced or 50 Vrms unbalanced. For lowest power applications where external ringing is preferred, three different battery voltages (V_{BATR}, V_{BATH}, V_{BATL}) can be used for optimizing the power consumption of the application.[1]

SLIC-E/-E2 and SLIC-P differ in supply voltage configuration and the ring voltages at Tip and Ring V_T and V_R. External ringing is supported by both SLIC's.

Both internal and external ringing is activated by switching the DuSLIC to ringing mode by setting the CIDD/CIOP bits M2, M1, M0 to 101.

External Ringing Support by DuSLIC

The following settings have to be made:

- Enabling the use of an external ring signal generator by setting bit REXT-EN in Register BCR2 to 1.
- A TTL compatible zero crossing signal has to be applied to the RSYNC pin of the *SLICOFI-2x* (see **Figure 26**).
- Activating the ringing mode by setting the CIDD/CIOP bits M2, M1, M0 to 101.
- Setting the DuSLIC internal ring frequency to a value according a factor of about 0.75 of the external ring frequency.

The ring relay is controlled by the IO1 pin (see **Figure 100**). Due to the high current drive capability of the IO1 ouput, no additional relay driver is necessary.

The relay is switched:

- **Synchronous** to the zero crossing of the external ringing frequency
  (bit ASYNCH-R in register XCR set to 0)

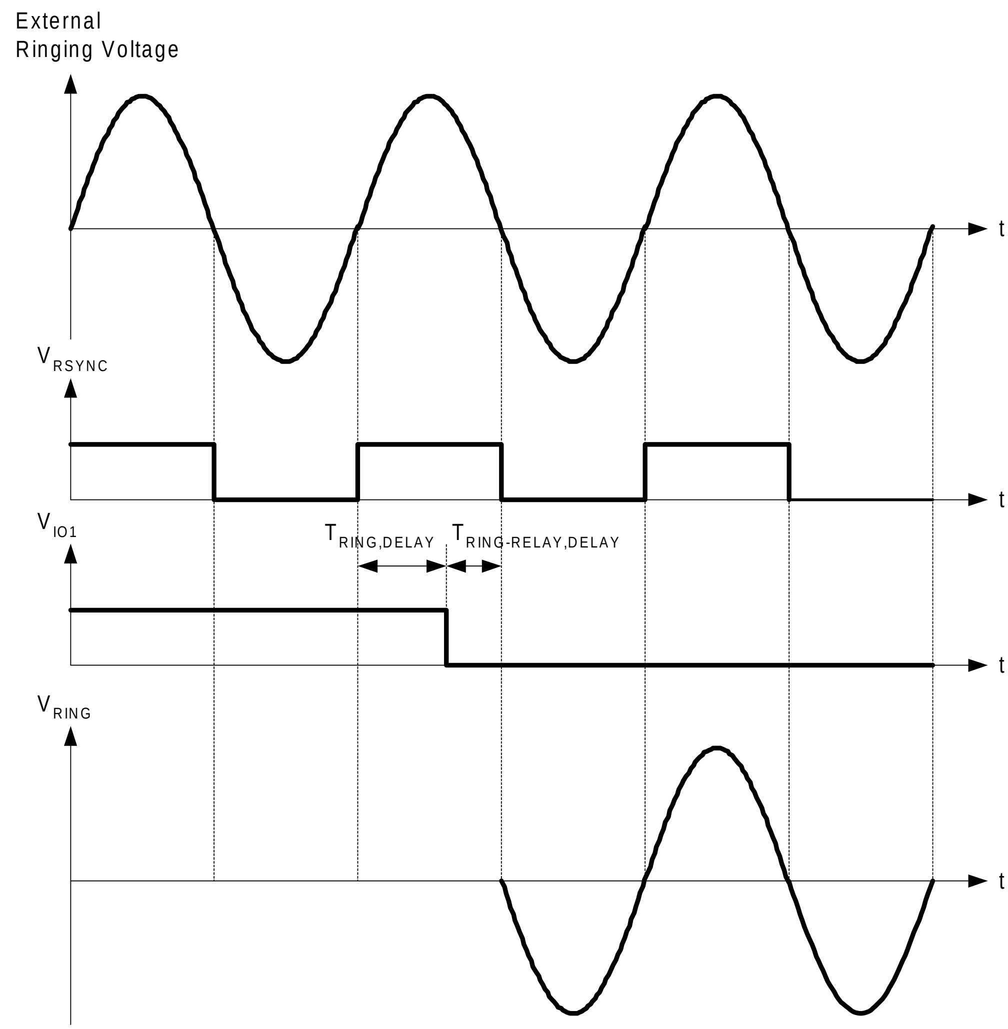
A ring generator delay $T_{RING,DELAY}$ (see DuSLICOS control parameters 2/3) can be programmed to consider the ring relay delay $T_{RING-RELAY,DELAY}$ as shown in **Figure 26**.

- **Asynchronous**
  (bit ASYNCH-R in register XCR set to 1)

The ring relay is switched immediately with the ring command.

---

[1] In this case V_{BATR} is typically used for the on-hook state, while V_{BATH} and V_{BATL} are used for optimized feeding of different loop length in the off-hook state.


External
Ringing Voltage
t
V RSYNC
t
V IO1
T RING,DELAY
T RING-RELAY,DELAY
t
V RING
t

duslic_0015_zero_crossing.emf

Figure 26 External Ringing Zero Crossing Synchronization

3.5.5 Internal Balanced Ringing via SLICs

SLIC-E/-E2 and SLIC-P support internal balanced ringing up to $V_{RING,RMS}$ = 85 Vrms, SLIC-S support balanced ringing up to $V_{RING,RMS}$ = 45 Vrms[1].

The ringing signal is generated digitally within *SLICOFI-2x*[2].

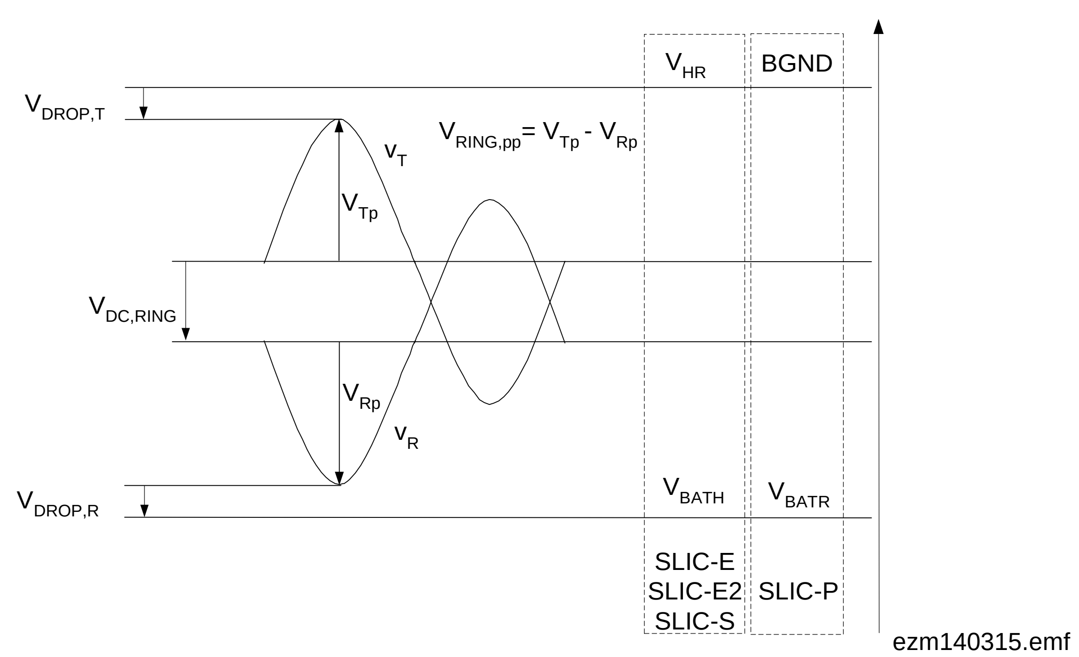


Figure 27 Balanced Ringing via SLIC-E/-E2, SLIC-S and SLIC-P

In ringing mode, the DC feeding regulation loop is not active. A programmable DC ring offset voltage is applied to the line instead. During ring bursts, the ringing DC offset and the ringing signal are summed digitally within *SLICOFI-2x* in accordance with the programmed values. This signal is then converted to an analog signal and applied to the SLIC. The SLIC amplifies the signal and supplies the line with ringing voltages up to 85 Vrms. In balanced ringing mode, the SLIC uses an additional supply voltage V_{HR} for SLIC-E/-E2/-S and V_{BATR} for SLIC-P. The total supply span is now $V_{HR} - V_{BATH}$ for SLIC-E/-E2/-S and V_{BATR} for SLIC-P.

The maximum ringing voltage that can be achieved is:

for SLIC-E/-E2/-S: $V_{RING,RMS} = (V_{HR} - V_{BATH} - V_{DROP,\,RT} - V_{DC,RING})/1.41$

for SLIC-P: $V_{RING,RMS} = (- V_{BATR} - V_{DROP,RT} - V_{DC,RING})/1.41$

where: $V_{DROP,RT} = V_{DROP,T} + V_{DROP,R}$

---

[1] In this case $V_{RING,RMS} = V_{RT,RMS} = V_{RT0,RMS}$ because of the low impedance of the SLIC output (< 1 Ω). $V_{RT,RMS}$ is the open-circuit rms voltage measured directly at pins RING and TIP at the SLIC output with ringer load. $V_{RT0,RMS}$ is the rms voltage measured directly at pins RING and TIP at the SLIC output without any ringer load. For calculation of the ringing voltage at the ringer load see the Voltage and Power Application Note and the accompanying MS Excel Sheet for calculation.

[2] SLICOFI-2S2 supports only external ringing

With the DuSLIC ringing voltages up to 85 Vrms sinusoidal can be applied, but also trapezoidal ringing can be programmed.
For a detailed application diagram of internal balanced ringing refer to the chapter on "Application Circuits" (see **Figure 97**, **Page 368**).

3.5.6 Internal Unbalanced Ringing with SLIC-P

The internal unbalanced ringing together with SLIC-P can be used for ringing voltages up to 50 Vrms. The SLICOFI-2 integrated ringing generator is used and the ringing signal is applied to either the Tip or Ring line. Ringing signal generation is the same as described above for balanced ringing. Since only one line is used for ringing, technology limits the ringing amplitude to about half the value of balanced ringing, to maximum 50 Vrms.

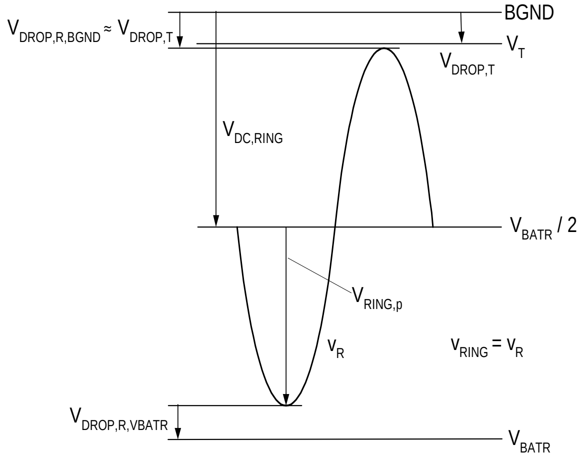


Figure 28 Unbalanced Ringing Signal

The above diagram shows an example with the ring line used for ringing and the Tip line fixed at $-V_{DROP,T}$ which is the drop in the output buffer of the Tip line of SLIC-P (typ. < 1 V). The ring line has a fixed DC voltage of $V_{BATR}/2$ used for ring trip detection.

The maximum ringing voltage is:

$$V_{RING,RMS} = (-V_{BATR} - V_{DROP,R,VBATR} - V_{DROP,T})/2.82$$

When the called subscriber goes off-hook, a DC path is established from the Ring to the Tip line. The DC current is recognized by the SLICOFI-2 because it monitors the IT pin. An interrupt indicates ring trip if the line current exceeds the programmed threshold.

The same hardware can be used for integrated balanced or unbalanced ringing. The balanced or unbalanced modes are configured by software. The maximum achievable amplitudes depend on the values selected for V_{BATR}.

In both balanced and unbalanced ringing modes, SLICOFI-2 automatically applies and removes the ringing signal during zero-crossing. This reduces noise and cross-talk to adjacent lines.

3.5.7 External Unbalanced Ringing

SLICOFI-2x supports external ringing for higher unbalanced ringing voltage requirements above 85 Vrms with all SLICs. For a detailed application diagram of unbalanced ringing see **Figure 100** and **Figure 101** on **Page 372** and **Page 373**.

Since high voltages are involved, an external relay should be used to switch the RING line off and to switch the external ringing signal together with a DC voltage to the line. The DC voltage has to be applied for the internal ring trip detection mechanism which operates for external ringing in the same way as for internal ringing.

The *SLICOFI-2x* has to be set to the external ringing mode by the REXT-EN bit in register BCR2. A synchronization signal of the external ringer is applied to the *SLICOFI-2x* via the RSYNC pin. The external relay is switched on or off synchronously to this signal via the IO1 pin of the *SLICOFI-2x* according to the actual mode of the DuSLIC. An interrupt is generated if the DC current exceeds the programmed ring trip threshold.

3.6 Signaling (Supervision)

Signaling in the subscriber loop is monitored internally by the DuSLIC chip set.

Supervision is performed by sensing the longitudinal and transversal line currents on the Ring and Tip wires. The scaled values of these currents are generated in the SLIC and fed to the *SLICOFI-2x* via the IT and IL pins.

Transversal line current: $I_{\mathrm{TRANS}} = (I_{\mathrm{R}} + I_{\mathrm{T}})/2$

Longitudinal line current: $I_{\mathrm{LONG}} = (I_{\mathrm{R}} - I_{\mathrm{T}})/2$

where I_{R}, I_{T} are the loop currents on the Ring and Tip wires.

Off-hook Detection

Loop start signaling is the most common type of signaling. The subscriber loop is closed by the hook switch inside the subscriber equipment.

- In Active mode, the resulting transversal loop current is sensed by the internal current sensor in the SLIC. The IT pin of the SLIC indicates the subscriber loop current to the *SLICOFI-2x*. External resistors (R_{IT1}, R_{IT2}, see **Figure 97**, **Page 368**) convert the current information to a voltage on the ITA (or ITB) pin.
  The analog information is first converted to a digital value. It is then filtered and processed further which effectively suppresses line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.

- In Sleep/Power Down mode (PDRx) a similar mechanism is used. In this mode, the internal current sensor of the SLIC is switched off to minimize power consumption. The loop current is therefore fed and sensed through 5 kΩ resistors integrated in the SLIC (see **Figure 9**, **Figure 10**, **Figure 11**). The information is made available on the IT pin and interpreted by the *SLICOFI-2x*.
  - In Sleep mode, the analog information is fed to an analog comparator integrated in the *SLICOFI-2x* who directly indicates off-hook.
  - In Power Down mode, the *SLICOFI-2x* converts the analog information to a digital value. It is then filtered and processed further which effectively suppresses line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.

In applications using ground start signaling, DuSLIC can be set in the ground start mode. In this mode, the Tip wire is switched to high impedance mode. Ring ground detection is performed by the internal current sensor in the SLIC and transferred to the *SLICOFI-2x* via the IT pin.

Ground Key Detection

The scaled longitudinal current information is transferred from the SLIC via the IL pin and the external resistor R_{IL} to *SLICOFI-2x*. This voltage is compared with a fixed threshold value. For the specified R_{IL} (1.6 kΩ, see application circuit **Figure 97**, **Page 368**) this threshold corresponds to 17 mA (positive and negative). After further post-processing, this information generates an interrupt (GNDK bit in the INTREG1 register) and ground key detection is indicated.

The polarity of the longitudinal current is indicated by the GNKP bit in the INTREG1 register. Each change of the GNKP bit generates an interrupt. Both bits (GNDK, GNKP) can be masked in the MASK register.

The post-processing is performed to guarantee ground key detection, even if longitudinal AC currents with frequencies of $16^2/_3$, 50 or 60 Hz are superimposed. The time delay between triggering the ground key function and registering the ground key interrupt will in most cases (f = 50 Hz, 60 Hz) be less than 40 ms.

For longitudinal DC signals, the blocking period can be programmed by the DUP value in register IOCTL3. DC signals with less duration will not be detected. The DUP time is equivalent to the half of the cycle time for the lowest frequency for AC suppression (for values see **Page 189**).

In Power Down mode, the SLIC's internal current sensors are switched off and ground key detection is disabled.

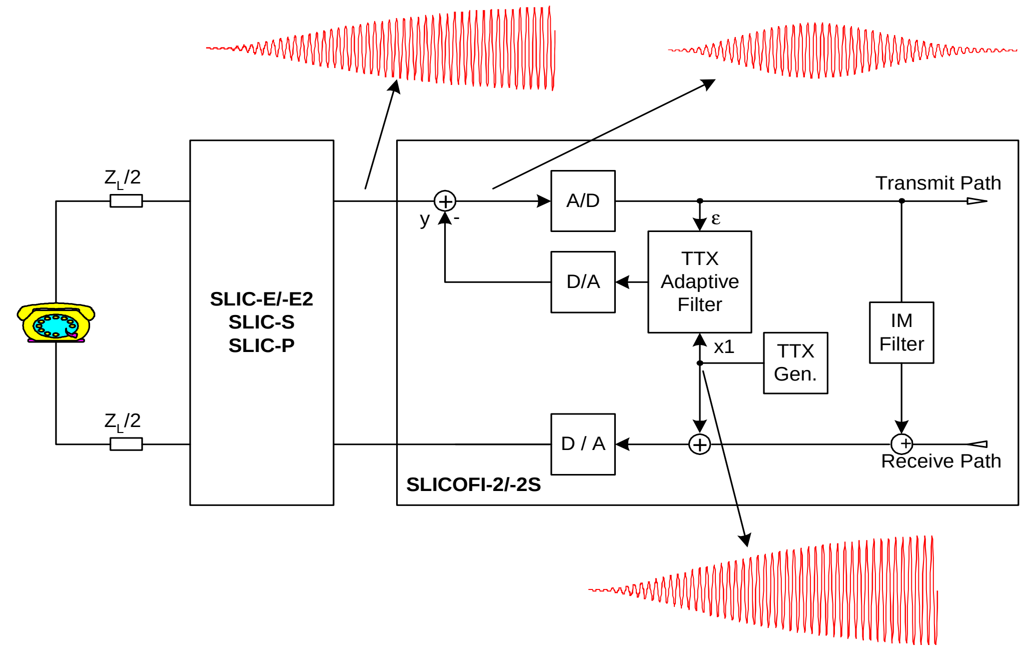
3.7 Metering

There are two different metering methods:

- Metering by sinusoidal bursts with either 12 or 16 kHz or
- Polarity reversal of Tip and Ring.

3.7.1 Metering by 12/16 kHz Sinusoidal Bursts

To satisfy worldwide application requirements, SLICOFI-2/-2S[1] offers integrated metering injection of either 12 or 16 kHz signals with programmable amplitudes. SLICOFI-2/-2S also has an integrated adaptive TTX notch filter and can switch the TTX signal to the line in a smooth way. When switching the signal to the line, the switching noise is less than 1 mV. **Figure 29** shows TTX bursts at certain points of the signal flow within SLICOFI-2/-2S.


$Z_L/2$
$Z_L/2$
SLIC-E/-E2
SLIC-S
SLIC-P
y
-
A/D
Transmit Path
ε
D/A
TTX
Adaptive
Filter
x1
TTX
Gen.
IM
Filter
D / A
Receive Path
SLICOFI-2/-2S

ezm14027.emf

Figure 29 Teletax Injection and Metering

The integrated, adaptive TTX notch filter guarantees an attenuation of > 40 dB. No external components for filtering TTX bursts are required.

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[1] Metering is not available with SLICOFI-2S2

3.7.2 Metering by Polarity Reversal

SLICOFI-2/-2S also supports metering by polarity reversal by changing the actual polarity of the voltages on the TIP/RING lines. Polarity reversal is activated by switching the REVPOL bit in register BCR1 to one or switching to the "Active with Metering" mode by the CIDD or CIOP command (see **"Operating Modes for the DuSLIC Chip Set" on Page 78**).

3.7.2.1 Soft Reversal

Some applications require a smooth polarity reversal (soft reversal), as shown in **Figure 30**. Soft reversal helps to prevent negative effects like non-required ringing. Soft reversal is deactivated by the SOFT-DIS bit in register BCR2.

SOFT-DIS = 1	Immediate reversal is performed (hard reversal)
SOFT-DIS = 0	Soft reversal is performed. Transition time (time from START to SR-END1, see **Figure 30**) is programmable by CRAM coefficients, default value 80 ms.

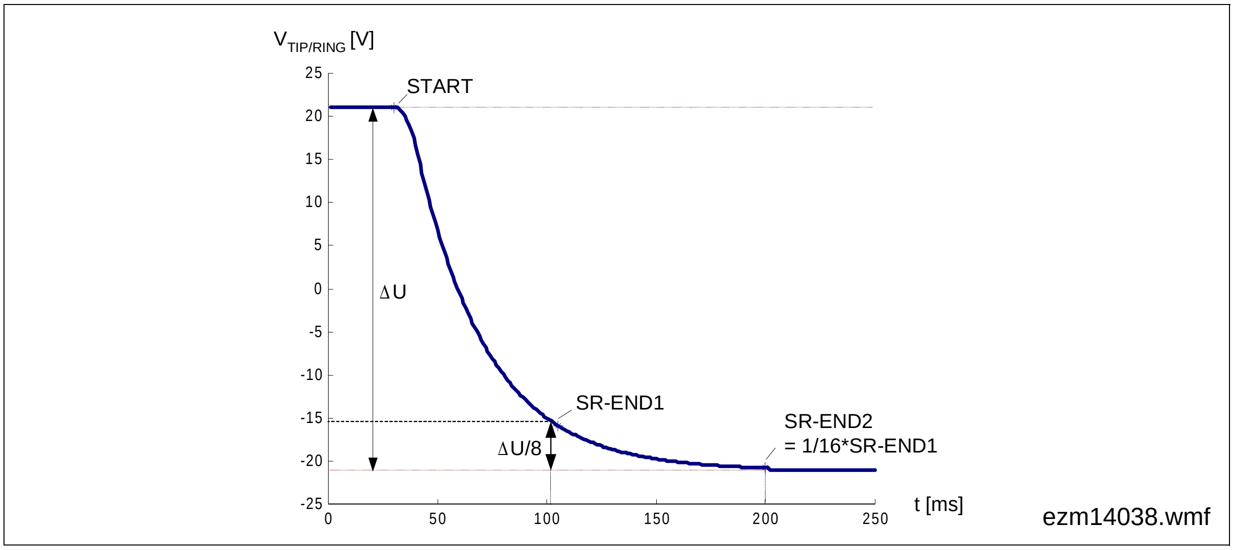


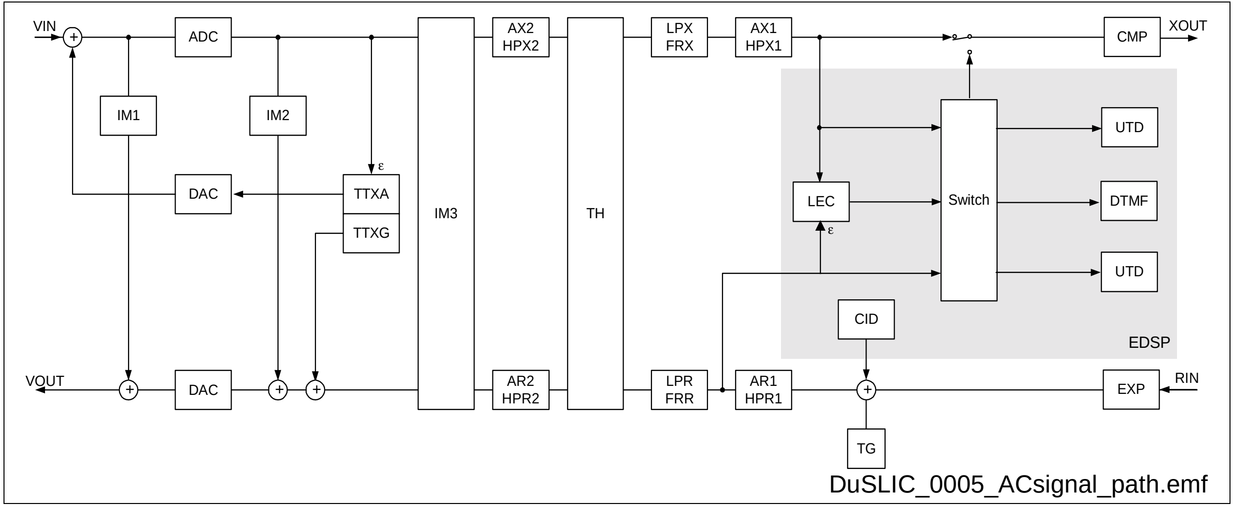
Figure 30 Soft Reversal (Example for Open Loop)

START: The soft ramp starts by setting the REVPOL bit in register BCR1 to 1. The DC characteristic is switched off.
SR-END1: At the soft reversal end one point, the DC characteristic is switched on again. Programmable by the DuSLICOS software, e.g. ΔU/8.
SR-END2: At the soft reversal end two point, the soft ramp is switched off. Programmable by the DuSLICOS software, e.g. 1/16 × SR-END1.
From START to SR-END2 the READY bit in register INTREG2 is set to 0 (see register description in **Chapter 6.3.1.2** for further information).

3.8 DuSLIC Enhanced Signal Processing Capabilities

The signal processing capabilities described in this chapter are realized by an Enhanced Digital Signal Processor (EDSP) except for DTMF generation. Each function can be individually enabled or disabled for each DuSLIC channel. Therefore power consumption can be reduced according to the needs of the application. For the MIPS requirements of the different EDSP algorithms see **Chapter 3.8.5**.

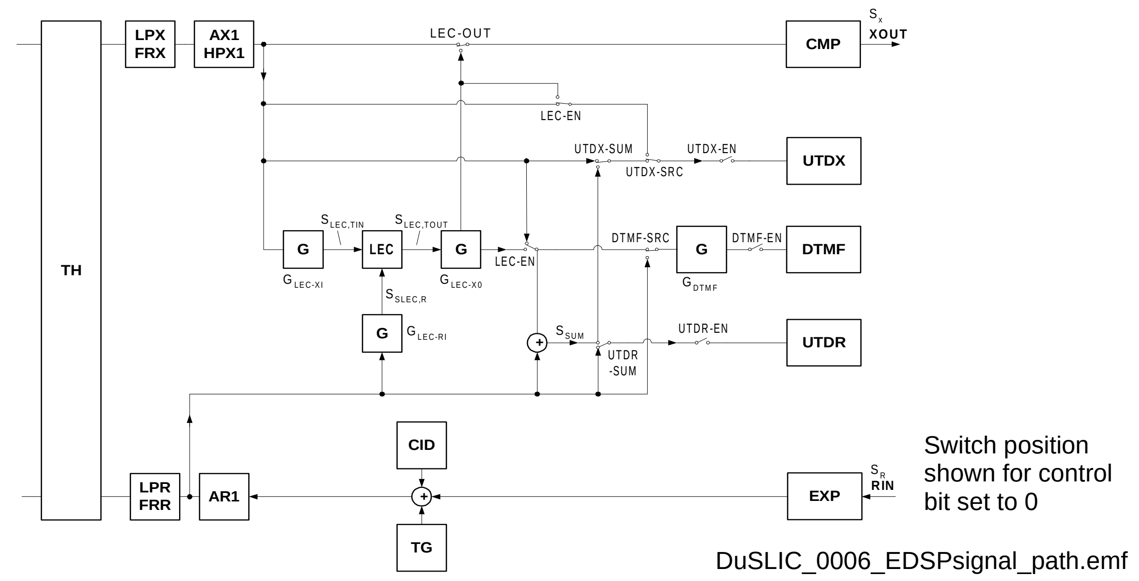
Figure 31 shows the AC signal path for DuSLIC with the ADCs and DACs, impedance matching loop, trans-hybrid filter, gain stages and the connection to the EDSP.


VIN
ADC
AX2
HPX2
LPX
FRX
AX1
HPX1
CMP
XOUT
IM1
IM2
UTD
ε
DAC
TTXA
TTXG
IM3
TH
LEC
Switch
DTMF
ε
UTD
CID
EDSP
VOUT
DAC
AR2
HPR2
LPR
FRR
AR1
HPR1
EXP
RIN
TG

DuSLIC_0005_ACsignal_path.emf

Figure 31 DuSLIC AC Signal Path

Figure 32 shows a closeup on the EDSP signal path shown in **Figure 31** outlining signal names and SOP commands.


TH
LPX
FRX
AX1
HPX1
LEC-OUT
CMP
S_X
XOUT
LEC-EN
UTDX-SUM
UTDX-EN
UTDX-SRC
UTDX
$S_{LEC,TIN}$
$S_{LEC,TOUT}$
G
LEC
G
LEC-EN
DTMF-SRC
G
DTMF-EN
DTMF
G_{LEC-XI}
G_{LEC-XO}
$S_{SLEC,R}$
G_{DTMF}
G
G_{LEC-RI}
S_{SUM}
UTDR-EN
UTDR
UTDR
-SUM
CID
LPR
FRR
AR1
EXP
S_R
RIN
TG

Switch position shown for control bit set to 0

DuSLIC_0006_EDSPsignal_path.emf

Figure 32 DuSLIC EDSP Signal Path

The enhanced Signal Processing Capabilities are available only for the DuSLIC-E/-E2/-P versions, with an exception of DTMF generation.

The DTMF generation is available for all DuSLIC versions.

The functions of the EDSP are configured and controlled by POP register settings (see **Chapter 6.2.3**).

3.8.1 DTMF Generation and Detection[1]

Dual Tone Multi-Frequency (DTMF) is a signaling scheme using voice frequency tones to signal dialing information. A DTMF signal is the sum of two tones, one from a low group (697 - 941 Hz) and one from a high group (1209 - 1633 Hz), with each group containing four individual tones. This scheme allows 16 unique combinations. Ten of these codes represent the numbers from zero through nine on the telephone keypad, the remaining six codes (*, #, A, B, C, D) are reserved for special signaling. The buttons are arranged in a matrix, with the rows determining the low group tones, and the columns determining the high group tone for each button.

In all *SLICOFI-2x* codec versions the 16 standard DTMF tone pairs can be generated independently in each channel via two integrated tone generators. Alternatively the frequency and the amplitude of the tone generators can be programmed individually via the digital interface. Each tone generator can be switched on and off. The generated DTMF tone signals meet the frequency variation tolerances specified in the ITU-T Q.23 recommendation.

Both channels (A and B) of SLICOFI-2[1] have a powerful built-in DTMF decoder that will meet most national requirements. The receiver algorithm performance meets the quality criteria for central office/exchange applications. It complies with the requirements of ITU-T Q.24, Bellcore GR-30-CORE (TR-NWT-000506) and Deutsche Telekom network (BAPT 223 ZV 5, Approval Specification of the Federal Office for Post and Telecommunications, Germany).

The performance of the algorithm can be adapted according to the needs of the application via the digital interface (detection level, twist, bandwidth and center frequency of the notch filter).

---

[1] DTMF Detection only available for DuSLIC-E/-E2/-P

Table 7 shows the performance characteristics of the DTMF decoder algorithm:

Table 7 Performance Characteristics of the DTMF Decoder Algorithm

	Characteristic	Value	Notes
1	Valid input signal detection level	– 48 to 0 dBm0	Programmable
2	Input signal rejection level	– 5 dB of valid signal detection level	–
3	Positive twist accept	< 8 dB	Programmable
4	Negative twist accept	< 8 dB	Programmable
5	Frequency deviation accept	< ± (1.5% + 4 Hz) and < ± 1.8%	Related to center frequency
6	Frequency deviation reject	> ± 3%	Related to center frequency
7	DTMF noise tolerance (could be the same as 14)	– 12 dB	dB referenced to lowest amplitude tone
8	Minimum tone accept duration	40 ms	–
9	Maximum tone reject duration	25 ms	–
10	Signaling velocity	≥ 93 ms/digit	–
11	Minimum inter-digit pause duration	40 ms	–
12	Maximum tone drop-out duration	20 ms	–
13	Interference rejection 30 Hz to 480 Hz for valid DTMF recognition	Level in frequency range 30 Hz … 480 Hz ≤ level of DTMF frequency + 22 dB	dB referenced to lowest amplitude tone
14	Gaussian noise influence Signal level – 22 dBm0, SNR = 23 dB	Error rate better than 1 in 10000	–
15	Pulse noise influence Impulse noise tape 201 according to Bellcore TR-TSY-000762	Error rate better than 14 in 10000	measured with DTMF level – 22 dBm0 Impulse Noise – 10 dBm0 and – 12 dBm0

In the event of pauses < 20 ms:

- If the pause is followed by a tone pair with the same frequencies as before, this is interpreted as drop-out.
- If the pause is followed by a tone pair with different frequencies and if all other conditions are valid, this is interpreted as two different numbers.

DTMF decoders can be switched on or off individually to reduce power consumption. In normal operation, the decoder monitors the Tip and Ring wires via the ITAC pins (transmit path). Alternatively the decoder can be switched also in the receive path. On detecting a valid DTMF tone pair, SLICOFI-2 generates an interrupt via the appropriate INT pin and indicates a change of status. The DTMF code information is provided by a register which is read via the digital interface.

The DTMF decoder also has excellent speech-rejection capabilities and complies with Bellcore TR-TSY-000763. The algorithm has been fully tested with the speech sample sequences in the Series-1 Digit Simulation Test Tapes for DTMF decoders from Bellcore. The characteristics of DTMF detection can be controlled by POP registers 30h to 39h.

3.8.2 Caller ID Generation (only DuSLIC-E/-E2/-P)

A generator to send calling line identification (Caller ID, CID) is integrated in the DuSLIC chip set. Caller ID is a generic name for the service provided by telephone utilities that supply information like the telephone number or the name of the calling party to the called subscriber at the start of a call. In call waiting, the Caller ID service supplies information about a second incoming caller to a subscriber already busy with a phone call.

In typical Caller ID (CID) systems, the coded calling number information is sent from the central exchange to the called phone. This information can be shown on a display on the subscriber telephone set. In this case, the Caller ID information is usually displayed before the subscriber decides to answer the incoming call. If the line is connected to a computer, caller information can be used to search in databases and additional services can be offered.

There are two methods used for sending CID information depending on the application and country-specific requirements:

- Caller ID generation using DTMF signaling (see **Chapter 3.8.1**)
- Caller ID generation using FSK

DuSLIC contains DTMF generation units and FSK generation units which can be used for both channels simultaneously.

The characteristics of the Caller ID generation circuitry can be controlled by POP registers 00h, 43h to 4Ah.

DuSLIC FSK Generation

Different countries use different standards to send Caller ID information. The DuSLIC chip set is compatible with the widely used standards Bellcore GR-30-CORE, British Telecom (BT) SIN227, SIN242 or the UK Cable Communications Association (CCA) specification TW/P&E/312. Continuous phase binary frequency shift keying (FSK) modulation is used for coding which is compatible with BELL 202 (see **Table 8**) and ITU-T V.23, the most common standards. SLICOFI-2 can be easily adapted to these requirements by programming via the microcontroller interface. Coefficient sets are provided for the most common standards.

Table 8 FSK Modulation Characteristics

Characteristic	ITU-T V.23	Bell 202
Mark (Logic 1)	1300 ± 3 Hz	1200 ± 3 Hz
Space (Logic 0)	2100 ± 3 Hz	2200 ± 3 Hz
Modulation	FSK	
Transmission rate	1200 ± 6 baud	
Data format	Serial binary asynchronous	

The Caller ID data of the calling party can be transferred via the microcontroller interface into a SLICOFI-2 buffer register. The SLICOFI-2 will start sending the FSK signal when the CIS-EN bit is set and the CID-data buffer is filled up to CIS-BRS plus 1 byte. The data transfer into the buffer register is handled by a SLICOFI-2 interrupt signal. Caller data is transferred from the buffer via the interface pins to the SLIC-E/-E2/-P and fed to the Tip and Ring wires. The Caller ID data bytes from CID-data buffer are sent LSB first.

DuSLIC offers two different levels of framing:

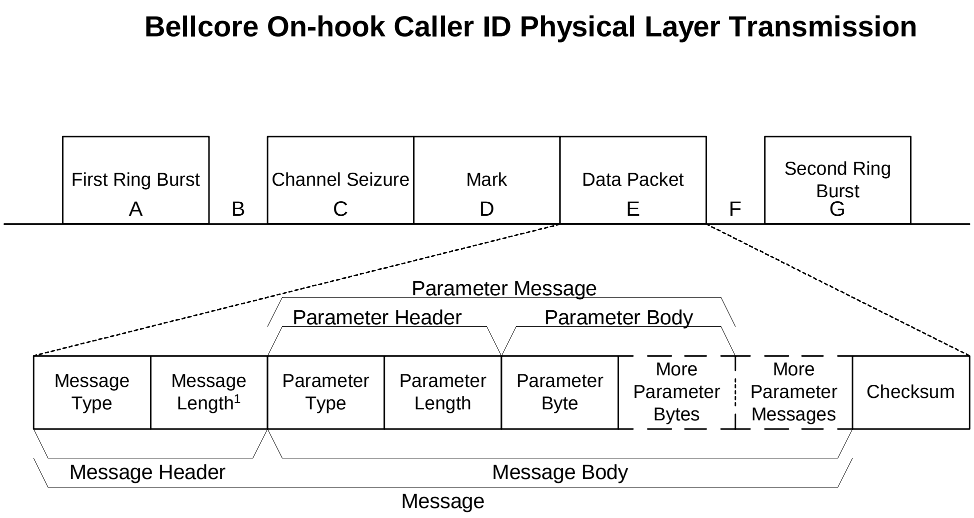
- A basic low-level framing mode

  All the data necessary to implement the FSK data stream – including channel seizure, mark sequence and framing for the data packet or checksum – has to be configured by firmware. SLICOFI-2 transmits the data stream in the same order in which the data is written to the buffer register.

- A high level framing mode

  The number of channel seizure and mark bits can be programmed and are automatically sent by the DuSLIC. Only the data packet information has to be written into the CID buffer. Start and Stop bits are automatically inserted by the SLICOFI-2.

The example below shows signaling of CID on-hook data transmission in accordance with Bellcore specifications. The Caller ID information applied on Tip and Ring is sent during the period between the first and second ring burst.


Bellcore On-hook Caller ID Physical Layer Transmission
First Ring Burst
A
B
Channel Seizure
C
Mark
D
Data Packet
E
F
Second Ring Burst
G
Parameter Message
Parameter Header
Parameter Body
Message Type
Message Length1
Parameter Type
Parameter Length
Parameter Byte
More Parameter Bytes
More Parameter Messages
Checksum
Message Header
Message Body
Message

1 Message length equals the number of bytes to follow in the message body, excluding the checksum.
A: 0.2 - 3 second ring burst
B: 0.5 - 1.5 seconds between first ring burst and start of data transmission
C: 300 alternating mark and space bits
D: 180 mark bits
C + D + E = 2.9 to 3.7 seconds
F: ≥200ms
G: 1.8 - 3 second ring burst

ezm14014.wmf

Figure 33 Bellcore On-hook Caller ID Physical Layer Transmission

3.8.3 Line Echo Cancelling (LEC) (only DuSLIC-E/-E2/-P)

The DuSLIC contains an adaptive line echo cancellation unit for the cancellation of near end echoes. With the adaptive balancing of the LEC unit the Transhybrid Loss can be improved up to a value of about 50 dB. The maximum echo cancellation time selectable is 8 ms. The line echo cancellation unit is especially useful in combination with the DTMF detection unit. In critical situations the performance of the DTMF detection can be improved.

If 8 ms line echo cancellation length (LEC Length) is used, please take care about the MIPS requirements described in **Chapter 3.8.5**.

The DuSLIC line echo canceller is compatible with applicable standards ITU-T G.165 and G.168. An echo cancellation delay time of up to 8 ms can be programmed.

The LEC unit consists basically of an FIR filter, a shadow FIR filter, and a coefficient adaption mechanism between these two filters as shown in **Figure 34**.

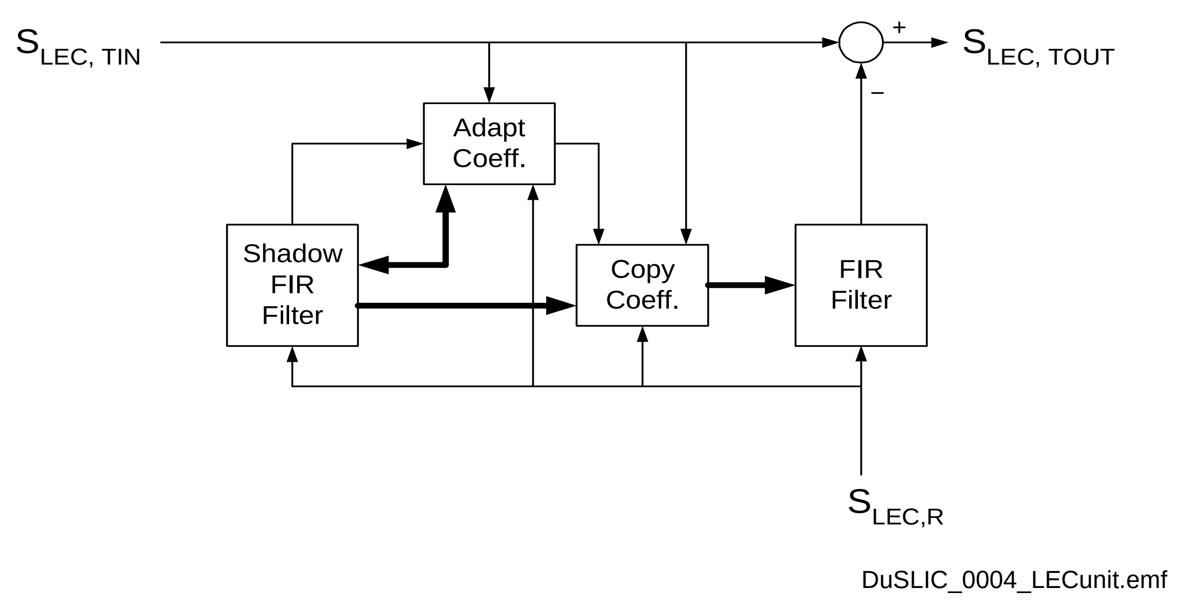


Figure 34 Line Echo Cancelling Unit - Block Diagram

The adaption process is controlled by the three parameters Pow_{LECR} (Power Detection Level Receive), $DeltaP_{LEC}$ (Delta Power) and DeltaQ (Delta Quality) (**“POP Command” on Page 228**). Adaptation takes place only if both of the following conditions hold:

1. $S_{LEC,R} > Pow_{LECR}$
2. $S_{LEC,R} – S_{LEC,TIN} > DeltaP_{LEC}$

With the first condition, adaptation to small signals can be avoided. The second condition avoids adaptation during double talk. The parameter $DeltaP_{LEC}$ represents the echo loss provided by external circuitry.

If the adaptation of the shadow filter is performed better than the adaption of the actual filter by a value of more than DeltaQ then the shadow filter coefficients will be copied to the actual filter.

At the start of an adaption process the coefficients of the LEC unit can be reset to default initial values or set to the old coefficient values. The coefficients may also be frozen.

3.8.4 Universal Tone Detection (UTD) (only DuSLIC-E/-E2/-P)

Each channel of the DuSLIC has two Universal Tone Detection units which can be used to detect special tones in the receive and transmit paths, especially fax or modem tones (e.g., see the modem startup sequence described in recommendation ITU-T V.8).

This allows the use of modem-optimized filter for V.34 and V.90 connections. If the DuSLIC UTD detects that a modem connection is about to be established, the optimized filter coefficients for the modem connection can be downloaded before the modem connection is set up. With this mechanism implemented in the DuSLIC chip set, the optimum modem transmission rate can always be achieved.

Figure 35 shows the functional block diagram of the UTD unit:

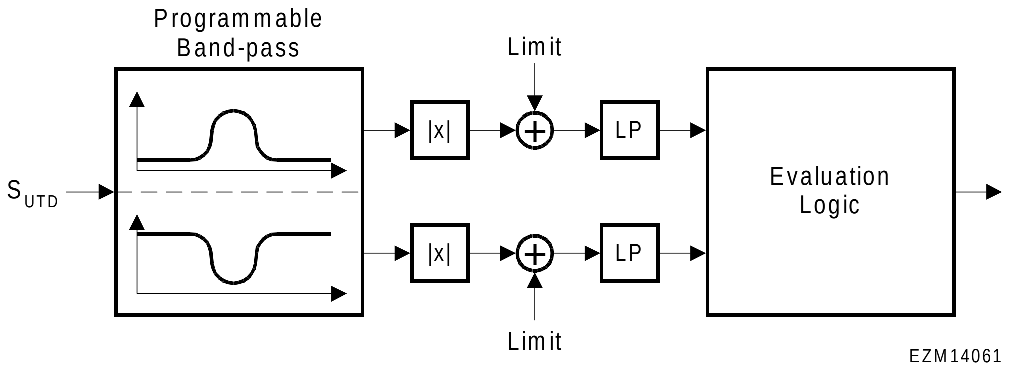


Figure 35 UTD Functional Block Diagram

Initially, the input signal is filtered by a programmable band-pass (center frequency f_C and bandwidth f_{BW}). Both the in-band signal (upper path) and the out-of-band signal (lower path) are determined, and the absolute value is calculated. Both signals are furthermore filtered by a limiter and a low-pass. All signal samples (absolute values) below a programmable limit Lev_N (Noise Level) are set to zero and all other signal samples are diminished by Lev_N. The purpose of this limiter is to increase noise robustness. After the limiter stages both signals are filtered by a fixed low-pass.

The evaluation logic block determines whether a tone interval or silence interval is detected and an interrupt is generated for the receive or transmit path.

The UTDR-OK respectively UTDX-OK bit (register INTREG3) will be set if both of the following conditions hold for a time span of at least RTIME without breaks longer than RBRKTime occurring:

1. The in-band signal exceeds a programmable level Lev_S.
2. The difference of the in-band and the out-of-band signal levels exceeds $Delta_{UTD}$.

The UTDR-OK respectively UTDX-OK bit will be reset if at least one of these conditions is violated for a timespan of at least ETime during which the violation does not cease for at least EBRKTime.

The times ETIME and EBRKTime help to reduce the effects of sporadic dropouts.

If the bandwidth parameter is programmed to a negative value, the UTD unit can be used for the detection of silence intervals in the whole frequency range.

The DuSLIC UTD unit is compatible with ITU-T G.164.

The UTD is resistant to a modulation with 15 Hz sinusoidal signals and a phase reversal but is not able to detect the 15 Hz modulation and the phase reversal.

3.8.5 MIPS Requirements for EDSP Capabilities

Table 9 shows the MIPS requirements for each algorithm using the EDSP:

Table 9 MIPS Requirements

Algorithm / Device	Used MIPS	Conditions
Caller ID Sender (CIS)	$1.736 * n_{CIS}$	$n_{CIS} = 0...2$
Universal Tone Detection (UTD)	$1.208 * n_{UTD}$	$n_{UTD} = 0...4$, transmit and receive for two channels
DTMF Receiver	$6.296 * n_{DTMF}$	$n_{DTMF} = 0...2$
Line Echo Canceller (LEC)	$(3.448 + 0.032 * LEN) * n_{LEC}$	$n_{LEC} = 0...2$ LEN - see **Page 239**
Operating System	1.432	–

The maximum capability of the EDSP is 32 MIPS.

Example:

- All devices enabled and LEC Length = 8 ms (LEN = 64):
  → 33.32 MIPS total computing load exceeding the 32 MIPS limit!
- All devices enabled and LEC Length = 4 ms (LEN = 32):
  → 31.272 MIPS total computing load within the 32 MIPS limit.
- 4 x UTD, 2 x DTMF Receiver and 2 x LEC (8 ms) enabled:
  → 29.85 MIPS total computing load within the 32 MIPS limit.

3.9 Message Waiting Indication (only DuSLIC-E/-E2/-P)

Message Waiting Indication (MWI) is usually performed using a glow lamp at the subscriber phone. Current does not flow through a glow lamp until the voltage reaches a threshold value above approximately 80 V. At this threshold, the neon gas in the lamp will start to glow. When the voltage is reduced, the current falls under a certain threshold and the lamp glow is extinguished. DuSLIC has high-voltage SLIC technology (170 V) which is able to activate the glow lamp without any external components.

The hardware circuitry is shown in **Figure 36** below. The figure shows a typical telephone circuit with the hook switch in the on-hook mode, together with the impedances for the on-hook (Z_R) and off-hook (Z_L) modes.

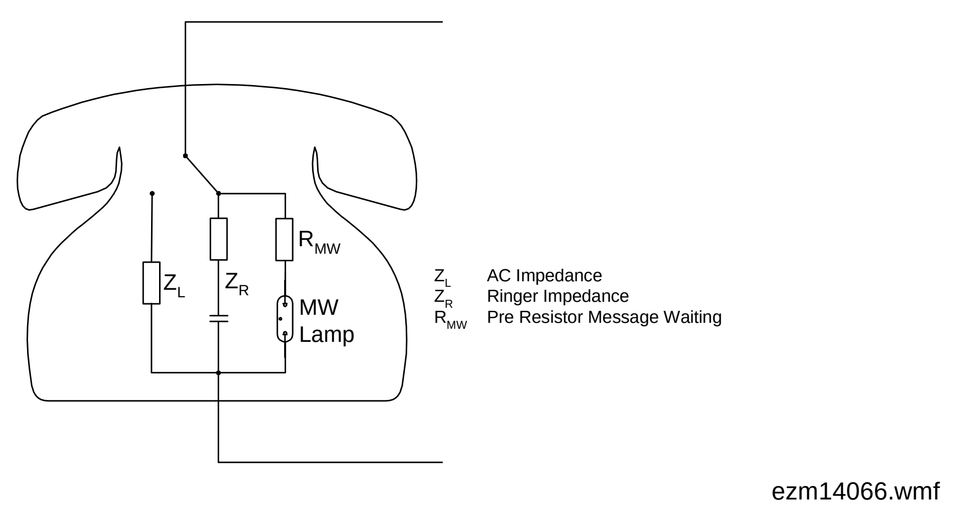


Figure 36 MWI Circuitry with Glow Lamp

The glow lamp circuit also requires a resistor (R_{MW}) and a lamp (MW Lamp) built into the phone. When activated, the lamp must be able to either blink or remain on constantly.

In non-DuSLIC solutions the telephone ringer may respond briefly if the signal slope is too steep, which is not desirable. DuSLIC's integrated ramp generator can be programmed to increase the voltage slowly, to ensure activating the lamp and not the ringer.

To activate the Message Waiting function of DuSLIC the following steps should be performed:

- Activating Ring Pause mode by setting the M0-M2 bits
- Select Ring Offset RO2 by setting the bits in register LMCR3
- Enable the ramp generator by setting bit RAMP-EN in register LMCR2
- Switching between the Ring Offsets RO3 and RO2 in register LMCR3 will flash the lamp on and off (see **Figure 37**).

The values for RO2 and RO3 have to be programmed in the CRAM to the according values before so that the lamp will flash on and off.

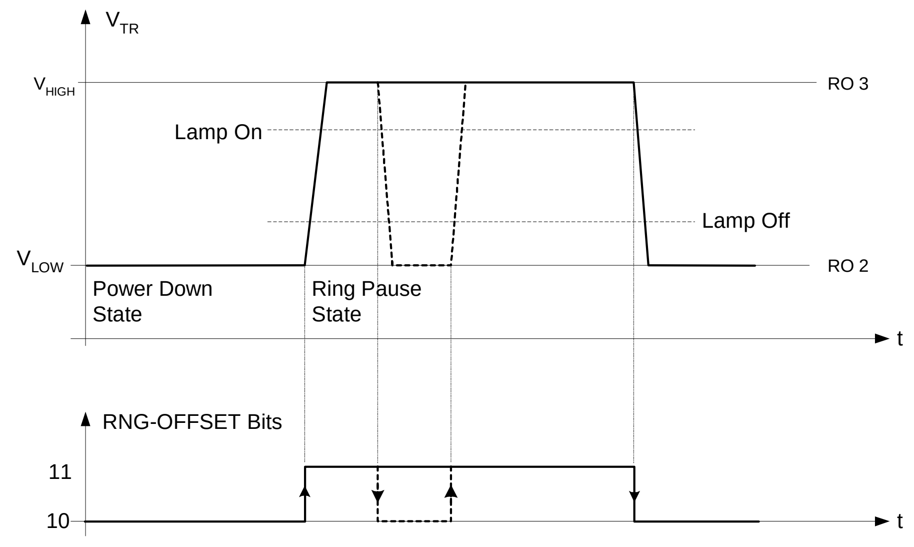

V_{TR}
V_{HIGH}
RO 3
Lamp On
Lamp Off
V_{LOW}
RO 2
Power Down State
Ring Pause State
t
RNG-OFFSET Bits
11
10
t

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Figure 37 Timing Diagram

3.10 Three-party Conferencing (only DuSLIC-E/-E2/-P)

Each DuSLIC channel has a three-party conferencing facility implemented which consist of four PCM registers, adders and gain stages in the microprogram and the corresponding control registers (see **Figure 38**).

This facility is available in PCM/µC mode only. The PCM control registers PCMR1 through PCMR4 and PCMX1 through PCMX4 control the timeslot assignment and PCM highway selection, while the bits PCMX-EN, CONF-EN and CONFX-EN in the BCR3 register control the behavior of the conferencing facility and the PCM line drivers (see **Figure 38**). A programmable gain stage G is able to adjust the gain of the conferencing voice data (B, C, D, S) in a range of – 6 dB to + 3 dB to prevent an overload of the sum signals.

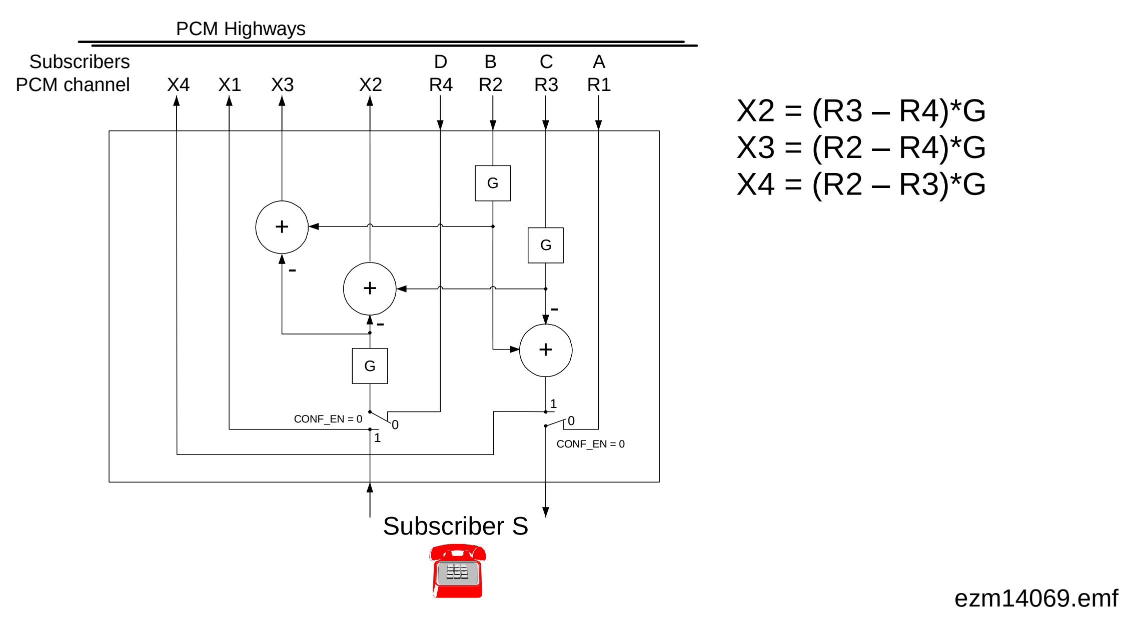
PCM Highways
Subscribers
PCM channel
X4
X1
X3
X2
D
R4
B
R2
C
R3
A
R1
X2 = (R3 – R4)*G
X3 = (R2 – R4)*G
X4 = (R2 – R3)*G
G
G
G
+
+
+
-
-
-
CONF_EN = 0
0
1
1
0
CONF_EN = 0
Subscriber S
ezm14069.emf

Figure 38 Conference Block for One DuSLIC Channel

Note: G … Gain Stage (Gain Factor) set in CRAM coefficients,
X1 - X4 … PCM transmit channels,
R1 - R4 … PCM receive channels,
A, B, C, D, S … examples for voice data on PCM channels X1 - X4, R1 - R4

3.10.1 Conferencing Modes

Table 10 Conference Modes

	Configuration Registers			Receive Channels				Transmit Channels				
Mode	PCMX -EN	CONF -EN	CONFX -EN	R1	R2	R3	R4	X1	X2	X3	X4	Subscriber S
PCM Off	0	0	0	–	–	–	–	off	off	off	off	off
PCM Active	1	0	0	A	–	–	–	S	off	off	off	A
External Conference	0	0	1	–	B	C	D	off	G (C+D)	G (B+D)	G (B+C)	off
External Conference + PCM Active	1	0	1	A	B	C	D	S	G (C+D)	G (B+D)	G (B+C)	A
Internal Conference	0	1	0	–	B	C	–	off	G (C+S)	G (B+S)	off	G (B+C)

(see also **“Control of the Active PCM Channels” on Page 142**)

- **PCM Off**
  After a reset, or in power down there is no communication via the PCM highways. Also when selecting new timeslots it is recommended to switch off the PCM line drivers by setting the control bits to zero.
- **PCM Active**
  This is the normal operating mode without conferencing. Only the channels R1 and X1 are in use, and voice data are transferred from subscriber A to analog subscriber S and vice versa.
- **External Conference**
  In this mode the SLICOFI-2 acts as a server for a three-party conference of subscribers B, C and D which may be controlled by any device connected to the PCM highways. The SLICOFI-2 channel itself can remain in power down mode to lower power consumption.
- **External Conference + PCM Active**
  Like in External Conference mode any external three-party conference is supported. At the same time an internal phone call is active using the channels R1 and X1.
- **Internal Conference**
  If the analog subscriber S is one of the conference partners, the internal conference mode will be selected. The partners (B, C) do not need any conference facility, since the SLICOFI-2 performs all required functions for them as well.

3.11 16 kHz Mode on PCM Highway

In addition to the standard 8 kHz transmission PCM interface modes, there are also two 16 kHz modes for high data transmission performance.

Table 11 shows the configuration of PCM channels for the different PCM interface modes.

Table 11 Possible Modes in PCM/µC Interface Mode1)

Config. Bits		**Receive PCM Channels**					**Transmit PCM Channels**				
PCM16K	**LIN**	**R1**	**R1L2)**	**R2**	**R3**	**R4**	**X1**	**X1L3)**	**X2**	**X3**	**X4**
PCM Mode											
0	0	A	4)	B	C	D	S	–	depends on conference mode		
LIN Mode											
0	1	A-HB	A-LB	B	C	D	S-HB	S-LB	depends on conference mode		
PCM16 Mode											
1	0	DS1	–	–	DS2	–	DS1	–	–	DS2	–
LIN16 Mode											
1	1	DS1-HB	–	DS1-LB	DS2-HB	DS2-LB	DS1-HB	–	DS1-LB	DS2-HB	DS2-LB

1) see **“Control of the Active PCM Channels” on Page 142**

2) Time slot R1 + 1

3) Time slot X1 + 1

4) Empty cells in the table mark unused data in the PCM receive channels and switched-off line drivers in the PCM transmit channels

The configuration bits PCM16K and LIN (in the BCR3 register) are used to select the following PCM interface modes:

- **PCM Mode**

Normal mode used for voice transmission via channels R1 and X1 (receive and transmit). The PCM input channels R2, R3 and R4 are always available for use in different conference configurations. The status of the PCM output channels depends on the conference mode configuration.

- **LIN Mode**

Similar to the PCM mode, but for 16 bit linear data at 8 kHz sample rate via the PCM channels R1, R1L (receive) and X1, X1L (transmit).

- **PCM16 Mode**

Mode for higher data transmission rate of PCM encoded data using a 16 kHz sample rate (only in PCM/µC Interface mode with the PCMX-EN bit in the BCR3 register set to one). In this mode the channels R1, R3 (X1, X3) are used to receive (transmit) two samples of data (DS1, DS2) in each 8 kHz frame.

- **LIN16 Mode**

Like the PCM16 mode for 16 kHz sample rate but for linear data. Channels R1 to R4 (X1 to X4) are used for receiving (transmitting) the high and low bytes of the two linear data samples DS1 and DS2.

4 Operational Description

4.1 Operating Modes for the DuSLIC Chip Set

Table 12 Overview of DuSLIC Operating Modes

***SLICOFI-2x* Mode**	**SLIC Type**			**CIDD/ CIOP[1]**			**Additional Bits used (Note [2])**
	SLIC-S/ SLIC-S2	**SLIC-E/ SLIC-E2**	**SLIC-P**	**M2**	**M1**	**M0**	
Sleep (SL)	–	PDRH	PDRH	1	1	1	SLEEP-EN = 1
			PDRR	1	1	1	SLEEP-EN = 1, ACTR = 1
Power Down Resistive (PDR)	PDRH	PDRH	PDRH	1	1	1	SLEEP-EN = 0
			PDRR	1	1	1	SLEEP-EN = 0, ACTR = 1
Power Down High Impedance (PDH)	PDH	PDH	PDH	0	0	0	–
Active High (ACTH)	ACTH	ACTH	ACTH	0	1	0	–
Active Low (ACTL)	ACTL	ACTL	ACTL	0	1	0	ACTL = 1
Active Ring (ACTR)	ACTR	ACTR	ACTR	0	1	0	ACTR = 1
Ringing (Ring)	ACTR[3]	ACTR	ACTR	1	0	1	–
	–	–	ROT	1	0	1	HIT = 1
	–	–	ROR	1	0	1	HIR = 1
Active with HIT	HIT	HIT		0	1	0	HIT = 1
			HIT	0	1	0	HIT = 1, ACTR = 0
Active with HIR	HIR	HIR		0	1	0	HIR = 0
			HIR	0	1	0	HIR = 0, ACTR = 0
Active with Ring to Ground			ROT	0	1	0	HIT = 1, ACTR = 1
Active with Tip to Ground			ROR	0	1	0	HIR = 1, ACTR = 1
HIRT	–	HIRT	HIRT	0	1	0	HIR = 1, HIT = 1
Active with Metering	ACTx[3] [4]	ACTx[4]	ACTx[4]	1	1	0	TTX-DIS to select Reverse Polarity or TTX Metering

Table 12 Overview of DuSLIC Operating Modes (cont'd)

SLICOFI-2x Mode	**SLIC Type**			**CIDD/ CIOP**[1]			**Additional Bits used (Note** [2]**)**
	SLIC-S/ SLIC-S2	**SLIC-E/ SLIC-E2**	**SLIC-P**	**M2**	**M1**	**M0**	
Ground Start	HIT	HIT		1	0	0	–
			HIT	1	0	0	ACTR = 0
Ring Pause	ACTR[3]	ACTR	ACTR	0	0	1	
			ROR				HIR = 1
			ROT				HIT = 1

[1] CIDD = Data Downstream Command/Indication Channel Byte (IOM-2 interface)
CIOP = Command/Indication Operation
For further information see **"SLICOFI-2x Command Structure and Programming" on Page 163**.

[2] if not otherwise stated in the table, the bits ACTL, ACTR, HIT, HIR have to be set to 0.

[3] only for SLIC-S

[4] ACTx means ACTH, ACTL or ACTR.

Sleep (SL) (only available with DuSLIC-E/-E2/-P)

The SLICOFI-2 is able to go into a sleep mode with minimal power dissipation. In this mode off-hook detection is performed without any checks on spikes or glitches. The sleep mode can be used for either channel, but for the most effective power saving, both channels should be set to this mode. Note that this requires the following:

- Due to the lack of persistence checking only non-noisy lines should use this feature.
- If both channels are set to the sleep mode, waking up takes about 1.25 ms, since the on-chip PLL is also switched off. Therefore it is also possible to switch off all external clocks. In this time no programming or other functionality is available. The off-hook event is indicated either by setting the interrupt pin to active mode if the PCM/µC interface mode is selected or by pulling down the DU pin if IOM-2 interface is used.
- If only one channel is set to sleep mode, persistence checking and off-hook indication is performed as in any other mode, but the off-hook level is fixed to 2 mA at the subscriber line. No special wake-up is needed if only one channel is in sleep mode. A simple mode change ends the sleep mode.
- A sleeping SLICOFI-2 is woken up if the $\overline{\text{CS}}$ pin is drawn to low level when the PCM/µC interface is used or the MX bit is set to zero when the IOM-2 interface is used. Note that no programming is possible until the SLICOFI-2 wakes up. In IOM-2 mode the identification request can be used as a wake-up signal since this command is independent of the internal clock. In the PCM/µC mode it is recommended to set the $\overline{\text{CS}}$ to 0 for only one clock cycle.
- After a wake up from Sleep mode the SLICOFI-2 enters the PDRH or PDRR mode. To re-enter the Sleep mode it is necessary to perform a mode change to any Active mode at least at one channel first.

Power Down Resistive (PDRH for SLIC-E/-E2/-S/-S2 and PDRR for SLIC-P)

The Power Down Resistive mode is the standard mode for none-active lines. Off-hook is detected by a current value fed to the DSP, compared with a programmable threshold, and filtered by a data upstream persistence checker. The power management SLIC-P can be switched to a Power Down Resistive High or a Power Down Resistive Ring mode.

HIRT

The line drivers in the SLIC-E/-E2/-P are shut down and no resistors are switched to the line. Off-hook detection is not possible. In HIRT mode the SLICOFI-2 is able to measure the input offset of the current sensors.

Power Down High Impedance (PDH)

In Power Down High Impedance mode, the SLIC is totally powered down. No off-hook sensing can be performed. This mode can be used for emergency shutdown of a line.

Active High (ACTH)

A regular call can be performed, voice and metering pulses can be transferred via the telephone line and the DC loop is operational in the Active High mode.

Active Low (ACTL)

The Active Low mode is similar to the Active High mode. The only difference is that the SLIC uses a lower battery voltage, V_{BATL} (bit ACTL = 1).

Active Ring (ACTR)

The Active Ring mode is different for the SLIC-E/-E2 and the SLIC-P. The SLIC-E/-E2 uses the additional positive voltage V_{HR} for extended feeding and the SLIC-P will switch to the negative battery voltage V_{BATR}.

Ringing

If the *SLICOFI-2x* is switched to Ringing mode, the SLIC is switched to ACTR mode.

With the SLIC-P connected to the SLICOFI-2, the Ring on Ring (ROR) mode allows unbalanced internal ringing on the Ring wire. The Tip wire is set to battery ground. The Ring signal will be superimposed by $V_{\mathrm{BATR}}/2$.

The Ring on Tip (ROT) mode is the equivalent to the ROR mode.

Active with HIT

This is a testing mode where the Tip wire is set to a high impedance mode. It is used for special line testing. It is only available in an active mode of the *SLICOFI-2x* to enable all necessary test features.

Active with HIR

HIR is similar to HIT but with the Ring wire set to high impedance.

Active with Metering

Any available active mode can be used for metering either with Reverse Polarity or with TTX Signals.

Ground Start

The Tip wire is set to high impedance in Ground Start mode. Any current drawn on the Ring wire leads to a signal on IT, indicating off-hook.

Ring Pause

The Ring burst is switched off in Ring Pause, but the SLIC remains in the specified mode and the off-hook recognition behaves like in ringing mode (Ring Trip).

4.2 Operating Modes for the DuSLIC-S/-S2 Chip Set

Table 13 DuSLIC-S/-S2 Operating Modes

SLICOFI-2S / SLICOFI-2S2 Mode	SLIC-S / SLIC-S2 Mode	SLIC-S/-S2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	Open/V_{BATH}	None	None	High Impedance
Power Down Resistive	PDRH	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL 1)	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BGND}/V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATL} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATL} - V_{AC} - V_{DC})/2$
Active High (ACTH)	ACTH	V_{BGND}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATH} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATH} - V_{AC} - V_{DC})/2$
Active Ring (ACTR)	ACTR	V_{HR}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX-generator (optional)	Tip: $(+ V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2$ Ring: $(+ V_{BATH} + V_{HR} - V_{AC} - V_{DC})/2$
Ringing (Ring)	ACTR	V_{HR}/V_{BATH}	Balanced ring signal feed (incl. DC offset)	Buffer, Sensor, DC loop, Ring generator	Tip: $(V_{BATH} + V_{HR} + V_{DC})/2$ Ring: $(V_{BATH} + V_{HR} - V_{DC})/2$

Table 13 DuSLIC-S/-S2 Operating Modes (cont'd)

SLICOFI-2S / SLICOFI-2S2 Mode	**SLIC-S / SLIC-S2 Mode**	**SLIC-S/-S2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]**	**System Functionality**	**Active Circuits**	**Tip/Ring Output Voltage**
Ring Pause	ACTR	V_{HR}/V_{BATH}	DC offset feed	Buffer, Sensor, DC loop, Ramp generator	Tip: $(V_{BATH} + V_{HR} + V_{DC})/2$ Ring: $(V_{BATH} + V_{HR} - V_{DC})/2$
Active with HIR	HIR	V_{HR}/V_{BATH}	E.g. line test (Tip)	Tip Buffer, Sensor, DC + AC loop	Tip: $(V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2$ Ring: High impedance
Active with HIT	HIT	V_{HR}/V_{BATH}	E.g. line test (Ring)	Ring Buffer, Sensor, DC + AC loop	Ring: $(V_{BATH} + V_{HR} - V_{AC} - V_{DC})/2$ Tip: High impedance

[1] load ext. C for switching from PDRH to ACTH in on-hook mode

V_{AC} … Tip/Ring AC Voltage

V_{DC} … Tip/Ring DC Voltage

4.3 Operating Modes for the DuSLIC-E/-E2 Chip Set

Table 14 DuSLIC-E/-E2 Operating Modes

SLICOFI-2 Mode	SLIC-E / SLIC-E2 Mode	SLIC-E/-E2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	Open/V_{BATH}	None	None	High Impedance
Sleep	PDRH	Open/V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATH} (via 5 kΩ)
Power Down Resistive	PDRH	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL[1]	Open/V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BGND}/V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATL} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATL} - V_{AC} - V_{DC})/2$
Active High (ACTH)	ACTH	V_{BGND}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATH} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATH} - V_{AC} - V_{DC})/2$
Active Ring (ACTR)	ACTR	V_{HR}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(+ V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2$ Ring: $(+ V_{BATH} + V_{HR} - V_{AC} - V_{DC})/2$

Table 14 **DuSLIC-E/-E2 Operating Modes** (cont'd)

SLICOFI-2 Mode	**SLIC-E / SLIC-E2 Mode**	**SLIC-E/-E2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]**	**System Functionality**	**Active Circuits**	**Tip/Ring Output Voltage**
Ringing (Ring)	ACTR	V_{HR}/V_{BATH}	Balanced Ring signal feed (incl. DC offset)	Buffer, Sensor, DC loop, Ring generator	Tip: $(V_{BATH} + V_{HR} + V_{DC})/2$ Ring: $(V_{BATH} + V_{HR} - V_{DC})/2$
Ring Pause	ACTR	V_{HR}/V_{BATH}	DC offset feed	Buffer, Sensor, DC loop, ramp generator	Tip: $(V_{BATH} + V_{HR} + V_{DC})/2$ Ring: $(V_{BATH} + V_{HR} - V_{DC})/2$
HIRT	HIRT	V_{HR}/V_{BATH}	E.g. sensor offset calibration	Sensor, DC transmit path	High Impedance
Active with HIR	HIR	V_{HR}/V_{BATH}	E.g. line test (Tip)	Tip-Buffer, Sensor, DC + AC loop	Tip: $(V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2$ Ring: High impedance
Active with HIT	HIT	V_{HR}/V_{BATH}	E.g. line test (Ring)	Ring-Buffer, Sensor, DC + AC loop	Ring: $(V_{BATH} + V_{HR} - V_{AC} - V_{DC})/2$ Tip: High impedance

[1] load ext. C for switching from PDRH to ACTH in on-hook mode

V_{AC} … Tip/Ring AC Voltage

V_{DC} … Tip/Ring DC Voltage

4.4 Operating Modes for the DuSLIC-P Chip Set

Table 15 DuSLIC P Operating Modes

SLICOFI-2 Mode	SLIC-P Mode	SLIC-P Internal Supply Voltages [V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	V_{BATR}	None	None	High impedance
Sleep	PDRH	V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATH} (via 5 kΩ)
Sleep	PDRR	V_{BATR}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATR} (via 5 kΩ)
Power Down Resistive	PDRH	V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL[1)]	V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRR	V_{BATR}	Off-hook detect as in active mode (DSP)	Off-hook, Analog comparator	V_{BGND}/V_{BATR} (via 5 kΩ)
–	PDRRL[2)]	V_{BATR}	Off-hook detect as in active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATR} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATL} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATL} - V_{AC} - V_{DC})/2$
Active High (ACTH)	ACTH	V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATH} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATH} - V_{AC} - V_{DC})/2$

Table 15 DuSLIC P Operating Modes (cont'd)

SLICOFI-2 Mode	SLIC-P Mode	SLIC-P Internal Supply Voltages [V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
Active Ring (ACTR)	ACTR	V_{BATR}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATR} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATR} - V_{AC} - V_{DC})/2$
Ringing (Ring)	ACTR	V_{BATR}	Balanced ring signal feed (incl. DC offset)	Buffer, Sensor, DC loop, ring generator	Tip: $(V_{BATR} + V_{DC})/2$ Ring: $(V_{BATR} - V_{DC})/2$
Ringing (Ring)	ROR	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC loop, ring generator	Ring: $(V_{BATR} - V_{DC})/2$ Tip: 0 V
Ringing (Ring)	ROT	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC loop, ring generator	Tip: $(V_{BATR} + V_{DC})/2$ Ring: 0 V
Ring Pause	ACTR, ROR, ROT	V_{BATR}	DC offset feed	Buffer, Sensor, DC loop, ramp generator	Tip: $(V_{BATR} + V_{DC})/2$ Ring: $(V_{BATR} - V_{DC})/2$
HIRT	HIRT	V_{BATR}	E.g. sensor offset calibration	Sensor, DC transmit path	High impedance
Active with HIR	HIR	V_{BATR}	E.g. line test (Tip)	Tip-Buffer, Sensor, DC + AC loop	Tip: $(V_{BATR} + V_{AC} + V_{DC})/2$ Ring: High impedance
Active with HIT	HIT	V_{BATR}	E.g. line test (Ring)	Ring-Buffer, Sensor, DC + AC loop	Ring: $(V_{BATR} - V_{AC} - V_{DC})/2$ Tip: High impedance

[1] load ext. C for switching from PDRH to ACTH in on-hook mode

[2] load ext. C for switching from PDRR to ACTR in on-hook mode

4.5 Reset Mode and Reset Behavior

4.5.1 Hardware and Power On Reset

A reset of the DuSLIC is initiated by a power-on reset or a hardware reset by setting the signal at RESET input pin to low level for at least 4 µs1). The reset input pin has a spike rejection which will safely suppress spikes with an duration of less than 1 µs2).

By setting the reset signal to low, the chip will be reset (see **Figure 39**):

- all I/O pins deactivated
- all outputs inactive (e.g. DXA/DXB)
- internal PLL stopped
- internal clocks deactivated
- chip in power down high impedance (PDH)

With the high going reset signal, the following actions take place:

- Clock detection
- PLL synchronization
- Running the reset routine

The internal reset routine will then initialize the whole chip to default condition as described in the SOP default register setting (see **Chapter 6**). To run through the internal reset routine it is necessary that all external clocks are supplied:

- µC/PCM mode: FSC, MCLK, PCLK
- IOM-2 mode: FSC and DCL.

Without valid and stable external clock signals, the DuSLIC will not finish the reset sequence properly.

The internal reset routine requires 12 frames (125 µs) to be finished (including PLL start up and clock synchronization) and is setting the default values given in **Table 16**. The first register access to the *SLICOFI-2x* may be done after the internal reset routine is finished.

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1) Maximum spike rejection time $t_{\text{rej, max}}$

2) Minimum spike rejection time $t_{\text{rej,min}}$

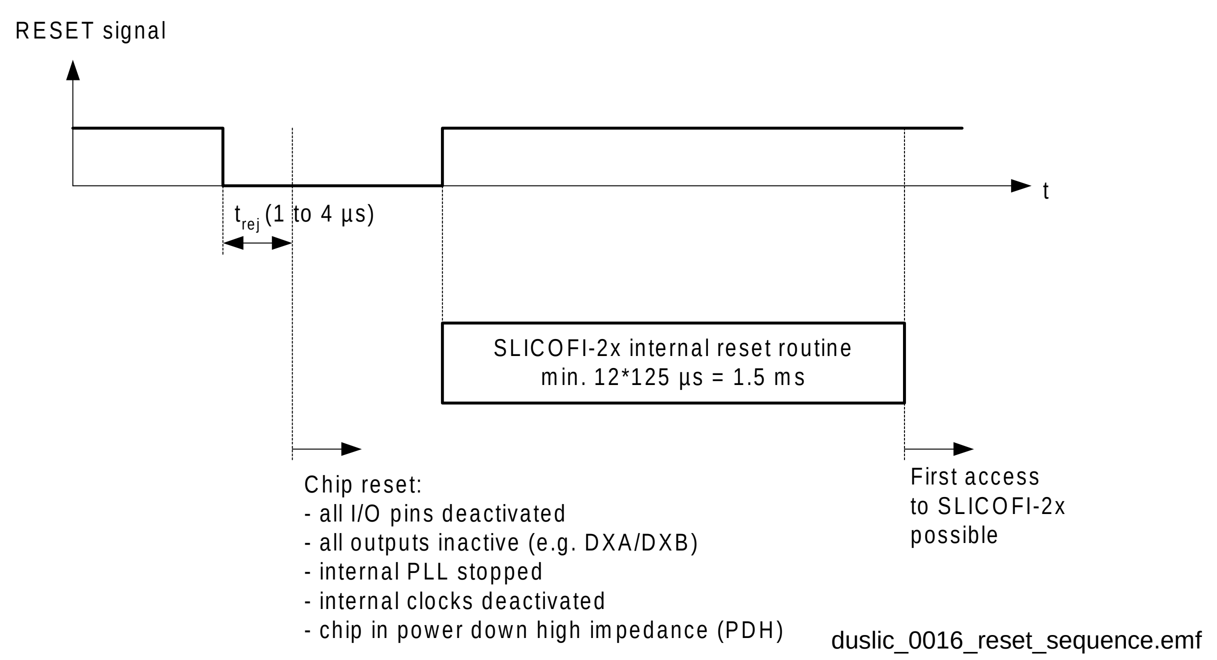

RESET signal
t
t_{rej} (1 to 4 µs)
SLICOFI-2x internal reset routine
min. 12*125 µs = 1.5 ms
Chip reset:
- all I/O pins deactivated
- all outputs inactive (e.g. DXA/DXB)
- internal PLL stopped
- internal clocks deactivated
- chip in power down high impedance (PDH)
First access
to SLICOFI-2x
possible
duslic_0016_reset_sequence.emf

Figure 39 DuSLIC Reset Sequence

4.5.2 Software Reset

When performing a software reset, the DuSLIC is running the reset routine and sets the default settings of the configuration registers. The software reset can be performed individually for each channel.

Table 16 Default Values

DC			
I_{K1}	20	mA	Limit for Constant Current
V_{K1}	34	V	Voltage of limit between Constant Current and Resistive Zone
K$_{B}$	1	–	Additional gain with extended battery feeding
R_{I}	10	kΩ	Output Resistance in constant current zone
R_{K12}	100	Ω	Programmable resistance in resistive zone
f_{RING}	25.4	Hz	Ring frequency
A_{RING}	62	Vrms	Ring amplitude at Ring/Tip wire
RO1	23	V	Ring offset voltage RO1
RO2	0	V	Ring offset voltage RO2
RO3	50	V	Ring offset voltage RO3
f_{RINGLP}	75	Hz	Corner frequency of Ring low-pass filter
Off-hookPD	2	mA	Current threshold for Off-hook Detection in Power Down mode
Off-hookAct	8	mA	Off-hook Detection in Active with 2 mA hysteresis
Off-hookRing	5	mA	DC-Current threshold for Off-hook Detection in Ringing mode
Off-hookMW	5	mA	DC-Current threshold for Off-hook Detection in Message Waiting
Off-hookAC	22	mArms	Current threshold for AC Ring-Trip detection
LineSup	5	mA	Current threshold Line-Supervision for ground start
Ring/Tip	30	V	Voltage threshold at Ring/Tip wire for VRTLIM bit
DC-Lowpass	1.2/20	Hz	DC low-pass set to 1.2 and 20 Hz respectively
ConstRamp	300	V/s	Slope of the ramp generator
delay$_{RING}$	0	ms	Delay of Ring burst
SRend1	1/128	–	Soft-reversal threshold 1 (referred to the input of the ramp generator)

Table 16 Default Values (cont'd)

SRend2	1/512	–	Soft-reversal threshold 2 (referred to the input of the ramp generator)
DUP	10	ms	Data Upstream Persistence Counter is set to 10 ms
DUP-IO	16.5	ms	Data Upstream Persistence Counter for I/O pins, VRTLIM and ICON bits (register INTREG1) is set to 16.5 ms
SR-Time	80	ms	Time for soft-reversal
		AC	
IM-Filter	900	Ω	Approximately 900 Ω real input impedance
TH-Filter	TH_{BRD}	–	Approximately BRD impedance for balanced network
LX	0	dB	Relative level in transmit
LR	7	dB	Relative level in receive
ATTX	2.5	Vrms	Teletax generator amplitude at the resistance of 200 Ω
f_{TTX}	16	kHz	Teletax generator frequency
TG1	940	Hz	Tone generator 1 (– 12 dBm)
TG2	1633	Hz	Tone generator 2 (– 10 dBm)
AC-LM-BP	1004	Hz	AC level meter band pass

4.6 Interrupt Handling

SLICOFI-2x provides much interrupt data for the host system. Interrupt handling is performed by the on chip microprogram which handles the interrupts in a fixed 2 kHz (500 µs) frame. Therefore, some delays up to 500 µs can occur in the reactions of *SLICOFI-2x* depending on when the host reads the interrupt registers.

Independent of the selected interface mode (PCM/µC or IOM-2), the general behavior of the interrupt is as follows:

- Any change (at some bits only transitions from 0 to 1) in one of the four interrupt registers leads to an interrupt. The interrupt channel bit INT-CH in INTREG1 is set to one and all interrupt registers of one DuSLIC channel are locked at the end of the interrupt procedure (500 µs period). Therefore all changes within one 2 kHz frame are stored in the interrupt registers. The lock remains until the interrupt channel bit is cleared (Release Interrupt by reading all four interrupt registers INTREG1 to INTREG4 with one command).
- In IOM-2 interface mode, the interrupt channel bits are fed to the CIDU channel (see IOM-CIDU). In PCM mode, the INT pin is set to active (low).
- The interrupt is released (INT-CH bit reset to zero) by reading all four interrupt registers by one command. Reading the interrupt registers one by one using a series of commands does not release the interrupt even if all four registers are read.
- A hardware or power-on reset of the chip clears all pending interrupts and resets the INT line to inactive (PCM/µC mode) or resets the INT-CH bit in CIDU (IOM-2 mode). The behavior after a software reset of both channels is similar, the interrupt signal switches to non-active within 500 µs. A software reset of one DuSLIC channel deactivates the interrupt signal if there is no active interrupt on the other DuSLIC channel.
  If the reset line is deactivated, a reset interrupt is generated for each channel (bit RSTAT in register INTREG2).

4.7 Operating Modes and Power Management

In many applications, the power dissipated on the line card is a critical parameter. In larger systems, the mean power value (taking into account traffic statistics and line length distribution) determines cooling requirements. Particularly in remotely fed systems, the maximum power for a line must not exceed a given limit.

4.7.1 Introduction

Generally, system power dissipation is determined mainly by the high-voltage part. The most effective power-saving method is to limit SLIC functionality and reduce supply voltage in line with requirements. This is achieved using different operating modes.
The three main modes – Power Down, Active and Ringing – correspond to the main system states: on-hook, signal transmission (voice and/or TTX) and ring signal feed.

For power critical applications the Sleep mode can be used for even lower power consumption than in Power Down mode.

- **Power Down**

Off-hook detection is the only function available. It is realized by 5 kΩ resistors applied by the SLIC from Tip to V_{BGND} and Ring to V_{BAT}, respectively. A simple sensing circuit supervises the DC current through these resistors (zero in on-hook and non-zero in off-hook state). This scaled transversal line current is transferred to the IT pin and compared with a programmable current threshold in the *SLICOFI-2x*. Only the DC loop in the *SLICOFI-2x* is active.

In **Sleep** mode, all functions of the *SLICOFI-2x* are switched off except for off-hook detection which is still available via an analog comparator. Both AC and DC loops are inactive. To achieve the lowest power consumption of the DuSLIC chip set, the clock cycles fed to the MCLK and PCLK pins have to be shut off.

For changing into another state the DuSLIC has to be woken up according to the procedure described in **Chapter 4.1**.

- **Active**

Both AC and DC loops are operative. The SLIC provides low-impedance voltage feed to the line. The SLIC senses, scales and separates transversal (metallic) and longitudinal line currents. The voltages at Tip and Ring are always symmetrical with reference to half the battery voltage (no ground reference!). An integrated switch makes it possible to choose between two (SLIC-S/-S2, SLIC-E/-E2) or even three (SLIC-P) different battery voltages. With these voltages selected according to certain loop lengths, power optimized solutions can be achieved.

– Ringing

For SLIC-E/-E2 and SLIC-S, an auxiliary positive supply voltage V_{HR} is used to give a total supply range of up to 150 V. For SLIC-P the whole supply range is provided by V_{BATR}. The low-impedance line feed (R_{STAB} (2x30 Ω) + R_{FUSE} (2x20 Ω) + appr. 1 Ω ≈ 101 Ω output impedance) with a balanced sinusoidal Ring signal of up to 85 Vrms, plus a DC offset of 20 V, is sufficient to supply very long lines at any kind of ringer load and to reliable detect Ring trip. Unbalanced ringing is supported by applying the Ring signal to only one line, while Ground is applied to the other line.

For an overview of all DuSLIC operating modes see **Table 13** for PEB 4264/-2, **Table 14** for PEB 4265/-2 and **Table 15** for PEB 4266.

4.7.2 Power Dissipation of the *SLICOFI-2x*

For an optimized power consumption unused EDSP functions have to be switched off.

Typical power dissipation values for different operating modes of the *SLICOFI-2x* are shown in **Chapter 7.4.3** and **Chapter 7.4.4**.

4.7.3 Power Dissipation of the SLIC

The SLIC power dissipation mainly comes from internal bias currents and the buffers output stage (to a lesser extent from the sensor) where additional power is dissipated whenever current is fed to the line.

4.7.3.1 Power Down Modes

In Power Down modes, the internal bias currents are reduced to a minimum and no current is fed to the line (see **Table 19**, **Table 21** and **Table 23**). Even with active off-hook detection, the power dissipation of 5 mW (6 mW for SLIC-P) is negligible. Note that this is the dominant factor for a low mean power value in large systems, as a large percentage of lines are always inactive.

4.7.3.2 Active Mode

In Active mode, the selected battery voltage V_{BATx}[1] has the strongest influence on power dissipation. The power dissipation in the output stage P_{O} (see **Chapter 7.1.5** and **Chapter 7.2.5**) is determined by the difference between V_{BATx} and the Tip-Ring voltage $V_{\mathrm{TIP/RING}}$. At constant DC line current I_{Trans}, the shortest lines (lowest R_{L}) cause lowest $V_{\mathrm{TIP/RING}}$, and accordingly exhibit the highest on-chip power dissipation. However, the minimum battery voltage required is determined by the longest line and therefore the maximum line resistance $R_{\mathrm{L,MAX}}$ and in addition R_{PROT} and R_{STAB}.

$$V_{\mathrm{BATx,min}} = I_{\mathrm{Trans}} \times (R_{\mathrm{L,MAX}} + R_{\mathrm{PROT}} + R_{\mathrm{STAB}}) + V_{\mathrm{AC,P}} + V_{\mathrm{DROP}}$$

$V_{\mathrm{AC,P}}$ .... Peak value of AC signal

V_{DROP} .... Sum of voltage drop in the SLIC buffers (**Table 17**)

Table 17 Typical Buffer Voltage Drops (Sum) for I_{TRANS} (I_{T} or I_{R})

Mode	**Total Voltage drop V_{DROP} [V]**	
	SLIC-E/-E2/-S/-S2	**SLIC-P**
ACTL	$I_{\mathrm{TRANS}} \times 96\ \Omega$	$I_{\mathrm{TRANS}} \times 88\ \Omega$
ACTH	$I_{\mathrm{TRANS}} \times 100\ \Omega$	$I_{\mathrm{TRANS}} \times 100\ \Omega$
ACTR	$(I_{\mathrm{TRANS}} \times 100\ \Omega) + 1\ \mathrm{V}$	$I_{\mathrm{TRANS}} \times 92\ \Omega$
ROR, ROT	–	$I_{\mathrm{TRANS}} \times 92\ \Omega$
HIR, HIT	$(I_{\mathrm{T\ or\ R}} \times 48\ \Omega) + 1\ \mathrm{V}$	$I_{\mathrm{T\ or\ R}} \times 52\ \Omega$

---

[1] $V_{\mathrm{BATx}} = V_{\mathrm{BATL}}$, V_{BATH} or V_{BATR}

The most efficient way to reduce short-loop power dissipation is to use a lower battery supply voltage (V_{BATL}) whenever line resistance is small enough. This method is supported on the SLIC-E/-E2 by integrating a battery switch. With a standard battery voltage of – 48 V, long lines up to 2 kΩ can be driven at 20 mA line current.

The SLIC-P PEB 4266 “low-power” version even allows three battery voltages (typically the most negative one, e.g. – 48 V, is used in Active mode (On-hook) and Power Down mode).

DuSLIC contains two mechanism which can be used as indication for the battery switching:

1. A threshold for the voltage at Tip/Ring can be set for generating an interrupt
2. The change between constant current and resistive feeding will generate an interrupt

4.7.3.3 SLIC Power Consumption Calculation in Active Mode

A scheme for a typical calculation is shown in **Figure 40**.

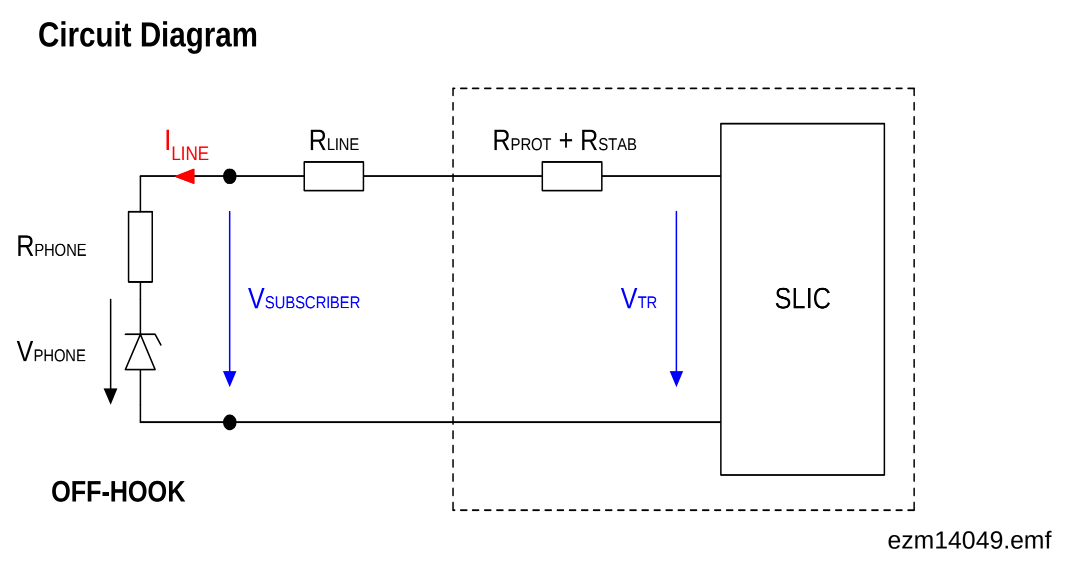


Figure 40 Circuit Diagram for Power Consumption

R_{PROT} = 40 Ω, R_{STAB} = 60 Ω, R_{PHONE} = 150 Ω, V_{PHONE} = 7 V, I_{LINE} = 20 mA

Conditions: $V_{Voice\ peak}$ = 2 V, $I_{Voice\ peak}$ = 2 mA, $V_{TTX,rms}$ (see example below)

Typical Power Consumption Calculation with SLIC-E/-E2

Assuming a typical application where the following battery voltages are used:

V_{DD} = 5 V, V_{BATL} = – 43 V, V_{BATH} = – 62 V, V_{HR} = 80 V and line feeding is guaranteed up to R_L = 1900 Ω. For longer lines (R_L > 1900 Ω) the extended battery feeding option can be used (Mode ACTR).
Requirement for TTX: V_{TTX} = 2.5 Vrms at a load of 200 Ω.

Table 18 shows line currents and output voltages for different operating modes.

Table 18 Line Feed Conditions for Power Calculation of SLIC-E/-E2

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	$I_{\mathrm{TRANS}} = 0$ mA	–
ACTL	$I_{\mathrm{TRANS}} = 20$ mA	$V_{\mathrm{TIP/RING}} = 32$ V
ACTH	$I_{\mathrm{TRANS}} = 20$ mA	$V_{\mathrm{TIP/RING}} = 50$ V
ACTR extended battery feeding at higher loop length ($R_{\mathrm{L}} > 1900\ \Omega$)	$I_{\mathrm{TRANS}} = 20$ mA	$V_{\mathrm{TIP/RING}} = 130$ V

With the line feed conditions given in the above table the total power consumption P_{TOT} and its shares at different operating modes are shown in **Table 19**. The output voltage at Tip and Ring is calculated for the longest line ($R_{\mathrm{L}} = 1900\ \Omega$ in ACTH, $R_{\mathrm{L}} = 996\ \Omega$ in ACTL).

Table 19 SLIC-E/-E2 Typical Total Power Dissipation

	P_{Q}[1]	P_{I}	P_{G}	P_{O}	P_{TOT}
Operating Mode	[mW]	[mW]	[mW]	[mW]	**[mW]**
PDH	4.6	0	0	0	**4.6**
PDRH	5.6	0	0	0	**5.6**
ACTL	127	51.3	27.1	220	**425.4**
ACTH	222	72.2	32.8	240	**567**
ACTR	379	96.2	412	240	**1127.3**

[1] The formulas for the calculation of the power shares P_{Q}, P_{I}, P_{G} and P_{O} can be found in **Chapter 7.2.5**.

Figure 41 shows the total power dissipation P_{TOT} of the SLIC-E/-E2 in Active Mode (ACTH and ACTL) with switched battery voltage (V_{BATH}, V_{BATL}) as a function of R_{Line}. The power dissipation in the SLIC is strongly reduced for short lines.

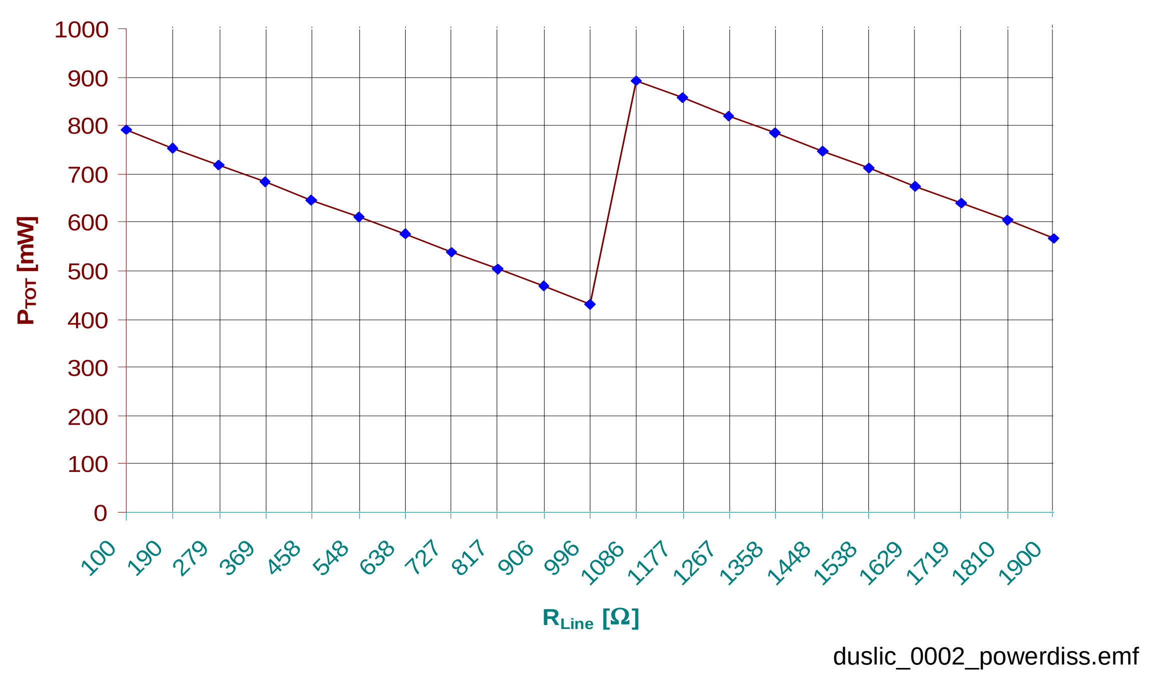


Figure 41 SLIC-E/-E2 Power Dissipation with Switched Battery Voltage

Typical Power Consumption Calculation with SLIC-P (Internal Ringing)

Assuming a typical application where the following battery voltages are used:

V_{DD} = 5 V, V_{BATL} = – 36 V, V_{BATH} = – 48 V, V_{BATR} = – 108 V and line feeding is guaranteed up to R_L = 1200 Ω.

Requirement for TTX: V_{TTX} = 2.5 Vrms at a load of 200 Ω.

Table 20 shows line currents and output voltages for different operating modes.

Table 20 Line Feed Conditions for Power Calculation for SLIC-P

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	–
ACTL	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 25.2 V
ACTH	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 36 V
ACTR	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 96 V

With the line feed conditions given in the above table, the total power consumption P_{TOT} and its shares at different operating modes are shown in **Table 21**. The output voltage at Tip and Ring is calculated for the longest line (R_L = 1200 Ω in ACTH, R_L = 662 Ω in ACTL).

Table 21 SLIC-P PEB 4266 Power Dissipation

	P_Q	P_I	P_G	P_O	P_{TOT}
Operating Mode	[mW]	[mW]	[mW]	[mW]	**[mW]**
PDH	8.8	0	0	0	**8.8**
PDRH	7.7	0	0	0	**7.7**
PDRR	10.4	0	0	0	**10.4**
ACTL	81.7	43.6	15.3	216	**357**
ACTH	135	56.8	0	240	**432**
ACTR (Extended Battery Feeding)	383	123	112	240	**857**
ROR, ROT (Ring Pause)	263	0	102	0	**365**

Figure 43 shows the total power dissipation PTOT of the SLIC-P in Active mode (ACTH and ACTL) with switched battery voltage (V_{BATH}, V_{BATL}) as a function of R_{Line}.

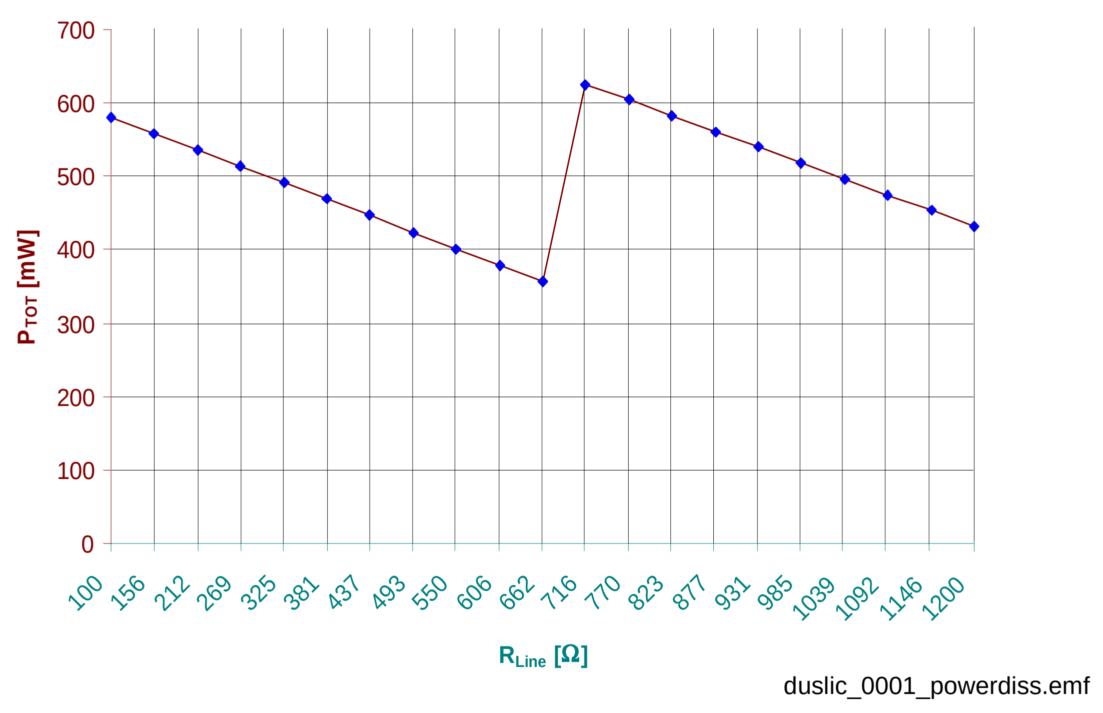


Figure 42 SLIC-P Power Dissipation (Switched Battery Voltage, Long Loops)

Typical Power Consumption Calculation with SLIC-P (External Ringing)

Assuming a typical application where the following battery voltages are used:

V_{DD} = 5 V, V_{BATL} = – 25 V, V_{BATH} = – 31 V, V_{BATR} = – 48 V and line feeding is guaranteed up to R_{L} = 600 Ω.

Requirement for TTX: $V_{\mathrm{TTX,rms}}$ = 0.7 V.

This is a typical lowest-power application, where V_{BATR} is used just in the On-hook state and V_{BATH} and V_{BATL} is used in the active modes with battery switching.

Table 22 shows line currents and output voltages for different operating modes.

Table 22 Line Feed Conditions for Power Calculation for SLIC-P

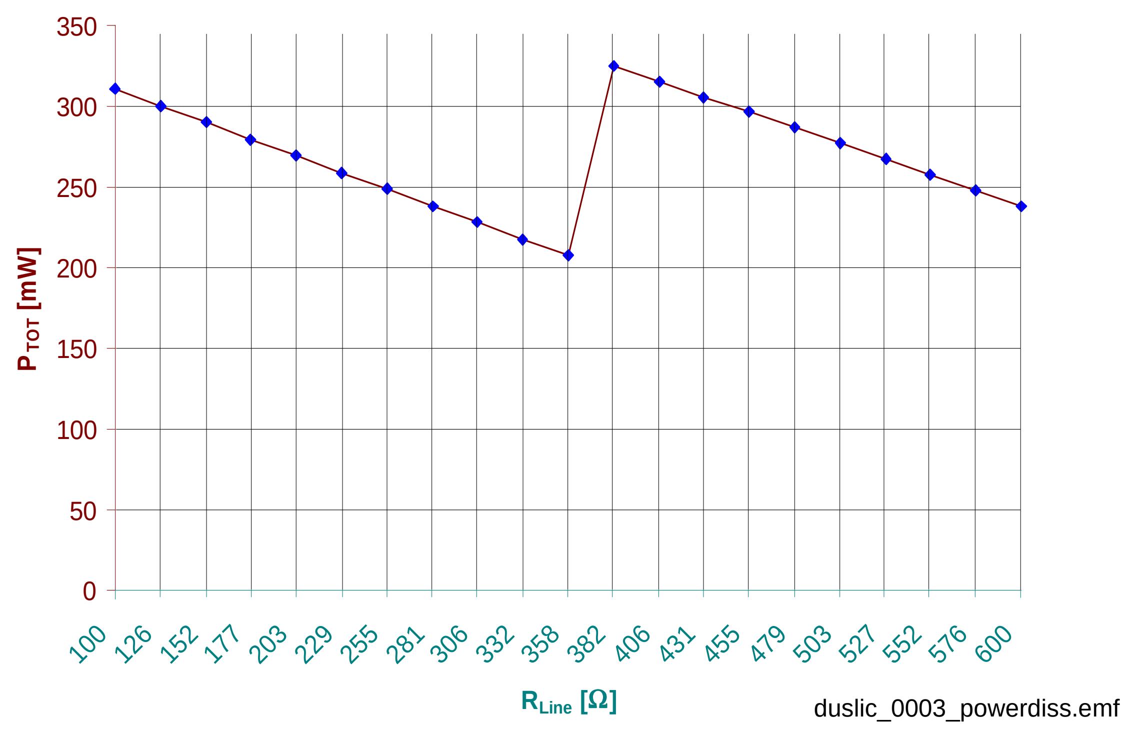
Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	–
ACTL	I_{TRANS} = 20 mA	$V_{\mathrm{TIP/RING}}$ = 19.2 V
ACTH	I_{TRANS} = 20 mA	$V_{\mathrm{TIP/RING}}$ = 24 V
ACTR	I_{TRANS} = 20 mA	$V_{\mathrm{TIP/RING}}$ = 41 V

With the line feed conditions given in the above table, the total power consumption P_{TOT} and its shares at different operating modes are shown in **Table 23**. The output voltage at Tip and Ring is calculated for the longest line (R_{L} = 600 Ω in ACTH, R_{L} = 358 Ω in ACTL).

Table 23 SLIC-P PEB 4266 Power Dissipation

	P_{Q}	P_{I}	P_{G}	P_{O}	P_{TOT}
Operating Mode	[mW]	[mW]	[mW]	[mW]	**[mW]**
PDH	4.3	0	0	0	**4.3**
PDRH	4.5	0	0	0	**4.5**
PDRR	5.0	0	0	0	**5.0**
ACTL	57.8	31.5	1.0	116	**206**
ACTH	88.7	38.1	-28.6	140	**238**
ACTR	172.5	56.8	-87.2	140	**282**

Figure 43 shows the total power dissipation P_{TOT} of the SLIC-P in Active mode (ACTH and ACTL) with switched battery voltage (V_{BATH}, V_{BATL}) as a function of R_{Line} (Lowest Power Applications).



duslic_0003_powerdiss.emf

Figure 43 SLIC-P Power Dissipation (Switched Battery Voltage, Short Loops)

4.7.3.4 Ringing Modes

Internal Balanced Ringing (SLIC-E/-E2 and SLIC-P)

The SLIC-E/-E2/-P internal balanced ringing facility requires a higher supply voltage (auxiliary voltage V_{HR}). The highest share of the total power is dissipated in the output stage of the SLIC-E/-E2/-P. The output stage power dissipation P_O (see **Table 24**, **Table 25**) depends on the ring amplitude ($V_{RNG,PEAK}$), the equivalent ringer load (R_{RNG} and C_{RNG}), the ring frequency (via $\cos\phi_L$) and the line length (R_L).

The minimum auxiliary voltage V_{HR} necessary for a required ring amplitude can be calculated using:

$$V_{HR} - V_{BATH} = V_{RNG,PEAK} + V_{RNG,DC} + V_{DROP} = V_{RNG,RMS} \times \text{crest factor} + V_{RNG,DC} + V_{DROP}$$

The crest factor is defined as peak value divided by RMS value (here always 1.41 because sinusoidal ringing is assumed).

$V_{RNG,DC}$	Superimposed DC voltage for Ring trip detection (10 to 20 V)
V_{DROP}	Sum of voltage drops in SLIC buffers (**Table 17**)
$V_{RNG,PEAK}$	Peak ring voltage at Tip/Ring

The strong influence of the ringer load impedance Z_{LD} and the number of ringers is demonstrated by the formula for the current sensor power dissipation ($P_I + P_O$) in **Table 24** and **Table 25**.

The ringer load impedance Z_{LD} can be calculated as follows:

$Z_{LD} = |Z_{LD}| \times e^{j\phi LD} = R_L + R_{RNG} + 1/j\omega C_{RNG}$ with

Z_{LD}	Load impedance
R_{RNG}	Ringer resistance
C_{RNG}	Ringer capacitance
R_L	Line resistance

Internal Unbalanced Ringing with SLIC-P

The ring signal is present just on one line (modes ROR, ROT), while the other line is connected to a potential of GND.

The minimum battery voltage V_{BATR} necessary for a required ring amplitude can be calculated using:

$- V_{BATR} - V_{DROP} = 2 \times V_{RNG, PEAK} = 2 \times V_{RNG,RMS} \times$ crest factor

External Ringing (SLIC-E/-E2 and SLIC-P)

When an external ring generator and ring relays are used, the SLIC can be switched to Power Down mode.

The “low-power” SLIC-P is optimized for extremely power-sensitive applications (see **Table 23**). SLIC-P has three different battery voltages. V_{BATR} can be used for on-hook, while V_{BATH} and V_{BATL} are normally used for off-hook mode.

4.7.3.5 SLIC Power Consumption Calculation in Ringing Mode

The average power consumption for a ringing cadence of 1 second on and 4 seconds off is given by

$$P_{\text{TOT, average}} = \mathrm{k} \times P_{\text{TOT, Ringing}} + (1 - \mathrm{k}) \times P_{\text{TOT, RingPause}}$$

with k = 0.20

The typical circuit for ringing is shown in **Figure 44**.

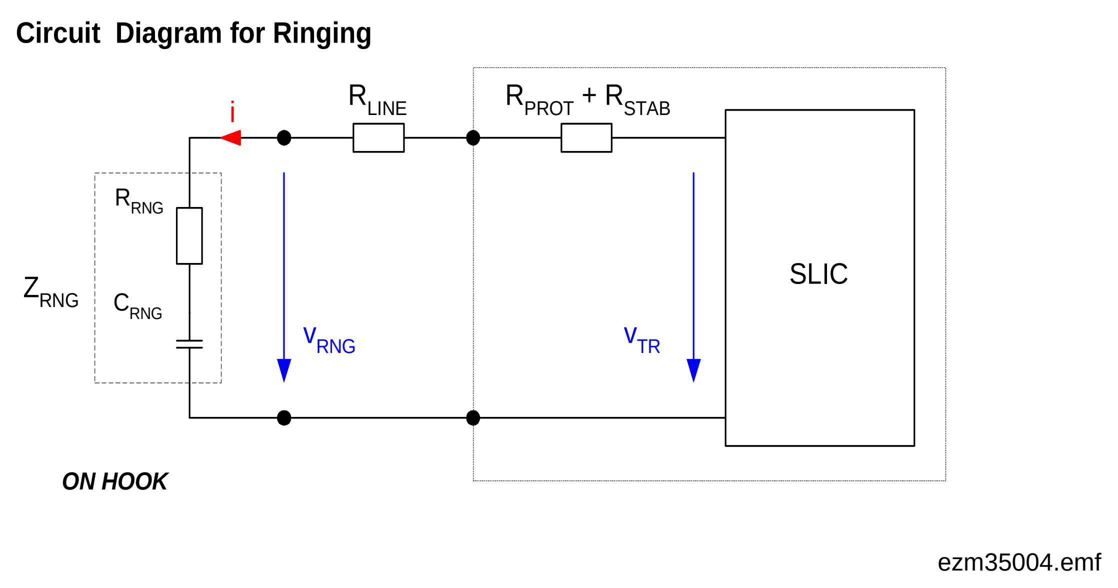

Circuit Diagram for Ringing
i
R_{LINE}
$R_{PROT} + R_{STAB}$
R_{RNG}
Z_{RNG}
C_{RNG}
V_{RNG}
V_{TR}
SLIC
ON HOOK
ezm35004.emf

Figure 44 Circuit Diagram for Ringing

– Power Consumption Calculation for SLIC-E/-E2 in Balanced Ringing Mode

With the example of the above calculation for SLIC-E/-E2 (see **Chapter 4.7.3.3**) and a typical ringer load.

$R_{\mathrm{RNG}} = 450\ \Omega$, $C_{\mathrm{RNG}} = 3.4\ \mu\mathrm{F}$, required ringing voltage $V_{\mathrm{RNG}} = 58$ Vrms and ringing frequency $f_{\mathrm{RNG}} = 20$ Hz. DC Offset Voltage for ring trip detection $V_{\mathrm{DC}} = 20$ V.

Table 24 shows the power calculation for the total power dissipation P_{TOT} of the SLIC-E/-E2 in balanced ringing mode consisting of the quiescent power dissipation P_{Q}, the current sensor power dissipation P_{I}, the gain stage power dissipation P_{G} and the output stage power dissipation P_{O}.

Table 24 SLIC-E/-E2 Balanced Ringing Power Dissipation (typical)

$P_{\mathrm{TOT,\ RingPause}} = P_{\mathrm{Q}} + P_{\mathrm{I}} + P_{\mathrm{G}} + P_{\mathrm{O}}\ (I_{\mathrm{Trans}} = 0\ \mathrm{mA})$	**710 mW**
$P_{\mathrm{TOT,\ Ringing}} = P_{\mathrm{Q}} + P_{\mathrm{I}} + P_{\mathrm{G}} + P_{\mathrm{O}}$	**2481 mW[1]**
$P_{\mathrm{Q}} = V_{\mathrm{DD}} \times I_{\mathrm{DD}} + \lvert V_{\mathrm{BATH}}\rvert \times I_{\mathrm{BATH}} + \lvert V_{\mathrm{BATL}}\rvert \times I_{\mathrm{BATL}} + V_{\mathrm{HR}} \times I_{\mathrm{HR}}$	390 mW
$P_{\mathrm{I}} = 0.015 \times I_{\mathrm{Trans,rms}} \times V_{\mathrm{HR}} + 0.055 \times I_{\mathrm{Trans,rms}} \times \lvert V_{\mathrm{BATH}}\rvert + 0.04 \times I_{\mathrm{Trans,rms}} \times V_{\mathrm{DD}}$ with $I_{\mathrm{Trans,rms}} = V_{\mathrm{TIP/RING,\ rms}}/\lvert Z_{\mathrm{LD}}\rvert$	118 mW
$P_{\mathrm{G}} = (V_{\mathrm{HR}} + \lvert V_{\mathrm{BATH}}\rvert) \times (\mathrm{SQRT}((V_{\mathrm{HR}} + V_{\mathrm{BATH}} + V_{\mathrm{DC\text{-}offset}})^2 + (V_{\mathrm{TIP/RING}}{}^2)/2) - \lvert V_{\mathrm{HR}} + V_{\mathrm{BATH}}\rvert)/60\mathrm{k} + (V_{\mathrm{HR2}} - 322 + V_{\mathrm{BATH}}{}^2 - 48^2) \times (1/60\mathrm{k} + 1/216\mathrm{k})$	320 mW
$P_{\mathrm{O}} = (V_{\mathrm{HR}} + \lvert V_{\mathrm{BATH}}\rvert) \times I_{\mathrm{Trans,rms}} \times 2 \times \mathrm{SQRT}(2)/\pi - V_{\mathrm{TIP/RING,\ rms}} \times I_{\mathrm{Trans,rms}} \times \cos(\phi_{\mathrm{Load}})$	1653 mW

[1] Values for $V_{\mathrm{DD}} = 5$ V, $V_{\mathrm{BATL}} = -43$ V, $V_{\mathrm{BATH}} = -62$ V, $V_{\mathrm{HR}} = 80$ V, $T_{\mathrm{J}} = 25$ °C

– Power Consumption Calculation for SLIC-P in Balanced Ringing Mode

With the example of the above calculation with R_L = 1200 Ω line length for SLIC-P (see **Chapter 4.7.3.3**) when the internal ringing feature will be used.

Typical ringer load: R_{RNG} = 1000 Ω, C_{RNG} = 3.7 µF. Required ringing voltage V_{RNGr} = 45 Vrms and ringing frequency f_{RNG} = 20 Hz. DC Offset voltage for ring trip detection V_{DC} = 20 V.

Table 25 shows the power calculation for the total power dissipation P_{TOT} of the SLIC-P in balanced ringing mode consisting of the quiescent power dissipation P_Q, the current sensor power dissipation P_I, the gain stage power dissipation P_G and the output stage power dissipation P_O.

Table 25 SLIC-P Balanced Ringing Power Dissipation (typical)

$P_{TOT, RingPause} = P_Q + P_I + P_G + P_O$ (I_{Trans} = 0 mA)	**482 mW**
$P_{TOT, Ringing} = P_Q + P_I + P_G + P_O$	**1618 mW[1]**
$P_Q = V_{DD} \times I_{DD} + \lvert V_{BATR} \rvert \times I_{BATR} + \lvert V_{BATH} \rvert \times I_{BATH} + \lvert V_{BATL} \rvert \times I_{BATL}$	370 mW
$P_I = 0.055 \times I_{Trans,rms} \times \lvert V_{BATR} \rvert + 0.04 \times I_{Trans,rms} \times V_{DD}$ with $I_{Trans,rms} = V_{TIP/RING, rms} / \lvert Z_{LD} \rvert$	117 mW
$P_G = (V_{BATR}^2 - 80^2) \times (1/60k + 1/216k)$	112 mW
$P_O = \lvert V_{BATR} \rvert \times I_{Trans,rms} \times 2 \times SQRT(2)/\pi - V_{TIP/RING, rms} \times I_{Trans,rms} \times \cos(\phi_{Load})$	1019 mW

[1] Values for V_{DD} = 5 V, V_{BATL} = – 36 V, V_{BATH} = – 48 V, V_{BATR} = – 108 V, T_J = 25 °C

– Power Consumption Calculation for SLIC-P in Unbalanced Ringing Mode

A similar power calculation is valid for internal unbalanced ringing mode, which is only available for the SLIC-P.

With the following example:

$V_{DD} = 5$ V, $V_{BATL} = -30$ V, $V_{BATH} = -36$ V, $V_{BATR} = -150$ V and line feeding is guaran-teed up to 600 Ω.

Typical ringer load $R_{RNG} = 1000\ \Omega$, $C_{RNG} = 3.7\ \mu F$, required ringing voltage $V_{RNG} = 45$ Vrms and ringing frequency $f_{RNG} = 20$ Hz.

Table 26 shows the power calculation for the total power dissipation P_{TOT} of the SLIC-P in unbalanced ringing mode.

Table 26 SLIC-P Unbalanced Ringing Power Dissipation (typical)

$P_{TOT, RingPause} = P_Q + P_I + P_G + P_O$ ($I_{Trans} = 0$ mA)	**644 mW**
$P_{TOT, Ringing} = P_Q + P_I + P_G + P_O$	**2756 mW[1)]**
$P_Q = V_{DD} \times I_{DD} + \lvert V_{BATR}\rvert \times I_{BATR} + \lvert V_{BATH}\rvert \times I_{BATH} + \lvert V_{BATL}\rvert \times I_{BATL}$	349 mW
$P_I = 0.055 \times I_{Trans,rms} \times \lvert V_{BATR}\rvert + 0.04 \times I_{Trans,rms} \times V_{DD}$ with $I_{Trans,rms} = V_{TIP/RING, rms}/\lvert Z_{LD}\rvert$	160 mW
$P_G = (0.5 \times V_{TIP/RING}^2 - (V_{BATR}/2)^2)/60k + (V_{BATR}^2 - 80^2) \times (1/60k + 1/216k)$	295 mW
$P_O = \lvert V_{BATR}\rvert \times I_{Trans,rms} \times 2 \times SQRT(2)/\pi - V_{TIP/RING, rms} \times I_{Trans,rms} \times \cos(\phi_{Load})$	1952 mW

1) Values for $V_{DD} = 5$ V, $V_{BATL} = -30$ V, $V_{BATH} = -36$ V, $V_{BATR} = -150$ V, $T_J = 25$ °C

4.8 Integrated Test and Diagnosis Functions (ITDF)[1)]

4.8.1 Introduction

Subscriber loops are affected by a variety of failures which have to be monitored. Monitoring the loop supposes the access to the subscriber loop and to have test equipment in place which are capable to perform certain measurements. The measurements or tests involve resistance, capacitance, leakage, and measurements of interfering currents and voltages.

4.8.1.1 Conventional Line Testing

Conventional linecards in Central Office (CO) applications usually need two test relays per channel to access the subscriber loop with the appropriate test equipment. One relay (test-out) connects the actual test unit to the local loop. All required line tests can be accomplished that way. The second relay (test-in) separates the local loop from the SLIC-E/-E2/-P and connects a termination impedance to it. Hence, by sending a tone signal the entire loop can be checked, including the SLICOFI-2 and SLIC-E/-E2/-P.

4.8.1.2 DuSLIC Line Testing

The DuSLIC with its Integrated Test and Diagnosis Functions (ITDF) is capable to perform all tests necessary to monitor the local loop without an external test unit and test relays. The fact, that measurements can be accomplished much faster as with conventional test capabilities makes it even more a compelling argument for the DuSLIC. With the DuSLIC both channels are able to perform line tests concurrently, which also has a tremendous impact on the test time. All in all, the DuSLIC increases the quality of service and reduces the costs in various applications.

[1)] only available with DuSLIC-E/-E2/-P

4.8.2 Diagnostics

The two-channel chip set has a set of signal generators and features implemented to accomplish a variety of diagnostic functions. The SLICOFI-2 device generates all test signals, processes the information that comes back from the SLIC-E/-E2/-P and provides the data to a higher level master device, e.g. a microprocessor. All the tests can be initiated by the micropocessor and the results can be read back very easily. The Integrated Test and Diagnosis Functions (ITDF) might prevent any problem which affects service caused by the subscriber line or line equipment before the customer complains. IDTF has been integrated to facilitate the monitoring of the subscriber loop.

4.8.2.1 Line Test Capabilities

The line test comprises the following functions:

- Loop resistance
- Leakage current Tip/Ring
- Leakage current Tip/GND
- Leakage current Ring/GND
- Ringer capacitance
- Line capacitance
- Line capacitance Tip/GND
- Line capacitance Ring/GND
- Foreign voltage measurement Tip/GND
- Foreign voltage measurement Ring/GND
- Foreign voltage measurement Tip/Ring
- Measurement of ringing voltage
- Measurement of line feed current
- Measurement of supply voltage V_{DD} of the SLICOFI-2
- Measurement of transversal- and longitudinal current

Two main transfer paths (levelmeter) are implemented to accomplish all the different line measurement functions (refer to **Figure 45**).

4.8.2.2 Integrated Signal Sources

The signal sources available on the DuSLIC chip set are:

- Constant DC voltage (three programmable ringing DC offset voltages)
  Please refer to the CRAM coefficient set and register LMCR3 (bits RNG-OFFSET[1:0]) on **Page 206**.
- 2 independent tone generators TG1 and TG2:
  Please refer to the CRAM coefficient set and register DSCR (bits PTG, TG2-EN, TG1-EN) on **Page 200**.

- TTX metering signal generator (12/16 kHz)
  Please refer to the CRAM coefficient set and register BCR2 (bits TTX-DIS, TTX-12k) on **Page 192**.
- Ramp generator (used for capacitance measurements)
  Please refer to the CRAM coefficient set and register LMCR2 (bit RAMP-EN) on **Page 204**.
- Ring generator (5 Hz - 300 Hz)
  Please refer to the CRAM coefficient **Table 51 "CRAM Coefficients" on Page 226**.

Figure 45 shows the entire levelmeter block for AC and DC:

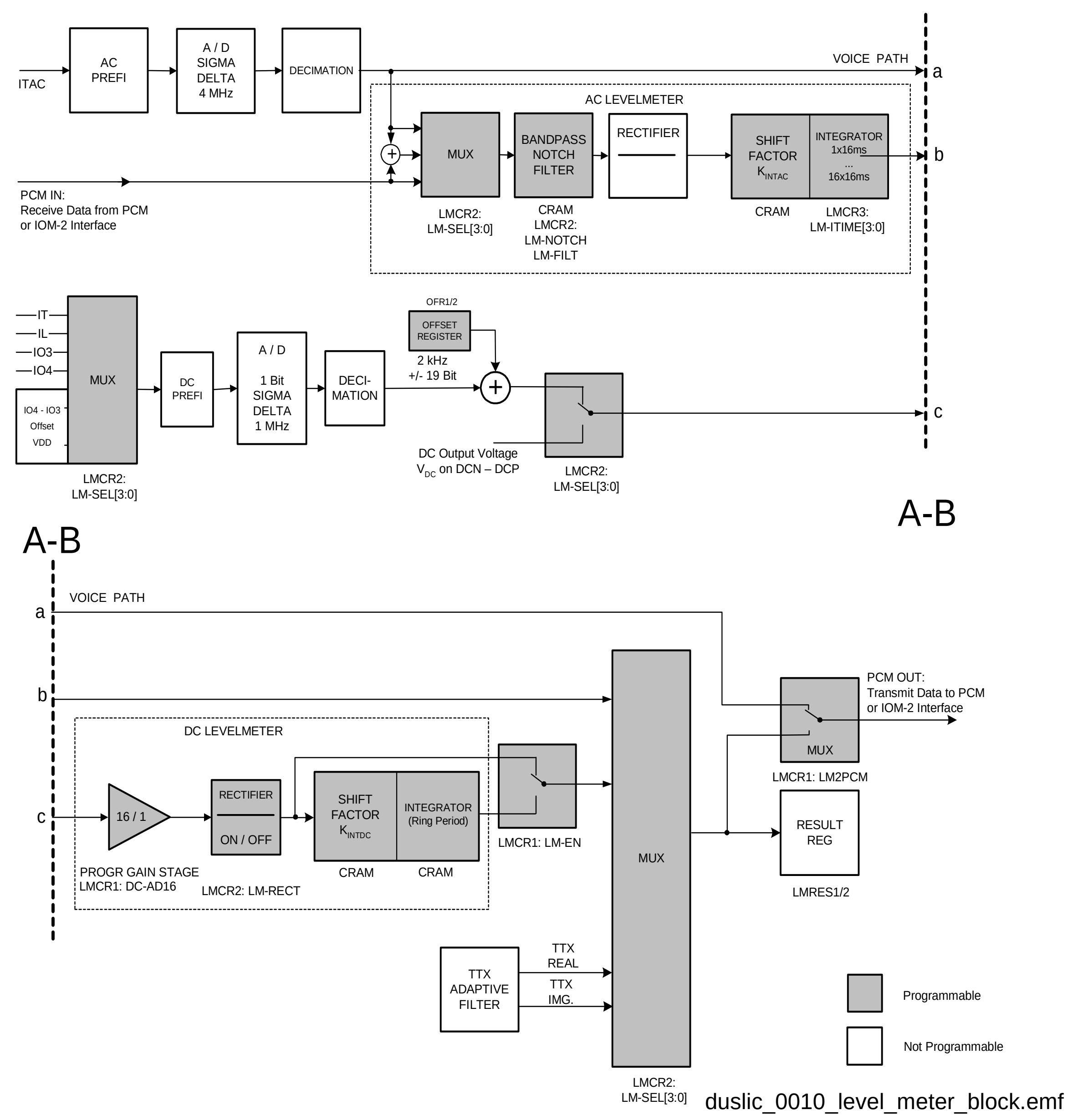

ITAC
AC PREFI
A / D SIGMA DELTA 4 MHz
DECIMATION
VOICE PATH
a
AC LEVELMETER
MUX
BANDPASS NOTCH FILTER
RECTIFIER
SHIFT FACTOR K_INTAC
INTEGRATOR 1x16ms ... 16x16ms
b
PCM IN: Receive Data from PCM or IOM-2 Interface
LMCR2: LM-SEL[3:0]
CRAM LMCR2: LM-NOTCH LM-FILT
CRAM
LMCR3: LM-ITIME[3:0]
IT
IL
IO3
IO4
IO4 - IO3
Offset
VDD
MUX
DC PREFI
A / D 1 Bit SIGMA DELTA 1 MHz
DECI-MATION
OFR1/2
OFFSET REGISTER
2 kHz +/- 19 Bit
c
DC Output Voltage V_DC on DCN – DCP
LMCR2: LM-SEL[3:0]
LMCR2: LM-SEL[3:0]
A-B
A-B
VOICE PATH
a
b
c
DC LEVELMETER
16 / 1
RECTIFIER
ON / OFF
SHIFT FACTOR K_INTDC
INTEGRATOR (Ring Period)
PROGR GAIN STAGE LMCR1: DC-AD16
LMCR2: LM-RECT
CRAM
CRAM
LMCR1: LM-EN
MUX
PCM OUT: Transmit Data to PCM or IOM-2 Interface
MUX
LMCR1: LM2PCM
RESULT REG
LMRES1/2
TTX ADAPTIVE FILTER
TTX REAL
TTX IMG.
LMCR2: LM-SEL[3:0]
Programmable
Not Programmable
duslic_0010_level_meter_block.emf

Figure 45 Blockdiagram Levelmeter

4.8.2.3 Result Register Data Format

The result of any measurement can be read via the result registers LMRES1/2. This gives a 16 bit value with LMRES1 being the high and LMRES2 being the low byte.

The result is coded in 16 bit two´s complement:

Table 27 Levelmeter Result Value Range

Negative Value Range		**Positive Value Range**	
– Fullscale			**+ Fullscale**
0x8000	0xFFFF	0	0x7FFF
– 32768	– 1	0	+ 32767

4.8.2.4 Using the Levelmeter Integrator

Both AC and DC levelmeter allow to use a programmable integrator. The integrator may be configured to run continuously or single.

Single Measurement Sequence (AC & DC Levelmeter)

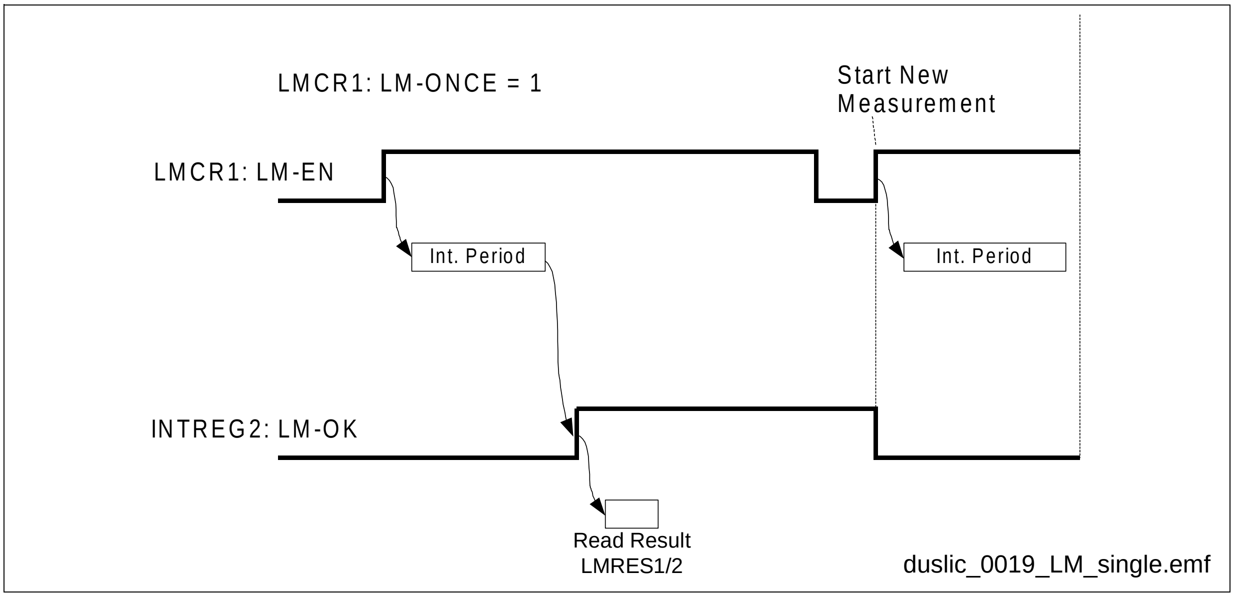

LMCR1: LM-ONCE = 1
Start New Measurement
LMCR1: LM-EN
Int. Period
Int. Period
INTREG2: LM-OK
Read Result LMRES1/2
duslic_0019_LM_single.emf

Figure 46 Single Measurement Sequence (AC&DC Levelmeter)

Continuous Measurement Sequence (DC Levelmeter)

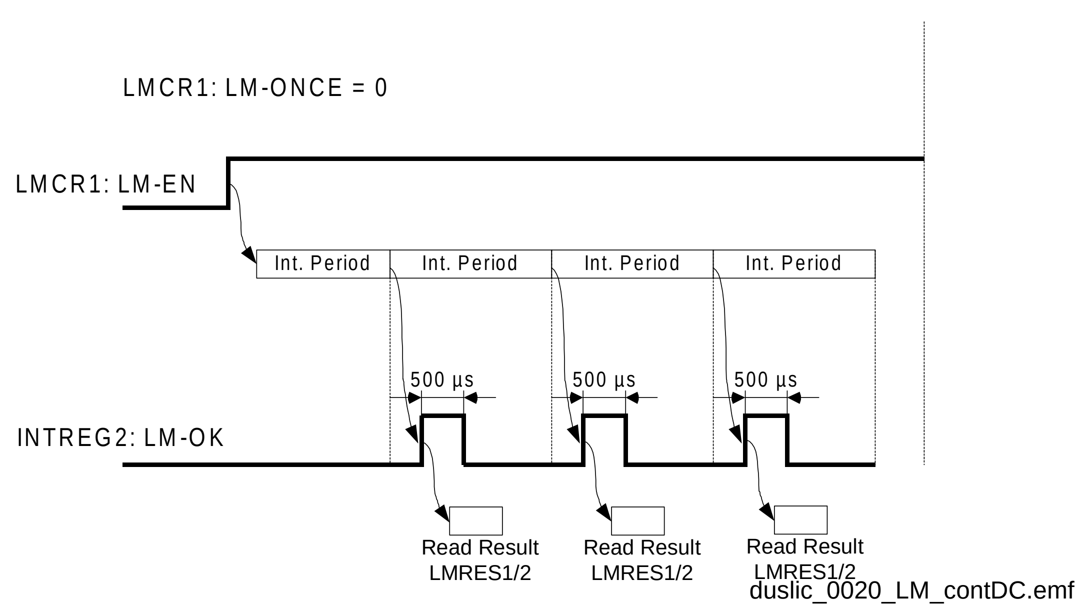

LMCR1: LM-ONCE = 0
LMCR1: LM-EN
Int. Period
Int. Period
Int. Period
Int. Period
500 µs
500 µs
500 µs
INTREG2: LM-OK
Read Result LMRES1/2
Read Result LMRES1/2
Read Result LMRES1/2
duslic_0020_LM_contDC.emf

Figure 47 Continuous Measurement Sequence (DC Levelmeter)

Continuous Measurement Sequence (AC Levelmeter)

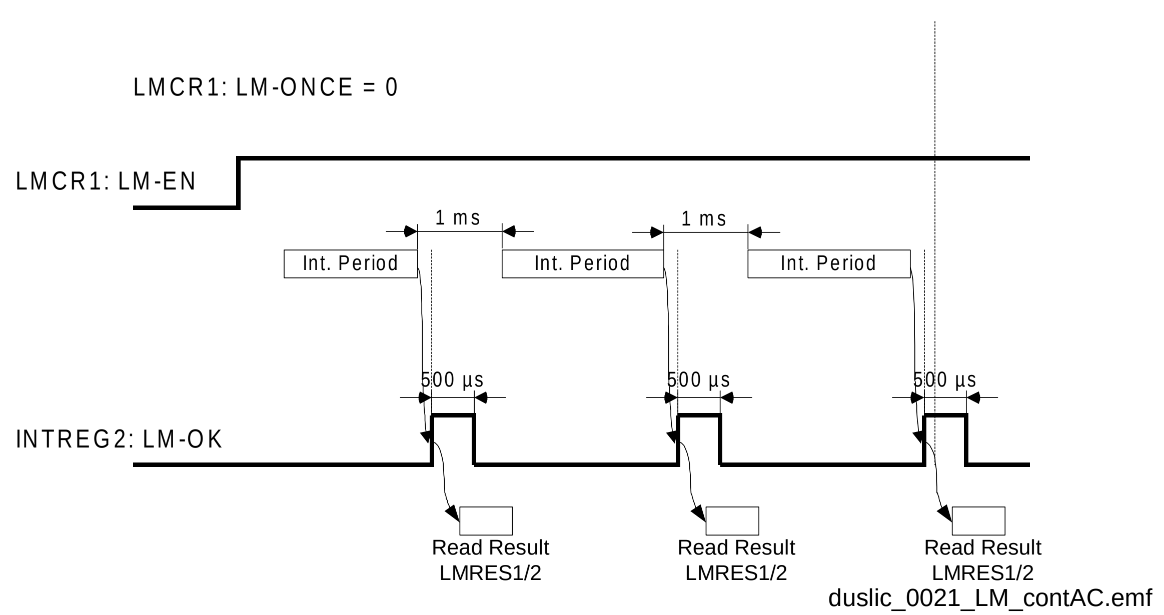

LMCR1: LM-ONCE = 0
LMCR1: LM-EN
1 ms
1 ms
Int. Period
Int. Period
Int. Period
500 µs
500 µs
500 µs
INTREG2: LM-OK
Read Result LMRES1/2
Read Result LMRES1/2
Read Result LMRES1/2
duslic_0021_LM_contAC.emf

Figure 48 Continuous Measurement Sequence (AC Levelmeter)

4.8.2.5 DC Levelmeter

The path of the DC levelmeter is shown in **Figure 45**. Hereby, the DC levelmeter results will be determined and prepared depending on certain configuration settings. The selected input signal becomes digitized after pre-filtering and analog-to-digital conversion. The DC levelmeter is selected and enabled as shown in **Table 28**:

Table 28 Selecting DC Levelmeter Path

LM-SEL[3:0] in register LMCR2	DC Levelmeter Path
0100	DC out voltage on DCP-DCN
0101	DC current on IT
1001	DC current on IL
1010	Voltage on IO3
1011	Voltage on IO4
1101	V_{DD}
1110	Offset of DC-pre-filter (short circuit on DC-pre-filter input)
1111	Voltage on IO4 – IO3

The effective sampling rate after the decimation stages is 2 kHz. The decimated value has a resolution of 19 bits. The offset compensation value (see **Chapter 4.8.2.8**) within the offset registers OFR1 (bits OFFSET-H[7:0]) and OFR2 (bits OFFSET-L[7:0]) can be set to eliminate the offset caused by the SLIC-E/-E2/-P current sensor, pre-filter, and analog-to-digital converter. After the summation point the signal passes a programmable digital gain filter. The additional gain factor is either 1 or 16 depending on register LMCR1 (bit DC-AD16):

- LMCR1 (bit DC-AD16) = 0: No additional gain factor
- LMCR1 (bit DC-AD16) = 1: Additional gain factor of 16

The rectifier after the gain filter can be turned on/off with:

- LMCR2 (bit LM-RECT) = 0: Rectifier disabled
- LMCR2 (bit LM-RECT) = 1: Rectifier enabled

A shift-factor K_{INTDC} in front of the integrator prevents the levelmeter during an integration operation to create an overflow. If an overflow in the levelmeter occurs, the output result will be ± fullscale (see **Table 27**).

If the shift factor K_{INTDC} is set to e.g. 1/8, the content of the levelmeter result register is the integration result divided by 8.

The shift factor K_{INTDC} is set in the CRAM (offset address 0x76):

CRAM:

Address 0x76: LMDC2/LMDC1
Address 0x77: 0/LMDC3

LMDC1, LMDC2 and LMDC3 are 4 bit nibbles which contain K_{INTDC}.

Table 29 K_{INTDC} Setting Table

LMDC1	**LMDC2**	**LMDC3**	**K_{INTDC}**
8	8	0	1
8	8	1	½
8	8	:	:
8	8	6	1/64
8	8	7	1/128

DuSLICOS allows to automatically calculate the coefficients for K_{INTDC} for I_{TRANS} measurement. The expected "Current for Ring Off-hook Detection" (see DuSLICOS DC Control Parameter 2/3) of e.g. 20 mA is entered in to the program and then K_{INTDC} is automatically calculated to achieve 50 % full scale if the current of 20 mA is integrated over the set ringer period.

The integration function accumulates and sums up the levelmeter values over a set time period. The time period is determined by the programmed ring frequency. A ring frequency f_{RING} of 20 Hz results in 100 samples ($N_{Samples}$), because of the 2 kHz effective DC sampling rate $f_{S,DC}$.

$$N_{Samples} = \frac{f_{S,DC}}{f_{RING}} = \frac{2000\,\mathrm{Hz}}{f_{RING}}$$

The number of integration samples $N_{Samples}$ may also be programmed directly by accessing dedicated bytes in the Coefficient RAM (CRAM).

CRAM:

Address 0x73: RGF2/RGF1
Address 0x74: RGA1/RGF3

RGF1, RGF2 and RGF3 are 4 bit nibbles which control the ring frequency $f_{RING.}$

RGA1 is a 4 bit nibble which is calculated by DuSLICOS and controls the ringer amplitude (see DuSLICOS byte file). To ensure that RGA1 is not changed please perform a read/modify/write operation.

Table 30 $N_{Samples}$ Setting Table

RGF1	RGF2	RGF3	f_{RING}	$N_{Samples}$
8	8	0	500	4
8	8	1	250	8
8	8	:	:	:
8	8	6	7.81	256
8	8	7	3.91	512

The integration function can be turned on and off by bit LM-EN in register LMCR1.

The levelmeter result of the selected signal source will be stored in the result registers LMRES1 (bits LM-VAL-H[7:0]) and LMRES2 (bits LM-VAL-L[7:0]) depending on the LM-SEL[3:0] bits in register LMCR2. The result registers get frequently updated every 500 µs if bit LM-EN in register LMCR1 = 0, or after an integration period, if bit LM-EN in register LMCR1 = 1. If the bit LM-ONCE in register LMCR1 is set to 1 then the integration is executed only once. To start again bit LM-EN has to be set from 0 to 1.
The levelmeter source/result can be transferred to the PCM/IOM-2 interface, depending on the bit LM2PCM in register LMCR1.

Table 31 shows the levelmeter results without and with integrator function. The integrator is enabled if bit LM-EN in register LMCR1 = 1.

The levelmeter result LM_{Value} is a 16 bit two´s complement value of LM-VAL-H[7:0] and LM-VAL-L[7:0].

The factor LM_{Result} used in **Table 31** is defined:

$$LM_{Result} = \frac{LM_{Value}}{32768}$$

- Example for positive value of LM_{Result}:

LM-VAL-H = "0010 0100" = 0x24

LM-VAL-L = "1010 0101" = 0xA5

LM_{Value} = 0x24A5 = 9381

LM_{Result} = 0.2863

- Example for negative value of LM_{Result}:

LM-VAL-H = "1001 1001" = 0x99

LM-VAL-L = "0110 0010" = 0x62

LM_{Value} = 0x9962 = – 26270

LM_{Result} = – 0.8017

Table 31 Levelmeter Results with and without Integrator Function

	LM-EN = 0 (without Integrator)	**LM-EN = 1 (with Integrator)**
I_{TRANS}1): Power Down Resistive	$I_{TRANS} = LM_{Result} \times \frac{K_{IT,PDR}}{R_{IT2}} \times V_{AD}$ $I_{TRANS} = LM_{Result} \times 7.966\text{ mA}$	$I_{TRANS} = LM_{Result} \times \frac{K_{IT,PDR} \times V_{AD}}{R_{IT2} \times N_{Samples} \times K_{INTDC}}$ $I_{TRANS} = LM_{Result} \times \frac{7.966\text{ mA}}{N_{Samples} \times K_{INTDC}}$
I_{TRANS}1): any other mode	$I_{TRANS} = LM_{Result} \times \frac{K_{IT}}{R_{IT2}} \times V_{AD}$ $I_{TRANS} = LM_{Result} \times 79.66\text{ mA}$	$I_{TRANS} = LM_{Result} \times \frac{K_{IT} \times V_{AD}}{R_{IT2} \times N_{Samples} \times K_{INTDC}}$ $I_{TRANS} = LM_{Result} \times \frac{79.66\text{ mA}}{N_{Samples} \times K_{INTDC}}$
I_{LONG}2)	$I_{LONG} = -LM_{Result} \times \frac{K_{IL}}{R_{IL}} \times V_{AD}$ $I_{LONG} = -LM_{Result} \times 67.7\text{ mA}$	$I_{LONG} = -LM_{Result} \times \frac{K_{IL} \times V_{AD}}{R_{IL} \times N_{Samples} \times K_{INTDC}}$ $I_{LONG} = -LM_{Result} \times \frac{67.7\text{ mA}}{N_{Samples} \times K_{INTDC}}$
Voltage: IO33), IO44), IO4-IO35)	$V_{INPUT} = -LM_{Result} \times V_{AD}$	$V_{INPUT} = -LM_{Result} \times \frac{V_{AD}}{N_{Samples} \times K_{INTDC}}$
V_{DD}	$V_{DD} = -LM_{Result} \times 3.9\text{ V}$	$V_{DD} = -LM_{Result} \times \frac{3.9\text{ V}}{N_{Samples} \times K_{INTDC}}$
V_{DC}6) with ACTL, ACTH	$V_{DC} = -LM_{Result} \times 76.35\text{ V}$	$V_{DC} = -LM_{Result} \times \frac{76.35\text{ V}}{N_{Samples} \times K_{INTDC}}$
V_{DC}6) with ACTR, ringing mode	$V_{DC} = -LM_{Result} \times 152.7\text{ V}$	$V_{DC} = -LM_{Result} \times \frac{152.7\text{ V}}{N_{Samples} \times K_{INTDC}}$

1) DC current on pin IT (bits LM-SEL[3:0] = 0101)

2) DC current on pin IL (bits LM-SEL[3:0] = 1001)

3) Voltage on IO3 referenced to V_{VCM} (typical 1.5 V) (bits LM-SEL[3:0] = 1010)

4) Voltage on IO4 referenced to V_{VCM} (typical 1.5 V) (bits LM-SEL[3:0] = 1011)

5) Voltage on IO4 – IO3 referenced to V_{VCM} (typical 1.5 V) (bits LM-SEL[3:0] = 1111)

6) DC output voltage at SLIC measured via DCN – DCP (bits LM-SEL[3:0] = 0100)

K_{INTDC}	Shift Factor (see **Table 29**)	
$K_{IT,PDR}$	Value of the current divider in power down resistive mode	5
K_{IT}	Value of the current divider for transversal current	50
K_{IL}	Value of the current divider for longitudinal current	100
R_{IT2}	Sense resistor for transversal current	680 Ω
R_{IL}	Sense resistor for longitudinal current	1600 Ω
V_{AD}	Voltage at A/D converter refered to digital fullscale	1.0834
V_{DC}	DC output voltage at SLIC measured via DCN – DCP	

Note: Measurement of pins IL, IO3, IO4, IO4-IO3 and VDD can cause problems in the DC loop. The measured value is always interpreted as I_{TRANS} *current. This can disturb the DC regulation and the off-hook indication. In active mode you can freeze the output of the DC loop by setting the bit LM-HOLD to '1'. In ringburst mode it is possible that DuSLIC automatically switches back to ringpause mode because the measurement result was interpreted as off-hook. This can be avoided by programming the off-hook current to the maximum value (79.66 mA).*

Measurement of AC signals via DC levelmeter

This method is applicable for a single frequency sinusoidal AC signal which is superimposed on a DC signal.

1. Set the ring frequency f_{RING} to the frequency of the signal to be measured. Multiples of the expected signal period may also be used.
2. Set the offset registers OFR1 and OFR2 to 0x00.
3. Measure the DC content with disabled rectifier (bit LM-RECT = 0).
   The DC content can be calculated as described in **Table 31**.
   Note: If there was an overflow inside the integrator during the integration period, the result will be ± fullscale. Reduce the shift factor K_{INTDC} *or the number of samples* $N_{Samples}$ *and start the measurement again.*
4. The offset registers OFR1 and OFR2 have to be programmed to the value
   $$\mathrm{OFFSET} = -\frac{LM_{Value}}{N_{Samples} \times K_{INTDC}}$$
   where OFR1 is the high byte and OFR2 is the low byte of the 16 bit word OFFSET.
5. Repeating the measurement of the DC content should result in a LM_{Value} of zero.
6. Perform a new measurement with the rectifier enabled (bit LM-RECT = 1). The result is the rectified mean value of the measured signal an can be calculated with the formulas of **Table 31**.
7. From this result the peak value and the RMS value can be calculated:

$$V_{Peak} = \frac{|V|_{Mean} \times \pi}{2}$$

$$V_{RMS} = \frac{V_{Peak}}{\sqrt{2}}$$

4.8.2.6 AC Levelmeter

The AC levelmeter is selected and enabled as shown in **Table 32**:

Table 32 Selecting AC Levelmeter Path

LM-SEL[3:0] in register LMCR2	AC Levelmeter Path
0000	AC levelmeter in transmit
0110	AC levelmeter in receive
0111	AC levelmeter receive + transmit

Figure 45 on **Page 109** shows the path of the AC/TTX levelmeter functions. The AC levelmeter allows access to the voice signal while the active voice signal is being processed. The input signal for the AC levelmeter might get processed with a programmable filter characteristic, i.e. bandpass- or notch filter. Depending on the following settings, the bandpass or notch filter is turned on or off:

- Register LMCR2 bit LM-FILT = 0: No filter enabled (normal operation)
- Register LMCR2 bit LM-FILT = 1: Bandpass/notch filter characteristics enabled
- Register LMCR2 bit LM-NOTCH = 0: Notch filter enabled, bandpass filter disabled
- Register LMCR2 bit LM-NOTCH = 1: Bandpass filter enabled, notch filter disabled

The rectifier cannot be turned off, it is always active in the AC path. A shift-factor in front of the integrator prevents the levelmeter during an integration operation to create an overflow. The shift-factor can be set by the coefficient LM-AC gain (see CRAM coefficient set **Table 51 "CRAM Coefficients" on Page 226**).

K_{INTAC} can be set via coefficient LM-AC:

CRAM:

Address 0x34: CG1/LM-AC

LM-AC is a 4 bit nibble which contains $K_{INTAC.}$

CG1 is a 4 bit nibble which is calculated by DuSLICOS and controls the conference gain (see DuSLICOS byte file). To ensure that CG1 is not changed please perform a read/ modify/write operation.

Table 33 K_{INTAC} Setting Table

LM-AC	K_{INTAC}
0	1
1	½
:	:
6	1/64
7	1/128

The integration function accumulates and sums up the levelmeter values over a set time period. The time period from 1*16 ms to 16*16 ms is set by the bits LM-ITIME[3:0] in register LMCR3. The integration function can be turned on and off by bit LM-EN in register LMCR1.

The number of samples $N_{Samples}$ for the integrator is defined by:

$N_{Samples}$ = LM-ITIME * 8000

The level can be calculated by:

$$U_{dBm0} = 20 \times \log\left(LM_{Result} \times \frac{\pi}{2 \times K_{INT} \times N_{Samples}}\right) + 3.14$$

The result registers get frequently updated after an integration period, if bit LM-EN in register LMCR1 = 1. If the bit LM-ONCE in register LMCR1 is set to 1 then the integration is executed only once. To start again bit LM-EN has to be set from 0 to 1.
The levelmeter result can be transferred to the PCM/IOM-2 interface, depending on bit LM2PCM in register LMCR1.

Measurement of currents via ITAC

In order to do current measurements via pin ITAC, all feedback loops (IM-filters and TH-filters) should be disabled. To simplify the formulas, the programmable receive and transmit gain is disabled.

This is done by setting the following bits:

Register BCR4:	AR-DIS = 1, AX-DIS = 1, TH-DIS = 1, IM-DIS = 1, FRR-DIS = 1, FRX-DIS = 1
Register TSTR4:	OPIM-AN = 1, OPIM-4M = 1
Register LMCR1:	TEST-EN = 1

This setting results in a receive gain of 11.88 dB caused by the internal filters. Based on this a factor K_{AD} (analog to digital) can be defined:

$$K_{AD} = \frac{10^{\frac{filter_{AD}}{20}}}{V_{ADC}} = \frac{10^{\frac{11.88\ V}{20}}}{1.2} = 3.272\ V^{-1}$$

Transversal current I_{RMS} measured at SLIC:

$$I_{RMS} = \frac{LM_{Result} \times K_{IT} \times \pi}{K_{AD} \times R_{ITAC} \times K_{INTAC} \times N_{Samples} \times 2 \times \sqrt{2}} = \frac{LM_{Result}}{K_{INTAC} \times N_{Samples}} \times 14.76\ mA$$

R_{ITAC}	Sense resistor for AC transversal current (R_{IT1} + R_{IT2})	1150 Ω
K_{AD}	Constant factor from Analog to Digital	$3.272\ V^{-1}$
V_{ADC}	Voltage at A/D converter refered to digital fullscale	1.2 V
K_{IT}	Value of the current divider for transversal current	50

In order not to overload the analog input, the maximum AC transversal current may not be higher than 9 mA rms.

Usage of Tone Generator as Signal Source

To simplify the formulas, the programmable receive and transmit gain is disabled.

This is done by setting the following bits:

Register BCR4:	AR-DIS = 1, AX-DIS = 1, TH-DIS = 1, IM-DIS = 1, FRR-DIS = 1, FRX-DIS = 1
Register TSTR4:	OPIM-AN = 1, OPIM-4M = 1
Register LMCR1:	TEST-EN = 1

The tone generator level is influenced by a factor K_{TG} which is set in the tone generator coefficients. The internal filter attenuation is 2.87 dB.

$$K_{DA} = V_{DAC} \times 10^{\frac{-2.87}{20}} \times \frac{Trapez}{\sqrt{2}} \times K_{AC,SLIC} = 1.2 \times 10^{\frac{-2.87}{20}} \times \frac{1.05}{\sqrt{2}} \times 6$$

K_{DA}	Constant factor from Digital to Analog	3.84 Vrms
$K_{AC,SLIC}$	Amplification factor of the SLIC	6
V_{DAC}	Voltage at D/A converter refered to digital fullscale	1.2 V
Trapez	Crestfactor of the trapazoidal signal	1.05

Output voltage between Tip and Ring:

$V_{OUT} = K_{DA} * K_{TG}$

The bytes below are valid for tone generator TG1 an a frequency of 1000 Hz.

CRAM:

Address 0x38: 0x08
Address 0x39: T11G/0
Address 0x40: T13G/T12G
Address 0x41: 0x05
Address 0x42: 0xB3
Address 0x43: 0x01

T11G, T12G and T13G are 4 bit nibbles which control the amplitude of the tone generator TG1.

Table 34 K_{TG} Setting Table

T11G	**T12G**	**T13G**	K_{TG}
8	9	1	7/8
8	0	8	½
8	1	8	¼
8	:	8	:
8	5	8	1/64
8	6	8	1/128
8	7	8	1/256

4.8.2.7 Levelmeter Threshold

For the levelmeter result a threshold can be set. When the result exceeds the threshold then bit LM-THRES in register INTREG 2 is set to '1'. It is also possible to activate an interrupt when the LM-THRES bit changes by setting the bit LM-THM (levelmeter threshold mask bit) in register LMCR2 to '0'.

The levelmeter threshold can be calculated with DuSLICOS or taken from **Table 35**.

CRAM:

Address 0x32: LMTH2/LMTH1
Address 0x33: 0/LMTH3

(LMTH1, LMTH2 and LMTH3 are 4 bit nibbles)

Table 35 Threshold Setting Table

LMTH1	**LMTH2**	**LMTH3**	**Threshold**
1	0	0	75.0 %
0	1	0	62.5 %
8	8	0	50.0 %
8	9	0	37.5 %
9	0	0	25.0 %
8	1	0	12.5 %
8	0	0	0.0 %

4.8.2.8 Current Offset Error Compensation

The current offset error caused by the current sensor inside the SLIC-E/-E2/-P can be compensated by programming the compensation registers OFR1 and OFR2 accordingly. The current offset error can be measured with the DC levelmeter. The following settings are necessary to accomplish this:

- The DuSLIC has to be set into the HIRT mode by setting the bits HIR and HIT in register BCR1 to 1.
  In HIRT mode the line-drivers of the SLIC-E/-E2/-P are shut down and no resistors are switched to the line. As a matter of fact, no current is present in that mode, but the current sensor wrongly indicates a current flowing (current offset error).
- The DC path for I_{TRANS} current levelmeter must be selected by setting the LM-SEL[3:0] bits in register LMCR2 to 0101 (see **Table 28**).
- The offset registers OFR1 and OFR2 must be set to 0000h.
- $I_{Off\text{-}Err}$ can be calculated like shown for "I_{TRANS}: any other mode" in **Table 31** (see also example below).

The current offset error can be eliminated by programming the offset registers OFR1 and OFR2 according to the inverse value of the measured current offset error.

Example:

$K_{INTDC} = 1$, $N_{Samples} = 256$, $LM_{Value} = 0x0605 = 1541$

$$LM_{Result} = \frac{LM_{Value}}{32768} = \frac{1541}{32768} = 0.047$$

$$I_{off-Err} = LM_{Result} \times \frac{79.66\text{ mA}}{N_{Samples} \times K_{INTDC}} = 0.047 \times \frac{79.66\text{ mA}}{256 \times 1} = 0.0146\text{ mA}$$

$$OFFSET = -\frac{I_{Off-Err}}{79.66\text{ mA}} \times 32768 = -\frac{0.0146\text{ mA}}{79.66\text{ mA}} \times 32768 \approx -6 = 0xFFFA$$

Short form:

$$OFFSET = -\frac{LM_{Value}}{N_{Samples} \times K_{INTDC}}$$

OFR1 = OFFSET-H = 0xFF

OFR2 = OFFSET-L = 0xFA

4.8.2.9 Loop Resistance Measurements

The DC loop resistance can be determined by supplying a constant DC voltage $V_{TR,DC}$ to the Ring- and Tip line and measuring the DC loop current via IT pin. The following steps are necessary to accomplish this:

- Program a certain ring offset voltage RO1, RO2, RO3 (see DuSLICOS DC Control Parameter 2/3).
- Select ring offset voltage RNG-OFFSET[1:0] in register LMCR3 either to 01, 10 or 11. If 00 is selected, the DC regulation would be still active and would not allow resistance measurement.
- Choose an operation mode, either Active High (ACTH) or Ring Pause.
- Select the DC path for levelmeter by setting the bits LM-SEL[3:0] in register LMCR2 to 0101 (DC current on IT).
- The transversal current can be determined by reading the levelmeter result registers LMRES1, LMRES2.
- Based on the known constant output voltage $V_{TR,DC}$ (DC voltage according to RNG-OFFSET[1:0]) and the measured I_{TRANS} current, the resistance can be calculated. It should be noted, that the calculated resistance includes also the onboard resistors R_{PROT} and R_{STAB}.

In order to increase the accuracy of the result, either the current offset can be compensated or the measurement can be done differentially. The latter one eliminates the current- and voltage offsets.

Figure 49 shows an example circuit for resistance measurement:

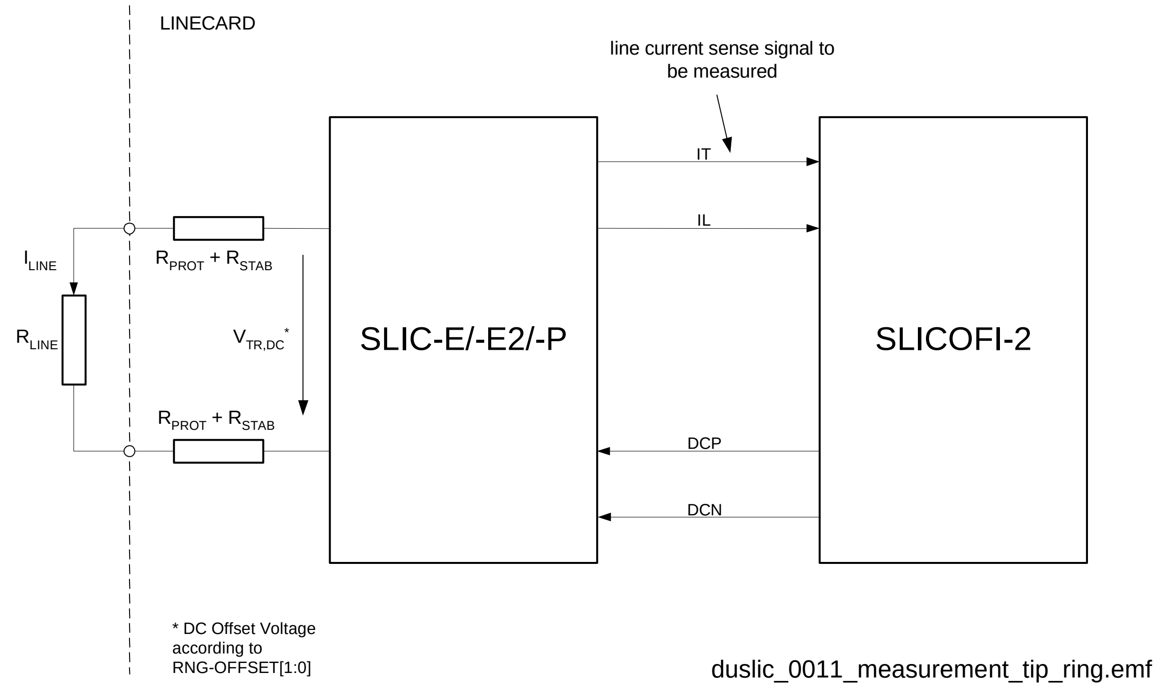

LINECARD
line current sense signal to be measured
IT
IL
DCP
DCN
SLIC-E/-E2/-P
SLICOFI-2
I_{LINE}
R_{LINE}
$R_{PROT} + R_{STAB}$
$V_{TR,DC}^{*}$
$R_{PROT} + R_{STAB}$
* DC Offset Voltage according to RNG-OFFSET[1:0]
duslic_0011_measurement_tip_ring.emf

Figure 49 Example Resistance Measurement

Assumption:

- Loop resistance $R_{loop} = 1000\ \Omega$; $R_{loop} = R_{LINE} + 2{*}R_{PROT} + 2{*}R_{STAB}$
- Ring offset RO2 = 60 V (CRAM coefficient set accordingly). Ring offset RO2 is selected by setting bits RNG-OFFSET[1:0] in register LMCR3 to 10.
  The exact value for the Ring offset voltage can be determined from the *.res result file generated by DuSLICOS during the calculation of the appropriate coefficients.
- Select Active High (ACTH) mode by setting the line mode command CIDD/CIOP bits M2, M1, M0 to 010. In ACTH mode half of the ring offset voltage RO2 of e.g. 60 V will be present and applied to Ring and Tip.

Sequence to determine the loop resistance R_{loop} differentially:

- Select DC levelmeter by setting bits LM-SEL[3:0] in register LMCR2 to 0101.
- Read levelmeter result registers LMRES1, LMRES2.
- Switch into reverse polarity mode by setting bit REVPOL in register BCR1 to 1.
- Read levelmeter result registers LMRES1, LMRES2.

If the loop resistor connected between Ring and Tip is 1000 Ω ($R_{LINE} + R_{PROT} + R_{STAB}$), the expected current will be 30 mA, because the actual voltage applied to Ring and Tip is 30 V. Considering the fact, that the current measurement in reverse polarity mode will also become inverted, the read results have to be added. The sum of both levelmeter results (normal- and reverse polarity) should therefore be 60 mA current difference.

Figure 50 shows the differential measurement method and the elimination of the offsets.

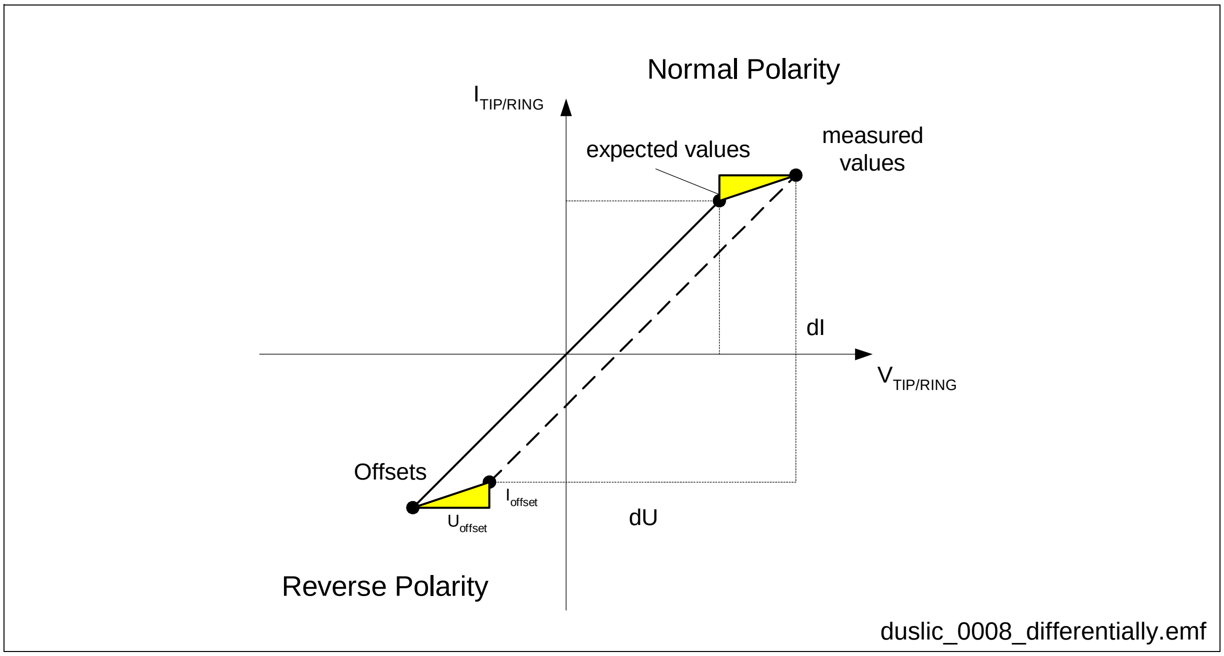


Figure 50 Differential Resistance Measurement

The following calculation shows the elimination of the voltage and current offset caused by output stage and current sensor. This differential measurement method both eliminates the offsets caused by the SLIC-E/-E2/-P current sensor and the offset caused by the DC voltage output (Ring offset voltage).

Differential Resistance Calculation:

$$I_{\mathrm{measure(normal)}} = \frac{V_{\mathrm{TR,\,prog}} + V_{\mathrm{offset}}}{R} + I_{\mathrm{offset}}$$

$$I_{\mathrm{measure(reverse)}} = \frac{-V_{\mathrm{TR,\,prog}} + V_{\mathrm{offset}}}{R} + I_{\mathrm{offset}}$$

$$I_{\mathrm{measure(normal)}} - I_{\mathrm{measure(reverse)}} = \frac{2 \times V_{\mathrm{TR,\,prog}}}{R}$$

$$R = \frac{2 \times V_{\mathrm{TR,\,prog}}}{I_{\mathrm{measure(normal)}} - I_{\mathrm{measure(reverse)}}} = R_{\mathrm{LINE}} + R_{\mathrm{PROT}} + R_{\mathrm{STAB}}$$

4.8.2.10 Line Resistance Tip/GND and Ring/GND

The DuSLIC offers the modes of setting either the Tip- or the Ring line to high impedance or even both by setting the bits HIR and HIT in register BCR1 accordingly. While one of both lines is set to high impedance, the other line is still active and able to supply a known voltage. The transversal and/or longitudinal current can be measured and the line impedance can be calculated.

Because of one line (Tip or Ring) being high impedance, there is only current flowing in either Tip or Ring line. This causes the calculated current (according **Table 31**) to be half the actual value. Therefore in either HIR or HIT mode the calculated current has to be multiplied by a factor of 2.

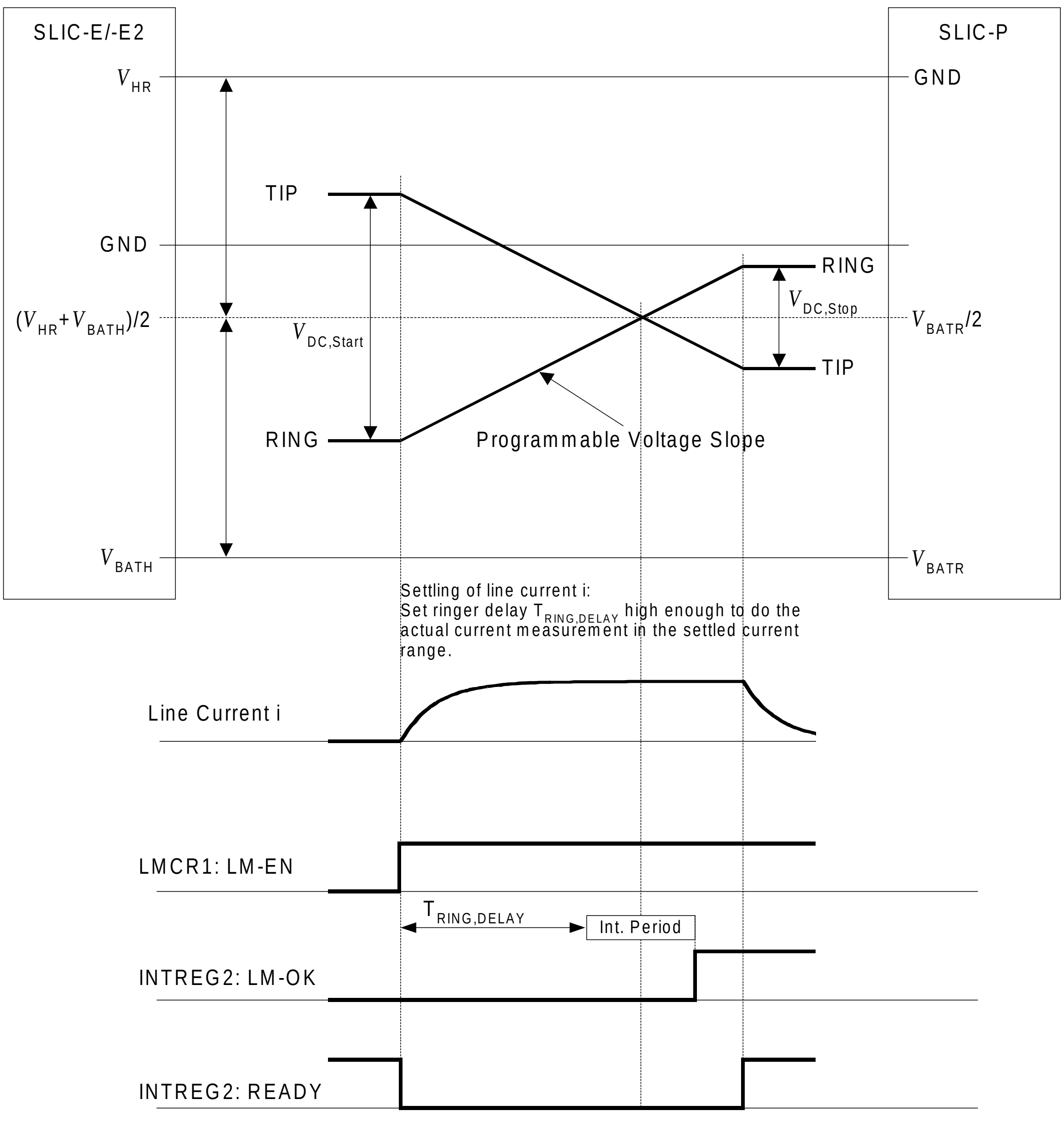
4.8.2.11 Capacitance Measurements

Capacitance measurements with the DuSLIC are accomplished by using the integrated ramp generator function. The ramp generator is capable of applying a voltage ramp to the Ring- and Tip line with the flexibility of:

- Programmable slopes from 30 V/s to 2000 V/s
- Programmable start- and stop DC voltage offsets via ring offsets
- Programmable start time of the voltage ramp after enabling the levelmeter function

Figure 51 shows the voltage ramp and the voltage levels at the Ring and Tip line.

The slope of the ramp can be programmed (refer to CRAM coefficients). The ring offset voltages RO1, RO2 and RO3 might be used as start and stop voltages. The ramp starts for instance at RO1 and stops at RO2. The current can be calculated as $i(t) = C_{Measure}*dU/dt$, where dU/dt is the slope and i(t) is the current which will be measured by the levelmeter. In order to measure accurate values, the integration has to start after the current has settled to a constant value. This can be calculated by the time constant of the ringer load. It is recommended to set the programmable ring generator delay higher than 3 times the time constant of the ringer load. When there is a resistor in parallel to the capacitor (e.g. leakage), it is recommended to measure symmetrically around the voltage zero crossing. This can be achieved by programming the ring generator delay appropriately (see DuSLICOS DC Control Parameter 2/3). The integration time for the current measurement is determinded by the ring frequency (refer to CRAM coefficients, see **Table 30**). After the integration time the measurement automatically stops only when the bit LM-ONCE in register LMCR1 is set. Otherwise the levelmeter would continuously measure the current even if the ramp is finished and turned into its constant voltage position, i.e., that because of the constant voltage no current will flow.


SLIC-E/-E2
V_{HR}
GND
$(V_{HR}+V_{BATH})/2$
V_{BATH}
SLIC-P
GND
$V_{BATR}/2$
V_{BATR}
TIP
RING
$V_{DC,Start}$
RING
TIP
$V_{DC,Stop}$
Programmable Voltage Slope
Settling of line current i:
Set ringer delay $T_{RING,DELAY}$ high enough to do the actual current measurement in the settled current range.
Line Current i
LMCR1: LM-EN
$T_{RING,DELAY}$
Int. Period
INTREG2: LM-OK
INTREG2: READY

ezm14053.emf

Figure 51 Capacitance Measurement

Example:

- Assumptions:
  - Capacitance as object to be determined: $C_{Measure}$ = 9.8 µF
  - Resistor $R_{Measure}$ in series to $C_{Measure}$: $R_{Measure}$ = 6930 Ω
  - $\tau = R_{Measure} * C_{Measure}$ = 67.9 ms
- Calculating parameter values:
  - Choose Ring Offset voltage 1: RO1 = 70 V (Start voltage on Ring/Tip where the ramp should start; programmed by ring offset voltage RO1)
  - Choose Ring Offset voltage 2: RO2 = – 30 V (End voltage on Ring/Tip where the ramp should stop; programmed by ring offset voltage RO2)
  - Choose slope of ramp while testing: dU/dt = 200 V/s
  - Time from start to stop of the ramp from RO1 to RO2 is 100 V/200 V/s = 500 ms
  - Time from start to zero cross is 70 V/200 V/s = 350 ms
  - Choose Integration time: $T_I = 1/f_{RING}$ = 1/100 Hz = 10 ms
  - Measure around zero cross → from 345 ms to 355 ms
  - $T_{RING,DELAY}$ is programmed to 345 ms
  - Check ring generator delay: $T_{RING,DELAY} > 3*\tau$ = 204 ms → OK!
  - Expected current $i = C_{Measure} * dU/dt$ = 1.96 mA
  - Choose current for LM off-hook threshold $I_{LM,DC}$ = 2 mA
    Note: A current of 2 mA will result in LM_{Result} = 0.5 (half of the fullscale value)

Program Sequence:

- Set the following parameter values:

Parameter	Symbol & Value	DuSLICOS
Slope of ramp while testing	dU/dt = 200 V/s	DC Control Parameter 3/3
Ring frequency	f_{RING} = 100 Hz	DC Control Parameter 2/3
Ring generator delay	$T_{RING,DELAY}$ = 345 ms	DC Control Parameter 2/3
Ring offset voltage 1	RO1 = 70 V	DC Control Parameter 2/3
Ring offset voltage 2	RO2 = – 30 V	DC Control Parameter 2/3
Current for LM off-hook threshold	$I_{LM,DC}$ = 2 mA	DC Control Parameter 2/3

- Integration time $T_I = 1/f_{RING}$ = 1/100 Hz = 10 ms
- Select the DC levelmeter by setting bits LM-SEL[3:0] in register LMCR2 to 0101
- Execute the levelmeter only once by setting bit LM-ONCE in register LMCR1 to 1.
- Apply Ring Offset voltage RO1 to Ring and Tip line by setting bits RNG-OFFSET[1:0] in register LMCR3 to 01.
- Enable the ramp generator by setting bit RAMP-EN in register LMCR2 to 1.

- Apply Ring Offset voltage RO2 to Ring and Tip line by setting bits RNG-OFFSET[1:0] in register LMCR3 to 10.
- Enable the levelmeter by setting bit LM-EN in register LMCR1 to 1.
  - Comment: The voltage ramp starts at RO1 and ramps up/down until RO2 is achieved. After the integration time, the result will be stored within LMRES1 and LMRES2 registers.
- Read the result registers LMRES1 and LMRES2

The actual current $I_{CMeasure}$ amounts to:

$$I_{CMeasure} = 2 \times I_{LM,DC} \times LM_{Result}$$

The capacitance $C_{Measure}$ calculates as:

$$C_{Measure} = \frac{I_{CMeasure}}{\frac{dU}{dt}}$$

Example:

LM_{Value} = 0x3AF2 = 15090

LM_{Result} = 0.4605

$I_{CMeasure}$ = 2*2 mA*0.4605 = 1.842 mA

$C_{Measure}$ = 1,842 mA/200 V/s = 9.21 µF

4.8.2.12 Line Capacitance Measurements Ring and Tip to GND

The voltage ramp can be applied to either line, whereas the other line is set to high impedance by setting bits HIR and HIT in register BCR1 accordingly. That way capacitance measurements from Ring and Tip to GND may be accomplished.

Because of one line being high impedance, the actual line current will be twice the calculated one (multiplication by a factor of 2 necessary).

4.8.2.13 Foreign- and Ring Voltage Measurements

The DuSLIC supports two user-programmable input/output pins (IO3, IO4) which can be used for measuring external voltages. If the pins IO3 and/or IO4 are led properly over a voltage divider to the Ring- and Tip wire, foreign voltages from external voltage sources supplied to the lines can be measured on either pin, even a differential measurement will be supported (IO4-IO3). The selection of which input information shall be taken for the measurement is done via bits LM-SEL[3:0] in configuration register LMCR2 (**Table 36**).

Table 36 Measurement Input Selection

LM-SEL[3:0] in register LMCR2	Measurement Input
1010	Voltage on IO3
1011	Voltage on IO4
1111	Voltage IO4 – IO3

The measurement is accomplished by the DC levelmeter function.

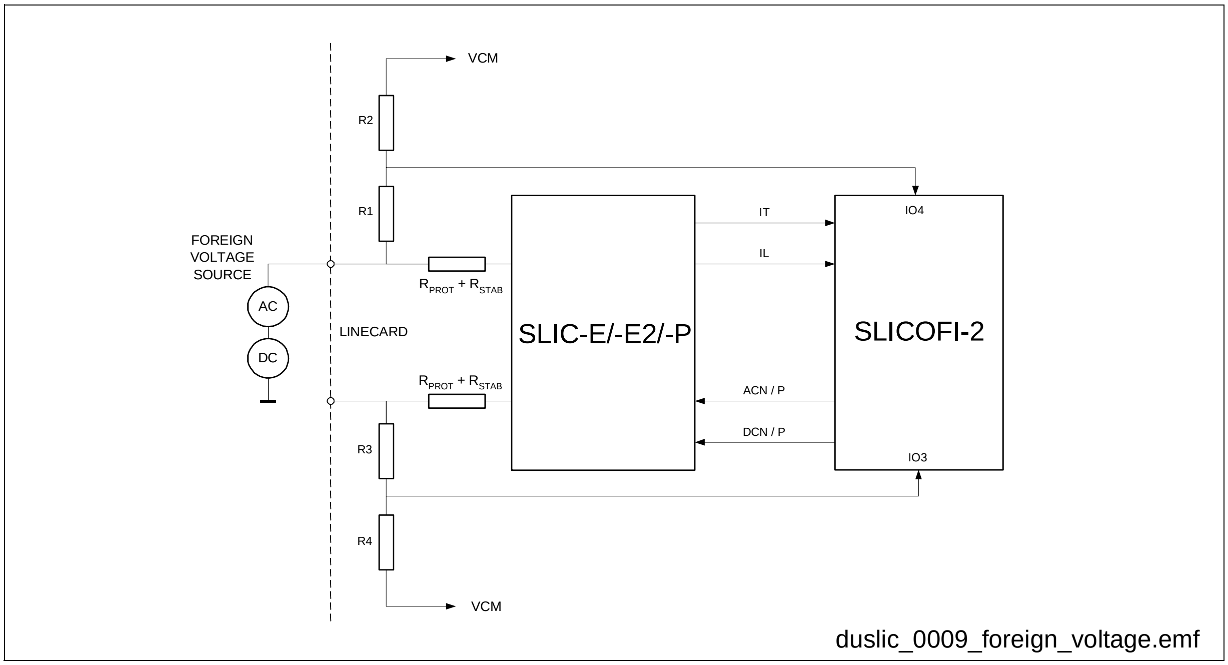

VCM
R2
R1
IT
IO4
IL
FOREIGN VOLTAGE SOURCE
R_PROT + R_STAB
AC
LINECARD
SLIC-E/-E2/-P
SLICOFI-2
DC
R_PROT + R_STAB
ACN / P
DCN / P
R3
IO3
R4
VCM
duslic_0009_foreign_voltage.emf

Figure 52 Foreign Voltage Measurement Principle

Figure 52 shows the connection and external resistors used for supporting foreign voltage measurements at the Ring and Tip lines.

Since the pins IO3 and IO4 support analog input functionality and are limited to a certain voltage range of V_{VCM} ± 1.0 V (typ. 1.5 V ± 1.0 V), the values for the voltage divider has to be determined according to following conditions:

- Maximum level of the expected foreign voltages
- Voltage range of IO3 and IO4 = V_{VCM} ± 1.0 V

The voltage on IO3 or IO4 is measured with a reference to VCM. Hence an input voltage of V_{VCM} on either input pin would result into zero output value. Whereas a voltage of V_{VCM} + 1 V would result into the negative full scale value, V_{VCM} – 1 V would result into the positive full scale value respectively. For that reason the voltage divider has to be referenced to VCM. The unknown foreign voltage $V_{FOREIGN}$ can be calculated as:

$$V_{FOREIGN} = V_{INPUT} \times \frac{R1 + R2}{R2} + V_{VCM}$$

$V_{INPUT} = V_{IOx} - V_{VCM}$ (refer to **Table 31**)

V_{IOx} = Voltage on pins IOx (e.g. pins IO3, IO4)

The resistor directly connected to either Ring or Tip (R1, R3) should be high enough so that the loop impedance will not be affected by them. Several MΩ s, e.g. 10 MΩ would be a reasonable value. The following example illustrates the potential voltage range that can be measured by chosing the values as:

- R1 = R3 = 10 MΩ
- R2 = R4 = 47 kΩ

The values given for the maximum and minimum voltage levels are:

- $V_{VCM} = 1.5$ V
- $V_{INPUT,max} = 1$ V $\rightarrow V_{IOX,max} = 2.5$ V
- $V_{INPUT,min} = -1$ V $\rightarrow V_{IOX,min} = 0.5$ V

$$V_{FOREIGN,max} = V_{INPUT,max} \times \frac{R1 + R2}{R2} + V_{VCM} = 215\text{ V}$$

$$V_{FOREIGN,min} = V_{INPUT,min} \times \frac{R1 + R2}{R2} + V_{VCM} = -212\text{ V}$$

The voltage range would span from 215 V to – 212 V.

In order to measure small input voltages on IO3/IO4 more accurately the user might consider to enable the integration function (see **Figure 45**) by setting bit LM-EN in register LMCR1 to 1.

In case of measuring the ring voltage supplied to either Ring or Tip or even both (balanced ringing) pins via IO3 and IO4, the rectifier can be enabled by setting bit LM-RECT in register LMCR2 to 1.

4.9 Signal Path and Test Loops

The following figures show the main AC and DC signal path and the integrated analog and digital loops of DuSLIC-E/-E2/-P, DuSLIC-S and DuSLIC-S2.

Please note the interconnections between the AC and DC pictures of the respective chip set.

4.9.1 Test Loops DuSLIC-E/-E2/-P

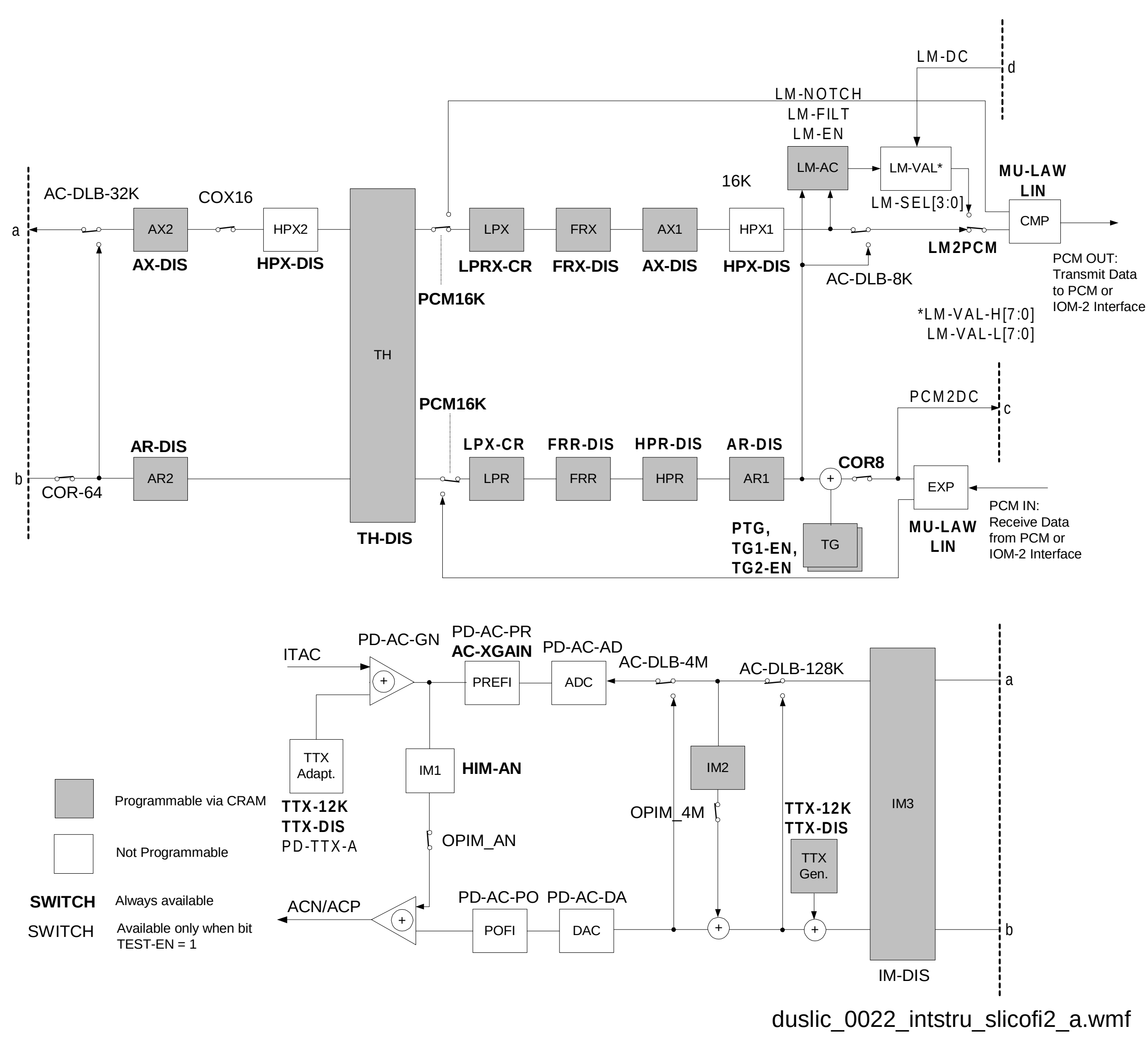

LM-DC
d
LM-NOTCH
LM-FILT
LM-EN
LM-AC
LM-VAL*
16K
MU-LAW
LIN
LM-SEL[3:0]
CMP
AC-DLB-32K
COX16
a
AX2
HPX2
TH
LPX
FRX
AX1
HPX1
LM2PCM
AX-DIS
HPX-DIS
LPRX-CR
FRX-DIS
AX-DIS
HPX-DIS
AC-DLB-8K
PCM OUT:
Transmit Data
to PCM or
IOM-2 Interface
PCM16K
*LM-VAL-H[7:0]
LM-VAL-L[7:0]
PCM16K
PCM2DC
c
AR-DIS
LPX-CR
FRR-DIS
HPR-DIS
AR-DIS
COR8
b
AR2
LPR
FRR
HPR
AR1
+
EXP
COR-64
PCM IN:
Receive Data
from PCM or
IOM-2 Interface
TH-DIS
PTG,
TG1-EN,
TG2-EN
TG
MU-LAW
LIN
ITAC
PD-AC-GN
PD-AC-PR
AC-XGAIN
PD-AC-AD
AC-DLB-4M
AC-DLB-128K
+
PREFI
ADC
a
TTX
Adapt.
IM1
HIM-AN
IM2
IM3
Programmable via CRAM
TTX-12K
TTX-DIS
PD-TTX-A
OPIM_AN
OPIM_4M
TTX-12K
TTX-DIS
Not Programmable
TTX
Gen.
SWITCH
Always available
ACN/ACP
PD-AC-PO
PD-AC-DA
SWITCH
Available only when bit
TEST-EN = 1
+
POFI
DAC
+
+
b
IM-DIS
duslic_0022_intstru_slicofi2_a.wmf

Figure 53 AC Test Loops DuSLIC-E/-E2/-P

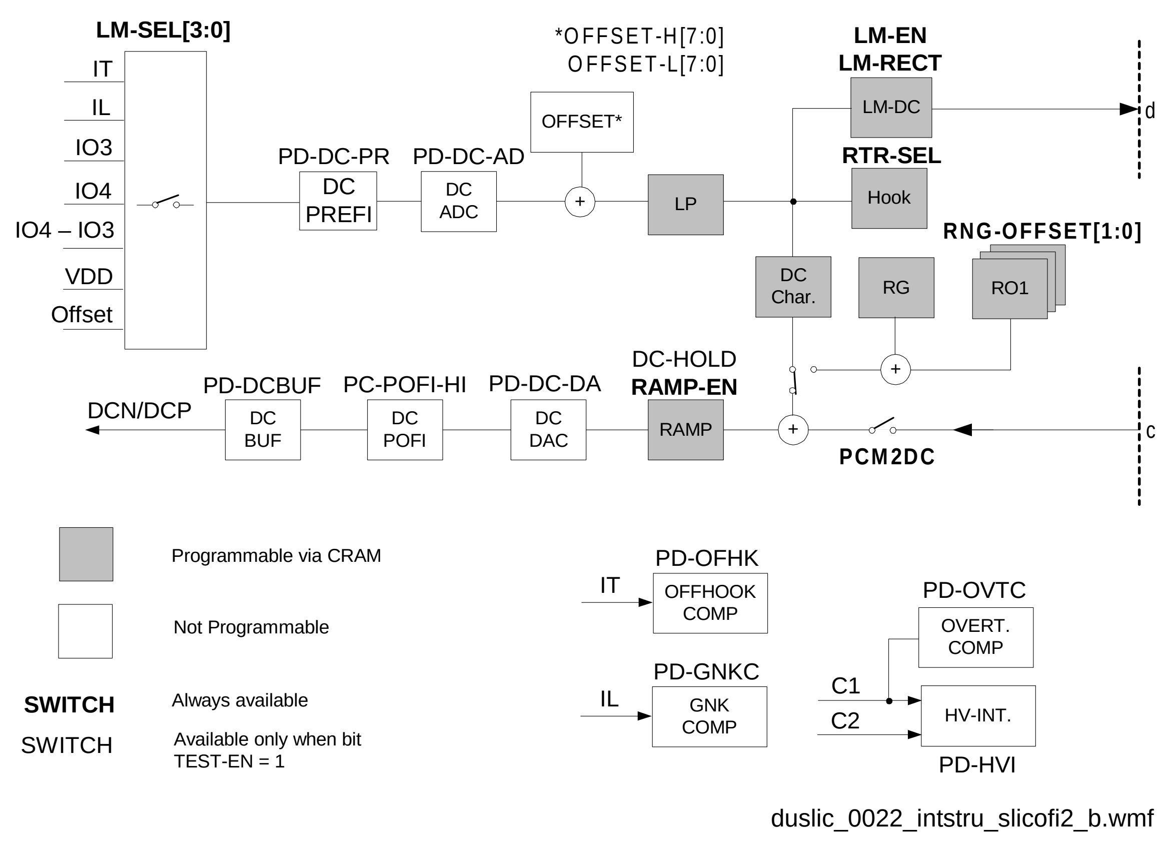
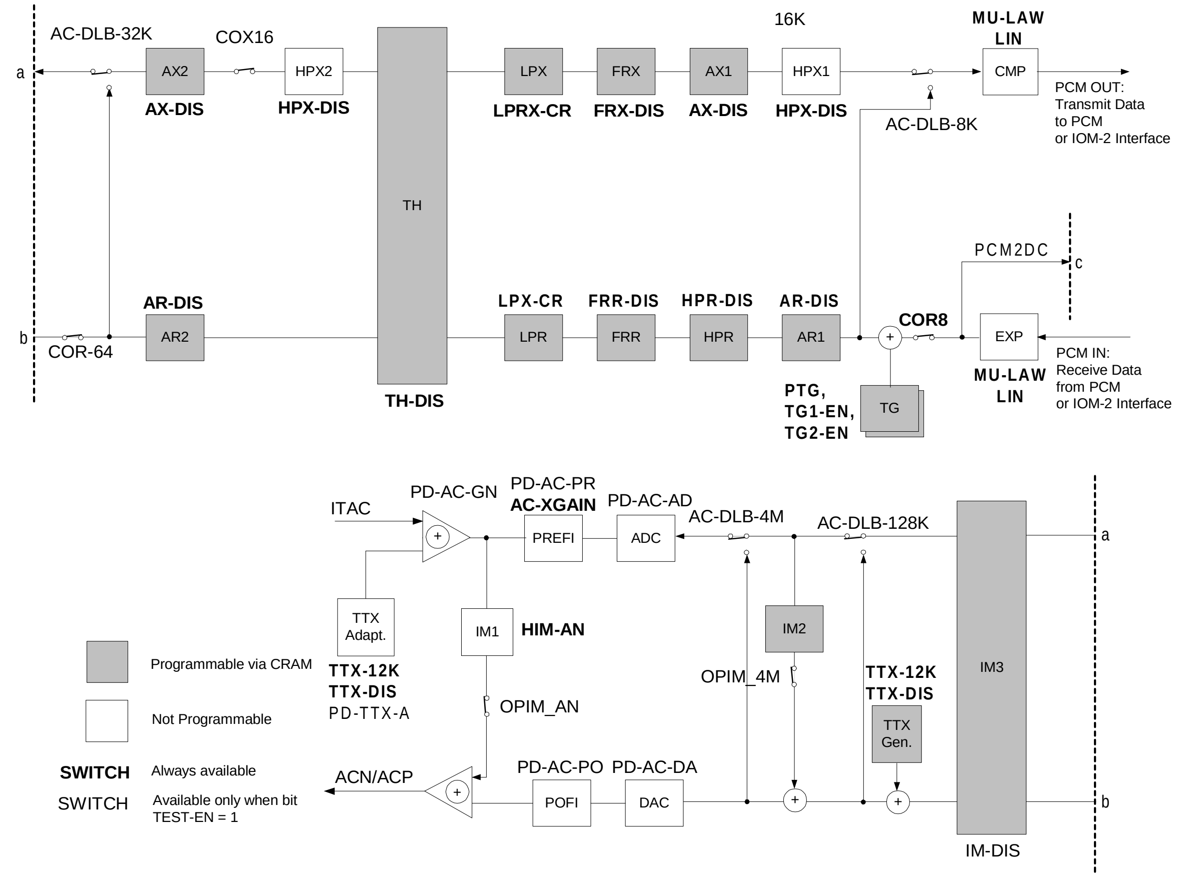

LM-SEL[3:0]
IT
IL
IO3
IO4
IO4 – IO3
VDD
Offset
PD-DC-PR
DC PREFI
PD-DC-AD
DC ADC
*OFFSET-H[7:0]
OFFSET-L[7:0]
OFFSET*
+
LP
LM-EN
LM-RECT
LM-DC
d
RTR-SEL
Hook
RNG-OFFSET[1:0]
DC Char.
RG
RO1
+
DC-HOLD
RAMP-EN
PD-DCBUF
PC-POFI-HI
PD-DC-DA
DCN/DCP
DC BUF
DC POFI
DC DAC
RAMP
+
PCM2DC
c
Programmable via CRAM
Not Programmable
SWITCH
Always available
SWITCH
Available only when bit TEST-EN = 1
PD-OFHK
IT
OFFHOOK COMP
PD-GNKC
IL
GNK COMP
PD-OVTC
OVERT. COMP
C1
C2
HV-INT.
PD-HVI
duslic_0022_intstru_slicofi2_b.wmf

Figure 54 DC Test Loops DuSLIC-E/-E2/-P

4.9.2 Test Loops DuSLIC-S/-S2

The AC test loops for DuSLIC-S (**Figure 55**) and DuSLIC-S2 (**Figure 56**) are different since Teletax (TTX) is not available with SLICOFI-2S2. The DC test loops are identical.


AC-DLB-32K
COX16
a
AX2
AX-DIS
HPX2
HPX-DIS
TH
LPX
LPRX-CR
FRX
FRX-DIS
AX1
AX-DIS
16K
HPX1
HPX-DIS
AC-DLB-8K
MU-LAW
LIN
CMP
PCM OUT:
Transmit Data
to PCM
or IOM-2 Interface
PCM2DC
c
b
COR-64
AR-DIS
AR2
TH-DIS
LPX-CR
LPR
FRR-DIS
FRR
HPR-DIS
HPR
AR-DIS
AR1
COR8
EXP
PCM IN:
Receive Data
from PCM
or IOM-2 Interface
MU-LAW
LIN
PTG,
TG1-EN,
TG2-EN
TG
ITAC
PD-AC-GN
PD-AC-PR
AC-XGAIN
PREFI
PD-AC-AD
ADC
AC-DLB-4M
AC-DLB-128K
a
TTX
Adapt.
IM1
HIM-AN
IM2
IM3
OPIM_4M
TTX-12K
TTX-DIS
PD-TTX-A
OPIM_AN
TTX-12K
TTX-DIS
TTX
Gen.
Programmable via CRAM
Not Programmable
SWITCH
Always available
SWITCH
Available only when bit
TEST-EN = 1
ACN/ACP
PD-AC-PO
POFI
PD-AC-DA
DAC
b
IM-DIS

duslic_0023_intstru_slicofi2S_c.wmf

Figure 55 AC Test Loops DuSLIC-S

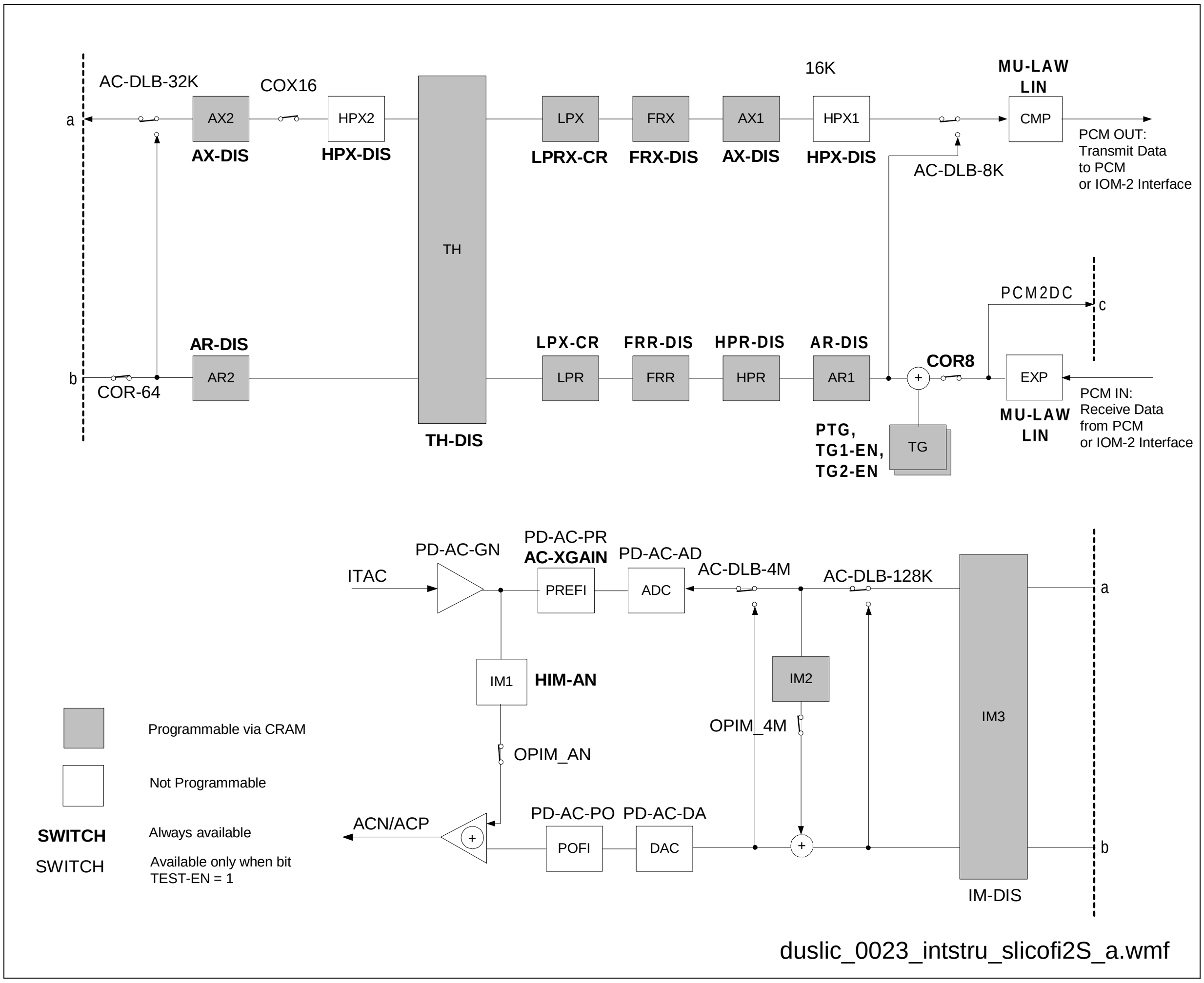

a
AC-DLB-32K
COX16
AX2
HPX2
AX-DIS
HPX-DIS
TH
LPX
FRX
AX1
HPX1
16K
MU-LAW
LIN
CMP
LPRX-CR
FRX-DIS
AX-DIS
HPX-DIS
AC-DLB-8K
PCM OUT:
Transmit Data
to PCM
or IOM-2 Interface
PCM2DC
c
b
COR-64
AR-DIS
AR2
LPX-CR
FRR-DIS
HPR-DIS
AR-DIS
LPR
FRR
HPR
AR1
COR8
+
EXP
PCM IN:
Receive Data
from PCM
or IOM-2 Interface
MU-LAW
LIN
TH-DIS
PTG,
TG1-EN,
TG2-EN
TG
ITAC
PD-AC-GN
PD-AC-PR
AC-XGAIN
PREFI
PD-AC-AD
ADC
AC-DLB-4M
AC-DLB-128K
a
IM1
HIM-AN
IM2
IM3
OPIM_AN
OPIM_4M
Programmable via CRAM
Not Programmable
SWITCH
Always available
SWITCH
Available only when bit
TEST-EN = 1
ACN/ACP
+
PD-AC-PO
POFI
PD-AC-DA
DAC
+
b
IM-DIS
duslic_0023_intstru_slicofi2S_a.wmf

Figure 56 AC Test Loops DuSLIC-S2

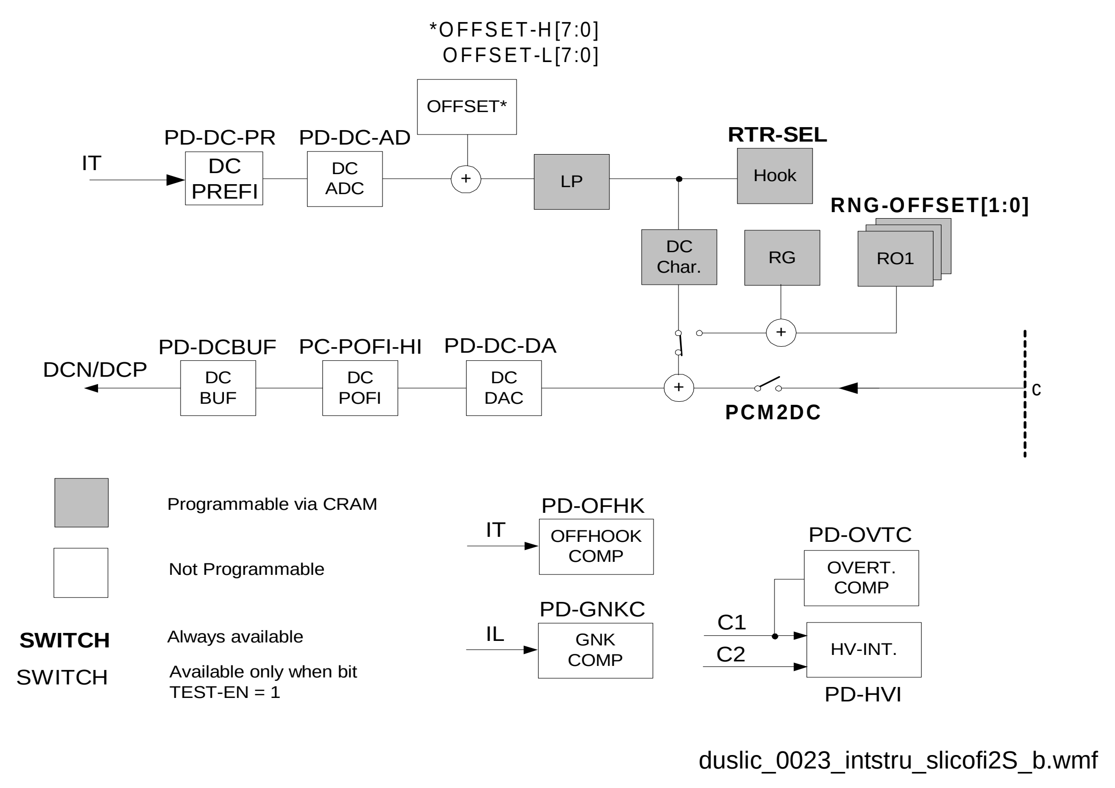

*OFFSET-H[7:0]
OFFSET-L[7:0]
OFFSET*
PD-DC-PR
PD-DC-AD
IT
DC PREFI
DC ADC
+
LP
RTR-SEL
Hook
RNG-OFFSET[1:0]
DC Char.
RG
RO1
+
PD-DCBUF
PC-POFI-HI
PD-DC-DA
DCN/DCP
DC BUF
DC POFI
DC DAC
+
PCM2DC
C
Programmable via CRAM
Not Programmable
SWITCH
Always available
SWITCH
Available only when bit TEST-EN = 1
PD-OFHK
IT
OFFHOOK COMP
PD-GNKC
IL
GNK COMP
PD-OVTC
OVERT. COMP
C1
C2
HV-INT.
PD-HVI
duslic_0023_intstru_slicofi2S_b.wmf

Figure 57 DC Test Loops DuSLIC-S/-S2

4.10 Caller ID Buffer Handling of SLICOFI-2

This chapter intends to describe the handling of the caller ID buffer and the corresponding handshake bits in the interrupt registers.

Programming Sequence

In order to send a caller ID information over the telephone line the following sequence should be programmed between the first and the second ring burst. The initialization part of the coefficients in the POP registers 43h to 4Ah must be done prior to that sequence.

1. Enable the extended feature DSP in register XCR (EDSP-EN = 1)
2. Enable the caller ID sender feature in register BCR5 (CIS-EN = 1)
3. Wait for an interrupt.
4. Read out all 4 interrupt registers to serve the interrupt and check the CIS-REQ bit.
5. If this bit is set, send at least BRS + 2 bytes (see POP register CIS-BRS) of caller ID data but not more than 48 bytes to the caller ID sender buffer register CIS-DAT.
6. Wait for the next interrupt and check again the CIS-REQ bit.
7. If this bit is set, send the next data to the caller ID-data buffer but not more than (48 – BRS) bytes. CIS-REQ bit gets reset to zero, if the data buffer is filled again above the Caller ID sender buffer request size (BRS).
8. Repeat steps 6 and 7 as long as there is data to be sent.
9. Right after sending the last data byte to the caller ID sender buffer, set the bit CIS-AUTO to 1 and the bit CIS-EN to 0. After processing the last bit the caller ID sender will stop automatically and set the CIS-ACT bit in INTREG4 to zero. No more CIS interrupt will be generated until the caller ID sender will be enabled again (interrupt bits: CIS-BOF, CIS-BUF and CIS-REQ).

The end of the CID transmission can also be controlled by not setting CIS-AUTO and leaving CIS-EN at one. If the caller ID buffer gets empty, an interrupt is generated to indicate buffer underflow (CIS-BUF). If CIS-BUF is set, set CIS-EN to zero with at least 1 ms delay, in order to allow to send the last bit of caller ID data.

In case of errors in the handling of the CID data buffer CIS-BUF (buffer underflow) and CIS-BOF (buffer overflow) indicate these errors. Please stop CID transmission in any of these cases since unpredictable results may occur.

Note: CID data will be sent out LSB first

If CIS-FRM is set to one: seizure and mark bits are generated automatically (according to the settings of CIS-SEIZ-H/L and CIS-MARK-H/L) as well as start and stop bits for every byte

5 Interfaces

The DuSLIC connects the analog subscriber to the digital switching network by two different types of digital interfaces to allow for the highest degree of flexibility in different applications:

- PCM interface combined with a serial microcontroller interface
- IOM-2 interface.

The PCM/$\overline{\text{IOM-2}}$ pin selects the interface mode.

PCM/$\overline{\text{IOM-2}}$ = 0: The IOM-2 interface is selected.
PCM/$\overline{\text{IOM-2}}$ = 1: The PCM/µC interface is selected.

The analog TIP/RING interface connects the DuSLIC to the subscriber.

5.1 PCM Interface with a Serial Microcontroller Interface

In PCM/µC interface mode, voice and control data are separated and handled by different pins of the *SLICOFI-2x*. Voice data are transferred via the PCM highways while control data are using the microcontroller interface.

5.1.1 PCM Interface

The serial PCM interface is used to transfer A-law or µ-law-compressed voice data. In test mode, the PCM interface can also transfer linear data. The eight pins of the PCM interface are used as follows (two PCM highways):

PCLK:	PCM Clock, 128 kHz to 8192 kHz
FSC:	Frame Synchronization Clock, 8 kHz
DRA:	Receive Data Input for PCM Highway A
DRB:	Receive Data Input for PCM Highway B
DXA:	Transmit Data Output for PCM Highway A
DXB:	Transmit Data Output for PCM Highway B
$\overline{\text{TCA}}$:	Transmit Control Output for PCM Highway A, Active low during transmission
$\overline{\text{TCB}}$:	Transmit Control Output for PCM Highway B, Active low during transmission

The FSC pulse identifies the beginning of a receive and transmit frame for both channels. The PCLK clock signal synchronizes the data transfer on the DXA (DXB) and DRA (DRB) lines. On all channels, bytes are serialized with MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to buffer the contents of the received data on DRA (DRB). If double clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to buffer the contents of the data line DRA (DRB).

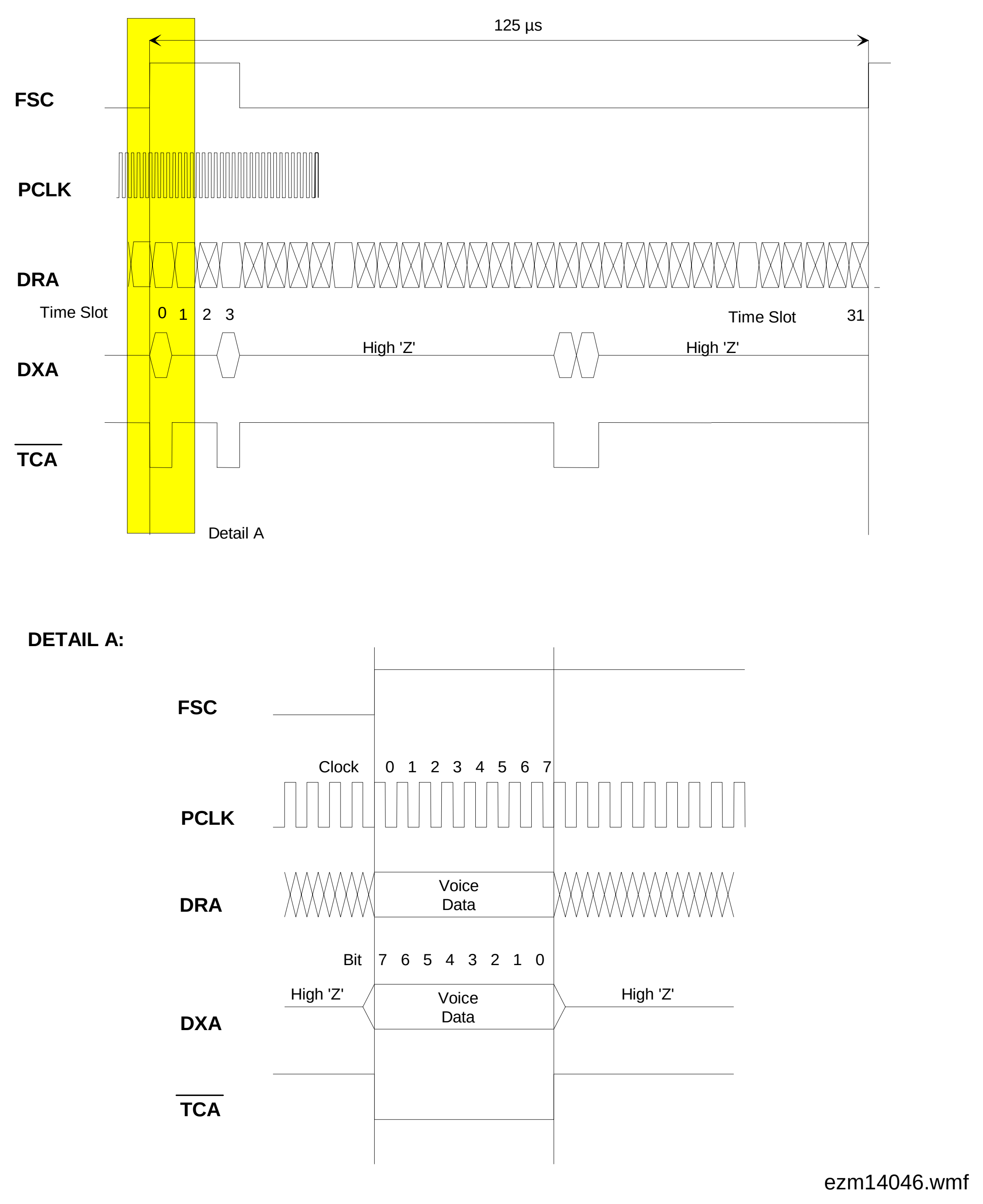

125 µs
FSC
PCLK
DRA
Time Slot
0 1 2 3
Time Slot
31
DXA
High 'Z'
High 'Z'
TCA
Detail A
DETAIL A:
FSC
Clock
0 1 2 3 4 5 6 7
PCLK
DRA
Voice Data
Bit
7 6 5 4 3 2 1 0
High 'Z'
Voice Data
High 'Z'
DXA
TCA
ezm14046.wmf

Figure 58 General PCM Interface Timing

The data rate of the interface can vary from 2*128 kbit/s to 2*8192 kbit/s (two highways). A frame may consist of up to 128 time slots of 8 bits each. The time slot and PCM highway assignment for each DuSLIC channel can be programmed. Receive and transmit time slots can also be programmed individually.

When DuSLIC is transmitting data on DXA (DXB), pin $\overline{\text{TCA}}$ ($\overline{\text{TCB}}$) is activated to control an external driving device.

The DRA/B and DXA/B pins may be connected to form a bidirectional data pin for special purposes, e.g., for the Serial Interface Port (SIP) with the Subscriber Line Data (SLD) bus. The SLD approach provides a common interface for analog or digital per-line components. For more details, please see the “ICs for Communications”1) User’s Manual available from Infineon Technologies on request.

Table 37 shows PCM interface examples; other frequencies (e.g., 1536 kHz) are also possible.

Table 37 *SLICOFI-2x* PCM Interface Configuration

Clock Rate PCLK [kHz]	**Single/Double Clock** [1/2]	**Time Slots** [per highway]	**Data Rate** [kbit/s per highway]
128	1	2	128
256	2	2	128
256	1	4	256
512	2	4	256
512	1	8	512
768	2	6	384
768	1	12	768
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
f	1	f/64	f
f	2	f/128	f/2

Valid PCLK clock rates are: $f = n \times 64$ kHz ($2 \leq n \leq 128$)

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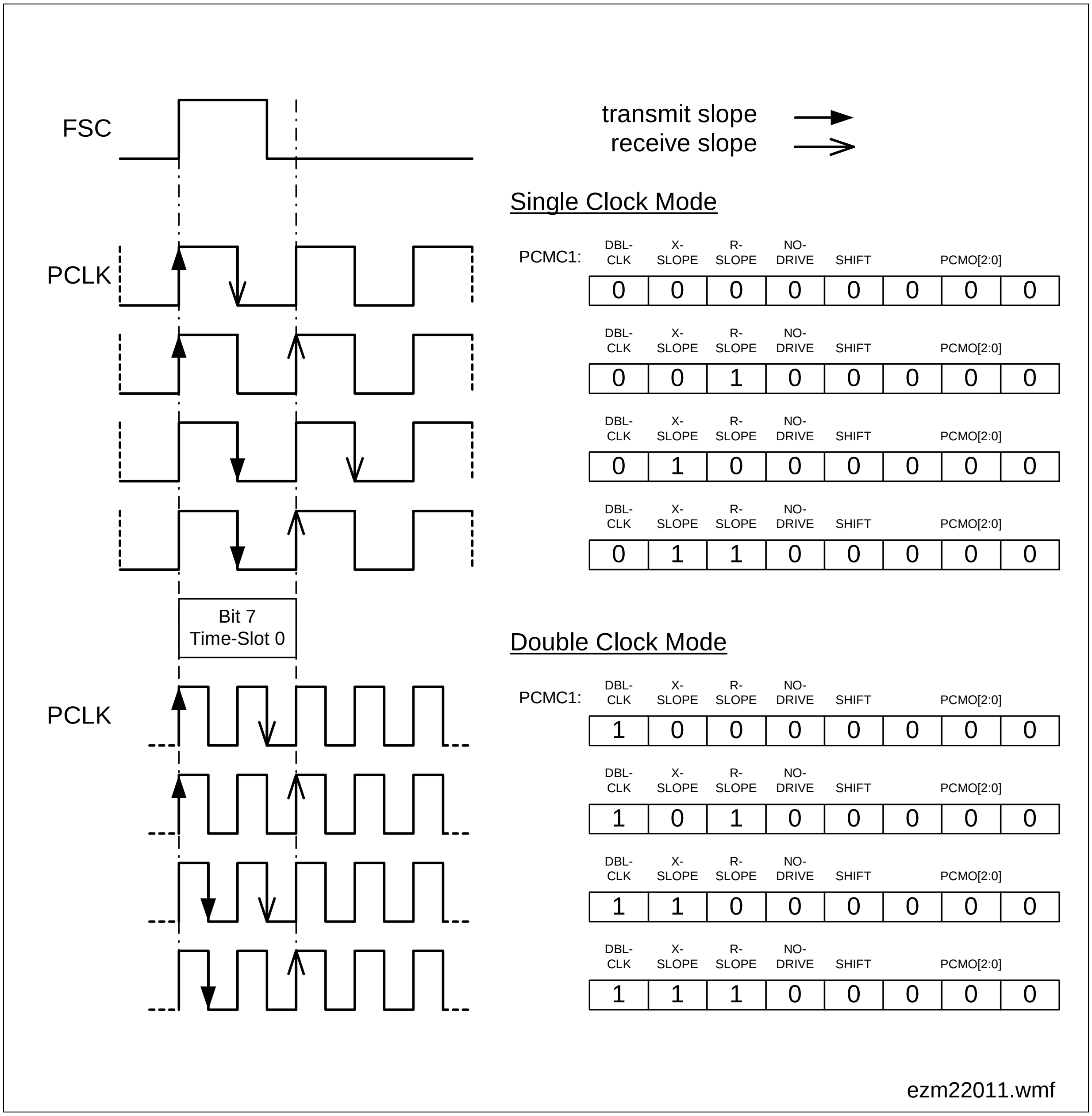
1) Ordering No. B115-H6377-X-X-7600, published by Infineon Technologies.


FSC
transmit slope
receive slope
PCLK
Bit 7
Time-Slot 0
PCLK
Single Clock Mode
Double Clock Mode
PCMC1:
ezm22011.wmf

Single Clock Mode

DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE	SHIFT	PCMO[2:0]		
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0

Double Clock Mode

DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE	SHIFT	PCMO[2:0]		
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0

Figure 59 Setting of Slopes in Register PCMC1

5.1.2 Control of the Active PCM Channels

The *SLICOFI-2x* offers additional functionality on the PCM interface including three-party conferencing and a 16 kHz sample rate. Five configuration bits control, together with the PCM configuration registers, the activation of the PCM transmit channels. For details of the different functions see **Chapter 6.2**.

Table 38 gives an overview of the data transmission configuration of the PCM channels.

X1L is used only when linear data are transmitted. In this case the time slot for X1 is defined by the number X1-TS from the PCMX1 register. The time slot for X1L is defined by the number X1-TS + 1.

Table 38 Active PCM Channel Configuration Bits

Control Bits					Transmit PCM Channel				
PCMX-EN	**CONF-EN**	**CONFX-EN**	**PCM16K**	**LIN**	**X1**	**X1L**	**X2**	**X3**	**X4**
0	0	0	–	–	–	–	–	–	–
1	0	0	0	0	PCM	–	–	–	–
1	0	0	0	1	HB	LB	–	–	–
0	1	0	–	–	–	–	PCM	PCM	–
1	1	0	0	0	PCM	–	PCM	PCM	–
1	1	0	0	1	HB	LB	PCM	PCM	–
0	0	1	–	–	–	–	PCM	PCM	PCM
1	0	1	0	0	PCM	–	PCM	PCM	PCM
1	0	1	0	1	HB	LB	PCM	PCM	PCM
0	1	1	–	–	–	–	PCM	PCM	PCM
1	1	1	0	0	PCM	–	PCM	PCM	PCM
1	1	1	0	1	HB	LB	PCM	PCM	PCM
1	–	–	1	0	DS1	–	–	DS2	–
1	–	–	1	1	HB1	–	LB1	HB2	LB2

Note: PCM means PCM-coded data (A-law / µ-law)
HB1, HB2, LB1, LB2 indicate the high byte, low byte of linearly transmitted data for an 8 kHz (16 kHz) sample rate.
Modes in rows with gray background are for testing purposes only.

5.1.3 Serial Microcontroller Interface

The microcontroller interface consists of four lines: $\overline{\text{CS}}$, DCLK, DIN and DOUT.

$\overline{\text{CS}}$	A synchronization signal starting a read or write access to *SLICOFI-2x*.
DCLK	A clock signal (up to 8.192 MHz) supplied to *SLICOFI-2x*.
DIN	Data input carries data from the master device to the *SLICOFI-2x*.
DOUT	Data output carries data from *SLICOFI-2x* to a master device.

There are two different command types. Reset commands have just one byte. Read/write commands have two command bytes with the address offset information located in the second byte.

A write command consists of two command bytes and the following data bytes. The first command byte determines whether the command is read or write, how the command field is to be used, and which DuSLIC channel (A or B) is written. The second command byte contains the address offset.

A read command consists of two command bytes written to DIN. After the second command byte is applied to DIN, a dump-byte consisting of '1's is written to DOUT. Data transfer starts with the first byte following the 'dump-byte'.

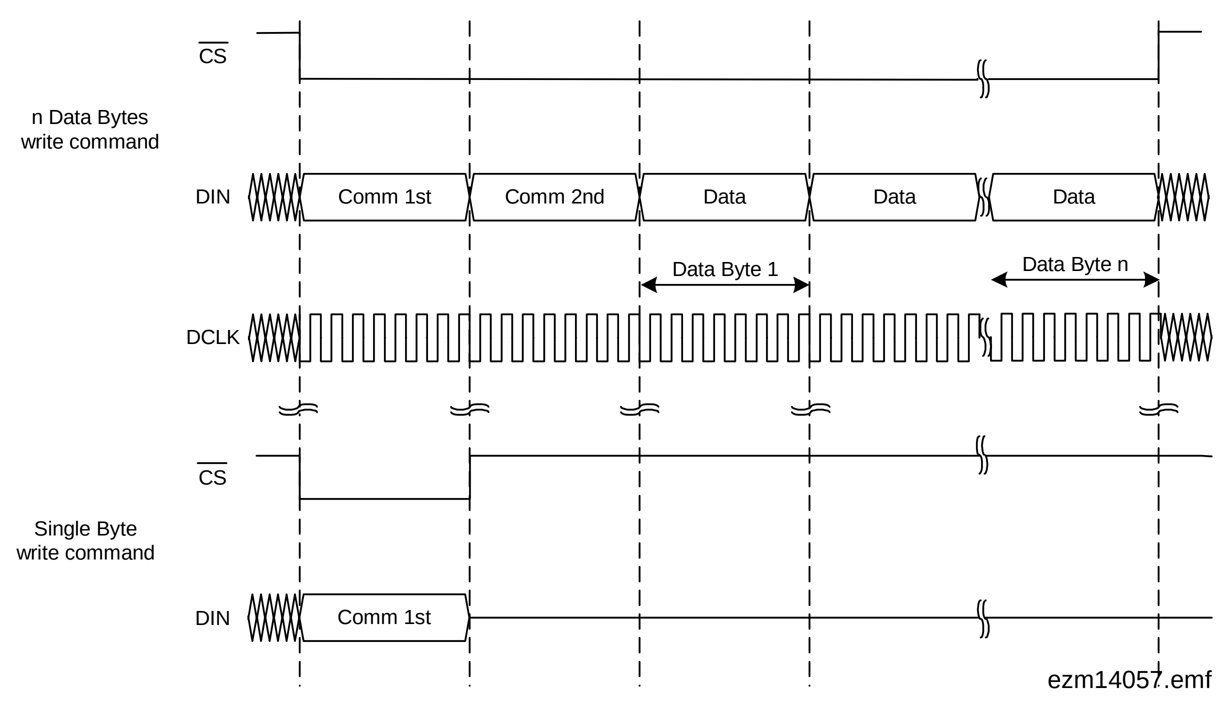

CS
n Data Bytes
write command
DIN
Comm 1st
Comm 2nd
Data
Data
Data
Data Byte 1
Data Byte n
DCLK
CS
Single Byte
write command
DIN
Comm 1st
ezm14057.emf

Figure 60 Serial Microcontroller Interface Write Access[1]

---

[1] for n data bytes and single byte command

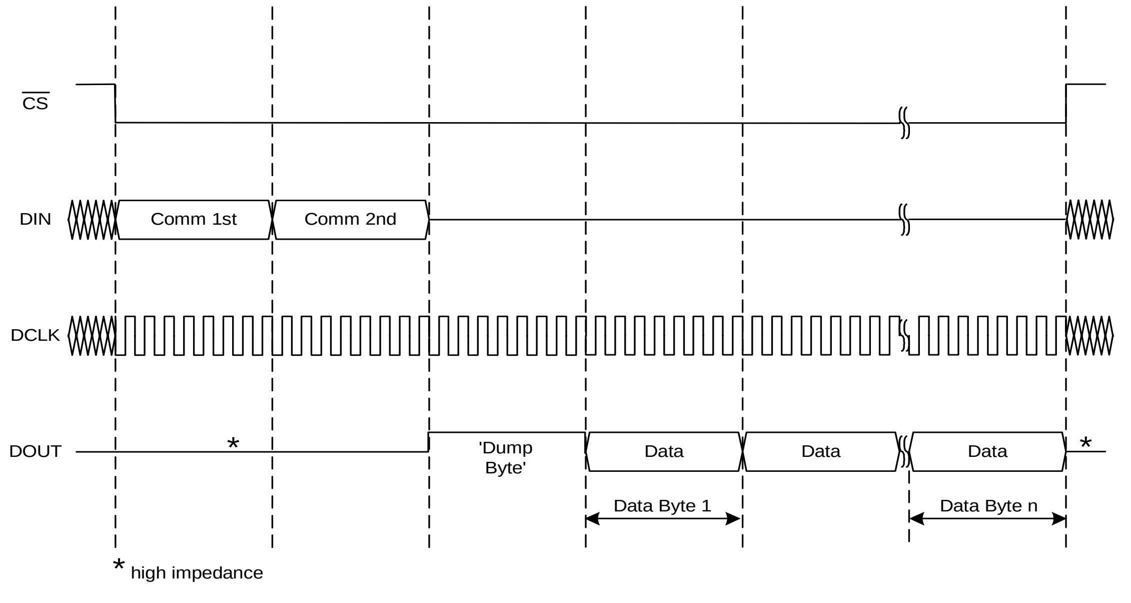

CS
DIN
DCLK
DOUT
Comm 1st
Comm 2nd
*
'Dump Byte'
Data
Data
Data
*
Data Byte 1
Data Byte n
* high impedance
ezm14058.wmf

Figure 61 Serial Microcontroller Interface Read Access

Programming the Microcontroller Interface Without Clocks at FSC, MCLK, PCLK

The *SLICOFI-2x* can also be programmed via the µC interface without any clocks connected to the FSC, MCLK, PCLK pins. This can be useful in Power Down modes when further power saving on system level is necessary. In this case a data clock of up to 1.024 MHz can be used on pin DCLK.

Since the *SLICOFI-2x* will leave the basic reset routine only if clocks at the FSC, MCLK and PCLK pins are applied, it is not possible to program the *SLICOFI-2x* without any clocks at these pins directly after the hardware reset or power on reset.

5.2 The IOM-2 Interface

IOM-2 defines an industry-standard serial bus for interconnecting telecommunication ICs for a broad range of applications - typically ISDN-based applications.

The IOM-2 bus provides a symmetrical full-duplex communication link containing data, control/programming and status channels. Providing data, control and status information via a serial channel reduces pin count and cost by simplifying the line card layout.

The IOM-2 Interface consists of two data lines and two clock lines as follows:

DU:	Data Upstream carries data from the *SLICOFI-2x* to a master device.
DD:	Data Downstream carries data from the master device to the *SLICOFI-2x*.
FSC:	A Frame Synchronization Signal (8 kHz) supplied to *SLICOFI-2x*.
DCL:	A Data Clock Signal (2048 kHz or 4096 kHz) supplied to *SLICOFI-2x*.

SLICOFI-2x handles data as described in the IOM-2 specification[1] for analog devices.

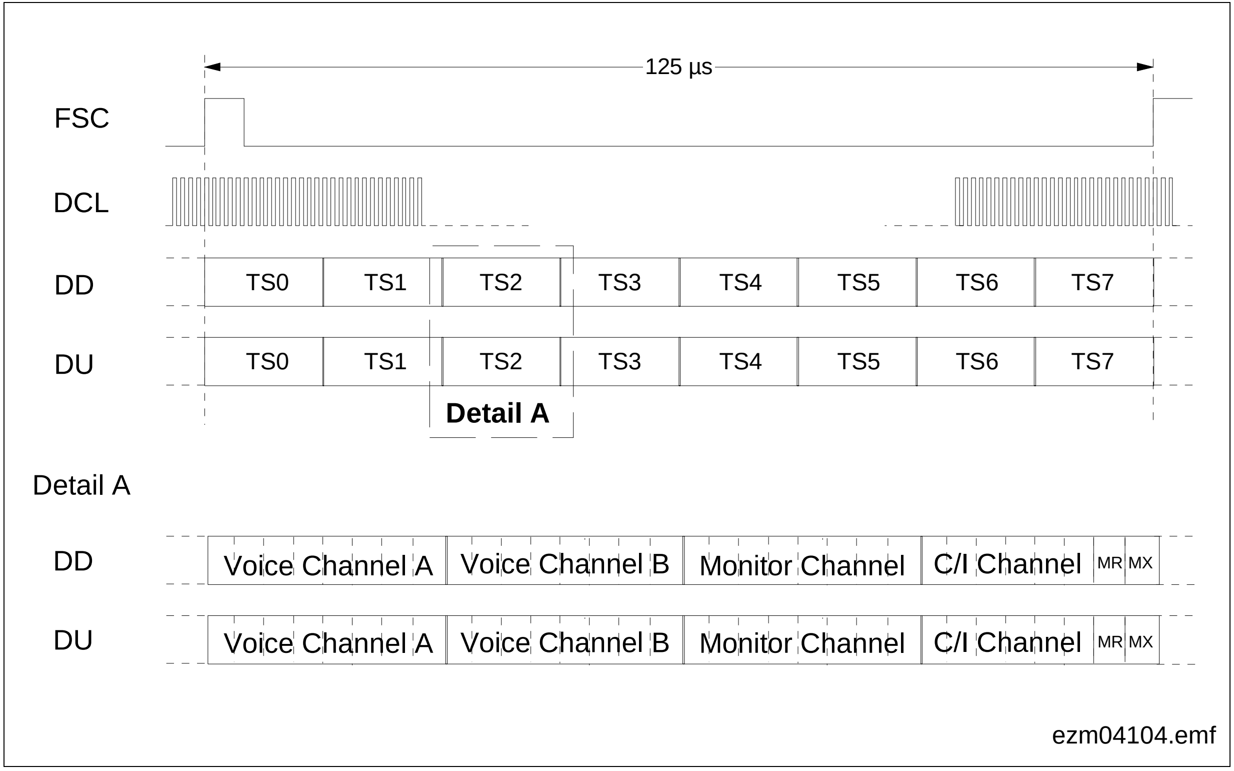

125 µs
FSC
DCL
DD
TS0
TS1
TS2
TS3
TS4
TS5
TS6
TS7
DU
TS0
TS1
TS2
TS3
TS4
TS5
TS6
TS7
Detail A
Detail A
DD
Voice Channel A
Voice Channel B
Monitor Channel
C/I Channel
MR
MX
DU
Voice Channel A
Voice Channel B
Monitor Channel
C/I Channel
MR
MX
ezm04104.emf

Figure 62 IOM-2 Int. Timing for up to 16 Voice Channels (Per 8-kHz Frame)

---

[1] Available on request from Infineon Technologies.

The information is multiplexed into frames, which are transmitted at an 8-kHz rate. The frames are subdivided into 8 sub-frames, with one sub-frame dedicated to each transceiver or pair of codecs (in this case, two *SLICOFI-2x* channels). The sub-frames provide channels for data, programming and status information for a single transceiver or codec pair.

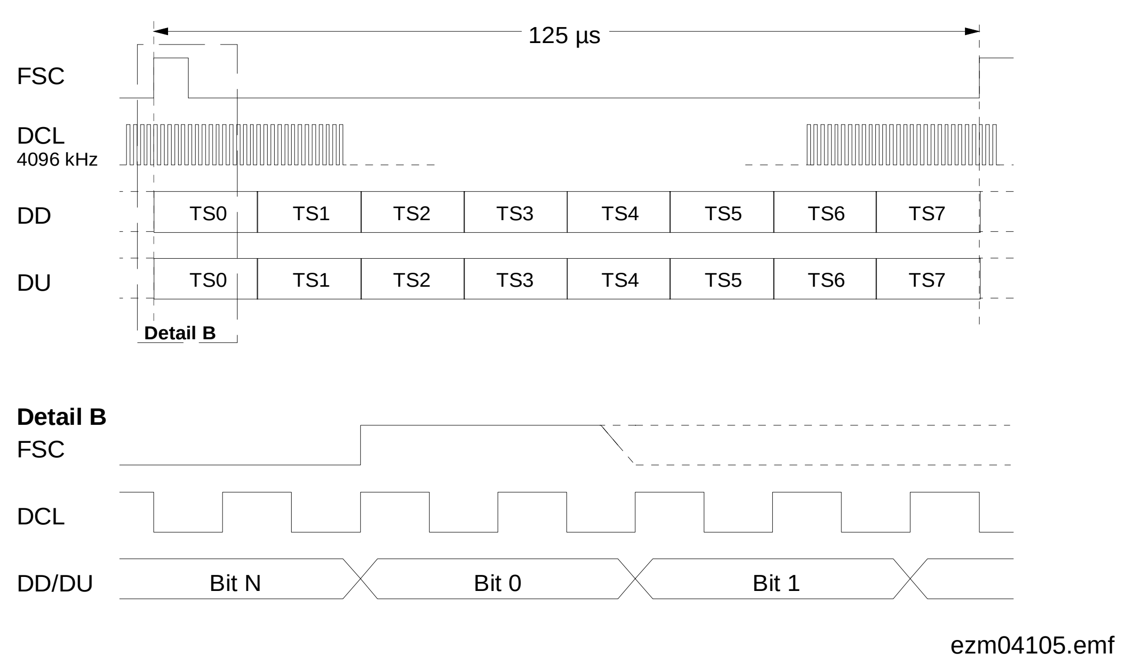

125 µs
FSC
DCL
4096 kHz
DD
DU
TS0
TS1
TS2
TS3
TS4
TS5
TS6
TS7
TS0
TS1
TS2
TS3
TS4
TS5
TS6
TS7
Detail B
Detail B
FSC
DCL
DD/DU
Bit N
Bit 0
Bit 1
ezm04105.emf

Figure 63 IOM-2 Interface Timing (DCL = 4096 kHz, Per 8-kHz Frame)

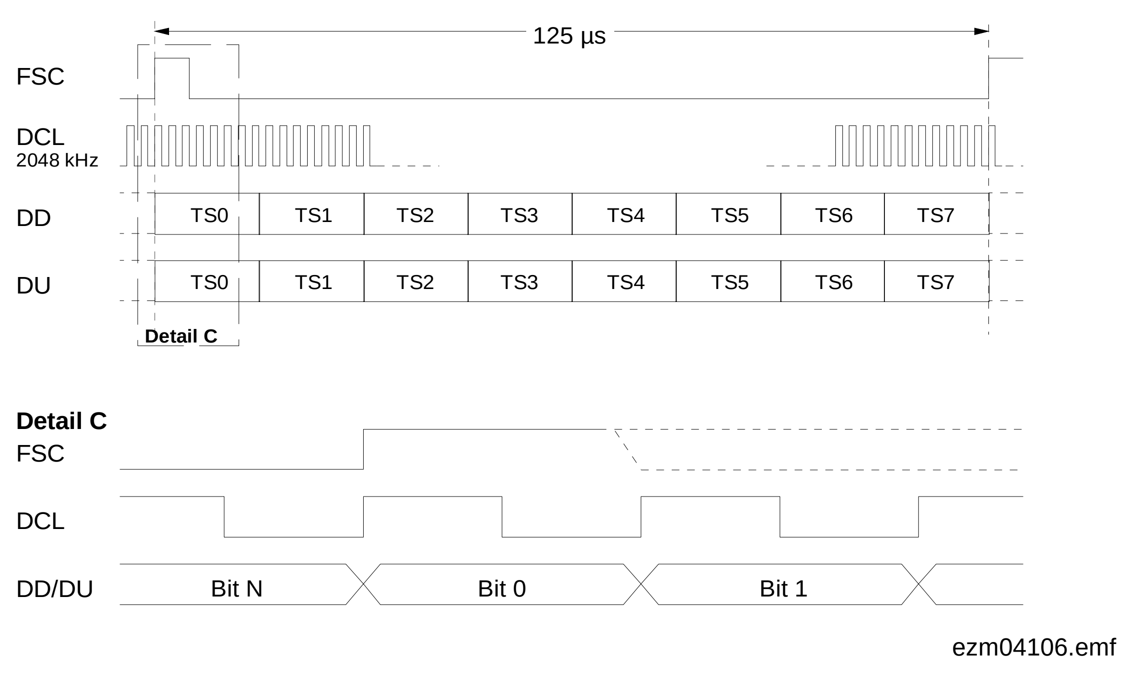

125 µs
FSC
DCL
2048 kHz
DD
TS0
TS1
TS2
TS3
TS4
TS5
TS6
TS7
DU
TS0
TS1
TS2
TS3
TS4
TS5
TS6
TS7
Detail C
Detail C
FSC
DCL
DD/DU
Bit N
Bit 0
Bit 1
ezm04106.emf

Figure 64 IOM-2 Interface Timing (DCL = 2048 kHz, Per 8-kHz Frame)

Both DuSLIC channels (see **Figure 62**) can be assigned to one of the eight time slots. Set the IOM-2 time slot selection as shown in **Table 39** below by pin-strapping. In this way, up to 16 channels can be handled with one IOM-2 interface on the line card.

Table 39 IOM-2 Time Slot Assignment

TS2	TS1	TS0	IOM-2 Operating Mode
0	0	0	Time slot 0; DCL = 2048, 4096 kHz
0	0	1	Time slot 1; DCL = 2048, 4096 kHz
0	1	0	Time slot 2; DCL = 2048, 4096 kHz
0	1	1	Time slot 3; DCL = 2048, 4096 kHz
1	0	0	Time slot 4; DCL = 2048, 4096 kHz
1	0	1	Time slot 5; DCL = 2048, 4096 kHz
1	1	0	Time slot 6; DCL = 2048, 4096 kHz
1	1	1	Time slot 7; DCL = 2048, 4096 kHz

2 MHz or 4 MHz DCL is selected by the SEL24 pin:

SEL24 = 0: DCL = 2048 kHz

SEL24 = 1: DCL = 4096 kHz

5.2.1 IOM-2 Interface Monitor Transfer Protocol

Monitor Channel Operation

The monitor channel is used for the transfer of maintenance information between two functional blocks. Using two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure. The MR and MX bits in the fourth byte (C/I channel) of the IOM-2 frame are used for the handshake procedure of the monitor channel.

The monitor channel transmission operates on a pseudo-asynchronous basis:

Data transfer (bits) on the bus is synchronized to Frame Sync FSC.

Data flow (bytes) is asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD-Monitor-Channel by the monitor transmitter of the master device (DD-MX-Bit is activated, i.e., set to zero). This data transfer will be repeated within each frame (125 µs rate) until it is acknowledged by the *SLICOFI-2x* monitor receiver by setting the DU-MR-bit to zero, which is checked by the monitor transmitter of the master device. The data rate on IOM-2 monitor channels is 4 kb/s.

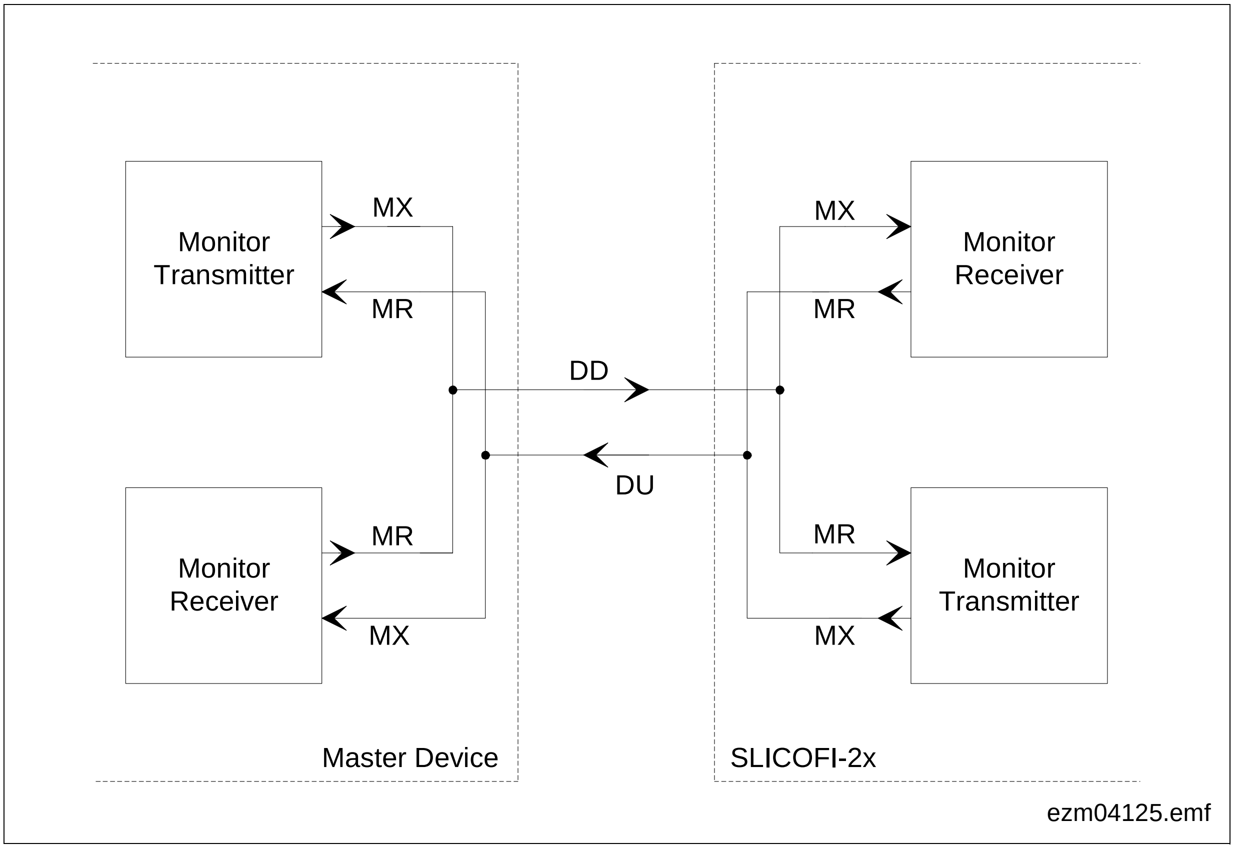

Monitor Transmitter
MX
MR
Monitor Receiver
MR
MX
DD
DU
MX
MR
Monitor Receiver
MR
MX
Monitor Transmitter
Master Device
SLICOFI-2x
ezm04125.emf

Figure 65 IOM-2 Interface Monitor Transfer Protocol

Monitor Handshake Procedure

The monitor channel works in three states

– idle state:	A pair of inactive (set to ‘1’) MR and MX bits during two or more consecutive frames: End of Message (EOM)
– sending state:	MX bit is activated (set to zero) by the monitor transmitter, together with data bytes (can be changed) on the monitor channel
– acknowledging:	MR bit is set to active (set to zero) by the monitor receiver, together with a data byte remaining in the monitor channel.

A start of a transmission is initiated by a monitor transmitter in sending out an active MX bit together with the first byte of data (the address of the receiver) to be transmitted in the monitor channel.

The monitor channel remains in this state until the addressed monitor receiver acknowledges the received data by sending out an active MR bit, which means that the data transmission is repeated each 125 µs frame (minimum is one repetition). During this time the monitor transmitter evaluates the MR bit.

Flow control can only take place when the transmitter’s MX and the receiver’s MR bit are in active state.

Since the receiver is capable to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received, the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (checking whether another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive (‘1’) phase of the MX bit and making a per-bit collision check on the transmitted monitor data (check if transmitted ‘1’s are on DU/DD line; DU/DD line are open-drain lines).

Any abort leads to a reset of the *SLICOFI-2x* command stack, the device is ready to receive new commands.

To maximum speed during data transfers the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the programming structure, duplex operation is not possible. It is not **allowed** to send any data to the *SLICOFI-2x*, while transmission is active.

Data transfer to the *SLICOFI-2x* starts with a *SLICOFI-2x*-specific address byte (81_H).

Attention: Each byte on the monitor channel has to be sent twice at least according to the IOM-2 Monitor handshake procedure.

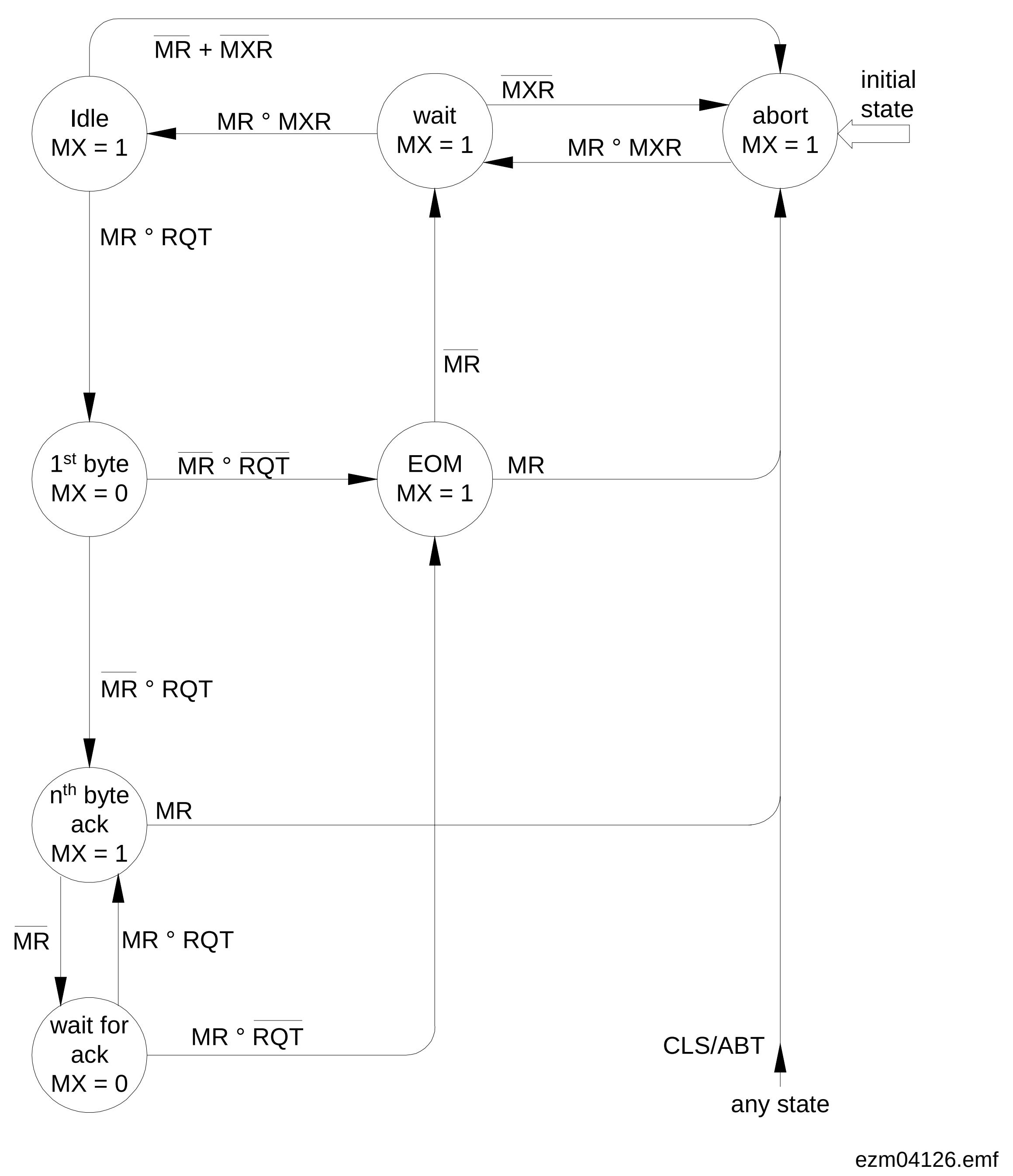

$\overline{MR}$ + $\overline{MXR}$
Idle
MX = 1
MR ° MXR
wait
MX = 1
$\overline{MXR}$
abort
MX = 1
MR ° MXR
initial
state
MR ° RQT
$\overline{MR}$
1st byte
MX = 0
$\overline{MR}$ ° $\overline{RQT}$
EOM
MX = 1
MR
$\overline{MR}$ ° RQT
nth byte
ack
MX = 1
MR
$\overline{MR}$
MR ° RQT
wait for
ack
MX = 0
MR ° $\overline{RQT}$
CLS/ABT
any state
ezm04126.emf

Figure 66 State Diagram of the *SLICOFI-2x* Monitor Transmitter

MR …	MR bit received on DD line
MX …	MX bit calculated and expected on DU line
MXR …	MX bit sampled on DU line
CLS …	Collision within the monitor data byte on DU line
RQT …	Request for transmission form internal source
ABT …	Abort request/indication

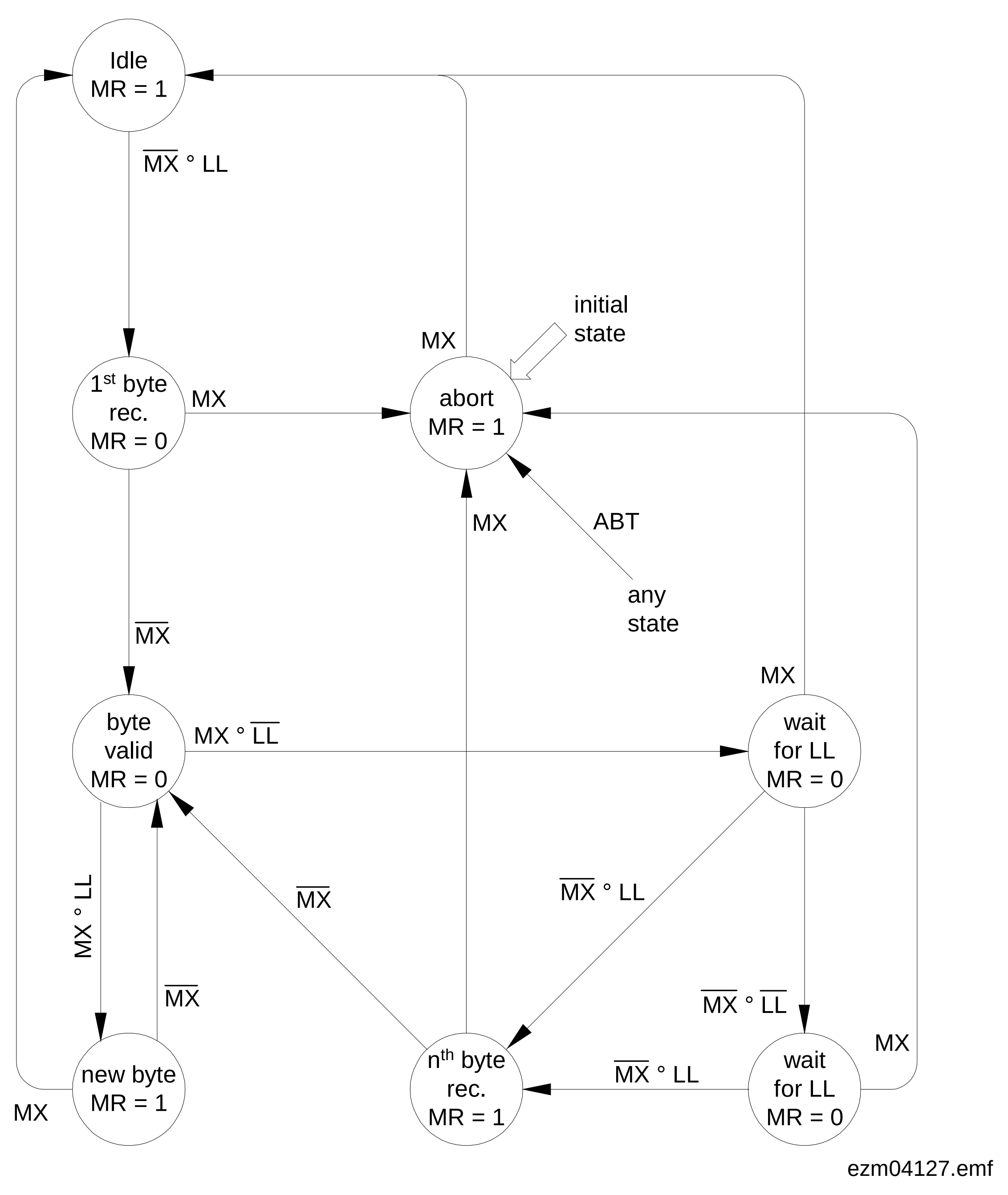

Idle
MR = 1
MX ° LL
1st byte
rec.
MR = 0
MX
abort
MR = 1
initial
state
MX
MX
ABT
any
state
MX
byte
valid
MR = 0
MX ° LL
MX
wait
for LL
MR = 0
MX ° LL
MX
MX ° LL
MX
MX ° LL
new byte
MR = 1
MX
nth byte
rec.
MR = 1
MX ° LL
wait
for LL
MR = 0
MX
ezm04127.emf

Figure 67 State Diagram of the *SLICOFI-2x* Monitor Receiver

MR …	MR bit calculated and transmitted on DU line
MX …	MX bit received data downstream (DD line)
LL …	Last lock of monitor byte received on DD line
ABT …	Abort indication to internal source

Address Byte

Messages to and from the *SLICOFI-2x* start with the following byte:

Bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	1

5.2.2 *SLICOFI-2x* Identification Command (only IOM-2 Interface)

In order to unambiguously identify different devices by software, a two-byte identification command is defined for analog line IOM-2 devices. A device requesting the identification of the *SLICOFI-2x* will send the following two byte code:

1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For the *SLICOFI-2x* this two byte identification code is:

1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1

5.3 TIP/RING Interface

The TIP/RING interface is the interface that connects the subscriber to the DuSLIC. It meets the ITU-T recommendation Q.552 for a Z interface and applicable LSSGR.

For the performance of the TIP/RING interface see **Chapter 7.5** and **Chapter 7.6**, for application circuits see **Chapter 8**.

5.4 SLICOFI-2S/-2S2 and SLIC-S/-S2 Interface

The SLIC-S/-S2 PEB 4264/-2 operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 40 SLIC-S/-S2 Interface Code

		C2 (Pin 17)		
		L	**M**	**H**
C1 (Pin 18)	**L**[1]	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	unused	HIT	HIR

[1] no “Overtemp” signaling possible via pin C1 if C1 is low.

Table 41 SLIC-S/-S2 Modes

SLIC Mode	Mode Description	Used SLIC-S/-S2 Battery Voltage
PDH	Power Down High Impedance	V_{BATH}
PDRH	Power Down Resistive High	V_{BATH}
PDRHL	Power Down Resistive High Load	V_{BATH}
ACTL	Active Low	V_{BATL}
ACTH	Active High	V_{BATH}
ACTR	Active Ring	V_{BATH}, V_{HR}
HIT	High Impedance on TIP	V_{BATH}, V_{HR}
HIR	High Impedance on RING	V_{BATH}, V_{HR}

Active (ACTL, ACTH): These are the regular transmit and receive modes for voice band. The line driving section is operated between V_{BATL}, V_{BATH} and V_{BGND}.

Active Ring (ACTR): In order to provide a balanced ring signal of up to 45 Vrms or to drive longer telephone lines, an auxiliary positive battery voltage V_{HR} is used, making possible a higher voltage across the line. Transmission performance remains unchanged compared with Active modes.

The **Power Down** mode PDRH is intended to reduce the power consumption of the linecard to a minimum: the SLIC-S/-S2 is switched off completely, no operation is available except off-hook detection.

With respect to the output impedance of TIP and RING, two Power Down modes have to be distinguished:

PDRH provides a connection of 5 kΩ each from TIP to V_{BGND} and RING to V_{BATH}, respectively, while the outputs of the buffers show high impedance. The current through these resistors is sensed and transferred to the IT pin to allow off-hook supervision.

PDRHL is used as a transition state at a mode change from PDRH or PDH to ACTH mode (automatically initiated by SLICOFI-2S/-2S2 at a mode change).

High Impedance (HIR/HIT): In this mode each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while the current through the RING output still can be measured by IT or IL. Programming HIR switches off the RING buffer.

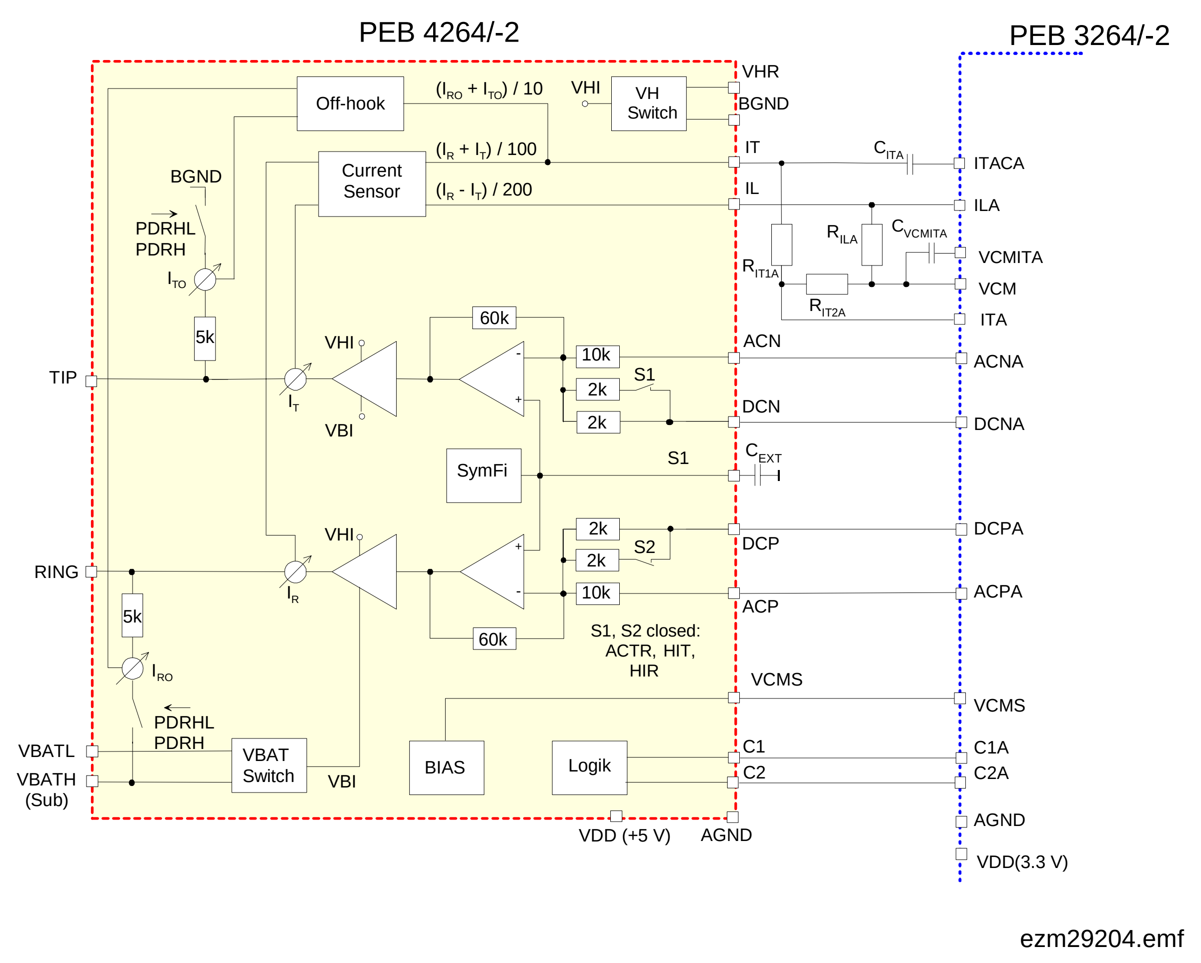

PEB 4264/-2
PEB 3264/-2
Off-hook
$(I_{RO} + I_{TO}) / 10$
VHI
VH Switch
VHR
BGND
Current Sensor
$(I_R + I_T) / 100$
$(I_R - I_T) / 200$
IT
IL
C_{ITA}
ITACA
ILA
R_{ILA}
C_{VCMITA}
VCMITA
R_{IT1A}
VCM
R_{IT2A}
ITA
BGND
PDRHL
PDRH
I_{TO}
5k
60k
10k
S1
2k
2k
VHI
VBI
I_T
TIP
ACN
ACNA
DCN
DCNA
SymFi
S1
C_{EXT}
2k
2k
S2
VHI
DCP
DCPA
RING
I_R
10k
ACP
ACPA
5k
60k
S1, S2 closed:
ACTR, HIT,
HIR
I_{RO}
VCMS
VCMS
PDRHL
PDRH
VBATL
VBATH
(Sub)
VBAT Switch
VBI
BIAS
Logik
C1
C1A
C2
C2A
VDD (+5 V)
AGND
AGND
VDD(3.3 V)
ezm29204.emf

Figure 68 **Interface SLICOFI-2S/-2S2 and SLIC-S/-S2**

Capacitor and resistor values are specified in **Chapter 8**.

5.5 SLICOFI-2 and SLIC-E/-E2 Interface

The SLIC-E/-E2 PEB 4265/-2 operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 42 SLIC-E/-E2 Interface Code

		C2		
		L	**M**	**H**
C1	**L**[1]	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

[1] no "Overtemp" signaling possible via pin C1 if C1 is low.

Table 43 SLIC-E/-E2 Modes

SLIC Mode	**Mode Description**	**Used SLIC-E/-E2 Battery Voltage**
PDH	Power Down High Impedance	V_{BATH}
PDRH	Power Down Resistive High	V_{BATH}
PDRHL	Power Down Resistive High Load	V_{BATH}
ACTL	Active Low	V_{BATL}
ACTH	Active High	V_{BATH}
ACTR	Active Ring	V_{BATH}, V_{HR}
HIRT	High Impedance on RING and TIP	V_{BATH}, V_{HR}
HIT	High Impedance on TIP	V_{BATH}, V_{HR}
HIR	High Impedance on RING	V_{BATH}, V_{HR}

High Impedance (HIR/HIT/HIRT): In this mode each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while the current through the RING output still can be measured by IT or IL. Programming HIR switches off the RING buffer. In the mode HIRT both buffers show high impedance.

Active (ACTL, ACTH): These are the regular transmit and receive modes for voice band. The line driving section is operated between V_{BATL}, V_{BATH} and V_{BGND}.

Active Ring (ACTR): In order to provide a balanced ring signal of up to 85 Vrms or to drive longer telephone lines, an auxiliary positive battery voltage V_{HR} is used, making possible a higher voltage across the line. Transmission performance remains unchanged compared with Active modes.

The **Power Down** modes are intended to reduce the power consumption of the linecard to a minimum: the SLIC-E/-E2 is switched off completely, no operation is available.

With respect to the output impedance of TIP and RING, three Power Down modes have to be distinguished:

A resistive one (**PDRH**) provides a connection of 5 kΩ each from TIP to V_{BGND} and RING to V_{BATH}, respectively, while the outputs of the buffers show high impedance. The current through these resistors is sensed and transferred to the IT pin to allow off-hook supervision.

PDRHL is used as a transition mode at a mode change from PDRH mode to ACTH mode (automatically initiated by SLICOFI-2 at a mode change from PDRH to ACTH).

The other mode (**PDH**) offers high impedance at TIP and RING.

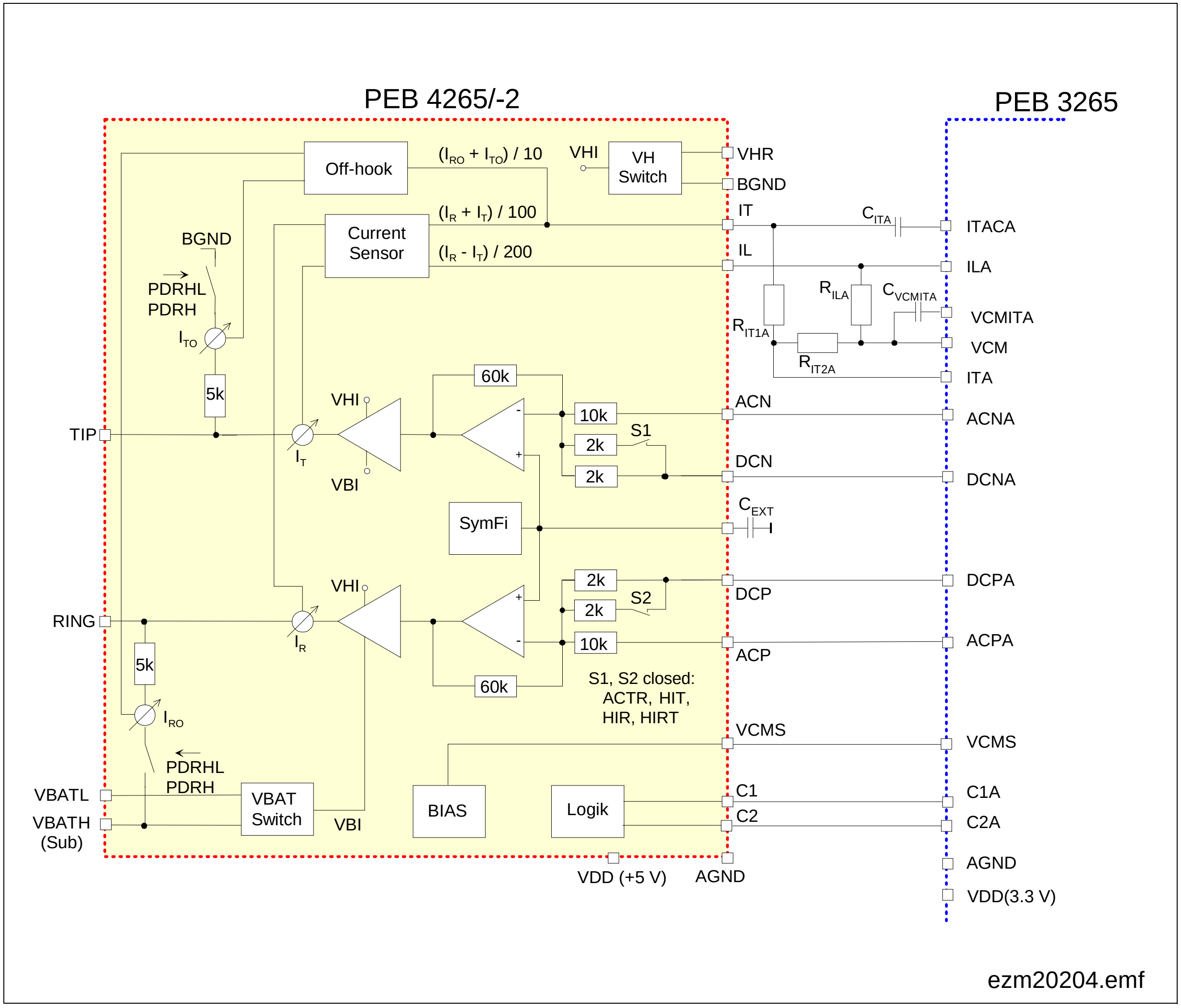

PEB 4265/-2
PEB 3265
Off-hook
$(I_{RO} + I_{TO}) / 10$
VHI
VH Switch
VHR
BGND
IT
C_{ITA}
ITACA
$(I_R + I_T) / 100$
Current Sensor
$(I_R - I_T) / 200$
IL
ILA
BGND
PDRHL
PDRH
I_{TO}
R_{ILA}
C_{VCMITA}
VCMITA
R_{IT1A}
VCM
R_{IT2A}
ITA
5k
60k
VHI
10k
ACN
ACNA
TIP
2k
S1
I_T
2k
DCN
DCNA
VBI
SymFi
C_{EXT}
2k
DCPA
VHI
DCP
S2
RING
2k
I_R
10k
ACP
ACPA
5k
60k
S1, S2 closed:
ACTR, HIT,
HIR, HIRT
I_{RO}
VCMS
VCMS
PDRHL
PDRH
VBATL
VBAT Switch
BIAS
Logik
C1
C1A
VBATH
(Sub)
VBI
C2
C2A
AGND
VDD (+5 V)
AGND
VDD(3.3 V)
ezm20204.emf

Figure 69 Interface SLICOFI-2 and SLIC-E/-E2

Capacitor and resistor values are specified in **Chapter 8**.

5.6 SLICOFI-2 and SLIC-P Interface

The SLIC-P PEB 4266 operates in the following modes controlled by a ternary logic signal at the C1, C2 inputs and a binary logic signal at C3 input:

Table 44 SLIC-P Interface Code

		C2		
		L	**M**	**H**
C1	**L**[1]	PDH	PDRR	PDRRL
			PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR
			ROT	ROR

C3 = H or L	C3 = H[2]	C3 = L[2]

---

[1] no "Overtemp" signaling possible via pin C1 if C1 is low.

[2] C3 pin of SLIC-P is typically connected to IO2 pin of SLICOFI-2. For extremely power-sensitive applications using external ringing the C3 pin can be connected to GND. In this case, SEL-SLIC[1:0] in register BCR1 has to be set to 10.

Operating Modes for SLIC-P with Two Battery Voltages (V_{BATH}, V_{BATL}) for Voice and an Additional Voltage (V_{BATR}) for Ringing:

Table 45 SLIC-P Modes

SLIC Mode	Mode Description	Used SLIC-P Battery Voltage
PDH	Power Down High Impedance	V_{BATR}
PDRH	Power Down Resistive High	V_{BATH}
PDRHL	Power Down Load Resistive High Load	V_{BATH}
ACTL	Active Low	V_{BATL}
ACTH	Active High	V_{BATH}
ACTR	Active Ring	V_{BATR}
HIRT	High Impedance on RING and TIP	V_{BATR}
ROR	Ring on RING	V_{BATR}
ROT	Ring on TIP	V_{BATR}

Active (ACTL, ACTH): These are the regular transmit and receive modes for voice band. The line driving section is operated between V_{BATL}, V_{BATH} and V_{BGND}.

Ringing:

Active Ring (ACTR): In order to provide a balanced ring signal of up to 85 Vrms or to drive longer telephone lines, an additional negative battery voltage V_{BATR} is used, making possible a higher voltage across the line. Transmission performance remains unchanged compared with ACT mode.

Ring on Tip (ROT): An unbalanced ring signal up to 50 Vrms can be fed to the Tip line. The Ring line is fixed to a potential near V_{BGND}.

Ring on Ring (ROR): An unbalanced ring signal up to 50 Vrms can be fed to the Ring line. The Tip line is fixed to a potential near V_{BGND}.

PDRH is a power down mode providing a connection of 5 kΩ each from TIP to V_{BGND} and RING to V_{BATH}, respectively, while the outputs of the buffers show high impedance. The current through these resistors is sensed and transferred to the IT pin to allow off-hook supervision.

PDRHL is used as a transition mode at a mode change from PDRH mode to ACTH mode (automatically initiated by SLICOFI-2 at a mode change from PDRH to ACTH).

Operating Modes for SLIC-P with Three Battery Voltages (V_{BATH}, V_{BATL}, V_{BATR}) for voice and External Ringing

Table 46 SLIC-P Modes

SLIC Mode	Mode Description	Used SLIC-P Battery Voltage
PDH	Power Down High Impedance	V_{BATR}
PDRR	Power Down Resistive Ring	V_{BATR}
PDRRL	Power Down Load Resistive Ring Load	V_{BATR}
ACTL	Active Low	V_{BATL}
ACTH	Active High	V_{BATH}
ACTR	Active Ring	V_{BATR}
HIRT	High Impedance on RING and TIP	V_{BATR}
HIT	High Impedance on TIP	V_{BATR}
HIR	High Impedance on RING	V_{BATR}

Active (ACTL, ACTH, ACTR): These are the regular transmit and receive modes for voice band. The line driving section is operated between V_{BATL}, V_{BATH}, V_{BATR} and V_{BGND}.

PDRR is a power down mode providing a connection of 5 kΩ each from TIP to V_{BGND} and RING to V_{BATR}, respectively, while the outputs of the buffers show high impedance. The current through these resistors is sensed and transferred to the IT pin to allow off-hook supervision.

PDRRL is used as a transition mode at a mode change from PDRR mode to ACTR mode (automatically initiated by SLICOFI-2 at a mode change from PDRR to ACTR).

High Impedance (HIR/HIT): In this mode each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while the current through the RING output still can be measured by IT or IL. Programming HIR switches off the RING buffer.

For Both Operating Modes of SLIC-P (Ringing and Non Ringing):

The **Power Down** modes are intended to reduce the power consumption of the linecard to a minimum: the PEB 4266 is switched off completely, no operation is available.

With respect to the output impedance of TIP and RING, the following Power Down modes have to be distinguished:

The **PDH** mode offers high impedance at TIP and RING.

High Impedance (HIRT): The output buffers of the Tip and Ring line show high impedance.

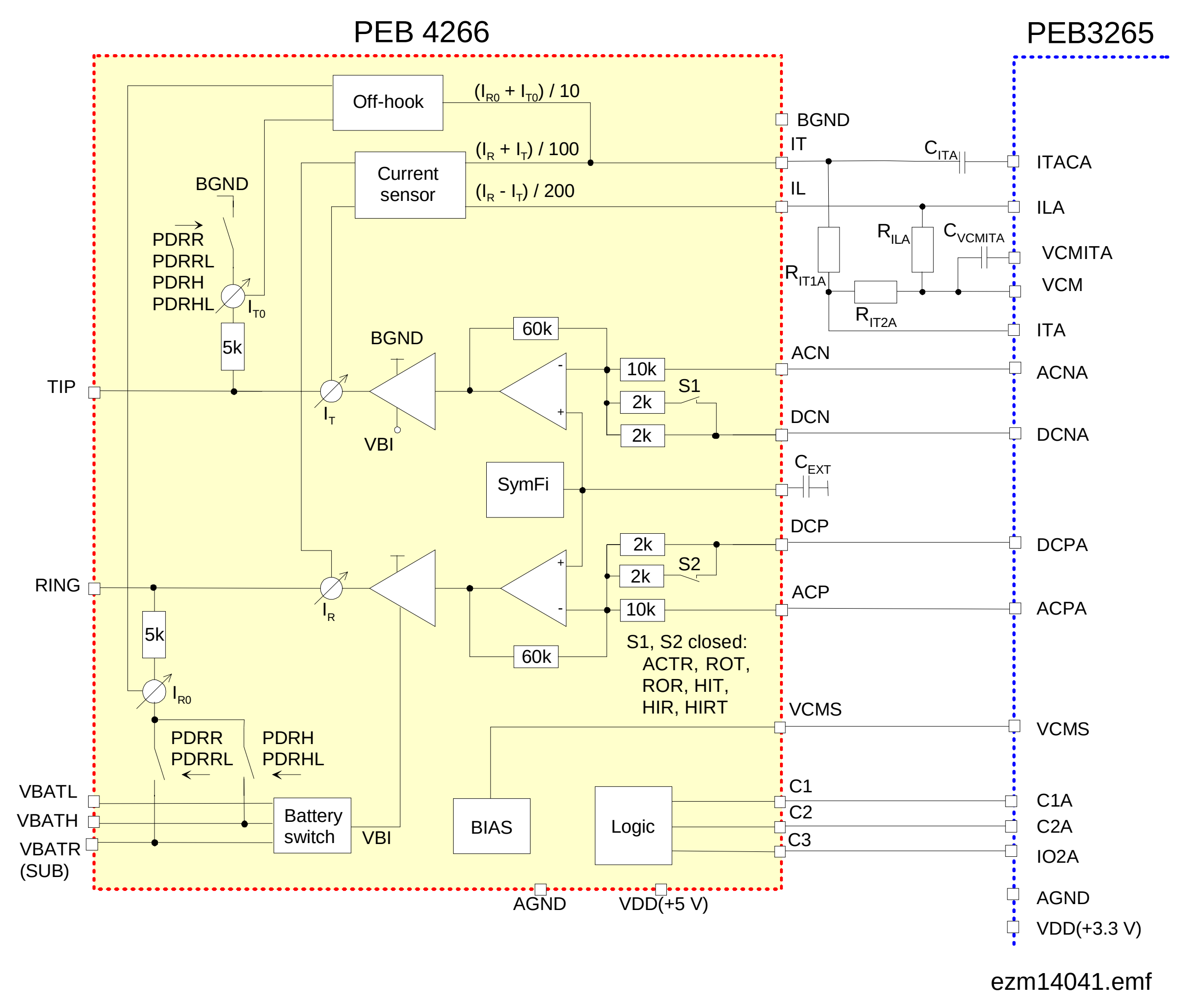

PEB 4266
PEB3265
Off-hook
$(I_{R0} + I_{T0}) / 10$
Current sensor
$(I_R + I_T) / 100$
$(I_R - I_T) / 200$
BGND
PDRR
PDRRL
PDRH
PDRHL
I_{T0}
5k
TIP
I_T
VBI
60k
10k
2k
2k
S1
SymFi
2k
2k
S2
10k
60k
RING
I_R
5k
I_{R0}
PDRR
PDRRL
PDRH
PDRHL
S1, S2 closed:
ACTR, ROT,
ROR, HIT,
HIR, HIRT
VBATL
VBATH
VBATR
(SUB)
Battery switch
VBI
BIAS
Logic
AGND
VDD(+5 V)
BGND
IT
IL
C_{ITA}
R_{ILA}
C_{VCMITA}
R_{IT1A}
R_{IT2A}
ACN
DCN
C_{EXT}
DCP
ACP
VCMS
C1
C2
C3
ITACA
ILA
VCMITA
VCM
ITA
ACNA
DCNA
DCPA
ACPA
VCMS
C1A
C2A
IO2A
AGND
VDD(+3.3 V)
ezm14041.emf

Figure 70 Interface SLICOFI-2 and SLIC-P

Capacitor and resistor values are specified in **Chapter 8**.

6 *SLICOFI-2x* Command Structure and Programming

With the commands described in this chapter, the *SLICOFI-2x* can be programmed, configured and tested very flexibly via the microcontroller interface or via the IOM-2 interface monitor channel.

The command structure uses one and two-byte commands in order to ensure a high flexible and quick programming procedure for the most common commands.

Structure of the First Command Byte

The first command byte includes the R/W bit, the addresses of the different channels and the command type.

Bit	7	6	5	4	3	2	1	0
	RD	**OP**	**ADR[2:0]**			**CMD[2:0]**		

RD Read Data

RD = 0 Write data to chip.

RD = 1 Read data from chip.

OP Selects the usage of the CMD field

OP = 0 The CMD field works as a CIOP (Command/Indication Operation) command and acts like the M[2:0] bits located in the CIDD byte of the IOM Interface (µC interface mode only). See **Table 47**.

Bit	7	6	5	4	3	2	1	0
	0	**0**	**ADR[2:0]**			**M2**	**M1**	**M0**

OP = 1 The CMD field acts as the SOP, COP or POP command described below.

Table 47 M2, M1, M0: General Operating Mode

Command/Indication Operation (CIOP)			***SLICOFI-2x* Operating Mode** (for details see **"Operating Modes for the DuSLIC Chip Set" on Page 78**)
M2	**M1**	**M0**	
1	1	1	Sleep, Power Down (PDRx)
0	0	0	Power Down High Impedance (PDH)
0	1	0	Any Active mode
1	0	1	Ringing (ACTR Burst On)
1	1	0	Active with Metering
1	0	0	Ground Start
0	0	1	Ring Pause

ADR[2:0] Channel address for the subsequent data

ADR[2:0] = 0 0 0	Channel A
ADR[2:0] = 0 0 1	Channel B

(other codes reserved for future use)

CMD[2:0] Command for programming the *SLICOFI-2x* (OP = 1) or command equivalent to the CIDD channel bits M[2:0] in microcontroller interface mode (OP = 0)
The first four commands have no second command byte following.
All necessary information is present in the first command byte.

CMD[2:0] = 0 0 0	Soft reset of the chip (Reset routine for all channels will reset all configuration registers, CRAM data is not affected).
CMD[2:0] = 0 0 1	Soft reset for the specified channel A or B in ADR field
CMD[2:0] = 0 1 0	Resychronization of the PCM interface (only available when pin PCM/$\overline{\text{IOM-2}}$ = 1)
CMD[2:0] = 0 1 1	reserved for future use

The second four commands are followed by a second command byte which defines additional information, e.g., specifying sub-adresses of the CRAM.

CMD[2:0] = 1 0 0	SOP command (status operation, programming and monitoring of all status-relevant data).
CMD[2:0] = 1 0 1	COP command (coefficient operation, programming and monitoring of all coefficients in the CRAM).

CMD[2:0] = 1 1 0	POP command (PINE access operation programming the EDSP).
CMD[2:0] = 1 1 1	reserved for production tests

Structure of the Second Command Byte

The second command byte specifies a particular SOP, COP or POP command, depending on the CMD[2:0] bits of the first command byte. In the following sections, the content of this register is described for each command group.

The second command byte specifies the initial offset for the subsequent data bytes. After each data byte transferred the internal offset is incremented automatically. Therefore it is possible to send a various number of data bytes with one SOP, COP or POP command. Writing over read-only registers will not destroy their contents.

Register Description Example

At the beginning of each register description a single line gives information about

- Offset: Offset of register address (hex)
- Name: Short name of the register
- Detailed name: Detailed name of the register
- Reset value: Value of the register after reset (hex)
  “hw” – value depends on specific hardware fuses
- Test status: “T” – the register has no effect unless the TEST-EN bit in register LMCR1 is set to 1
- Channel selection: “N” – the register effects both *SLICOFI-2x* channels,
  “Y” – the register effects a specific *SLICOFI-2x* channel

The line is organized as follows (with example):

Offset	Name	Detailed Name	Reset Value	Test	Per Channel
27_H	**TSTR1**	**Test Register 1**	**00_H**	**T**	**Y**

6.1 Overview of Commands

SOP STATUS OPERATION

Bit	7	6	5	4	3	2	1	0
Byte 1	RD	**1**	ADR[2:0]			**1**	**0**	**0**
Byte 2	OFFSET[7:0]							

COP COEFFICIENT OPERATION

Bit	7	6	5	4	3	2	1	0
Byte 1	RD	**1**	ADR[2:0]			**1**	**0**	**1**
Byte 2	OFFSET[7:0]							

POP POP OPERATION (only SLICOFI-2 PEB 3265 used for DuSLIC-E/-E2/-P)

Bit	7	6	5	4	3	2	1	0
Byte 1	RD	**1**	ADR[2:0]			**1**	**1**	**0**
Byte 2	OFFSET[7:0]							

6.2 SLICOFI-2 Command Structure and Programming

This chapter comprises only the SLICOFI-2 PEB 3265 and therefore the DuSLIC-E, DuSLIC-E2 and DuSLIC-P chip sets.

6.2.1 SOP Command

The SOP “Status Operation” command provides access to the configuration and status registers of the SLICOFI-2. Common registers change the mode of the entire SLICOFI-2 chip, all other registers are channel-specific. It is possible to access single or multiple registers. Multiple register access is realized by an automatic offset increment. Write access to read-only registers is ignored and does not abort the command sequence. Offsets may change in newer versions of the SLICOFI-2.

(All empty register bits have to be filled with zeros.)

6.2.1.1 SOP Register Overview

00_H REVISION Revision Number (read-only)

REV[7:0]

01_H CHIPID 1 Chip Identification 1 (read-only)

for internal use only

02_H CHIPID 2 Chip Identification 2 (read-only)

for internal use only

03_H CHIPID 3 Chip Identification 3 (read-only)

for internal use only

04_H FUSE1 Fuse Register 1

for internal use only

05_H PCMC1 PCM Configuration Register 1

DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE-0	SHIFT	PCMO[2:0]

06_H XCR Extended Configuration Register

EDSP-EN	ASYNCH-R	0	0	0	0

07_H INTREG1 Interrupt Register 1 (read-only)

INT-CH	HOOK	GNDK	GNKP	ICON	VRTLIM	OTEMP	SYNC-FAIL

08_H INTREG2 Interrupt Register 2 (read-only)

LM-THRES	READY	RSTAT	LM-OK	IO[4:1]-DU

09_H INTREG3 Interrupt Register 3 (read-only)

DTMF-OK	DTMF-KEY[4:0]	UTDR-OK	UTDX-OK

$0A_H$ INTREG4 Interrupt Register 4 (read-only)

EDSP-FAIL	0	0	0	CIS-BOF	CIS-BUF	CIS-REQ	CIS-ACT

$0B_H$ CHKR1 Checksum Register 1 (High Byte) (read-only)

SUM-OK	CHKSUM-H[6:0]

$0C_H$ CHKR2 Checksum Register 2 (Low Byte) (read-only)

CHKSUM-L[7:0]

$0D_H$ LMRES1 Level Metering Result 1 (High Byte) (read-only)

LM-VAL-H[7:0]

$0E_H$ LMRES2 Level Metering Result 2 (Low Byte) (read-only)

LM-VAL-L[7:0]

$0F_H$ FUSE2 Fuse Register 2

for internal use only

10_H FUSE3 Fuse Register 3

for internal use only

11_H MASK Mask Register

READY-M	HOOK-M	GNDK-M	GNKP-M	ICON-M	VRTLIM-M	OTEMP-M	SYNC-M

12_H IOCTL1 IO Control Register 1

IO[4:1]-INEN	IO[4:1]-M

13_H IOCTL2 IO Control Register 2

IO[4:1]-OEN	IO[4:1]-DD

14_H IOCTL3 IO Control Register 3

DUP[3:0]	DUP-IO[3:0]

15_H BCR1 Basic Configuration Register 1

HIR	HIT	SLEEP-EN	REVPOL	ACTR	ACTL	SEL-SLIC[1:0]

16_H BCR2 Basic Configuration Register 2

REXT-EN	SOFT-DIS	TTX-DIS	TTX-12K	HIM-AN	AC-XGAIN	UTDX-SRC	PDOT-DIS

17_H BCR3 Basic Configuration Register 3

MU-LAW	LIN	PCM16K	PCMX-EN	CONFX-EN	CONF-EN	LPRX-CR	CRAM-EN

18_H BCR4 Basic Configuration Register 4

TH-DIS	IM-DIS	AX-DIS	AR-DIS	FRX-DIS	FRR-DIS	HPX-DIS	HPR-DIS

19_H BCR5 Basic Configuration Register 5

UTDR-EN	UTDX-EN	CIS-AUTO	CIS-EN	LEC-OUT	LEC-EN	DTMF-SRC	DTMF-EN

$1A_H$ DSCR DTMF Sender Configuration Register

DG-KEY[3:0]	COR8	PTG	TG2-EN	TG1-EN

$1B_H$ reserved

0	0	0	0	0	0	0	0

$1C_H$ LMCR1 Level Metering Configuration Register 1

TEST-EN	LM-EN	LM-THM	PCM2DC	LM2 PCM	LM-ONCE	LM-MASK	DC-AD16

$1D_H$ LMCR2 Level Metering Configuration Register 2

LM-NOTCH	LM-FILT	LM-RECT	RAMP-EN	LM-SEL[3:0]

$1E_H$ LMCR3 Level Metering Configuration Register 3

AC-SHORT-EN	RTR-SEL	LM-ITIME[3:0]	RNG-OFFSET[1:0]

$1F_H$ OFR1 Offset Register 1 (High Byte)

OFFSET-H[7:0]

20_H OFR2 Offset Register 2 (Low Byte)

OFFSET-L[7:0]

21_H PCMR1 PCM Receive Register 1

R1-HW	R1-TS[6:0]

22_H PCMR2 PCM Receive Register 2

R2-HW	R2-TS[6:0]

23_H PCMR3 PCM Receive Register 3

R3-HW	R3-TS[6:0]

24_H PCMR4 PCM Receive Register 4

R4-HW	R4-TS[6:0]

25_H PCMX1 PCM Transmit Register 1

X1-HW	X1-TS[6:0]

26_H PCMX2 PCM Transmit Register 2

X2-HW	X2-TS[6:0]

27_H PCMX3 PCM Transmit Register 3

X3-HW	X3-TS[6:0]

28_H PCMX4 PCM Transmit Register 4

X4-HW	X4-TS[6:0]

29_H TSTR1 Test Register 1

PD-AC-PR	PD-AC-PO	PD-AC-AD	PD-AC-DA	PD-AC-GN	PD-GNKC	PD-OFHC	PD-OVTC

$2A_H$ TSTR2 Test Register 2

PD-DC-PR	0	PD-DC-AD	PD-DC-DA	PD-DCBUF	0	PD-TTX-A	PD-HVI

$2B_H$ TSTR3 Test Register 3

0	0	AC-DLB-4M	AC-DLB-128K	AC-DLB-32K	AC-DLB-8K	0	0

$2C_H$ TSTR4 Test Register 4

OPIM-AN	OPIM-4M	COR-64	COX-16	0	0	0	0

$2D_H$ TSTR5 Test Register 5

0	0	0	DC-POFI-HI	DC-HOLD	0	0	0

6.2.1.2 SOP Register Description

00_H	**REVISION**	Revision Number (read-only)	**curr. rev.**		**N**

Bit	7	6	5	4	3	2	1	0
	REV[7:0]							

REV[7:0] Current revision number of the SLICOFI-2.

01_H	**CHIPID 1**	Chip Identification 1 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

02_H	**CHIPID 2**	Chip Identification 2 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

03_H	**CHIPID 3**	Chip Identification 3 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

04_H	**FUSE1**	**Fuse Register 1**	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

05_H	**PCMC1**	PCM Configuration Register 1	**00_H**		**N**

Bit	7	6	5	4	3	2	1	0
	DBL-CLK	**X-SLOPE**	**R-SLOPE**	**NO-DRIVE-0**	**SHIFT**	**PCMO[2:0]**		

DBL-CLK Clock mode for the PCM interface (see **Figure 59** on **Page 141**)

DBL-CLK = 0 Single-clocking is used.

DBL-CLK = 1 Double-clocking is used.

X-SLOPE Transmit slope (see **Figure 59** on **Page 141**)

X-SLOPE = 0 Transmission starts with rising edge of the clock.

X-SLOPE = 1 Transmission starts with falling edge of the clock.

R-SLOPE Receive slope (see **Figure 59** on **Page 141**)

R-SLOPE = 0 Data is sampled with falling edge of the clock.

R-SLOPE = 1 Data is sampled with rising edge of the clock.

NO-DRIVE-0 Driving mode for bit 0 (only available in single-clocking mode).

NO-DRIVE = 0 Bit 0 is driven the entire clock period.

NO-DRIVE = 1 Bit 0 is driven during the first half of the clock period only.

SHIFT Shifts the access edges by one clock cycle in double-clocking mode.

SHIFT = 0 No shift takes place.

SHIFT = 1 Shift takes place.

PCMO[2:0] The whole PCM timing is moved by PCMO data periods against the FSC signal.

PCMO[2:0] = 0 0 0 No offset is added.

PCMO[2:0] = 0 0 1 One data period is added.

…

PCMO[2:0] = 1 1 1 Seven data periods are added.

06_H	XCR	Extended Configuration Register	00_H		N

Bit	7	6	5	4	3	2	1	0
	EDSP-EN	**ASYNCH-R**	**0**	**0**	**0**	**0**		

EDSP-EN Enables the Enhanced Digital Signal Processor EDSP.

EDSP-EN = 0	Enhanced Digital Signal Processor is switched off.
EDSP-EN = 1	Enhanced Digital Signal Processor is switched on.

ASYNCH-R Enables asynchronous ringing in case of external ringing.

ASYNCH-R = 0	External ringing with zero crossing selected.
ASYNCH-R = 1	Asynchronous ringing selected.

07$_H$	**INTREG1**	Interrupt Register 1 (read-only)	**80$_H$**		**Y**

Bit	7	6	5	4	3	2	1	0
	INT-CH	**HOOK**	**GNDK**	**GNKP**	**ICON**	**VRTLIM**	**OTEMP**	**SYNC-FAIL**

INT-CH Interrupt channel bit. This bit indicates that the corresponding channel caused the last interrupt. Will be automatically set to zero after all interrupt registers were read.

INT-CH = 0	No interrupt in corresponding channel.
INT-CH = 1	Interrupt caused by corresponding channel.

HOOK On/off-hook information for the loop in all operating modes, filtered by the DUP (Data Upstream Persistence) counter and interrupt generation masked by the HOOK-M bit. A change of this bit generates an interrupt.

HOOK = 0	On-hook.
HOOK = 1	Off-hook.

GNDK Ground-Key or Ground Start information via the IL pin in all active modes, filtered for AC suppression by the DUP counter and interrupt generation masked by the GNDK-M bit. A change of this bit generates an interrupt.

GNDK = 0	No longitudinal current detected.
GNDK = 1	Longitudinal current detected (Ground Key or Ground Start).

GNKP Ground Key polarity. Indicating the active Ground Key level (positive/negative) interrupt generation masked by the GNKP-M bit. A change of this bit generates an interrupt. This bit can be used to get information about interference voltage influence.

GNKP = 0	Negative Ground Key threshold level active.
GNKP = 1	Positive Ground Key threshold level active.

ICON	Constant current information. Filtered by DUP-IO counter and interrupt generation masked by the ICON-M bit. A change of this bit generates an interrupt.
	ICON = 0 Resistive or constant voltage feeding.
	ICON = 1 Constant current feeding.
VRTLIM	Exceeding of a programmed voltage threshold for the TIP/RING voltage, filtered by the DUP-IO counter and interrupt generation masked by the VRTLIM-M bit. A change of this bit causes an interrupt. The voltage threshold for the TIP/RING voltage is set in CRAM (calculated with DuSLICOS DC Control Parameter 2/3: Tip-Ring Threshold).
	VRTLIM = 0 Voltage at Ring/Tip is below the limit.
	VRTLIM = 1 Voltage at Ring/Tip is above the limit.
OTEMP	Thermal overload warning from the SLIC-E/-E2/-P line drivers masked by the OTEMP-M bit. An interrupt is only generated if the OTEMP bit changes from 0 to1.
	OTEMP = 0 Temperature at SLIC-E/-E2/-P is below the limit.
	OTEMP = 1 Temperature at SLIC-E/-E2/-P is above the limit. In case of bit PDOT-DIS = 0 (register BCR2) the DuSLIC is switched automatically into PDH mode and OTEMP is hold at 1 until the SLICOFI-2 is set to PDH by a CIOP/CIDD command.
SYNC-FAIL	Failure of the Synchronization of the IOM-2/PCM interface. An interrupt is only generated if the SYNC-FAIL bit changes from 0 to1. Resynchronization of the PCM interface can be done with the Resynchronization command (see **Chapter 6**)
	SYNC-FAIL = 0 Synchronization OK.
	SYNC-FAIL = 1 Synchronization failure.

08_H	**INTREG2**	Interrupt Register 2 (read-only)	**20_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	LM-THRES	**READY**	**RSTAT**	**LM-OK**	**IO[4:1]-DU**			

After a hardware reset the RSTAT bit is set and generates an interrupt. Therefore the default value of INTREG2 is 20h. After reading all four interrupt registers, the INTREG2 value changes to 4Fh.

LM-THRES Indication whether the level metering result is above or below the threshold set by the CRAM coefficients

LM-THRES = 0	Level metering result is below threshold.
LM-THRES = 1	Level metering result is above threshold.

READY Indication whether the ramp generator has finished. An interrupt is only generated if the READY bit changes from 0 to 1. Upon a new start of the ramp generator, the bit is set to 0. For further information regarding soft reversal see **Chapter 3.7.2.1**.

READY = 0	Ramp generator active.
READY = 1	Ramp generator not active.

RSTAT Reset status since last interrupt.

RSTAT = 0	No reset has occurred since the last interrupt.
RSTAT = 1	Reset has occurred since the last interrupt.

LM-OK Level metering sequence has finished. An interrupt is only generated if the LM-OK bit changes from 0 to 1.

LM-OK = 0	Level metering result not ready.
LM-OK = 1	Level metering result ready.

IO[4:1]-DU Data on IO pins 1 to 4 filtered by DUP-IO counter and interrupt generation masked by the IO[4:1]-DU-M bits. A change of any of this bits generates an interrupt.

09_H	**INTREG3**	Interrupt Register 3 (read-only)	00_H		Y

Bit	7	6	5	4	3	2	1	0
	DTMF-OK	**DTMF-KEY[4:0]**					**UTDR-OK**	**UTDX-OK**

DTMF-OK Indication of a valid DTMF Key by the DTMF receiver. A change of this bit generates an interrupt.

DTMF-OK = 0 No valid DTMF Key was encountered by the DTMF receiver.

DTMF-OK = 1 A valid DTMF Key was encountered by the DTMF receiver.

DTMF-KEY[4:0] Valid DTMF keys decoded by the DTMF receiver.

Table 48 Valid DTMF Keys (Bit DTMF-KEY4 = 1)

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DTMF-KEY4	DTMF-KEY3	DTMF-KEY2	DTMF-KEY1	DTMF-KEY0
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1336	0	1	1	0	1	0
941	1209	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0

Table 48 Valid DTMF Keys (Bit DTMF-KEY4 = 1) (cont'd)

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DTMF-KEY4	DTMF-KEY3	DTMF-KEY2	DTMF-KEY1	DTMF-KEY0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0

UTDR-OK	Universal Tone Detection Receive (e.g., Fax/Modem tones)	
	UTDR-OK = 0	No specific tone signal was detected.
	UTDR-OK = 1	A specific tone signal was detected.
UTDX-OK	Universal Tone Detection Transmit (e.g., Fax/Modem tones)	
	UTDX-OK = 0	No specific tone signal was detected.
	UTDX-OK = 1	A specific tone signal was detected.

$0A_H$	**INTREG4**	Interrupt Register 4 (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	EDSP-FAIL	**0**	**0**	**0**	**CIS-BOF**	**CIS-BUF**	**CIS-REQ**	**CIS-ACT**

EDSP-FAIL	Indication of a malfunction of the Enhanced Digital Signal Processor EDSP.	
	EDSP-FAIL = 0	Enhanced Digital Signal Processor EDSP normal operation.
	EDSP-FAIL = 1	Enhanced Digital Signal Processor EDSP failure. It is necessary to restart this DSP with bit EDSP-EN in the XCR register set.
CIS-BOF	Caller ID buffer overflow. An interrupt is only generated if the CIS-BOF bit changes from 0 to 1.	
	CIS-BOF = 0	Not data buffer overflow has occurred.
	CIS-BOF = 1	Too many bytes have been written to the data buffer for Caller ID generation. Caller ID generation is aborted and the buffer is cleared.
CIS-BUF	Caller ID buffer underflow. An interrupt is only generated if the CIS-BUF bit changes from 0 to 1.	
	CIS-BUF = 0	Data buffer for Caller ID generation is filled.
	CIS-BUF = 1	Data buffer for Caller ID generation is empty (underflow).

CIS-REQ	Caller ID data request. An interrupt is only generated if the CIS-REQ bit changes from 0 to 1.	
	CIS-REQ = 0	Caller ID data buffer requests no data.
	CIS-REQ = 1	Caller ID data buffer requests more data to transmit, when the amount of data stored in the buffer is less than the buffer request size.
CIS-ACT	Caller ID generator active. This is a status bit only. No interrupt will be generated.	
	CIS-ACT = 0	Caller ID generator is not active.
	CIS-ACT = 1	Caller ID generator is active.

$0B_H$	**CHKR1**	Checksum Register 1 (High Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	SUM-OK	**CHKSUM-H[6:0]**						

SUM-OK Information about the validity of the checksum. The checksum is valid if the internal checksum calculation is finished.
Checksum calculation:

```
For (cram_adr = 0 to 159) do
cram_dat = cram[cram_adr]
csum[14:0] = (csum[13:0] &1) '0') xor
('0000000' & cram_dat[7:0]) xor
('0000000000000' & csum[14] & csum[14])
End
```

SUM-OK = 0 CRAM checksum is not valid.

SUM-OK = 1 CRAM checksum is valid.

---

[1] "&" means a concatenation, not the logic operation

CHKSUM-H[6:0] CRAM checksum high byte

$0C_H$	**CHKR2**	Checksum Register 2 (Low Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	CHKSUM-L[7:0]							

CHKSUM-L[7:0] CRAM checksum low byte

$0D_H$	**LMRES1**	Level Metering Result 1 (High Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	LM-VAL-H[7:0]							

LM-VAL-H[7:0]	LM result high byte (selected by the LM-SEL bits in the LMCR2 register)

$0E_H$	**LMRES2**	Level Metering Result 2 (Low Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	LM-VAL-L[7:0]							

LM-VAL-L[7:0]	LM result low byte (selected by the LM-SEL bits in the LMCR2 register)

$0F_H$	**FUSE2**	Fuse Register 2	**hw**		**Y**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

10_H	**FUSE3**	Fuse Register 3	hw		Y

Bit	7	6	5	4	3	2	1	0
	for internal use only							

11_H	**MASK**	Mask Register	**FF_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	READY -M	**HOOK -M**	**GNDK -M**	**GNKP -M**	**ICON -M**	**VRTLIM -M**	**OTEMP -M**	**SYNC -M**

The mask bits in the mask register only influence the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers gets updated to show the current status of the corresponding event.

READY-M Mask bit for Ramp Generator READY bit

READY-M = 0	An interrupt is generated if the READY bit changes from 0 to 1.
READY-M = 1	Changes of the READY bit don’t generate interrupts.

HOOK-M Mask bit for Off-hook Detection HOOK bit

HOOK-M = 0	Each change of the HOOK bit generates an interrupt.
HOOK-M = 1	Changes of the HOOK bit don’t generate interrupts.

GNDK-M Mask bit for Ground Key Detection GNDK bit

GNDK-M = 0	Each change of the GNDK bit generates an interrupt.
GNDK-M = 1	Changes of the GNDK bit don’t generate interrupts.

GNKP-M Mask bit for Ground Key Level GNKP bit

GNKP-M = 0	Each change of the GNKP bit generates an interrupt.
GNKP-M = 1	Changes of the GNKP bit don’t generate interrupts.

ICON-M Mask bit for Constant Current Information ICON bit

ICON-M = 0	Each change of the ICON bit generates an interrupt.
ICON_M = 1	Changes of the ICON bit don’t generate interrupts.

VRTLIM-M Mask bit for Programmed Voltage Limit VRTLIM bit

VRTLIM-M = 0	Each change of the VRTLIM bit generates an interrupt.
VRTLIM-M = 1	Changes of the VRTLIM bit don’t generate interrupts.

OTEMP-M	Mask bit for Thermal Overload Warning OTEMP bit	
	OTEMP-M = 0	A change of the OTEMP bit from 0 to 1 generates an interrupt.
	OTEMP-M = 1	A change of the OTEMP bit from 0 to 1 doesn't generate interrupts.
SYNC-M	Mask bit for Synchronization Failure SYNC-FAIL bit	
	SYNC-M = 0	A change of the SYNC-FAIL bit from 0 to 1 generates an interrupt.
	SYNC-M = 1	A change of the SYNC-FAIL bit from 0 to 1 doesn't generate interrupts.

12_H	**IOCTL1**	IO Control Register 1	**$0F_H$**		**Y**

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-INEN				**IO[4:1]-M**			

The mask bits IO[4:1]-M only influence the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers gets updated to show the current status of the corresponding event.

IO4-INEN Input enable for programmable IO pin IO4

IO4-INEN = 0 Input Schmitt trigger of pin IO4 is disabled.

IO4-INEN = 1 Input Schmitt trigger of pin IO4 is enabled.

IO3-INEN Input enable for programmable IO pin IO3

IO3-INEN = 0 Input Schmitt trigger of pin IO3 is disabled.

IO3-INEN = 1 Input Schmitt trigger of pin IO3 is enabled.

IO2-INEN Input enable for programmable IO pin IO2

IO2-INEN = 0 Input Schmitt trigger of pin IO2 is disabled.

IO2-INEN = 1 Input Schmitt trigger of pin IO2 is enabled.

IO1-INEN Input enable for programmable IO pin IO1

IO1-INEN = 0 Input Schmitt trigger of pin IO1 is disabled.

IO1-INEN = 1 Input Schmitt trigger of pin IO1 is enabled.

IO4-M Mask bit for IO4-DU bit

IO4-M = 0 Each change of the IO4 bit generates an interrupt.

IO4-M = 1 Changes of the IO4 bit don't generate interrupts.

IO3-M Mask bit for IO3-DU bit

IO3-M = 0 Each change of the IO3 bit generates an interrupt.

IO3-M = 1 Changes of the IO3 bit don't generate interrupts.

IO2-M	Mask bit for IO2-DU bit	
	IO2-M = 0	Each change of the IO2 bit generates an interrupt.
	IO2-M = 1	Changes of the IO2 bit don’t generate interrupts.
IO1-M	Mask bit for IO1-DU bit	
	IO1-M = 0	Each change of the IO1 bit generates an interrupt.
	IO1-M = 1	Changes of the IO1 bit don’t generate interrupts.

13_H	**IOCTL2**	IO Control Register 2	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-OEN				**IO[4:1]-DD**			

IO4-OEN Enabling output driver of the IO4 pin

IO4-OEN = 0	The output driver of the IO4 pin is disabled.
IO4-OEN = 1	The output driver of the IO4 pin is enabled.

IO3-OEN Enabling output driver of the IO3 pin

IO3-OEN = 0	The output driver of the IO3 pin is disabled.
IO3-OEN = 1	The output driver of the IO3 pin is enabled.

IO2-OEN Enabling output driver of the IO2 pin.
If SLIC-P is selected (bits SEL-SLIC [1:0] in register BCR1 set to 01), pin IO2 cannot be controlled by the user but is utilized by the SLICOFI-2 to control the C3 input of SLIC-P.

IO2-OEN = 0	The output driver of the IO2 pin is disabled.
IO2-OEN = 1	The output driver of the IO2 pin is enabled.

IO1-OEN Enabling output driver of the IO1 pin.
If external ringing is selected (bit REXT-EN in register BCR2 set to 1), pin IO1 cannot be controlled by the user but is utilized by the SLICOFI-2 to control the ring relay.

IO1-OEN = 0	The output driver of the IO1 pin is disabled.
IO1-OEN = 1	The output driver of the IO1 pin is enabled.

IO4-DD Value for the programmable IO pin IO4 if programmed as an output pin.

IO4-DD = 0	The corresponding pin is driving a logic 0.
IO4-DD = 1	The corresponding pin is driving a logic 1.

IO3-DD Value for the programmable IO pin IO3 if programmed as an output pin.

IO3-DD = 0	The corresponding pin is driving a logic 0.
IO3-DD = 1	The corresponding pin is driving a logic 1.

IO2-DD	Value for the programmable IO pin IO2 if programmed as an output pin.	
	IO2-DD = 0	The corresponding pin is driving a logic 0.
	IO2-DD = 1	The corresponding pin is driving a logic 1.
IO1-DD	Value for the programmable IO pin IO1 if programmed as an output pin.	
	IO1-DD = 0	The corresponding pin is driving a logic 0.
	IO1-DD = 1	The corresponding pin as driving a logic 1.

14_H	**IOCTL3**	IO Control Register 3	**94_H**		**Y**

Bit	**7**	**6**	**5**	4	3	2	1	0
	DUP[3:0]				**DUP-IO[3:0]**			

DUP[3:0] Data Upstream Persistence Counter end value. Restricts the rate of interrupts generated by the HOOK bit in the interrupt register INTREG1. The interval is programmable from 1 to 16 ms in steps of 1 ms (reset value is 10 ms).
The DUP[3:0] value affects the blocking period for ground key detection (see **Chapter 3.6**).

DUP[3:0]	HOOK Active, Ringing	HOOK Power Down	GNDK	GNDK $f_{min,ACsup}$ (1)
0000	1	2 ms	4 ms	125 Hz
0001	2	4 ms	8 ms	62.5 Hz
...				
1111	16	32 ms	64 ms	7.8125 Hz

(1) Minimum frequency for AC suppression.

DUP-IO[3:0] Data Upstream Persistence Counter end value for

- the IO pins when used as digital input pins.
- the bits ICON and VRTLIM in register INTREG1.

The interval is programmable from 0.5 to 60.5 ms in steps of 4 ms (reset value is 16.5 ms).

15_H	**BCR1**	Basic Configuration Register 1	00_H		**Y**

Bit	7	6	5	4	3	2	1	0
	HIR	**HIT**	**SLEEP-EN**	**REVPOL**	**ACTR**	**ACTL**	**SEL-SLIC[1:0]**	

HIR This bit modifies different basic modes. In ringing mode an unbalanced ringing on the RING wire (ROR) is enabled. In active mode, high impedance on the RING wire is activated (HIR). If the HIT bit is set in addition to the HIR bit, the HIRT mode is activated.

HIR = 0	Normal operation (ringing mode).
HIR = 1	Controls SLIC-E/-E2/-P interface and sets the RING wire to high impedance (active mode).

HIT This bit modifies different basic modes. In ringing mode an unbalanced ringing on the TIP wire (ROT) is enabled. In active mode, high impedance on the TIP wire is performed (HIT).If the HIR bit is set in addition to the HIT bit, the HIRT mode is activated.

HIT = 0	Normal operation (ringing mode).
HIT = 1	Controls SLIC-E/-E2/-P interface and sets the TIP wire to high impedance (active mode).

SLEEP-EN Enables Sleep mode of the DuSLIC channel. Valid only in the Power Down mode of the SLICOFI-2.

SLEEP-EN = 0	Sleep mode is disabled.
SLEEP-EN = 1	Sleep mode is enabled.

REVPOL Reverses the polarity of DC feeding

REVPOL = 0	Normal polarity.
REVPOL = 1	Reverse polarity.

ACTR	Selection of extended battery feeding in Active mode. Changes also the voltage in Power Down Resistive mode for SLIC-P. In this case V_{BATR} for SLIC-P and $V_{\mathrm{HR}} - V_{\mathrm{BATH}}$ for SLIC-E/-E2 is used.	
	ACTR = 0	No extended battery feeding selected.
	ACTR = 1	Extended battery feeding selected.

ACTL	Selection of the low battery supply voltage V_{BATL} on SLIC-E/-E2/-P if available. Valid only in the Active mode of the SLICOFI-2.	
	ACTL = 0	Low battery supply voltage on SLIC-E/-E2/-P is not selected.
	ACTL = 1	Low battery supply voltage on SLIC-E/-E2/-P is selected.

SEL-SLIC[1:0]	Selection of the current SLIC type used. For SLIC-E/-E2 and SLIC-P, the appropriate predefined mode table has to be selected.	
	SEL-SLIC[1:0] = 0 0	SLIC-E/-E2 selected.
	SEL-SLIC[1:0] = 0 1	SLIC-P selected.
	SEL-SLIC[1:0] = 1 0	SLIC-P selected for extremely power sensitive applications using external ringing.
	SEL-SLIC[1:0] = 1 1	Reserved for future use.

For SLIC-P two selections are possible.

- The standard SLIC-P selection automatically uses the IO2 pin of the SLICOFI-2 to control the C3 pin of the SLIC-P. By using pin C3 additionaly to the pins C1 and C2 all possible operating modes of the SLIC-P can be selected.
- For extremely power sensitive applications using external ringing with SLIC-P SEL-SLIC[1:0] = 10 should be chosen. In this case internal unbalanced ringing in not needed and therefore there is no need to switch the C3 pin of the SLIC-P to 'High'. The C3 pin of the SLIC-P has be connected to GND and the IO2 pin of the SLICOFI-2 is free programmable for the user.
  There is no need for a high battery voltage for ringing either. This mode uses VBATR for the on-hook voltage (e.g. – 48 V) in Power Down Resistive (PDR) mode and the other battery supply voltages (e.g. VBATH = – 24 V and VBATL = – 18 V) can be used for the off-hook state. This will help to save power because the lowest possible battery voltage can be selected (see DuSLIC Voltage and Power Application Note).

16_H	**BCR2**	Basic Configuration Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	REXT-EN	**SOFT-DIS**	**TTX-DIS**	**TTX-12K**	**HIM-AN**	**AC-XGAIN**	**UTDX-SRC**	**PDOT-DIS**

REXT-EN Enables the use of an external ring signal generator. The synchronization is done via the RSYNC pin and the Ring Burst Enable signal is transferred via the IO1 pin.

REXT-EN = 0	External ringing is disabled.
REXT-EN = 1	External ringing enabled.

SOFT-DIS Polarity soft reversal (to minimize noise on DC feeding)

SOFT-DIS = 0	Polarity soft reversal active.
SOFT-DIS = 1	Polarity hard reversal.

TTX-DIS Disables the generation of TTX bursts for metering signals. If TTX bursts are disabled, reverse polarity will be used instead.

TTX-DIS = 0	TTX bursts are enabled.
TTX-DIS = 1	TTX bursts are disabled, reverse polarity used.

TTX-12K Selection of TTX frequencies

TTX-12K = 0	Selects 16 kHz TTX signals instead of 12 kHz signals.
TTX-12K = 1	12 kHz TTX signals.

HIM-AN Higher impedance in analog impedance matching loop.
HIM-AN corresponds to the coefficients calculated with DuSLICOS. If the coefficients are calculated with standard impedance in analog impedance matching loop, HIM-AN must be set to 0; if the coefficients are calculated with high impedance in analog impedance matching loop, HIM-AN must be set to 1.

HIM-AN = 0	Standard impedance in analog impedance matching loop (300 Ω).
HIM-AN = 1	High impedance in analog impedance matching loop (600 Ω).

AC-XGAIN Analog gain in transmit direction (should be set to zero).

AC-XGAIN = 0	No additional analog gain in transmit direction.
AC-XGAIN = 1	Additional 6 dB analog amplification in transmit direction.

UTDX-SRC Universal Tone Detector transmit source

UTDX-SRC = 0	The Universal Tone Detection unit uses the data from the transmit path directly (UTDX-SUM = 0) or uses the data from the sum signal of receive path and LEC (if LEC is enabled) (UTDX-SUM = 1).
UTDX-SRC = 1	The Universal Tone Detection unit uses the data from the LEC output, if the LEC is enabled (LEC-EN = 1), otherwise the UTD unit uses automatically the transmit signal.

(see **Figure 32** on **Page 63**)

PDOT-DIS Power Down Overtemperature Disable

PDOT-DIS = 0	When overtemperature is detected, the SLIC is automatically switched into Power Down High Impedance mode (PDH). This is the safe operation mode for the SLIC-E/-E2/-P in case of overtemperature. To leave the automatically activated PDH mode, DuSLIC has to be switched manually to PDH mode and then in the mode as desired.
PDOT-DIS = 1	When over temperature is detected, the SLIC-E/-E2/-P doesn't automatically switch into Power Down High Impedance mode. In this case the output current of the SLIC-E/-E2/-P buffers is limited to a value which keeps the SLIC-E/-E2/-P temperature below the upper temperature limit.

17_H	**BCR3**	Basic Configuration Register 3	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	MU-LAW	**LIN**	**PCM16K**	**PCMX-EN**	**CONFX-EN**	**CONF-EN**	**LPRX-CR**	**CRAM-EN**

MU-LAW Selects the PCM Law

MU-LAW = 0	A-Law enabled.
MU-LAW = 1	µ-Law enabled.

LIN Voice transmission in a 16-bit linear representation for test purposes.

Note: Voice transmission on the other channel is inhibited if one channel is set to linear mode and IOM-2-interface is used. In the PCM/µC interface mode both channels can be in linear mode using two consecutive PCM timeslots on the highways. A proper timeslot selection must be specified.

LIN = 0	PCM mode enabled (8 bit, A-law or µ-law).
LIN = 1	Linear mode enabled (16 bit).

PCM16K Selects 16-kHz sample rate for the PCM interface.

PCM16K = 0	16-kHz mode disabled (8 kHz sampling rate).
PCM16K = 1	16-kHz mode enabled.

PCMX-EN Enables writing of subscriber voice data to the PCM highway.

PCMX-EN = 0	Writing of subscriber voice data to PCM highway is disabled.
PCMX-EN = 1	Writing of subscriber voice data to PCM highway is enabled.

CONFX-EN Enables an external three-party conference.

CONFX-EN = 0	External conference is disabled.
CONFX-EN = 1	External conference is enabled.

CONF-EN	Selection of three-party conferencing for this channel. The voice data of this channel and the voice data from the corresponding conferencing channels (see **Chapter 5.1.1**) are added and fed to analog output (see **Chapter 3.10**).

CONF-EN = 0	Three-party conferencing is not selected.
CONF-EN = 1	Three-party conferencing is selected.

LPRX-CR	Select CRAM coefficients for the filter characteristic of the LPR/LPX filters. These coefficients my be enabled in case of a modem transmission to improve modem performance.

LPRX-CR = 0	Coefficients from ROM are used.
LPRX-CR = 1	Coefficients from CRAM are used.

CRAM-EN	Coefficients from CRAM are used for programmable filters and DC loop behavior.

CRAM-EN = 0	Coefficients from ROM are used.
CRAM-EN = 1	Coefficients from CRAM are used.

18_H	**BCR4**	Basic Configuration Register 4	00_H		**Y**

Bit	7	6	5	4	3	2	1	0
	TH-DIS	**IM-DIS**	**AX-DIS**	**AR-DIS**	**FRX-DIS**	**FRR-DIS**	**HPX-DIS**	**HPR-DIS**

TH-DIS	Disables the TH filter.	
	TH-DIS = 0	TH filter is enabled.
	TH-DIS = 1	TH filter is disabled (H_{TH} = 0).
IM-DIS	Disables the IM filter.	
	IM-DIS = 0	IM filter is enabled.
	IM-DIS = 1	IM filter is disabled (H_{IM} = 0).
AX-DIS	Disables the AX filter.	
	AX-DIS = 0	AX filter is enabled.
	AX-DIS = 1	AX filter is disabled (H_{AX} = 1).
AR-DIS	Disables the AR filter.	
	AX-DIS = 0	AR filter is enabled.
	AX-DIS = 1	AR filter is disabled (H_{AR} = 1).
FRX-DIS	Disables the FRX filter.	
	FRX-DIS = 0	FRX filter is enabled.
	FRX-DIS = 1	FRX filter is disabled (H_{FRX} = 1).
FRR-DIS	Disables the FRR filter.	
	FRR-DIS = 0	FRR filter is enabled.
	FRR-DIS = 1	FRR filter is disabled (H_{FRR} = 1).
HPX-DIS	Disables the high-pass filter in transmit direction.	
	HPX-DIS = 0	High-pass filter is enabled.
	HPX-DIS = 1	High-pass filter is disabled (H_{HPX} = 1).

HPR-DIS	Disables the high-pass filter in receive direction.	
	HPR-DIS = 0	High-pass filter is enabled.
	HPR-DIS = 1	High-pass filter is disabled (H_{HPR} = 1).

19_H	**BCR5**	Basic Configuration Register 5	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	UTDR-EN	**UTDX-EN**	**CIS-AUTO**	**CIS-EN**	**LEC-OUT**	**LEC-EN**	**DTMF-SRC**	**DTMF-EN**

UTDR-EN Enables the Universal Tone detection in receive direction.

UTDR-EN = 0	Universal Tone detection is disabled.
UTDR-EN = 1	Universal Tone detection is enabled.

UTDX-EN Enables the Universal Tone detection in transmit direction.

UTDX-EN = 0	Universal Tone detection is disabled.
UTDX-EN = 1	Universal Tone detection is enabled.

CIS-AUTO Controls the turn-off behavior of the Caller ID sender.

CIS-AUTO = 0	The Caller ID sender stops when CIS-EN is switched to 0.
CIS-AUTO = 1	The Caller ID sender continues sending data until the data buffer is empty.

CIS-EN Enables the Caller ID sender in the SLICOFI-2.

Note: The Caller ID sender is configured directly by programming the according POP registers. Caller ID data are written to a 48 byte RAM buffer. According to the buffer request size this influences the CIS-REQ and CIS-BUF bits.

CIS-EN = 0	Caller ID sender is disabled and Caller ID data buffer is cleared after all data are sent or if CIS-AUTO = 0.
CIS-EN = 1	Caller ID sender is enabled and Caller ID data can be written to the data buffer. After the last data bit is sent, stop bits are sent to the subscriber. Caller ID data are sent to the subscriber when the number of bytes written to the buffer exceeds CIS-BRS + 2.

LEC-OUT Line Echo Canceller result for transmit path.

LEC-OUT = 0	Line Echo Canceller result used for DTMF only.
LEC-OUT = 1	Line Echo Canceller result fed to transmit path.

LEC-EN Line Echo Canceller

LEC-EN = 0	Line Echo Canceller for DTMF disabled.
LEC-EN = 1	Line Echo Canceller for DTMF enabled.

DTMF-SRC Selects data source for DTMF receiver.

DTMF-SRC = 0	The Transmit path data (with or without LEC) is used for the DTMF detection.
DTMF-SRC = 1	The Receive path data is used for the DTMF detection.

DTMF-EN Enables the DTMF receiver of the SLICOFI-2. The DTMF receiver will be configured in a proper way by programming registers in the EDSP.

DTMF-EN = 0	DTMF receiver is disabled.
DTMF-EN = 1	DTMF receiver is enabled.

$1A_H$	DSCR	DTMF Sender Configuration Register	00_H		Y

Bit	7	6	5	4	3	2	1	0
	DG-KEY[3:0]				COR8	PTG	TG2-EN	TG1-EN

DG-KEY[3:0] Selects one of sixteen DTMF keys generated by the two tone generators. The key will be generated if TG1-EN and TG2-EN are ‘1’.

Table 49 DTMF Keys

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DG-KEY3	DG-KEY2	DG-KEY1	DG-KEY0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

COR8 Cuts off receive path at 8 kHz before the tone generator summation point. Allows sending of tone generator signals with no overlaid voice.

COR8 = 0	Cut off receive path disabled.
COR8 = 1	Cut off receive path enabled.

PTG	Programmable coefficients for tone generators will be used.	
	PTG = 0	Frequencies set by DG-KEY are used for both tone generators.
	PTG = 1	CRAM coefficients used for both tone generators.
TG2-EN	Enables tone generator two	
	TG2-EN = 0	Tone generator is disabled.
	TG2-EN = 1	Tone generator is enabled.
TG1-EN	Enables tone generator one	
	TG1-EN = 0	Tone generator is disabled.
	TG1-EN = 1	Tone generator is enabled.

1B$_H$		reserved	**00$_H$**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$1C_H$	LMCR1	Level Metering Configuration Register 1	22_H		Y

Bit	7	6	5	4	3	2	1	0
	TEST-EN	LM-EN	LM-THM	PCM2DC	LM2 PCM	LM-ONCE	LM-MASK	DC-AD16

TEST-EN Activates the SLICOFI-2 test features controlled by test registers TSTR1 to TSTR5.

TEST-EN = 0	SLICOFI-2 test features are disabled.
TEST-EN = 1	SLICOFI-2 test features are enabled.

(The Test Register bits can be programmed before the TEST-EN bit is set to 1.)

LM-EN Enables level metering. A positive transition of this bit starts level metering (AC and DC).

LM-EN = 0	Level metering stops.
LM-EN = 1	Level metering enabled.

LM-THM Level metering threshold mask bit

LM-THM = 0	A change of the LM-THRES bit (register INTREG2) generates an interrupt.
LM-THM = 1	No interrupt is generated.

PCM2DC PCM voice channel data added to the DC-output.

PCM2DC = 0	Normal operation.
PCM2DC = 1	PCM voice channel data is added to DC output.

LM2PCM Level metering source/result (depending on LM-EN bit) feeding to PCM or IOM-2 interface.

LM2PCM = 0	Normal operation.
LM2PCM = 1	Level metering source/result is fed to the PCM or IOM-2 interface.

LM-ONCE	Level metering execution mode.	
	LM-ONCE = 0	Level metering is executed continuously.
	LM-ONCE = 1	Level metering is executed only once. To start the levelmeter again, the LM-EN bit must again be set from 0 to 1.
LM-MASK	Interrupt masking for level metering.	
	LM-MASK = 0	An interrupt is generated after level metering.
	LM-MASK = 1	No interrupt is generated.
DC-AD16	Additional digital amplification in the DC AD path for level metering.	
	DC-AD16 = 0	Additional gain factor 16 disabled.
	DC-AD16 = 1	Additional gain factor 16 enabled.

$1D_H$	LMCR2	Level Metering Configuration Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	LM-NOTCH	LM-FILT	LM-RECT	RAMP-EN	LM-SEL[3:0]			

LM-NOTCH Selection of a notch filter instead of the band-pass filter for level metering.

LM-NOTCH = 0	Notch filter selected.
LM-NOTCH = 1	Band-pass filter selected.

LM-FILT Enabling of a programmable band-pass or notch filter for level metering.

LM-FILT = 0	Normal operation.
LM-FILT = 1	Band-pass/notch filter enabled.

LM-RECT Rectifier in DC level meter

LM-RECT = 0	Rectifier disabled.
LM-RECT = 1	Rectifier enabled.

RAMP-EN The ramp generator works together with the RNG-OFFSET bits in LMCR3 and the LM-EN bit to create different voltage slopes in the DC-Path.

RAMP-EN = 0	Ramp generator disabled.
RAMP-EN = 1	Ramp generator enabled.

LM-SEL[3:0] Selection of the source for the level metering.

LM-SEL[3:0] = 0 0 0 0	AC level metering in transmit
LM-SEL[3:0] = 0 0 0 1	Real part of TTX (TTX_{REAL})
LM-SEL[3:0] = 0 0 1 0	Imaginary part of TTX (TTX_{IMG})
LM-SEL[3:0] = 0 0 1 1	Not used
LM-SEL[3:0] = 0 1 0 0	DC out voltage on DCN-DCP
LM-SEL[3:0] = 0 1 0 1	DC current on IT
LM-SEL[3:0] = 0 1 1 0	AC level metering in receive

LM-SEL[3:0] = 0 1 1 1	AC level metering in receive and transmit
LM-SEL[3:0] = 1 0 0 0	Not used
LM-SEL[3:0] = 1 0 0 1	DC current on IL
LM-SEL[3:0] = 1 0 1 0	Voltage on IO3
LM-SEL[3:0] = 1 0 1 1	Voltage on IO4
LM-SEL[3:0] = 1 1 0 0	Not used
LM-SEL[3:0] = 1 1 0 1	V_{DD}
LM-SEL[3:0] = 1 1 1 0	Offset of DC-Prefi (short circuit on DC-Prefi input)
LM-SEL[3:0] = 1 1 1 1	Voltage on IO4 – IO3

1E$_H$	**LMCR3**	Level Metering Configuration Register 3	**00$_H$**		**Y**

Bit	7	6	5	4	3	2	1	0
	AC-SHORT-EN	**RTR-SEL**	**LM-ITIME[3:0]**				**RNG-OFFSET[1:0]**	

AC-SHORT-EN The input pin ITAC will be set to a lower input impedance so that the capacitor C_{ITAC} can be recharged faster during a soft reversal which makes it more silent during conversation.

AC-SHORT-EN = 0	Input impedance of the ITAC pin is standard.
AC-SHORT-EN = 1	Input impedance of the ITAC pin is lowered.

RTR-SEL Ring Trip method selection.

RTR-SEL = 0	Ring Trip with a DC offset is selected.
RTR-SEL = 1	AC Ring Trip is selected. Recommended for short lines only.

LM-ITIME[3:0] Integration Time for AC Level Metering.

LM-ITIME[3:0] = 0 0 0 0	16 ms
LM-ITIME[3:0] = 0 0 0 1	2 × 16 ms
LM-ITIME[3:0] = 0 0 1 0	3 × 16 ms
…	
LM-ITIME[3:0] = 1 1 1 1	16 × 16 ms

RNG-OFFSET[1:0] Selection of the Ring Offset source.

RNG-OFFSET[1:0]	Ring Offset Voltage in Given Mode		
	Active ACTH ACTL	Active Ring ACTR	Ring Pause Ringing
0 0	Voltage given by DC regulation	Voltage given by DC regulation	Ring Offset RO1 Hook Threshold Ring
0 1	Ring Offset RO1/2 (no DC regulation)	Ring Offset RO1 (no DC regulation)	Ring Offset RO1 Hook Threshold Ring
1 0	Ring Offset RO2/2 (no DC regulation)	Ring Offset RO2 (no DC regulation)	Ring Offset RO2 Hook Message Waiting
1 1	Ring Offset RO3/2 (no DC regulation)	Ring Offset RO3 (no DC regulation)	Ring Offset RO3 Hook Message Waiting

By setting the RAMP_EN bit to 1, the ramp generator is started by setting LM_EN from 0 to 1 (see **Figure 71**).
Exception: Transition of RNG-OFFSET from 10 to 11 or 11 to 10 where the ramp generator is started automatically (see **Figure 71**).

For Ring Offset RO1 the usual "Hook Threshold Ring" is used. Using Ring Offset RO2 or RO3 in any ringing mode (Ringing and Ring Pause) also changes the hook thresholds. In this case the "Hook Message Waiting" threshold is used automatically.

When using the Ring Offsets RO2 and RO3 for Message Waiting an additional lamp current is expected. In this case the Hook Message Waiting threshold should be programmed higher than the Hook Threshold Ring.

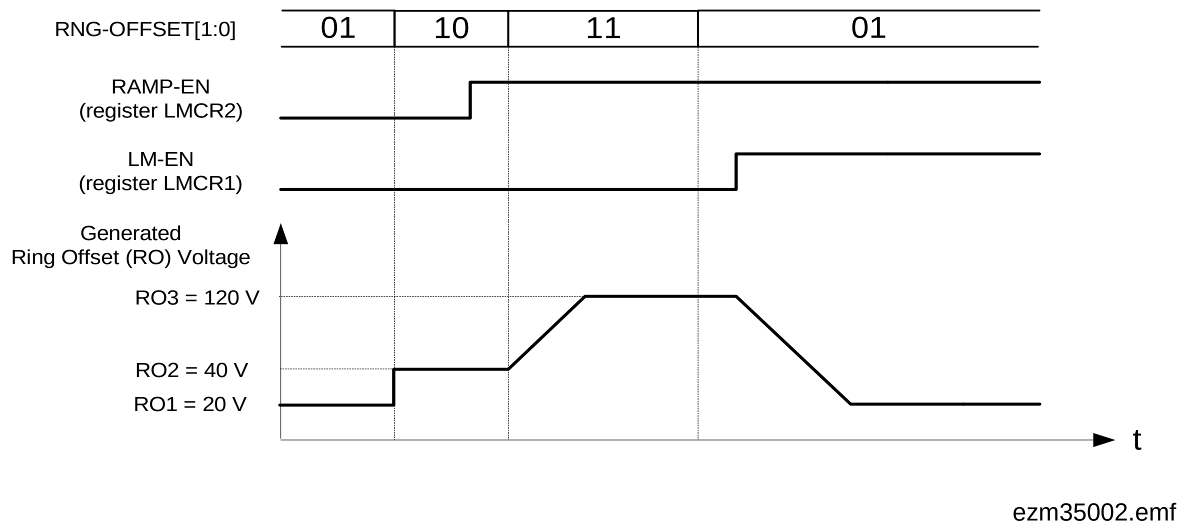

RNG-OFFSET[1:0]
01
10
11
01
RAMP-EN
(register LMCR2)
LM-EN
(register LMCR1)
Generated
Ring Offset (RO) Voltage
RO3 = 120 V
RO2 = 40 V
RO1 = 20 V
t
ezm35002.emf

Figure 71 Example for Switching Between Different Ring Offset Voltages

The three programmable Ring Offsets are typically used for the following purposes:

Table 50 Typical Usage for the three Ring Offsets

Ring Offset Voltage	Application
Ring Offset RO1	Ringing
Ring Offset RO2	Low voltage for message waiting lamp
Ring Offset RO3	High voltage for message waiting lamp

Besides the typical usage described in **Table 50** the Ring Offsets RO1, RO2 and RO3 can also be used for the generation of different custom waveforms (see **Figure 71**).

$1F_H$	**OFR1**	Offset Register 1 (High Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-H[7:0]							

OFFSET-H[7:0]	Offset register high byte.

20_H	**OFR2**	Offset Register 2 (Low Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-L[7:0]							

OFFSET-L[7:0]	Offset register low byte. The value of this register together with OFFSET-H is added to the input of the DC loop to compensate a given offset of the current sensors in the SLIC-E/-E2/-P.

21_H	**PCMR1**	PCM Receive Register 1	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	R1-HW	**R1-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

R1-HW Selection of the PCM highway for receiving PCM data or the higher byte of the first data sample if a linear 16-kHz PCM mode is selected.

R1-HW = 0	PCM highway A is selected.
R1-HW = 1	PCM highway B is selected.

R1-TS[6:0] Selection of the PCM time slot used for data reception.

Note: The programmed PCM time slot must correspond to the available slots defined by the PCLK frequency. No reception will occur if a slot outside the actual numbers of slots is programmed. In linear mode (bit LIN = 1 in register BCR3) R1-TS defines the first of two consecutive slots used for reception.

22_H	**PCMR2**	PCM Receive Register 2	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	R2-HW	**R2-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

R2-HW Selection of the PCM highway for receiving conferencing data for conference channel B or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

R2-HW = 0	PCM highway A is selected.
R2-HW = 1	PCM highway B is selected.

R2-TS[6:0] Selection of the PCM time slot used for receiving data (see description of PCMR1 register).

23_H	**PCMR3**	PCM Receive Register 3	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	R3-HW	**R3-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

R3-HW Selection of the PCM highway for receiving conferencing data for conference channel C or the higher byte of the second data sample if a linear 16-kHz PCM mode is selected.

R3-HW = 0	PCM highway A is selected.
R3-HW = 1	PCM highway B is selected.

R3-TS[6:0] Selection of the PCM time slot used for receiving data (see description of PCMR1 register).

24_H	**PCMR4**	PCM Receive Register 4	00_H		**Y**

Bit	7	6	5	4	3	2	1	0
	R4-HW	**R4-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

R4-HW	Selection of the PCM highway for receiving conferencing data for conference channel D or the lower byte of the second data sample if alinear 16-kHz PCM mode is selected.

R4-HW = 0 PCM highway A is selected.

R4-HW = 1 PCM highway B is selected.

R4-TS[6:0]	Selection of the PCM time slot used for receiving data (see description of PCMR1 register).

25_H	**PCMX1**	PCM Transmit Register 1	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	X1-HW	**X1-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

X1-HW Selection of the PCM highway for transmitting PCM data or the higher byte of the first data sample if a linear 16-kHz PCM mode is selected.

X1-HW = 0	PCM highway A is selected.
X1-HW = 1	PCM highway B is selected.

X1-TS[6:0] Selection of the PCM time slot used for data transmission.

Note: The programmed PCM time slot must correspond to the available slots defined by the PCLK frequency. No transmission will occur if a slot outside the actual numbers of slots is programmed. In linear mode X1-TS defines the first of two consecutive slots used for transmission. PCM data transmission is controlled by the bits 6 through 2 in register BCR3.

26_H	**PCMX2**	PCM Transmit Register 2	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	X2-HW	**X2-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

X2-HW Selection of the PCM highway for transmitting conferencing data for conference channel C + S or C + D or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

X2-HW = 0	PCM highway A is selected.
X2-HW = 1	PCM highway B is selected.

X2-TS[6:0] Selection of the PCM time slot used for transmitting data (see description of PCMX1 register).

27_H	**PCMX3**	PCM Transmit Register 3	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	X3-HW	**X3-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

X3-HW Selection of the PCM highway for transmitting conferencing data for conference channel B + S or B + D or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

X3-HW = 0 PCM highway A is selected.

X3-HW = 1 PCM highway B is selected.

X3-TS[6:0] Selection of the PCM time slot used for transmitting data (see description of PCMX1 register).

28_H	**PCMX4**	PCM Transmit Register 4	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	X4-HW	**X4-TS[6:0]**						

This register is not applicable and not used in IOM-2 mode. Only enabled in PCM/µC mode.

X4-HW	Selection of the PCM highway for transmitting conferencing data for conference channel B + C or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

X4-HW = 0 PCM highway A is selected.

X4-HW = 1 PCM highway B is selected.

X4-TS[6:0]	Selection of the PCM time slot used for transmitting data (see description of PCMX1 register).

29_H	**TSTR1**	Test Register 1	00_H	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	PD-AC-PR	**PD-AC-PO**	**PD-AC-AD**	**PD-AC-DA**	**PD-AC-GN**	**PD-GNKC**	**PD-OFHC**	**PD-OVTC**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

PD-AC-PR AC-PREFI power down

PD-AC-PR = 0 Normal operation.

PD-AC-PR = 1 Power Down mode.

PD-AC-PO AC-POFI power down

PD-AC-PO = 0 Normal operation.

PD-AC-PO = 1 Power Down mode.

PD-AC-AD AC-ADC power down

PD-AC-AD = 0 Normal operation.

PD-AC-AD = 1 Power Down mode, transmit path is inactive.

PD-AC-DA AC-DAC power down

PD-AC-DA = 0 Normal operation.

PD-AC-DA = 1 Power Down mode, receive path is inactive.

PD-AC-GN AC-Gain power down

PD-AC-GN = 0 Normal operation.

PD-AC-GN = 1 Power Down mode.

PD-GNKC Groundkey comparator (GNKC) is set to power down

PD-GNKC = 0 Normal operation.

PD-GNKC = 1 Power Down mode.

PD-OFHC	Off-hook comparator (OFHC) power down	
	PD-OFHC = 0	Normal operation.
	PD-OFHC = 1	Power Down mode.
PD-OVTC	Overtemperature comparator (OVTC) power down	
	PD-OVTC = 0	Normal operation.
	PD-OVTC = 1	Power Down mode.

$2A_H$	**TSTR2**	Test Register 2	**00_H**	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	PD-DC-PR	**0**	**PD-DC-AD**	**PD-DC-DA**	**PD-DCBUF**	**0**	**PD-TTX-A**	**PD-HVI**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

PD-DC-PR	DC-PREFI power down	
	PD-DC-PR = 0	Normal operation.
	PD-DC-PR = 1	Power Down mode.
PD-DC-AD	DC-ADC power down	
	PD-DC-AD = 0	Normal operation.
	PD-DC-AD = 1	Power Down mode, transmit path is inactive.
PD-DC-DA	DC-DAC power down	
	PD-DC-DA = 0	Normal operation.
	PD-DC-DA = 1	Power Down mode, receive path is inactive.
PD-DCBUF	DC-BUFFER power down	
	PD-DCBUF = 0	Normal operation.
	PD-DCBUF = 1	Power Down mode.
PD-TTX-A	TTX Adaptation DAC and POFI power down	
	PD-TTX-A = 0	Normal operation.
	PD-TTX-A = 1	Power Down mode.
PD-HVI	HV interface (to SLIC-E/-E2/-P) power down	
	PD-HVI = 0	Normal operation.
	PD-HVI = 1	Power Down mode.

$2B_H$	**TSTR3**	Test Register 3	**00_H**	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**AC-DLB-4M**	**AC-DLB-128K**	**AC-DLB-32K**	**AC-DLB-8K**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

AC-DLB-4M AC digital loop via a 4-MHz bitstream. (Loop encloses all digital hardware in the AC path. Together with DLB-DC, a pure digital test is possible because there is no influence from the analog hardware.)

AC-DLB-4M = 0 Normal operation.

AC-DLB-4M = 1 Digital loop closed.

AC-DLB-128K AC digital loop via 128 kHz

AC-DLB-128K = 0 Normal operation.

AC-DLB-128K = 1 Digital loop closed.

AC-DLB-32K AC digital loop via 32 kHz

AC-DLB-32K = 0 Normal operation.

AC-DLB-32K = 1 Digital loop closed.

AC-DLB-8K AC digital loop via 8 kHz

AC-DLB-8K = 0 Normal operation.

AC-DLB-8K = 1 Digital loop closed.

$2C_H$	TSTR4	Test Register 4	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	OPIM-AN	**OPIM-4M**	**COR-64**	**COX-16**	**0**	**0**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

OPIM-AN Open Impedance Matching Loop in the analog part.

OPIM-AN = 0	Normal operation.
OPIM-AN = 1	Loop opened.

OPIM-4M Open fast digital Impedance Matching Loop in the hardware filters.

OPIM-4M = 0	Normal operation.
OPIM-4M = 1	Loop opened.

COR-64 Cut off the AC receive path at 64 kHz (just before the IM filter).

COR-64 = 0	Normal operation.
COR-64 = 1	Receive path is cut off.

COX-16 Cut off the AC transmit path at 16 kHz. (The TH filter can be tested without influencing the analog part.)

COX-16 = 0	Normal operation.
COX-16 = 1	Transmit path is cut off.

$2D_H$	**TSTR5**	Test Register 5	**00_H**	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**DC-POFI-HI**	**DC-HOLD**	**0**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

DC-POFI-HI Higher value for DC post filter limit

DC-POFI-HI = 0	Limit frequency is set to 100 Hz (normal operation).
DC-POFI-HI = 1	Limit frequency is set to 300 Hz.

DC-HOLD Actual DC output value hold (value of the last DSP filter stage will be kept)

DC-HOLD = 0	Normal operation.
DC-HOLD = 1	DC output value hold.

6.2.2 COP Command

The COP command gives access to the CRAM data of the DSPs. It is organized in the same way as the SOP command. The offset value allows a direct as well as a block access to the CRAM. Writing beyond the allowed offset will be ignored, reading beyond it will give unpredictable results.
The value of a specific CRAM coefficient is calculated by the DuSLICOS software.

Bit	7	6	5	4	3	2	1	0
Byte 1	**RD**	**1**	**ADR[2:0]**			**1**	**0**	**1**
Byte 2	**OFFSET[7:0]**							

RD Read Data

RD = 0 Write data to chip.

RD = 1 Read data from chip.

ADR[2:0] Channel address for the subsequent data

ADR[2:0] = 0 0 0 Channel A

ADR[2:0] = 0 0 1 Channel B

(other codes reserved for future use)

Offset [7:0]	Short Name	Long Name
00_H	TH1	Transhybrid Filter Coefficients Part 1
08_H	TH2	Transhybrid Filter Coefficients Part 2
10_H	TH3	Transhybrid Filter Coefficients Part 3
18_H	FRR	Frequency-response Filter Coefficients Receive Direction
20_H	FRX	Frequency-response Filter Coefficients Transmit Direction
28_H	AR	Amplification/Attenuation Stage Coefficients Receive
30_H	AX	Amplification/Attenuation Stage Coefficients Transmit
38_H	PTG1	Tone Generator 1 Coefficients
40_H	PTG2	Tone Generator 2 Coefficients
48_H	LPR	Low Pass Filter Coefficients Receive
50_H	LPX	Low Pass Filter Coefficients Transmit
58_H	TTX	Teletax Coefficients
60_H	IM1	Impedance Matching Filter Coefficients Part 1
68_H	IM2	Impedance Matching Filter Coefficients Part 2
70_H	RINGF	Ringer Frequency and Amplitude Coefficients (DC loop)
78_H	RAMPF	Ramp Generator Coefficients (DC loop)
80_H	DCF	DC Characteristics Coefficients (DC loop)
88_H	HF	Hook Threshold Coefficients (DC loop)
90_H	TPF	Low-pass Filter Coefficients (DC loop)
98_H		Reserved

Table 51 CRAM Coefficients

<table>
<tr><th colspan="2">Byte 7</th><th colspan="2">Byte 6</th><th colspan="2">Byte 5</th><th colspan="2">Byte 4</th><th colspan="2">Byte 3</th><th colspan="2">Byte 2</th><th colspan="2">Byte 1</th><th colspan="2">Byte 0</th><th colspan="2">Offset [7:0]</th></tr>
<tr><td colspan="16">Transhybrid Coefficient Part 1</td><td>00_H</td><td>TH1</td></tr>
<tr><td></td><td colspan="15">Transhybrid Coefficient Part 2</td><td>08_H</td><td>TH2</td></tr>
<tr><td></td><td></td><td colspan="14">Transhybrid Coefficient Part 3</td><td>10_H</td><td>TH3</td></tr>
<tr><td></td><td colspan="15">FIR Filter in Receive Direction</td><td>18_H</td><td>FRR</td></tr>
<tr><td></td><td colspan="15">FIR Filter in Transmit Direction</td><td>20_H</td><td>FRX</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td colspan="3">LM Threshold</td><td colspan="3">2nd Gain Stage Receive</td><td colspan="5">1st Gain Stage Receive</td><td>28_H</td><td>AR</td></tr>
<tr><td colspan="5">Bandpass for AC LM</td><td colspan="2">Conference Gain</td><td>LM-AC</td><td colspan="3">2nd Gain Stage Transmit</td><td colspan="5">1st Gain Stage Transmit</td><td>30_H</td><td>AX</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td colspan="5">TG1 Bandpass</td><td colspan="3">TG1 Gain</td><td colspan="3">TG1 Frequency</td><td>38_H</td><td>PTG1 $^{1)}$</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td colspan="5">TG2 Bandpass</td><td colspan="3">TG2 Gain</td><td colspan="3">TG2 Frequency</td><td>40_H</td><td>PTG2 $^{1)}$</td></tr>
<tr><td></td><td colspan="15">LPR</td><td>48_H</td><td>LPR $^{2)}$</td></tr>
<tr><td></td><td colspan="15">LPX</td><td>50_H</td><td>LPX $^{2)}$</td></tr>
<tr><td></td><td></td><td></td><td colspan="6">FIR Filter for TTX</td><td></td><td></td><td colspan="2">TTX Slope</td><td colspan="3">TTX Level</td><td>58_H</td><td>TTX</td></tr>
<tr><td></td><td></td><td colspan="2">IM K Factor</td><td colspan="12">IM FIR Filter</td><td>60_H</td><td>IM1_F</td></tr>
<tr><td></td><td></td><td colspan="4">IM 4 MHz Filter</td><td></td><td colspan="9">IM WDF Filter</td><td>68_H</td><td>IM2_F</td></tr>
<tr><td></td><td colspan="3">LM DC Gain</td><td colspan="3">Ring Generator Amplitude</td><td colspan="3">Ring Generator Frequency</td><td colspan="3">Ring Generator Low-pass</td><td colspan="3">Ring Offset RO1</td><td>70_H</td><td>RINGF</td></tr>
<tr><td></td><td></td><td colspan="2">Extended Battery Feeding Gain</td><td colspan="3">Soft Reversal End</td><td colspan="3">Constant Ramp CR</td><td colspan="3">Soft Ramp SS</td><td colspan="3">Ring Delay RD</td><td>78_H</td><td>RAMPF</td></tr>
<tr><td colspan="3">Res. in Resistive Zone R_{K12}</td><td colspan="3">Res. in Constant Current Zone R_I</td><td colspan="4">Constant Current I_{K1}</td><td colspan="3">Knee Voltage V_{K1}</td><td colspan="3">Open Circuit Volt. V_{LIM}</td><td>80_H</td><td>DCF</td></tr>
<tr><td></td><td colspan="3">Hook Message Waiting</td><td colspan="3">Hook Threshold AC Ringtrip</td><td colspan="3">Hook Threshold Ring</td><td colspan="3">Hook Threshold Active</td><td colspan="3">Hook Threshold Power Down</td><td>88_H</td><td>HF</td></tr>
<tr><td colspan="3">Ring Offset RO3</td><td colspan="3">Ring Offset RO2</td><td colspan="3">Voltage Level VRT</td><td colspan="3">DC Low-pass Filter TP2</td><td colspan="4">DC Low-pass Filter TP1</td><td>90_H</td><td>TPF</td></tr>
<tr><td colspan="16">Reserved</td><td>98_H</td><td></td></tr>
<tr><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td></td><td></td></tr>
</table>

Note: CRAM coefficients are enabled by setting bit CRAM-EN in register BCR3 to 1, except coefficients marked $^{1)}$ and $^{2)}$:
Coefficients market $^{1)}$ are enabled by setting bit PTG in register DSCR to 1.
Coefficients market $^{2)}$ are enabled by setting bit LPRX-CR in register BCR3 to 1.

6.2.2.1 CRAM Programming Ranges

Table 52 CRAM Programming Ranges

Parameter	Programming Range
Constant Current I_{K1}	0...50 mA, Δ < 0.5 mA
Hook Message Waiting, Hook Thresholds	0..25 mA, Δ < 0.7 mA 25...50 mA, Δ < 1.3 mA
Ring Generator Frequency f_{RING}	3..40 Hz, Δ < 1 Hz 40..80 Hz, Δ < 2 Hz > 80 Hz, Δ < 4 Hz
Ring Generator Amplitude	0..20 V, Δ < 1.7 V 20..85 V, Δ < 0.9 V
Ring Offset RO1, RO2, RO3	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V 50..100 V, Δ < 2.4 V, max. 150 V
Knee Voltage V_{K1}, Open Circuit Voltge V_{LIM}	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V > 50 V, Δ < 2.4 V
Resistance in Resistive Zone R_{K12}	0..1000 Ω, Δ < 30 Ω
Resistance in Constant Current Zone R_I	1.8 kΩ..4.8 kΩ, Δ < 120 Ω 4.8 kΩ..9.6 kΩ, Δ < 240 Ω 9.6 kΩ..19 kΩ, Δ < 480 Ω 19 kΩ..38 kΩ, Δ < 960 Ω, max. 40 kΩ

6.2.3 POP Command

The POP command provides access to the EDSP registers of the SLICOFI-2.

Before using an EDSP function the according POP registers have to be programmed.

Any change in any of the POP registers (except registers CIS-DAT and CIS/LEC-MODE) is only updated with enabling the corresponding device. For example a change of the center frequency f_C of the UTD is handled by changing the registers UTD-CF-H and UTD-CF-L, switching off the UTD and switching it on again.

The POP registers do no have default values after any kind of reset.

6.2.3.1 POP Register Overview

00_H CIS-DAT Caller ID Sender Data Buffer (write-only)

30_H DTMF-LEV DTMF Receiver Level Byte

0	b	e

31_H DTMF-TWI DTMF Receiver Twist Byte

TWI

32_H DTMF-NCF-H DTMF Receiver Notch Filter Center Frequency High Byte

NCF-H

33_H DTMF-NCF-L DTMF Receiver Notch Filter Center Frequency Low Byte

NCF-L

34_H DTMF-NBW-H DTMF Receiver Notch Filter Bandwidth High Byte

NBW-H

35_H DTMF-NBW-L DTMF Receiver Notch Filter Bandwidth Low Byte

NBW-L

36_H DTMF-GAIN Gain Stage Control for DTMF Input Signal

e	m

37_H	DTMF-RES1	DTMF Receiver Reserved Byte 1

38_H	DTMF-RES2	DTMF Receiver Reserved Byte 2

39_H	DTMF-RES3	DTMF Receiver Reserved Byte 3

$3A_H$	LEC-LEN	Line Echo Canceller Length

LEN

$3B_H$	LEC-POWR	Line Echo Canceller Power Detection Level

POWR

$3C_H$	LEC-DELP	Line Echo Canceller Delta Power

DELP

$3D_H$	LEC-DELQ	Line Echo Canceller Delta Quality

DELQ

$3E_H$	LEC-GAIN-XI	Line Echo Canceller Input Gain Transmit

e	m

$3F_H$	LEC-GAIN-RI	Line Echo Canceller Input Gain Receive

e	m

40_H	LEC-GAIN-XO	Line Echo Canceller Output Gain Transmit

e	m

41_H	LEC-RES1	Line Echo Canceller Reserved Byte 1

42_H LEC-RES2 Line Echo Canceller Reserved Byte 2

43_H CIS-LEV-H Caller ID Sender Level High Byte

LEV-H

44_H CIS-LEV-L Caller ID Sender Level Low Byte

LEV-L

45_H CIS-BRS Caller ID Sender Buffer Request Size

BRS

46_H CIS-SEIZ-H Caller ID Sender Number of Seizure Bits High Byte

SEIZ-H

47_H CIS-SEIZ-L Caller ID Sender Number of Seizure Bits Low Byte

SEIZ-L

48_H CIS-MARK-H Caller ID Sender Number of Mark Bits High Byte

MARK-H

49_H CIS-MARK-L Caller ID Sender Number of Mark Bits Low Byte

MARK-L

$4A_H$ CIS/LEC-MODE CIS/LEC Mode Setting

LEC-ADAPT	LEC-FREZE	UTDX-SUM	UTDR-SUM	0	0	CIS-FRM	CIS-V23

$4B_H$ UTD-CF-H Universal Tone Detection Center Frequency High Byte

CF-H

$4C_H$ UTD-CF-L Universal Tone Detection Center Frequency Low Byte

CF-L

$4D_H$	UTD-BW-H	Universal Tone Detection Bandwidth High Byte
	BW-H	

$4E_H$	UTD-BW-L	Universal Tone Detection Bandwidth Low Byte
	BW-L	

$4F_H$	UTD-NLEV	Universal Tone Detection Noise Level
	NLEV	

50_H	UTD-SLEV-H	Universal Tone Detection Signal Level High Byte
	SLEV-H	

51_H	UTD-SLEV-L	Universal Tone Detection Signal Level Low Byte
	SLEV-L	

52_H	UTD-DELT	Universal Tone Detection Delta
	DELT-H	

53_H	UTD-RBRK	Universal Tone Detection Recognition Break Time
	RBRK	

54_H	UTD-RTIME	Universal Tone Detection Recognition Time
	RTIME	

55_H	UTD-EBRK	UTD Allowed Tone End Detection Break Time
	EBRK	

56_H	UTD-ETIME	UTD Tone End Detection Time
	ETIME	

6.2.4 POP Register Description

00_H	**CIS-DAT**	Caller ID Sender Data Buffer (write-only)			**Y**

<table>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td></td><td colspan="8">Byte 0</td></tr>
<tr><td></td><td colspan="8">Byte 1</td></tr>
<tr><td></td><td colspan="8">Byte 2</td></tr>
<tr><td></td><td colspan="8">⋮</td></tr>
<tr><td></td><td colspan="8">Byte 47</td></tr>
</table>

30_H	**DTMF-LEV**	DTMF Receiver Level Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	0			**b**		**e**		

Minimum DTMF Signal Detection Level $\text{Level}_{\text{DTMFdet}}$

- for DTMF detection in transmit:

  $\text{Level}_{\text{DTMFdet}}[\text{dB}] = \text{Level}_{\text{DTMFdet}}[\text{dBm0}] - 3.14 + G_{\text{DTMF}}[\text{dB}]$

  $\text{Level}_{\text{DTMFdet}}[\text{dB}] = \text{Level}_{\text{DTMFdet}}[\text{dBm}] - L_X[\text{dBr}] - 3.14 + G_{\text{DTMF}}[\text{dB}]$

- for DTMF detection in receive:

  $\text{Level}_{\text{DTMFdet}}[\text{dB}] = \text{Level}_{\text{DTMFdet}}[\text{dBm0}] - 3.14 + \text{AR1}[\text{dB}] + G_{\text{DTMF}}[\text{dB}]$

  $\text{Level}_{\text{DTMFdet}}[\text{dB}] = \text{Level}_{\text{DTMFdet}}[\text{dBm}] - L_R[\text{dBr}] - 3.14 + \text{AR1}[\text{dB}] + G_{\text{DTMF}}[\text{dB}]$

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file;
approximate value AR1 $\approx L_R$ for $L_R \leq -2$ dBr, AR1 ≈ -2 dB for $L_R > -2$ dBr.

$\text{Level}_{\text{DTMFdet}}[\text{dB}] = -30 - b - 3 \times e[\text{dB}]$

$-54\ \text{dB} \leq \text{Level}_{\text{DTMFdet}} \leq -30\ \text{dB}$

with

$0 \leq e \leq 7$

$0 \leq b \leq 3$

Alternative representation

$b = \text{MOD}[(-\text{Level}_{\text{DTMFdet}}[\text{dB}] - 30),3]$

$e = \text{INT}[(-\text{Level}_{\text{DTMFdet}}[\text{dB}] - 30)/3]$

Note: MOD = Modulo function, INT = Integer function

31_H	**DTMF-TWI**	DTMF Receiver Twist Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	TWI							

DTMF Receiver Twist is the maximum allowed difference between the signal levels of the two tones for DTMF detection:

$$\mathrm{TWI[dB]} = 2 \times \mathrm{Twist}_{acc}\mathrm{[dB]}$$

$$0\ \mathrm{dB} \leq \mathrm{Twist}_{acc} \leq 12\ \mathrm{dB}$$

32_H	**DTMF-NCF-H**	DTMF Receiver Notch Filter Center Frequency High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	NCF-H							

33_H	**DTMF-NCF-L**	DTMF Receiver Notch Filter Center Frequency Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	NCF-L							

DTMF Receiver Notch Filter Center Frequency:

$$NCF = 32768 \times \cos\left(2\pi \frac{f_{NCF}[Hz]}{8000}\right) = NCF\text{-}L + 256 \times NCF\text{-}H$$

$$0\ Hz \le f_{NCF} \le 2000\ Hz$$

The bytes are calculated as follows:

NCF-L = MOD (NCF,256) = NCF & 0x00FF

NCF-H = INT (NCF/256) = NCF >> 8

The echo of the dial tone can activate the double talk detection which means that the DTMF tone will not be detected. Therefore a notchfilter can be programmed to filter out the echo of the dialtone, because the frequency of the dialtone is known. The center frequency and the bandwith of the notch filter can be programmed.

34_H	**DTMF-NBW-H**	DTMF Receiver Notch Filter Bandwidth High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	NBW-H							

35_H	**DTMF-NBW-L**	DTMF Receiver Notch Filter Bandwidth Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	NBW-L							

DTMF Receiver Notch Filter Bandwidth:

$$\mathrm{NBW} = 65536 \times \frac{a}{1+a} = \mathrm{NBW\text{-}L} + 256 \times \mathrm{NBW\text{-}H}$$

with

$$a = \tan\left(\pi \cdot \frac{F_{NBW}[\mathrm{Hz}]}{8000}\right)$$

$$0\ \mathrm{Hz} \leq F_{NBW} \leq 2000\ \mathrm{Hz}$$

NBW_L = MOD (NBW,256)

NBW_H = INT (NBW/256)

36_H	**DTMF-GAIN**	Gain Stage Control for DTMF Input Signal			**Y**

Bit	7	6	5	4	3	2	1	0
	e			**m**				

DTMF Input Signal Gain:

$G_{DTMF}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$

$-24.08\ dB \leq G_{DTMF} \leq 23.95\ dB$

with

$g = 2^{(9-e)}\ (32 + m)$ and

$0 \leq m \leq 31,\quad 0 \leq e \leq 7$

Table 53 Ranges of G_{DTMF}[dB] dependent on “e”

e	**DTMF Input Signal Gain G_{DTMF} [dB] Range**
0	$23.95\ dB \geq G_{DTMF} \geq 18.06\ dB$
1	$17.93\ dB \geq G_{DTMF} \geq 12.04\ dB$
7	$-18.20\ dB \geq G_{DTMF} \geq -24.08\ dB$

Alternative representation:

Choose "e" as the next integer number which is bigger than or equal to:

$$e \geq 3 - \log_2 G_{DTMF} = 3 - \frac{\log_{10} G_{DTMF}}{\log_{10} 2} \approx 3 - \frac{G_{DTMF}[dB]}{6.02}$$

$$m = G_{DTMF} \times 2^{2+e} - 32 = 10^{\frac{G_{DTMF}[dB]}{20}} \times 2^{2+e} - 32$$

Table 54 Example for DTMF-GAIN Calculation

G_{DTMF}[dB]	G_{DTMF}	**e**	**m**	**DTMF-GAIN**
0	1	3	0	0x60
– 6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

37_H	**DTMF-RES1**	DTMF Receiver Reserved Byte 1			**Y**

Bit	7	6	5	4	3	2	1	0

38_H	**DTMF-RES2**	DTMF Receiver Reserved Byte 2			**Y**

Bit	7	6	5	4	3	2	1	0

39_H	**DTMF-RES3**	DTMF Receiver Reserved Byte 3			**Y**

Bit	7	6	5	4	3	2	1	0

$3A_H$	**LEC-LEN**	Line Echo Canceller Length			**Y**

Bit	7	6	5	4	3	2	1	0
	LEN							

Line Echo Canceller Length:

LEN = LEC Length[ms] / 0.125

LEC Length has to be entered in multiples of 0.125 ms.

The selected LEC Length has to be higher than the maximum line echo length but not higher than 8 ms.

Table 6-1 LEC Length

LEN	**LEC Length**
1	0.125 ms
…	
64	8 ms

$3B_H$	**LEC-POWR**	Line Echo Canceller Power Detection Level			**Y**

Bit	7	6	5	4	3	2	1	0
	POWR							

Minimum Power Detection Level for Line Echo Canceller:

$Pow_{LECR}[dB] = S_{R,LEC\text{-}POWR}[dBm0] - 3.14 + AR1[dB] + G_{LEC\text{-}RI}[dB] - 20*\log_{10}(\pi/2)$

$S_{R,LEC\text{-}POWR}[dBm0]$: Minimum Power Detection Level for Line Echo Canceller at digital input

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file;
approximate value $AR1 \approx L_R$ for $L_R \leq -2$ dBr, $AR1 \approx -2$ dB for $L_R > -2$ dBr.

$$POWR = (6.02 \times 16 + Pow_{LECR}[dB]) \times 2 / (5 \times \log_{10}2)$$
$$= (96.32 + Pow_{LECR}[dB]) \times 1.329$$

$-96\ dB \leq Pow_{LECR} \leq 0\ dB$

Table 55 Characteristic Values

POWR	**Pow_{LECR}[dB]**
0x00	– 96
…	
0x7F	0

Example:

AR1 = – 3 dB

$S_{R,LEC\text{-}POWR} = -40$ dBm0

$Pow_{LECR} = -46.14$ dB

$POWR = 66.69 \approx 67 = 0x43$

$3C_H$	**LEC-DELP**	Line Echo Canceller Delta Power			**Y**

Bit	7	6	5	4	3	2	1	0
	DELP							

Line Echo Canceller Delta Power for Double Talk Detection (DTD):

$\text{DeltaP}_{\text{LEC}}[\text{dB}] = (S_R - S_X)_{\text{DTDThr}}[\text{dB}] + \text{AR1}[\text{dB}] + G_{\text{LEC-RI}}[\text{dB}] - G_{\text{LEC-XI}}[\text{dB}]$

$(S_R - S_X)_{\text{DTDThr}}[\text{dB}]$: Double Talk Detection threshold

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file;
approximate value $\text{AR1} \approx L_R$ for $L_R \leq -2$ dBr, $\text{AR1} \approx -2$ dB for $L_R > -2$ dBr.

$\text{DELP} = \text{DeltaP}_{\text{LEC}}[\text{dB}] \times 2/5 \times \log_{10}2 = \text{DeltaP}_{\text{LEC}}[\text{dB}] \times 1.329$

$-96 \text{ dB} \leq \text{DeltaP}_{\text{LEC}} \leq 96 \text{ dB}$

Table 56 Characteristic Values

DELP	$\text{DeltaP}_{\text{LEC}}$[dB]
0x81	– 96
…	
0x7F	96

Example:

AR1 = – 3 dB

expected echo signal < – 15 dB → $(S_R - S_X)_{\text{DTDThr}} = -15$ dB

$\text{DeltaP}_{\text{LEC}} = 12$ dB

DELP = 16 = 0x10

$3D_H$	**LEC-DELQ**	Line Echo Canceller Delta Quality			**Y**

Bit	7	6	5	4	3	2	1	0
	DELQ							

Line Echo Canceller Delta Quality Between Shadow Filter and Main Filter:

The higher DeltaQ is, the less copying between shadow filter and main filter takes place and the higher is the quality.

DELQ[dB] = DeltaQ[dB] $\times$ 2/5 $\times$ $\log_{10}2$ = DeltaQ[dB] $\times$ 1.329

0 dB $\leq$ DeltaQ $\leq$ 10 dB

Table 57 Characteristic Values

DELQ	DeltaQ[dB]
8	6.02 dB
4	3.01 dB (typical)
3	2.26 dB
2	1.505 dB

$3E_H$	LEC-GAIN-XI	Line Echo Canceller Input Gain Transmit			Y

Bit	7	6	5	4	3	2	1	0
	e			m				

Line Echo Canceller Input Gain Transmit:
It is important, that $G_{LEC\text{-}XI}$[dB] will not be changed, so $G_{LEC\text{-}XI}[dB] = – G_{LEC\text{-}X0}[dB]$

$G_{LEC\text{-}XI}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$

$– 24.08\ dB \leq G_{LEC\text{-}XI} \leq 23.95\ dB$

with
$g = 2^{9-e}\ (32 + m)$ and
$0 \leq m \leq 31,\ 0 \leq e \leq 7$

Table 58 Ranges of $G_{LEC\text{-}XI}$[dB] Dependent on “e”

e	Input Gain $G_{LEC\text{-}XI}$[dB] Range
0	$23.95\ dB \geq G_{LEC\text{-}XI} \geq 18.06\ dB$
1	$17.93\ dB \geq G_{LEC\text{-}XI} \geq 12.04\ dB$
7	$– 18.20\ dB \geq G_{LEC\text{-}XI} \geq – 24.08\ dB$

Alternative representation:

Choose "e" as the next integer number which is bigger than or equal to:

$$e \geq 3 - \log_2 G_{LEC-XI} = 3 - \frac{\log_{10} G_{LEC-XI}}{\log_{10} 2} \approx 3 - \frac{G_{LEC-XI}[dB]}{6.02}$$

$$m = G_{LEC-XI} \times 2^{2+e} - 32 = 10^{\frac{G_{LEC-XI}[dB]}{20}} \times 2^{2+e} - 32$$

Table 59 Example for LEC-GAIN-XI Calculation

$G_{LEC\text{-}XI}$[dB]	$G_{LEC\text{-}XI}$	e	m	LEC-GAIN-XI
0	1	3	0	0x60
– 6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

$3F_H$	**LEC-GAIN-RI**	Line Echo Canceller Input Gain Receive			**Y**

Bit	7	6	5	4	3	2	1	0
		e				**m**		

Line Echo Canceller Input Gain Receive:

$G_{LEC\text{-}RI}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$

$-24.08 \text{ dB} \le G_{LEC\text{-}RI} \le 23.95 \text{ dB}$

with

$g = 2^{9-e}(32 + m)$ and

$0 \le m \le 31, 0 \le e \le 7$

Table 60 Ranges of $G_{LEC\text{-}RI}$[dB] Dependent on “e”

e	**Input Gain $G_{LEC\text{-}RI}$[dB] Range**
0	$23.95 \text{ dB} \ge G_{LEC\text{-}RI} \ge 18.06 \text{ dB}$
1	$17.93 \text{ dB} \ge G_{LEC\text{-}RI} \ge 12.04 \text{ dB}$
7	$-18.20 \text{ dB} \ge G_{LEC\text{-}RI} \ge -24.08 \text{ dB}$

Alternative representation:

Choose "e" as the next integer number which is bigger than or equal to:

$$e \ge 3 - \log_2 G_{LEC-RI} = 3 - \frac{\log_{10} G_{LEC-RI}}{\log_{10} 2} \approx 3 - \frac{G_{LEC-RI}[dB]}{6.02}$$

$$m = G_{LEC-RI} \times 2^{2+e} - 32 = 10^{\frac{G_{LEC-RI}[dB]}{20}} \times 2^{2+e} - 32$$

Table 61 Example for LEC-GAIN-RI Calculation

$G_{LEC\text{-}RI}$[dB]	$G_{LEC\text{-}RI}$	**e**	**m**	**LEC-GAIN-RI**
0	1	3	0	0x60
– 6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

40_H	**LEC-GAIN-XO**	Line Echo Canceller Output Gain Transmit			**Y**

Bit	7	6	5	4	3	2	1	0
		e				**m**		

Line Echo Canceller Output Gain Transmit:
It is important, that $G_{LEC\text{-}X0}$[dB] will not be changed, so $G_{LEC\text{-}X0}[dB] = -G_{LEC\text{-}XI}[dB]$

$$G_{LEC\text{-}X0}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$$

$$-24.08 \text{ dB} \le G_{LEC\text{-}X0} \le 23.95 \text{ dB}$$

with

$g = 2^{9-e}(32 + m)$ and

$0 \le m \le 31,\ 0 \le e \le 7$

Table 62 Ranges of $G_{LEC\text{-}X0}$[dB] Dependent on “e”

e	**Output Gain $G_{LEC\text{-}X0}$[dB] Range**
0	$23.95 \text{ dB} \ge G_{LEC\text{-}X0} \ge 18.06 \text{ dB}$
1	$17.93 \text{ dB} \ge G_{LEC\text{-}X0} \ge 12.04 \text{ dB}$
7	$-18.20 \text{ dB} \ge G_{LEC\text{-}X0} \ge -24.08 \text{ dB}$

Alternative representation:

Choose "e" as the next integer number which is bigger than or equal to:

$$e \ge 3 - \log_2 G_{LEC-X0} = 3 - \frac{\log_{10} G_{LEC-X0}}{\log_{10} 2} \approx 3 - \frac{G_{LEC-X0}[dB]}{6.02}$$

$$m = G_{LEC-X0} \times 2^{2+e} - 32 = 10^{\frac{G_{LEC-X0}[dB]}{20}} \times 2^{2+e} - 32$$

Table 63 Example for LEC-GAIN-X0 Calculation

$G_{LEC\text{-}X0}$[dB]	$G_{LEC\text{-}X0}$	**e**	**m**	**LEC-GAIN-X0**
0	1	3	0	0x60
– 6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

41_H	**LEC-RES1**	Line Echo Canceller Reserved Byte 1			**Y**

Bit	7	6	5	4	3	2	1	0

42_H	**LEC-RES2**	Line Echo Canceller Reserved Byte 2			**Y**

Bit	7	6	5	4	3	2	1	0

43_H	**CIS-LEV-H**	Caller ID Sender Level High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	LEV-H							

44_H	**CIS-LEV-L**	Caller ID Sender Level Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	LEV-L							

Caller ID Sender Level:

$Lev_{CIS}[dB] = Lev_{CIS}[dBm0] - 3.14 - 3.37$

$Lev_{CIS}[dB] = Lev_{CIS}[dBm] - L_R[dBr] - 3.14 - 3.37$

$LEV = 32767 \times 10^{(Lev_{CIS}[dB]/20)}$

$-90.31\ dB \leq Lev_{CIS} \leq 0\ dB$

LEV-L = MOD (LEV,256)

LEV-H = INT (LEV/256)

Table 64 Examples

LEV	**Level [dB]**
0	$-\infty$ (signal off)
1	– 90.31
32767	0

45_H	**CIS-BRS**	Caller ID Sender Buffer Request Size			**Y**

Bit	7	6	5	4	3	2	1	0
	BRS							

Caller ID Sender Buffer Request Size:

$0 \leq BRS \leq 46$

CIS-BRS is a threshold to be set within the Caller ID sender buffer (CIS-DAT, 48 bytes).

If the number of bytes in the CID sender buffer falls below the buffer request size an interrupt is generated. This is the indication to fill up the buffer again.

The first bit will be sent if the number of bytes in the CID sender buffer exceeds the buffer request size (start sending with BRS + 1 number of bytes).

The buffer request size BRS must always be smaller than the number of bytes to be sent:

BRS < Number of bytes to be sent

Typical values: 10 – 30.

46_H	**CIS-SEIZ-H**	Caller ID Sender Number of Seizure Bits High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	SEIZ-H							

47_H	**CIS-SEIZ-L**	Caller ID Sender Number of Seizure Bits Low Byte			**Y**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	SEIZ-L							

Caller ID Sender Number of Seizure Bits:
(only if High Level Framing is selected in the CIS/LEC-MODE register (see **Page 251**))

$0 \le \text{SEIZ} \le 32767$

SEIZ-L = MOD (SEIZ,256)

SEIZ-H = INT (SEIZ/256)

48_H	**CIS-MARK-H**	Caller ID Sender Number of Mark Bits High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	MARK-H							

49_H	**CIS-MARK-L**	Caller ID Sender Number of Mark Bits Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	MARK-L							

Caller ID Sender Number of Mark Bits:
(only if High Level Framing is selected in the CIS/LEC-MODE register)

$0 \leq \text{MARK} \leq 32767$

MARK-L = MOD (MARK,256)
MARK-H = INT (MARK/256)

$4A_H$	**CIS/LEC-MODE**	CIS/LEC Mode Setting			**Y**

Bit	7	6	5	4	3	2	1	0
	LEC-ADAPT	**LEC-FREEZE**	**UTDX-SUM**	**UTDR-SUM**	**0**	**0**	**CIS-FRM**	**CIS-V23**

LEC-ADAPT Line Echo Canceller Adaptation Start. The LEC-ADAPT bit is only evaluated if the LEC-EN is changed from 0 to 1.
To initialize the LEC coefficients to 0 requires the LEC-ADAPT bit set to 0 followed by the LEC-EN bit changed from 0 to 1.
It is not possible to reset the LEC coefficients to 0 while the LEC is running. The LEC has to be disabled first by setting bit LEC-EN to 0 and then it is necessary to enable the LEC again (LEC-EN = 1, LEC-ADAPT = 0). If valid coefficients from a former LEC adaptation are present in the RAM, it is possible to activate the LEC with this coefficents by setting bit LEC-ADAPT to 1.
It is also possible to read out adapted coefficients from the LEC for external storage and to reuse these coefficients as a start up value for the next connection (see the available Apllication Notes).

LEC-ADAPT = 0	Line Echo Canceller coefficients initialized with zero
LEC-ADAPT = 1	Line Echo Canceller coefficients initialized with old coefficients

LEC-FREEZE Line Echo Canceller Adaptation Freeze

LEC-FREEZE = 0	No freezing of coefficients
LEC-FREEZE = 1	Freezing of coefficients

UTDX-SUM Sum signal for Universal Tone Detection unit in transmit direction

UTDX-SUM = 0	The transmit signal is fed through
UTDX-SUM = 1	The sum signal S_{SUM} (receive signal + LEC signal, if LEC is enabled) is fed through (see bit UTDX-SRC in BCR2 and **Figure 32**)

UTDR-SUM Sum signal for Universal Tone Detection unit in receive direction

UTDR-SUM = 0 The receive signal is fed to the UDT unit

UTDR-SUM = 1 The sum signal S_{SUM} (receive signal + LEC signal, if LEC is enabled) is fed to the UTD unit

CIS-FRM Caller ID Sender Framing

CIS-FRM = 0 Low-level framing: all data for CID transmissions have to be written to the CID Buffer including channel seizure and mark sequence, start and stop bits.

CIS-FRM = 1 High-level framing: channel seizure and mark sequence as well as start and stop bits are automatically inserted by the SLICOFI-2x. Only transmission bytes from the Data Packet (see **Figure 33**) have to be written to the CIS buffer.

CIS-V23 Caller ID Sender Mode

CIS-V23 = 0 Bell 202 selected

CIS-V23 = 1 V.23 selected

$4B_H$	**UTD-CF-H**	Universal Tone Detection Center Frequency High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	CF-H							

$4C_H$	**UTD-CF-L**	Universal Tone Detection Center Frequency Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	CF-L							

Universal Tone Detection Center Frequency:

$$CF = 32768 \times \cos\left(\frac{2\pi f_c[\mathrm{Hz}]}{8000}\right)$$

$0 < f_C < 4000$ Hz

CF-L = MOD (CF,256)
CF-H = INT (CF/256)

$4D_H$	**UTD-BW-H**	Universal Tone Detection Bandwidth High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	BW-H							

$4E_H$	**UTD-BW-L**	Universal Tone Detection Bandwidth Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	BW-L							

Universal Tone Detection Bandwidth:

$$BW = 65536 \times \frac{a}{1 + a}$$

with

$$a = \tan\left(\frac{f_{BW}[Hz] \times \pi}{8000}\right)$$

$0 < f_{BW} < 2000$ Hz

BW-L = MOD (BW,256)

BW-H = INT (BW/256)

$4F_H$	**UTD-NLEV**	Universal Tone Detection Noise Level			**Y**

Bit	7	6	5	4	3	2	1	0
	NLEV							

Universal Tone Detection Noise Level:

$$NLEV = 32768 \times 10^{(Lev_N[dB])/20}$$

$$-96\text{ dB} \leq Lev_N \leq -42.18\text{ dB}$$

50_H	**UTD-SLEV-H**	Universal Tone Detection Signal Level High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	SLEV-H							

51_H	**UTD-SLEV-L**	Universal Tone Detection Signal Level Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	SLEV-L							

Universal Tone Detection Signal Level:

Calculation for Transmit:

$\mathrm{Lev_S[dB] = Lev_S[dBm0] - 3.14 - 20{*}log_{10}(\pi/2)}$

$\mathrm{Lev_S[dB] = Lev_S[dBm] - L_x[dBr] - 3.14 - 20{*}log_{10}(\pi/2)}$

Calculation for Receive:

$\mathrm{Lev_S[dB] = Lev_S[dBm0] - 3.14 + AR1[dB] - 20{*}log_{10}(\pi/2)}$

$\mathrm{Lev_S[dB] = Lev_S[dBm] - L_R[dBr] - 3.14 + AR1[dB] - 20{*}log_{10}(\pi/2)}$

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file; approximate value AR1 $\approx L_R$ for $L_R \leq -2$ dBr, AR1 ≈ -2 dB for $L_R > -2$ dBr.

$\mathrm{SLEV = 32768 \times 10^{(Lev_S[dB])/20} - NLEV}$

$-96\ \mathrm{dB} \leq \mathrm{Lev_S} \leq 0\ \mathrm{dB}$

Signal Level:

SLEV-L = MOD (SLEV,256)

SLEV-H = INT (SLEV/256)

UTD for Receive and Transmit:

By enabling the UTD the coefficients in the UTD registers are copied to the main memory. Therefore different coefficients can be set for receive and transmit direction.

52_H	**UTD-DELT**	Universal Tone Detection Delta			**Y**

Bit	7	6	5	4	3	2	1	0
	DELT							

Universal Tone Detection Delta Inband/Outband:

$$\text{DELT} = \text{Sign}(\text{Delta}_{\text{UTD}}) \times 128 \times 10^{-|\text{Delta}_{\text{UTD}}[\text{dB}]|/20}$$

$$-42\text{ dB} \leq \text{Delta}_{\text{UTD}} \leq 42\text{ dB}$$

Example:

Detection of a tone that is between 1975 Hz and 2025 Hz → f_C = 2000 Hz

- f_{BW} = 50 Hz
  Tone at 2025 Hz: Outband = – 3 dB, Inband = – 3 dB (see **Table 65**)
  $\text{Delta}_{\text{UTD}}$ = 0 dB → DELT = 128 = 0x80
- f_{BW} = 500 Hz
  Tone at 2025 Hz: Outband = – 20 dB, Inband = – 0.04 dB (see **Table 65**)
  $\text{Delta}_{\text{UTD}}$ ≈ 20 dB → DELT = 13 = 0x0D

Table 65 UTD Inband/Outband Attenuation

f	Outband	Inband
$f_C \pm f_{BW}/0.2$	– 0.04 dB	– 20 dB
$f_C \pm f_{BW}/2$	– 3 dB	– 3 dB
$f_C \pm f_{BW}/20$	– 20 dB	– 0.04 dB
$f_C \pm f_{BW}/200$	– 40 dB	– 0 dB

53_H	**UTD-RBRK**	Universal Tone Detection Recognition Break Time			**Y**

Bit	7	6	5	4	3	2	1	0
	RBRK							

Allowed Recognition Break Time for Universal Tone Detection:

RBRK = RBRKTime[ms]/4
RBRKTime has to be entered in multiples of 4 ms.

0 ms ≤ RBRKTime ≤ 1000 ms

For an example see **Figure 72**.

54_H	**UTD-RTIME**	Universal Tone Detection Recognition Time			**Y**

Bit	7	6	5	4	3	2	1	0
	RTIME							

Universal Tone Detection Recognition Time:

RTIME = RTime[ms]/16

RTime has to be entered in multiples of 16 ms.

0 ms ≤ RTime ≤ 4000 ms

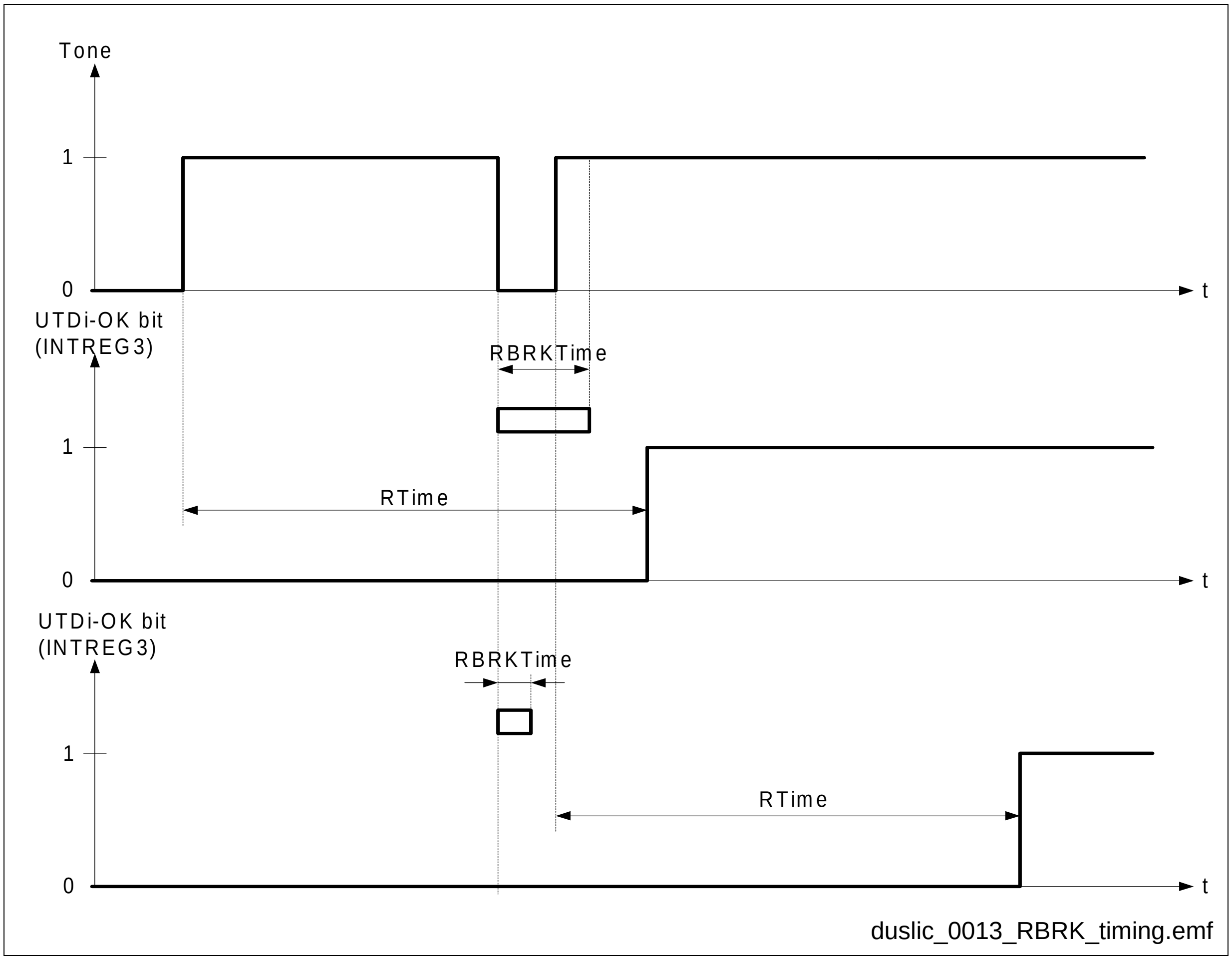

Tone
1
0
t
UTDi-OK bit
(INTREG3)
RBRKTime
1
RTime
0
t
UTDi-OK bit
(INTREG3)
RBRKTime
1
RTime
0
t
duslic_0013_RBRK_timing.emf

Figure 72 Example for UTD Recognition Timing

55_H	**UTD-EBRK**	UTD Allowed Tone End Detection Break Time			**Y**

Bit	7	6	5	4	3	2	1	0
	EBRK							

Allowed tone end detection break time for Universal Tone Detection:

EBRK = EBRKTime [ms]

0 ms ≤ EBRKTime ≤ 255 ms

For an example see **Figure 73**.

56_H	**UTD-ETIME**	UTD Tone End Detection Time			**Y**

Bit	7	6	5	4	3	2	1	0
	ETIME							

Tone End Detection Time for Universal Tone Detection:

ETIME = ETime[ms]/4

ETime has to be entered in multiples of 4 ms.

0 ms ≤ ETime ≤ 1000 ms

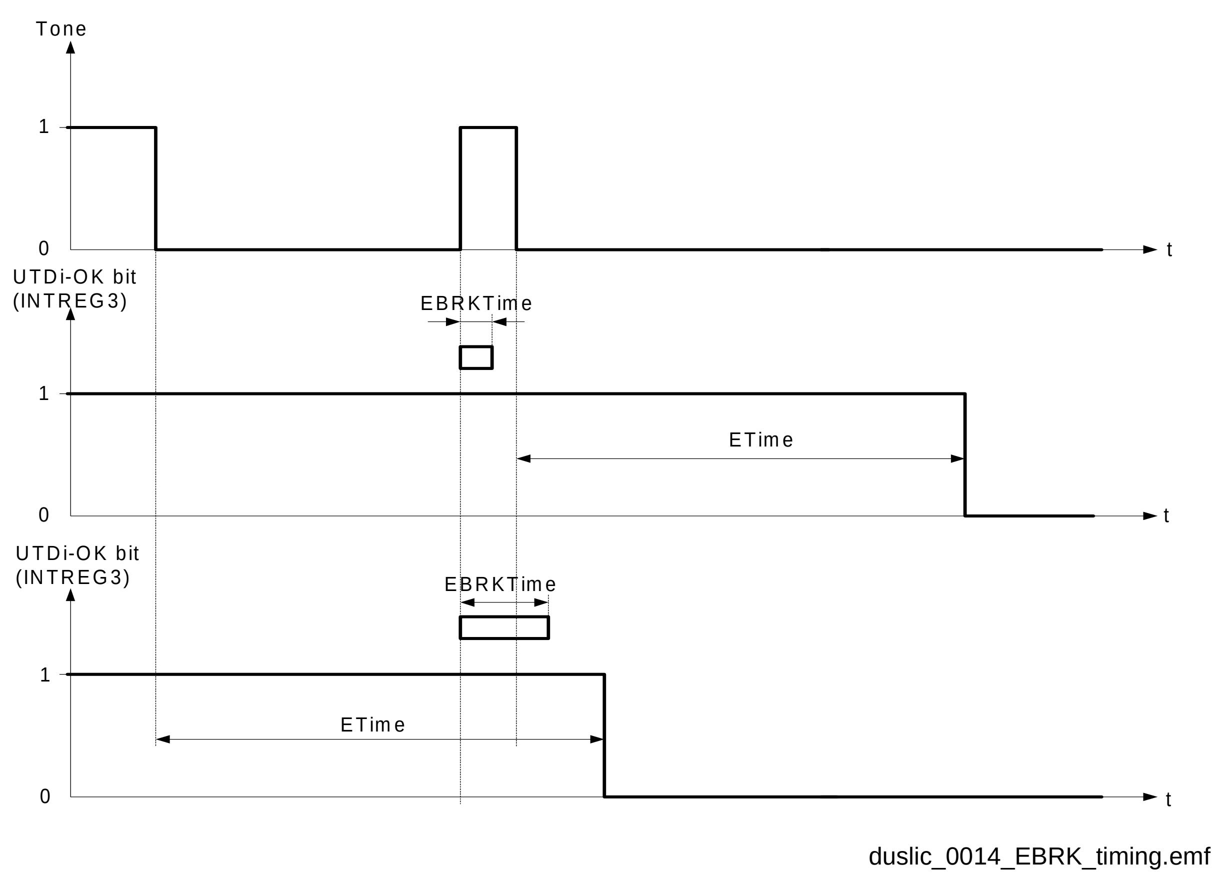

Tone
1
0
t
UTDi-OK bit
(INTREG3)
EBRKTime
1
ETime
0
t
UTDi-OK bit
(INTREG3)
EBRKTime
1
ETime
0
t
duslic_0014_EBRK_timing.emf

Figure 73 Example for UTD Tone End Detection Timing

6.2.5 IOM-2 Interface Command/Indication Byte

The Command/Indication (C/I) channel is used to communicate real-time status information and for fast controlling of the DuSLIC. Data on the C/I channel are continuously transmitted in each frame until new data are sent.

Data Downstream C/I – Channel Byte (Receive) – IOM-CIDD

The first six CIDD data bits control the general operating modes for both DuSLIC channels. According to the IOM-2 specifications, new data have to be present for at least two frames to be accepted.

Table 66 M2, M1, M0: General Operating Mode

CIDD			**SLICOFI-2 Operating Mode** (for details see **“Operating Modes for the DuSLIC Chip Set” on Page 78**)
M2	**M1**	**M0**	
1	1	1	Sleep, Power Down (PDRx)
0	0	0	Power Down High Impedance (PDH)
0	1	0	Any Active mode
1	0	1	Ringing (ACTR Burst On)
1	1	0	Active with Metering
1	0	0	Ground Start
0	0	1	Ring Pause

	CIDD	Data Downstream C/I – Channel Byte			**N**

Bit	7	6	5	4	3	2	1	0
	M2A	**M1A**	**M0A**	**M2B**	**M1B**	**M0B**	**MR**	**MX**

M2A, M1A, M0A	Select operating mode for DuSLIC channel A
M2B, M1B, M0B	Select operating mode for DuSLIC channel B
MR, MX	Handshake bits Monitor Receive and Transmit (see **“IOM-2 Interface Monitor Transfer Protocol” on Page 148**)

Data Upstream C/I – Channel Byte (Transmit) – IOM-CIDU

This byte is used to quickly transfer the most important and time-critical information from the DuSLIC. Each transfer from the DuSLIC lasts for at least 2 consecutive frames.

	CIDU	Data Upstream C/I – Channel Byte	**00_H**		**N**

Bit	7	6	5	4	3	2	1	0
	INT-CHA	**HOOKA**	**GNDKA**	**INT-CHB**	**HOOKB**	**GNDKB**	**MR**	**MX**

INT-CHA	Interrupt information channel A	
	INT-CHA = 0	No interrupt in channel A
	INT-CHA = 1	Interrupt in channel A
HOOKA	Hook information channel A	
	HOOKA = 0	On-hook channel A
	HOOKA = 1	Off-hook channel A
GNDKA	Ground key information channel A	
	GNDKA = 0	No longitudinal current detected
	GNDKA = 1	Longitudinal current detected in channel A
INT-CHB	Interrupt information channel B	
	INT-CHB = 0	No interrupt in channel B
	INT-CHB = 1	Interrupt in channel B
HOOKB	Hook information channel B	
	HOOKB = 0	On-hook Channel B
	HOOKB = 1	Off-hook Channel B
GNDKB	Ground key information channel B	
	GNDKB = 0	No longitudinal current detected
	GNDKB = 1	Longitudinal current detected in channel B
MR, MX	Handshake bits Monitor Receive and Transmit (see **“IOM-2 Interface Monitor Transfer Protocol” on Page 148**)	

6.2.6 Programming Examples of the SLICOFI-2

6.2.6.1 Microcontroller Interface

SOP Write to Channel 0 Starting After the Channel Specific Read-only Registers

01000100	First command byte (SOP write for channel 0)
00010101	Second command byte (Offset to BCR1 register)
00000000	Contents of BCR1 register
00000000	Contents of BCR2 register
00010001	Contents of BCR3 register
00000000	Contents of BCR4 register
00000000	Contents of BCR5 register

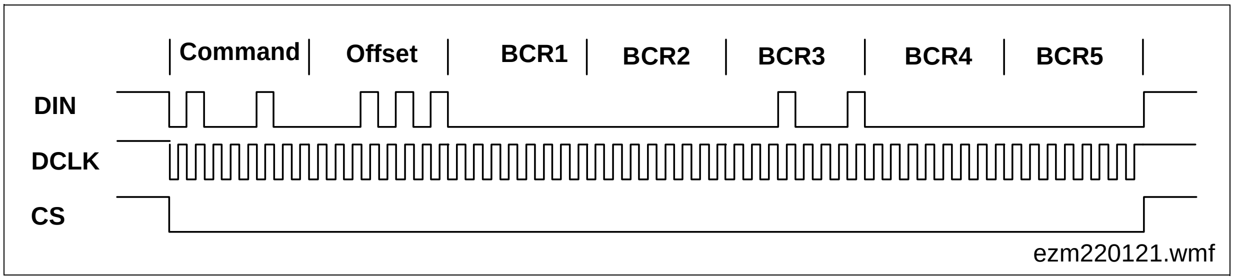

Command
Offset
BCR1
BCR2
BCR3
BCR4
BCR5
DIN
DCLK
CS
ezm220121.wmf

Figure 74 Waveform of Programming Example SOP-Write to Channel 0

SOP Read from Channel 1 Reading Out the Interrupt Registers

11001100	First command byte (SOP read for channel 1).
00000111	Second command byte (Offset to Interrupt register 1).

The SLICOFI-2 will send data when it has completely received the second command byte.

11111111	Dump byte (This byte is always FF_H).
11000000	Interrupt register INTREG1 (An interrupt has occurred, Off-hook was detected).
00000010	Interrupt register INTREG2 (IO pin 2 is ‘1’).
00000000	Interrupt register INTREG3
00000000	Interrupt register INTREG4

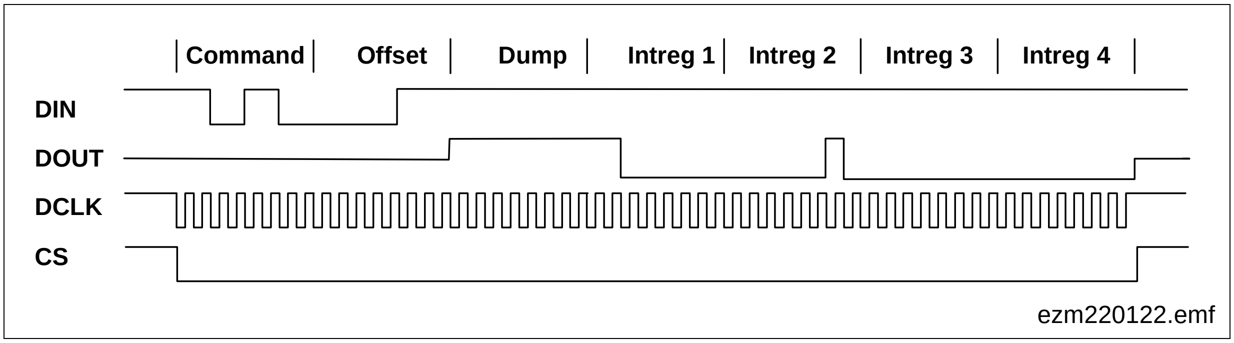

Command
Offset
Dump
Intreg 1
Intreg 2
Intreg 3
Intreg 4
DIN
DOUT
DCLK
CS
ezm220122.emf

Figure 75 Waveform of Programming Example SOP Read from Channel 0

6.2.6.2 IOM-2 Interface

An example with the same programming sequence as before, using the IOM-2 interface is presented here to show the differences between the microcontroller interface and the IOM-2 interface.

SOP Write to Channel 0 Starting After the Channel-Specific Read-only Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	11111111	11	IOM-2 address first byte
10000001	10	11111111	01	IOM-2 address second byte
01000100	11	11111111	01	First command byte (SOP write for channel 0)
01000100	10	11111111	11	First command byte second time
00010101	11	11111111	01	Second command byte (Offset to BCR1 register)
00010101	10	11111111	11	Second command byte second time
00000000	11	11111111	01	Contents of BCR1 register
00000000	10	11111111	11	Contents of BCR1 register second time
00000000	11	11111111	01	Contents of BCR2 register
00000000	10	11111111	11	Contents of BCR2 register second time
00010001	11	11111111	01	Contents of BCR3 register
00010001	10	11111111	11	Contents of BCR3 register second time
00000000	11	11111111	01	Contents of BCR4 register
00000000	10	11111111	11	Contents of BCR4 register second time
11111111	11	11111111	01	No more information (dummy byte)
11111111	11	11111111	11	Signaling EOM (end of message) by holding MX bit at ‘1’.

Since the SLICOFI-2 has an open command structure there is no fixed command length. The IOM-2 handshake protocol allows for an infinite length of a data stream, therefore the host has to terminate the data transfer by sending an end-of-message signal (EOM) to the SLICOFI-2. The SLICOFI-2 will abort the transfer only if the host tries to write or read beyond the allowed maximum offset given by the different types of commands. Each transfer has to start with the SLICOFI-2-specific IOM-2 address (81_H) and must end with an EOM of the handshake bits. Appending a command immediately to its predecessor without an EOM in between is not allowed.

When reading interrupt registers, SLICOFI-2 stops the transfer after the fourth register in IOM-2 mode. This is to prevent some host chips reading 16 bytes because they can’t terminate the transfer after n bytes.

SOP-Read from Channel 1 Reading Out the Interrupt Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	11111111	11	IOM-2 address first byte
10000001	10	11111111	01	IOM-2 address second byte
11001100	11	11111111	01	First command byte (SOP read for channel 1)
11001100	10	11111111	11	First command byte second time
00001000	11	11111111	01	Second command byte (offset to interrupt register 1)
00001000	10	11111111	11	Second command byte second time
11111111	11	11111111	01	Acknowledgement for the second command byte
11111111	11	10000001	10	IOM-2 Address first byte (answer)
11111111	01	10000001	10	IOM-2 Address second byte
11111111	01	11000000	11	Interrupt register INTREG1
11111111	11	11000000	10	Interrupt register INTREG1 second time
11111111	01	00000010	11	Interrupt register INTREG2
11111111	11	00000010	10	Interrupt register INTREG2 second time
11111111	01	00000000	11	Interrupt register INTREG3
11111111	11	00000000	10	Interrupt register INTREG3 second time
11111111	01	00000000	11	Interrupt register INTREG4
11111111	11	00000000	10	Interrupt register INTREG4 second time
11111111	11	01001101	11	SLICOFI-2 sends the next register
11111111	11	11111111	11	SLICOFI-2 aborts transmission

6.3 SLICOFI-2S/-2S2 Command Structure and Programming

This chapter comprises only the SLICOFI-2S/-2S2 PEB 3264/-2 and therefore the DuSLIC-S and DuSLIC-S2 chip sets.

6.3.1 SOP Command

The SOP “Status Operation” command provides access to the configuration and status registers of the SLICOFI-2S/-2S2. Common registers change the mode of the entire SLICOFI-2S/-2S2 chip, all other registers are channel-specific. It is possible to access single or multiple registers. Multiple register access is realized by an automatic offset increment. Write access to read-only registers is ignored and does not abort the command sequence. Offsets may change in newer versions of the SLICOFI-2S/-2S2.

(All empty register bits have to be filled with zeros.)

6.3.1.1 SOP Register Overview

00_H REVISION Revision Number (read-only)

REV[7:0]

01_H CHIPID 1 Chip Identification 1 (read-only)

for internal use only

02_H CHIPID 2 Chip Identification 2 (read-only)

for internal use only

03_H CHIPID 3 Chip Identification 3 (read-only)

for internal use only

04_H FUSE1 Fuse Register 1

for internal use only

05_H PCMC1 PCM Configuration Register 1

DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE-0	SHIFT	PCMO[2:0]		

06_H XCR Extended Configuration Register

0	ASYNCH-R	0	0	0	0	0	0

07_H INTREG1 Interrupt Register 1 (read-only)

INT-CH	HOOK	GNDK	GNKP	ICON	VRTLIM	OTEMP	SYNC-FAIL

08_H INTREG2 Interrupt Register 2 (read-only)

0	READY	RSTAT	0	IO[4:1]-DU			

09_H INTREG3 Interrupt Register 3 (read-only)

0	0	0	0	0	0	0	0

$0A_H$ INTREG4 Interrupt Register 4 (read-only)

0	0	0	0	0	0	0	0

$0B_H$ CHKR1 Checksum Register 1 (High Byte) (read-only)

SUM-OK	CHKSUM-H[6:0]						

$0C_H$ CHKR2 Checksum Register 2 (Low Byte) (read-only)

CHKSUM-L[7:0]							

$0D_H$ reserved

0	0	0	0	0	0	0	0

$0E_H$ reserved

0	0	0	0	0	0	0	0

$0F_H$ FUSE2 Fuse Register 2

for internal use only							

10_H FUSE3 Fuse Register 3

for internal use only							

11_H MASK Mask Register

READY-M	HOOK-M	GNDK-M	GNKP-M	ICON-M	VRTLIM-M	OTEMP-M	SYNC-M

12_H IOCTL1 IO Control Register 1

IO[4:1]-INEN	IO[4:1]-M

13_H IOCTL2 IO Control Register 2

IO[4:1]-OEN	IO[4:1]-DD

14_H IOCTL3 IO Control Register 3

DUP[3:0]	DUP-IO[3:0]

15_H BCR1 Basic Configuration Register 1

HIR	HIT	0	REVPOL	ACTR	ACTL	0	0

16_H BCR2 Basic Configuration Register 2

REXT-EN	SOFT-DIS	TTX-DIS1)	TTX-12K2)	HIM-AN	AC-XGAIN	0	PDOT-DIS

17_H BCR3 Basic Configuration Register 3

MU-LAW	LIN	0	PCMX-EN	0	0	0	CRAM-EN

18_H BCR4 Basic Configuration Register 4

TH-DIS	IM-DIS	AX-DIS	AR-DIS	FRX-DIS	FRR-DIS	HPX-DIS	HPR-DIS

19_H reserved

0	0	0	0	0	0	0	0

$1A_H$ DSCR DTMF Sender Configuration Register

DG-KEY[3:0]	COR8	PTG	TG2-EN	TG1-EN

$1B_H$ reserved

0	0	0	0	0	0	0	0

$1C_H$ LMCR1 Level Metering Configuration Register 1

TEST-EN	0	1	PCM2DC	0	0	1	0

1D$_H$ LMCR2 Level Metering Configuration Register 2

0	0	0	0	0	0	0	0

1E$_H$ LMCR3 Level Metering Configuration Register 3

AC-SHORT-EN	RTR-SEL	0	0	0	0	0	0

1F$_H$ OFR1 Offset Register 1 (High Byte)

OFFSET-H[7:0]

20$_H$ OFR2 Offset Register 2 (Low Byte)

OFFSET-L[7:0]

21$_H$ PCMR1 PCM Receive Register 1

R1-HW	R1-TS[6:0]

22$_H$ reserved

23$_H$ reserved

24$_H$ reserved

25$_H$ PCMX1 PCM Transmit Register 1

X1-HW	X1-TS[6:0]

26$_H$ reserved

27_H reserved

28_H reserved

29_H TSTR1 Test Register 1

PD-AC-PR	PD-AC-PO	PD-AC-AD	PD-AC-DA	PD-AC-GN	PD-GNKC	PD-OFHC	PD-OVTC

$2A_H$ TSTR2 Test Register 2

PD-DC-PR	0	PD-DC-AD	PD-DC-DA	PD-DCBUF	0	PD-TTX-A2)	PD-HVI

$2B_H$ TSTR3 Test Register 3

0	0	AC-DLB-4M	AC-DLB-128K	AC-DLB-32K	AC-DLB-8K	0	0

$2C_H$ TSTR4 Test Register 4

OPIM-AN	OPIM-4M	COR-64	COX-16	0	0	0	0

$2D_H$ TSTR5 Test Register 5

0	0	0	DC-POFI-HI	DC-HOLD	0	0	0

1) Only for DuSLIC-S, is set to 1 for DuSLIC-S2

2) Only for DuSLIC-S, is set to 0 for DuSLIC-S2

6.3.1.2 SOP Register Description

00_H	**REVISION**	Revision Number (read-only)	**curr. rev.**		**N**

Bit	7	6	5	4	3	2	1	0
	REV[7:0]							

REV[7:0] Current revision number of the SLICOFI-2S/-2S2.

01_H	**CHIPID 1**	Chip Identification 1 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

02_H	**CHIPID 2**	Chip Identification 2 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

03_H	**CHIPID 3**	Chip Identification 3 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

04_H	**FUSE1**	Fuse Register 1	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

05_H	**PCMC1**	PCM Configuration Register 1	**00_H**		**N**

Bit	7	6	5	4	3	2	1	0
	DBL-CLK	**X-SLOPE**	**R-SLOPE**	**NO-DRIVE-0**	**SHIFT**	**PCMO[2:0]**		

DBL-CLK Clock mode for the PCM interface (see **Figure 59** on **Page 141**).

DBL-CLK = 0	Single clocking is used.
DBL-CLK = 1	Double clocking is used.

X-SLOPE Transmit Slope (see **Figure 59** on **Page 141**).

X-SLOPE = 0	Transmission starts with rising edge of the clock.
X-SLOPE = 1	Transmission starts with falling edge of the clock.

R-SLOPE Receive Slope (see **Figure 59** on **Page 141**).

R-SLOPE = 0	Data is sampled with falling edge of the clock.
R-SLOPE = 1	Data is sampled with rising edge of the clock.

NO-DRIVE-0 Driving Mode for Bit 0 (only available in single-clocking mode).

NO-DRIVE = 0	Bit 0 is driven the entire clock period.
NO-DRIVE = 1	Bit 0 is driven during the first half of the clock period only.

SHIFT Shifts the access edges by one clock cycle in double clocking mode.

SHIFT = 0	No shift takes place.
SHIFT = 1	Shift takes place.

PCMO[2:0] The whole PCM timing is moved by PCMO data periods against the FSC signal.

PCMO[2:0] = 0 0 0	No offset is added.
PCMO[2:0] = 0 0 1	One data period is added.
…	
PCMO[2:0] = 1 1 1	Seven data periods are added.

06_H	**XCR**	Extended Configuration Register	**00_H**		**N**

Bit	7	6	5	4	3	2	1	0
	0	**ASYNCH -R**	**0**	**0**	**0**	**0**	**0**	**0**

ASYNCH-R Enables asynchronous ringing in case of external ringing.

ASYNCH-R = 0	External ringing with zero crossing selected
ASYNCH-R = 1	Asynchronous ringing selected.

07_H	**INTREG1**	Interrupt Register 1 (read-only)	80_H		Y

Bit	7	6	5	4	3	2	1	0
	INT-CH	**HOOK**	**GNDK**	**GNKP**	**ICON**	**VRTLIM**	**OTEMP**	**SYNC-FAIL**

INT-CH Interrupt channel bit. This bit indicates that the corresponding channel caused the last interrupt. Will be set automatically to zero after all interrupt registers were read.

INT-CH = 0	No interrupt in corresponding channel.
INT-CH = 1	Interrupt caused by corresponding channel.

HOOK On/Off-hook information for the loop in all operating modes, filtered by DUP (Data Upstream Persistence) counter and interrupt generation masked by the HOOK-M bit. A change of this bit generates an interrupt.

HOOK = 0	On-hook.
HOOK = 1	Off-hook.

GNDK Ground Key or Ground Start information via the IL pin in all active modes, filtered for AC suppression by the DUP counter and interrupt generation masked by the GNDK-M bit. A change of this bit generates an interrupt.

GNDK = 0	No longitudinal current detected.
GNDK = 1	Longitudinal current detected (Ground Key or Ground Start).

GNKP Ground key polarity. Indicating the active ground key level (positive/negative) interrupt generation masked by the GNKP-M bit. A change of this bit generates an interrupt. This bit can be used to get information about interference voltage influence.

GNKP = 0	Negative ground key threshold level active.
GNKP = 1	Positive ground key threshold level active.

ICON Constant current information. Filtered by DUP-IO counter and interrupt generation masked by the ICON-M bit. A change of this bit generates an interrupt.

ICON = 0	Resistive or constant voltage feeding.
ICON = 1	Constant current feeding.

VRTLIM Exceeding of a programmed voltage threshold for the TIP/RING voltage, filtered by the DUP-IO counter and interrupt generation masked by the VRTLIM-M bit. A change of this bit causes an interrupt.
The voltage threshold for the TIP/RING voltage is set in CRAM (calculated with DuSLICOS DC Control Parameter 2/3: Tip-Ring Threshold).

VRTLIM = 0	Voltage at Ring/Tip is below the limit.
VRTLIM = 1	Voltage at Ring/Tip is above the limit.

OTEMP Thermal overload warning from the SLIC-S/-S2 line drivers masked by the OTEMP-M bit. An interrupt is only generated if the OTEMP bit changes from 0 to1.

OTEMP = 0	Temperature at SLIC-S/-S2 is below the limit.
OTEMP = 1	Temperature at SLIC-S/-S2 is above the limit. In case of bit PDOT-DIS = 0 (register BCR2) the DuSLIC is switched automatically into PDH mode and OTEMP is hold at 1 until the SLICOFI-2S/-2S2 is set to PDH by a CIOP/CIDD command.

SYNC-FAIL Failure of the synchronization of the IOM-2/PCM Interface. An interrupt is only generated if the SYNC-FAIL bit changes from 0 to 1.
Resynchronization of the PCM interface can be done with the Resynchronization command (see **Chapter 6**)

SYNC-FAIL = 0	Synchronization OK.
SYNC-FAIL = 1	Synchronization failure.

08_H	**INTREG2**	Interrupt Register 2 (read-only)	**20_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**READY**	**RSTAT**	**0**	**IO[4:1]-DU**			

After a hardware reset the RSTAT bit is set and generates an interrupt. Therefore the default value of INTREG2 is 20h. After reading all four interrupt registers, the INTREG2 value changes to 4Fh.

READY Indication whether ramp generator has finished. An interrupt is only generated if the READY bit changes from 0 to 1. At a new start of the ramp generator, the bit is set to 0. For further information regarding soft reversal see **Chapter 3.7.2.1**.

READY = 0	Ramp generator active.
READY = 1	Ramp generator not active.

RSTAT Reset status since last interrupt.

RSTAT = 0	No reset has occurred since the last interrupt.
RSTAT = 1	Reset has occurred since the last interrupt.

IO[4:1]-DU Data on IO pins 1 to 4 filtered by the DUP-IO counter and interrupt generation masked by the IO[4:1]-DU-M bits. A change of any of these bits generates an interrupt.

09_H	**INTREG3**	Interrupt Register 3 (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$0A_H$	**INTREG4**	Interrupt Register 4 (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$0B_H$	**CHKR1**	Checksum Register 1 (High Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	SUM-OK	**CHKSUM-H[6:0]**						

SUM-OK Information about the validity of the checksum. The checksum is valid if the internal checksum calculation is finished.

Checksum calculation:

```
For (cram_adr = 0 to 159) do
cram_dat = cram[cram_adr]
csum[14:0] = (csum[13:0] &1) ‘0’) xor
(‘0000000’ & cram_dat[7:0]) xor
(‘0000000000000’ & csum[14] & csum[14])
End
```

SUM-OK = 0	CRAM checksum is not valid.
SUM-OK = 1	CRAM checksum is valid.

1) “&” means a concatenation, not the logic operation

CHKSUM-H[6:0]	CRAM checksum high byte

0C$_H$	**CHKR2**	Checksum Register 2 (Low Byte) (read-only)	**00$_H$**		**Y**

Bit	7	6	5	4	3	2	1	0
	CHKSUM-L[7:0]							

CHKSUM-L[7:0] CRAM-checksum low byte

0D$_H$		reserved	**00$_H$**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

0E$_H$		reserved	**00$_H$**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

0F$_H$	**FUSE2**	Fuse Register 2	**hw**		**Y**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

10$_H$	**FUSE3**	Fuse Register 3	**hw**		**Y**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

11_H	MASK	Mask Register	FF_H		Y

Bit	7	6	5	4	3	2	1	0
	READY -M	**HOOK -M**	**GNDK -M**	**GNKP -M**	**ICON -M**	**VRTLIM -M**	**OTEMP -M**	**SYNC -M**

The mask bits in the mask register only influence the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers gets updated to show the current status of the corresponding event.

READY-M Mask bit for Ramp Generator READY bit

READY-M = 0 An interrupt is generated if the READY bit changes from 0 to 1.

READY-M = 1 Changes of the READY bit don’t generate interrupts.

HOOK-M Mask bit for Off-Hook Detection HOOK bit

HOOK-M = 0 Each change of the HOOK bit generates an interrupt.

HOOK-M = 1 Changes of the HOOK bit don’t generate interrupts.

GNDK-M Mask bit for Ground Key Detection GNDK bit

GNDK-M = 0 Each change of the GNDK bit generates an interrupt.

GNDK-M = 1 Changes of the GNDK bit don’t generate interrupts.

GNKP-M Mask bit for Ground Key Level GNKP bit

GNKP-M = 0 Each change of the GNKP bit generates an interrupt.

GNKP-M = 1 Changes of the GNKP bit don’t generate interrupts.

ICON-M Mask bit for Constant Current Information ICON bit

ICON-M = 0 Each change of the ICON bit generates an interrupt.

ICON_M = 1 Changes of the ICON bit don’t generate interrupts.

VRTLIM-M Mask bit for Programmed Voltage Limit VRTLIM bit

VRTLIM-M = 0 Each change of the VRTLIM bit generates an interrupt.

VRTLIM-M = 1 Changes of the VRTLIM bit don’t generate interrupts.

OTEMP-M Mask bit for Thermal Overload Warning OTEMP bit

OTEMP-M = 0	A change of the OTEMP bit from 0 to 1 generates an interrupt.
OTEMP-M = 1	A change of the OTEMP bit from 0 to 1 doesn't generate interrupts.

SYNC-M Mask bit for Synchronization Failure SYNC-FAIL bit

SYNC-M = 0	A change of the SYNC-FAIL bit from 0 to 1 generates an interrupt.
SYNC-M = 1	A change of the SYNC-FAIL bit from 0 to 1 doesn't generate interrupts.

12_H	**IOCTL1**	IO Control Register 1	$0F_H$		**Y**

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-INEN				**IO[4:1]-M**			

The mask bits IO[4:1]-M only influence the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers gets updated to show the current status of the corresponding event.

IO4-INEN Input enable for programmable IO pin IO4

IO4-INEN = 0 Input Schmitt trigger of pin IO4 is disabled.

IO4-INEN = 1 Input Schmitt trigger of pin IO4 is enabled.

IO3-INEN Input enable for programmable IO pin IO3

IO3-INEN = 0 Input Schmitt trigger of pin IO3 is disabled.

IO3-INEN = 1 Input Schmitt trigger of pin IO3 is enabled.

IO2-INEN Input enable for programmable IO pin IO2

IO2-INEN = 0 Input Schmitt trigger of pin IO2 is disabled.

IO2-INEN = 1 Input Schmitt trigger of pin IO2 is enabled.

IO1-INEN Input enable for programmable IO pin IO1

IO1-INEN = 0 Input Schmitt trigger of pin IO1 is disabled.

IO1-INEN = 1 Input Schmitt trigger of pin IO1 is enabled.

IO4-M Mask bit for IO4-DU bit

IO4-M = 0 Each change of the IO4 bit generates an interrupt.

IO4-M = 1 Changes of the IO4 bit don’t generate interrupts.

IO3-M Mask bit for IO3-DU bit

IO3-M = 0 Each change of the IO3 bit generates an interrupt.

IO3-M = 1 Changes of the IO3 bit don’t generate interrupts.

IO2-M	Mask bit for IO2-DU bit	
	IO2-M = 0	Each change of the IO2 bit generates an interrupt.
	IO2-M = 1	Changes of the IO2 bit don’t generate interrupts.
IO1-M	Mask bit for IO1-DU bit	
	IO1-M = 0	Each change of the IO1 bit generates an interrupt.
	IO1-M = 1	Changes of the IO1 bit don’t generate interrupts.

13_H	IOCTL2	IO Control Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-OEN				IO[4:1]-DD			

IO4-OEN Enabling the output driver of pin IO4

IO4-OEN = 0 The output driver of pin IO4 is disabled.

IO4-OEN = 1 The output driver of pin IO4 is enabled.

IO3-OEN Enabling the output driver of pin IO3

IO3-OEN = 0 The output driver of pin IO3 is disabled.

IO3-OEN = 1 The output driver of pin IO3 is enabled.

IO2-OEN Enabling the output driver of pin IO2

IO2-OEN = 0 The output driver of pin IO2 is disabled.

IO2-OEN = 1 The output driver of pin IO2 is enabled.

IO1-OEN Enabling the output driver of pin IO1
If external ringing is selected (bit REXT-EN in register BCR2 set to 1), pin IO1 cannot be controlled by the user but is utilized by the SLICOFI-2S/-2S2 to control the ring relay.

IO1-OEN = 0 The output driver of pin IO1 is disabled.

IO1-OEN = 1 The output driver of pin IO1 is enabled.

IO4-DD Value for the programmable IO pin IO4 if programmed as an output pin.

IO4-DD = 0 The corresponding pin is driving a logical 0.

IO4-DD = 1 The corresponding pin is driving a logical 1.

IO3-DD Value for the programmable IO pin IO3 if programmed as an output pin.

IO3-DD = 0 The corresponding pin is driving a logical 0.

IO3-DD = 1 The corresponding pin is driving a logical 1.

IO2-DD	Value for the programmable IO pin IO2 if programmed as an output pin.	
	IO2-DD = 0	The corresponding pin is driving a logical 0.
	IO2-DD = 1	The corresponding pin is driving a logical 1.
IO1-DD	Value for the programmable IO pin IO1 if programmed as an output pin.	
	IO1-DD = 0	The corresponding pin is driving a logical 0.
	IO1-DD = 1	The corresponding pin as driving a logical 1.

14_H	**IOCTL3**	IO Control Register 3	94_H		**Y**

Bit	7	6	5	4	3	2	1	0
	DUP[3:0]				**DUP-IO[3:0]**			

DUP[3:0] Data Upstream Persistence Counter end value. Restricts the rate of interrupts generated by the HOOK bit in the interrupt register INTREG1. The interval is programmable from 1 to 16 ms in steps of 1 ms (reset value is 10 ms).
The DUP[3:0] value affects the blocking period for ground key detection (see **Chapter 3.6**).

DUP[3:0]	HOOK Active, Ringing	HOOK Power Down	GNDK	GNDK $f_{min,ACsup}$[1]
0000	1	2 ms	4 ms	125 Hz
0001	2	4 ms	8 ms	62.5 Hz
...				
1111	16	32 ms	64 ms	7.8125 Hz

[1] Minimum frequency for AC suppression.

DUP-IO[3:0] Data Upstream Persistence Counter end value for

- the IO pins when used as digital input pins.
- the bits ICON and VRTLIM in register INTREG1.

The interval is programmable from 0.5 to 60.5 ms in steps of 4 ms (reset value is 16.5 ms).

15_H	**BCR1**	Basic Configuration Register 1	00_H		**Y**

Bit	7	6	5	4	3	2	1	0
	HIR	**HIT**	**0**	**REVPOL**	**ACTR**	**ACTL**	**0**	**0**

HIR This bit modifies different basic modes. In ringing mode an unbalanced ringing on the RING-wire (ROR) is enabled. In active mode, high impedance on the RING-wire is performed (HIR). It enables the HIRT-mode together with the HIT bit.

HIR = 0	Normal operation (ringing mode).
HIR = 1	Controls SLIC-S/-S2-interface and sets the RING wire to high impedance (active mode).

HIT This bit modifies different basic modes. In ringing mode an unbalanced ringing on the TIP-wire (ROT) is enabled. In active mode, high impedance on the TIP-wire is performed (HIT). It enables the HIRT-mode together with the HIR bit.

HIT = 0	Normal operation (ringing mode).
HIT = 1	Controls SLIC-S/-S2-interface and sets the TIP-wire to high impedance (active mode).

REVPOL Reverse polarity of DC feeding

REVPOL = 0	Normal polarity.
REVPOL = 1	Reverse polarity.

ACTR Selection of extended battery feeding in Active mode. In this case $V_{HR} – V_{BATH}$ for SLIC-S/-S2 is used.

ACTR = 0	No extended battery feeding selected.
ACTR = 1	Extended battery feeding selected.

ACTL Selection of the low battery supply voltage V_{BATL} on SLIC-S/-S2 if available. Valid only in Active mode of the SLICOFI-2S/-2S2.

ACTL = 0	Low battery supply voltage on SLIC-S/-S2 is not selected.
ACTL = 1	Low battery supply voltage on SLIC-S/-S2 is selected.

16_H	**BCR2**	Basic Configuration Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	REXT-EN	**SOFT-DIS**	**TTX-DIS**[1]	**TTX-12K**[2]	**HIM-AN**	**AC-XGAIN**	**0**	**PDOT-DIS**

[1] Only for DuSLIC-S, is set to 1 for DuSLIC-S2

[2] Only for DuSLIC-S, is set to 0 for DuSLIC-S2

REXT-EN Enables the use of an external ring-signal generator. The synchronization is done via the RSYNC pin and the ring-burst-enable signal is transferred via the IO1 pin.

REXT-EN = 0	External ringing is disabled.
REXT-EN = 1	External ringing enabled.

SOFT-DIS Polarity soft reversal (to minimize noise on DC feeding)

SOFT-DIS = 0	Polarity soft reversal active.
SOFT-DIS = 1	Polarity hard reversal.

TTX-DIS Disables the generation of TTX bursts for metering signals. If they are disabled, revese polarity is used instead.

TTX-DIS = 0	TTX bursts are enabled.
TTX-DIS = 1	TTX bursts are disabled, reverse polarity used.

TTX-12K Selection of TTX frequencies

TTX-12K = 0	Selects 16 kHz TTX signals instead of 12 kHz signals.
TTX-12K = 1	12 kHz TTX signals.

HIM-AN Higher impedance in analog impedance matching loop.
HIM-AN corresponds to the coefficients calculated with DuSLICOS. If the coefficients are calculated with standard impedance in analog impedance matching loop, HIM-AN must be set to 0; if the coefficients are calculated with high impedance in analog impedance matching loop, HIM-AN must be set to 1.

HIM-AN = 0	Standard impedance in analog impedance matching loop (300 Ω).
HIM-AN = 1	High impedance in analog impedance matching loop (600 Ω).

AC-XGAIN Analog gain in transmit direction (should be set to zero).

AC-XGAIN = 0	No additional analog gain in transmit direction.
AC-XGAIN = 1	Additional 6 dB analog amplification in transmit direction.

PDOT-DIS Power Down Overtemperature Disable

PDOT-DIS = 0	When over temperature is detected, the SLIC-S/-S2 is automatically switched into Power Down High Impedance mode (PDH). This is the safe operation mode for the SLIC-S/-S2 in case of overtemperature. To leave the automatically activated PDH mode, DuSLIC has to be switched manually to PDH mode and then in the mode as desired.
PDOT-DIS = 1	When over temperature is detected, the SLIC-S/-S2 doesn’t automatically switch into Power Down High Impedance mode. In this case the output current of the SLIC-S/-S2 buffers is limited to a value which keeps the SLIC-S/-S2 temperature below the upper temperature limit.

17_H	**BCR3**	Basic Configuration Register 3	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	MU-LAW	**LIN**	**0**	**PCMX-EN**	**0**	**0**	**0**	**CRAM-EN**

MU-LAW Selects the PCM Law

MU-LAW = 0 A-Law enabled.

MU-LAW = 1 µ-Law enabled.

LIN Voice transmission in a 16 bit linear representation for test purposes.

Note: Voice transmission on the other channel is inhibited if one channel is set to linear mode and the IOM-2 interface is used. In PCM/µC interface mode both channels can be in linear mode using two consecutive PCM timeslots on the highways. A proper timeslot selection must be specified.

LIN = 0 PCM mode enabled (8 bit, A-law or µ-law).

LIN = 1 Linear mode enabled (16 bit).

PCMX-EN Enables writing of subscriber voice data to the PCM highway.

PCMX-EN = 0 Writing of subscriber voice data to PCM highway is disabled.

PCMX-EN = 1 Writing of subscriber voice data to PCM highway is enabled.

CRAM-EN Coefficients from CRAM are used for programmable filters and DC loop behavior.

CRAM-EN = 0 Coefficients from ROM are used.

CRAM-EN = 1 Coefficients from CRAM are used.

18_H	**BCR4**	Basic Configuration Register 4	00_H		Y

Bit	7	6	5	4	3	2	1	0
	TH-DIS	**IM-DIS**	**AX-DIS**	**AR-DIS**	**FRX-DIS**	**FRR-DIS**	**HPX-DIS**	**HPR-DIS**

TH-DIS Disables the TH filter.

TH-DIS = 0	TH filter is enabled.
TH-DIS = 1	TH filter is disabled (H_{TH} = 0).

IM-DIS Disables the IM filter.

IM-DIS = 0	IM filter is enabled.
IM-DIS = 1	IM filter is disabled (H_{IM} = 0).

AX-DIS Disables the AX filter.

AX-DIS = 0	AX filter is enabled.
AX-DIS = 1	AX filter is disabled (H_{AX} = 1).

AR-DIS Disables the AR filter.

AX-DIS = 0	AR filter is enabled.
AX-DIS = 1	AR filter is disabled (H_{AR} = 1).

FRX-DIS Disables the FRX filter.

FRX-DIS = 0	FRX filter is enabled.
FRX-DIS = 1	FRX filter is disabled (H_{FRX} = 1).

FRR-DIS Disables the FRR filter.

FRR-DIS = 0	FRR filter is enabled.
FRR-DIS = 1	FRR filter is disabled (H_{FRR} = 1).

HPX-DIS Disables the high-pass filter in transmit direction.

HPX-DIS = 0	High-pass filter is enabled.
HPX-DIS = 1	High-pass filter is disabled (H_{HPX} = 1).

HPR-DIS	Disables the high-pass filter in receive direction. HPR-DIS = 0 High-pass filter is enabled. HPR-DIS = 1 High-pass filter is disabled (H_{HPR} = 1).

19_H		reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$1A_H$	DSCR	DTMF Sender Configuration Register	00_H		Y

Bit	7	6	5	4	3	2	1	0
	DG-KEY[3:0]				COR8	PTG	TG2-EN	TG1-EN

DG-KEY[3:0] Selects one of sixteen DTMF keys generated by the two tone generators. The key will be generated if both TG1-EN and TG2-EN are ‘1’.

Table 67 DTMF Keys

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DG-KEY3	DG-KEY2	DG-KEY1	DG-KEY0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

COR8 Cuts off the receive path at 8 kHz before the tone generator summation point. Allows sending of tone generator signals without overlaid voice.

COR8 = 0	Cut off receive path disabled.
COR8 = 1	Cut off receive path enabled.

PTG	Programmable coefficients for tone generators will be used.	
	PTG = 0	Frequencies set by DG-KEY are used for both tone generators.
	PTG = 1	CRAM coefficients used for both tone generators.
TG2-EN	Enables tone generator two	
	TG2-EN = 0	Tone generator is disabled.
	TG2-EN = 1	Tone generator is enabled.
TG1-EN	Enables tone generator one	
	TG1-EN = 0	Tone generator is disabled.
	TG1-EN = 1	Tone generator is enabled.

$1B_H$		reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$1C_H$	**LMCR1**	Level Metering Configuration Register 1	**22_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	TEST-EN	**0**	**1**	**PCM2DC**	**0**	**0**	**1**	**0**

TEST-EN Activates the SLICOFI-2S/-2S2 test features controlled by test registers TSTR1 to TSTR5.

TEST-EN = 0	SLICOFI-2S/-2S2 test features are disabled.
TEST-EN = 1	SLICOFI-2S/-2S2 test features are enabled.

(The Test Register bits can be programmed before the TEST-EN bit is set to 1.)

PCM2DC PCM voice channel data added to the DC-output.

PCM2DC = 0	Normal operation.
PCM2DC = 1	PCM voice channel data is added to DC-output.

$1D_H$	**LMCR2**	Level Metering Configuration Register 2	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$1E_H$	**LMCR3**	Level Metering Configuration Register 3	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	AC-SHORT-EN	**RTR-SEL**	**0**	**0**	**0**	**0**	**0**	**0**

AC-SHORT-EN The input pin ITAC will be set to a lower input impedance so that the capacitor C_{ITAC} can be recharged faster during soft reversal which makes it more silent during conversation.

AC-SHORT-EN = 0	Input impedance of the ITAC pin is standard.
AC-SHORT-EN = 1	Input impedance of the ITAC pin is lowered.

RTR-SEL Ring Trip method selection.

RTR-SEL = 0	Ring Trip with a DC offset is selected.
RTR-SEL = 1	AC Ring Trip is selected. Recommended for short lines only.

$1F_H$	**OFR1**	Offset Register 1 (High Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-H[7:0]							

OFFSET-H[7:0] Offset register high byte.

20_H	**OFR2**	Offset Register 2 (Low Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-L[7:0]							

OFFSET-L[7:0] Offset register low byte.
The value of this register together with OFFSET-H is added to the input of the DC loop to compensate a given offset of the current sensors in the SLIC-S/-S2.

21_H	**PCMR1**	PCM Receive Register 1	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	R1-HW	**R1-TS[6:0]**						

R1-HW Selection of the PCM highway for receiving PCM data or the higher byte of the first data sample if linear 16 kHz PCM mode is selected.

R1-HW = 0	PCM highway A is selected.
R1-HW = 1	PCM highway B is selected.

R1-TS[6:0] Selection of the PCM time slot used for data reception.

Note: The programmed PCM time slot must correspond to the available slots defined by the PCLK frequency. No reception will occur if a slot outside the actual numbers of slots is programmed. In linear mode (bit LIN = 1 in register BCR3) R1-TS defines the first of two consecutive slots used for reception.

22_H		reserved	00_H		Y

Bit	7	6	5	4	3	2	1	0

23_H		reserved	00_H		Y

Bit	7	6	5	4	3	2	1	0

24_H		reserved	00_H		Y

Bit	7	6	5	4	3	2	1	0

25_H	**PCMX1**	PCM Transmit Register 1	00_H		**Y**

Bit	7	6	5	4	3	2	1	0
	X1-HW	**X1-TS[6:0]**						

X1-HW Selection of the PCM highway for transmitting PCM data or the higher byte of the first data sample if linear 16 kHz PCM mode is selected.

X1-HW = 0 PCM highway A is selected.

X1-HW = 1 PCM highway B is selected.

X1-TS[6:0] Selection of the PCM time slot used for data transmission.

Note: The programmed PCM time slot must correspond to the available slots defined by the PCLK frequency. No transmission will occur if a slot outside the actual numbers of slots is programmed. In linear mode X1-TS defines the first of two consecutive slots used for transmission. PCM data transmission is controlled by bits 6 to 2 in register BCR3.

26_H		reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0

27_H		reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0

28_H		reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0

29_H	**TSTR1**	Test Register 1	00_H	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	PD-AC-PR	**PD-AC-PO**	**PD-AC-AD**	**PD-AC-DA**	**PD-AC-GN**	**PD-GNKC**	**PD-OFHC**	**PD-OVTC**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

PD-AC-PR	AC-PREFI power down	
	PD-AC-PR = 0	Normal operation.
	PD-AC-PR = 1	Power down mode.
PD-AC-PO	AC-POFI power down	
	PD-AC-PO = 0	Normal operation.
	PD-AC-PO = 1	Power down mode.
PD-AC-AD	AC-ADC power down	
	PD-AC-AD = 0	Normal operation.
	PD-AC-AD = 1	Power down mode, transmit path is inactive.
PD-AC-DA	AC-DAC power down	
	PD-AC-DA = 0	Normal operation.
	PD-AC-DA = 1	Power down mode, receive path is inactive.
PD-AC-GN	AC-Gain power down	
	PD-AC-GN = 0	Normal operation.
	PD-AC-GN = 1	Power down mode.
PD-GNKC	Ground Key comparator (GNKC) is set to power down	
	PD-GNKC = 0	Normal operation.
	PD-GNKC = 1	Power down mode.

PD-OFHC	Off-hook comparator (OFHC) power down	
	PD-OFHC = 0	Normal operation.
	PD-OFHC = 1	Power down mode.
PD-OVTC	Overtemperature comparator (OVTC) power down	
	PD-OVTC = 0	Normal operation.
	PD-OVTC = 1	Power down mode.

$2A_H$	TSTR2	Test Register 2	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	PD-DC-PR	**0**	**PD-DC-AD**	**PD-DC-DA**	**PD-DCBUF**	**0**	**PD-TTX-A**[1]	**PD-HVI**

[1] Only for DuSLIC-S, is set to 0 for DuSLIC-S2

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

PD-DC-PR DC-PREFI power down

PD-DC-PR = 0 Normal operation.

PD-DC-PR = 1 Power down mode.

PD-DC-AD DC-ADC power down

PD-DC-AD = 0 Normal operation.

PD-DC-AD = 1 Power down mode, transmit path is inactive.

PD-DC-DA DC-DAC power down

PD-DC-DA = 0 Normal operation.

PD-DC-DA = 1 Power down mode, receive path is inactive.

PD-DCBUF DC-BUFFER power down

PD-DCBUF = 0 Normal operation.

PD-DCBUF = 1 Power down mode.

PD-TTX-A TTX adaptation DAC and POFI power down

PD-TTX-A = 0 Normal operation.

PD-TTX-A = 1 Power down mode.

PD-HVI HV interface (to SLIC-S/-S2) power down

PD-HVI = 0 Normal operation.

PD-HVI = 1 Power down mode.

$2B_H$	**TSTR3**	Test Register 3	**00_H**	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**AC-DLB-4M**	**AC-DLB-128K**	**AC-DLB-32K**	**AC-DLB-8K**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

AC-DLB-4M AC digital loop via 4 MHz bitstream. (The loop encloses all digital hardware in the AC path. Together with DLB-DC a pure digital test is possible because there is no influence the analog hardware.)

AC-DLB-4M = 0	Normal operation.
AC-DLB-4M = 1	Digital loop closed.

AC-DLB-128K AC digital loop via 128 kHz

AC-DLB-128K = 0	Normal operation.
AC-DLB-128K = 1	Digital loop closed.

AC-DLB-32K AC digital loop via 32 kHz

AC-DLB-32K = 0	Normal operation.
AC-DLB-32K = 1	Digital loop closed.

AC-DLB-8K AC digital loop via 8 kHz

AC-DLB-8K = 0	Normal operation.
AC-DLB-8K = 1	Digital loop closed.

$2C_H$	**TSTR4**	Test Register 4	**00_H**	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	OPIM-AN	**OPIM-4M**	**COR-64**	**COX-16**	**0**	**0**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

OPIM-AN Open Impedance Matching Loop in the analog part.

OPIM-AN = 0	Normal operation.
OPIM-AN = 1	Loop opened.

OPIM-4M Open fast digital Impedance Matching Loop in the hardware filters.

OPIM-4M = 0	Normal operation.
OPIM-4M = 1	Loop opened.

COR-64 Cut off the AC receive path at 64 kHz (just before the IM filter).

COR-64 = 0	Normal operation.
COR-64 = 1	Receive path is cut off.

COX-16 Cut off the AC transmit path at 16 kHz. (The TH filter can be tested without influencing the analog part.)

COX-16 = 0	Normal operation.
COX-16 = 1	Transmit path is cut off.

$2D_H$	**TSTR5**	Test Register 5	**00_H**	**T**	**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**DC-POFI-HI**	**DC-HOLD**	**0**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

DC-POFI-HI	DC post filter limit frequency higher value	
	DC-POFI-HI = 0	Limit frequency is set to 100 Hz (normal operation).
	DC-POFI-HI = 1	Limit frequency is set to 300 Hz.
DC-HOLD	Actual DC output value hold (value of the last DSP filter stage will be kept)	
	DC-HOLD = 0	Normal operation.
	DC-HOLD = 1	DC output value hold.

6.3.2 COP Command

The COP command gives access to the CRAM data of the DSPs. It is organized in the same way as the SOP command. The offset value allows a direct as well as a block access to the CRAM. Writing beyond the allowed offset will be ignored, reading beyond it will give unpredictable results.
The value of a specific CRAM coefficient is calculated by the DuSLICOS software.

Bit	7	6	5	4	3	2	1	0
Byte 1	**RD**	**1**	**ADR[2:0]**			**1**	**0**	**1**
Byte 2	**OFFSET[7:0]**							

RD	Read Data
	RD = 0 Write data to chip.
	RD = 1 Read data from chip.
ADR[2:0]	Channel address for the subsequent data
	ADR[2:0] = 0 0 0 Channel A
	ADR[2:0] = 0 0 1 Channel B
	(other codes reserved for future use)

Offset [7:0]	**Short Name**	**Long Name**
00_H	TH1	Transhybrid Filter Coefficients Part 1
08_H	TH2	Transhybrid Filter Coefficients Part 2
10_H	TH3	Transhybrid Filter Coefficients Part 3
18_H	FRR	Frequency-response Filter Coefficients Receive Direction
20_H	FRX	Frequency-response Filter Coefficients Transmit Direction
28_H	AR	Amplification/Attenuation Stage Coefficients Receive
30_H	AX	Amplification/Attenuation Stage Coefficients Transmit
38_H	PTG1	Tone Generator 1 Coefficients
40_H	PTG2	Tone Generator 2 Coefficients
48_H	LPR	Low Pass Filter Coefficients Receive
50_H	LPX	Low Pass Filter Coefficients Transmit
58_H	TTX	Teletax Coefficients
60_H	IM1	Impedance Matching Filter Coefficients Part 1
68_H	IM2	Impedance Matching Filter Coefficients Part 2
70_H	RINGF	Ringer Frequency and Amplitude Coefficients (DC loop)
78_H	RAMPF	Ramp Generator Coefficients (DC loop)
80_H	DCF	DC-Characteristics Coefficients (DC loop)
88_H	HF	Hook Threshold Coefficients (DC loop)
90_H	TPF	Low Pass Filter Coefficients (DC loop)
98_H		Reserved

Table 68 CRAM Coefficients

Byte 7		Byte 6		Byte 5		Byte 4		Byte 3		Byte 2		Byte 1		Byte 0		Offset [7:0]	
Transhybrid Coefficient Part 1																00_H	TH1
	Transhybrid Coefficient Part 2															08_H	TH2
		Transhybrid Coefficient Part 3														10_H	TH3
	FIR Filter in Receive Direction															18_H	FRR
	FIR Filter in Transmit Direction															20_H	FRX
								2nd Gain Stage Receive			1st Gain Stage Receive					28_H	AR
								2nd Gain Stage Transmit			1st Gain Stage Transmit					30_H	AX
					TG1 Bandpass					TG1 Gain			TG1 Frequency			38_H	PTG1[1]
					TG2 Bandpass					TG2 Gain			TG2 Frequency			40_H	PTG2[1]
Reserved																48_H	
Reserved																50_H	
			FIR Filter for TTX								TTX Slope		TTX Level			58_H	TTX
		IM K Factor		IM FIR Filter												60_H	IM1_F
		IM 4 MHz Filter					IM WDF Filter									68_H	IM2_F
				Ring Generator Amplitude			Ring Generator Frequency			Ring Generator Lowpass			Ring Offset RO1			70_H	RINGF
		Extended Battery Feeding Gain		Soft Reversal End			Constant Ramp CR			Soft Ramp SS			Ring Delay RD			78_H	RAMPF
Res. in Resistive Zone R_{K12}			Res. in Constant Current Zone R_I			Constant Current I_{K1}				Knee Voltage V_{K1}			Open Circuit Volt. V_{LIM}			80_H	DCF
	Hook Message Waiting			Hook Threshold AC Ring Trip			Hook Threshold Ring			Hook Threshold Active			Hook Threshold Power Down			88_H	HF
						Voltage Level VRT			DC Lowpass Filter TP2			DC Lowpass Filter TP1				90_H	TPF
Reserved																98_H	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

Note: CRAM coefficients are enabled by setting bit CRAM-EN in register BCR3 to 1, except coefficients PTG1 and PTG2[1] *which are enabled by setting bit PTG in register DSCR to 1.*

6.3.2.1 CRAM Programming Ranges

Table 69 CRAM Programming Ranges

Parameter	Programming Range
Constant Current I_{K1}	0...50 mA, Δ < 0.5 mA
Hook Message Waiting, Hook Thresholds	0..25 mA, Δ < 0.7 mA 25...50 mA, Δ < 1.3 mA
Ring Generator Frequency f_{RING}	3..40 Hz, Δ < 1 Hz 40..80 Hz, Δ < 2 Hz > 80 Hz, Δ < 4 Hz
Ring Generator Amplitude	0..20 V, Δ < 1.7 V 20..85 V, Δ < 0.9 V
Ring Offset RO1	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V 50..100 V, Δ < 2.4 V, max. 150 V
Knee Voltage V_{K1}, Open Circuit Voltge V_{LIM}	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V > 50 V, Δ < 2.4 V
Resistance in Resistive Zone R_{K12}	0..1000 Ω, Δ < 30 Ω
Resistance in Constant Current Zone R_I	1.8 kΩ..4.8 kΩ, Δ < 120 Ω 4.8 kΩ..9.6 kΩ, Δ < 240 Ω 9.6 kΩ..19 kΩ, Δ < 480 Ω 19 kΩ..38 kΩ, Δ < 960 Ω, max. 40 kΩ

6.3.3 IOM-2 Interface Command/Indication Byte

The Command/Indication (C/I) channel is used to communicate real time status information and for fast controlling of the DuSLIC. Data on the C/I channel are continuously transmitted in each frame until new data are sent.

Data Downstream C/I – Channel Byte (Receive) – IOM-CIDD

The first six CIDD data bits control the general operating modes for both DuSLIC channels. According to the IOM-2 specification, new data have to be present for at least two frames to be accepted.

Table 70 M2, M1, M0: General Operating Mode

CIDD			**SLICOFI-2S/-2S2 Operating Mode** (for details see **"Operating Modes for the DuSLIC Chip Set" on Page 78**)
M2	**M1**	**M0**	
1	1	1	Sleep, Power Down (PDRx)
0	0	0	Power Down High Impedance (PDH)
0	1	0	Any Active mode
1	0	1	Ringing (ACTR Burst On)
1	1	0	Active with Metering
1	0	0	Ground Start
0	0	1	Ring Pause

	CIDD	Data Downstream C/I – Channel Byte			**N**

Bit	7	6	5	4	3	2	1	0
	M2A	**M1A**	**M0A**	**M2B**	**M1B**	**M0B**	**MR**	**MX**

M2A, M1A, M0A	Select operating mode for DuSLIC channel A
M2B, M1B, M0B	Select operating mode for DuSLIC channel B
MR, MX	Handshake bits Monitor Receive and Transmit (see **"IOM-2 Interface Monitor Transfer Protocol" on Page 148**)

Data Upstream C/I – Channel Byte (Transmit) – IOM-CIDU

This byte is used to quickly transfer the most important and time-critical information from the DuSLIC. Each transfer from the DuSLIC lasts for at least two consecutive frames.

	CIDU	Data Upstream C/I – Channel Byte	**00$_H$**		**N**

Bit	7	6	5	4	3	2	1	0
	INT-CHA	**HOOKA**	**GNDKA**	**INT-CHB**	**HOOKB**	**GNDKB**	**MR**	**MX**

INT-CHA Interrupt information channel A

INT-CHA = 0	No interrupt in channel A
INT-CHA = 1	Interrupt in channel A

HOOKA Hook information channel A

HOOKA = 0	On-hook channel A
HOOKA = 1	Off-hook channel A

GNDKA Ground key information channel A

GNDKA = 0	No longitudinal current detected
GNDKA = 1	Longitudinal current detected in channel A

INT-CHB Interrupt information channel B

INT-CHB = 0	No interrupt in channel B
INT-CHB = 1	Interrupt in channel B

HOOKB Hook information channel B

HOOKB = 0	On-hook Channel B
HOOKB = 1	Off-hook Channel B

GNDKB Ground key information channel B

GNDKB = 0	No longitudinal current detected
GNDKB = 1	Longitudinal current detected in channel B

MR, MX Handshake bits Monitor Receive and Transmit
(see **“IOM-2 Interface Monitor Transfer Protocol” on Page 148**)

6.3.4 Programming Examples of the SLICOFI-2S/-2S2

6.3.4.1 Microcontroller Interface

SOP Write to Channel 0 Starting After the Channel-Specific Read-Only Registers

01000100	First command byte (SOP write for channel 0)
00010101	Second command byte (offset to BCR1 register)
00000000	Contents of BCR1 register
00000000	Contents of BCR2 register
00010001	Contents of BCR3 register
00000000	Contents of BCR4 register
00000000	Contents of BCR5 register

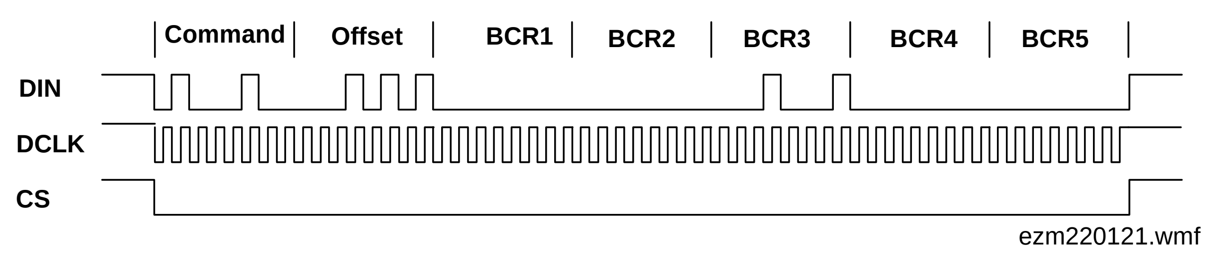

Command
Offset
BCR1
BCR2
BCR3
BCR4
BCR5
DIN
DCLK
CS
ezm220121.wmf

Figure 76 Waveform of Programming Example SOP Write to Channel 0

SOP Read from Channel 1 Reading Out the Interrupt Registers

11001100	First command byte (SOP read for channel 1).
00000111	Second command byte (offset to Interrupt register 1).

The SLICOFI-2S/-2S2 will send data when it has completely received the second command byte.

11111111	Dump byte (this byte is always FF_H).
11000000	Interrupt register INTREG1 (an interrupt has occurred, Off-hook was detected).
00000010	Interrupt register INTREG2 (IO pin 2 is ‘1’).
00000000	Interrupt register INTREG3
00000000	Interrupt register INTREG4

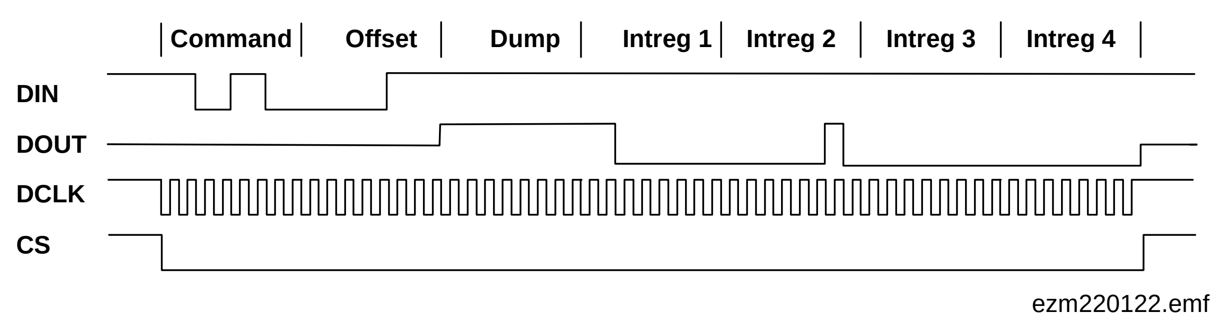

Command
Offset
Dump
Intreg 1
Intreg 2
Intreg 3
Intreg 4
DIN
DOUT
DCLK
CS
ezm220122.emf

Figure 77 Waveform of Programming Example SOP Read from Channel 0

6.3.4.2 IOM-2 Interface

An example with the same programming sequence as before, using the IOM-2 interface is presented here to show the differences between the microcontroller interface and the IOM-2 interface.

SOP Write to Channel 0 Starting After the Channel-Specific Read-Only Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	11111111	11	IOM-2 address first byte
10000001	10	11111111	01	IOM-2 address second byte
01000100	11	11111111	01	First command byte (SOP write for channel 0)
01000100	10	11111111	11	First command byte second time
00010101	11	11111111	01	Second command byte (offset to BCR1 register)
00010101	10	11111111	11	Second command byte second time
00000000	11	11111111	01	Contents of BCR1 register
00000000	10	11111111	11	Contents of BCR1 register second time
00000000	11	11111111	01	Contents of BCR2 register
00000000	10	11111111	11	Contents of BCR2 register second time
00010001	11	11111111	01	Contents of BCR3 register
00010001	10	11111111	11	Contents of BCR3 register second time
00000000	11	11111111	01	Contents of BCR4 register
00000000	10	11111111	11	Contents of BCR4 register second time
11111111	11	11111111	01	No more information (dummy byte)
11111111	11	11111111	11	Signaling EOM (end of message) by holding MX bit at ‘1’.

Since the SLICOFI-2S/-2S2 has an open command structure, no fixed command length is given. The IOM-2 handshake protocol allows for an infinite length of a data stream, therefore the host has to terminate the data transfer by sending an end-of-message signal (EOM) to the SLICOFI-2S/-2S2. The SLICOFI-2S/-2S2 will abort the transfer only if the host tries to write or read beyond the allowed maximum offsets given by the different types of commands. Each transfer has to start with the SLICOFI-2S/-2S2-specific IOM-2 Address (81_H) and must end with an EOM of the handshake bits. Appending a command immediately to its predecessor without an EOM in between is not allowed.

When reading interrupt registers, SLICOFI-2S/-2S2 stops the transfer after the fourth register in IOM-2 mode. This is to prevent some host chips reading 16 bytes because they can’t terminate the transfer after n bytes.

SOP-Read from Channel 1 Reading Out the Interrupt Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	11111111	11	IOM-2 address first byte
10000001	10	11111111	01	IOM-2 address second byte
11001100	11	11111111	01	First command byte (SOP read for channel 1)
11001100	10	11111111	11	First command byte second time
00001000	11	11111111	01	Second command byte (offset to interrupt register 1)
00001000	10	11111111	11	Second command byte second time
11111111	11	11111111	01	Acknowledgement for the second command byte
11111111	11	10000001	10	IOM-2 Address first byte (answer)
11111111	01	10000001	10	IOM-2 Address second byte
11111111	01	11000000	11	Interrupt register INTREG1
11111111	11	11000000	10	Interrupt register INTREG1 second time
11111111	01	00000010	11	Interrupt register INTREG2
11111111	11	00000010	10	Interrupt register INTREG2 second time
11111111	01	00000000	11	Interrupt register INTREG3
11111111	11	00000000	10	Interrupt register INTREG3 second time
11111111	01	00000000	11	Interrupt register INTREG4
11111111	11	00000000	10	Interrupt register INTREG4 second time
11111111	11	01001101	11	SLICOFI-2S/-2S2 sends the next register
11111111	11	11111111	11	SLICOFI-2S/-2S2 aborts transmission

7 Electrical Characteristics

7.1 Electrical Characteristics PEB 4264/-2 (SLIC-S/-S2)

7.1.1 Absolute Maximum Ratings PEB 4264/-2 (SLIC-S/-S2)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L	V_{BATL} $V_{\mathrm{BATL}} - V_{\mathrm{BATH}}$	– 65 – 0.4	0.4	V	referred to V_{BGND}
Battery voltage	V_{BATH}	– 70	0.4	V	referred to V_{BGND}
Auxiliary supply voltage	V_{HR}	– 0.4	50	V	referred to V_{BGND}
Total battery supply voltage, continuous	$V_{\mathrm{HR}} - V_{\mathrm{BATH}}$	– 0.4	95	V	–
V_{DD} supply voltage	V_{DD}	– 0.4	7	V	referred to V_{AGND}
Ground voltage difference	$V_{\mathrm{BGND}} - V_{\mathrm{AGND}}$	– 0.4	0.4	V	–
Input voltages	V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{C1}, V_{C2}, V_{CMS}	– 0.4	$V_{\mathrm{DD}} + 0.4$	V	referred to V_{AGND}
Voltages on current outputs	V_{IT}, V_{IL}	– 0.4	$V_{\mathrm{DD}} + 0.4$	V	referred to V_{AGND}
RING, TIP voltages, continuous	V_{R}, V_{T}	$V_{\mathrm{BATL}} - 0.4$	0.4	V	ACTL
		$V_{\mathrm{BATH}} - 0.4$	0.4	V	ACTH, PDRH, PDRHL
		$V_{\mathrm{BATH}} - 0.4$	$V_{\mathrm{HR}} + 0.4$	V	ACTR, PDH, HIT, HIR
RING,TIP voltages, pulse < 10 ms	V_{R}, V_{T}	t.b.d	t.b.d	V	all modes
RING,TIP voltages, pulse < 1 ms	V_{R}, V_{T}	$V_{\mathrm{BATH}} - 10$	$V_{\mathrm{HR}} + 10$	V	all modes
RING, TIP voltages, pulse < 1 µs	V_{R}, V_{T}	$V_{\mathrm{BATH}} - 10$	$V_{\mathrm{HR}} + 30$	V	all modes

7.1.1 Absolute Maximum Ratings PEB 4264/-2 (SLIC-S/-S2) (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model)[1]
Junction temperature	T_j	–	150 [2]	°C	

[1] EOS/ESD Assn. Standard DS5.3-1993.

[2] Even higher value is possible when internal junction temperature protection is operative.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum ratings are absolute ratings; even if only one of these values is exceeded, the integrated circuit may be irreversibly damaged.

7.1.2 Operating Range PEB 4264/-2 (SLIC-S/-S2)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L[1]	V_{BATL}	– 60	– 15	V	referred to V_{BGND}
Battery voltage H[1]	V_{BATH}	– 65	– 20	V	referred to V_{BGND}
Auxiliary supply voltage	V_{HR}	5	45	V	referred to V_{BGND}
Total battery supply voltage	$V_{HR} - V_{BATH}$	–	90	V	–
V_{DD} supply voltage	V_{DD}	4.75	5.25	V	referred to V_{AGND}
Ground voltage difference	$V_{BGND} - V_{AGND}$	– 0.4	0.4	V	–
Junction temperature	T_j	–	125	°C	simulated for a lifetime of 15 years
Voltage at pins IT, IL	V_{IT}, V_{IL}	– 0.4	3.5	V	referred to V_{AGND}
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	referred to V_{AGND}

[1] If the battery switch is not used both pins VBATL and VBATH should be connected together externally. In this case the full voltage range of – 15 V to – 65 V can be used.

7.1.3 Thermal Resistances PEB 4264/-2 (SLIC-S/-S2)

Parameter	Symbol	Limit Values	Unit	Test Condition
Junction to case	$R_{th, jC}$	< 2	K/W	–
Junction to ambient	$R_{th, jA}$	< 50	K/W	without heatsink

7.1.4 Electrical Parameters PEB 4264/-2 (SLIC-S/-S2)

Minimum and maximum values are valid within the full operating range.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extented temperature range operation at – 40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Testing is performed according to the specific test figures. Unless otherwise stated, load impedance R_L = 600 Ω, V_{BATH} = – 48 V, V_{BATL} = – 24 V, V_{HR} = + 32 V and V_{DD} = + 5 V, R_{IT} = 1 kΩ, R_{IL} = 2 kΩ, C_{EXT} = 470 nF. Typical values are tested at T_A = 25 °C.

Supply Currents and Power Dissipation

($I_R = I_T$ = 0 A; $V_{CMS} = V_{ACP} = V_{ACN} = V_{DCP} = V_{DCN}$ = 1.5 V)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	
Power Down High Impedance, Power Down Resistive High							
1. 2.	V_{DD} current	I_{DD}	PDH PDRH	– –	120 120	– –	µA
3. 4.	V_{BATH} current	I_{BATH}	PDH PDRH	– –	65 80	– –	µA
5. 6.	V_{BATL} current	I_{BATL}	PDH PDRH	– –	0 0	– –	µA
7. 8.	V_{HR} current	I_{HR}	PDH PDRH	– –	0 0	– –	µA
9. 10.	Quiescent power dissipation	P_Q	PDH PDRH	– –	3.7 4.4	– –	mW
Active Low							
11.	V_{DD} current	I_{DD}	ACTL	–	1000	1200	µA
12.	V_{BATH} current	I_{BATH}	ACTL	–	25	45	µA
13.	V_{BATL} current	I_{BATL}	ACTL	–	2800	3400	µA
14.	V_{HR} current	I_{HR}	ACTL	–	0	10	µA
15.	Quiescent power dissipation	P_Q	ACTL	–	73.4	89.8	mW

Supply Currents and Power Dissipation

($I_R = I_T = 0$ A; $V_{CMS} = V_{ACP} = V_{ACN} = V_{DCP} = V_{DCN} = 1.5$ V) (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	
Active High							
16.	V_{DD} current	I_{DD}	ACTH	–	1000	1300	µA
17.	V_{BATH} current	I_{BATH}	ACTH	–	3500	4300	µA
18.	V_{BATL} current	I_{BATL}	ACTH	–	0	10	µA
19.	V_{HR} current	I_{HR}	ACTH	–	0	10	µA
20.	Quiescent power dissipation	P_Q	ACTH	–	173	213.5	mW
Active Ring							
21.	V_{DD} current	I_{DD}	ACTR	–	500	700	µA
22.	V_{BATH} current	I_{BATH}	ACTR	–	3100	3700	µA
23.	V_{BATL} current	I_{BATL}	ACTR	–	0	10	µA
24.	V_{HR} current	I_{HR}	ACTR	–	2300	2800	µA
25.	Quiescent power dissipation	P_Q	ACTR	–	225	271	mW
High Impedance on RING, High Impedance on TIP							
26.	V_{DD} current	I_{DD}	HIR, HIT	–	500	700	µA
27.	V_{BATH} current	I_{BATH}	HIR, HIT	–	2100	2600	µA
28.	V_{BATL} current	I_{BATL}	HIR, HIT	–	0	10	µA
29.	V_{HR} current	I_{HR}	HIR, HIT	–	1500	2200	µA
30.	Quiescent power dissipation	P_Q	HIR, HIT	–	151	199	mW

7.1.5 Power Calculation PEB 4264/-2 (SLIC-S/-S2)

The total power dissipation consists of the quiescent power dissipation P_Q given above, the current sensor power dissipation P_I (see **Table 71**), the gain stage power dissipation correction P_G[1] (see **Table 72**) and the output stage power dissipation P_O (see **Table 73**):

$$P_{tot} = P_Q + P_I + P_G + P_O$$

with $P_Q = V_{DD} \times I_{DD} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL} + V_{HR} \times I_{HR}$

For the calculation of P_I, P_G and P_O see the following tables:

Table 71 **P_I Calculation PEB 4264/-2 (SLIC-S/-S2)**

Operating Mode	**Equation for P_I Calculation**
PDH	$P_I = 0$ (no DC loop current)
PDRH, PDRHL	$P_I = I_{Trans} \times I_{Trans} \times (10000 + 500 + 16) + I_{Trans} \times (0.6 + 0.425 \times \lvert V_{BATH}\rvert)$
ACTL	$P_I = 0.055 \times I_{Trans} \times \lvert V_{BATL}\rvert + 0.04 \times I_{Trans} \times V_{DD}$
ACTH	$P_I = 0.055 \times I_{Trans} \times \lvert V_{BATH}\rvert + 0.04 \times I_{Trans} \times V_{DD}$
ACTR	$P_I = 0.015 \times I_{Trans} \times V_{HR} + 0.055 \times I_{Trans} \times \lvert V_{BATH}\rvert + 0.04 \times I_{Trans} \times V_{DD}$
HIR, HIT	$P_I = 0.015 \times I_{TorR}{}^{1)} \times V_{HR} + 0.04 \times I_{TorR} \times \lvert V_{BATH}\rvert + 0.02 \times I_{TorR} \times V_{DD}$
HIRT	$P_I = 0$ (no DC loop current)

1) $I_{TorR} = I_{TIP}$ or I_{RING}

.

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[1] The gain stage power dissipation correction P_G is a correcting term necessary to ensure a correct power calculation if other as the defined supply voltages are used.

Table 72 P_G **Calculation PEB 4264/-2 (SLIC-S/-S2)**

Operating Mode	Equation for P_G Calculation
PDH, PDRH	P_G = 0 (gain stage not working)
ACTL	$P_G = (V_{BATL}{}^2 - 24^2) \times (1/60k + 1/216k)$
ACTH, PDRHL	$P_G = (V_{BATH}{}^2 - 48^2) \times (1/60k + 1/216k)$
ACTR	$P_G = (V_{HR} + \lvert V_{BATH}\rvert) \times (\lvert V_{HR} + V_{BATH} + V_{TIP/RING}\rvert +$ $\lvert V_{HR} + V_{BATH} - V_{TIP/RING}\rvert - 2 \times \lvert V_{HR} + V_{BATH}\rvert)/120k +$ $(V_{HR}{}^2 - 32^2 + V_{BATH}{}^2 - 48^2) \times (1/60k + 1/216k)$
HIR, HIT, HIRT	$P_G = (V_{HR} + \lvert V_{BATH}\rvert) \times (\lvert V_{HR} + V_{BATH} + \exp V_{TIP/RING}{}^{1)}\rvert +$ $\lvert V_{HR} + V_{BATH} - V_{TIP/RING}\rvert - 2 \times \lvert V_{HR} + V_{BATH}\rvert)/120k +$ $(V_{HR}{}^2 - 32^2 + V_{BATH}{}^2 - 48^2) \times (1/60k + 1/216k)$

1) Expected $V_{TIP/RING}$ when SLIC-S/-S2 output buffer in high impedance.

Table 73 P_O **Calculation PEB 4264/-2 (SLIC-S/-S2)**

Operating Mode	Equation for P_O Calculation
PDH, PDRH, PDRHL	P_O = 0 (output stage not working)
ACTL	$P_O = (\lvert V_{BATL}\rvert - V_{TIP/RING}) \times I_{Trans}$
ACTH	$P_O = (\lvert V_{BATH}\rvert - V_{TIP/RING}) \times I_{Trans}$
ACTR	$P_O = (V_{HR} + \lvert V_{BATH}\rvert - V_{TIP/RING}) \times I_{Trans}$
HIR, HIT	$P_O = V_{Supply\text{-}TorR}{}^{1)} \times I_{TorR}$
HIRT	P_O = 0 (output stage not working)

1) $V_{Supply\text{-}TorR} = V_{Supply} - V_{TIP}$ or V_{RING}

7.1.6 Power Up Sequence PEB 4264/-2 (SLIC-S/-S2)

The supply voltages of the SLIC-S/-S2 have to be applied in the following order to the respective pin:

1) Ground to pins AGND and BGND
2) V_{DD} to pin VDD
3) V_{BATH} to pin VBATH
4) V_{HR} to pin VHR and V_{BATL} to pin VBATL

If the V_{DD} voltage is applied more than one second later as V_{BATH}, V_{HR} or V_{BATL} thermal damage of the SLIC-S/-S2 can accur.

If the above sequence of the battery voltages can not be guaranteed, a diode (1N4007) has to be inserted in the VBATH line

7.2 Electrical Characteristics PEB 4265/-2 (SLIC-E/-E2)

7.2.1 Absolute Maximum Ratings PEB 4265/-2 (SLIC-E/-E2)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L	V_{BATL} $V_{\mathrm{BATL}} - V_{\mathrm{BATH}}$	– 85 – 0.4	0.4 –	V V	referred to V_{BGND}
Battery voltage H	V_{BATH}	– 90	0.4	V	referred to V_{BGND}
Auxiliary supply voltage	V_{HR}	– 0.4	90	V	referred to V_{BGND}
Total battery supply voltage, continuous	$V_{\mathrm{HR}} - V_{\mathrm{BATH}}$	–	160	V	–
V_{DD} supply voltage	V_{DD}	– 0.4	7	V	referred to V_{AGND}
Ground voltage difference	$V_{\mathrm{BGND}} - V_{\mathrm{AGND}}$	– 0.4	0.4	V	–
Input voltages	V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{C1}, V_{C2}, V_{CMS}	– 0.4	$V_{\mathrm{DD}} + 0.4$	V	referred to V_{AGND}
Voltages on current outputs	V_{IT}, V_{IL}	– 0.4	$V_{\mathrm{DD}} + 0.4$	V	referred to V_{AGND}
RING, TIP voltages, continuous	V_{R}, V_{T}	$V_{\mathrm{BATL}} - 0.4$ $V_{\mathrm{BATH}} - 0.4$ $V_{\mathrm{BATH}} - 0.4$	0.4 0.4 $V_{\mathrm{HR}} + 0.4$	V V V	ACTL ACTH, PDRH, PDRHL ACTR, PDH, HIRT, HIT, HIR
RING, TIP voltages, pulse < 10 ms	V_{R}, V_{T}	t.b.d	t.b.d	V	all modes
RING, TIP voltages, pulse < 1 ms	V_{R}, V_{T}	$V_{\mathrm{BATH}} - 10$	$V_{\mathrm{HR}} + 10$	V	all modes
RING, TIP voltages, pulse < 1 µs	V_{R}, V_{T}	$V_{\mathrm{BATH}} - 10$	$V_{\mathrm{HR}} + 30$	V	all modes
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model)[1]
Junction temperature	T_{j}	–	150 [2]	°C	

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[1] EOS/ESD Assn. Standard DS5.3-1993.

[2] Even higher value is possible when internal junction temperature protection is operative.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; even if only one of these values is exceeded, the integrated circuit may be irreversibly damaged.

7.2.2 Operating Range PEB 4265/-2 (SLIC-E/-E2)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L[1]	V_{BATL}	– 80	– 15	V	referred to V_{BGND}
Battery voltage H[1]	V_{BATH}	– 85	– 20	V	referred to V_{BGND}
Auxiliary supply voltage	V_{HR}	5	85	V	referred to V_{BGND}
Total battery supply voltage	$V_{HR} – V_{BATH}$	–	150	V	–
V_{DD} supply voltage	V_{DD}	4.75	5.25	V	referred to V_{AGND}
Ground voltage difference	$V_{BGND} – V_{AGND}$	– 0.4	0.4	V	–
Junction temperature	T_j	–	125	°C	simulated for a lifetime of 15 years
Voltage at pins IT, IL	V_{IT}, V_{IL}	– 0.4	3.5	V	referred to V_{AGND}
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	referred to V_{AGND}

[1] If the battery switch is not used both pins VBATL and VBATH should be connected together externally. In this case the full voltage range of – 15 V to – 85 V can be used.

7.2.3 Thermal Resistances PEB 4265/-2 (SLIC-E/-E2)

Parameter	Symbol	Limit Values	Unit	Test Condition
Junction to case	$R_{th, jC}$	< 2	K/W	–
Junction to ambient	$R_{th, jA}$	< 50	K/W	without heatsink

7.2.4 Electrical Parameters PEB 4265/-2 (SLIC-E/-E2)

Minimum and maximum values are valid within the full operating range.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extented temperature range operation at – 40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Testing is performed according to the specific test figures. Unless otherwise stated, load impedance R_L = 600 Ω, V_{BATH} = – 48 V, V_{BATL} = – 24 V, V_{HR} = + 32 V and V_{DD} = + 5 V, R_{IT} = 1 kΩ, R_{IL} = 2 kΩ, C_{EXT} = 470 nF. Typical values are tested at T_A = 25 °C.

Supply Currents and Power Dissipation
($I_R = I_T$ = 0 A; $V_{CMS} = V_{ACP} = V_{ACN} = V_{DCP} = V_{DCN}$ = 1.5 V)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	
Power Down High Impedance, Power Down Resistive High							
1. 2.	V_{DD} current	I_{DD}	PDH PDRH	– –	120 120	– –	µA
3. 4.	V_{BATH} current	I_{BATH}	PDH PDRH	– –	65 80	– –	µA
5. 6.	V_{BATL} current	I_{BATL}	PDH PDRH	– –	0 0	– –	µA
7. 8.	V_{HR} current	I_{HR}	PDH PDRH	– –	0 0	– –	µA
9. 10.	Quiescent power dissipation	P_Q	PDH PDRH	– –	3.7 4.4	– –	mW
Active Low							
11.	V_{DD} current	I_{DD}	ACTL	–	1000	1200	µA
12.	V_{BATH} current	I_{BATH}	ACTL	–	25	45	µA
13.	V_{BATL} current	I_{BATL}	ACTL	–	2800	3400	µA
14.	V_{HR} current	I_{HR}	ACTL	–	0	10	µA
15.	Quiescent power dissipation	P_Q	ACTL	–	73.4	89.8	mW

Supply Currents and Power Dissipation

(I_R = I_T = 0 A; V_{CMS} = V_{ACP} = V_{ACN} = V_{DCP} = V_{DCN} = 1.5 V) (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	
Active High							
16.	V_{DD} current	I_{DD}	ACTH	–	1000	1300	µA
17.	V_{BATH} current	I_{BATH}	ACTH	–	3500	4300	µA
18.	V_{BATL} current	I_{BATL}	ACTH	–	0	10	µA
19.	V_{HR} current	I_{HR}	ACTH	–	0	10	µA
20.	Quiescent power dissipation	P_Q	ACTH	–	173	213.5	mW
Active Ring							
21.	V_{DD} current	I_{DD}	ACTR	–	500	700	µA
22.	V_{BATH} current	I_{BATH}	ACTR	–	3100	3700	µA
23.	V_{BATL} current	I_{BATL}	ACTR	–	0	10	µA
24.	V_{HR} current	I_{HR}	ACTR	–	2300	2800	µA
25.	Quiescent power dissipation	P_Q	ACTR	–	225	271	mW
High Impedance on RING, High Impedance on TIP							
26.	V_{DD} current	I_{DD}	HIR, HIT	–	500	700	µA
27.	V_{BATH} current	I_{BATH}	HIR, HIT	–	2100	2600	µA
28.	V_{BATL} current	I_{BATL}	HIR, HIT	–	0	10	µA
29.	V_{HR} current	I_{HR}	HIR, HIT	–	1500	2200	µA
30.	Quiescent power dissipation	P_Q	HIR, HIT	–	151	199	mW
High Impedance on RING and TIP							
31.	V_{DD} current	I_{DD}	HIRT	–	500	700	µA
32.	V_{BATH} current	I_{BATH}	HIRT	–	1000	1500	µA
33.	V_{BATL} current	I_{BATL}	HIRT	–	0	10	µA
34.	V_{HR} current	I_{HR}	HIRT	–	600	800	µA
35.	Quiescent power dissipation	P_Q	HIRT	–	69.7	101.3	mW

7.2.5 Power Calculation PEB 4265/-2 (SLIC-E/-E2)

The total power dissipation consists of the quiescent power dissipation P_Q given above, the current sensor power dissipation P_I (see **Table 74**), the gain stage power dissipation correction P_G[1] (see **Table 75**) and the output stage power dissipation PO (see **Table 76**):

$$P_{tot} = P_Q + P_I + P_G + P_O$$

with $P_Q = V_{DD} \times I_{DD} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL} + V_{HR} \times I_{HR}$

For the calculation of P_I, P_G and P_O see the following tables:

Table 74 P_I Calculation PEB 4265/-2 (SLIC-E/-E2)

Operating Mode	Equation for P_I Calculation
PDH	$P_I = 0$ (no DC loop current)
PDRH, PDRHL	$P_I = I_{Trans} \times I_{Trans} \times (10000 + 500 + 16) + I_{Trans} \times (0.6 + 0.425 \times \|V_{BATH}\|)$
ACTL	$P_I = 0.055 \times I_{Trans} \times \|V_{BATL}\| + 0.04 \times I_{Trans} \times V_{DD}$
ACTH	$P_I = 0.055 \times I_{Trans} \times \|V_{BATH}\| + 0.04 \times I_{Trans} \times V_{DD}$
ACTR	$P_I = 0.015 \times I_{Trans} \times V_{HR} + 0.055 \times I_{Trans} \times \|V_{BATH}\| + 0.04 \times I_{Trans} \times V_{DD}$
HIR, HIT	$P_I = 0.015 \times I_{TorR} \times V_{HR} + 0.04 \times I_{TorR} \times \|V_{BATH}\| + 0.02 \times I_{TorR} \times V_{DD}$
HIRT	$P_I = 0$ (no DC loop current)

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[1] The gain stage power dissipation correction P_G is a correcting term necessary to ensure a correct power calculation if other as the defined supply voltages are used.

Table 75 P_G Calculation PEB 4265/-2 (SLIC-E/-E2)

Operating Mode	Equation for P_G Calculation
PDH, PDRH	$P_G = 0$ (gain stage not working)
ACTL	$P_G = (V_{BATL}^2 - 24^2) \times (1/60k + 1/216k)$
ACTH, PDRHL	$P_G = (V_{BATH}^2 - 48^2) \times (1/60k + 1/216k)$
ACTR	$P_G = (V_{HR} + \lvert V_{BATH}\rvert) \times (\lvert V_{HR} + V_{BATH} + V_{TIP/RING}\rvert +$ $\lvert V_{HR} + V_{BATH} - V_{TIP/RING}\rvert - 2 \times \lvert V_{HR} + V_{BATH}\rvert)/120k +$ $(V_{HR}^2 - 32^2 + V_{BATH}^2 - 48^2) \times (1/60k + 1/216k)$
HIR, HIT, HIRT	$P_G = (V_{HR} + \lvert V_{BATH}\rvert) \times (\lvert V_{HR} + V_{BATH} + \exp V_{TIP/RING}{}^{1)}\rvert +$ $\lvert V_{HR} + V_{BATH} - \exp V_{TIP/RING}\rvert - 2 \times \lvert V_{HR} + V_{BATH}\rvert)/120k +$ $(V_{HR}^2 - 32^2 + V_{BATH}^2 - 48^2) \times (1/60k + 1/216k)$

1) Expected $V_{TIP/RING}$ when SLIC-E/-E2 output buffer in high impedance.

Table 76 P_O Calculation PEB 4265/-2 (SLIC-E/-E2)

Operating Mode	Equation for P_O Calculation
PDH, PDRH, PDRHL	$P_O = 0$ (output stage not working)
ACTL	$P_O = (\lvert V_{BATL}\rvert - V_{TIP/RING}) \times I_{Trans}$
ACTH	$P_O = (\lvert V_{BATH}\rvert - V_{TIP/RING}) \times I_{Trans}$
ACTR	$P_O = (V_{HR} + \lvert V_{BATH}\rvert - V_{TIP/RING}) \times I_{Trans}$
HIR, HIT	$P_O = V_{Supply-TorR} \times I_{TorR}$
HIRT	$P_O = 0$ (output stage not working)

7.2.6 Power Up Sequence PEB 4265/-2 (SLIC-E/-E2)

The supply voltages of the SLIC-E/-E2 have to be applied in the following order to the respective pin:

1) Ground to pins AGND and BGND
2) V_{DD} to pin VDD
3) V_{BATH} to pin VBATH
4) V_{HR} to pin VHR and V_{BATL} to pin VBATL

If the V_{DD} voltage is applied more than one second later as V_{BATH}, V_{HR} or V_{BATL} thermal damage of the SLIC-E/-E2 can accur.

If the above sequence of the battery voltages can not be guaranteed, a diode (1N4007) has to be inserted in the VBATH line.

7.3 Electrical Characteristics PEB 4266 (SLIC-P)

7.3.1 Absolute Maximum Ratings PEB 4266 (SLIC-P)

Parameter	**Symbol**	**Limit Values**		**Unit**	**Test Condition**
		min.	**max.**		
Battery voltage L	V_{BATL} $V_{BATL} - V_{BATH}$	– 145 – 0.4	0.4	V	referred to V_{BGND}
Battery voltage H	V_{BATH}	– 150	0.4	V	referred to V_{BGND}
Battery voltage R	V_{BATR} $V_{BATH} - V_{BATR}$	– 155 – 0.4	0.4	V	referred to V_{BGND}
Total battery supply voltage, continuous	$V_{DD} - V_{BATR}$	–	160	V	–
V_{DD} supply voltage	V_{DD}	– 0.4	7	V	referred to V_{AGND}
Ground voltage difference	$V_{BGND} - V_{AGND}$	– 0.4	0.4	V	–
Input voltages	V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{CMS} V_{C1}, V_{C2}, V_{C3}	– 0.4	$V_{DD} + 0.4$	V	referred to V_{AGND}
Voltages on current outputs	V_{IT}, V_{IL}	– 0.4	$V_{DD} + 0.4$	V	referred to V_{AGND}
RING, TIP voltages, continuous	V_R, V_T	$V_{BATL} - 0.4$ $V_{BATH} - 0.4$ $V_{BATR} - 0.4$	+ 0.4 + 0.4 + 0.4	V V V	ACTL ACTH, PDRH, PDRHL ACTR, PDH, PDRR, PDRRL, HIRT, HIT, HIT, ROT, ROR
RING,TIP voltages, pulse < 10 ms	V_R, V_T	t.b.d	t.b.d	V	all modes
RING,TIP voltages, pulse < 1 ms	V_R, V_T	$V_{BATR} - 10$	+ 10	V	all modes
RING, TIP voltages, pulse < 1 µs	V_R, V_T	$V_{BATR} - 10$	+ 30	V	all modes

7.3.1 Absolute Maximum Ratings PEB 4266 (SLIC-P) (cont'd)

Parameter	**Symbol**	**Limit Values**		**Unit**	**Test Condition**
		min.	**max.**		
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model)[1]
Junction temperature	T_j	–	150 [2]	°C	

[1] EOS/ESD Assn. Standard DS5.3-1993.

[2] Even higher value is possible when internal junction temperature protection is operative.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum ratings are absolute ratings; even if only one of these values is exceeded, the intergated circuit may be irreversibly damaged.

7.3.2 Operating Range PEB 4266 (SLIC-P)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L[1]	V_{BATL}	– 140	– 15	V	referred to V_{BGND}
Battery voltage H[1]	V_{BATH}	– 145	– 20	V	referred to V_{BGND}
Battery voltage R[1]	V_{BATR}	– 150	– 25	V	referred to V_{BGND}
Total battery supply voltage	$V_{\mathrm{DD}} - V_{\mathrm{BATR}}$	–	155	V	–
V_{DD} supply voltage	V_{DD}	3.1	5.5	V	referred to V_{AGND}
Ground voltage difference	$V_{\mathrm{BGND}} - V_{\mathrm{AGND}}$	– 0.4	0.4	V	–
Junction temperature	T_{j}	–	125	°C	simulated for a lifetime of 15 years
Voltage at pins IT, IL	V_{IT}, V_{IL}	– 0.4	3.5	V	referred to V_{AGND}
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	referred to V_{AGND}

[1] Internal ringing: If the battery switch is not used both pins VBATL and VBATH should be connected together externally. In this case the full voltage range of – 15 V to – 145 V can be used.
External ringing: If only one negative battery voltage is used the pins VBATL, VBATH and VBATR should be connected together externally. In this case the full voltage range of – 15 V to – 145 V can be used.

7.3.3 Thermal Resistances PEB 4266 (SLIC-P)

Parameter	Symbol	Limit Values	Unit	Test Condition
Junction to case	$R_{\mathrm{th,\ jC}}$	2	K/W	–
Junction to ambient	$R_{\mathrm{th,\ jA}}$	50	K/W	without heatsink

7.3.4 Electrical Parameters PEB 4266 (SLIC-P)

Minimum and maximum values are valid within the full operating range.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extented temperature range operation at – 40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Testing is performed according to the test figures with external circuitry as indicated in the tables. Unless otherwise stated, load impedance R_L = 600 Ω, V_{BATH} = – 48 V, V_{BATL} = – 24 V, V_{BATR} = – 80 V and V_{DD} = + 5 V, R_{IT} = 1 kΩ, R_{IL} = 2 kΩ, C_{EXT} = 470 nF. Typical values are tested at T_A = 25 °C.

Supply Currents and Power Dissipation
($I_R = I_T$ = 0 A; $V_{CMS} = V_{ACP} = V_{ACN} = V_{DCP} = V_{DCN}$ = 1.5 V)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	
Power Down High Impedance, Power Down Resistive Ring, Power Down Resistive High							
1. 2. 3.	V_{DD} current	I_{DD}	PDH PDRR PDRH	–	130 140 140	180 190 190	µA µA µA
4. 5. 6.	V_{BATH} current	I_{BATH}	PDH PDRR PDRH	–	0 0 60	10 10 120	µA µA µA
7. 8. 9.	V_{BATL} current	I_{BATL}	PDH PDRR PDRH	–	0 0 0	10 10 10	µA µA µA
10. 11. 12.	V_{BATR} current	I_{BATR}	PDH PDRR PDRH	–	75 90 35	110 150 90	µA µA µA
13. 14. 15.	Quiescent power dissipation	P_Q	PDH PDRR PDRH	–	6.7 7.9 6.4	10.4 13.7 14.1	mW mW mW

Supply Currents and Power Dissipation

($I_R = I_T = 0$ A; $V_{CMS} = V_{ACP} = V_{ACN} = V_{DCP} = V_{DCN} = 1.5$ V) (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	
	Active Low						
16.	V_{DD} current	I_{DD}	ACTL	–	900	1100	µA
17.	V_{BATH} current	I_{BATH}	ACTL	–	10	15	µA
18.	V_{BATL} current	I_{BATL}	ACTL	–	2100	2700	µA
19.	V_{BATR} current	I_{BATR}	ACTL	–	10	25	µA
20.	Quiescent power dissipation	P_Q	ACTL	–	56.1	73.0	mW
	Active High						
21.	V_{DD} current	I_{DD}	ACTH	–	900	1100	µA
22.	V_{BATH} current	I_{BATH}	ACTH	–	2700	3400	µA
23.	V_{BATL} current	I_{BATL}	ACTH	–	0	10	µA
24.	V_{BATR} current	I_{BATR}	ACTH	–	10	25	µA
25.	Quiescent power dissipation	P_Q	ACTH	–	134.9	170.9	mW
	Active Ring1)						
26.	V_{DD} current	I_{DD}	ACTR	–	900	1200	µA
27.	V_{BATH} current	I_{BATH}	ACTR	–	0	10	µA
28.	V_{BATL} current	I_{BATL}	ACTR	–	0	10	µA
29.	V_{BATR} current	I_{BATR}	ACTR	–	3500	4400	µA
30.	Quiescent power dissipation	P_Q	ACTR	–	284.5	358.7	mW
	Ring on Ring, Ring on Tip						
31.	V_{DD} current	I_{DD}	ROR, ROT	–	800	1100	µA
32.	V_{BATH} current	I_{BATH}	ROR, ROT	–	0	10	µA
33.	V_{BATL} current	I_{BATL}	ROR, ROT	–	0	10	µA
34.	V_{BATR} current	I_{BATR}	ROR, ROT	–	2400	2800	µA
35.	Quiescent power dissipation	P_Q	ROR, ROT	–	196	230.2	mW

Supply Currents and Power Dissipation

($I_R = I_T = 0$ A; $V_{CMS} = V_{ACP} = V_{ACN} = V_{DCP} = V_{DCN} = 1.5$ V) (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	

High Impedance on RING, High Impedance on TIP

No.	Parameter	Symbol	Mode	min.	typ.	max.	Unit
36.	V_{DD} current	I_{DD}	HIR, HIT	–	700	900	µA
37.	V_{BATH} current	I_{BATH}	HIR, HIT	–	0	10	µA
38.	V_{BATL} current	I_{BATL}	HIR, HIT	–	0	10	µA
39.	V_{BATR} current	I_{BATR}	HIR, HIT	–	3000	3900	µA
40.	Quiescent power dissipation	P_Q	HIR, HIT	–	243.5	317.2	mW

High Impedance on RING and TIP

No.	Parameter	Symbol	Mode	min.	typ.	max.	Unit
41.	V_{DD} current	I_{DD}	HIRT	–	500	800	µA
42.	V_{BATH} current	I_{BATH}	HIRT	–	0	10	µA
43.	V_{BATL} current	I_{BATL}	HIRT	–	0	10	µA
44.	V_{BATR} current	I_{BATR}	HIRT	–	2400	2900	µA
45.	Quiescent power dissipation	P_Q	HIRT	–	194.5	236.7	mW

[1] ROR and ROT for $I_R = I_T = 0$ and $V_{TR} = V_{BATR}/2$

7.3.5 Power Calculation PEB 4266 (SLIC-P)

The total power dissipation includes the quiescent power dissipation P_Q given above, the current sensor power dissipation P_I (see **Table 77**), the gain stage power dissipation correction P_G[1] (see **Table 78**), and the output stage power dissipation P_O (see **Table 79**):

$$P_{tot} = P_Q + P_I + P_G + P_O$$

with $P_Q = V_{DD} \times I_{DD} + |V_{BATR}| \times I_{BATR} + |V_{BATH}| \times I_{BATH} + V_{BATL} \times I_{BATL}$

For the calculation of P_I, P_G and P_O see the following tables:

Table 77 P_I Calculation PEB 4266 (SLIC-P)

Operating Mode	Equation for P_I Calculation
PDH	$P_I = 0$ (no DC loop current)
PDRH, PDRHL	$P_I = I_{Trans} \times I_{Trans} \times (10000 + 500 + 24)$ $+ I_{Trans} \times (0.6 + 0.425 \times \|V_{BATH}\|)$
PDRR, PDRRL	$P_I = I_{Trans} \times I_{Trans} \times (10000 + 500 + 16)$ $+ I_{Trans} \times (0.6 + 0.425 \times \|V_{BATR}\|)$
ACTL	$P_I = 0.055 \times I_{Trans} \times \|V_{BATL}\| + 0.04 \times I_{Trans} \times V_{DD}$
ACTH	$P_I = 0.055 \times I_{Trans} \times \|V_{BATH}\| + 0.04 \times I_{Trans} \times V_{DD}$
ACTR	$P_I = 0.055 \times I_{Trans} \times \|V_{BATR}\| + 0.04 \times I_{Trans} \times V_{DD}$
ROR, ROT	$P_I = 0.055 \times I_{Trans} \times \|V_{BATR}\| + 0.04 \times I_{Trans} \times V_{DD}$
HIR, HIT	$P_I = 0.055 \times I_{TorR} \times \|V_{BATR}\| + 0.04 \times I_{TorR} \times V_{DD}$
HIRT	$P_I = 0$ (no DC loop current)

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[1] The gain stage power dissipation correction P_G is a correcting term necessary to ensure a correct power calculation if other as the defined supply voltages are used.

Table 78 P_G **Calculation PEB 4266 (SLIC-P)**

Operating Mode	Equation for P_G Calculation
PDH, PDRH, PDRR	$P_G = 0$ (gain stage not working)
ACTL	$P_G = (V_{BATL}{}^2 - 24^2) \times (1/60k + 1/216k)$
ACTH, PDRHL	$P_G = (V_{BATH}{}^2 - 48^2) \times (1/60k + 1/216k)$
ACTR, PDRRL, HIR, HIT, HIRT	$P_G = (V_{BATR}{}^2 - 80^2) \times (1/60k + 1/216k)$
ROR, ROT	$P_G = (V_{TIP/RING}{}^2 - (V_{BATR}/2)^2)/60k$ $+ (V_{BATR}{}^2 - 80^2 \times (1/60k + 1/216k)$

Table 79 P_O **Calculation PEB 4266 (SLIC-P)**

Operating Mode	Equation for P_O Calculation
PDH, PDRH, PDRHL, PDRR, PDRRL	$P_O = 0$ (output stage not working)
ACTL	$P_O = (\lvert V_{BATL}\rvert - V_{TIP/RING}) \times I_{Trans}$
ACTH	$P_O = (\lvert V_{BATH}\rvert - V_{TIP/RING}) \times I_{Trans}$
ACTR	$P_O = (\lvert V_{BATR}\rvert - V_{TIP/RING}) \times I_{Trans}$
ROR, ROT	$P_O = (\lvert V_{BATR}\rvert - V_{TIP/RING}) \times I_{Trans}$
HIR, HIT	$P_O = V_{Supply\text{-}TorR} \times I_{TorR}$
HIRT	$P_O = 0$ (output stage not working)

7.3.6 Power Up Sequence PEB 4266 (SLIC-P)

The supply voltages of the SLIC-P have to be applied in the following order to the respective pin:

1) Ground to pins AGND and BGND
2) V_{DD} to pin VDD
3) V_{BATR} to pin VBATR
4) V_{BATH} to pin VBATH and V_{BATL} to pin VBATL

If the V_{DD} voltage is applied more than one second later as V_{BATR}, V_{BATH} or V_{BATL} thermal damage of the SLIC-P can accur.

If the above sequence of the battery voltages can not be guaranteed, a diode (1N4007) has to be inserted in the VBATR line.

7.4 Electrical Characteristics PEB 3265/PEB 3264/PEB 3264-2 (SLICOFI-2/-2S/-2S2)

7.4.1 Absolute Maximum Ratings

Parameter[1]	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply pins (VDDi) referred to the corresponding ground pin (GNDi)	–	– 0.3	4.6	V	–
Ground pins (GNDi) referred to any other ground pin (GNDj)	–	– 0.3	0.3	V	–
Supply pins (VDDi) referred to any other supply pin (VDDj)	–	– 0.3	0.3	V	–
Analog input and output pins	–	– 0.3	3.6	V	V_{DDA} = 3.3 V, $V_{GNDA/B}$ = 0 V
Digital input and output pins	–	– 0.3	5.5	V	V_{DDD} = 3.3 V, V_{GNDD} = 0 V
DC input and output current at any input or output pin (free from latch-up)	–	–	100	mA	–
Storage temperature	T_{STG}	– 65	125	°C	–
Ambient temperature under bias	T_A	– 40	85	°C	–
Power dissipation	P_D	–	1	W	–
ESD voltage	–	–	2	kV	Human body model[2]
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model)[3]

[1] i, j = A, B, D, R, PLL

[2] MIL STD 883D, method 3015.7 and ESD Assn. standard S5.1-1993.

[3] EOS/ESD Assn. Standard DS5.3-1993.

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional operation under these conditions is not guaranteed. Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.

7.4.2 Operating Range

$V_{\mathrm{GNDD}} = V_{\mathrm{GNDPLL}} = V_{\mathrm{GNDR}} = V_{\mathrm{GNDA/B}} = 0$ V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply pins (VDDi) referred to the corresponding ground pin (GNDi) (i = A, B, D, R, PLL)		3.135	3.3	3.465	V	
Analog input pins referred to the ground pin (GNDj) (j = A, B) ITj, ILj, ITACj, VCMITj		0	–	3.3	V	$V_{\mathrm{DDj}} = 3.3$ V $V_{\mathrm{GNDj}} = 0$ V
Analog output pins referred to the ground pin (GNDj) (j = A, B)						$V_{\mathrm{DDj}} = 3.3$ V $V_{\mathrm{GNDj}} = 0$ V
ACPj, DCPj, ACNj, DCNj,		0.3	–	2.7	V	
VCMS, VCM		1.3	–	1.7	V	
C1, C2		0	–	3.3	V	
Analog pins for passive devices to ground pin (GNDj) (j = A, B)						$V_{\mathrm{DDj}} = 3.3$ V $V_{\mathrm{GNDj}} = 0$ V
CDCPj, CDCNj		0	–	3.3	V	
CREF		1.3	–	1.7	V	
Digital input and output pins		0	–	5	V	
Ambient temperature	T_{A}	– 40	–	+ 85	°C	

7.4.3 Power Dissipation PEB 3265 (SLICOFI-2)

T_A = – 40 °C to 85 °C, unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{DDB} = V_{DDR} = V_{DDPLL} = 3.3\ V \pm 5\ \%$;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL} = 0\ V$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current [1]						
Sleep both channels	$I_{DDSleep}$	–	5	7	mA	(MCLK, PCLK = 2 MHz)
Power Down both channels	$I_{DDPDown}$	–	24	30	mA	–
Active one channel	I_{DDAct1}	– – –	39 43 47	46 50 55	mA mA mA	without EDSP[2] with 8 MIPS (DTMF detection) with 16 MIPS
Active both channels	I_{DDAct2}	– –	55 70	70 90	mA mA	without EDSP with 32 MIPS
Power dissipation[1]						
Sleep both channels	$P_{DDSleep}$	–	17	25	mW	(MCLK, PCLK = 2 MHz)
Power Down both channels	$P_{DDPDown}$	–	79	104	mW	–
Active one channel	P_{DDAct1}	– – –	129 142 155	160 174 191	mW mW mW	without EDSP with 8 MIPS (DTMF detection) with 16 MIPS
Active both channels	P_{DDAct2}	– –	182 231	243 315	mW mW	without EDSP with 32 MIPS

---

[1] Power dissipation and supply currents are target values

[2] EDSP features are DTMF detection, Caller ID generation, Line Echo Cancellation (LEC) and Universal Tone Detection (UTD).

7.4.4 Power Dissipation PEB 3264, PEB 3264-2 (SLICOFI-2S/-2S2)

T_A = – 40 °C to 85 °C, unless otherwise stated.

$V_{\text{DDD}} = V_{\text{DDA}} = V_{\text{DDB}} = V_{\text{DDR}} = V_{\text{DDPLL}} = 3.3\ \text{V} \pm 5\ \%$;

$V_{\text{GNDA}} = V_{\text{GNDB}} = V_{\text{GNDR}} = V_{\text{GNDD}} = V_{\text{GNDPLL}} = 0\ \text{V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current [1]						
Power Down both channels	I_{DDPDown}	–	24	30	mA	–
Active one channel	I_{DDAct1}	–	39	46	mA	
Active both channels	I_{DDAct2}	–	55	70	mA	
Power dissipation[1]						
Power Down both channels	P_{DDPDown}	–	79	104	mW	–
Active one channel	P_{DDAct1}	–	129	160	mW	
Active both channels	P_{DDAct2}	–	182	243	mW	

[1] Power dissipation and supply currents are target values

7.4.5 Power Up Sequence for Supply Voltages

The power up of VDDA, VDDB, VDDR, VDDD and VDDPLL should be performed simultaneously. No voltage should be supplied to any input or output pin before the VDD voltages are applied.

7.4.6 Digital Interface

T_A = – 40 to + 85 °C, unless otherwise stated.

$V_{DD} = V_{DDD} = V_{DDA/B}$ = 3.3 V ± 5%; $V_{GNDD} = V_{GNDA/B}$ = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
For all input pins (including IO pins):						
Low-input pos.-going	V_{T+}	–	1.70	1.82	V	see **Figure 78**
High-input neg.-going	V_{T-}	1.13	1.20	–	V	see **Figure 78**
Input hysteresis	V_H	0.48	0.5	0.56	V	$V_H = V_{T+} - V_{T-}$
Spike rejection for reset	t_{rej}	1	–	4	µs	–
For all output pins except DU, DXA, DXB, IO1, IO2 (including IO pins):						
Low-output voltage	V_{OL}	–	0.35	0.4	V	I_O = – 3.6 mA
High-output voltage	V_{OH}	2.7	3.0	–	V	I_O = 3.3 mA
for pins DU, DXA, DXB						
Low-output voltage	V_{OLDU}	–	0.35	0.4	V	I_O = – 6 mA
High-output voltage	V_{OHDU}	2.7	3.0	–	V	I_O = 5.3 mA
for pins IO1, IO2						
Low-output voltage	V_{OLDU}	–	0.35	0.4	V	I_O = – 50 mA (PEB 3265)
	V_{OLDU}	–	0.35	0.4	V	I_O = – 30 mA (PEB 3264/-2)
High-output voltage	V_{OHDU}	2.7	3.0	–	V	I_O = 3.3 mA

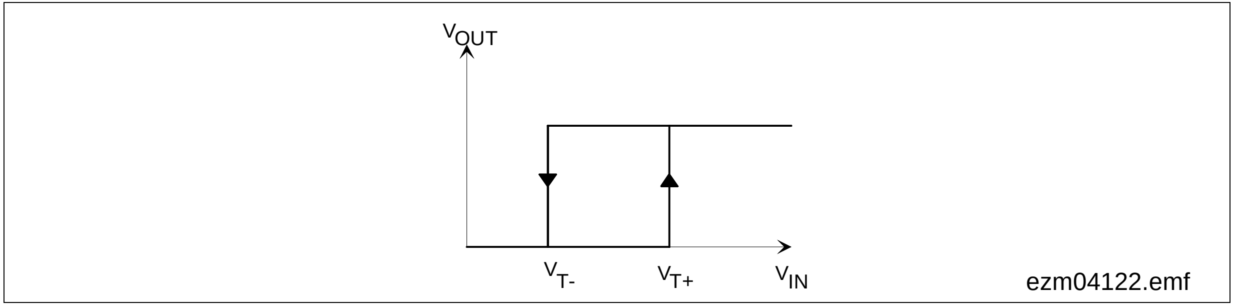

Figure 78 Hysteresis for Input Pins

7.5 AC Transmission DuSLIC

The target figures in this specification are based on the subscriber linecard requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires the consideration of the complete analog environment of the *SLICOFI-2x* device.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extented temperature range operation at – 40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Test Conditions

T_A = – 40 °C to 85 °C, unless otherwise stated.

$V_{\mathrm{DDD}} = V_{\mathrm{DDA}} = V_{\mathrm{DDB}} = V_{\mathrm{DDR}} = V_{\mathrm{DDPLL}} = 3.3\ \mathrm{V} \pm 5\%$;

$V_{\mathrm{GNDA}} = V_{\mathrm{GNDB}} = V_{\mathrm{GNDR}} = V_{\mathrm{GNDD}} = V_{\mathrm{GNDPLL}} = 0\ \mathrm{V}$

$R_\mathrm{L} > 600\ \Omega$; $C_\mathrm{L} < 10$ pF

$\mathrm{L_R} = 0 \ldots -10$ dBr

$\mathrm{L_X} = 0 \ldots +3$ dBr

f = 1014 Hz; 0 dBm0; A-Law or µ-Law;

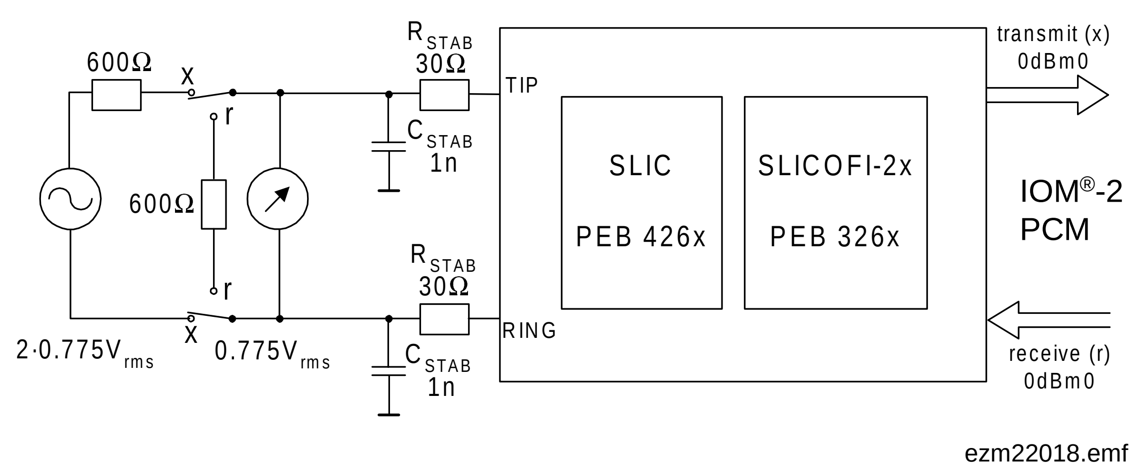
600Ω
x
r
R STAB 30Ω
C STAB 1n
600Ω
r
x
R STAB 30Ω
C STAB 1n
2·0.775V rms
0.775V rms
TIP
RING
SLIC
PEB 426x
SLICOFI-2x
PEB 326x
transmit (x)
0dBm0
IOM®-2
PCM
receive (r)
0dBm0
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Figure 79 Signal Definitions Transmit, Receive

Note: To ensure the stability of the SLIC output buffer, R_{STAB} and C_{STAB} have to be set to the values $R_{STAB} = 30\ \Omega$ and $C_{STAB} \geq 300$ pF (1 nF in the test circuit ***Figure 79****).*

For electromagnetic compatibility C_{STAB} must be set to the much higher value of C_{STAB} = 15 nF (see ***Figure 98****).*

The 0 dBm0 definitions for Receive and Transmit are:

A 0 dBm0 AC signal in Transmit direction is equivalent to 0.775 Vrms (referred to an impedance of 600 Ω).

A 0 dBm0 AC signal in Receive direction is equivalent to 0.775 Vrms (referred to an impedance of 600 Ω).

L_R = – 10 dBr means:

A signal of 0 dBm0 at the digital input correspond to -10 dBm at the analog interface.

L_X = + 3 dBr means:

A signal of 3 dBm at the analog interface correspond to 0 dBm0 at the digital output.

Table 80 AC Transmission

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Longitudinal current capability AC	I_{ll}	per active line	30	–	–	mArms
Overload level	V_{RT}	300 - 4000 Hz	2.3	–	–	Vrms

Transmission Performance (2-wire)

Return loss	RL	200 - 3600 Hz	26	–	–	dB

Insertion Loss (2-wire to 4-wire and 4-wire to 2-wire)

Gain accuracy – Transmit	G_X	0 dBm0, 1014 Hz	– 0.25	–	+ 0.25	dB
Gain accuracy – Receive	G_R	0 dBm0, 1014 Hz	– 0.25	–	+ 0.25	dB
Gain variation with temperature – 40 … + 85 °C	–	–	–	–	± 0.1	dB

Table 80 AC Transmission (cont'd)

Parameter	**Symbol**	**Conditions**	**Limit Values**			**Unit**
			min.	**typ.**	**max.**	
Frequency Response (see Figure 81 and Figure 82)						
Receive loss Frequency variation	G_{RAF}	Reference frequency 1014 Hz, signal level 0 dBm0, H_{FRR} = 1				
		f = 0 - 300 Hz	– 0.25	–	–	dB
		f = 300 - 400 Hz	– 0.25	–	0.9	dB
		f = 400 - 600 Hz	– 0.25	–	0.65	dB
		f = 600 - 2400 Hz	– 0.25	–	0.25	dB
		f = 2400 - 3000 Hz	– 0.25	–	0.45	dB
		f = 3000 - 3400 Hz	– 0.25	–	1.4	dB
		f = 3400 - 3600 Hz	– 0.25	–	–	dB
Transmit loss Frequency variation	G_{XAF}	Reference frequency 1014 Hz, signal level 0 dBm0, H_{FRX}= 1				
		f = 0 - 200 Hz	0	–	–	dB
		f = 200 - 300 Hz	– 0.25	–	–	dB
		f = 300 - 400 Hz	– 0.25	–	0.9	dB
		f = 400 - 600 Hz	– 0.25	–	0.65	dB
		f = 600 - 2400 Hz	– 0.25	–	0.25	dB
		f = 2400 - 3000 Hz	– 0.25	–	0.45	dB
		f = 3000 - 3400 Hz	– 0.25	–	1.4	dB
		f = 3400 - 3600 Hz	– 0.25	–	–	dB

Table 80 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Gain Tracking (see Figure 83 and Figure 84)						
Transmit gain Signal level variation	G_{XAL}	Sinusoidal test method f = 1014 Hz, reference level – 10 dBm0				
		VF_XI = – 55 to – 50 dBm0	– 1.4	–	1.4	dB
		VF_XI = – 50 to – 40 dBm0	– 0.5	–	0.5	dB
		VF_XI = – 40 to + 3 dBm0	– 0.25	–	0.25	dB
Receive gain Signal level variation	G_{RAL}	Sinusoidal test method f = 1014 Hz, reference level – 10 dBm0				
		D_R0 = – 55 to – 50 dBm0	– 1.4	–	1.4	dB
		D_R0 = – 50 to – 40 dBm0	– 0.5	–	0.5	dB
		D_R0 = – 40 to + 3 dBm0	– 0.25	–	0.25	dB
Balance return loss		300 - 3400 Hz	26	–	–	dB
Group Delay (see Figure 85)						
Transmit delay, absolute	D_{XA}	f = 500 - 2800 Hz	400	490	585	µs
Receive delay, absolute	D_{RA}	f = 500 - 2800 Hz	290	380	475	µs
Group delay, Receive and Transmit, relative to 1500 Hz	D_{XR}					
		f = 500 - 600 Hz	–	–	300	µs
		f = 600 - 1000 Hz	–	–	150	µs
		f = 1000 - 2600 Hz	–	–	100	µs
		f = 2600 - 2800 Hz	–	–	150	µs
		f = 2800 - 3000 Hz	–	–	300	µs
Overload compression A/D	OC	–	–	–	–	–

Table 80 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Longitudinal Balance (according to ITU-T O.9)						
Longitudinal conversion loss	L-T	300 - 1000 Hz				
		DuSLIC-S/-E/-P	53	58	–	dB
		DuSLIC-S2/-E2	60	65	–	dB
		3400 Hz				
		DuSLIC-S/-E/-P	52	55	–	dB
		DuSLIC-S2/-E2	56	59	–	dB
Input longitudinal interference loss	L-4	300 - 1000 Hz				
		DuSLIC-S/-E/-P	53	58	–	dB
		DuSLIC-S2/-E2	60	65	–	dB
		3400 Hz				
		DuSLIC-S/-E/-P	52	55	–	dB
		DuSLIC-S2/-E2	56	59	–	dB
Transversal to longitudinal	T-L	300 - 4000 Hz	46	–	–	dB
Longitudinal signal generation	4-L	300 - 4000 Hz	46	–	–	dB
TTX Signal Generation						
TTX signal	V_{TTX}	at 200 Ω	–	–	2.5	Vrms
Out-of-Band Noise (Single Frequency Inband – 25 dBm0)						
Transversal	V_{RT}	12 kHz - 200 kHz	–	– 55	– 50	dBm
Longitudinal	V_{RT}	12 kHz - 200 kHz	–	– 55	– 50	dBm
Out-of-Band Idle Channel Noise at Analog Output Measured with 3 kHz Bandwidth						
	V_{RT}	10 kHz	–	–	– 50	dBm
	V_{RT}	300 kHz	–	–	– 50	dBm
	V_{RT}	500 kHz	–	–	– 70	dBm
	V_{RT}	1000 kHz	–	–	– 70	dBm

Table 80 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Out-of-Band Signals at Analog Output (Receive) (see Figure 86)						
Out-of-Band Signals at Analog Input (Transmit) (see Figure 87)						
Total Harmonic Distortion						
2-wire to 4-wire	THD4	– 7 dBm0, 300 - 3400 Hz	–	– 50	– 44	dB
4-wire to 2-wire	THD2	– 7 dBm0, 300 - 3400 Hz	–	– 50	– 44	dB
Idle Channel Noise						
2-wire port (receive) A-law	N_{RP}	Psophometric TTX disabled TTX enabled	 – –	 – –	 – 74 – 70	 dBmp dBmp
µ-law	N_{RC}	C message TTX disabled TTX enabled	 – –	 – –	 16 20	 dBrnC dBrnC
PCM side (transmit) A-Law	N_{TP}	Psophometric TTX disabled TTX enabled	 – –	 – –	 – 69 – 67	 dBm0p dBm0p
µ-Law	N_{TC}	C message TTX disabled TTX enabled	 – –	 – –	 18 20	 dBrnC dBrnC

Table 80 AC Transmission (cont'd)

Parameter	**Symbol**	**Conditions**	**Limit Values**			**Unit**
			min.	**typ.**	**max.**	
Distortion (Sinusoidal Test Method, see Figure 89, Figure 88 and Figure 90)						
Signal to total distortion Transmit	STD_X	Output connection: L_X = 0 dBr *f* = 1014 Hz (C message-weighted for µ-law, psophometrically weighted for A-law)				
		– 45 dBm0	22	–	–	dB
		– 40 dBm0	27	–	–	dB
		– 30 dBm0	34	–	–	dB
		– 20 dBm0	36	–	–	dB
		– 10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB
Signal to total distortion Receive	STD_R	Input connection: L_R = – 7 dBr *f* = 1014 Hz (C message-weighted for µ-law, psophometrically weighted for A-law)				
		– 45 dBm0	17	–	–	dB
		– 40 dBm0	22	–	–	dB
		– 30 dBm0	31	–	–	dB
		– 20 dBm0	35.5	–	–	dB
		– 10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB
Signal to total distortion Receive	STD_R	Input connection: L_R = 0 dBr *f* = 1014 Hz (C message-weighted for µ-law, psophometrically weighted for A-law)				
		– 45 dBm0	22	–	–	dB
		– 40 dBm0	27	–	–	dB
		– 30 dBm0	34	–	–	dB
		– 20 dBm0	36	–	–	dB
		– 10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB

Table 80 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Power Supply Rejection Ratio						
V_{DD}/V_{RT} (SLIC)	PSRR	300 - 3400 Hz ACTL, ACTH	33	–	–	dB
V_{DDi}/V_{RT} (*SLICOFI-2x*) i = A, B, D, R, PLL	PSRR	300 - 3400 Hz ACTL, ACTH	27	–	–	dB
V_{BATH}/V_{RT}, V_{BATL}/V_{RT} (SLIC)	PSRR	300 - 3400 Hz	33	–	–	dB

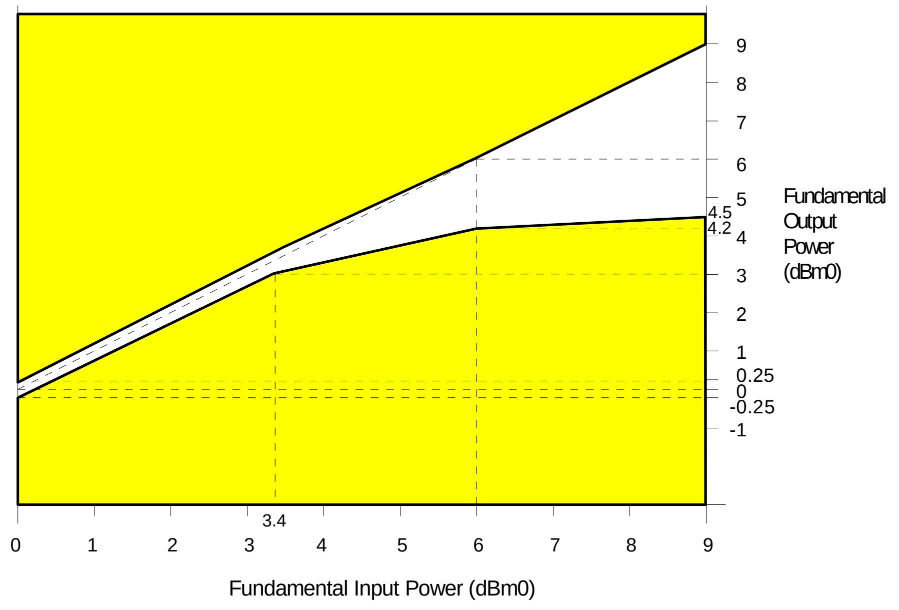

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Figure 80 Overload Compression

7.5.1 Frequency Response

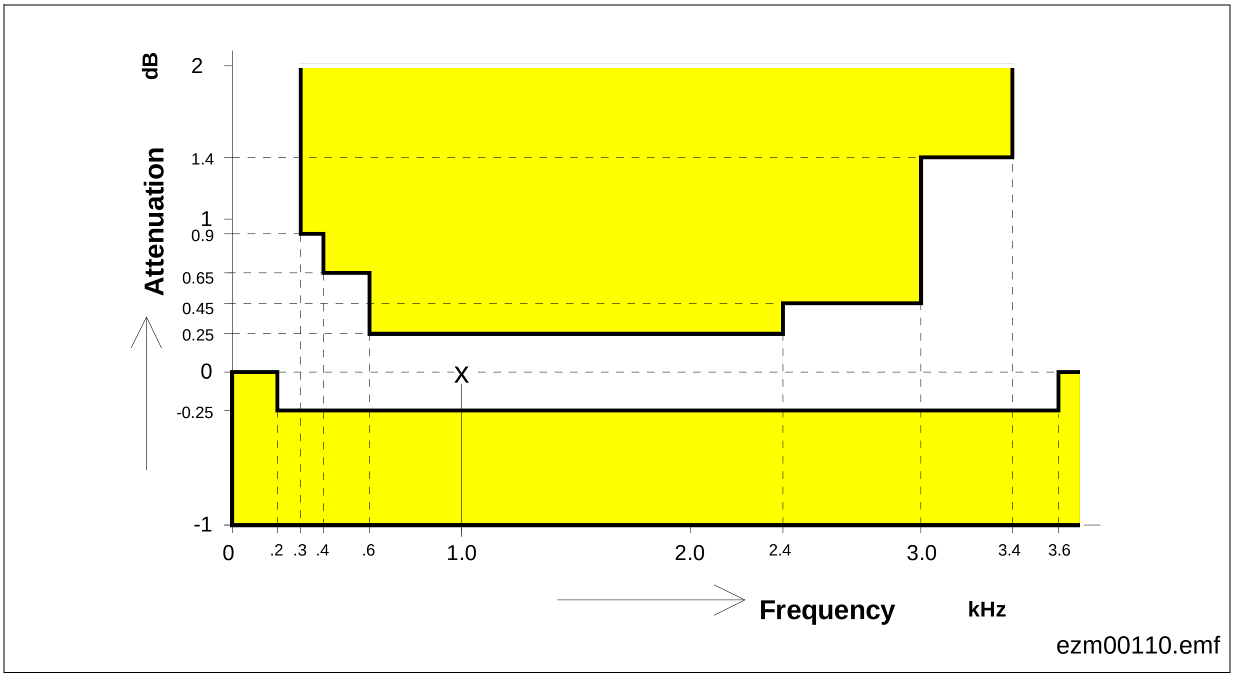


Figure 81 **Frequency Response Transmit**

Reference frequency 1 kHz, signal level 0 dBm0, $H_{FRX} = 1$

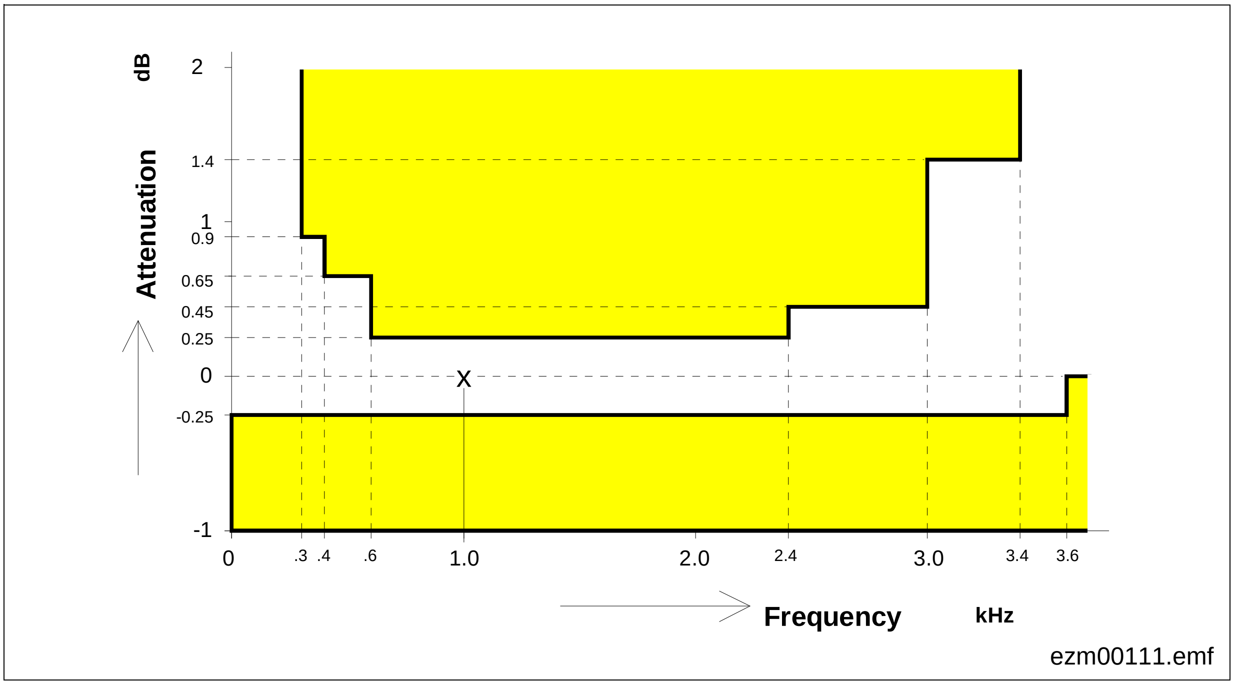


Figure 82 **Frequency Response Receive**

Reference frequency 1 kHz, signal level 0 dBm0, $H_{FRR} = 1$

7.5.2 Gain Tracking (Receive or Transmit)

The gain deviations stay within the limits in the figures below.

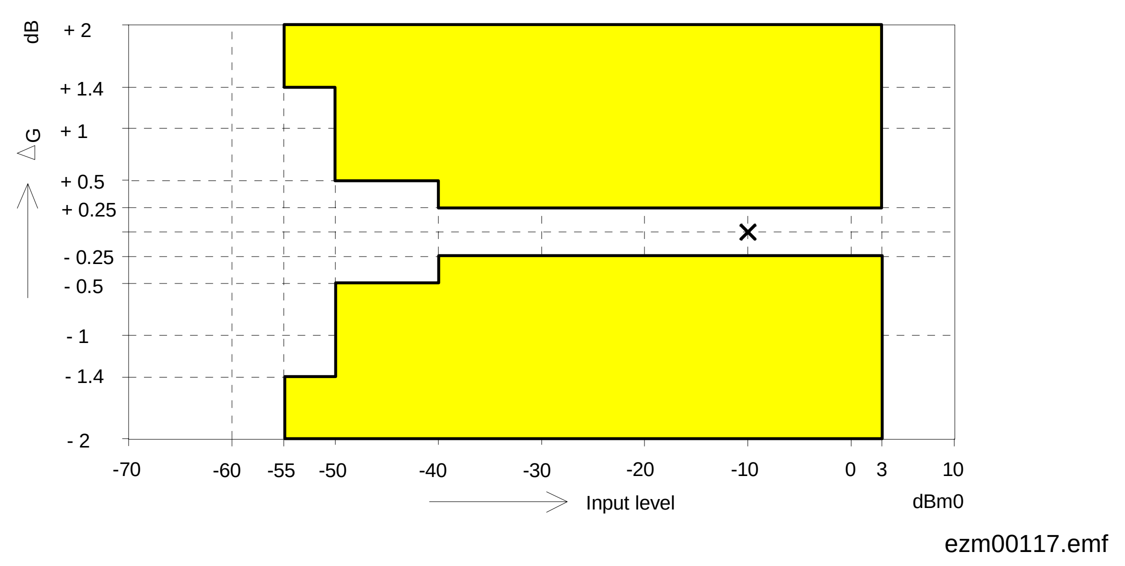


Figure 83 Gain Tracking Receive

Measured with a sine wave of *f* = 1014 Hz, the reference level is – 10 dBm0.

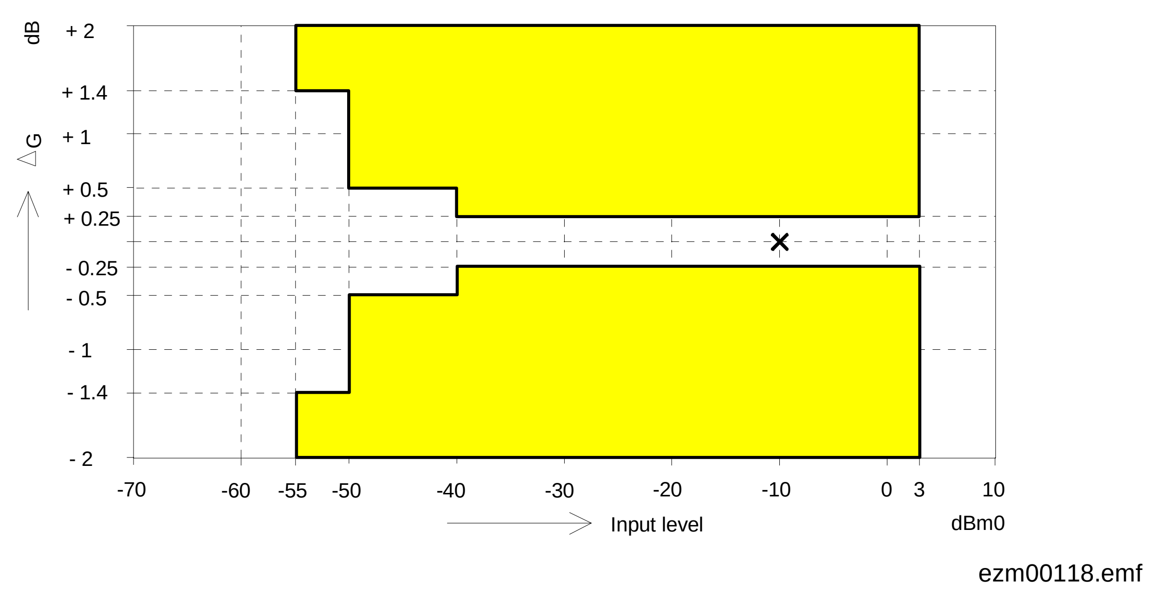


Figure 84 Gain Tracking Transmit

Measured with a sine wave of *f* = 1014 Hz, the reference level is – 10 dBm0.

7.5.3 Group Delay

Minimum delays occure when the *SLICOFI-2x* is operating with disabled Frequency Response Receive and Transmit filters (bit FRR-DIS and bit FRX-DIS in register BCR4 set to 1) including the delay through A/D and D/A converters. Specific filter programming may cause additional group delays. Absolute Group delay also depends on the programmed time slot.

Group delay distortion stays within the limits in the figures below.

Table 81 Group Delay Absolute Values: Signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit	Test Condition	Fig.
		min.	typ.	max.			
Transmit delay	D_{XA}	400	490	585	µs	f = 1.5 kHz	–
Receive delay	D_{RA}	290	380	475	µs	f = 1.5 kHz	–

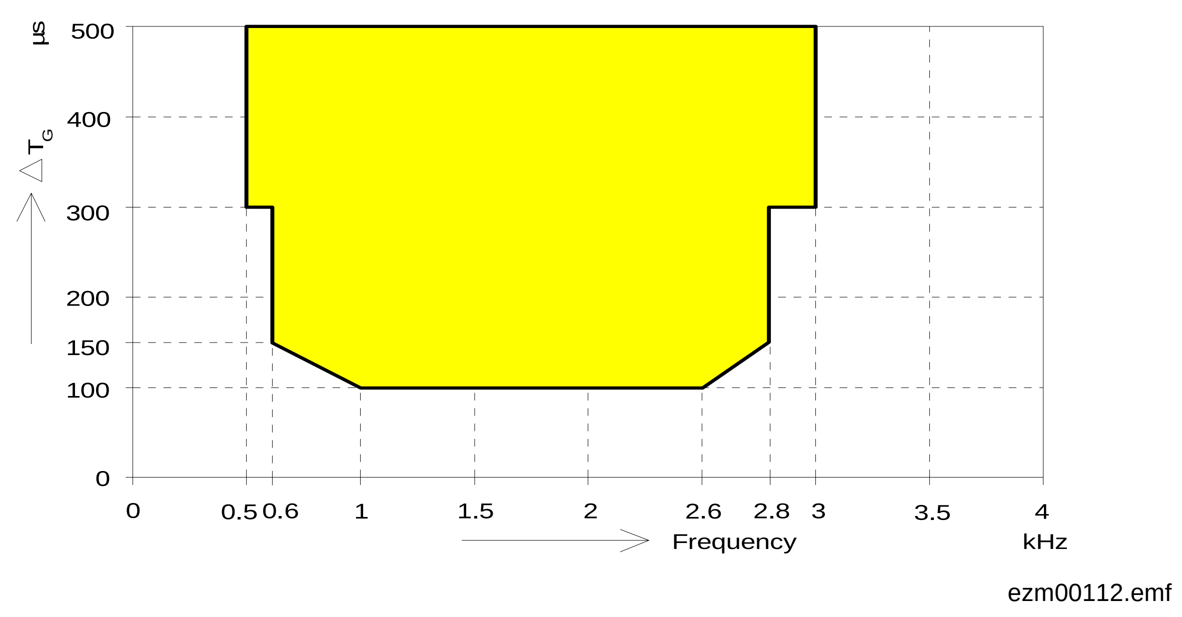
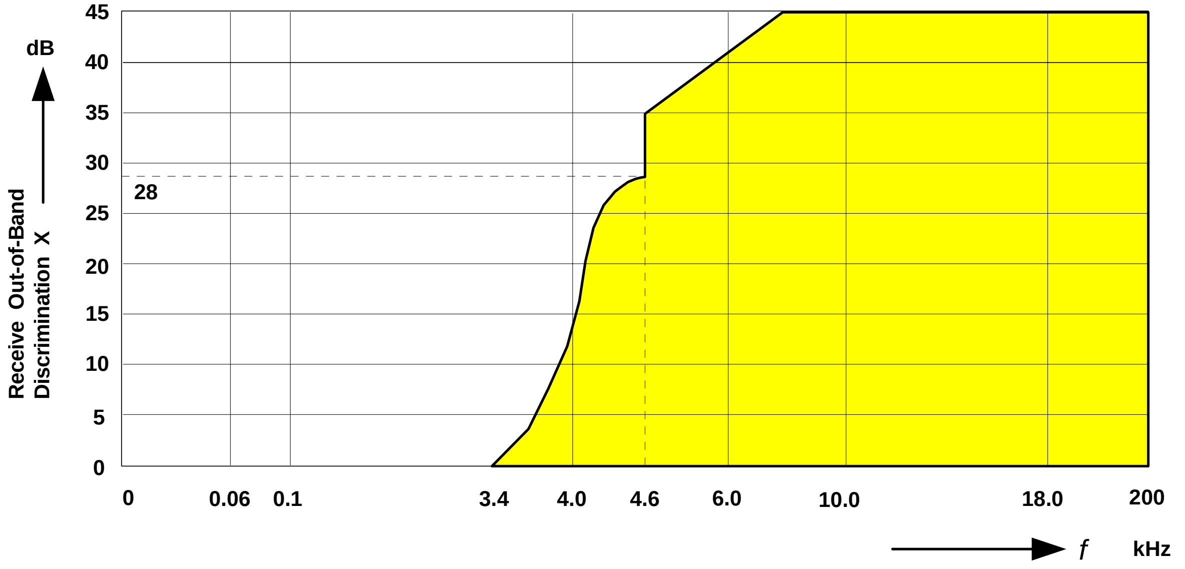


Figure 85 Group Delay Distortion Receive and Transmit

Signal level 0 dBm0

7.5.4 Out-of-Band Signals at Analog Output (Receive)

With a 0 dBm0 sine wave with a frequency of *f* (300 Hz to 3.4 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.



$$3.4 \ldots 4.6\ \text{kHz:}\quad X = -14\left(\sin\left(\pi\frac{4000-f}{1200}\right)-1\right)$$

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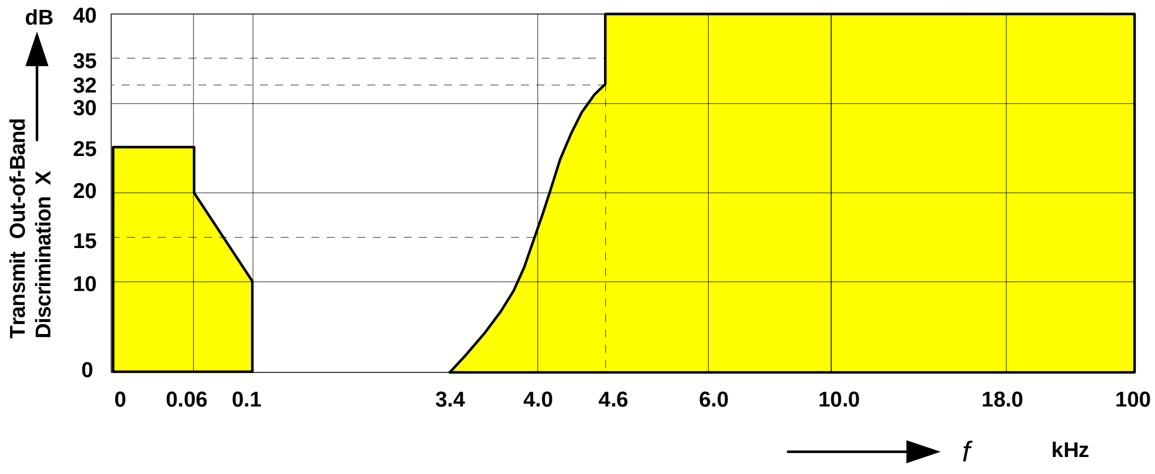
Figure 86 Out-of-Band Signals at Analog Output (Receive)

7.5.5 Out-of-Band Signals at Analog Input (Transmit)

With a 0 dBm0 out-of-band sine wave signal with a frequency of f (< 100 Hz or 3.4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input.[1]



$$3.4 \ldots 4.0\ \text{kHz:} \quad X = -14\left(\sin\left(\pi\frac{4000-f}{1200}\right) - 1\right)$$

$$4.0 \ldots 4.6\ \text{kHz:} \quad X = -18\left(\sin\left(\pi\frac{4000-f}{1200}\right) - \frac{7}{9}\right)$$

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Figure 87 Out-of-Band Signals at Analog Input (Transmit)

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[1] Poles at 12 kHz ± 150 Hz and 16 kHz ± 150 Hz respectively and harmonics will be provided

7.5.6 Total Distortion Measured with Sine Wave

The signal to total distortion ratio exceeds the limits in the following figure:

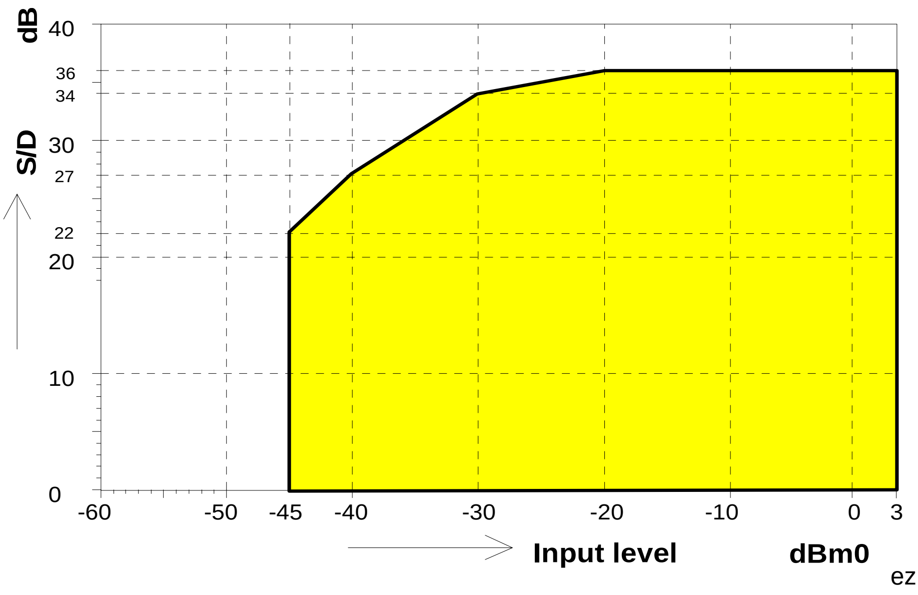


Figure 88 **Total Distortion Transmit (L_X = 0 dBr)**

Measured with a sine wave of *f* = 1014 Hz (C message-weighted for µ-law, psophometrically weighted for A-law).

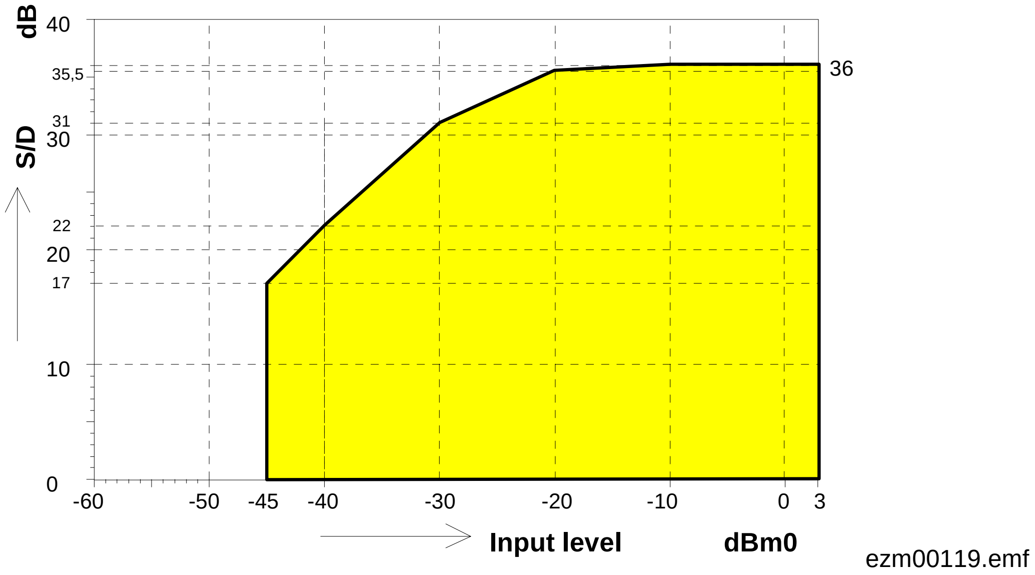


Figure 89 **Total Distortion Receive (L_R = – 7 dBr)**

Measured with a sine wave of *f* = 1014 Hz (C message-weighted for µ-law, psophometrically weighted for A-law).

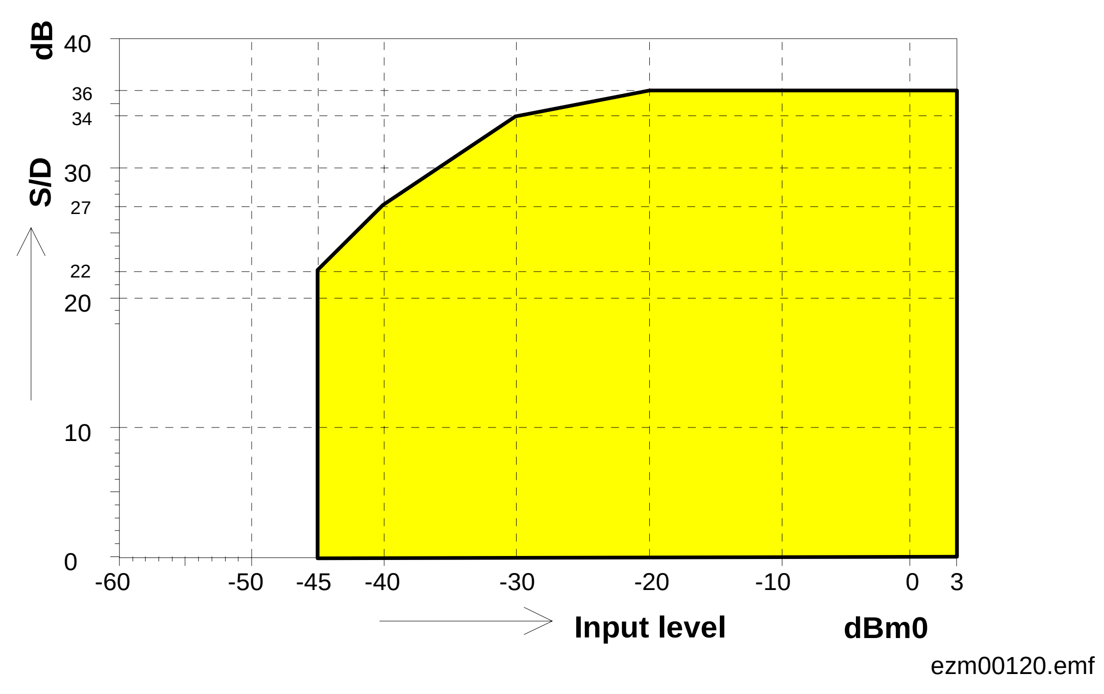


Figure 90 Total Distortion Receive (L_R = 0 dBr)

Measured with a sine wave of *f* = 1014 Hz (C message-weighted for µ-law, psophometrically weighted for A-law).

7.6 DC Characteristics

T_A = – 40 °C to 85 °C, unless otherwise stated.

Table 82 DC Characteristics

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Line Termination Tip, Ring						
Sinusoidal Ringing						
Max. ringing voltage	V_{RNG0}	$V_{HR} - V_{BATH}$ = 150 V, V_{DC} = 20 V for ring trip (DuSLIC-E/-E2)	85	–	–	Vrms
		$- V_{BATR}$ = 150 V, V_{DC} = 20 V for ring trip (DuSLIC-P)	85			Vrms
		$V_{HR} - V_{BATH}$ = 90 V, V_{DC} = 20 V for ring trip (DuSLIC-S/-S2)	45	–	–	Vrms
Output impedance	R_{OUT}	SLIC output buffer and R_{STAB}	–	61	–	Ω
Harmonic distortion	THD	–	–	–	5	%
Output current limit	$\lvert I_{R, max.}\rvert$, $\lvert I_{T, max.}\rvert$	Modes: Active		–		
		SLIC-E/-E2/-S/-S2:	80	105	130	mA
		SLIC-P:	70	90	110	mA
Loop current gain accuracy	–	–	–	–	3	%
Loop current offset error[1]	–	–	– 0.75		0.75	mA
Loop open resistance TIP to V_{BGND}	R_{TG}	Modes: Power Down I_T = 2 mA, T_A = 25 °C	–	5	–	kΩ
Loop open resistance RING to V_{BAT}	R_{BG}	Modes: Power Down I_R = 2 mA, T_A = 25 °C	–	5	–	kΩ
Ring trip function	–	–	–	–	–	–
Ring trip DC voltage	–	SLIC-E/-E2/-S/-S2:	0		30	Vdc
		SLIC-P: balanced	0		30	Vdc
		SLIC-P: unbalanced	–	$V_{BATR}/2$	–	Vdc

Table 82 **DC Characteristics** (cont'd)

Parameter	**Symbol**	**Conditions**	**Limit Values**			**Unit**
			min.	**typ.**	**max.**	
Ring trip detection time delay	–	–	–	–	2	periods
Ring off time delay	–	–	–	–	2	periods

[1] can be reduced with current offset error compensation described in **Chapter 4.8.2.8**

7.7 DuSLIC Timing Characteristics

T_A = – 40 °C to 85 °C, unless otherwise stated.

7.7.1 MCLK/FSC Timing

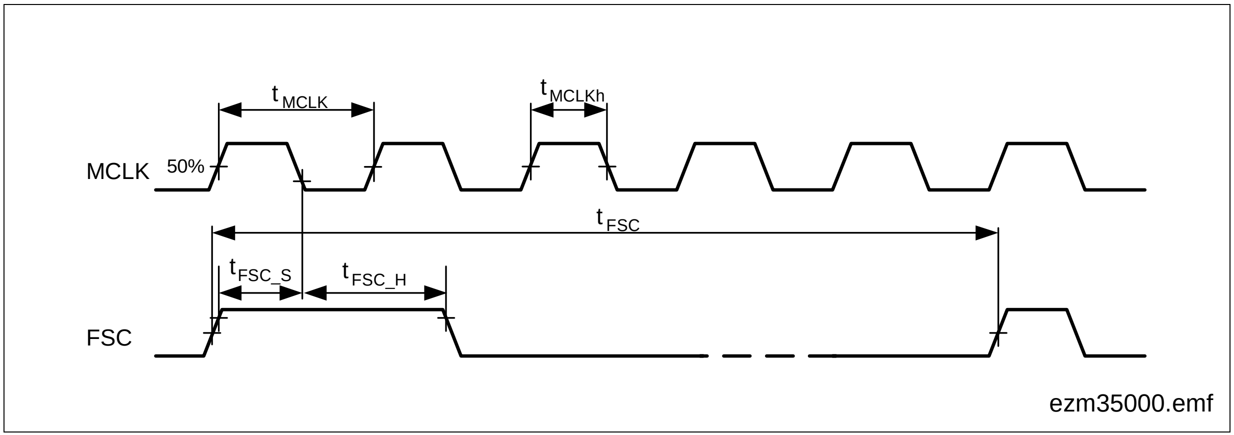


Figure 91 MCLK / FSC-Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period MCLK[1] 512 kHz ± 100 ppM 1536 kHz ± 100 ppM 2048 kHz ± 100 ppM 4096 kHz ± 100 ppM 7168 kHz ± 100 ppM 8192 kHz ± 100 ppM	t_{MCLK}	 1952.93 650.98 488.23 244.116 139.495 122.058	 1953.13 651.04 488.28 244.141 139.509 122.070	 1953.32 651.11 488.33 244.165 139.523 122.082	ns
MCLK high time	t_{MCLKh}	$0.4 \times t_{MCLK}$	$0.5 \times t_{MCLK}$	$0.6 \times t_{MCLK}$	µs
Period FSC[1]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time	t_{FSC_h}	40	50	–	ns
FSC (or PCM) jitter time		$-0.2 \times t_{MCLK}$		$+0.2 \times t_{MCLK}$	ns

[1] The MCLK frequency must be an integer multiple of the FSC frequency.

7.7.2 PCM Interface Timing

7.7.2.1 Single-Clocking Mode

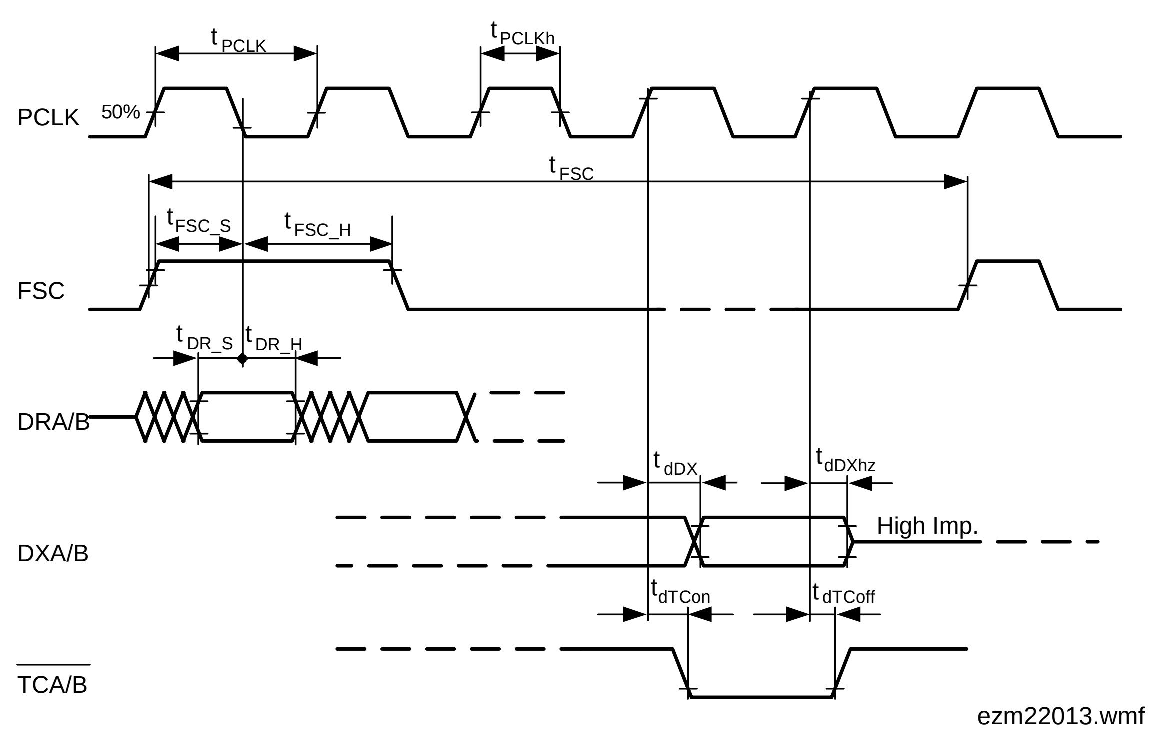

t PCLK
t PCLKh
PCLK
50%
t FSC
t FSC_S
t FSC_H
FSC
t DR_S
t DR_H
DRA/B
t dDX
t dDXhz
DXA/B
High Imp.
t dTCon
t dTCoff
TCA/B
ezm22013.wmf

Figure 92 PCM Interface Timing - Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK1)	t_{PCLK}	1/8192	1/(n*64) with $2 \le n \le 128$	1/128	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	$0.5 \times t_{PCLK}$	$0.6 \times t_{PCLK}$	µs
Period FSC1)	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time	t_{FSC_h}	40	50	–	ns
DRA/B setup time	t_{DR_s}	10	50	–	ns
DRA/B hold time	t_{DR_h}	10	50	–	ns
DXA/B delay time2)	t_{dDX}	25	–	t_{dDX_min} + $0.4 \times C_{Load}$[pF]	ns

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DXA/B delay time to high Z	t_{dDXhz}	25	–	50	ns
TCA/B delay time on	t_{dTCon}	25	–	$t_{\text{dTCon\_min}} + 0.4 \times C_{\text{Load}}[\text{pF}]$	ns
TCA/B delay time off	t_{dTCoff}	25	–	$t_{\text{dTCoff\_min}} + (R_{\text{Pullup}}[\text{k}\Omega] \times C_{\text{Load}}[\text{pF}])$	ns

[1] The PCLK frequency must be an integer multiple of the FSC frequency.

[2] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, $R_{\text{Pullup}} > 1.5\ \text{k}\Omega$)

7.7.2.2 Double-Clocking Mode

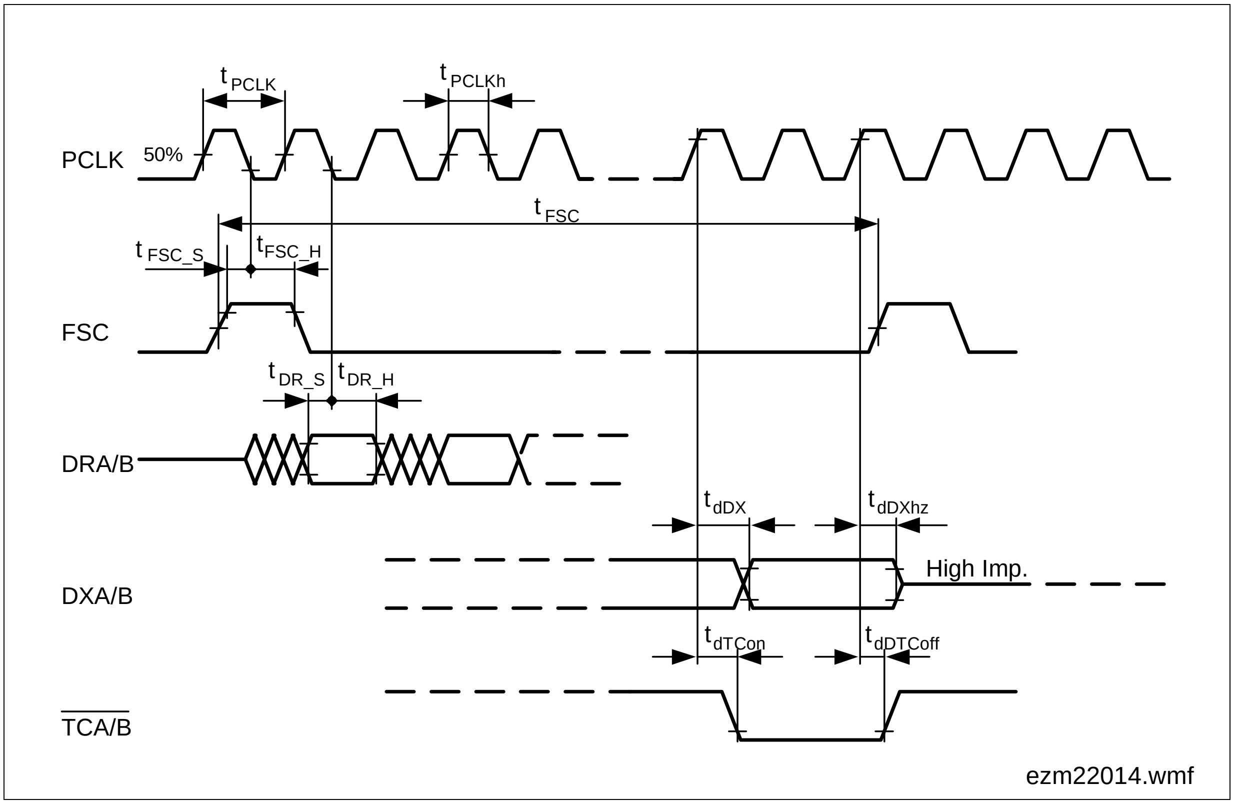

t PCLK
t PCLKh
PCLK
50%
t FSC
t FSC_S
tFSC_H
FSC
t DR_S
t DR_H
DRA/B
t dDX
t dDXhz
DXA/B
High Imp.
t dTCon
t dDTCoff
$\overline{\text{TCA/B}}$
ezm22014.wmf

Figure 93 PCM Interface Timing – Double-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK$^{1)}$	t_{PCLK}	1/8192	1/(n*64) with $2 \leq n \leq 64$	1/256	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	$0.5 \times t_{PCLK}$	$0.6 \times t_{PCLK}$	µs
Period FSC$^{1)}$	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time	t_{FSC_h}	40	50	–	ns
DRA/B setup time	t_{DR_s}	10	50	–	ns
DRA/B hold time	t_{DR_h}	10	50	–	ns
DXA/B delay time$^{2)}$	t_{dDX}	25	–	t_{dDX_min} + $0.4 \times C_{Load}$[pF]	ns
DXA/B delay time to high Z	t_{dDXhz}	25	–	50	ns
TCA/B delay time on	t_{dTCon}	25	–	t_{dTCon_min} + $0.4 \times C_{Load}$[pF]	ns
TCA/B delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + $(R_{Pullup}[\text{k}\Omega] \times C_{Load}[\text{pF}])$	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency.

2) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

7.7.3 Microcontroller Interface Timing

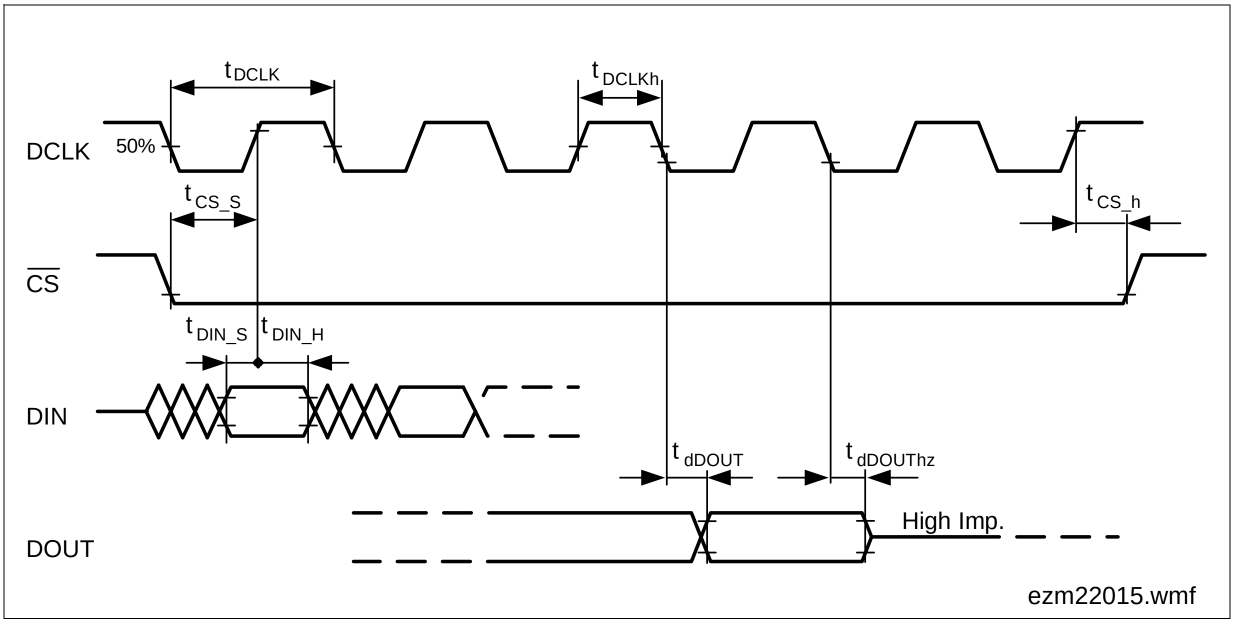

t DCLK
t DCLKh
DCLK
50%
t CS_S
t CS_h
$\overline{CS}$
t DIN_S
t DIN_H
DIN
t dDOUT
t dDOUThz
High Imp.
DOUT
ezm22015.wmf

Figure 94 Microcontroller Interface Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCLK	t_{DCLK}	1/8192	–	–	ms
DCLK high time	t_{DCLKh}	–	$0.5 \times t_{DCLK}$	–	µs
CS setup time	t_{CS_s}	10	50	–	ns
CS hold time	t_{CS_h}	30	50	–	ns
DIN setup time	t_{DIN_s}	10	50	–	ns
DIN hold time	t_{DIN_h}	10	50	–	ns
DOUT delay time1)	t_{dDOUT}	30	–	$t_{dDOUT\_min} + 0.4 \times C_{Load}$[pF]	ns
DOUT delay time to high Z	$t_{dDOUThz}$	30	–	50	ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load})

7.7.4 IOM-2 Interface Timing

7.7.4.1 Single-Clocking Mode

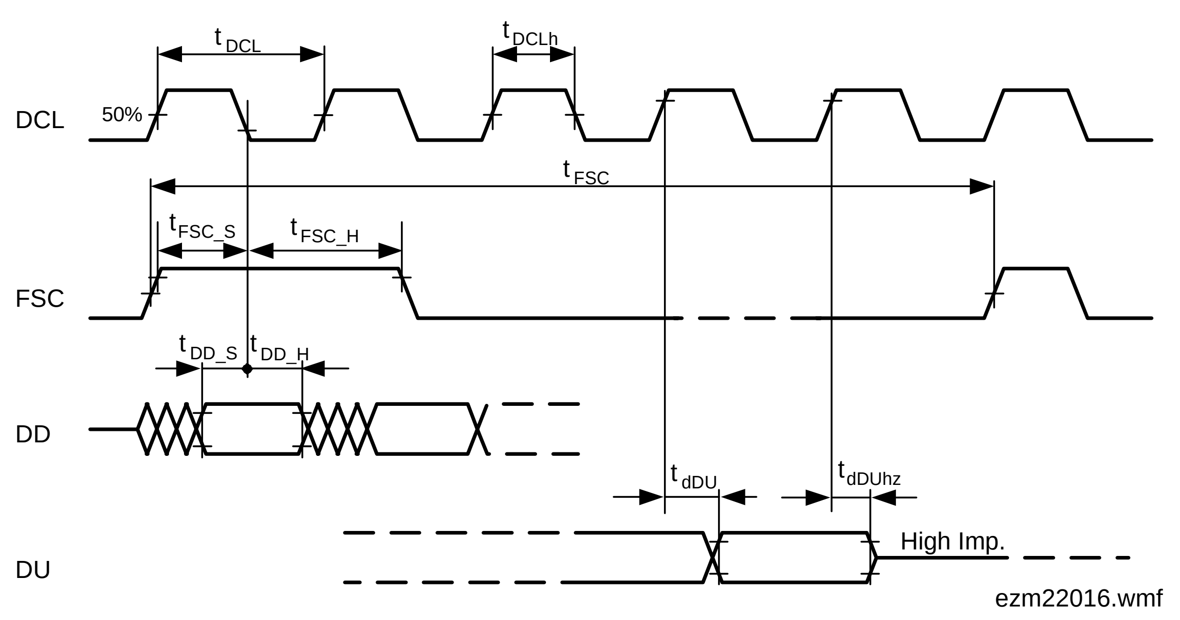


Figure 95 IOM-2 Interface Timing – Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL[1]	t_{DCL}	–	1/2048	–	ms
DCL high time	t_{DCLh}	$0.4 \times t_{\mathrm{DCL}}$	$0.5 \times t_{\mathrm{DCL}}$	$0.6 \times t_{\mathrm{DCL}}$	µs
Period FSC[1]	t_{FSC}	–	125	–	µs
FSC setup time	$t_{\mathrm{FSC\_s}}$	10	50	–	ns
FSC hold time	$t_{\mathrm{FSC\_h}}$	40	50	–	ns
DD setup time	$t_{\mathrm{DD\_s}}$	10	50	–	ns
DD hold time	$t_{\mathrm{DD\_h}}$	10	50	–	ns
DU delay time[2]	t_{dDX}	25	–	$t_{\mathrm{dDX\_min}}$ + $0.4 \times C_{\mathrm{Load}}$[pF]	ns
DU delay time to high Z	t_{dDXhz}	25	–	50	ns

[1] The DCL frequency must be an integer multiple of the FSC frequency.

[2] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

7.7.4.2 Double-Clocking Mode

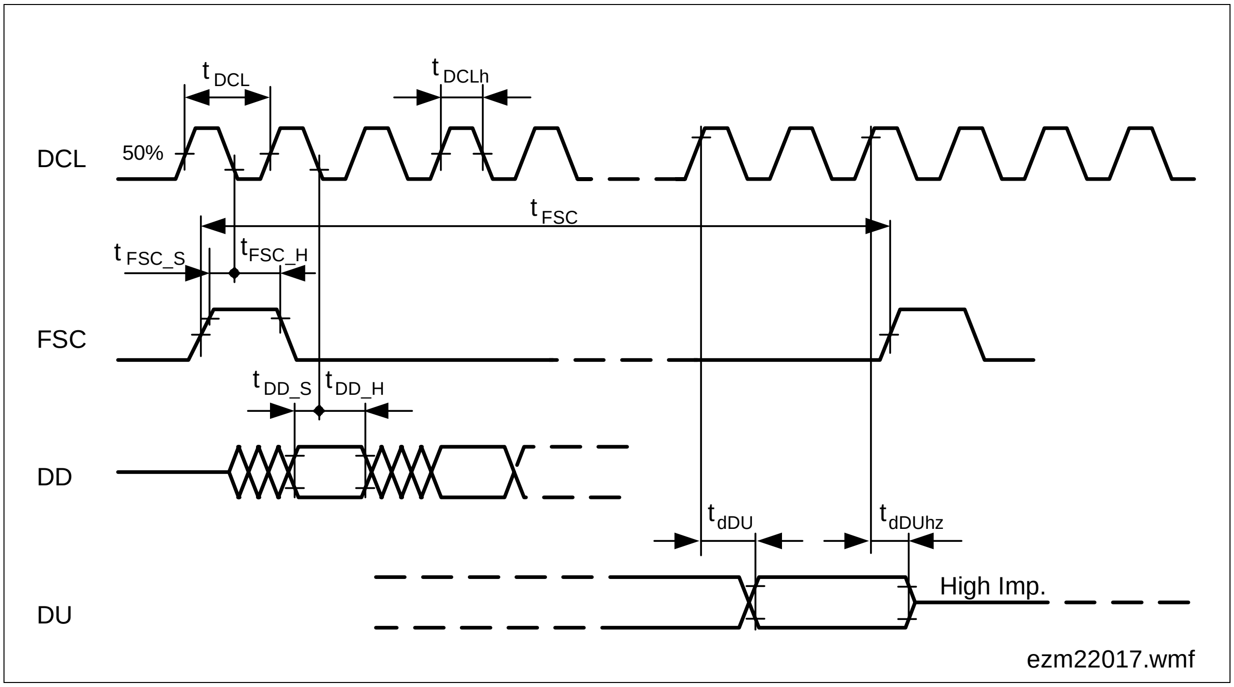

t DCL
t DCLh
DCL
50%
t FSC
t FSC_S
tFSC_H
FSC
t DD_S
t DD_H
DD
tdDU
tdDUhz
DU
High Imp.
ezm22017.wmf

Figure 96 IOM-2 Interface Timing – Double-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL[1]	t_{DCL}	–	1/4096	–	ms
DCL high time	t_{DCLh}	$0.4 \times t_{DCL}$	$0.5 \times t_{DCL}$	$0.6 \times t_{DCL}$	µs
Period FSC[1]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time	t_{FSC_h}	40	50	–	ns
DD setup time	t_{DD_s}	10	50	–	ns
DD hold time	t_{DD_h}	10	50	–	ns
DU delay time[2]	t_{dDX}	25	–	t_{dDX_min} + $0.4 \times C_{Load}$[pF]	ns
DU delay time to high Z	t_{dDXhz}	25	–	50	ns

[1] The DCL frequency must be an integer multiple of the FSC frequency.

[2] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

8 Application Circuits

Application circuits are shown for internal ringing with DuSLIC-E/-E2/-S/-P (balanced and unbalanced) and for external unbalanced ringing with DuSLIC-E/-E2/-S/-S2/-P for one line. Channel A and the SLIC have to be duplicated in the circuit diagrams to show all components for 2 channels.

8.1 Internal Ringing (Balanced/Unbalanced)

Internal balanced ringing is supported up to 85 Vrms for DuSLIC-E/-E2/-P and up to 45 Vrms for DuSLIC-S. Internal unbalanced ringing is supported for SLIC-P with ringing amplitudes up to 50 Vrms without any additional external components. Off-hook detection and ring trip detection are also fully internal in the DuSLIC chip set.

8.1.1 Circuit Diagram Internal Ringing

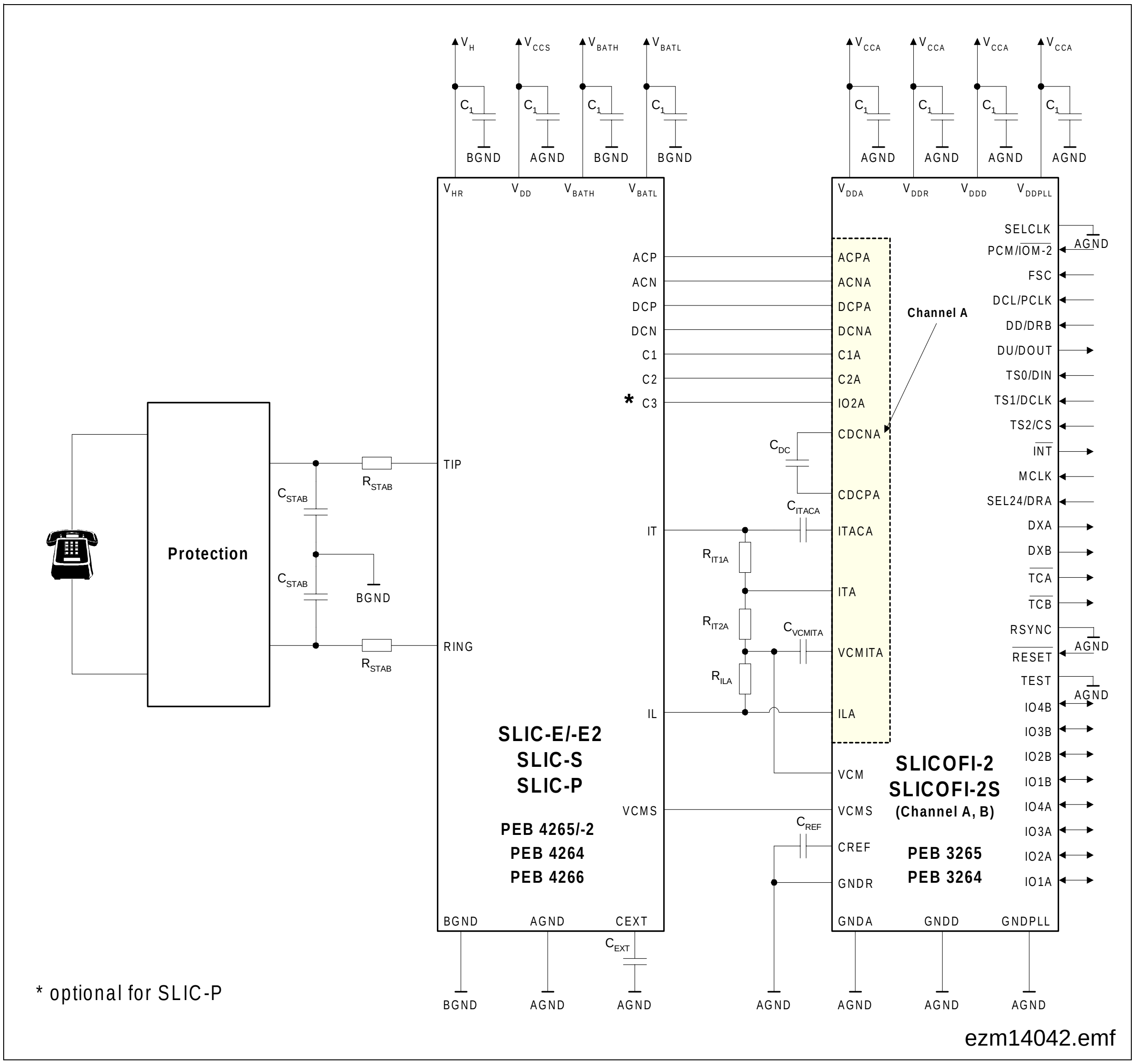

V_H
V_CCS
V_BATH
V_BATL
V_CCA
V_CCA
V_CCA
V_CCA
C_1
BGND
AGND
BGND
BGND
AGND
AGND
AGND
AGND
V_HR
V_DD
V_BATH
V_BATL
V_DDA
V_DDR
V_DDD
V_DDPLL
ACP
ACN
DCP
DCN
C1
C2
* C3
TIP
IT
RING
IL
VCMS
SLIC-E/-E2
SLIC-S
SLIC-P
PEB 4265/-2
PEB 4264
PEB 4266
BGND
AGND
CEXT
C_EXT
Protection
C_STAB
R_STAB
BGND
C_DC
C_ITACA
R_IT1A
R_IT2A
C_VCMITA
R_ILA
C_REF
ACPA
ACNA
DCPA
DCNA
C1A
C2A
IO2A
CDCNA
CDCPA
ITACA
ITA
VCMITA
ILA
VCM
VCMS
CREF
GNDR
Channel A
SLICOFI-2
SLICOFI-2S
(Channel A, B)
PEB 3265
PEB 3264
GNDA
GNDD
GNDPLL
SELCLK
PCM/IOM-2
FSC
DCL/PCLK
DD/DRB
DU/DOUT
TS0/DIN
TS1/DCLK
TS2/CS
INT
MCLK
SEL24/DRA
DXA
DXB
TCA
TCB
RSYNC
RESET
TEST
IO4B
IO3B
IO2B
IO1B
IO4A
IO3A
IO2A
IO1A
AGND
* optional for SLIC-P
ezm14042.emf

Figure 97 Application Circuit, Internal Ringing (Balanced & Unbalanced)

As sown in **Figure 97** both balanced and unbalanced internal ringing uses the same line circuit.

Note: Only the codec/SLIC combinations shown in ***Table 1 "DuSLIC Chip Sets" on Page 16*** *are possible.*

8.1.2 Protection Circuit for SLIC-E/-E2 and SLIC-S

A typical overvoltage protection circuit for SLIC-E/S is shown in **Figure 98**. Other proved application schemes are available on request.

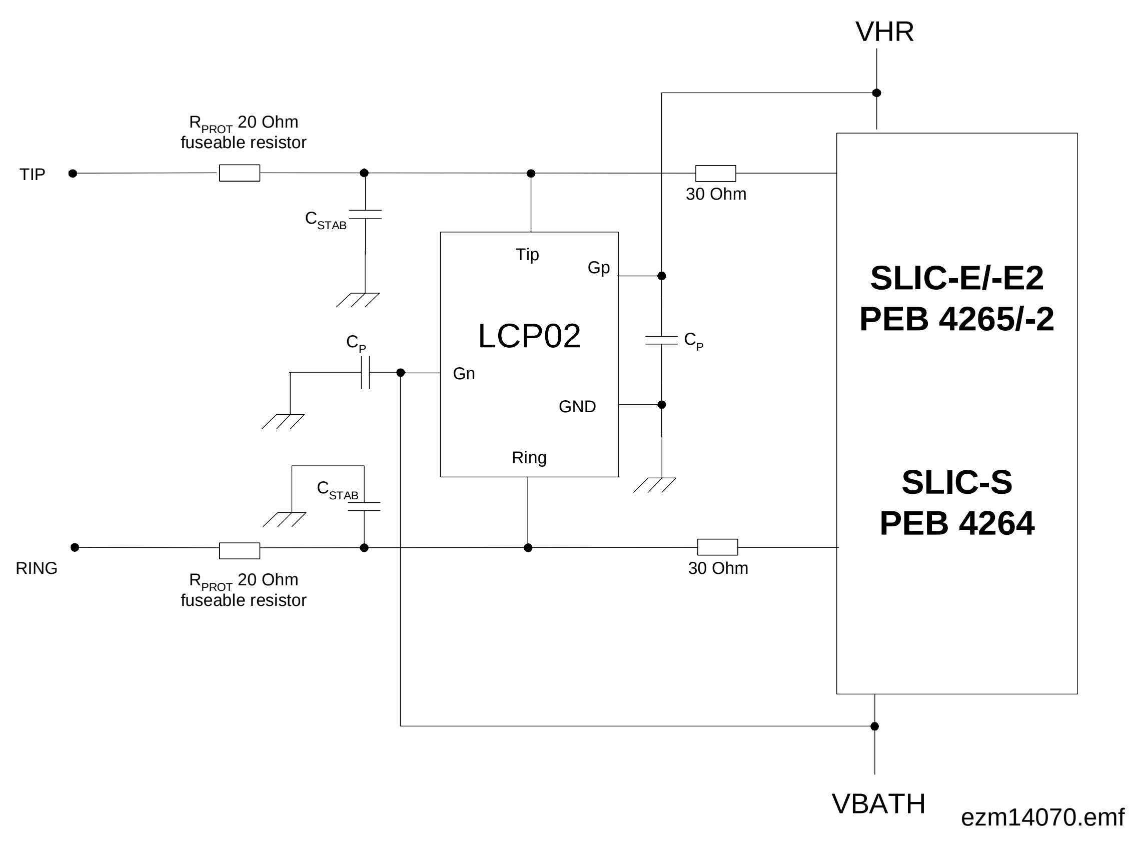

VHR
R_{PROT} 20 Ohm
fuseable resistor
TIP
C_{STAB}
30 Ohm
Tip
Gp
LCP02
C_P
Gn
C_P
GND
Ring
SLIC-E/-E2
PEB 4265/-2
SLIC-S
PEB 4264
C_{STAB}
RING
R_{PROT} 20 Ohm
fuseable resistor
30 Ohm
VBATH
ezm14070.emf

Figure 98 Typical Overvoltage Protection for SLIC-E/-E2 and SLIC-S

The LCP02 (from STM) protects against overvoltage strikes exceeding V_{HR} and V_{BATH}. Protection resistors must be rated for lightning pulses. In case of power contact, protection resistors must become high impedance or additional fuses are needed.

8.1.3 Protection Circuit for SLIC-P

A typical protection circuit for SLIC-P is shown in **Figure 99**. Other proved application schemes are available on request.

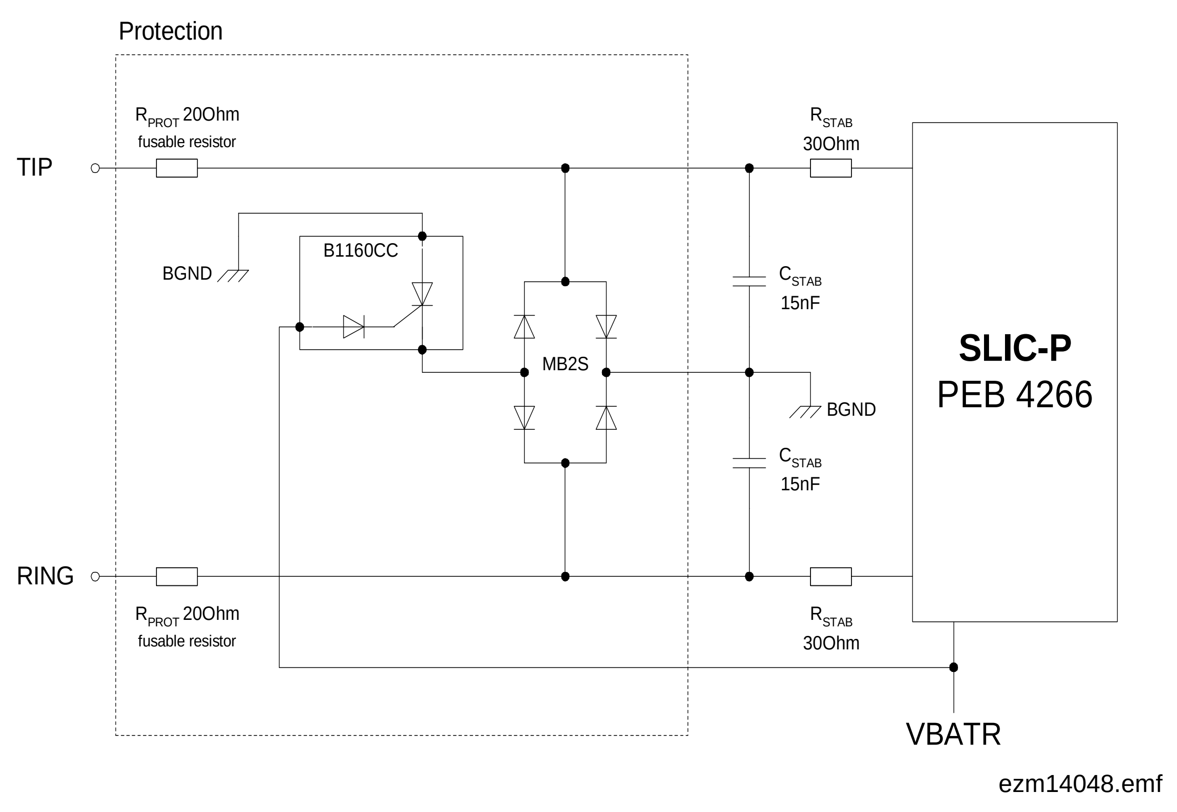

Protection
R_{PROT} 20Ohm
fusable resistor
TIP
BGND
B1160CC
MB2S
R_{STAB}
30Ohm
C_{STAB}
15nF
BGND
C_{STAB}
15nF
SLIC-P
PEB 4266
RING
R_{PROT} 20Ohm
fusable resistor
R_{STAB}
30Ohm
VBATR
ezm14048.emf

Figure 99 Typical Overvoltage Protection for SLIC-P

The gate trigger voltage of the Battrax B1160CC (Teccor) can be set down to the battery voltage of V_{BATR} (– 150 V).

Protection resistors must be rated for lightning pulses. In case of power contact, protection resistors must become high impedance or additional fuses are needed.

8.1.4 Bill of Materials (Including Protection)

Table 83 shows the external passive components needed for a dual channel solution consisting of one SLICOFI-2/-2S and two SLIC-E/-E2/-S/-P.

Table 83 External Components in Application Circuit for DuSLIC-E/-E2/-S/-P

No.	Symbol	Value	Unit	Tolerance	Rating	DuSLIC -E/-E2/-S	DuSLIC -P
2	R_{IT1}	470	Ω	1 %		x	x
2	R_{IT2}	680	Ω	1 %		x	x
2	R_{IL}	1.6	kΩ	1 %		x	x
4	R_{STAB}	30	Ω	0.1 %		x	x
4	R_{PROT}	20	Ω	0.1 %		x	x
4	C_{STAB}	15	nF	10 %	see [1]	x	x
2	C_{DC}	120	nF	10 %	10 V	x	x
2	C_{ITAC}	680	nF	10 %	10 V	x	x
2	C_{VCMIT}	680	nF	10 %	10 V	x	x
1	C_{REF}	68	nF	20 %	10 V	x	x
2	C_{EXT}	470	nF	20 %	10 V	x	x
12	C_1	100	nF	10 %		x	x
2	Battrax	B1160CC	–	–	according to supply voltage V_{BATR}		x
2	Diode-bridge	MB2S					x
2	STM	LCP-02				x	
4	C_P	220	nF	20 %	according to supply voltage V_{BATH} and V_{HR}	x	

[1] according to the highest used battery voltage $|V_{BATR}|$ for SLIC-P and $|V_{HR}|$ or $|V_{BATH}|$ for SLIC-E/-E2/-S

For handling higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, e.g., a current-compensated choke of 470 µH in the Ring/Tip lines.

Additionally to the capacitors C_1 a 22 µF capacitor per 8 Ring/Tip lines is recommended for buffering the supply voltages.

8.2 External Unbalanced Ringing with DuSLIC-E/-E2/-S/-S2/-P

External unbalanced ringing applications are shown for a standard solution (see **Figure 100**) and for a solution dedicated to higher loop lenghts (see **Figure 101**).

Note: Only the codec/SLIC combinations shown in ***Table 1 "DuSLIC Chip Sets" on Page 16*** *are possible.*

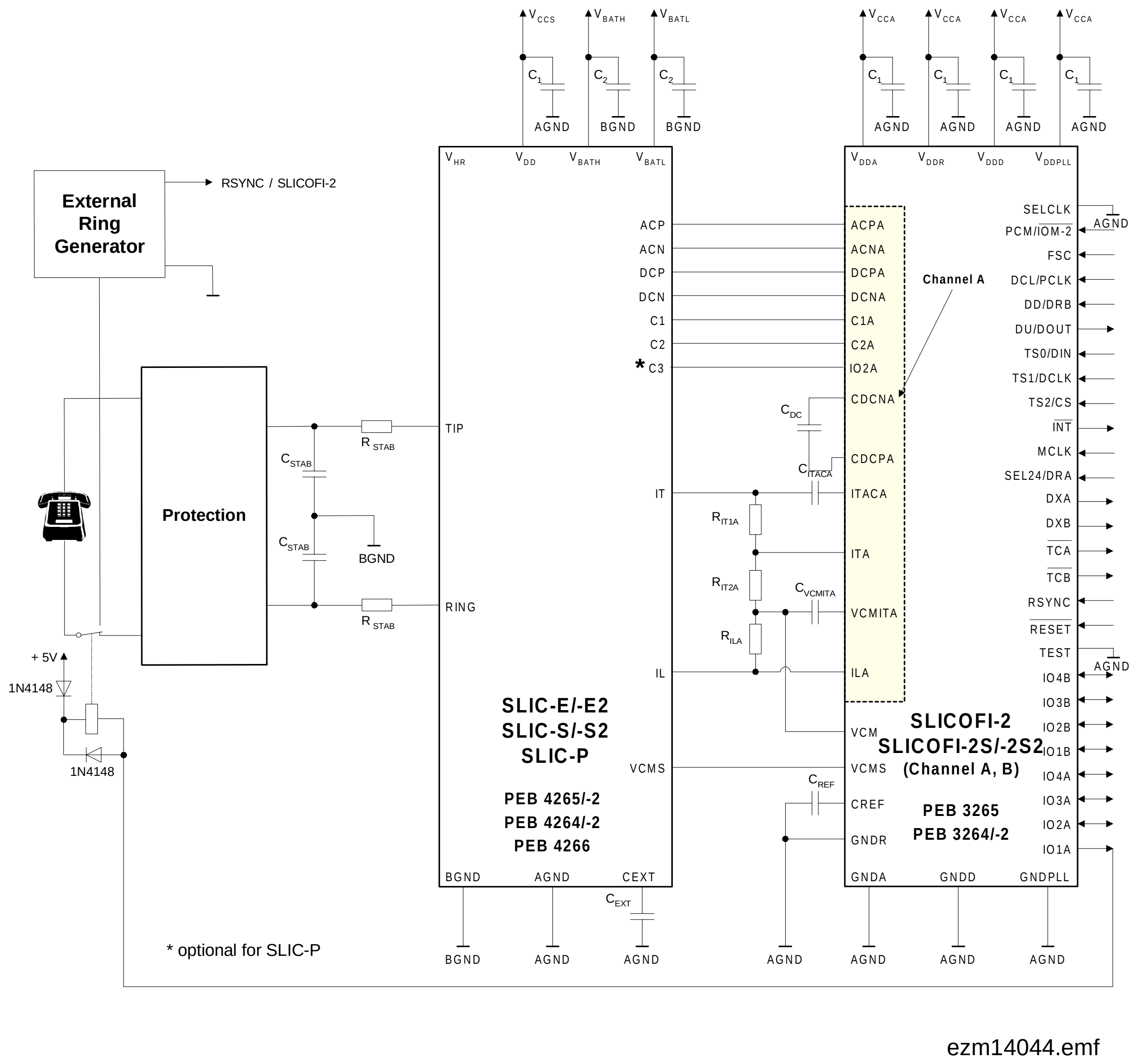

VCCS
VBATH
VBATL
C1
C2
C2
AGND
BGND
BGND
VCCA
VCCA
VCCA
VCCA
C1
C1
C1
C1
AGND
AGND
AGND
AGND
External Ring Generator
RSYNC / SLICOFI-2
VHR
VDD
VBATH
VBATL
ACP
ACN
DCP
DCN
C1
C2
* C3
TIP
IT
RING
IL
VCMS
SLIC-E/-E2
SLIC-S/-S2
SLIC-P
PEB 4265/-2
PEB 4264/-2
PEB 4266
BGND
AGND
CEXT
CEXT
BGND
AGND
AGND
Protection
CSTAB
CSTAB
RSTAB
RSTAB
BGND
+ 5V
1N4148
1N4148
* optional for SLIC-P
VDDA
VDDR
VDDD
VDDPLL
ACPA
ACNA
DCPA
DCNA
C1A
C2A
IO2A
CDCNA
CDCPA
ITACA
ITA
VCMITA
ILA
VCM
VCMS
CREF
GNDR
Channel A
CDC
CITACA
RIT1A
RIT2A
CVCMITA
RILA
CREF
SELCLK
AGND
PCM/IOM-2
FSC
DCL/PCLK
DD/DRB
DU/DOUT
TS0/DIN
TS1/DCLK
TS2/CS
INT
MCLK
SEL24/DRA
DXA
DXB
TCA
TCB
RSYNC
RESET
TEST
AGND
IO4B
IO3B
IO2B
IO1B
IO4A
IO3A
IO2A
IO1A
SLICOFI-2
SLICOFI-2S/-2S2
(Channel A, B)
PEB 3265
PEB 3264/-2
GNDA
GNDD
GNDPLL
AGND
AGND
AGND
AGND
AGND
ezm14044.emf

Figure 100 Application Circuit, External Unbalanced Ringing

This circuit senses the ring current on only one line (Tip line). It is therefore restricted to applications with low longitudinal influence (short lines).

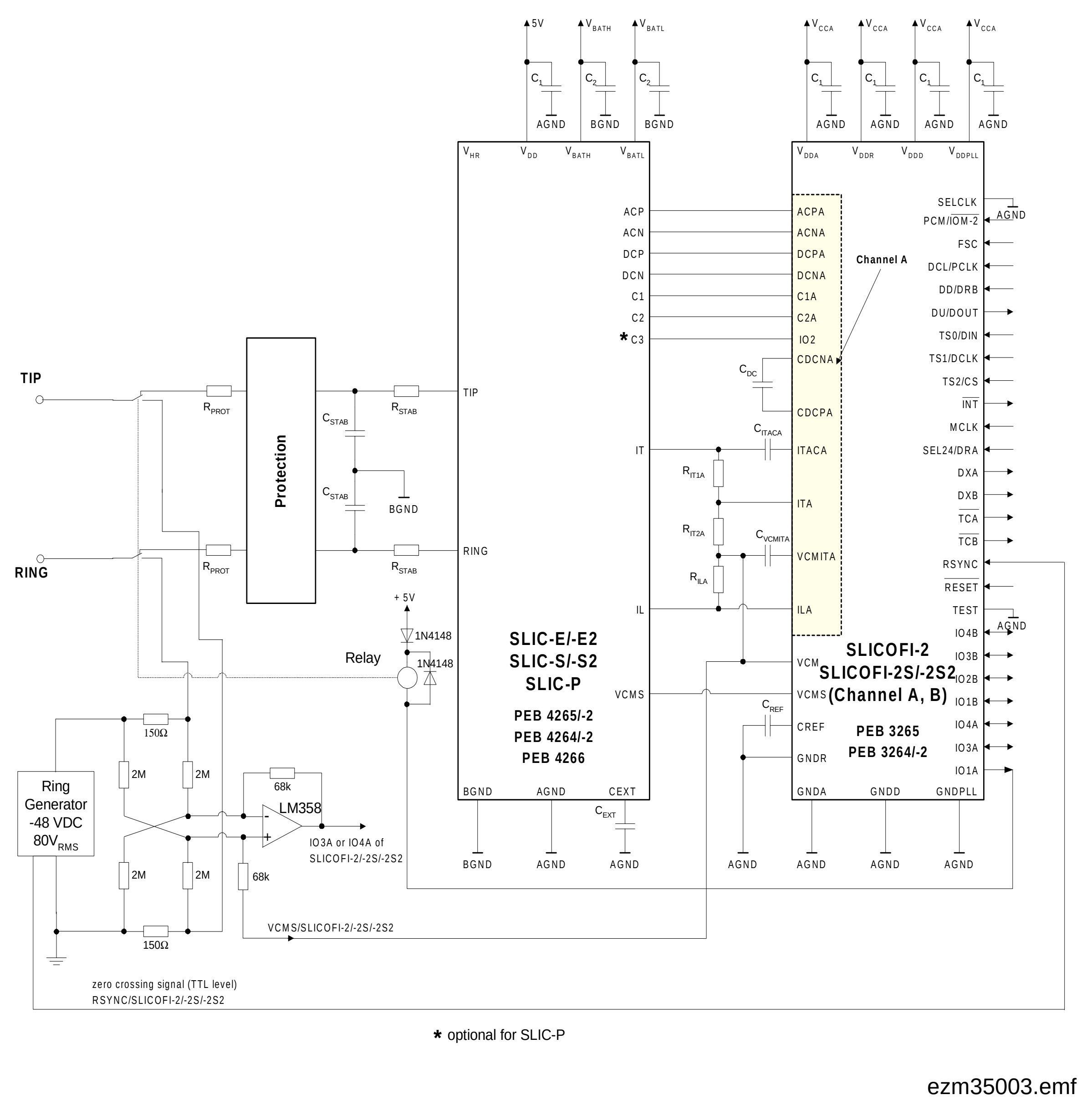

5V
V_{BATH}
V_{BATL}
V_{CCA}
C_1
C_2
AGND
BGND
V_{HR}
V_{DD}
V_{BATH}
V_{BATL}
V_{DDA}
V_{DDR}
V_{DDD}
V_{DDPLL}
ACP
ACN
DCP
DCN
C1
C2
* C3
ACPA
ACNA
DCPA
DCNA
C1A
C2A
IO2
CDCNA
CDCPA
ITACA
ITA
VCMITA
ILA
Channel A
C_{DC}
C_{ITACA}
C_{VCMITA}
R_{IT1A}
R_{IT2A}
R_{ILA}
SELCLK
PCM/IOM-2
FSC
DCL/PCLK
DD/DRB
DU/DOUT
TS0/DIN
TS1/DCLK
TS2/CS
INT
MCLK
SEL24/DRA
DXA
DXB
TCA
TCB
RSYNC
RESET
TEST
IO4B
IO3B
IO2B
IO1B
IO4A
IO3A
IO1A
TIP
RING
R_{PROT}
Protection
C_{STAB}
R_{STAB}
IT
IL
VCMS
+ 5V
1N4148
Relay
SLIC-E/-E2
SLIC-S/-S2
SLIC-P
PEB 4265/-2
PEB 4264/-2
PEB 4266
CEXT
C_{EXT}
VCM
SLICOFI-2
SLICOFI-2S/-2S2
(Channel A, B)
PEB 3265
PEB 3264/-2
CREF
C_{REF}
GNDR
GNDA
GNDD
GNDPLL
150Ω
2M
68k
LM358
Ring Generator
-48 VDC
$80V_{RMS}$
IO3A or IO4A of SLICOFI-2/-2S/-2S2
VCMS/SLICOFI-2/-2S/-2S2
zero crossing signal (TTL level)
RSYNC/SLICOFI-2/-2S/-2S2
* optional for SLIC-P
ezm35003.emf

Figure 101 Application Circuit, External Unbalanced Ringing for Long Loops

For handling higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, e.g., a current-compensated choke of 470 µH in the Ring/Tip lines.

This circuit senses the ring current in both Tip and Ring lines. Longitudinal influence is cancelled out. This circuit therefore is recommended for long line applications.

8.3 DuSLIC Layout Recommendation

- For each of the supply pins of *SLICOFI-2x* and SLIC, 100 nF capacitors should be used. These capacitors should be placed as close as possible to the supply pin of the associated ground/supply pins
- *SLICOFI-2x* and SLIC should be placed as close to each other as possible.
- *SLICOFI-2x* and SLIC should be placed in such way that lines ACP, ACN, DCP, DCN, IT, ITAC are as short as possible
- ACP/ACN lines should be placed parallel and symmetrical;
  via holes should be avoided
  ACP/ACN lines should be run above a GND plane;
- DCP/DCN lines should be placed parallel and symmetrical;
  via holes should be avoided
  DCP/DCN lines should be run above a GND plane
- VCMITA and VCM should be connected directly (VCMITA via C_{VCMITA}) at resistor R_{IT2A} (680 Ω)
- VCMITB and VCM should be connected directly (VCMITB via C_{VCMITB}) at resistor R_{IT2B} (680 Ω)
- Use separate traces for connecting VCM/VCMITA and VCM/VCMITB
  these two VCM traces should be connected directly at the VCM pin of *SLICOFI-2x*
- In case of a multilayer board it is recommended to use one common ground layer (AGND, BGND, GNDD, GNDA, GNDB, GNDPLL connected together and share one ground layer)
- In case of a two-layer board a common ground should be used for AGND, BGND, GNDD, GNDA, GNDB and GNDPLL. Ground traces should be layed out as large as possible. Connections to and from groud pins should be as short as possible. Any unused area of the board should be filled with ground (copper pouring)
- The connection of GND, V_{H} and V_{BAT} to the protection devices should be low-impedance in order to avoid, e.g., a GND shift due to the high impulse currents in case of an overvoltage strike.
- Tip/ring traces from the SLIC should be symmetrical

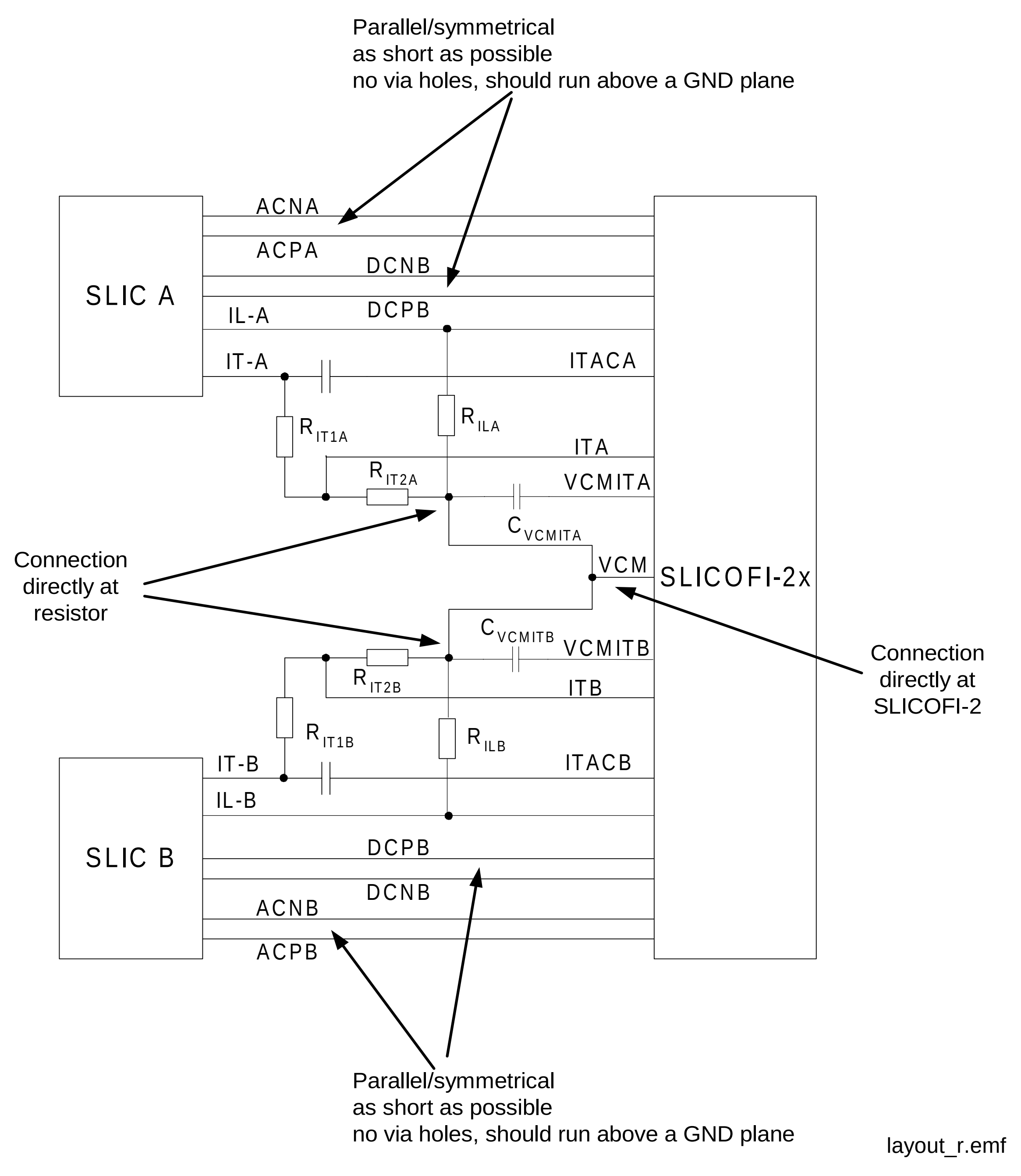
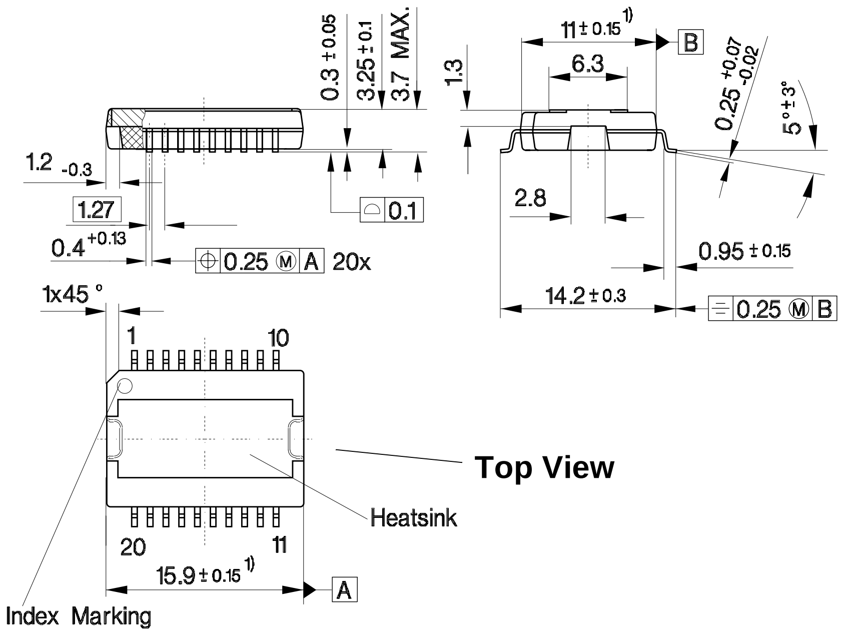

Parallel/symmetrical
as short as possible
no via holes, should run above a GND plane
SLIC A
ACNA
ACPA
DCNB
DCPB
IL-A
IT-A
ITACA
R IT1A
R ILA
ITA
R IT2A
VCMITA
C VCMITA
VCM
SLICOFI-2x
Connection
directly at
resistor
Connection
directly at
SLICOFI-2
C VCMITB
VCMITB
R IT2B
ITB
R IT1B
R ILB
IT-B
ITACB
IL-B
SLIC B
DCPB
DCNB
ACNB
ACPB
Parallel/symmetrical
as short as possible
no via holes, should run above a GND plane
layout_r.emf

Figure 102 DuSLIC Layout Recommendation

9 Package Outlines

**P-DSO-20-5
(Plastic Dual Small Outline)**


0.3 ±0.05
3.25 ±0.1
3.7 MAX.
1.3
11 ±0.15 1)
B
6.3
0.25 +0.07 -0.02
5° ±3°
1.2 -0.3
1.27
0.1
2.8
0.4 +0.13
0.25 M A 20x
0.95 ±0.15
14.2 ±0.3
0.25 M B
1x45 °
1
10
Top View
Heatsink
20
11
15.9 ±0.15 1)
A
Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

Gps05755.eps

Figure 103 PEB426x (SLIC-S/-S2, SLIC-E/-E2, SLIC-P)

Note: The SLIC is only available in a P-DSO-20-5 package with heatsink on top. Please note that the pin counting for the P-DSO-20-5 package is clockwise (top view) in contrast to similar type packages which mostly count counterclockwise.

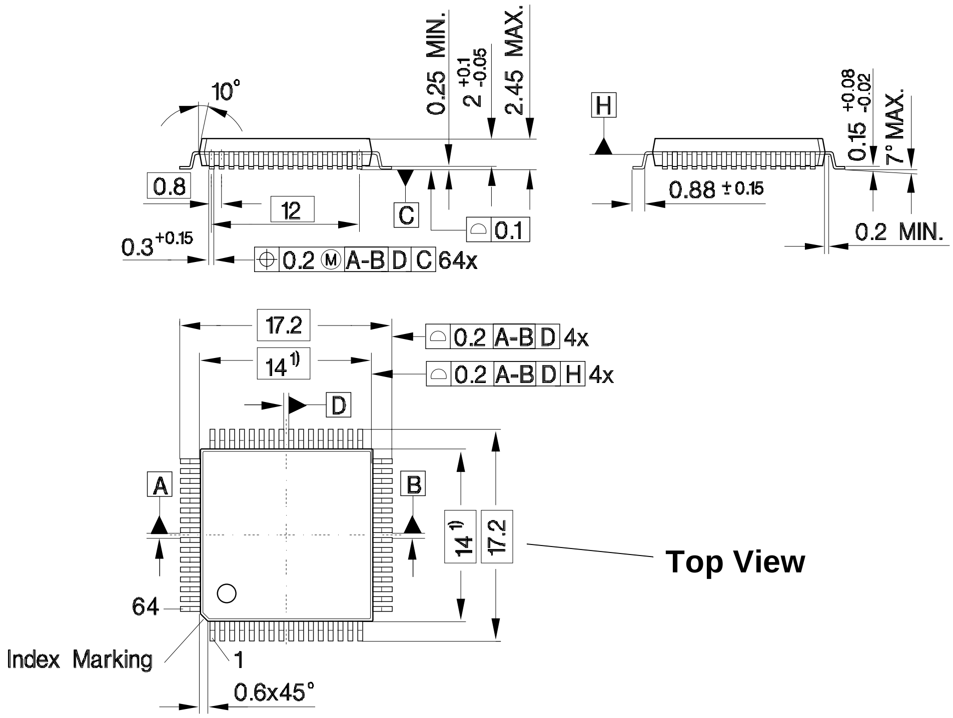
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our data book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-MQFP-64-1
(Plastic Metric Quad Flat Package)


10°
0.25 MIN.
2 +0.1 -0.05
2.45 MAX.
H
+0.08 -0.02
0.15
7° MAX.
0.8
12
C
0.1
0.88 ±0.15
0.2 MIN.
0.3 +0.15
0.2 Ⓜ A-B D C 64x
17.2
14 1)
0.2 A-B D 4x
0.2 A-B D H 4x
D
A
B
14 1)
17.2
Top View
64
Index Marking
1
0.6x45°

1) Does not include plastic or metal protrusion of 0.25 max. per side

Gpm05250.eps

Figure 104 PEB 3264, PEB 3264-2, PEB 3265 (SLICOFI-2x)

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our data book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

10 Glossary

10.1 List of Abbreviations

ACTL	Active with V_{BATL} and V_{BGND}
ACTH	Active with V_{BATH} and V_{BGND}
ACTR	Active with V_{BATR} and V_{GND} or V_{HR} and V_{BATH}
ADC	Analog Digital Converter
AR	Attenuation Receive
AX	Attenuation Transmit
BP	Band Pass
CMP	Compander
Codec	Coder Decoder
COP	Coefficient Operation
CRAM	Coefficient RAM
DAC	Digital Analog Converter
DSP	Digital Signal Processor
DUP	Data Upstream Persistence Counter
DuSLIC	Dual Channel Subscriber Line Interface Concept
EXP	Expander
FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter
LSSGR	Local area transport access Switching System Generic Requirements
PCM	Pulse Code Modulation
PDH	Power Down High Impedance

PDRHL	Power Down Load Resistive on V_{BATH} and V_{BGND}
PDRRL	Power Down Load Resisitve on V_{BATR} and V_{BGND}
PDRH	Power Down Resistive on V_{BATH} and V_{BGND}
PDRR	Power Down Resistive on V_{BATR} and V_{BGN}
POFI	Post Filter
PREFI	Antialiasing Pre Filter
RECT	Rectifier (Testloops, Levelmetering)
SLIC	Subscriber Line Interface Circuit (synonym for all versions)
SLIC-S/-S2	Subscriber Line Interface Circuit Standard Feature Set PEB 4264/-2
SLIC-E/-E2	Subscriber Line Interface Circuit Enhanced Feature Set PEB 4265/-2
SLIC-P	Subscriber Line Interface Circuit Enhanced Power Management PEB 4266
SLICOFI-2x	Dual Channel Signal Processing Subscriber Line Interface Codec Filter (synonym for all versions)
SLICOFI-2	Dual Channel Signal Processing Subscriber Line Interface Codec Filter PEB 3265
SLICOFI-2S/-2S2	Dual Channel Signal Processing Subscriber Line Interface Codec Filter PEB 3264/-2
SOP	Status Operation
TG	Tone Generator
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
TS	Time Slot
TTX	Teletax

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