LXT973

10/100 Mbps Dual-Port Fast Ethernet PHY Transceiver

Datasheet

The LXT973 is an IEEE-compliant, 2-port, Fast Ethernet PHY transceiver that directly supports both 100BASE-TX and 10BASE-T applications. Each port provides a Media Independent Interface (MII) for easy attachment to 10 and 100 Mbps Media Access Controllers (MACs). The device also provides a pseudo-ECL interface per port for use with 100BASE-FX fiber networks. The LXT973 incorporates the auto MDIX feature, allowing it to automatically switch twisted-pair inputs and outputs.

The LXT973 is an ideal building block for systems that require two Ethernet ports, such as Internet Protocol (IP) Telephones, Twisted-Pair (TX)-to-Fiber (FX) converter modules, and for telecom applications, such as Telecom Central Office (TCO) and Customer Premise Equipment (CPE) devices.

The LXT973 supports full-duplex operation at both 10 and 100 Mbps. Its operating modes can be set using auto-negotiation, parallel detection, or manual control.

Applications

- VoIP Telephone Handsets
- Media Converter
  - —Fiber-to-Twisted-Pair
- Internet Access Devices
  - —Cable Modem, ADSL Modem
- Ethernet Backplane Connections

Product Features

- Dual-port Fast Ethernet PHY
- 2.5V operation
- 3.3V operation I/O compatibility
- Low power consumption; 250 mW per port typical
- Full 2-port MII interface with extended registers
- Auto MDI/MDIX switch over capability
- Signal Quality Error (SQE) enable/disable
- 100BASE-FX fiber-optic capability on both ports
- Integrated transmit and receive termination resistors
- Supports both auto-negotiation systems and legacy systems without auto-negotiation capability
- Support for Next Page
- 20 MHz Register Access
- Configurable via MDIO port or external control pins
- Integrated termination resistors
- 100-pin Plastic Quad Flat Package (PQFP)
  - —LXT973QC - Commercial (0° to 70°C ambient).
  - —LXT973QE - Extended (-40° to +85°C ambient).

For technical assistance on this product, please call 1-800-628-8686, or send an e-mail tosupport@mailbox.intel.com.

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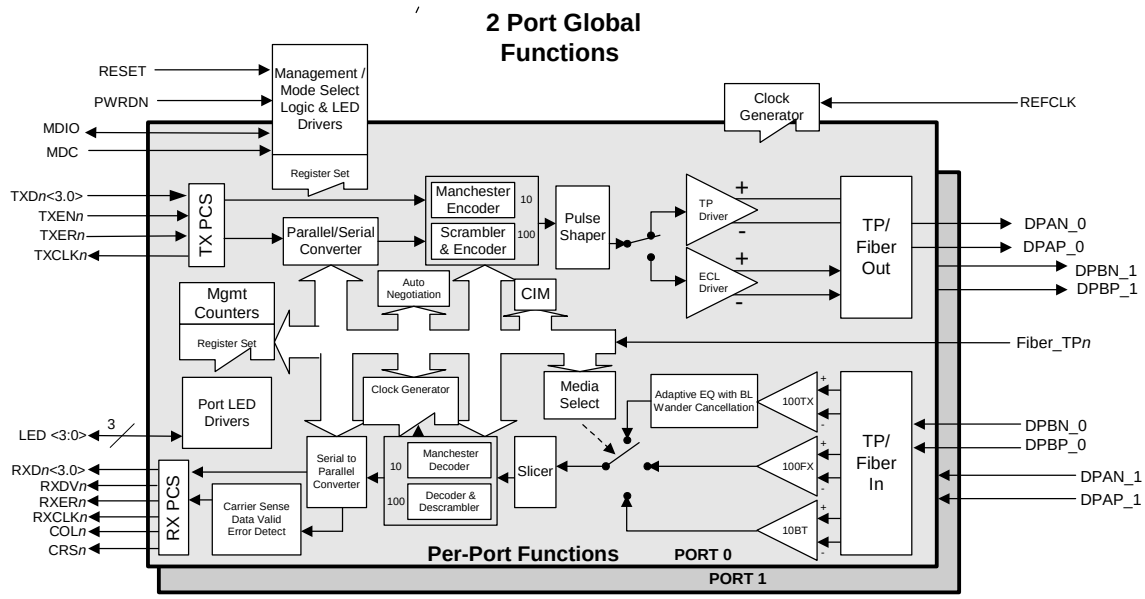
Revision History

Date	Revision	Page	Description
March 1, 2001	002	11	Figure 1 “LXT973 Block Diagram”: Added note to diagram.
		37	Under Section 3.8.4, “PMA Sublayer”: Removed Table 10: 4B/5B Coding.
		39	Section 3.10.1, “Monitoring Auto-Negotiation”: Removed paragraphs 3 and 4, and Figure 11.
		53	Under Section 8.1, “Displaying Symbol Errors”: Removed Table 16: 4B/5B Coding.
		61	Section 12.0, “Register Definitions” Removed “multiple 11-bit registers, with” from first sentence.
		64	Table 20 “PHY Identification Register 2 (Address 3)”: Changed default for Register bits 3.9:4 from “001110” to “100001”.
		72	Table 29 “Absolute Maximum Ratings” Modified Power Supply: added VCCA, VCC, VCCPECL, VCCIO information. Added three table notes.
		73	Table 40 “Digital Input/Output Characteristics” Modified table note 2.
		73	Table 32 “Digital Input/Output Characteristics - MII Pins” Removed “Driver Output Impedance.”
		74	Table 34 “LED Pin Characteristics” Added MAX value to Output High Current.
		74	Table 35 “100BASE-TX Transceiver Characteristics” Added Typ values.
		75	Table 36 “10BASE-T Transceiver Characteristics” Added/replaced Typ values. Removed “Receiver Input Impedance.”
		75	Table 37 “100BASE-FX Transceiver Characteristics” Added Typ values
		75	Table 38 “10BASE-T Link Integrity Timing Characteristics” Added Typ value for Link Pulse Width
		76	Added Table 39 “Twisted-Pair Pins”.
		77-85	Modified Table 40 on page 77 through Table 49 on page 85.
		86	Added Figure 39 “Power-Up Timing” and Table 50 “Power-Up Timing Parameters”.
		86	Added Figure 40 “RESET Pulse Width and Recovery Timing” and Table 51 “RESET Pulse Width and Recovery Timing Parameters”
		88	Section A, “Product Ordering Information”: Added product ordering information table and diagram.
May 2001	001		Initial Release (Preliminary datasheet)
April 2001	0.2		Advance Datasheet (See Specification Update for Detail)
February 2001	0.1		Advance Datasheet

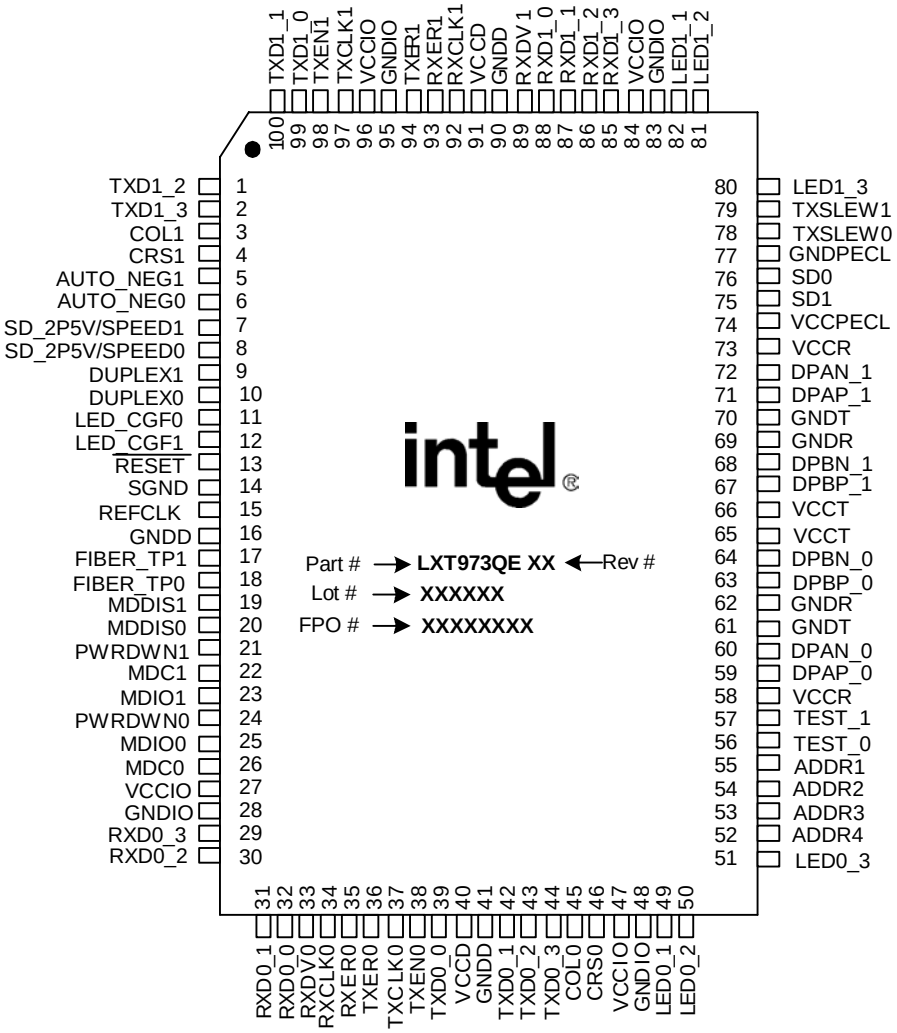
Figure 1. LXT973 Block Diagram



Please see Table 4, “LXT973 Network Interface Signal Descriptions” on page 18 and Table 5, “LXT973 Global Control & Configuration Signal Descriptions” on page 19 for complete network interface signal

1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT973 Pin Assignments



Package Topside Markings

Marking	Definition
Part #	LXT973 is the unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” (Refer to Specification Update for additional stepping information.)
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. LXT973 PQFP Pin List

Pin	Signal Names	Type[1]	Reference for Full Description
1	TXD1_2	I	Table 3 on page 17
2	TXD1_3	I	Table 3 on page 17
3	COL1	O, TS	Table 3 on page 17
4	CRS1	O, TS	Table 3 on page 17
5	AUTO_NEG1	I	Table 7 on page 20
6	AUTO_NEG0	I	Table 7 on page 20
7	SD_2P5V/SPEED1	I	Table 7 on page 20
8	SD_2P5V/SPEED0	I	Table 7 on page 20
9	DUPLEX1	I	Table 7 on page 20
10	DUPLEX0	I	Table 7 on page 20
11	LED_CGF0	I	Table 5 on page 19
12	LED_CGF1	I	Table 5 on page 19
13	$\overline{\text{RESET}}$	I	Table 5 on page 19
14	SGND	–	Table 6 on page 20
15	REFCLK	I	Table 5 on page 19
16	GNDD	–	Table 6 on page 20
17	FIBER_TP1	I	Table 7 on page 20
18	FIBER_TP0	I	Table 7 on page 20
19	MDDIS1	I	Table 3 on page 17
20	MDDIS0	I	Table 2 on page 16
21	PWRDWN1	I	Table 7 on page 20
22	MDC1	I	Table 3 on page 17
23	MDIO1	I/O	Table 3 on page 17
24	PWRDWN0	I	Table 7 on page 20
25	MDIO0	I/O	Table 2 on page 16
26	MDC0	I	Table 2 on page 16
27	VCCIO	–	Table 6 on page 20
28	GNDIO	–	Table 6 on page 20
29	RXD0_3	O, TS	Table 2 on page 16
30	RXD0_2	O, TS	Table 2 on page 16
31	RXD0_1	O, TS	Table 2 on page 16
32	RXD0_0	O, TS	Table 2 on page 16
33	RXDV0	O, TS	Table 2 on page 16

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 1. LXT973 PQFP Pin List (Continued)

Pin	Signal Names	Type[1]	Reference for Full Description
34	RXCLK0	O, TS	Table 2 on page 16
35	RXER0	O, TS	Table 2 on page 16
36	TXER0	I	Table 2 on page 16
37	TXCLK0	O, TS	Table 2 on page 16
38	TXEN0	I	Table 2 on page 16
39	TXD0_0	I	Table 2 on page 16
40	VCCD	–	Table 6 on page 20
41	GNDD	–	Table 6 on page 20
42	TXD0_1	I	Table 2 on page 16
43	TXD0_2	I	Table 2 on page 16
44	TXD0_3	I	Table 2 on page 16
45	COL0	O, TS	Table 2 on page 16
46	CRS0	O, TS	Table 2 on page 16
47	VCCIO	–	Table 6 on page 20
48	GNDIO	–	Table 6 on page 20
49	LED0_1	O, OD	Table 7 on page 20
50	LED0_2	O, OD	Table 7 on page 20
51	LED0_3	O, OD	Table 7 on page 20
52	ADDR4	I	Table 5 on page 19
53	ADDR3	I	Table 5 on page 19
54	ADDR2	I	Table 5 on page 19
55	ADDR1	I	Table 5 on page 19
56	TEST_0	I	Table 5 on page 19
57	TEST_1	I	Table 5 on page 19
58	VCCR	–	Table 6 on page 20
59	DPAP_0	AI/AO, SL	Table 4 on page 18
60	DPAN_0	AI/AO, SL	Table 4 on page 18
61	GNDT	–	Table 6 on page 20
62	GNDR	–	Table 6 on page 20
63	DPBP_0	AI/AO, SL	Table 4 on page 18
64	DPBN_0	AI/AO, SL	Table 4 on page 18
65	VCCT	–	Table 6 on page 20
66	VCCT	–	Table 6 on page 20
67	DPBP_1	AI/AO, SL	Table 4 on page 18

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 1. LXT973 PQFP Pin List (Continued)

Pin	Signal Names	Type[1]	Reference for Full Description
68	DPBN_1	AI/AO, SL	Table 4 on page 18
69	GNDR	–	Table 6 on page 20
70	GNDT	–	Table 6 on page 20
71	DPAP_1	AI/AO, SL	Table 4 on page 18
72	DPAN_1	AI/AO, SL	Table 4 on page 18
73	VCCR	–	Table 6 on page 20
74	VCCPECL	–	Table 6 on page 20
75	SD1	I	Table 4 on page 18
76	SD0	I	Table 4 on page 18
77	GNDPECL	–	Table 6 on page 20
78	TxSLEW0	I	Table 5 on page 19
79	TxSLEW1	I	Table 5 on page 19
80	LED1_3	O. OD	Table 7 on page 20
81	LED1_2	O, OD	Table 7 on page 20
82	LED1_1	O, OD	Table 7 on page 20
83	GNDIO	–	Table 6 on page 20
84	VCCIO	–	Table 6 on page 20
85	RXD1_3	O, TS	Table 3 on page 17
86	RXD1_2	O, TS	Table 3 on page 17
87	RXD1_1	O, TS	Table 3 on page 17
88	RXD1_0	O, TS	Table 3 on page 17
89	RXDV1	O, TS	Table 3 on page 17
90	GNDD	–	Table 6 on page 20
91	VCCD	–	Table 3 on page 17
92	RXCLK1	O, TS	Table 3 on page 17
93	RXER1	O, TS	Table 3 on page 17
94	TXER1	I	Table 6 on page 20
95	GNDIO	–	Table 6 on page 20
96	VCCIO	–	Table 3 on page 17
97	TXCLK1	O, TS	Table 3 on page 17
98	TXEN1	I	Table 3 on page 17
99	TXD1_0	I	Table 3 on page 17
100	TXD1_1	I	Table 3 on page 17

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

2.0 Signal Descriptions

Table 2. LXT973 Port 0 Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
44 43 42 39	TXD0_3 TXD0_2 TXD0_1 TXD0_0	I	**Transmit Data**. TXD0_*n* is a bundle of parallel data signals driven by the MAC controller, which TXD0<3:0> transition synchronously with respect to the TXCLK0. TXD0<0> is the least significant bit. TXD0<3:0> are monitored in normal mode only.
38	TXEN0	I	**Transmit Enable.** The MAC asserts TXEN0 when it drives data on TXD0*n*. This signal must be synchronized to TXCLK0.
36	TXER0	I	**Transmit Error.** TXER0 is a 100 Mbps only signal. The MAC asserts this input when an error has occurred in the transmit data stream. When operating at 100 Mbps, the LXT973 responds by sending "H symbols" on the line. In Symbol mode, this pin acts as TXD0_4.
37	TXCLK0	O, TS	**Transmit Clock.** TXCLK0 is sourced by the LXT973 in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
29 30 31 32	RXD0_3 RXD0_2 RXD0_1 RXD0_0	O, TS	**Receive Data.**The LXT973 drives received data on these outputs, synchronous to RXCLK0.
33	RXDV0	O, TS	**Receive Data Valid.** The LXT973 asserts this signal when it drives valid data on RXD0*n*. This output is synchronous to RXCLK0.
35	RXER0	O, TS	**Receive Error.** The LXT973 asserts this output when it receives invalid symbols from the network. RXER0 is synchronous to RXCLK0. In Symbol mode, this pin acts as RXD0_4.
34	RXCLK0	O, TS	**Receive Clock.** RXCLK0 is sourced by the LXT973 in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
45	COL0	O, TS	**Collision Detected.** The LXT973 asserts this output when a collision is detected. This output remains High for the duration of the collision. COL0 is asynchronous and is inactive during full-duplex operation.
46	CRS0	O, TS	**Carrier Sense.** During half-duplex operation, the LXT973 asserts this output when either the transmit or receive medium is non-idle. During full-duplex operation, CRS0 is asserted only when receive medium is non-idle.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 2. LXT973 Port 0 Signal Descriptions (Continued)

Pin #	Signal Names	Type[1]	Signal Description
20	MDDIS0	I	**Management Disable**. When MDDIS0 is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS0 is pulled Low at power-up or reset via the internal pull-down resistor or by tying it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
26	MDC0	I	**Management Data Clock.** Clock for MDIO0 serial channel. Maximum frequency is 20 MHz.
25	MDIO0	I/O	**Management Data Input/Output.** Bi-directional serial data channel for PHY/STA communication.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 3. LXT973 Port 1 Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
2 1 100 99	TXD1_3 TXD1_2 TXD1_1 TXD1_0	I	**Transmit Data.** TXD1_n is a bundle of parallel data signals driven by the MAC controller. TXD1<3:0> transition synchronously with respect to the TXCLK1. TXD1<0> is the least significant bit. In normal mode, only TXD1<3:0> are monitored.
98	TXEN1	I	**Transmit Enable.** The MAC asserts TXEN1 when it drives data on TXD0*n*. This signal must be synchronized to TXCLK1.
94	TXER1	I	**Transmit Error.** (TXER1 is a 100 Mbps only signal.**)** The MAC asserts this input when an error has occurred in the transmit data stream. When operating at 100 Mbps, the LXT973 responds by sending "H Symbols" on the line. In Symbol mode, this pin acts as TXD1_4.
97	TXCLK1	O, TS	**Transmit Clock.** TXCLK1 is sourced by the LXT973 in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
85 86 87 88	RXD1_3 RXD1_2 RXD1_1 RXD1_0	O, TS	**Receive Data.**The LXT973 drives received data on these outputs, synchronous to RXCLK1.
89	RXDV1	O, TS	**Receive Data Valid.** The LXT973 asserts this signal when it drives valid data on RXD0*n*. This output is synchronous to RXCLK1.
93	RXER1	O, TS	**Receive Error.** The LXT973 asserts this output when it receives invalid symbols from the network. RXER1 is synchronous to RXCLK1. In Symbol mode, this pin acts as RXD1_4.
92	RXCLK1	O, TS	**Receive Clock.** RXCLK1 is sourced by the LXT973 in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 3. LXT973 Port 1 Signal Descriptions (Continued)

Pin #	Signal Names	Type[1]	Signal Description
3	COL1	O, TS	**Collision Detected.** The LXT973 asserts this output when a collision is detected. This output remains High for the duration of the collision. COL is asynchronous and is inactive during full-duplex operation.
4	CRS1	O, TS	**Carrier Sense.** During half-duplex operation, the LXT973 asserts this output when either the transmit or receive medium is non-idle. During full-duplex operation, CRS1 is asserted only when receive medium is non-idle.
19	MDDIS1	I	**Management Disable**. When MDDIS is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS is pulled Low at power-up or reset via the internal pull-down resistor or by tieing it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
22	MDC1	I	**Management Data Clock.** Clock for MDIO1 serial channel. Maximum frequency is 20 MHz. (**Note:** 20 MHz value to be verified prior to final production release of product.)
23	MDIO1	I/O	**Management Data Input/Output.** Bidirectional serial data channel for PHY/STA communication.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 4. LXT973 Network Interface Signal Descriptions

Pin #	Signal Names	TP Op	Fiber Op	Port	Pair Type	Type[1]	Signal Description
59 60	DPAP_0 DPAN_0	TX+ TX-	RX+ RX-	0 0	A A	AI/AO, SL	**Twisted-Pair/Fiber Pair A, Positive & Negative - Port 0.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as receiver in Fiber mode.
63 64	DPBP_0 DPBN_0	RX+ RX-	TX+ TX-	0 0	B B	AI/AO, SL	**Twisted-Pair/Fiber Pair B, Positive & Negative - Port 0.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as transmitter in Fiber mode.
76	SD0	-	-	-	-	I	**Signal Detect.** This signal is used for signal quality indication in Fiber mode. In twisted-pair mode, this pin should be tied Low.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 4. LXT973 Network Interface Signal Descriptions (Continued)

Pin #	Signal Names	TP Op	Fiber Op	Port	Pair Type	Type[1]	Signal Description
67 68	DPBP_1 DPBN_1	TX+ TX-	TX- TX+	1 1	B B	AI/AO, SL	**Twisted-Pair/Fiber Pair B, Positive & Negative - Port 1.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as transmitter in Fiber mode.
71 72	DPAP_1 DPAN_1	RX+ RX-	RX- RX+	1 1	A A	AI/AO, SL	**Twisted-Pair/Fiber Pair A, Positive & Negative - Port 1.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as receiver in Fiber mode.
75	SD1	-	-	-	-	I	**Signal Detect.** This signal is used for signal quality indication in Fiber mode. In twisted-pair mode, this pin should be tied Low.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 5. LXT973 Global Control & Configuration Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
78 79	TxSLEW0 TxSLEW1	I	**Tx Output Slew Controls 0 & 1.** These pins select the TX output slew rate (rise and fall time) for both cores in the LXT973 device. The various options are defined in Register bits 27.11:10. The TxSLEW pins set the power-on value of these register bits.
13	$\overline{\text{RESET}}$	I	**Reset.** This active Low input is OR'd with Control Register bit 0.15.
52 53 54 55	ADDR4 ADDR3 ADDR2 ADDR1	I	**Address <4:1>.** Sets device Port 0 PHY address. Note that ADDR0 is set internally so that Port 1 is always "1" address higher than Port 0.
56 57	TEST_0 TEST_1	I	**Test Pins.** Tie Low for normal operation.
15	REFCLK	I	**Master Clock Input.** A 25 MHz, 50 ppm clock is input here to act as the master clock. Full clock requirements are detailed in the Clock Requirements section of the Functional Description. See Section 3.4.2, "Clock Requirements" on page 28.
11 12	LED_CFG0 LED_CFG1	I	**LED Configuration 0 & 1.** These pins are used to select one of four LED modes. The decode or each mode is shown below:

LED_CFG0	LED_CFG1	LEDn_1	LEDn_2	LEDn_3
0	0	Speed	Link	Duplex
1	0	Speed	Link/Activity	Duplex/Collision
0	1	Link	Receive	Transmit
1	1	Speed	Link/MII Isolate	Duplex/Collision

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 6. LXT973 Power Supply Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
40, 91	VCCD	_	**Digital Power Supply - Core. +**2.5V supply for core digital circuits.
27, 47, 84, 96	VCCIO	_	**Digital Power Supply - I/O Ring.** +2.5/3.3V supply for digital I/O circuits. The digital input circuits running off this rail, having a TTL-level threshold and over-voltage protection, may be interfaced with 3.3/5.0V when the I/O supply is 3.3V, and 2.5/3.3/5.0V when the I/O supply is 2.5V.
74	VCCPECL	_	**Digital Power Supply - PECL Signal Detect Inputs.** +2.5/3.3V supply for PECL Signal Detect input circuits. If Fiber Mode is not used, tie these pins to GNDPECL to save power.
58, 73	VCCR	_	**Analog Power Supply - Receive.** +2.5V supply for all analog receive circuits.
65, 66	VCCT	_	**Analog Power Supply - Transmit.** +2.5V supply for all analog transmit circuits.
16, 41, 90,	GNDD	_	**Digital Ground**. Ground return for core digital supplies (VCCD). All ground pins can be tied together using a single ground plane.
28, 48, 83, 95	GNDIO	_	**Digital GND - I/O Ring.** Ground return for digital I/O circuits (VCCIO).
77	GNDPECL	_	**Digital GND - PECL Signal Detect Inputs.** Ground return for PECL Signal Detect input circuits.
69, 62	GNDR	_	**Analog Ground - Receive**. Ground return for receive analog supply. All ground pins can be tied together using a single ground plane.
61, 70	GNDT	_	**Analog Ground - Transmit**. Ground return for transmit analog supply. All ground pins can be tied together using a single ground plane.
14	SGND	_	**Substrate Ground**. Ground for chip substrate. All ground pins can be tied together using a single ground plane.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 7. LXT973 Per Port LED and Configuration Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
49 50 51	LED0_1 LED0_2 LED0_3	OD, TS, SL, IP	**Port 0 LED Drivers 1-3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register.
82 81 80	LED1_1 LED1_2 LED1_3	OD, TS, SL, IP	**Port 1 LED Drivers 1-3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register.
6 5	AUTO_NEG0 AUTO_NEG1	I I	**Auto Negotiation Enable.** When this pin is High, auto-negotiation is enabled on the relevant port.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 7. LXT973 Per Port LED and Configuration Signal Descriptions (Continued)

Pin #	Signal Names	Type[1]	Signal Description
8 7	SD_2P5V/SPEED0 SD_2P5V/SPEED1	I I	**SD_2P5V.** In fiber mode, these pins select between a 2.5V or 3.3V fiber transceiver. High is for 2.5V and low is for 3.3V. **Speed.** Set the default speed of the port in Hardware mode. High is 100 Mbps and Low is 10 Mbps.
10 9	DUPLEX0 DUPLEX1	I I	**Duplex.** Sets the duplex setting of the port in Hardware mode. High is full-duplex and Low is half-duplex.
18 17	FIBER_TP0 FIBER_TP1	I I	**Fiber/Twisted-Pair.** Sets the operating state of the port in Hardware mode. High is twisted-pair and Low is fiber.
24 21	PWRDWN0 PWRDWN1	I	**Power-Down.** When set High, this pin puts the relevant PHY into power-down mode.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Tri-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

3.0 Functional Description

3.1 Introduction

The LXT973 is an IEEE-compliant, dual-port, Fast Ethernet PHY transceiver that directly supports both 100BASE-TX and 10BASE-T applications. The device incorporates full Media Independent Interface (MII), enabling each individual network port to connect with 10/100 Mbps MACs. Each port directly drives either a 100BASE-TX line or a 10BASE-T line (up to 160 meters). The LXT973 also supports 100BASE-FX operation via a Pseudo-ECL (PECL) interface. The device uses a 100-pin QFP package.

3.1.1 Comprehensive Functionality

The LXT973 performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

On power-up, the LXT973 reads its configuration inputs to check for forced operation settings. If not configured for forced operation, each port uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the link partner supports auto-negotiation, the LXT973 auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT973 automatically detects (parallel detection) the presence of either link pulses (10 Mbps PHY) or IDLE symbols (100 Mbps PHY) and sets its operating conditions accordingly. When parallel detection is used to establish link, the resulting link is at half-duplex. The LXT973 provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

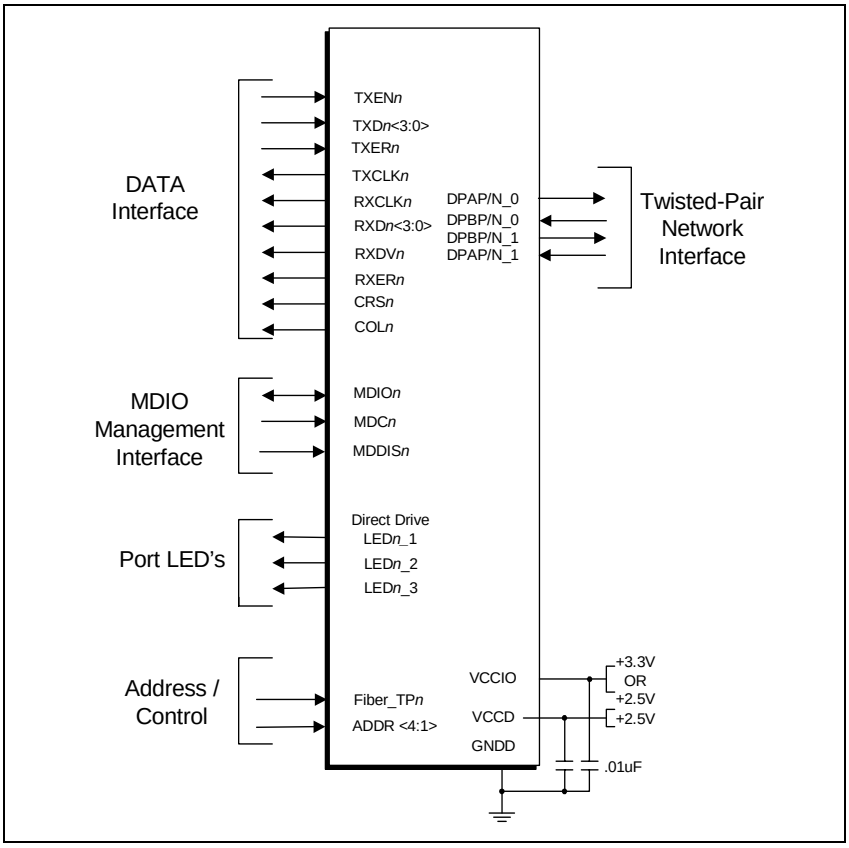
3.2 Interface Descriptions

3.2.1 10/100 Mbps Network Interface

The LXT973 supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX). Each network interface port consists of four external pins (two differential signal pairs). The pins are shared between twisted-pair and fiber.

The LXT973 output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the device generates IEEE 802.3-compliant link pulses or IDLE code. Input signals are decoded either as a 100BASE-TX, 100BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface. Polarity is determined by the MDI crossover function.

Figure 3. LXT973 Interfaces



3.2.1.1 Twisted-Pair Interface

The LXT973 supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted-Pair (UTP). Only a transformer, RJ-45, and bypass capacitors are required to complete this interface. Using Intel's patented waveshaping technology, the transmitter shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings allow the designer to match the output waveform to the magnetic characteristics. Both transmit and receive terminations are built into the LXT973. Therefore, no external components are required between the LXT973 and the external transformer. The transmitter uses a transformer with a center tap to help reduce power consumption.

When operating at 100 Mbps, MLT3 symbols are continuously transmitted and received. When not transmitting data, the LXT973 generates "IDLE" symbols.

During 10 Mbps operation, LXT973 encoded data is exchanged. When no data is exchanged, the line transmits normal link pulses to maintain link.

3.2.1.2 MDI Crossover (MDIX)

The LXT973 crossover function, which is compliant to the IEEE 802.3, clause 23 standard, connects the transmit output of the device to the far-end receiver in a link segment. This function can be configured via Register bits 27.9:8. Please refer to Section 7.0, "Auto MDI/MDIX" on page 52. Default mode is auto-MDIX enabled.

3.2.1.3 Fiber Interface

The LXT973 provides a PECL interface that complies with the ANSI X3.166 specification. This interface is suitable for driving a fiber-optic coupler (see Figure 14 on page 46).

Fiber ports cannot be enabled via auto-negotiation and must be enabled via the Global Hardware Control Interface pins or MDIO registers. Using external circuitry, the LXT973 can interface the fiber transceiver with 2.5V or 3.3V supply voltages. Fiber mode per port may be selected using Register bit 16.0. Please refer to Table 4 on page 18 for correct pin assignments.

3.3 MII Operation

The LXT973 device implements the Media Independent Interface (MII) as defined in the IEEE 802.3 standard. Separate channels are provided for transmitting data from the MAC to the LXT973 (TXD), and for passing data received from the line (RXD) to the MAC. Each channel has its own clock, data bus, and control signals. Nine signals are used to pass received data to the MAC: RXD<3:0>, RXCLK, RXDV, RXER, COL and CRS. Seven signals are used to transmit data from the MAC: TXD<3:0>, TXCLK, TXEN, and TXER.

The LXT973 supplies both clock signals as well as separate outputs for carrier sense and collision. Data transmission across the MII is normally implemented in 4-bit-wide nibbles.

3.3.1 MII Clocks

The LXT973 is the master clock source for data transmission and supplies both MII clocks (RXCLK and TXCLK). It automatically sets the clock speeds to match link conditions. When the link is operating at 100 Mbps, the clocks are set to 25 MHz. When the link is operating at 10 Mbps, the clocks are set to 2.5 MHz. The transmit data and control signals must always be synchronized to TXCLK by the MAC. The LXT973 samples these signals on the rising edge of TXCLK.

3.3.2 Transmit Enable

The MAC must assert TXEN at the same time as the first nibble of preamble, and de-assert TXEN after the last bit of the packet.

3.3.3 Receive Data Valid

The LXT973 asserts RXDV when it receives a valid packet. Timing changes depend on line operating speed:

- For 100BASE-TX links, RXDV is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BASE-T links, the entire preamble is truncated. RXDV is asserted with the first nibble of the Start-of-Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.

3.3.4 Carrier Sense

Carrier Sense (CRS) is an asynchronous output. CRS is generated when a packet is received from the line regardless of duplex mode, and for a transmission to the line in half-duplex mode. Table 8 on page 26 summarizes the conditions for assertion of carrier sense, collision, and data loopback signals. Carrier sense is not generated when a packet is transmitted in full-duplex mode.

For 100BASE-TX and 100BASE-FX links, a Start-of-Stream Delimiter (SSD) or /J/K/ symbol pair causes assertion of carrier sense (CRS). An End-of-Stream Delimiter (ESD), or /T/R/ symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R/. In this event, the RXER bit in the RX Status Frame is asserted for one clock cycle when CRS is de-asserted.

For 10BASE-T links, CRS assertion is based on receipt of a valid preamble, and de-assertion is based on receipt of an End-of-Frame (EOF) marker.

3.3.5 Error Signals

When the LXT973 is in 100 Mbps mode and receives an invalid symbol from the network, it asserts RXER and drives “1110” on the RXD pins.

When the MAC asserts TXER, the LXT973 drives “H” symbols out on the DPAP/N_0 or DPAP/N_1 pins.

3.3.6 Collision

The LXT973 asserts its collision signal, asynchronously to any clock, when the line state is half-duplex and the transmitter and receiver are active at the same time. Table 8 on page 26 summarizes the conditions for assertion of carrier sense, collision, and data loopback signals.

3.3.7 Loopback

The LXT973 provides two loopback functions, operational and test (see Table 8 on page 26). Loopback paths are shown in Figure 4 on page 26.

3.3.7.1 Operational Loopback

Operational loopback is provided for 10 Mbps half-duplex links when Register bit 16.8 = 0. Data transmitted by the MAC (TXD) is looped back on the receive side of the MII (RXD). Operational loopback is not provided for 100 Mbps links, full-duplex links, or when Register bit 16.8 = 1.

3.3.7.2 Test Loopback

A test loopback function is provided for diagnostic testing of the LXT973. During test loopback, twisted-pair and fiber interfaces are disabled. Data transmitted by the MAC is internally looped back by the LXT973 and returned to the MAC.

Test loopback is available for both 100BASE-TX and 10BASE-T operation. Test loopback is enabled by setting the register bits as follows:

- Register bit 0.14 = 1 (loopback mode)

- Register bit 0.8 = 1 (full-duplex)
- Register bit 0.12 = 0 (disable auto-negotiation).

Figure 4. Loopback Paths

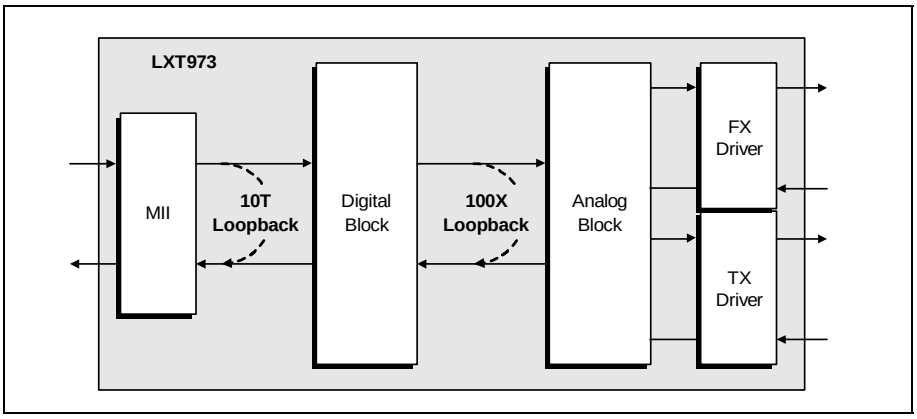


Table 8. Carrier Sense, Loopback, and Collision Conditions

Speed	Duplex Condition	Carrier Sense	Test[1] Loopback	Operational Loopback	Collision
100 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Full-Duplex	Receive Only	No	No	None
	Half-Duplex	Transmit or Receive	No	No	Transmit and Receive
10 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Full-Duplex	Receive Only	No	No	None
	Half-Duplex, Register bit 16.8 = 0	Transmit or Receive	Yes	Yes	Transmit and Receive
	Half-Duplex, Register bit 16.8 = 1	Transmit or Receive	No	No	Transmit and Receive

1. Test Loopback is enabled when Register bits 0.14 = 1, 0.8 = 1, and 0.12 = 0.

3.3.8 Configuration Management Interface

The LXT973 provides an MDIO Management Interface and a Hardware Control Interface for device configuration and management.

3.3.8.1 MII Management Interface

The LXT973 supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT973. The MDIO interface consists of a physical connection, a specific protocol which runs across the connection, and an internal set of addressable registers. The physical interface consists of a data line (MDIO) and clock line (MDC), and a control line (MDDIS). The maximum speed of MDC is 20 MHz.

Operation of this interface is controlled by the MDDIS*n* input pin. When MDDIS*n* is High, the MDIO is completely disabled. When MDDIS*n* is Low, read and write are enabled. The timing for the MDIO Interface is shown in Table 49 on page 85. See Figure 5 for read operations, and Figure 6 for write operations. The protocol allows one controller to communicate with multiple LXT973 devices. Each LXT973 port is assigned an address between 0 and 31, as described in Table 5 on page 19 (ADDR<4:1>).

The LXT973 supports the core 16-bit MDIO registers. Registers 0-10 and 15 are required and their functions are specified by the IEEE 802.3 specification. Additional registers are included for expanded functionality. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15)

Figure 5. Management Interface Read Frame Structure

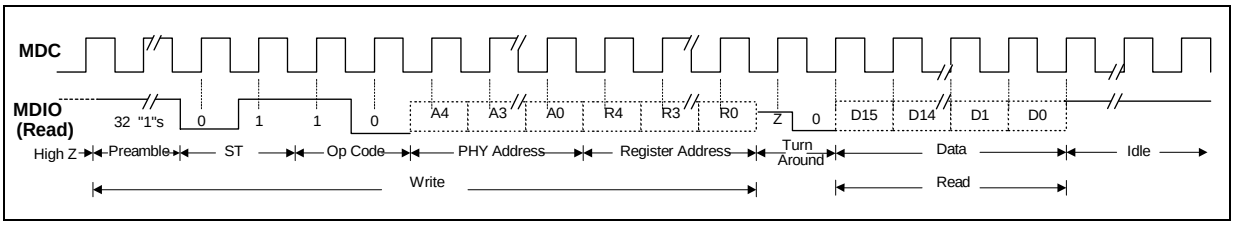
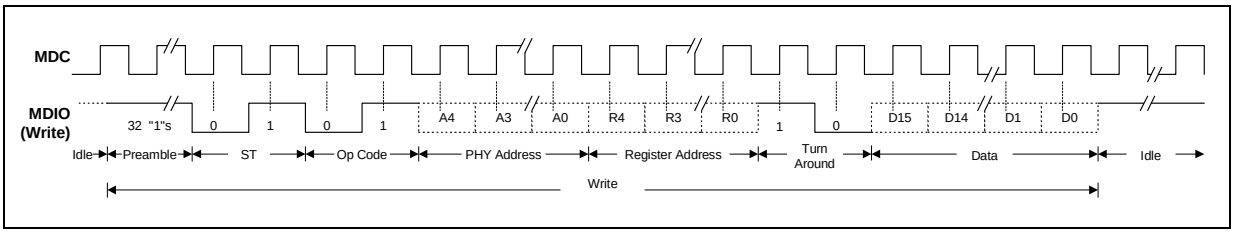


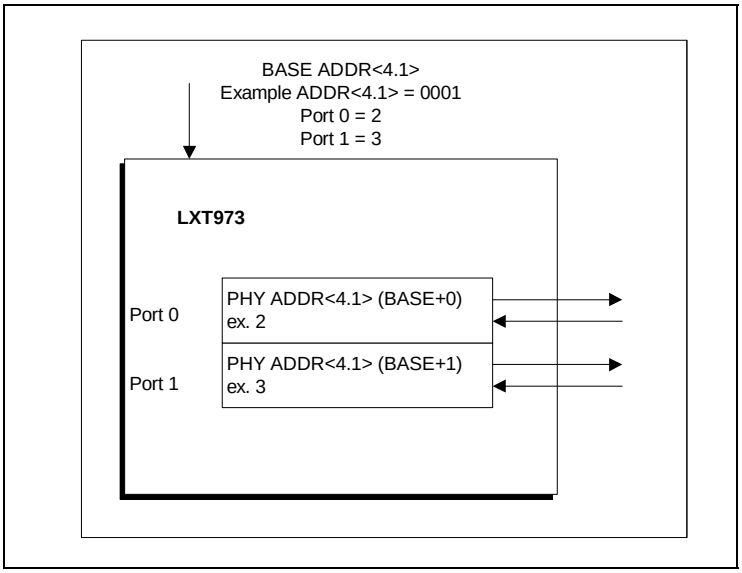
Figure 6. Management Interface Write Frame Structure



3.3.8.2 MII Addressing

The MDIO management protocol allows one controller to communicate with multiple LXT973 chips. Pins ADDR_<4:1> determine the base address. Each port adds its port number to the base address to obtain its port address as shown in Figure 7 on page 28.

Figure 7. Port Address Scheme



3.3.8.3 Hardware Control Interface

The LXT973 provides a Hardware Control Interface for applications where the MDIO is not desired. Refer to Figure 16, “LXT973 Initialization Sequence” on page 47 for additional details.

3.4 Operating Requirements

3.4.1 Power Requirements

The LXT973 requires five power supply inputs: VCCD, VCCR, VCCT, VCCPECL, and VCCIO. The digital and analog circuits require 2.5V supplies (VCCD, VCCR, and VCCT). These inputs may be supplied from a single source although decoupling is required to each respective ground. The fiber VCCPECL supply can be connected to either 2.5V or 3.3V.

A separate power supply may be used for MII and MDIO (VCCIO) interfaces. The power supply may be either +2.5V or +3.3V. VCCIO should be supplied from the same power source used to supply the controller on the other side of the interface. As a matter of good practice, these supplies should be as clean as possible.

3.4.2 Clock Requirements

3.4.2.1 Reference Clock / External Oscillator

The LXT973 requires a constant enabled reference clock (REFCLK). REFCLK’s frequency must be 25 MHz. Considering overall system performance first, the clock is best derived by providing a crystal-based oscillator. PLL-based oscillators with known stability may also be used. In general, an oscillator-based clock source is recommended over a derived clock due to frequency stability

and overall signal integrity. Regardless of clock source, careful consideration should be given to physical placement, board layout, and signal routing of the source to maintain the highest possible level of signal integrity. Refer to Table 33 on page 74 for clock timing requirements.

3.4.2.2 MDIO Clock

The MII management channel (MDIO) also requires an external clock. The managed data clock (MDC) speed is a maximum of 20 MHz. Refer to Table 49 on page 85 for details.

3.5 Initialization

When the LXT973 is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link. The configuration bits may be set by the Hardware Control or MDIO interface as shown in Table 9 on page 31.

3.5.1 MDIO Control Mode

In the MDIO Control mode, the LXT973 reads the Hardware Control Interface pins to set the initial (default) values of the MDIO registers. Once the initial values are set, bit control reverts to the MDIO interface.

3.5.2 Hardware Control Mode

In the Hardware Control Mode, the LXT973 disables direct write operations to the MDIO registers via the MDIO Interface. On power-up or hardware reset the LXT973 reads the Hardware Control Interface pins and sets the MDIO registers accordingly.

The following modes are available using either Hardware Control or MDIO Control:

- Forced network link to 100BASE-FX (Fiber)
- Forced network link operation to:
  100BASE-TX, full-duplex
  100BASE-TX, half-duplex
  10BASE-T, full-duplex
  10BASE-T, half-duplex
- Allow auto-negotiation/parallel-detection

When the network link is forced to a specific configuration, the LXT973 immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT973 begins the auto-negotiation/parallel-detection operation.

3.5.3 Power-Down Mode

The LXT973 incorporates numerous features to maintain the lowest power possible. The device can be put into a low-power state via Register 0 as well as a near-zero power state with the power-down pin. When in power-down mode, the device is not capable of receiving or transmitting packets.

The lowest power operation is achieved using the global power-down pin. This active High pin powers down every circuit in the device, including all clocks. All registers are unaltered and maintained when the global PWRDWN pin is released and the registers are reloaded with the value of the last hardware reset.

Individual ports (software power-down) can be powered down using Control Register bit 0.11. This bit powers down a significant portion of the port, but clocks to the register section remain active. This allows the management interface to remain active during register power-down. The power-down bit is active High.

3.5.3.1 Hardware Power-Down

The hardware power-down per port mode is controlled by the PWRDWN 0/1 pins. When PWRDWN 0/1 is High, the following conditions are true:

- All LXT973 ports and the clock are shut down.
- All outputs are tri-stated.
- The MDIO registers are not accessible.
- Configuration pins are not read upon release of the PWRDWN 0/1 pins, and registers are reloaded with the value of the last hardware reset.

3.5.3.2 Software Power-Down

Software port power-down control is provided by Register 11 in the respective port Control Registers (refer to Table 17 on page 62). During individual port power-down, the following conditions are true:

- The individual port is shut down.
- The MDIO registers remain accessible.
- The register remains unchanged.

3.5.4 Reset

The LXT973 provides both hardware and software resets. Configuration control of auto-negotiation, speed, and duplex mode selection is handled differently for each. During a hardware reset, settings for Register bits 0.13, 0.12, and 0.8 are read in from the pins (refer to Table 9 on page 31 for pin settings and Table 17 on page 62 for register bit definitions).

During a software reset (Register bit 0.15 = 1), the bit settings are not re-read from the pins, and revert back to the values that were read in during the last hardware reset. Any changes to pin values from the last hardware reset are not detected during a software reset. Also, during a software reset (Register bit 0.15 = 1), the registers are available for reading. The reset bit is polled to see when the part has completed reset (Register bit 0.15 = 0).

During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. All the MII interface pins are disabled during a hardware reset and released to the bus on de-assertion of reset.

3.5.5 Hardware Configuration Settings

The LXT973 provides a hardware option to set the initial device configuration. The hardware option uses four per-port configuration pins that provide control (see Table 9 on page 31).

Table 9. Configuration Settings (Hardware Control Interface)

FIBER/TP*x*	AUTO-NEG*x*	SPEED*x*	DUPLEX*x*	Mode
Low	-	-	Low	100BASE-FX is enabled in half-duplex mode. Auto-negotiation is disabled.
Low	-	-	High	100BASE-FX is enabled in full-duplex mode. Auto-negotiation is disabled.
High	High	High	High	AUTO_NEG is enabled. All capabilities are advertised. Register bits 4.8, 4.7, 4.6, and 4.5 are all set to 1.
High	High	High	Low	AUTO_NEG is enabled. Only 100 Mbps capabilities are advertised. Register bits 4.8 and 4.7 are set 1. Register bits 4.6 and 4.5 are cleared to 0.
High	High	Low	High	AUTO_NEG is enabled. Only 10 Mbps capability is advertised. Register bits 4.8 and 4.7 are cleared to 0. Register bits 4.6 and 4.5 are set to 1.
High	High	Low	Low	AUTO_NEG is enabled. Only half -duplex capability is advertised. Register bits 4.7 and 4.5 are set 1. Register bits 4.8 and 4.6 are cleared to 0.
High	Low	High	High	AUTO_NEG is disabled. LXT973 port x is forced to 100 Mbps full-duplex operation.
High	Low	High	Low	AUTO_NEG is disabled. LXT973 port x is forced to 100 Mbps half-duplex operation.
High	Low	Low	High	AUTO_NEG is disabled. LXT973 port x is forced to 10 Mbps full-duplex operation.
High	Low	Low	Low	AUTO_NEG is disabled. LXT973 port x is forced to 10 Mbps half-duplex operation.
1. These pins also set the default values for Registers 0 and 4 accordingly.				

3.6 Link Establishment

3.6.1 Auto-Negotiation

The LXT973 attempts to auto-negotiate with its link partner by sending Fast Link Pulse (FLP) bursts. Each burst consists of 33 pulse positions spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may also be present or absent to indicate a “1” or a “0”. Each FLP burst exchanges 16 bits of data, referred to as a “page.” All devices that support auto-negotiation must implement the “Base Page”, defined by IEEE 802.3 (Registers 4 and 5). The LXT973 also supports the optional “Next Page” function (Registers 7 and 8).

3.6.1.1 Base Page Exchange

By exchanging Base Pages, the LXT973 and its link partner communicate their capabilities to each other. Both sides must receive at least three identical base pages for negotiation to proceed. Each side finds their highest common capabilities, exchange more pages, and agree on the operating state of the line.

3.6.1.2 Next Page Exchange

Additional information, exceeding that required by Base Page exchange, can also be sent via “Next Pages.” The LXT973 fully supports the IEEE 802.3 method of negotiation via Next Page exchange. The Next Page exchange uses Register 7 to send information and Register 8 to receive information, and occurs only if both ends of the link advertise their ability to exchange Next Pages. The LXT973 is configured to make Next Page exchange easier for software. When a Base Page or Next Page is received, the Page Received Register bit 6.1 remains set until read. When Register bit 6.2 (Next Page Able) is received, it stays set until read. This bit should be cleared whenever a new negotiation occurs. This prevents the user from reading an old value in Register 6 and assuming there is valid information in Registers 5 and 8. Additionally, Register 6 contains a new bit (Register bit 6.5) that indicates when the current Received Page is the Base Page. This information is useful for recognizing when next pages must be re-sent due to the start of a new negotiation process. Register bit 16.1 and the Page Received bit (Register bit 6.1) are also cleared upon reading Register 6.

3.6.1.3 Controlling Auto-Negotiation

When auto-negotiation is controlled by software, the following steps are recommended:

1. After power-up, power-down, or reset, the power-down recovery time (max = 300 µs) must be exhausted before proceeding.
2. Set the auto-negotiation advertisement register bits.
3. Enable auto-negotiation (set MDIO Register bit 0.12 = 1).

3.6.1.4 Link Criteria

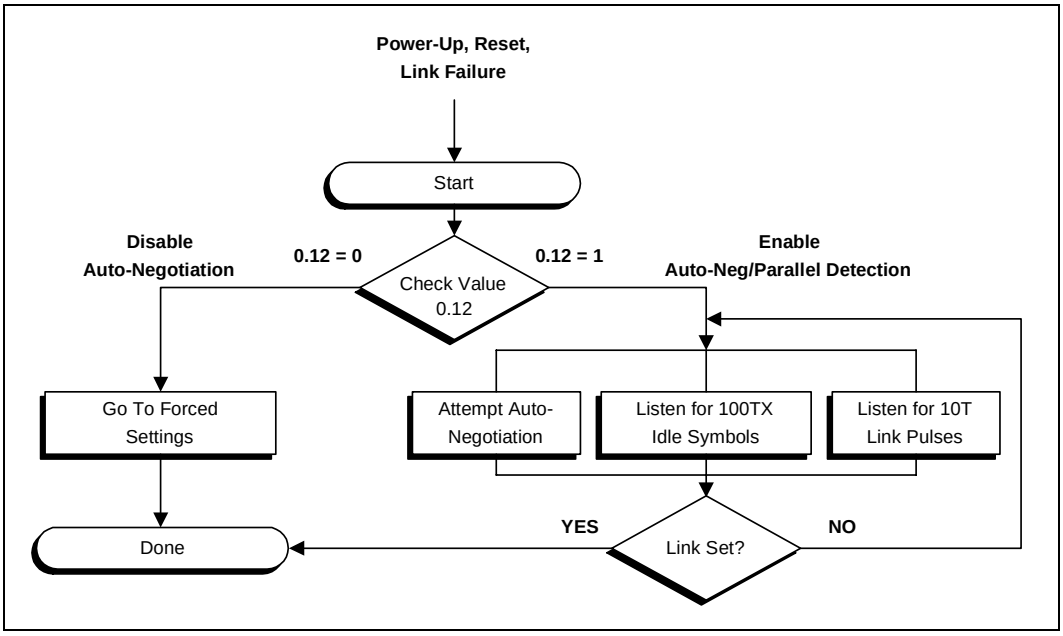
In 100 Mbps mode, link is established when the scrambler becomes locked and remains locked for approximately 50 ms. Link remains up unless the de-scrambler receives less than 12 consecutive IDLE symbols in any 2 ms period. This provides a very robust operation, filtering out any small noise hits that may disrupt the link.

In 10 Mbps mode, link is established based on the link state machine found in the IEEE 802.3, Clause 14.X specification. Receiving 100 Mbps idle patterns does not bring up a 10 Mbps link.

3.6.1.5 Parallel Detection

In parallel with auto-negotiation, the LXT973 also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps IDLE symbols. If either is detected, the device automatically reverts to the corresponding operating mode. Parallel detection allows the LXT973 to communicate with devices that do not support auto-negotiation. The established link is always set at half-duplex.

Figure 8. Auto-Negotiation Operation



3.7 Network Media/Protocol Support

The LXT973 supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX).

3.7.1 10/100 Mbps Network Interface

The network interface port consists of five external pins (two differential signal pairs and a signal detect pin). The differential signal pins are shared between twisted-pair and fiber. Refer to Figure 3 on page 23 for specific pin assignments.

The LXT973 output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the LXT973 generates IEEE 802.3-compliant link pulses or an IDLE code. Input signals are decoded either as a 100BASE-TX, 100BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

3.7.2 Twisted-Pair Interface

When operating at 100 Mbps, the LXT973 continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT973 generates IDLE symbols.

During 10 Mbps operation, Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state. Link pulses are transmitted periodically to keep the link up.

The LXT973 supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted-Pair (UTP) cable. Only a transformer, RJ-45 connector, and bypass capacitors are required to complete this interface. On the transmit side, Intel's patented waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings (refer to Table 5 on page 19) allow the designer to match the output waveform to the magnetic characteristics.

3.7.3 Fiber Interface

The LXT973 fiber port is designed to interface with common industry-standard fiber modules. It incorporates a PECL interface that complies with the ANSI X3.166 standard for seamless integration.

Fiber mode is selected by putting a low level on the Fiber_TP*n* pin. This is only sensed upon completion of reset.

3.7.4 Fault Detection and Reporting

The LXT973 supports two fault detection and reporting mechanisms. "Remote Fault" refers to a MAC-to-MAC communication function that is essentially transparent to PHY layer devices, and is used only during auto-negotiation. Therefore, Remote Fault is applicable only to twisted-pair links. "Far End Fault" is an optional PMA-layer function that may be embedded within PHY devices. The LXT973 supports both functions, which are explained in more detail in sections that follow.

3.7.5 Remote Fault

Register bit 4.13 in the Auto-Negotiation Advertisement Register is reserved for Remote Fault indications. This bit is typically used when restarting the auto-negotiation sequence, indicating to the link partner that link is down because the advertising device detected a fault.

When the LXT973 receives a Remote Fault indication from its partner during auto-negotiation it:

- Sets Register bit 5.13 in the Link Partner Base Page Ability Register, and
- Sets the Remote Fault Register bit 1.4 in the MII Status Register to pass this information to the local controller.

3.7.6 Far End Fault

In fiber mode, the SD*n* pin monitors signal quality. If signal quality degrades beyond the fault threshold, the fiber transceiver reports a signal quality fault condition via the SD*n* pin. Loss of signal quality blocks any fiber data from being received and causes a loss of link.

If the LXT973 detects a signal fault condition, it transmits the Far End Fault Indication (FEFI) over the fiber link. The FEFI consists of 84 consecutive “1s” followed by a single “0.” This pattern must be repeated at least three times. The LXT973 transmits the Far-End Fault code a minimum of three times if all the following conditions are true:

- Fiber mode is selected.
- Far End Fault Code transmission is enabled (Register bit 16.2 = 1).
- Signal Detect indicates either no signal or the receive PLL cannot lock.
- Loopback is not enabled.

3.8 100 Mbps Operation

3.8.1 100BASE-X Network Operations

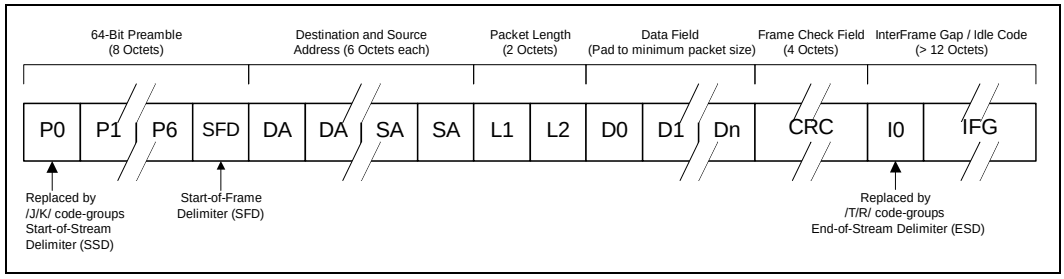
During 100BASE-X operation, the LXT973 transmits and receives 5-bit symbols across the network link. Figure 9 shows the structure of a standard frame packet. When the MAC is not actively transmitting data, the LXT973 sends out IDLE symbols on the line.

In 100BASE-TX mode, the device scrambles the data and transmits it to the network using MLT-3 line code. The MLT-3 signals received from the network are de-scrambled and decoded, and sent across the MII to the MAC.

In 100BASE-FX mode, the LXT973 transmits and receives NRZI signals across the PECL interface. An external 100BASE-FX transceiver module is required to complete the fiber connection.

As shown in Figure 9, the MAC starts each transmission with a preamble pattern. As soon as the LXT973 detects the start of preamble, it transmits a J/K Start-of-Stream Delimiter (SSD) symbol to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the Start-of-Frame Delimiter (SFD), packet data, and CRC. Once the packet ends, the LXT973 transmits the T/R End-of-Stream Delimiter (ESD) symbol and returns to transmitting IDLE symbols.

Figure 9. 100BASE-X Frame Format



3.8.2 100BASE-X Protocol Sublayer Operations

In the 7-layer OSI communications model, the LXT973 is a Physical Layer 1 (PHY) device. The LXT973 implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers of the reference model defined by the IEEE 802.3u specification. The following paragraphs discuss the LXT973 operation from the reference model point of view.

3.8.3 PCS Sublayer

The Physical Coding Sublayer (PCS) provides the MII interface, as well as the 4B/5B encoding/decoding function. For 100BASE-TX and 100BASE-FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TXEN is de-asserted. For 10BASE-T operation, the PCS layer merely provides a bus interface and serialization/de-serialization function. 10BASE-T operation does not use the 4B/5B encoder.

3.8.3.1 Preamble Handling

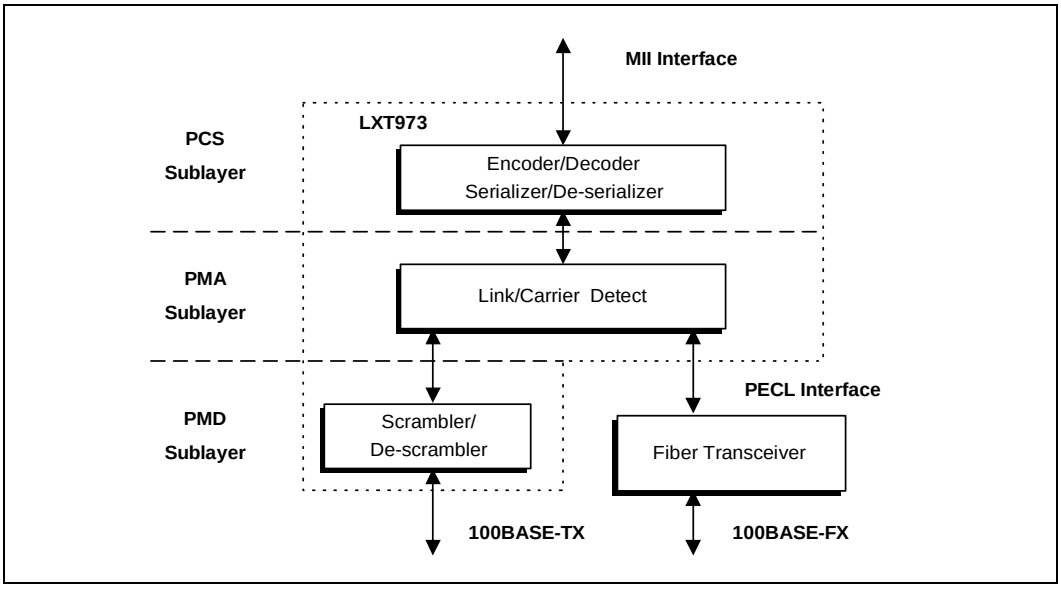
When the MAC asserts TXEN, the PCS substitutes a /J/K/ symbol pair, also known as the Start-of-Stream Delimiter (SSD), for the first two nibbles received across the MII. The PCS layer continues to encode the remaining MII data until TXEN is de-asserted. It then returns to supplying IDLE symbols to the line driver.

The PCS layer performs the opposite function in the receive direction by substituting two preamble nibbles for the SSD.

3.8.3.2 Dribble Bits

The LXT973 handles dribble bits in all modes. If one through four dribble bits are received, the nibble is passed across the MII, and padded with ones if necessary. If five through seven dribble bits are received, the second nibble is not sent to the MII bus.

Figure 10. Protocol Sublayers



3.8.4 PMA Sublayer

3.8.4.1 Link Failure Override

The LXT973 normally transmits 100 Mbps data packets or IDLE symbols only if it detects that link is up, and transmits FLP bursts in auto-negotiation mode or IDLE symbols in forced mode. Setting Register bit 16.14 = 1 overrides this function, allowing the LXT973 to transmit data packets even when link is down. This feature is provided as a diagnostic tool.

Note: Auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT973 automatically begins transmitting FLP bursts if the link goes down.

3.8.4.2 Carrier Sense

For 100BASE-TX and 100BASE-FX links, a Start-of-Stream Delimiter (SSD) or /J/K/ symbol pair causes assertion of carrier sense (CRS). An End-of-Stream Delimiter (ESD), or /T/R/ symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R/. In this event, the RXER bit in the RX Status Frame is asserted for one clock cycle when CRS is de-asserted.

3.8.4.3 Twisted-Pair PMD Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides the signal scrambling and descrambling, line coding and decoding (MLT-3), as well as receiving, polarity correction, and baseline wander correction functions.

3.8.4.4 Scrambler/Descrambler

The purpose of the scrambler is to spread the signal power spectrum and further reduce EMI using an 11-bit, non-data-dependent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

The scrambler/de scrambler can be bypassed by setting Register bit 16.12 = 1. The scrambler is automatically bypassed when the fiber port is enabled. Scrambler bypass is provided for diagnostic and test support.

3.8.4.5 Baseline Wander Correction

The LXT973 provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is, by definition, “unbalanced.” This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander may cause receiver errors, particularly in less robust designs, at long-line lengths (100 meters). The exact characteristics of the wander are completely data dependent.

The LXT973 baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case “killer” packets over all cable lengths.

3.8.5 Fiber PMD Sublayer

The LXT973 provides a PECL interface for connection to an external fiber-optic transceiver. (The external transceiver provides the PMD function for fiber media.) The device uses an NRZI format for the fiber interface. The fiber interface operates at 100 Mbps only and does not support 10 Mbps applications.

3.8.5.1 Far End Fault Indications

The LXT973 Signal Detect pins independently detect signal faults from the local fiber transceivers via the SD pins. The device also uses Register bit 1.4 to report Remote Fault indications received from its link partner. The device ORs both fault conditions to set Register bit 1.4. This bit is set once and cleared when read.

Either fault condition causes the LXT973 to drop the link unless Forced Link Pass is selected (Register bit 16.14 = 1). A link-down condition is then reported via status bits.

In response to locally detected signal faults (SD activated by the local fiber transceiver), the affected port can transmit the Far End Fault code if a fault code transmission is enabled by Register bit 16.2.

- When Register bit 16.2 = 1, transmission of the Far End Fault code is enabled. The LXT973 transmits Far End Fault code if fault conditions are detected by the Signal Detect pins.
- When Register bit 16.2 = 0, the LXT973 does not transmit Far End Fault code. It continues to transmit IDLE code and may or may not drop link, depending on the setting for Register bit 16.14.

The occurrence of a Far End Fault causes all transmission of data from the Reconciliation Sublayer to stop and the Far End fault code to begin. The Far End Fault code consists of 84 “1s” followed by a single “0”, and is repeated until the Far End Fault condition is removed.

3.9 10 Mbps Operation

The LXT973 operates as a standard 10BASE-T transceiver and supports all the standard 10 Mbps functions. During 10BASE-T operation, the LXT973 transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the device sends out link pulses on the line.

In 10BASE-T mode, the polynomial scrambler/de-scrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT973 and sent across the MII to the MAC.

3.9.1 Polarity Correction

The LXT973 automatically detects and corrects for an inverted receive signal. Reversed polarity is detected if eight inverted link pulses or four inverted End-of-Frame (EOF) markers are received consecutively. If link pulses or data are not received by the maximum receive time-out period, the polarity state is reset to a non-inverted state.

Note: The LXT973 does not support fiber connections at 10 Mbps.

3.9.2 Dribble Bits

The LXT973 device handles dribble bits in all modes. If one through four dribble bits are received, the nibble is passed across the MII. If five through seven dribble bits are received, the second nibble is not sent to the MII bus.

3.9.3 Link Test

The LXT973 always transmits link pulses in 10BASE-T mode. When enabled, the link test function monitors the connection for link pulses. Once link pulses are detected, data transmission is enabled and remains enabled as long as either the link pulses or data transmission continues. If link pulses stop, the data transmission is disabled.

If the link test function is disabled, the LXT973 transmits to the connection regardless of detected link pulses. The link test function is disabled by setting Register bit 16.14 = 1.

3.9.4 Link Failure

Link failure occurs if Link Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT973 returns to the auto-negotiation phase if auto-negotiation is enabled.

3.9.5 Jabber

If a transmission exceeds the jabber timer, the LXT973 disables the transmit and loopback functions. The LXT973 automatically exits jabber mode after the unjab time has expired. This function is disabled by setting Register bit 16.10 = 1.

3.10 Monitoring Operations

3.10.1 Monitoring Auto-Negotiation

Auto-negotiation may be monitored as follows:

- Link Status Register bit 1.2 = 1 once the link is established.
- Additional bits in Register 1 can be used to determine the link operating conditions and status (refer to Table 18 on page 63).

3.10.2 Per-Port LED Driver Functions

The LXT973 incorporates three direct drive LEDs per port (LED*n*_1, LED*n*_2, and LED*n*_3). On power-up, all the LEDs light up for approximately one second after reset de-asserts. Each LED may be configured to one of several different display modes using the LED Configuration Pins, as shown in Table 10 on page 40.

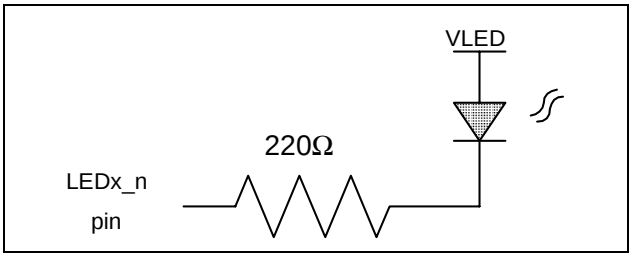
The LED driver pins are open drain circuits (10 mA maximum current rating). If an LEDx_*n* pin is unused, terminate with a 10KΩ pull-up resistor. Figure 11 shows a typical LED implementation. When configured for modes 2 or 4, the LEDs blink at the rate of 100 ms to display multiple status.

Table 10 provides LED configurations for the LXT973.

Table 10. LED Configurations

LED_CFG0	LED_CFG1	LEDn_1	LEDn_2	LEDn_3
0	0	Speed	Link	Duplex
1	0	Speed	Link/Activity	Duplex/Collision
0	1	Link	Receive	Transmit
1	1	Speed	Link/MII Isolate	Duplex/Collision

Figure 11. Typical LED Implementation



4.0 Application Information

4.1 Design Recommendations

The LXT973 is designed to comply with IEEE 802.3 requirements to provide outstanding receive Bit Error Rate (BER), and long-line-length performance. To achieve maximum performance from the LXT973, attention to detail and good design practices are required. *Refer to the LXT973 Design and Layout Guide for detailed design and layout information.*

4.1.1 General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to a maximum noise level of 50 mV is considered acceptable. High-frequency switching noise can be reduced, and its effects eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and de-coupling capacitors throughout the design (a value of 0.01 µF is recommended for de-coupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-to-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT973 and the RJ-45 connectors at the edge of the board.
- Do not extend any circuit power and ground planes past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

4.1.2 Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane may cause EMI problems and degrade line performance. To minimize ground noise as much as possible, use good general techniques and filter the VCC plane. It is difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having problems:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (32-bits+) running at a high clock rate.
- DC-to-DC converters.

Intel recommends filtering the power supply to the analog VCC pins of the LXT973. This has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT973, helping with line performance. Second, if the VCC planes are laid out correctly, digital switching noise is kept away from external connectors, reducing EMI problems.

The recommended implementation is to break the VCC plane into two sections. The digital section supplies power to the VCCD and VCCIO pins of the LXT973. The analog section supplies power to the VCCR, VCCT, VCCPECL pins. The break between the two planes should run underneath the device. In designs with more than one LXT973 device, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. Beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. A bulk cap (2.2 -10 µF) should be placed on each side of each bead. In addition, a high-frequency bypass cap (0.01 µF) should be placed near each analog VCC pin.

4.1.3 Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes.

- Follow the guidelines in the *LXT973 Design and Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the DPAP/N_*n* and DPBP/N_*n* signals, the magnetics, and the RJ-45 connectors.
- Place the layers so that the DPAP/N_*n* and DPBP/N_*n* signals can be routed near or next to the ground plane.

4.1.3.1 Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ-45 connectors to the magnetics, and can be used to terminate unused signal pairs (Bob Smith termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2 kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2 kV isolation to the Bob Smith termination.

4.1.4 MII Terminations

Series termination resistors are required on all the output signals driven by the LXT973. Keep all traces orthogonal and as short as possible. Whenever possible, route the clock traces evenly between the longest and shortest data routes. This minimizes round-trip, clock-to-data delays and allows a larger margin to the setup and hold requirements. Please refer to the *LXT973 Design and Layout Guide* for series resistor values.

4.1.5 The Fiber Interface

The fiber interface consists of a PECL transmit and receive pair to an external fiber-optic transceiver. The transmit and receive pair should be DC-coupled to the transceiver, and biased appropriately. Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 14 on page 46 shows a typical example.

4.1.6 Twisted-Pair Interface

Use the following standard guidelines for a twisted-pair interface:

- Place the magnetics as close as possible to the LXT973.
- Keep transmit pair traces as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- Route the transmit pair adjacent to a ground plane. The optimum arrangement is to place the transmit traces two to three layers from the ground plane with no intervening signals.
- Improve EMI performance by filtering the TPO center tap. A single ferrite bead rated at 100 mA may be used to supply center tap current to all ports.

4.1.6.1 Magnetics Information

The LXT973 requires a 1:1 ratio for the receive transformers and a 1:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 11 for transformer requirements. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and validate the magnetics for the specific application.

Table 11. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1:1	–	–	–
Tx turns ratio	–	1:1	–	–	–
Insertion loss	0.0	0.6	1.1	dB	–
Primary inductance	350	–	–	µH	–
Transformer isolation	2	–	–	kV	–
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

4.2 Typical Application Circuits

Figure 12 through Figure 15 on page 46 show typical application circuits for the LXT973.

Figure 12. Power and Ground Supply Connections

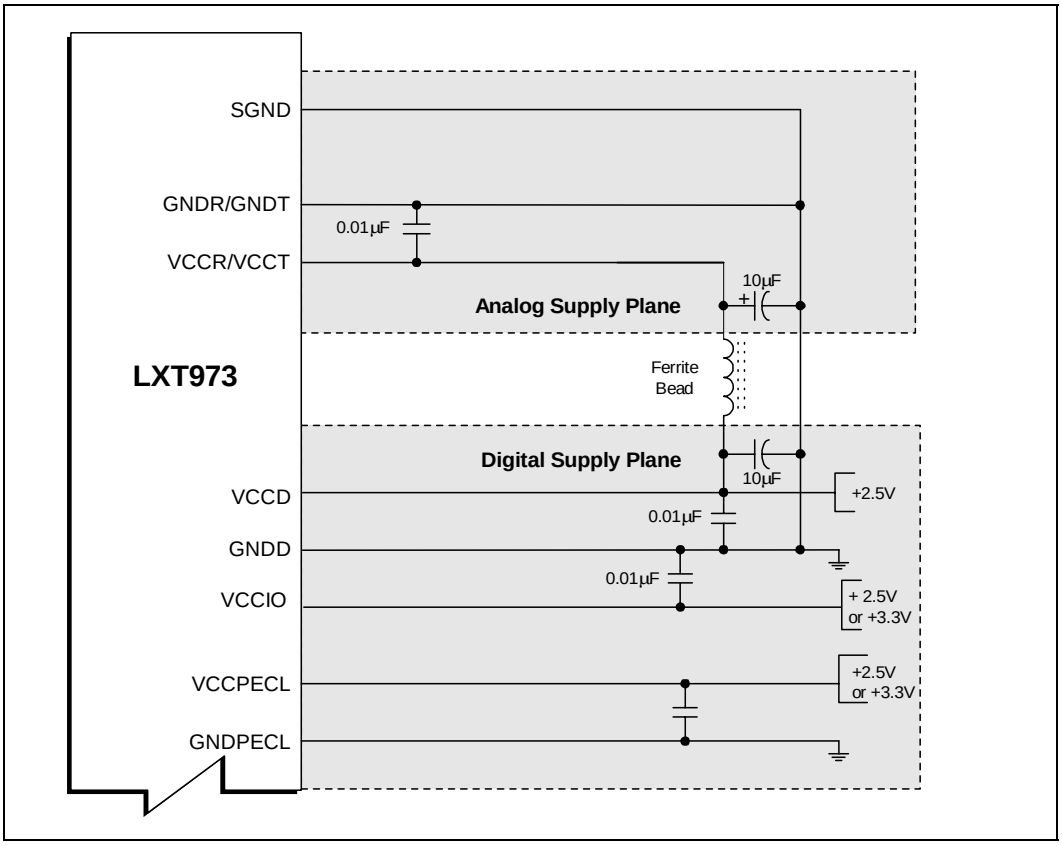
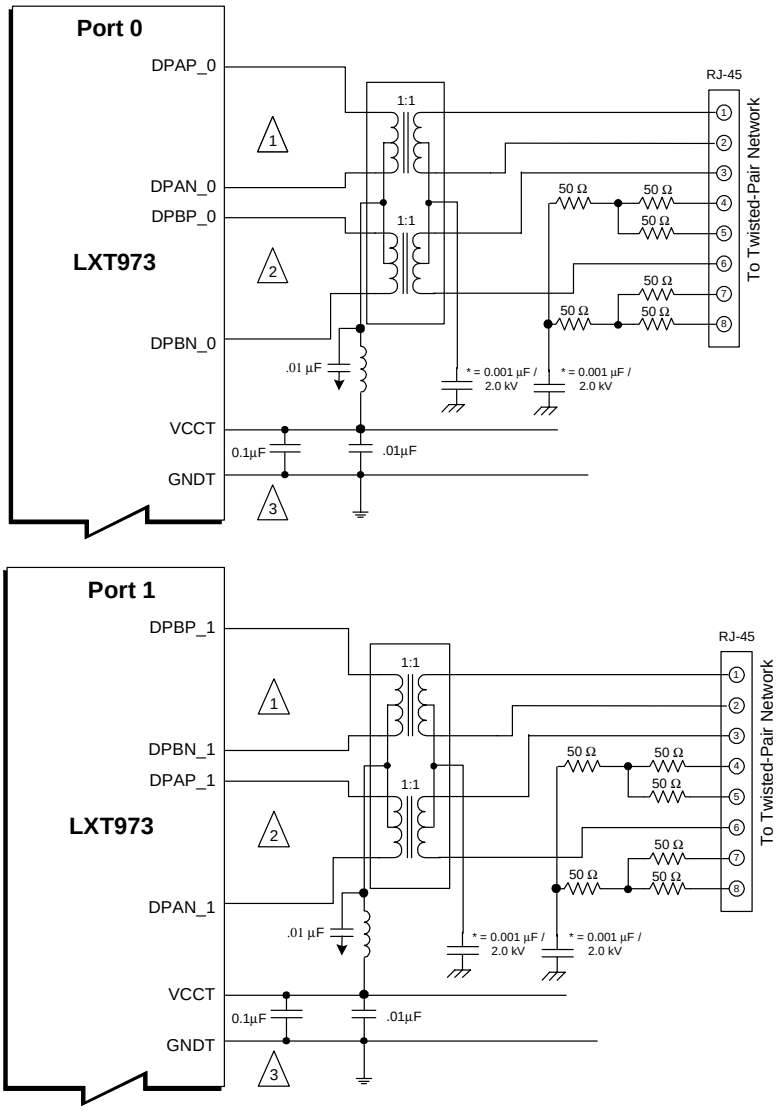
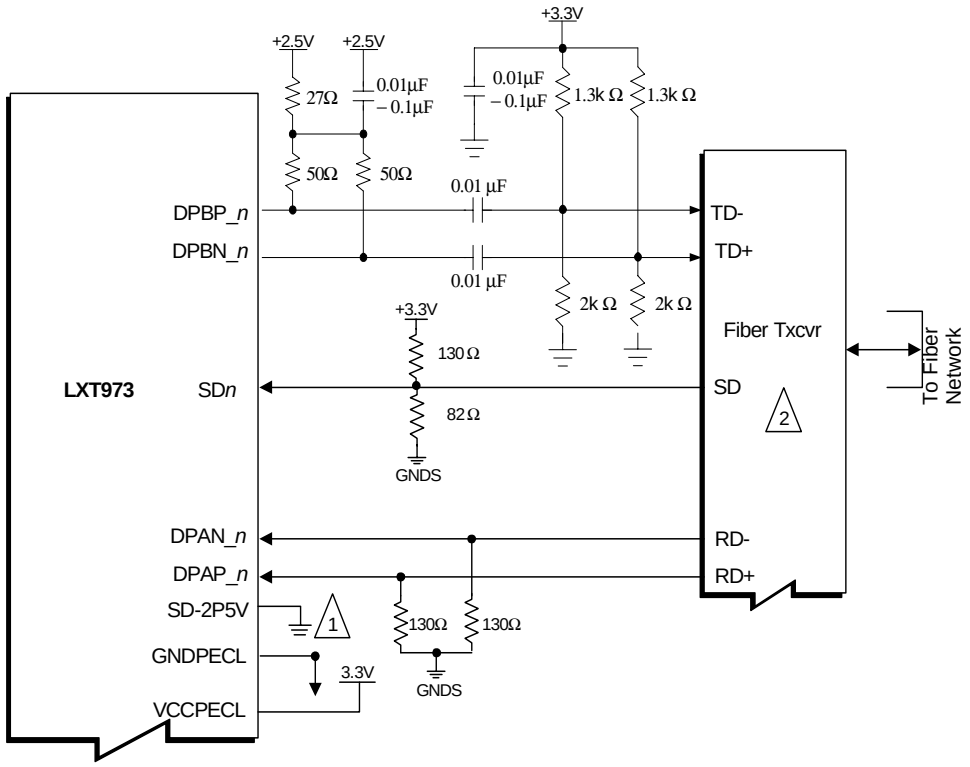


Figure 13. Typical Twisted-Pair Interface



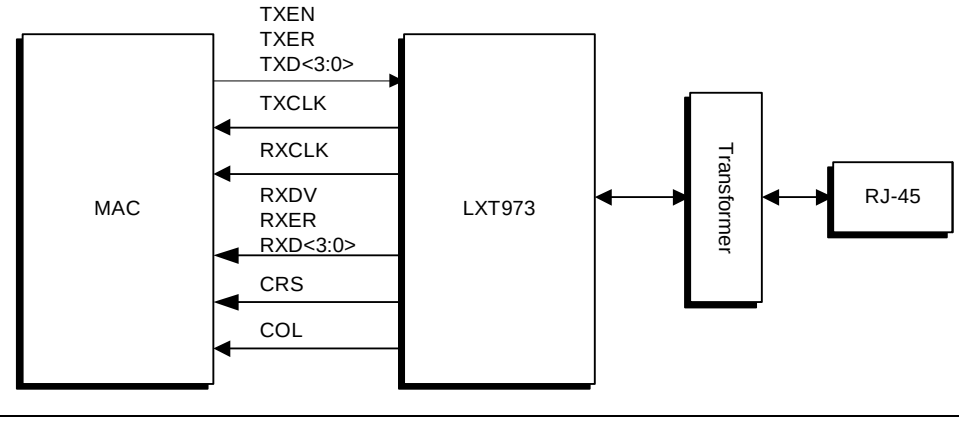
1. The 100Ω transmit load termination resistor typically required is integrated in the LXT973.
2. The 100Ω receive load termination resistor typically required is integrated in the LXT973.
3. Recommended 0.1 µF capacitor to improve EMI performance.

Figure 14. Typical Fiber Interface



1. This pin selects between 2.5V and 3.3V fiber transceivers. The figure shows the connection for a 3.3V fiber transceiver.
2. Refer to the transceiver manufacturers' recommendations for termination circuitry.

Figure 15. Typical MII Interface



4.3 Initialization

At power-up or reset, the LXT973 performs the initialization as shown in Figure 16 on page 47. When the MDDIS*n* pin is High, the LXT973 enters Manual Control Mode for that port. When MDDIS*n* is Low, MDIO Control Mode is enabled for that port. Mode control selection is provided via the MDDIS*n* pin as shown in Table 12 on page 48.

4.4 MDIO Control Mode

In the MDIO Control mode, the LXT973 uses the Hardware Control Interface to set up initial (default) values of the MDIO registers. Once initial values are set, bit control reverts to the MDIO interface.

4.5 Manual Control Mode

In the Manual Control Mode, LXT973 disables direct write operations to the MDIO registers on the MDIO interface. The Hardware Control Interface is monitored during Reset to set up the MDIO registers.

Figure 16. LXT973 Initialization Sequence

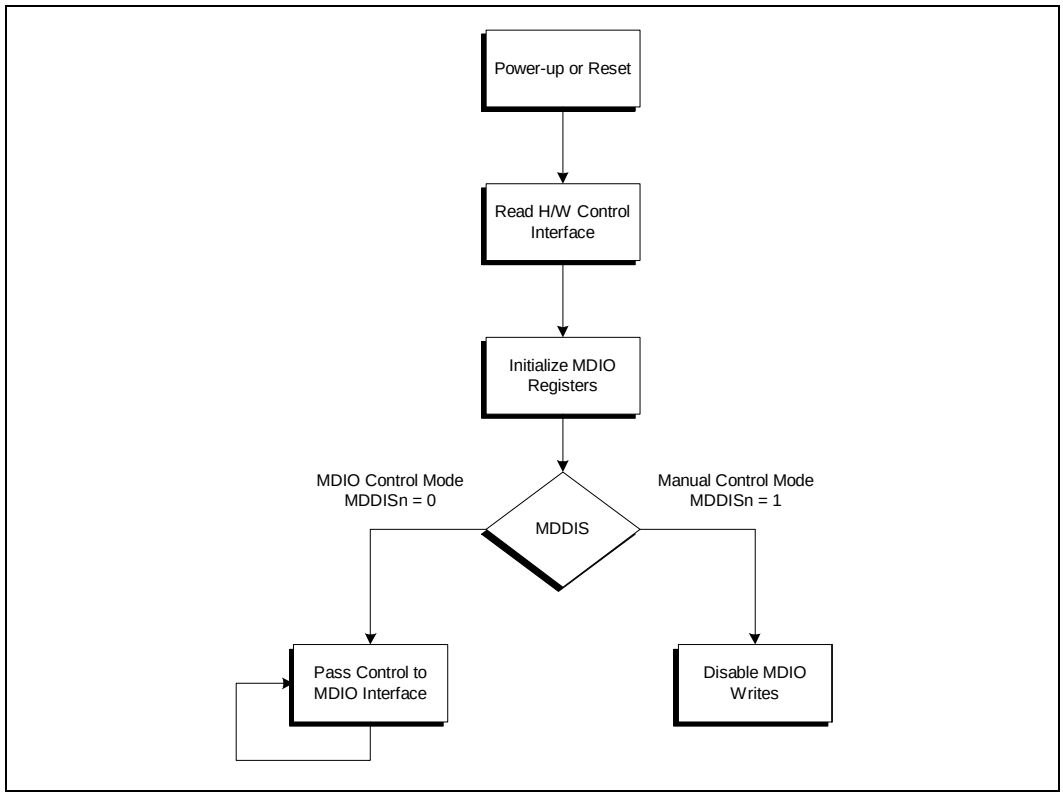


Table 12. Mode Control Settings

MDDISn	$\overline{\text{RESET}}$	PWRDWN	Mode
Low	High	Low	MDIO Control
High	High	Low	Manual Control
-	Low	Low	Reset - Latch default configuration
-	-	High	Low Power and reset mode

5.0 Configuration

When the LXT973 is first powered on, reset, or encounters a link-down state, it must determine the line speed and operating conditions to use for the network link. The LXT973 first checks the MDIO registers (initialized via the Hardware Control Interface or written by software) for operating instructions. Using these mechanisms, the user can command the LXT973 to do one of the following:

- Forced 100BASE-FX operation
- Forced twisted-pair link operation to:
  - 100BASE-TX, full-duplex
  - 100BASE-TX, half-duplex
  - 10BASE-T, full-duplex
  - 10BASE-T, half-duplex
- Allow auto-negotiation/parallel-detection.

In forced twisted-pair link operation, the LXT973 immediately begins operating the network interface as commanded. In the last case, the LXT973 begins the auto-negotiation/parallel-detection process.

Several pins are used to configure the LXT973 device. Table 13 summarizes the available manual configurations to the port. Usually these pins are decodes of chip pins. This is useful for manual configuration.

Table 13. Configuration Settings (Hardware Control Interface)

FIBER_TP*n*	AUTO_NEG*x*	SPEED*x*	DUPLEX*x*	Mode
Low	-	-	Low	100BASE-FX is enabled in half-duplex mode. Auto-negotiation is disabled
Low	-	-	High	100BASE-FX is enabled in full-duplex mode. Auto-negotiation is disabled.
High	High	High	High	AUTO_NEG is enabled. All capabilities are advertised. Register bits 4.8, 4.7, 4.6 and 4.5 are all set to 1.
High	High	High	Low	AUTO_NEG is enabled. Only 100 Mbps capabilities are advertised. Register bits 4.8 and 4.7are set to 1. Register bits 4.6 and 4.5 are cleared to 0.
High	High	Low	High	AUTO_NEG is enabled. Only 10 Mbps capabilities are advertised. Register bits 4.8 and 4.7 are cleared to 0. Register bits 4.6 and 4.5 are set to 1.
High	High	Low	Low	AUTO_NEG is enabled. Only half-duplex capabilities are advertised. Register bits 4.7 and 4.5 are set 1. Register bits 4.8 and 4.6 are cleared to 0.
High	Low	High	High	AUTO_NEG is disabled. LXT973 port x is forced to 100 Mbps full-duplex operation.
1. These pins also set the default values for Registers 0 and 4 accordingly.				

Table 13. Configuration Settings (Hardware Control Interface) (Continued)

FIBER_TP*n*	AUTO_NEG*x*	SPEED*x*	DUPLEX*x*	Mode
High	Low	High	Low	AUTO_NEG is disabled. LXT973 port x is forced to 100 Mbps half-duplex operation.
High	Low	Low	High	AUTO_NEG is disabled. LXT973 port x is forced to 10 Mbps full-duplex operation.
High	Low	Low	Low	AUTO_NEG is disabled. LXT973 port x is forced to 10 Mbps half-duplex operation.
1. These pins also set the default values for Registers 0 and 4 accordingly.				

6.0 Auto Negotiation

The LXT973 PHY supports the IEEE 802.3u auto-negotiation scheme with Next Page capability. Next Page exchange utilizes Register 7 to send information and Register 8 to receive them. Next Page exchange can only occur if both ends of the link advertise their ability to exchange Next Pages.

The LXT973 is configured to make Next Page exchange easier for software. When a Base Page or Next Page is received, the Page Received Register bit 6.1 remains set until read. When Register bit 6.2 (Next Page Able) is received, it stays set until read. This bit is cleared whenever a new negotiation occurs. This prevents the user from reading an old value in Register 6 and assuming there is valid information in Registers 5 and 8. Additionally, Register 6 contains a new bit (Register bit 6.5) that indicates when the current Received Page is the Base Page. This information is useful for recognizing when next pages must be re-sent due to the start of a new negotiation process. Register bit 16.1 and the Page Received bit (Register bit 6.1) are also cleared upon reading Register 6.

Table 14. Next Page Code Word Definitions

Next Page Encoding	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OUI tagged Message	1	a	1	0	t	0	0	0	0	0	0	0	0	1	0	1
user page 1	1	a	0	0	t	3.10	3.11	3.12	3.13	3.14	3.15	2.0	2.1	2.2	2.3	2.4
user page 2	1	a	0	0	t	2.5	2.6	2.7	2.8	2.9	2.10	2.11	2.12	2.13	2.14	2.15
user page 3	1	a	0	0	t	0	0	L.8	L.7	L.6	L.5	L.4	L.3	L.2	L.1	L.0
user page 4	1	a	0	0	t	L.10	L.9	L.8	L.7	L.6	L.5	L.4	L.3	L.2	L.1	L.0

1. a is the acknowledge bit; t is the toggle bit; L is the LFSR.

7.0 Auto MDI/MDIX

Twisted-pair Ethernet PHYs must be correctly configured for MDI or MDIX operation to inter operate. This has historically been accomplished using special patch cables, magnetics pinouts, or PCB wiring.

The LXT973 PHY supports the automatic MDI/MDIX configuration originally developed for 1000BASE-T and standardized in IEEE 802.3u, section 40. A manual configuration (for example, non-automatic) is still possible using configuration register bits. The automatic MDI/MDIX function is not intended for fiber applications.

The automatic MDI/MDIX state machine facilitates switching of the twisted-pair input signals (DPBP/N_0 and DPAP/N_1) with the twisted-pair output signals (DPAP/N_0 and DPBP/N_1), respectively, prior to the auto-negotiation mode of operation. This is done so that FLPs can be transmitted and received in compliance with Clause 28, Auto-Negotiation specifications.

The correct polarization of the crossover circuit is determined by an algorithm that controls the switching function. This algorithm uses an 11-bit Linear Feedback Shift Register (LFSR) to create a pseudo-random sequence that each end of the link uses to determine its proposed configuration.

After selecting MDI or MDIX, the node waits for a specified amount of time, while evaluating its receive channel, to determine whether the other end of the link is sending link pulses or PHY-dependent data. If link pulses or PHY-dependent data are detected, it remains in that configuration. If link pulses or PHY-dependent data are not detected, it increments its LFSR and makes a decision to switch based on the value of the next bit. The state machine does not move from one state to another while link pulses are being transmitted.

8.0 100 Mbps Operation

The MAC passes data to the LXT973 over the MII. The LXT973 encodes and scrambles the data, then transmits it using MLT-3 (for 100BASE-TX-over-copper), or NRZI signaling (for 100BASE-FX-over-fiber). The LXT973 descrambles and decodes MLT-3 data received from the network. When the MAC is not actively transmitting data, the LXT973 sends out IDLE symbols on the line.

As shown in Figure 17 on page 53, the MAC starts each transmission with a preamble pattern. When TXEN is asserted, the LXT973 transmits a /J/K/ symbol to the network (Start of Stream Delimiter or SSD). It then encodes and transmits the rest of the packet, including the balance of the preamble, the SFD (Start of Frame Delimiter), packet data, and CRC. Once the packet ends, the LXT973 transmits the
/T/R/symbol (End-of-Stream Delimiter (ESD)) and then returns to transmitting IDLE symbols.

The encoder translates the 4-bit nibbles into 5-bit symbols, which are sent over the 100BASE-TX connection. A fifth bit is provided on pins TXER0 and TXER1 during symbol mode to allow a 5-bit symbol to be sent across the MII interface. The 5B encoder is bypassed in symbol mode.

Figure 18 shows the data conversion flow from nibbles to symbols.

8.1 Displaying Symbol Errors

The PHY provides the MAC with an indication of errors that occur during the receive process. This output is called RXER. It is possible to map the symbol error detection output to the RXER pin using Register bit 26.9. In normal mode (Register bit 26.9 = 0), the RXER output is active per the IEEE 802.3 standard. When this register bit = 1, the RXER output goes active only when a symbol error is detected. This provides a quick measure of bit error rate.

Figure 17. 100BASE-TX Frame Format

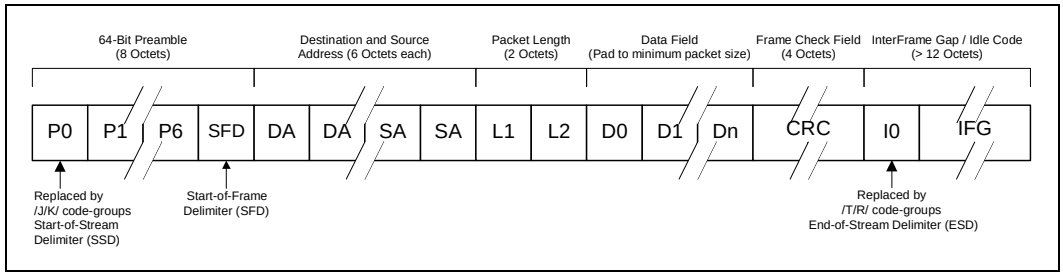
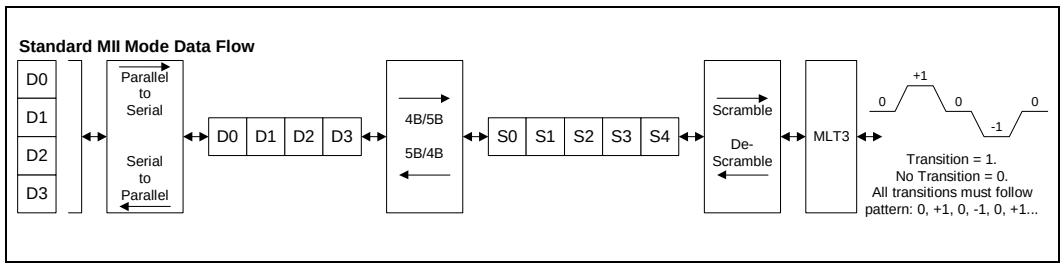


Figure 18. 100BASE-TX Data Path



8.1.1 Scrambler Seeding

Once the transmit data (or IDLE symbols) are properly encoded, they are scrambled to further reduce EMI and to spread the power spectrum using an 11-bit scrambler seed. Five-seed bits are determined by global PHY address, and six-seed bits are selected by the port number. One of the 11 bits must be a “1”.

8.1.2 Scrambler Bypass

The scrambler can be bypassed by setting Register bit 16.12 = 1. Scrambler Bypass is provided for diagnostic and test support.

The descrambler cannot be bypassed. The 100BASE-TX receiver in the LXT973 will not converge to unscrambled idle, so a descrambler bypass is useless.

8.1.3 100BASE-T Link Failure Criteria and Override

The LXT973 normally transmits 100Mbps data packets only if it detects the link is up, and transmits only Idle symbols or FLP bursts if the link is not up. Setting Register bit 16.14 = 1 overrides this function, allowing the LXT973 to transmit data packets even when the link is down. This feature is provided as a diagnostic tool. Note that auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT973 automatically begins transmitting FLP bursts if the link goes down.

8.1.4 Baseline Wander Correction

The LXT973 provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander can cause receiver errors, particularly at long line lengths (160 meters). The exact characteristics of the wander are completely data dependent. “Killer Packets” have been created that exhibit worst case baseline wander characteristics. The LXT973 baseline wander correction characteristics allow the LXT973 to recover error-free data, even at long line lengths.

8.1.5 Programmable Tx Slew Rate

The LXT973 device supports a slew rate mechanism where one of four pre-selected slew rates can be used, set either through the input pins or through Register 27.

Figure 19. 100BASE-TX Reception with no Errors

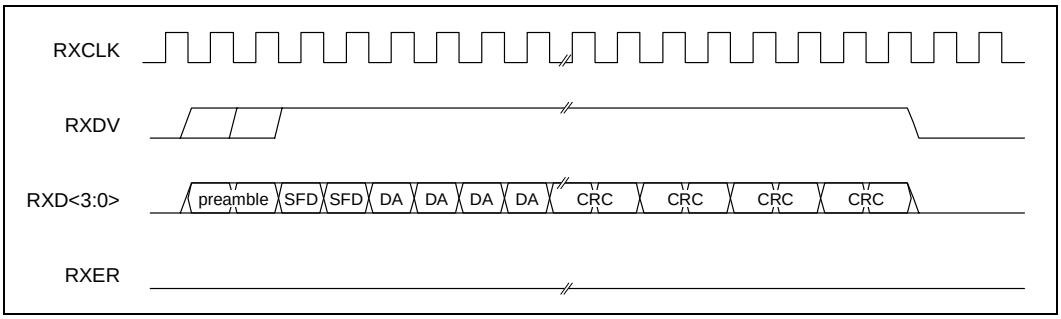


Figure 20. 100BASE-TX Reception with Invalid Symbol

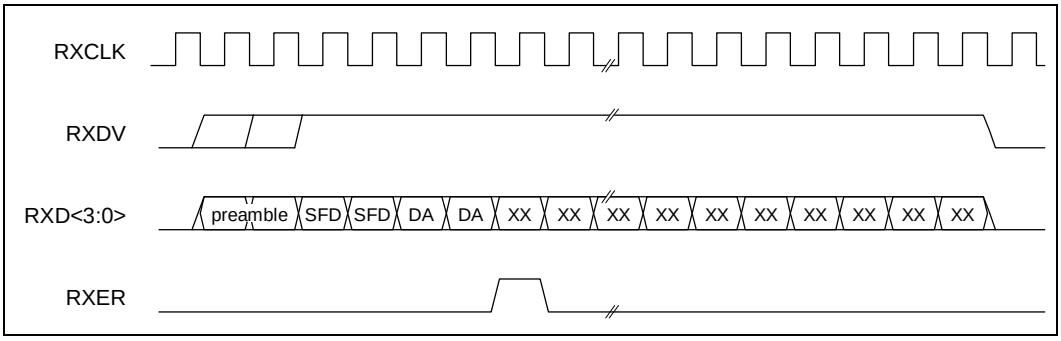


Figure 21. 100BASE-TX Transmission with no Errors

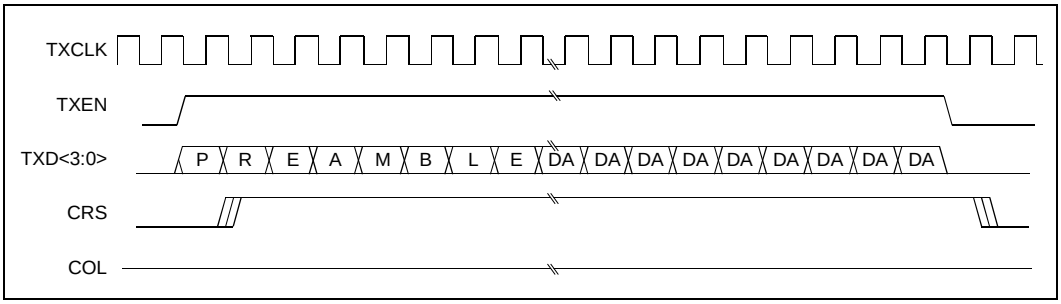
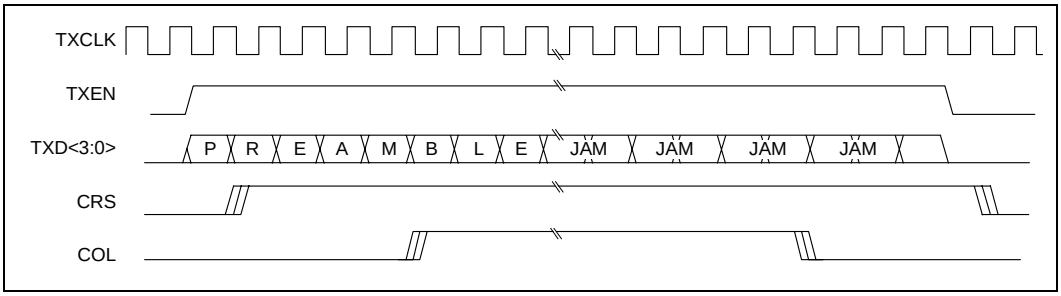


Figure 22. 100BASE-TX Transmission with Collision



9.0 Fiber Interface

The fiber ports of the LXT973 are designed to connect to common industry standard fiber modules. The fiber ports incorporate PECL receivers and drivers, allowing for seamless integration. The LXT973 provides a separate pin for the signal detect function. If designers wish to implement this feature, they need to provide a separate signal for this function. If the signal quality starts to degrade, this pin is essentially used to detect a remote fault condition and signals it accordingly. Loss of signal quality also blocks any fiber data from being received and causes a loss of link.

The remote fault code consists of 84 consecutive ones followed by a single zero. This pattern must be repeated at least three times. The LXT973 transmits the remote fault code a minimum of three times if all the following conditions are true:

1. Signal Detect indicates no signal
2. Far End Fault Enable bit (Register bit 16.2 Test Register) is set
3. Auto-negotiation is not enabled
4. Fiber mode is selected

The remote fault (Register bit 1.4) is set when the LXT973 is either actively transmitting a remote fault or if the LXT973 has received a remote fault from its link partner. The transmitted remote fault can come from the above conditions if auto-negotiation is not enabled. If auto-negotiation is enabled, the transmitted remote fault condition is indicated by Register bit 4.13 in the Auto-Negotiation Advertisement Register. Likewise, a remote fault can be set by the LXT973's link partner in two ways. If auto-negotiation is enabled, Register bit 5.13 is set in the Auto-Negotiation Link Partner Ability Register. If auto-negotiation is disabled, the remote fault condition is set by the remote fault code being received on the fiber inputs.

A register bit has been provided that either selects normal, unscrambled fiber data, or scrambles the transmitted fiber data (Register bit 26.10).

When in loopback mode, the remote fault condition is not transmitted.

10.0 10 Mbps Operation

The LXT973 operates as a standard 10 Mbps transceiver. Data transmitted by the MAC as a 4-bit nibble is serialized, Manchester-encoded, and transmitted on the twisted-pair outputs (DPAP/N_0 and DPBP/N_1). Received data is decoded, de-serialized into 4-bit nibbles, and passed on RXD[3:0] to the MAC across the MII. The LXT973 supports all the standard 10 Mbps functions.

10.1 Link Test

In 10 Mbps mode, the LXT973 always transmits link pulses. If the Link Test Function is enabled, it monitors the connection for link pulses. Once it detects two to seven link pulses, data transmission is enabled and remains enabled as long as the link pulses or data reception continues. If the link pulses stop, the data transmission is disabled.

If the Link Test function is disabled, the LXT973 may transmit packets regardless of detected link pulses. The Link Test function can be disabled by setting Port Configuration Register bit 16.14.

10.2 10Base-T Link Failure Criteria and Override

Link failure occurs if Link Test is enabled and link pulses stop being received. If this condition occurs, the LXT973 returns to the auto-negotiation phase if auto-negotiation is enabled. If the Link Integrity Test function is disabled by setting the Port Configuration Register bit 16.14, the LXT973 transmits packets, regardless of link status.

10.3 SQE (Heartbeat)

By default, the SQE (heartbeat) function is disabled on the LXT973. To enable this function, set Register bit 16.9 = 1. When this function is enabled, the LXT973 asserts its COL output for 5 - 15 bit times after each packet. See Figure 33 on page 83 for SQE timing parameters.

10.4 Jabber

If the MAC begins a transmission that exceeds the jabber timer, the LXT973 disables the transmit and loopback functions and enables the COL pin. The LXT973 automatically exits jabber mode after 250 - 750 ms. This function can be disabled by setting Register bit 16.10 = 1. See Figure 34 on page 83 for jabber timing parameters.

10.5 Polarity Correction

The LXT973 automatically detects and corrects for the condition where the receive signal (DPBP/N_0 and DPAP/N_1) is inverted. Reversed polarity is detected if 8 inverted link pulses, or 4 inverted end-of-frame markers, are received consecutively. If link pulses or data are not received for 96-130 ms, the polarity state is reset to a non-inverted state.

10.6 Dribble Bits

The LXT973 device handles dribbles bits. If one to four dribble bits are received, the nibble is passed across the interface. The data passed across is padded with ones, if necessary. If five to seven dribble bits are received, the second nibble is not sent to the MII bus. This ensures that dribble bits one through seven will not cause a MAC to discard the frame due to a CRC error. (In 10 Mbps serial mode, all bits are simply passed across the interface unmodified.)

10.7 Transmit Polarity Control

The LXT973 allows control over 10BASE-T transmit signal polarity for simplified integration. In combination with selectable MDI/MDIX mode and automatic polarity detection, this allows maximum flexibility in pinout definition. (Either of the twisted pairs may be transmit or receive, and either side of each twisted pair may be set to positive or negative.)

10.8 PHY Address

The LXT973 provides four bits to set the PHY address.The least significant bit is fixed internally with Port 1 always being one address higher than Port 0.

11.0 Clock Generation

11.1 External Oscillator

Figure 23 through Figure 25 on page 60 illustrate the different frequencies of clock for 10BASE-T and 100BASE-TX in the LXT973.

Figure 23. MII 10BASE-T DTE Mode Auto-Negotiation

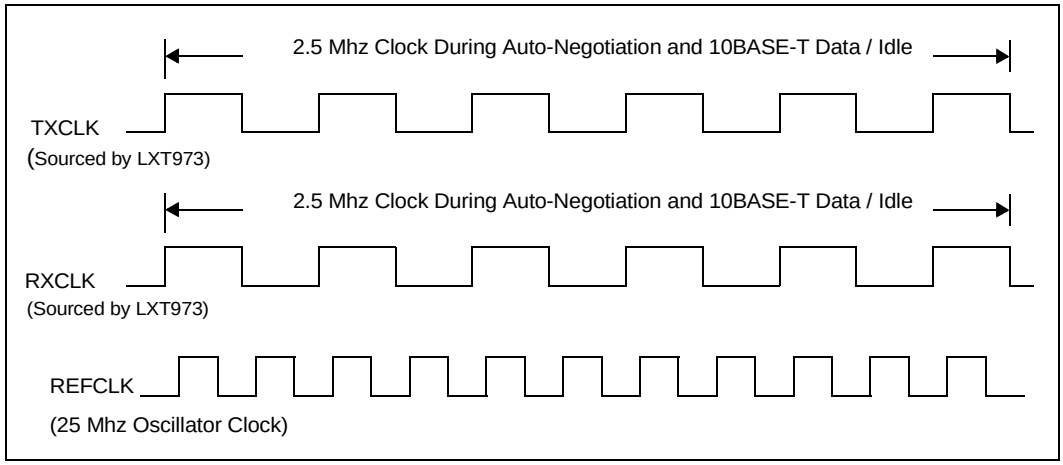


Figure 24. 100BASE-T DTE Mode Auto-Negotiation

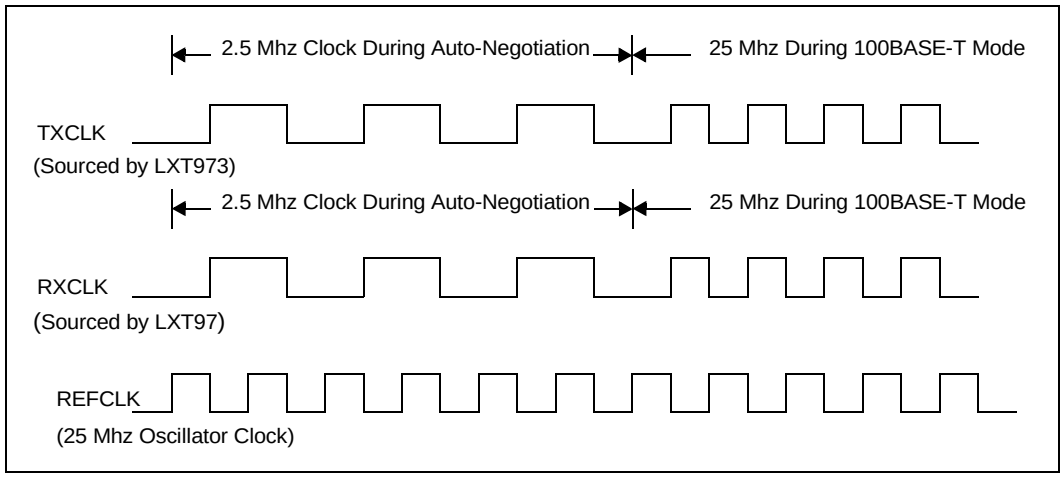
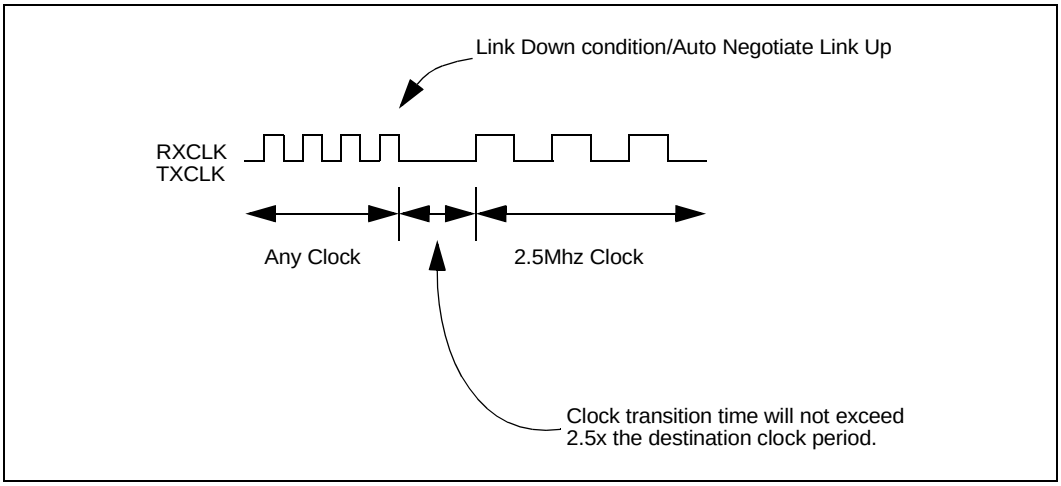


Figure 25. Link Down Clock Transition



12.0 Register Definitions

The LXT973 register set includes 16 registers per port. Refer to Table 15 for a complete register listing.

Base Registers 0 through 8 are defined in accordance with the “Reconciliation Sublayer and Media Independent Interface” and “Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation” sections of the IEEE 802.3 specification.

Additional registers are defined in accordance with the IEEE 802.3 specification for adding unique chip functions.

Table 15. Common Register Set

Address	Register Name	Bit Definitions
0	Control Register	Refer to Table 17 on page 62
1	Status Register	Refer to Table 18 on page 63
2	PHY Identification Register 1	Refer to Table 19 on page 64
3	PHY Identification Register 2	Refer to Table 20 on page 64
4	Auto-Negotiation Advertisement Register	Refer to Table 21 on page 65
5	Auto-Negotiation Link Partner Base Page Ability Register	Refer to Table 22 on page 66
6	Auto-Negotiation Expansion Register	Refer to Table 23 on page 67
7	Auto-Negotiation Next Page Transmit Register	Refer to Table 24 on page 67
8	Auto-Negotiation Link Partner Received Next Page Register	Refer to Table 25 on page 68
16	Port Configuration Register	Refer to Table 26 on page 68
18	Reserved	
26	Reserved	
27	Special Function Register	Refer to Table 27 on page 70
28	Reserved	
29	Reserved	
30	Reserved	
31	Reserved	

Table 16. Register Bit Descriptions

Bit Type	Description
R/W	Read and Write capable
RO	Read Only
WO	Write Only
AC	Auto Clear on Read
LHR	Latched from external pins on reset

Table 17. Control Register (Address 0)

Bit	Name	Description	Type[1,2]	Default
0.15	$\overline{\text{RESET}}$	1 = PHY reset 0 = Normal operation	R/W AC	0 Note 2
0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W	0
0.13	Speed Selection (LSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	LHR Note 3
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process	R/W	LHR Note 3
0.11	Power-Down	1 = Power-Down 0 = Normal operation	R/W	0
0.10	Isolate	1 = Electrically isolate PHY from MII 0 = normal operation	R/W	0 Note 4
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = Normal operation	R/W AC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	R/W	LHR Note 3
0.7	Collision Test	1 = Enable COL signal test 0 = Disable COL signal test	R/W	0
0.6	Speed Selection (MSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	00
0.5:0	Reserved	Write as 0, ignore on Read	R/W	000000

1. Refer to Table 16 on page 61 for Register Bit Descriptions.
2. During a hardware reset, all LHR information is latched in from the pins. During a software reset (Register bit 0.15), the LHR information is not re-read from the pins. This information reverts back to the information that was read in during the hardware reset. During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. During a software reset (Register bit 0.15) the registers are available for reading. The reset bit should be polled to see when the part has completed reset.
3. LHR = Latched on Hardware Reset. Register bits 0.12, 0.13 and 0.8 are initialized based on the pin configuration value.
4. The Isolate function (Register bit 0.10) tri-states all port MAC interface outputs. On the input side, TXEN and TXER are ignored.

Table 18. Status Register (Address 1)

Bit	Name	Description	Type[1,2]	Default
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO	0
1.14	100BASE-X Full- Duplex	1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X	RO	1
1.13	100BASE-X Half- Duplex	1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X	RO	1
1.12	10 Mbps Full-Duplex	1 = PHY able to operate at 10 Mbps in full-duplex mode 0 = PHY not able to operate at 10 Mbps full-duplex mode	RO	1
1.11	10 Mbps Half-Duplex	1 = PHY able to operate at 10 Mbps in half-duplex mode 0 = PHY not able to operate at 10 Mbps in half-duplex	RO	1
1.10	100BASE-T2 Full- Duplex	1 = PHY able to perform full-duplex 100BASE-T2 0 = PHY not able to perform full-duplex 100BASE-T2	RO	0
1.9	100BASE-T2 Half- Duplex	1 = PHY able to perform half-duplex 100BASE-T2 0 = PHY not able to perform half-duplex 100BASE-T2	RO	0
1.8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO	0
1.7	Reserved	0 = Write as 0, ignore on read	RO	0
1.6	MF Preamble Suppression	1 = PHY accepts management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO	0
1.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault condition detected 0 = No remote fault condition detected	RO/LH Note 2	0
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL Note 2	0
1.1	Jabber Detect	1 = Jabber condition detected 0 = Jabber condition not detected	RO/LH Note 2	0
1.0	Extended Capability	1 = Extended register capabilities 0 = Basic register set capabilities only	RO	1

1. Refer to Table 16 on page 61 for Register Bit Descriptions.
2. Bits that Latch High (LH) or Latch Low (LL) automatically clear when read.

Table 19. PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type[1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI	RO	0013
1. Refer to Table 16 on page 61 for Register Bit Descriptions.				

Table 20. PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type[1]	Default
3.15:10	PHY ID number	The PHY identifier composed of bits 19 through 24 of the OUI	RO	011110
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number	RO	100001
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number	RO	xxxx (See the LXT973 Specification Update)
1. Refer to Table 16 on page 61 for Register Bit Descriptions.				

Figure 26. PHY Identifier Bit Mapping

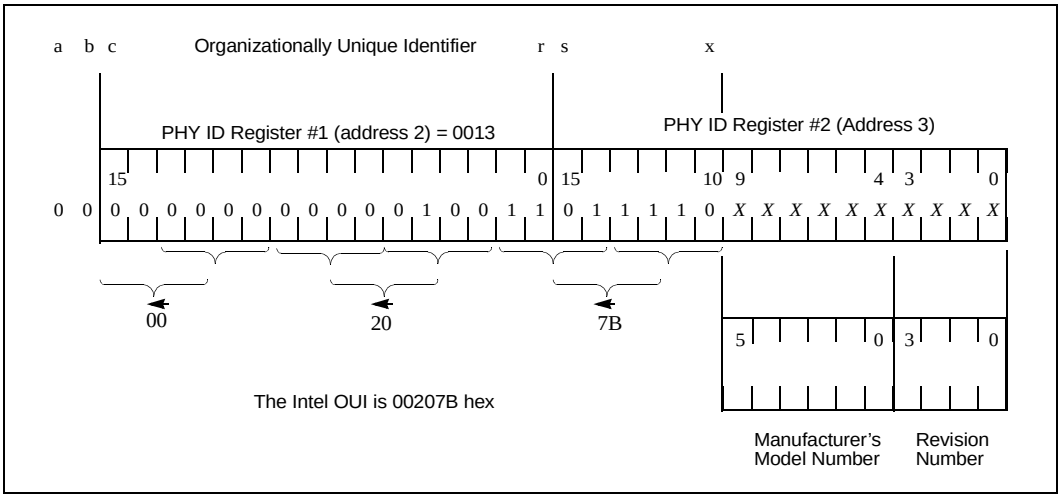


Table 21. Auto-Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type[1]	Default
4.15	Next Page	1 = PHY is capable of Next Page exchanges 0 = PHY is not capable of Next Page exchanges	R/W	0
4.14	Reserved	Write as 0, ignore on read	RO	0
4.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0
4.12	Reserved	Write as 0, ignore on read	R/W	0
4.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27	R/W	0
4.10	Pause	Pause operation defined per IEEE 802.3x standard	R/W	0
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT973 does not support 100BASE-T4 but allows this bit to be set to advertise in the auto-negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver may be switched in, if this capability is desired.)	R/W	0
4.8	100BASE-TX Full-Duplex	1 = DTE is 100BASE-TX full-duplex capable. 0 = DTE is not 100BASE-TX full-duplex capable.	R/W	0 Note 2
4.7	100BASE-TX	1 = DTE is 100BASE-TX capable. 0 = DTE is not 100BASE-TX capable.	R/W	0 Note 2
4.6	10BASE-T Full-Duplex	1 = DTE is 10BASE-T full-duplex capable. 0 = DTE is not 10BASE-T full-duplex capable.	R/W	0 Note 2
4.5	10BASE-T	1 = DTE is 10BASE-T capable. 0 = DTE is not 10BASE-T capable.	R/W	0 Note 2
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future auto-negotiation development <11111> = Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted. **Note:** The selector field can be programmed to any value. In order for auto-negotiation to complete, the link partner's received selector field must match the value programmed in this register.	R/W	00001

1. Refer to Table 16 on page 61 for Register Bit Descriptions.
2. Register bits 4.10 and 4.8:5 are initialized based on the pin configuration value.

Table 22. Auto-Negotiation Link Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type[1]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages. 0 = Link Partner has no ability to send multiple pages.	RO	0
5.14	Acknowledge	1 = Link Partner has received Link Code Word from LXT973. 0 = Link Partner has not received Link Code Word from LXT973.	RO	0
5.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	RO	0
5.12	Reserved	Write as 0, ignore on read.	RO	0
5.12:11	Asymmetric Pause	Pause operation defined in IEEE 802.3, Clauses 40 and 27	RO	0
5.10	Pause	Pause operation defined as of IEEE 802.3x	RO	0
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO	0
5.8	100BASE-TX Full-Duplex	1 = Link Partner is 100BASE-TX full-duplex capable. 0 = Link Partner is not 100BASE-TX full-duplex capable.	RO	0
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO	0
5.6	10BASE-T Full-Duplex	1 = Link Partner is 10BASE-T full-duplex capable. 0 = Link Partner is not 10BASE-T full-duplex capable.	RO	0
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO	0
5.4:0	Selector Field S[4:0]	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future auto-negotiation development <11111> = Reserved for future auto-negotiation development Unspecified or reserved combinations shall not be transmitted.	RO	00000

1. Refer to Table 16 on page 61 for Register Bit Descriptions.

NOTE: Per IEEE revised standard November 1997, this register is no longer used to store Link Partner Next Pages. Register 8 is now used for this purpose.

Table 23. Auto-Negotiation Expansion Register (Address 6)

Bit	Name	Description	Type[1]	Default
6.15:6	Reserved	Write as 0, ignore on read	RO	0
6.5	Base Page	This bit indicates the status of the auto-negotiation variable, Base Page. It also flags synchronization with the auto-negotiation state diagram, allowing detection of interrupted links. This bit is only used if Register bit 16.1 (Alternate Next Page feature) is set. 1 = base_page = true 0 = base_page = false	RO/LH Note 2	0
6.4	Parallel Detection Fault	1 = Parallel Detection Fault has occurred. 0 = Parallel Detection Fault has not occurred.	RO/LH Note 2	0
6.3	Link Partner Next Page Able	1 = Link partner is Next Page able. 0 = Link partner is not Next Page able.	RO	0
6.2	Next Page Able	1 = Local device is Next Page able 0 = Local device is not Next Page able	RO	1
6.1	Page Received	Indicates that a new page has been received and the received code word has been loaded into Register 5 (Base Pages) or Register 8 (Next Pages) as specified in clause 28 of IEEE 802.3. This bit is cleared on read. If Register bit 16.1 is set, the Page Received bit is also cleared when mr_page_rx = false, or transmit_disable = true.	RO/LH Note 2	0
6.0	Link Partner Auto-Neg Able	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.	RO	0

1. Refer to Table 16 on page 61 for Register Bit Descriptions.
2. Bits that Latch High (LH) or Latch Low (LL) automatically clear when read.

NOTE: This table contains modifications that are selectable in Intel PHYs. These modifications are used to ease the implementation of software Next Page. See separate Intel tutorial/white-paper on the usage of Next Pages.

Table 24. Auto-Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type[1]	Default
7.15	Next Page (NP)	1 = Additional Next Pages follow 0 = Last page	R/W	0
7.14	Reserved	Write as 0, ignore on read	RO	0
7.13	Message Page (MP)	1 = Message Page 0 = Unformatted page	R/W	1

1. Refer to Table 16 on page 61 for Register Bit Descriptions.

Table 24. Auto-Negotiation Next Page Transmit Register (Address 7) (Continued)

Bit	Name	Description	Type[1]	Default
7.12	Acknowledge 2 (ACK2)	1 = Complies with message 0 = Does not comply with message	R/W	0
7.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word was equal to logic zero 0 = Previous value of the transmitted Link Code Word was equal to logic one	R/W	0
7.10:0	Message/Unformatted Code Field	See Appendix C of the IEEE 802.3 standards for Next Page descriptions	R/W	00000000001

1. Refer to Table 16 on page 61 for Register Bit Descriptions.

Table 25. Auto-Negotiation Link Partner Next Page Ability Register (Address 8)

Bit	Name	Description	Type[1]	Default
8.15	Next Page (NP)	1 = Link Partner has additional Next Pages to send 0 = Link Partner has no additional Next Pages to send	RO	0
8.14	Acknowledge (ACK)	1 = Link Partner has received Link Code Word from LXT973 0 = Link Partner has not received Link Code Word from LXT973	RO	0
8.13	Message Page (MP)	1 = Page sent by the Link Partner is a Message Page 0 = Page sent by the Link Partner is an Unformatted Page	RO	0
8.12	Acknowledge 2 (ACK2)	1 = Link Partner complies with the message 0 = Link Partner cannot comply with the message	RO	0
8.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word was equal to logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	RO	0
8.10:0	Message/ Unformatted Code Field	See Appendix C of the IEEE 802.3 standards for Next Page descriptions	RO	00000000000

1. Refer to Table 16 on page 61 for Register Bit Descriptions.

Table 26. Port Configuration Register (Address 16)

Bit	Name	Description	Type[1]	Default
16.15	Reserved	Write as 0, ignore on read	R/W	0
16.14	Link Test Disable	1 = Force Link pass (sets appropriate registers and LEDs to pass) 0 = Normal operation	R/W	0
16.13	Transmit Disable	1 = Disable twisted-pair transmitter 0 = Normal operation	R/W	0

1. Refer to Table 16 on page 61 for Register Bit Descriptions.
2. Register bit 16.0 is latched in from hardware pins on hardware reset.

Table 26. Port Configuration Register (Address 16) (Continued)

Bit	Name	Description	Type[1]	Default
16.12	Bypass Scramble (100BASE-TX)	1 = Bypass Scrambler and De-scrambler 0 = Normal operation	R/W	0
16.11	Bypass 4B/5B (100BASE-TX)	1 = Bypass 4B/5B encoder and decoder 0 = Normal Operation	R/W	0
16.10	Jabber (10BASE-T)	1 = Disable Jabber 0 = Normal operation	R/W	0
16.9	SQE (10BASE-T)	1 = Enable Heart Beat 0 = Disable Heart Beat	R/W	0
16.8	TP Loopback (10BASE-T)	1 = Disable twisted-pair loopback during half-duplex operation 0 = Normal Operation - loopback in 10BASE-T, half-duplex	R/W	0
16.7	CRS Select (10BASE-T)	1 = CRS de-assert extends to RXDV de-assert 0 = Normal operation	R/W	1
16.6	Reserved	Write as 0, ignore on read	R/W	0
16.5	PRE_EN	Preamble Enable. 0 = Set RXDV High coincident with SFD 1 = Set RXDV High and RXD = preamble when CRS is asserted.	R/W	0
16.4	Reserved	Write as 0, ignore on read	R/W	0
16.3	10M Serial	1 = 10BASE_T serial mode. 10 Mbps data is driven serially on RXD<0> in this mode. 0 = Utilize normal MII mode-nibble.	R/W	0
16.2	Far End Fault Transmission Enable	1 = Enable Far End Fault transmission. 0 = Disable Far End Fault transmission.	R/W	1
16.1	Alternate NP Feature	1 = Enable Alternate auto-negotiation Next Page feature. 0 = Disable Alternate auto-negotiation Next Page feature.	R/W	0
16.0	Fiber Select	1 = Select fiber mode for this port. 0 = Select twisted-pair mode for this port.	R/W	LHR Note 2

1. Refer to Table 16 on page 61 for Register Bit Descriptions.
2. Register bit 16.0 is latched in from hardware pins on hardware reset.

Table 27. Special Function Register (Address 27)

Bit	Name	Description		Type[1]	Default
Line Length Indication					
27.15:13	Line Length Indicator	111 = Longest 110 = 101 = 100 = 011 = 010 = 001 = 000 = Shortest	Approximate line-length corresponding to each value will be determined at design verification (Not valid when agcset (Register bit 30.13 = 1)	RO	000
Special Functions					
27.12	Reserved	Write as 0, ignore on read		R/W	0
27.11:10	Per-Port Rise time Control	00 = 3.3 ns (default pins TxSLEW<1:0>) 01 = 3.6 ns 10 = 3.9 ns 11 = 4.2 ns		R/W	LHR Note 2
27.9	Auto MDIX enable	0 = Disable Auto-MDIX 1 = Enable Auto-MDIX		R/W	1
27.8	Auto-MDIX	MDI/MDIX selection 0 = MDI, transmit on pair A and receive on pair B 1 = MDIX, transmit on pair B and receive on pair A		R/W	1
27.7	Analog Loopback	1 = Enable Analog Loopback (transmits on twisted-pair) 0 = Disable Analog Loopback		R/W	0
27.6	Loopback Detect Enable	1 = Enable automatic loopback detection. 0 = Disable automatic loopback detection		R/W	0
27.5	Loopback Speed-Up Enable	1 = Enable automatic loopback detection speed-up 0 = Disable automatic loopback detection speed-up		R/W	0
27.4	Loopback Detected	1 = Loopback detected 0 = No loopback detected		RO	0
27.3:0	Reserved	Write as 0, ignore on read		R/W	00

1. Refer to Table 16 on page 61 for Register Bit Descriptions.
2. Register bits 27.11:10 are latched in from hardware pins on hardware reset.

13.0 Magnetics Information

The LXT973 requires a 1:1 ratio for both the receive and transmit path. Refer to Table 28 for transformer requirements. Transformers meeting these requirements are available from various manufacturers. Designers should test and validate all magnetics before using them in production.

Table 28. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Turns Ratio	–	1:1, 1:1	–	–	–
Insertion Loss	0.0	–	0.6	dB	–
Primary Inductance	350	–	–	µH	–
Transformer Isolation	2	–	–	kV	–
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	17	–	–	dB	.1 to 60 MHz
	15	–	–	dB	60 to 100 MHz
Rise Time	2.0	–	3.5	ns	10% to 90%

14.0 Test Specifications

Note: Table 29 through Table 51 on page 86 and Figure 27 on page 77 through Figure 40 on page 86 represent the performance specifications of the LXT973. These specifications are guaranteed by test except where noted "by design." Minimum and maximum values listed in Table 31 on page 73 through Table 51 on page 86 apply over the recommended operating conditions specified in Table 30.

Table 29. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
Supply Voltage[1,2]	VCCA, Vcc[3]	-0.3	3.0	V
	VCCPECL, VCCIO[3]	-0.3	4.0	V
Storage Temperature	TST	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

1. The voltage setting for VCCIO must be equal to or greater than the voltage setting for VCC core.
2. VCCIO and VCC core must be run at the same voltage extremes (for example, do not run VCCIO at maximum voltage and VCC core at minimum voltage.
3. VCCA = VCCR plus VCCT
   VCC = VCCD (Digital Core)
   VCCIO = Digital I/O Ring
   VCCPECL = PECL supply for fiber

Table 30. Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units
Commercial Operating Temperature		TA	0	–	+70	ºC
Extended Operating Temperature		TA	-40		+85	ºC
Recommended Supply Voltage[2]	Analog & Digital	VCCA, Vcc[3]	2.38	2.5	2.63	V
	I/O @ 3.3V	VCCIO[3]	3.14	3.3	3.45	V
	I/O @ 2.5V	VCCIO[3]	2.38	2.5	2.63	V
	I/O @ 3.3V	VCCPECL[3]	3.14	3.3	3.45	V
	I/O @ 2.5V	VCCPECL[3]	2.38	2.5	2.63	V
V_{cc} Current	100BASE-TX	ICC	–	–	150	mA
	10BASE-T	ICC	–	–	80	mA

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Voltages are with respect to ground unless otherwise specified.
3. VCCA = VCCR plus VCCT
   VCC = VCCD (digital core)
   VCCIO = digital I/O ring
   VCCPECL = PECL supply for fiber

Table 30. Operating Conditions (Continued)

Parameter		Sym	Min	Typ[1]	Max	Units
V_{CC} Current	100BASE-FX	ICC			105	mA
	Power-Down Mode	ICC	–	–	12	mA
	Auto-Negotiation	ICC	–	–	85	mA

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Voltages are with respect to ground unless otherwise specified.
3. VCCA = VCCR plus VCCT
   VCC = VCCD (digital core)
   VCCIO = digital I/O ring
   VCCPECL = PECL supply for fiber

Table 31. Digital Input/Output Characteristics[2]

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	–
Input High voltage	VIH	2.0	–	–	V	–
Input Current	II	-10	–	10	µA	0.0 < VI < VCC
Output Low voltage	VOL	–	–	0.4	V	IOL = 4 mA
Output High voltage	VOH	2.4	–	–	V	IOH = -4 mA

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Applies to all pins except MII, REFCLK, and LED pins. Refer to Table 32 for MII I/0 Characteristics.

Table 32. Digital Input/Output Characteristics - MII Pins

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	–
Input High voltage	VIH	2.0	–	–	V	–
Input Current	II	-10	–	10	µA	0.0 < VI < VCC
Output Low voltage	VOL	–	–	0.4	V	IOL = 4 mA
Output High voltage	VOH	2.4	–	–	V	IOH = -4 mA, VCCIO = 3.3V
	VOH	2.0	–	–	V	IOH = -4 mA, VCCIO = 2.5V

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design and not subject to production testing.

Table 33. REFCLK Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input Clock Frequency Tolerance[2]	Δf	–	–	±50	ppm	–
Input Clock Duty Cycle[2]	Tdc	40	–	60	%	–
Input Capacitance[2]	C_{IN}	–	3.0	–	pF	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design: not subject to production testing.

Table 34. LED Pin Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 10 mA
Output High Current	I_{OH}	–	–	10	µA	V_{OH} = VCC max
Input Leakage Current	I_I	-10	–	10	µA	0 < V_I < VCCIO

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 35. 100BASE-TX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	V_P	0.95	1.0	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	100	102	%	Note 2
Signal rise/fall time	T_{RF}	3.0	3.5	5.0	ns	Note 2
Rise/fall time symmetry	T_{RFS}	–	.25	0.5	ns	Note 2
Duty cycle distortion	D_{CD}	35	50	65	%	Offset from 16 ns pulse width at 50% of pulse peak
Overshoot/Undershoot	V_{OS}	–	–	5	%	–
Jitter (measured differentially)	–	–	0.75	1.4	ns	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω (+/-1%) resistor.

Table 36. 10BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VOP	2.2	2.5	2.8	V	Note 2
Jitter magnitude added by the MAU and PLS sections [3, 4]	$t_{tx\text{-}jit}$	–	3.2	11	ns	–
Receiver						
Differential squelch threshold	VDS	300	500	585	mV Peak	5 MHz square wave input

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter addition at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.
4. After line model specified by IEEE 802.3 for 10BASE-T MAU.

Table 37. 100BASE-FX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single-ended)[2]	VOP	0.6	1.3	1.5	V	–
Signal rise/fall time	TRF	–	1.2	1.9	ns	20% <–> 80% 2.0 pF load
Jitter (measured differentially)	–	–	0.5	1.4	ns	–
Receiver						
Peak differential input voltage	VIP	0.55	–	1.5	V	–
Common mode input range	VCMIR	–	–	VCC - 0.7	V	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω (+/-1%) resistor.

Table 38. 10BASE-T Link Integrity Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Time Link Loss Receive	TLL	50	–	150	ms	–
Link Detection	TLP	2	–	7	Link Pulses	–
Link Min Receive Timer	TLR MIN	2	–	7	ms	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 38. 10BASE-T Link Integrity Timing Characteristics (Continued)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Link Max Receive Timer	TLR MAX	50	–	150	ms	–
Link Transmit Period	Tlt	8	–	24	ms	–
Link Pulse Width	Tlpw	60	114	150	ns	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 39. Twisted-Pair Pins

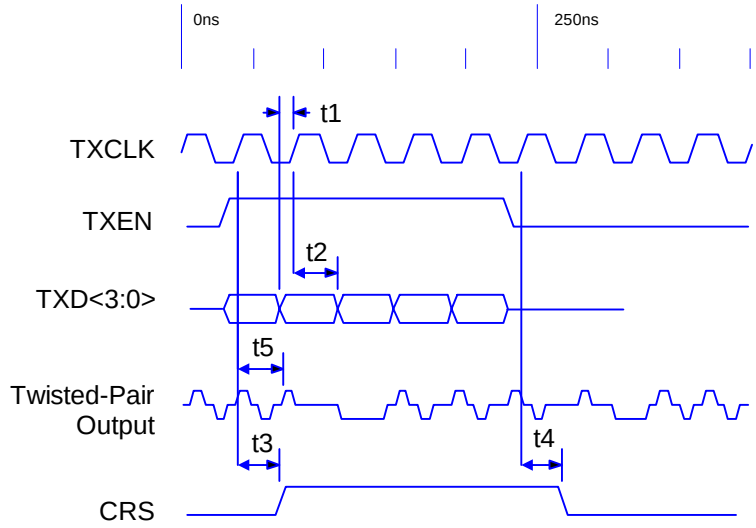
Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive input impedance[2]	ZIN	–	100	–	Ω	Between RX+ and RX-
Driver output impedance[2] (Line driver output enabled)	RO	–	100	–	Ω	Between TX+ and TX-

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

15.0 Timing Diagrams

The LXT973 device meets all timings for MII per the IEEE 802.3u standard. Table 27 through Table 32 on page 82 refer to MII timings.

Figure 27. 100BASE-TX Transmit Timing - 4B Mode



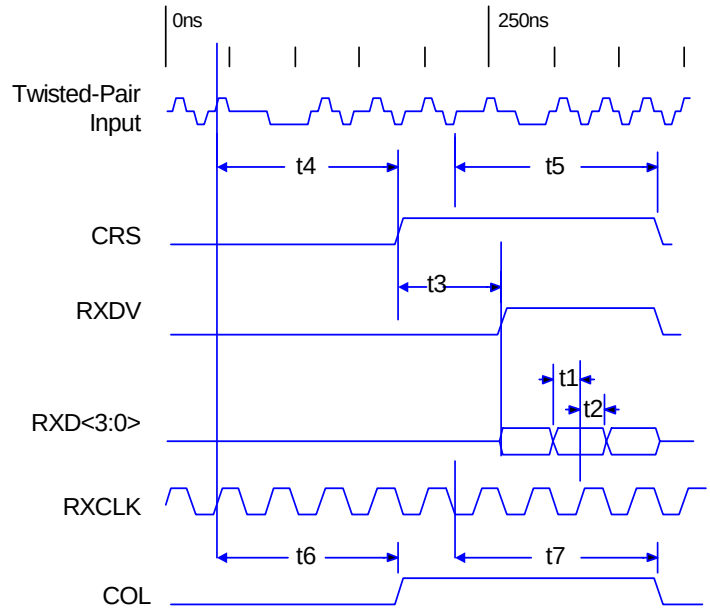
NOTE: Twisted-pair output default pins are as follows: DPAP/N_0 and DPBP/N_1.

Table 40. MII - 100BASE-TX Transmit Timing Parameters - 4B Mode

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<3:0>, TXEN, TXER setup to TXCLK High	t1	12	–	–	ns	–
TXD<3:0>, TXEN, TXER hold from TXCLK High	t2	0	–	–	ns	–
TXEN sampled to CRS asserted	t3	2	4	5	BT	–
TXEN sampled to CRS de-asserted	t4	2	4	5	BT	–
TXEN sampled to twisted-pair output (Tx latency)	t5	–	5	–	BT	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 28. 100BASE-TX Receive Timing - 4B Mode



NOTE: Twisted-pair input default pins are as follows: DPBP/N_0 and DPAP/N_1.

Table 41. MII - 100BASE-TX Receive Timing Parameters - 4B Mode

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<3:0>, RXDV, RXER setup to RXCLK High	t1	10	–	–	ns	–
RXD<3:0>, RXDV, RXER hold from RXCLK High	t2	10	–	–	ns	–
CRS asserted to RXD<3:0>, RXDV	t3	3	4	5	BT	–
Receive start of “J” to CRS asserted	t4	11	–	16	BT	–
Receive start of “T” to CRS de-asserted	t5	10	14	17	BT	–
Receive start of “J” to COL asserted	t6	10	–	15	BT	–
Receive start of “T” to COL de-asserted	t7	14	17	20	BT	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 29. 100BASE-FX Transmit Timing

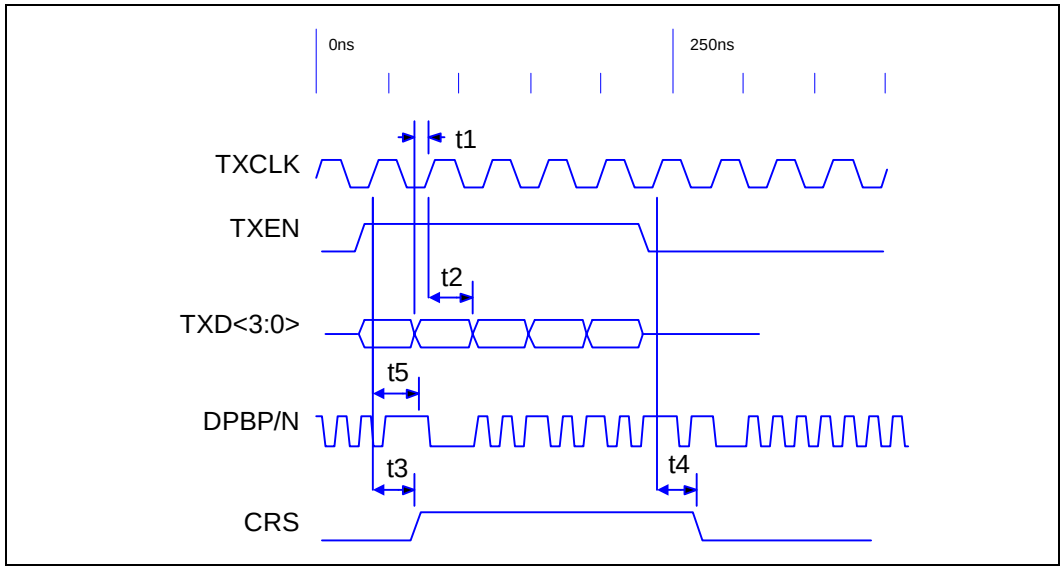


Table 42. 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<3:0>, TXEN, TXER setup to TXCLK High	t1	12	–	–	ns	–
TXD<3:0>, TXEN, TXER hold from TXCLK High	t2	0	–	–	ns	–
TXEN sampled to CRS asserted	t3	2	–	5	BT	–
TXEN sampled to CRS de-asserted	t4	1	–	5	BT	–
TXEN sampled to fiber output (Tx latency)	t5	–	4	–	BT	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 30. 100BASE-FX Receive Timing

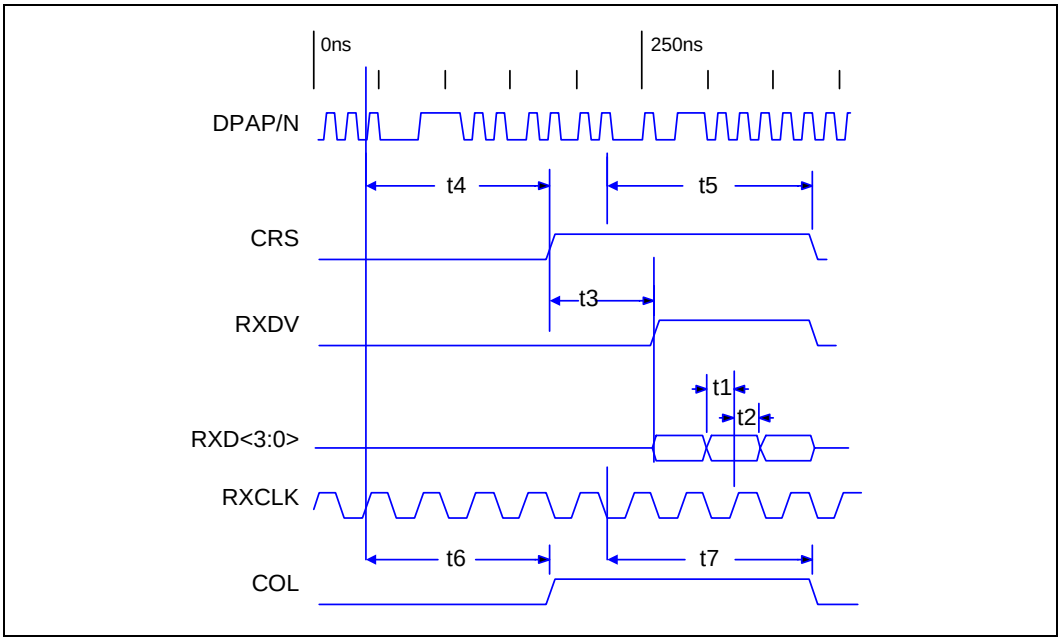
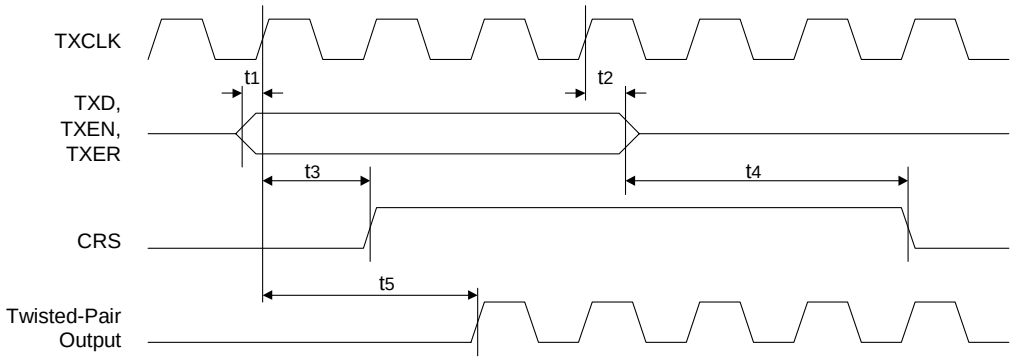


Table 43. 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<3:0>, RXDV, RXER setup to RXCLK High	t1	10	–	–	ns	–
RXD<3:0>, RXDV, RXER hold from RXCLK High	t2	10	–	–	ns	–
CRS asserted to RXD<3:0>, RXDV	t3	3	–	5	BT	–
Receive start o “J” to CRS asserted	t4	9	–	14	BT	–
Receive start of “T” to CRS de-asserted	t5	13	–	17	BT	–
Receive start of “J” to COL asserted	t6	10	–	14	BT	–
Receive start of “T” to COL de-asserted	t7	13	–	18	BT	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 31. 10BASE-T Transmit Timing (Parallel Mode)



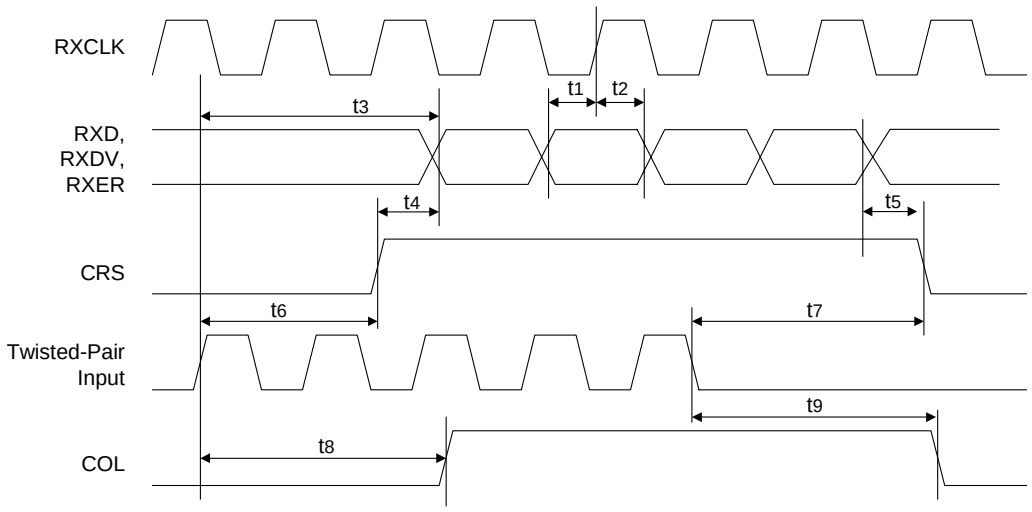
NOTE: Twisted-pair output default pins are as follows: DPAP/N_0 and DPBP/N_1.

Table 44. MII - 10BASE-T Transmit Timing Parameters (Parallel Mode)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD, TXEN, TXER setup to TXCLK High	t1	10	–	–	ns	–
TXD, TXEN, TXER hold from TXCLK High	t2	0	–	–	ns	–
TXEN sampled to CRS asserted	t3	–	5.5	–	BT	–
TXEN sampled to CRS de-asserted	t4	–	5	–	BT	–
TXEN sampled to twisted-pair output (Tx latency)	t5	–	575	–	ns	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 32. 10BASE-T Receive Timing (Parallel Mode)



NOTE: Twisted-pair input default pins are as follows: DPBP/N_0 and DPAP/N_1.

Table 45. MII - 10BASE-T Receive Timing Parameters (Parallel Mode)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD, RXDV, RXER setup to RXCLK High	t1	10	–	–	ns	–
RXD, RXDV, RXER hold from RXCLK High	t2	10	–	–	ns	–
Twisted-pair input to RXD out (Rx latency)	t3	–	64	–	BT	–
CRS asserted to RXD, RXDV, RXER asserted[2]	t4	–	62	–	BT	–
RXD, RXDV, RXER de-asserted to CRS de-asserted[3]	t5	–	0.5	–	BT	–
Twisted-pair input to CRS asserted	t6	–	4	–	BT	–
Twisted-pair input quiet to CRS de-asserted	t7	–	4	–	BT	–
Twisted-pair input to COL asserted	t8	–	4	–	BT	–
Twisted-pair input quiet to COL de-asserted	t9	–	4	–	BT	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. CRS is asserted. RXD/RXDV are driven at the start of SFD (64 BT) unless Register bit 16.5 is set.
3. If Register bit 16.7 is set, CRS extends to RXDV de-assert.

Figure 33. 10BASE-T SQE (Heartbeat) Timing

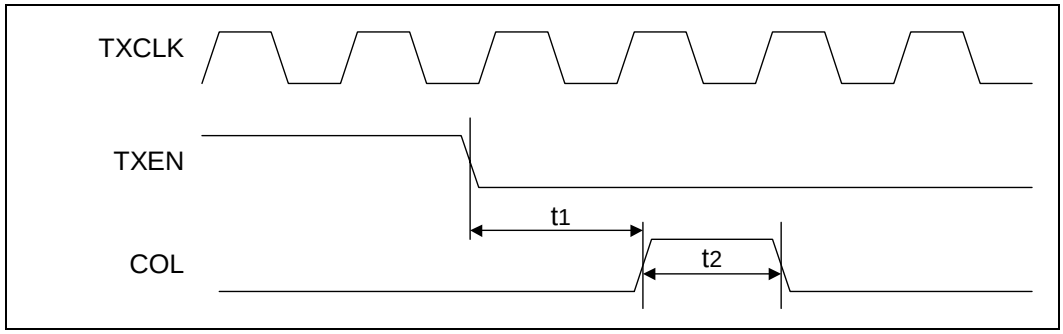


Table 46. 10BASE-T SQE (Heartbeat) Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
COL (SQE) delay after TXEN de-asserted	t1	0.65	1.2	1.6	µs	–
COL (SQE) pulse duration	t2	0.5	.95	1.5	µs	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 34. 10BASE-T Jab and Unjab Timing

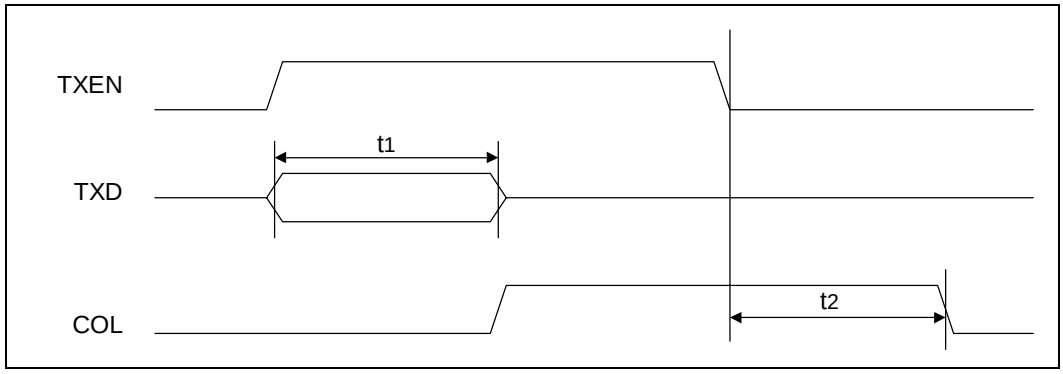
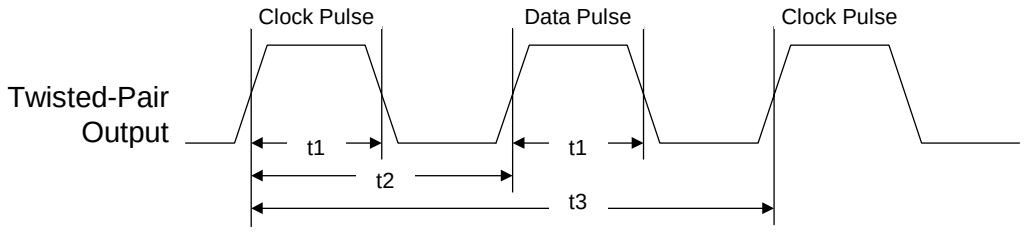


Table 47. 10BASE-T Jab and Unjab Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Maximum transmit time	t1	20	–	150	ms	–
Unjab time	t2	250	–	750	ms	–

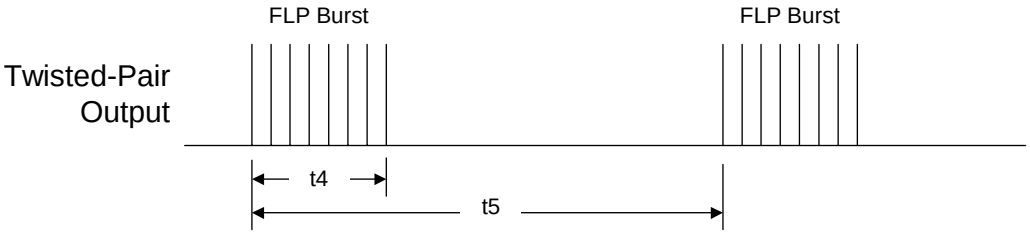
1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 35. Fast Link Pulse Timing



NOTE: Twisted-pair output default pins are as follows: DPAP/N_0 and DPBP/N_1.

Figure 36. FLP Burst Timing



NOTE: Twisted-pair output default pins are as follows: DPAP/N_0 and DPBP/N_1.

Table 48. Fast Link Pulse Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	115	116	118	ns	–
Clock pulse to Data pulse	t2	55.5	63	69.5	µs	–
Clock pulse to Clock pulse	t3	111	126	139	µs	–
FLP burst width	t4	–	2.0	–	ms	–
FLP burst to FLP burst	t5	8	10	24	ms	–
Clock/Data pulses per burst	–	17	–	33	ea	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.

Figure 37. MDIO Input Timing

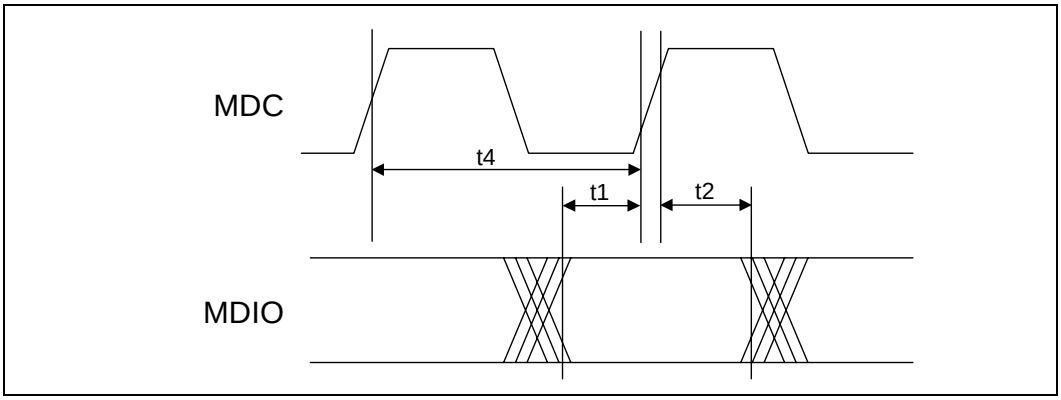


Figure 38. MDIO Output Timing

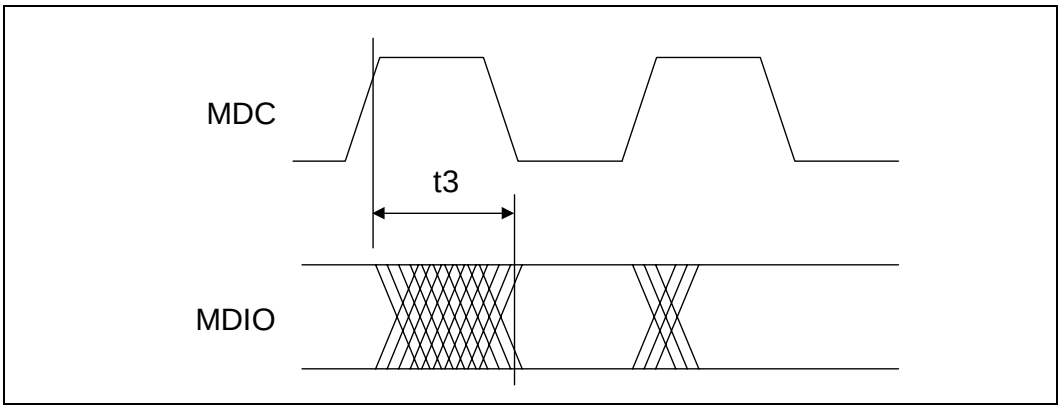


Table 49. MDIO Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO setup before MDC	t1	10	–	–	ns	When sourced by STA
MDIO hold after MDC	t2	10	–	–	ns	When sourced by STA
MDC to MDIO output delay	t3	10	–	300[2]	ns	When sourced by PHY
MDC Clock Speed	t4	–	–	20	MHz	–

1. Typical values are at 25°C, and are for design aid only, are not guaranteed, and are not subject to production testing.
2. When operated at 2.5 MHz.

Figure 39. Power-Up Timing

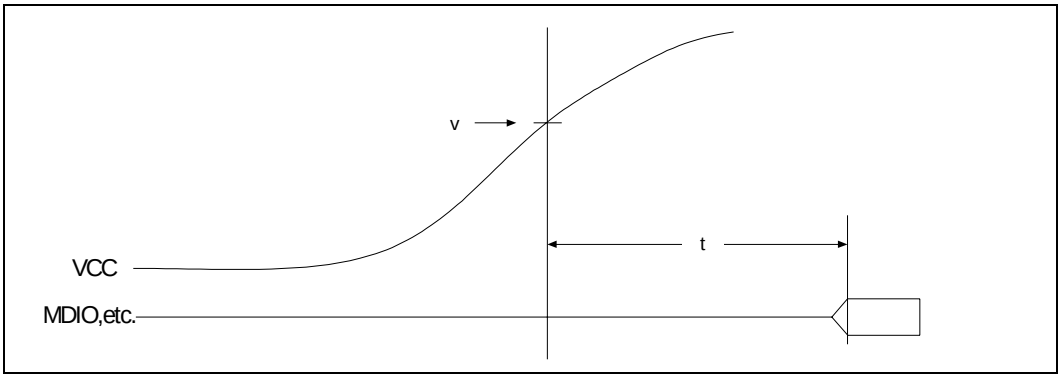


Table 50. Power-Up Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Voltage threshold	v1	2.9	–	–	V	–
Power-up delay[2]	t1	–	–	300	µs	–

1. Typical values are at 25°C and are for design aid only; not guaranteed and not subject to producing testing.
2. Power-up delay is specified as a maximum value because it refers to the PHY's guaranteed performance. - the PHY comes out of reset after a delay of No MORE Than 300 µS. System designers should consider this as a minimum value. After threshold v1 is reached, the MAC should delay No LESS than 300 µS before accessing the MDIO port.

Figure 40. $\overline{\text{RESET}}$ Pulse Width and Recovery Timing

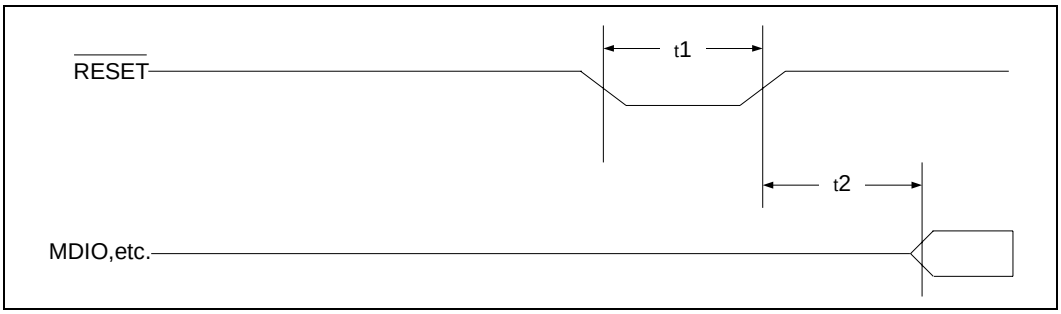


Table 51. $\overline{\text{RESET}}$ Pulse Width and Recovery Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
$\overline{\text{RESET}}$ pulse width	t1	10	–	–	ηs	–
$\overline{\text{RESET}}$ recovery delay[2]	t2	–	–	300	µs	–

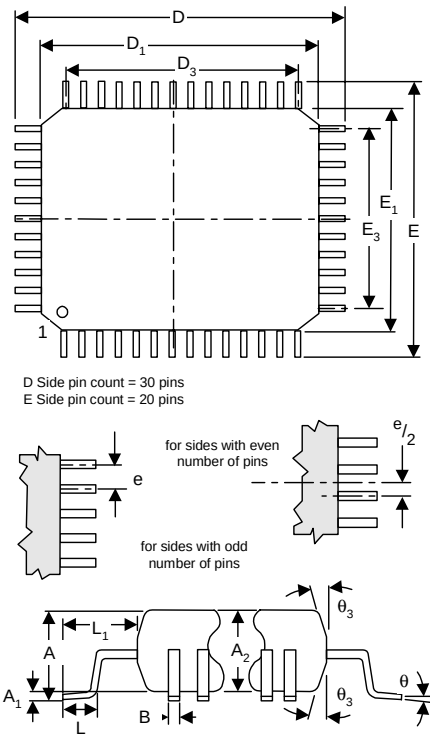
1. Typical values are at 25°C and are for design aid only; not guaranteed and not subject to producing testing.
2. Reset recovery delay is specified as a maximum value because it refers to the PHY's guaranteed performance. - the PHY comes out of reset after a delay of No MORE Than 300 µS. System designers should consider this as a minimum value. After de-asserting $\overline{\text{RESET}}$, the MAC should delay No LESS than 300 µS before accessing the MDIO port.

16.0 Mechanical Specifications

Figure 41. LXT973 Mechanical Specifications

100-Pin Plastic Quad Flat Pack

- Part Number: LXT973QC & LXT973QE
- Temperature Range:
  - — Commercial: 0° to 70°C &
  - — Extended: -40° to +85°C.



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.134	–	3.40
A_1	0.010	–	0.25	–
A_2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
D	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10
D_3	0.742 REF		18.85 REF	
E	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10
E_3	0.486 REF		12.35 REF	
e	0.026 BSC (nominal)		0.65 BSC (nominal)	
L	0.026	0.037	0.65	0.95
L_1	0.077 REF		1.95 REF	
q_3	5°	16°	5°	16°
q	0°	7°	0°	7°

BSC: Basic Spacing Between Centers

Appendix A Product Ordering Information

Number	Revision	Qualification	Tray MM	Tape & Reel MM
SLXT973QC.A2	A2	S	836691	842054
SLXT973QE.A2	A2	S	836689	842053