agere systems

Product Brief
December 2004

FW322 06 T100
*1394*A PCI PHY/Link Open Host Controller

Features

- *1394*a-2000 OHCI link and PHY core function in a single device:
  - — 100-pin TQFP package (also available in a lead-free package*.)
  - — Single-chip link and PHY enable smaller, simpler, more efficient motherboard and add-in card designs
  - — Enables lower system costs
  - — Leverages proven *1394*a-2000 PHY core design
  - — Demonstrated compatibility with current *Microsoft Windows*® drivers and common applications
  - — Demonstrated interoperability with existing, as well as older, *1394*™ consumer electronics and peripherals products
  - — Feature-rich implementation for high performance in common applications
  - — Supports low-power system designs (CMOS implementation, power management features)
- OHCI:
  - — Complies with the *1394 OHCI 1.1 Specification*
  - — OHCI 1.0 backwards compatible—configurable via EEPROM to operate in either OHCI 1.0 or OHCI 1.1 mode
  - — Complies with *Microsoft Windows* logo program system and device requirements
  - — Listed on *Windows* hardware compatibility list http://www.microsoft.com/hcl/results.asp
  - — Compatible with *Microsoft Windows* and *MacOS*® operating systems
  - — 4 Kbyte isochronous transmit FIFO
  - — 2 Kbyte asynchronous transmit FIFO
  - — 4 Kbyte isochronous receive FIFO
  - — 2 Kbyte asynchronous receive FIFO
  - — Dedicated asynchronous and isochronous descriptor-based DMA engines
  - — Eight isochronous transmit contexts
  - — Eight isochronous receive contexts
  - — Prefetches isochronous transmit data
  - — Supports posted write transactions
  - — Supports parallel processing of incoming physical read and write requests
  - — Supports notification (via interrupt) of a failed register access
- *1394*a-2000 PHY core:
  - — Compliant with *IEEE*® *1394*a-2000, *Standard for a High Performance Serial Bus* (Supplement)
  - — Provides two fully compliant cable ports, each supporting 400 Mbits/s, 200 Mbits/s, and 100 Mbits/s traffic
  - — Supports extended BIAS_HANDSHAKE time for enhanced interoperability with camcorders
  - — While unpowered and connected to the bus, will not drive TPBIAS on a connected port even if receiving incoming bias voltage on that port
  - — Does not require external filter capacitor for PLL
  - — Supports link-on as a part of the internal PHY core-link interface
  - — 25 MHz crystal oscillator and internal PLL provide a 50 MHz internal link-layer controller clock as well as transmit/receive data at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s.
  - — Interoperable across *1394* cable with *1394* physical layers (PHY core) using 5 V supplies
  - — Provides node power-class information signaling for system power management
  - — Supports ack-accelerated arbitration and fly-by concatenation
  - — Supports arbitrated short bus reset to improve utilization of the bus
  - — Fully supports suspend/resume
  - — Supports connection debounce
  - — Supports multispeed packet concatenation
  - — Supports PHY pinging and remote PHY access packets
  - — Reports cable power fail interrupt when voltage at CPS pin falls below 7.5 V
  - — Provides separate cable bias and driver termination voltage supply for each port
- Link:
  - — Cycle master and isochronous resource manager capable
  - — Supports *1394*a-2000 acceleration features
- PCI:
  - — Revision 2.2 compliant
  - — 33 MHz/32-bit operation
  - — Programmable burst size thresholds for PCI data transfer
  - — Supports optimized memory read line, memory read multiple, and memory write invalidate burst commands
  - — Supports *PCI Bus Power Management Interface Specification* v.1.1.

Note: This device does not support D3cold wakeup, CLKRUN protocol, *mini PCI*® applications, and CardBus applications. Use the FW322 06 120-pin TQFP device if one or more of these features are needed.

* In an effort to better serve its customers and the environment, Agere is switching to lead-free packaging on this product (no intentional addition of lead).

Features (continued)

Other Features

- I^2C serial ROM interface
- CMOS process
- 3.3 V operation, 5 V tolerant inputs
- 100-pin TQFP package

FW322 Functional Overview

The FW322 is a high-performance, PCI bus-based open host controller designed by Agere Systems Inc. for implementation of *IEEE 1394*a-2000 compliant systems and devices. Link-layer functions are handled by the FW322, utilizing the on-chip *1394*a-2000 compliant link core and physical layer core. A high-performance and cost-effective solution for connecting and servicing multiple *IEEE 1394* (both *1394*-1995 and *1394*a-2000) peripheral devices can be realized using this PHY/link OHCI device.

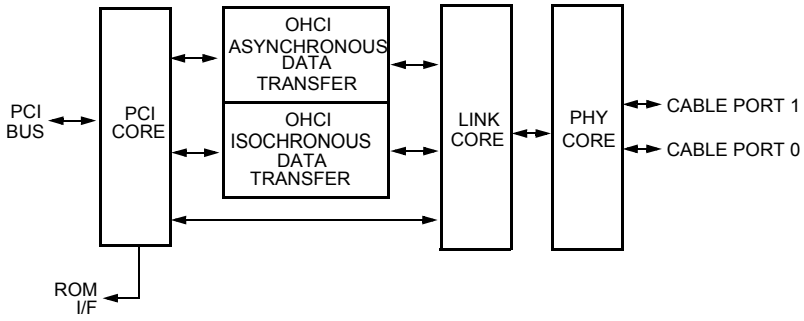


Figure 1. FW322 Conceptual Block Diagram

FW322 Functional Description

The FW322 is comprised of four major functional sections (see Figure 1): PCI core, OHCI isochronous and asynchronous data transfer, link core, and PHY core. The following is a general description of each of the major sections.

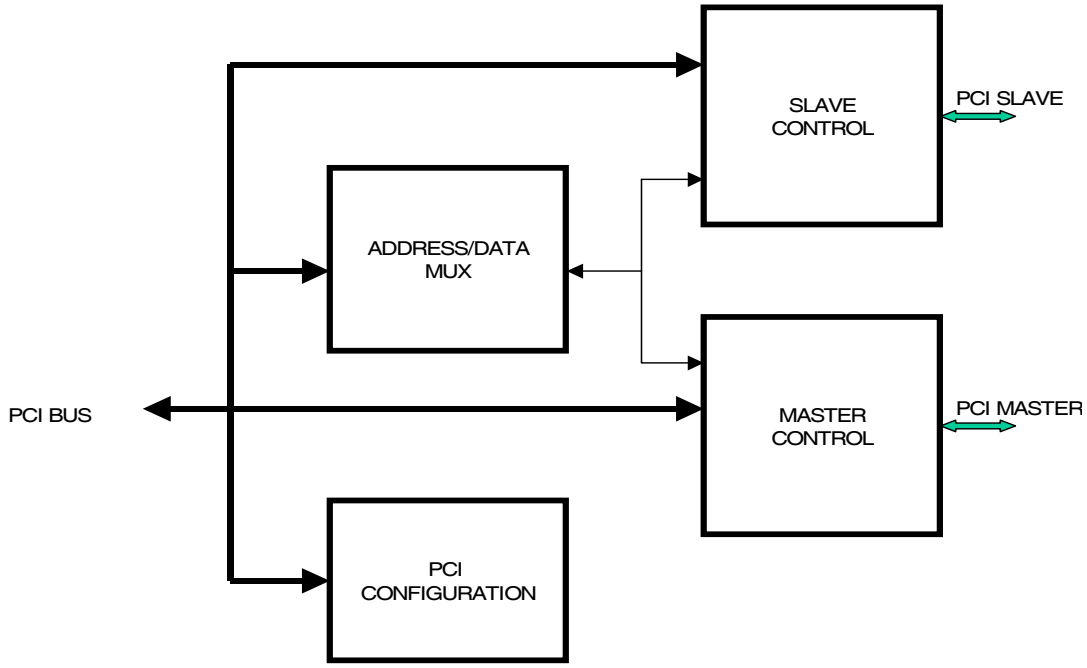


Figure 2. PCI Core Block Diagram

PCI Core

The PCI core (shown in Figure 2) serves as the interface to the PCI bus. It contains the state machines that allow the FW322 to respond properly when it is the target of the transaction. Also, during *1394* packet transmission or reception, the PCI core arbitrates for the PCI bus and enables the FW322 to become the bus master for reading the different buffer descriptors and management of the actual data transfers to/from host system memory.

The PCI core also supports the *PCI Bus Power Management Interface Specification* v.1.1. Included in this support is a standard power management register interface accessible through the PCI configuration space. Through this register interface, software is able to transition the FW322 into four distinct power consumption states (D0, D1, D2, and D3hot). This permits software to selectively increase/decrease the power consumption of the FW322 for reasons such as periods of system inactivity or power conservation. In addition, the FW322 also includes support for waking up the system through the generation of a power management event (PME).

The FW322 supports generation of a power management event (PME) while in the D0, D1, D2, and D3hot power states.

FW322 Functional Description (continued)

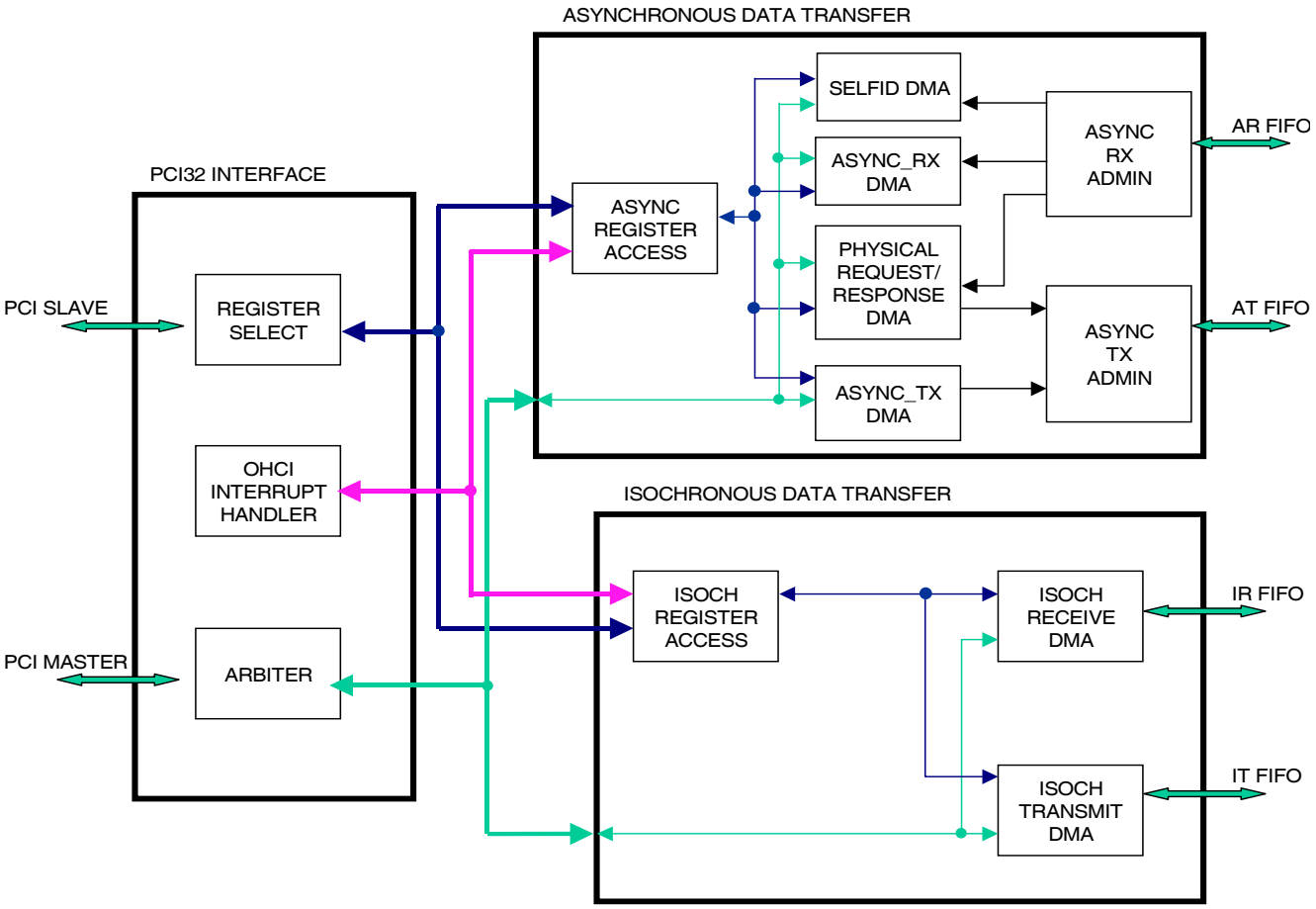


Figure 3. OHCI Core Block Diagram

OHCI Data Transfer

The OHCI core consists of the three blocks shown in Figure 3: the PCI interface (PCI32_interface), the isochronous data transfer, and the asynchronous data transfer blocks. The PCI interface provides an interface between the OHCI blocks and the PCI core. It contains an arbiter to select the appropriate OHCI data engine to gain access to the PCI core. In addition, the PCI interface includes a register select function to decode slave accesses to the OHCI core and select data from appropriate sources. The PCI interface also has an OHCI interrupt handler to service OHCI generated interrupts, which are ultimately translated into PCI interrupts.

OHCI Isochronous Data Transfer

The isochronous data transfer logic, which is incorporated into the OHCI core, handles the transfer of isochronous data between the link core and the PCI interface module. It consists of the Isochronous register access module, the isochronous transmit DMA module, the isochronous receive DMA module, the isochronous transmit (IT) FIFO, and the isochronous receive (IR) FIFO.

FW322 Functional Description (continued)

Isochronous Register Access

The Isochronous register access module services PCI slave accesses to OHCI registers within the isochronous block. The module also maintains the status of interrupts generated within the isochronous block and sends the isochronous interrupt status to the OHCI interrupt handler block.

Isochronous Transmit DMA (ITDMA)

The isochronous transmit DMA (ITDMA) module moves data from host memory to the link core, which will then send the data via the PHY core to the *1394* bus. This module consists of eight isochronous transmit contexts, each of which is independently configurable by software, and is capable of sending data on a separate *1394* isochronous channel.

During each *1394* isochronous cycle, the ITDMA module will service each of the contexts and attempt to process one *1394* packet for each active context. While processing an active context, ITDMA will request access to the PCI bus. When granted PCI access, a descriptor block is fetched from host memory. This data is decoded by ITDMA to determine how much data is required and where in host memory the data resides. ITDMA initiates another PCI access to fetch this data, which is placed into the isochronous transmit FIFO for processing by the link core. If the context is not active, it is skipped by ITDMA for the current cycle.

After processing each context, ITDMA writes a cycle marker word in the transmit FIFO to indicate to the link core that there is no more data for this isochronous cycle. As a summary, the major steps for the FW322 ITDMA to transmit a packet are the following:

1. Fetch a descriptor block from host memory.
2. Fetch data specified by the descriptor block from host memory, and place it into the isochronous transmit FIFO.
3. Data in FIFO is read by the link and sent to the PHY core device interface.

Isochronous Receive DMA (IRDMA)

The isochronous receive DMA (IRDMA) module moves data from the isochronous receive FIFO to host memory. It consists of eight isochronous contexts, each of which is independently controlled by software. Normally, each context can process data on a single *1394* isochronous channel. However, software can select one context to receive data on multiple channels.

When IRDMA detects that the link core has placed data into the receive FIFO, it immediately reads out the first word in the FIFO, which makes up the header of the isochronous packet. IRDMA extracts the channel number for the packet and packet filtering controls from the header. This information is compared with the Control registers for each context to determine if any context is to process this packet.

If a match is found, IRDMA will request access to the PCI bus. When granted PCI access, a descriptor block is fetched from host memory. The descriptor provides information about the host memory block allocated for the incoming packet. IRDMA then reads the packet from the receive FIFO and writes the data to host memory via the PCI bus.

If no match is found, IRDMA will read the remainder of the packet from the receive FIFO, but not process the data in any way.

OHCI Asynchronous Data Transfer

The asynchronous data transfer block within the OHCI core is functionally partitioned into blocks responsible for processing incoming SelfID packet streams, transmitting and receiving asynchronous *1394* packets, processing incoming physical request packets and outgoing physical response packets, and servicing accesses to OHCI registers within the respective asynchronous blocks.

Asynchronous Register Access

The Asynchronous register access module operates on PCI slave accesses to OHCI registers within the asynchronous block. The module also maintains the status of interrupts generated within the asynchronous block and sends the asynchronous interrupt status to the OHCI interrupt handler block.

FW322 Functional Description (continued)

Asynchronous Transmit DMA (ASYNC_TX DMA, ASYNC_TX_ADMIN)

The ASYNC_TX DMA and ASYNC_TX_ADMIN blocks of the FW322 manage the asynchronous transmission of either request or response packets. The mechanism for asynchronous transmission of requests and responses is similar. The only difference is the system memory location of the buffer descriptor list when processing the two contexts. Therefore, the discussion below, which pertains to asynchronous transmit requests, parallels that of asynchronous transmit responses.

The FW322 asynchronous transmission of packets involves the following steps:

1. Fetch complete buffer descriptor block from host memory.
2. Get data from system memory and store into asynchronous transmit (AT) FIFO.
3. Request transfer of data from FIFO to the link core.
4. Handle retries, if any.
5. Handle errors in steps 1 to 4.
6. End the transfer if there are no errors.

Asynchronous Receive DMA (ASYNC_RX DMA, ASYNC_RX_ADMIN)

The ASYNC_RX DMA and ASYNC_RX_ADMIN blocks of the FW322 manage the processing of received packets. Data packets are parsed and stored in a dedicated asynchronous receive (AR) FIFO. Command descriptors are read through the PCI interface to determine the disposition of the data arriving through the *1394* link.

The header of the received packet is processed to determine, among other things, the following:

1. The type of packet received.
2. The source and destinations.
3. The data and size, if any.
4. Any required operation, for example, compare and swap operation.

The asynchronous data transfer block also handles DMA transfers of SelfID packets during the *1394* bus initialization phase and block transactions associated with physical requests.

Physical Request/Response DMA

The Physical DMA block within the FW322 is responsible for processing incoming physical requests and outgoing physical responses. When an incoming asynchronous packet is received, the FW322 will process the packet automatically without software intervention if the packet meets a set of criteria defined within the OHCI specification. When the criteria are met, the asynchronous packet is reclassified as a physical packet. Requests that do not meet the criteria remain asynchronous packets and are processed as described above in the Asynchronous Receive DMA section. Processing packets as physical requests/responses allows the FW322 to either receive or transmit an asynchronous packet without the use of DMA descriptors. Instead, the FW322 directly writes or reads data to/from memory using the address defined within the packet header. Since physical packets can be processed independently of the system's software and CPU, processing a packet as physical results in a system performance optimization.

SelfID DMA

The SelfID DMA block within the FW322 is responsible for receiving SelfID packets during the bus initialization process. The received SelfID packets are written into a software-defined host memory buffer.

FW322 Functional Description (continued)

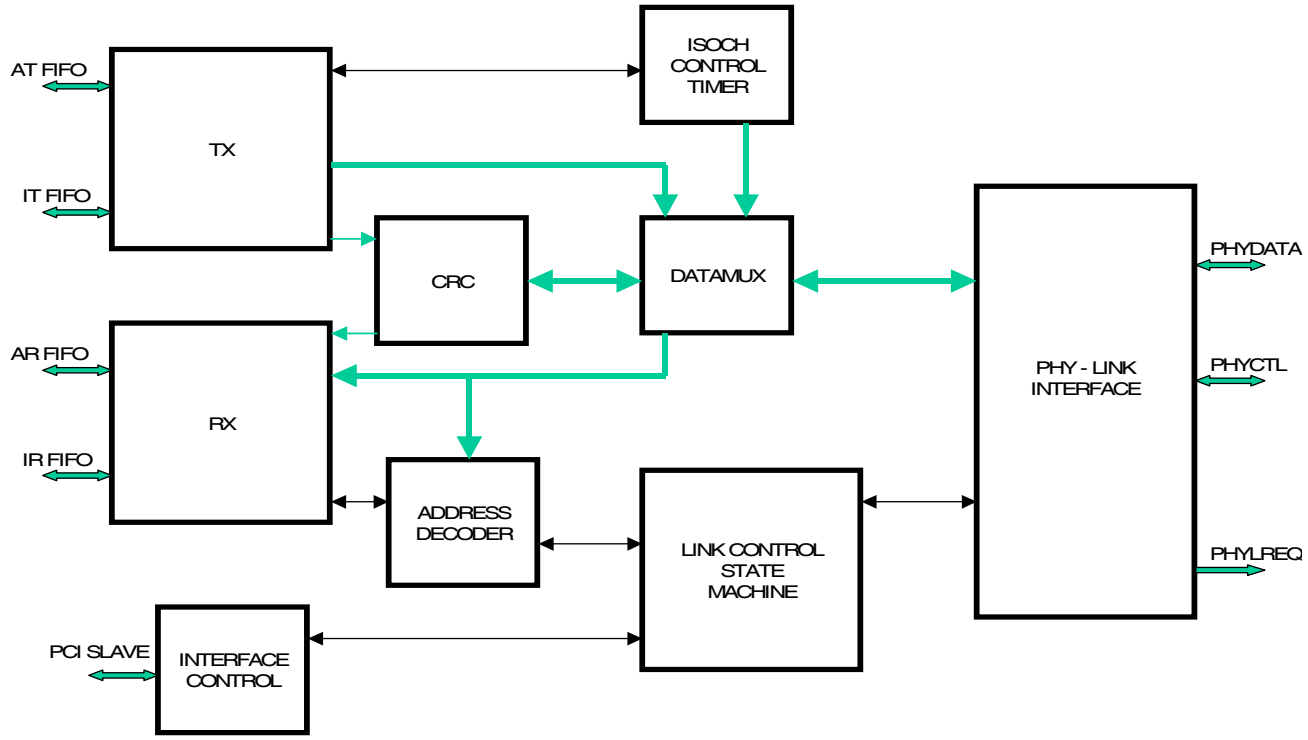


Figure 4. Link Core Block Diagram

Link Core

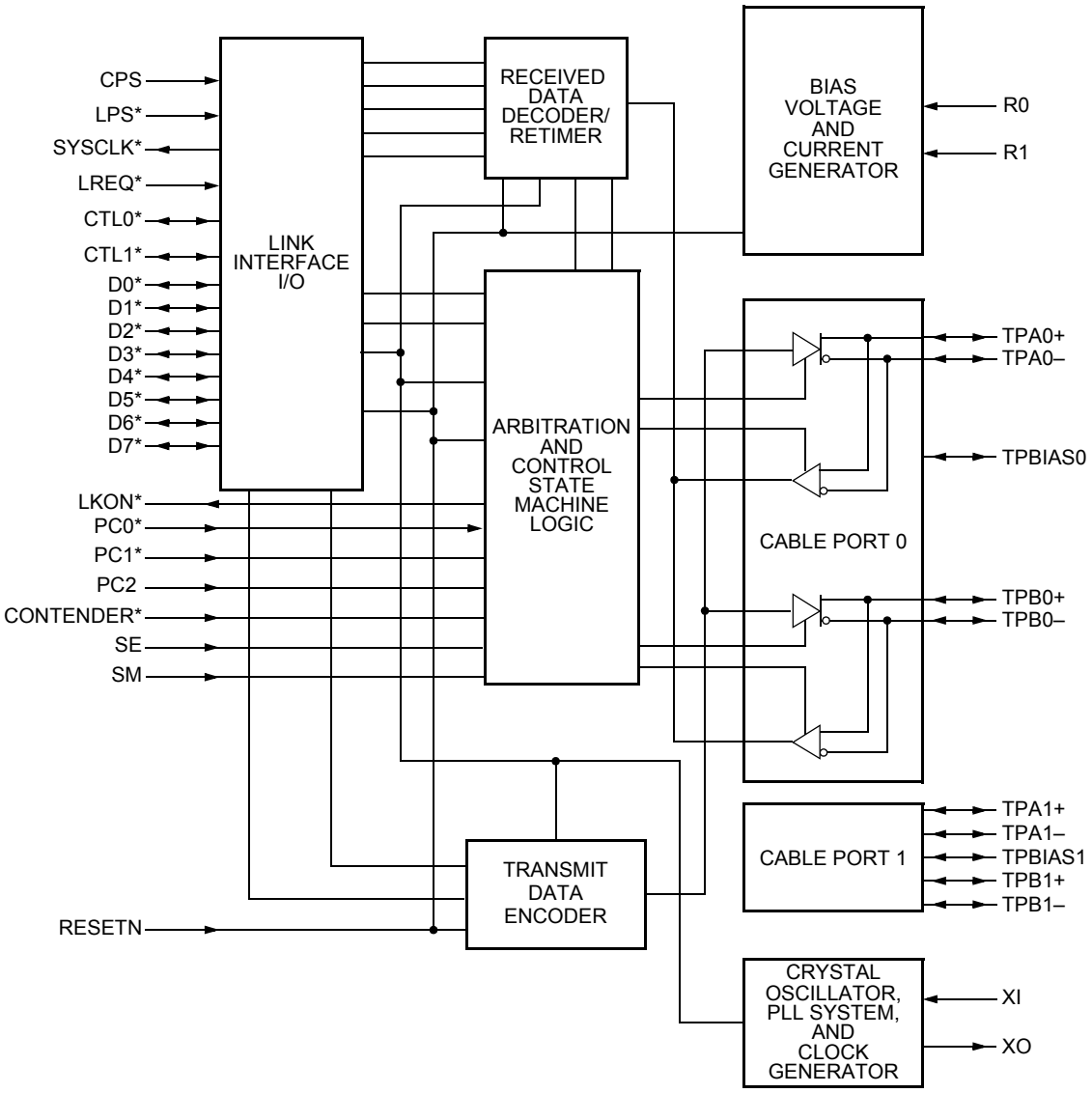
The link core shown in Figure 4 consists of the following blocks:

- **Link Control State Machine**: main link state machine that controls all other link core modules.
- **Transmit (TX)**: reads from the AT and IT FIFOs and forms *1394* packets for transmit.
- **Receive (RX)**: pipes incoming *1394* packet data to appropriate FIFO (if any).
- **Address Decoder**: decodes the destination ID of an incoming *1394* packet to determine if an acknowledge is needed.
- **CRC**: calculates and checks CRC on outgoing and incoming packets.
- **Isochronous Control Timer**: contains the logic for the *1394* cycle timer.
- **DataMUX**: pipes *1394* data to and from various modules.
- **Interface Control**: contains interrupt and registers for the link core. Interfaces with the slave control block of the PCI core.
- **PHY-Link Interface**: interfaces with the *1394* physical layer.

FW322 Functional Description (continued)

It is the responsibility of the link to ascertain if a received packet is to be forwarded to the OHCI for processing. If so, the packet is directed to a proper inbound FIFO for either the isochronous block or the asynchronous block to process. The link is also responsible for CRC generation on outgoing packets and CRC checking on received packets.

To become aware of data to be sent outbound on the *1394* bus, the link must monitor the OHCI FIFOs looking for packets in need of transmission. Based on data received from the OHCI block, the link will form packet headers for the *1394* bus. The link will alert the PHY core regarding the availability of the outbound data. It is the link's function to generate CRC for the outbound data. The link also provides PHY core register access for the OHCI.



5-5459.i(F) R.01

* Internal points, unaccessible via external package pins.

Figure 5. The PHY Core Block Diagram

FW322 Functional Description (continued)

PHY Core

The PHY core in Figure 5 on the preceding page, provides the analog physical layer functions needed to implement a two-port node in a cable-based *IEEE 1394*-1995 and *IEEE 1394*a-2000 network.

Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The PHY core interfaces with the link core.

The PHY core requires either an external 24.576 MHz crystal or crystal oscillator. The internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference signal. The 393.216 MHz reference signal is internally divided to provide the 49.152 MHz, 98.304 MHz, and 196.608 MHz clock signals that control transmission of the outbound encoded strobe and data information. The 49.152 MHz clock signal is also supplied to the associated link layer controller (LLC) for synchronization of the link with the PHY core and is used for resynchronization of the received data.

The PHY/link interface is a direct connection and does not provide isolation.

Data bits to be transmitted through the cable ports are received from the LLC on two, four, or eight data lines (D[0:7]), and are latched internally in the PHY in synchronization with the 49.152 MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304 Mbits/s, 196.608 Mbits/s, or 393.216 Mbits/s as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPA and TPB cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA and TPB cable pair. The received data strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two (for S100), four (for S200), or eight (for S400) parallel streams, resynchronized to the local system clock, and sent to the associated LLC. The received data is also transmitted (repeated) out of the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission.

In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. This monitor is called bias-detect.

The TPBIAS circuit monitors the value of incoming TPA pair common-mode voltage when local TPBIAS is inactive. Because this circuit has an internal current source and the connected node has a current sink, the monitored value indicates the cable connection status. The monitor is called connect-detect.

Both the TPB bias-detect monitor and TPBIAS connect-detect monitor are used in suspend/resume signaling and cable connection detection.

The PHY core provides a 1.86 V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceiver chips operating from 5 V or 3 V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of approximately 0.33 μF.

The port transmitter circuitry and the receiver circuitry are disabled when the port is disabled, suspended, or disconnected.

The line drivers in the PHY core operate in a high-impedance current mode and are designed to work with external 112 Ω line-termination resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56 Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A (TPA) signals is connected to the TPBIAS voltage signal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B (TPB) signals is coupled to ground through a parallel RC network with recommended resistor and capacitor values of 5 kΩ and 220 pF, respectively. The values of the external resistors are specified to meet the *1394a-2000 Specification* when connected in parallel with the internal receiver circuits.

FW322 Functional Description (continued)

An external resistor sets the driver output current, along with other internal operating currents. This resistor is connected between the R0 and R1 signals and has a value of 2.49 kΩ ± 1%.

The **C** bit (20) in the SelfID packet (see Section 4.3.4.1 of the *IEEE 1394*a-2000 specification for more details) has a default value of 0 which means this node is not a contender for bus manager. A value of 0 still allows this node to be considered by software for bus manager.

The least significant bit (23) in the Power Class (Pwr) field in the SelfID packet is set to the value of the PC2 pin. The two most significant bits (21 and 22) in the Pwr field are set to a default of 00. The PC2 pin is tied low or high to create a Pwr field of 000 (PC2 low) or 001 (PC2 high). See Section 4.3.4.1 of the *IEEE 1394*a-2000 specification for additional details.

When the power supply of the PHY core is removed while the twisted-pair cables are connected, the PHY core transmitter and receiver circuitry has been designed to present a high impedance to the cable in order to not load the TPBIAS signal voltage on the other end of the cable.

Whenever the TPA±/TPB± signals are wired to a connector, they must be terminated using the normal termination network. This is required for reliable operation. For those applications when one or more of the FW322 ports are not wired to a connector, those unused ports may be left unconnected without normal termination. When a port does not have a cable connected, internal connect-detect circuitry will keep the port in a disconnected state.

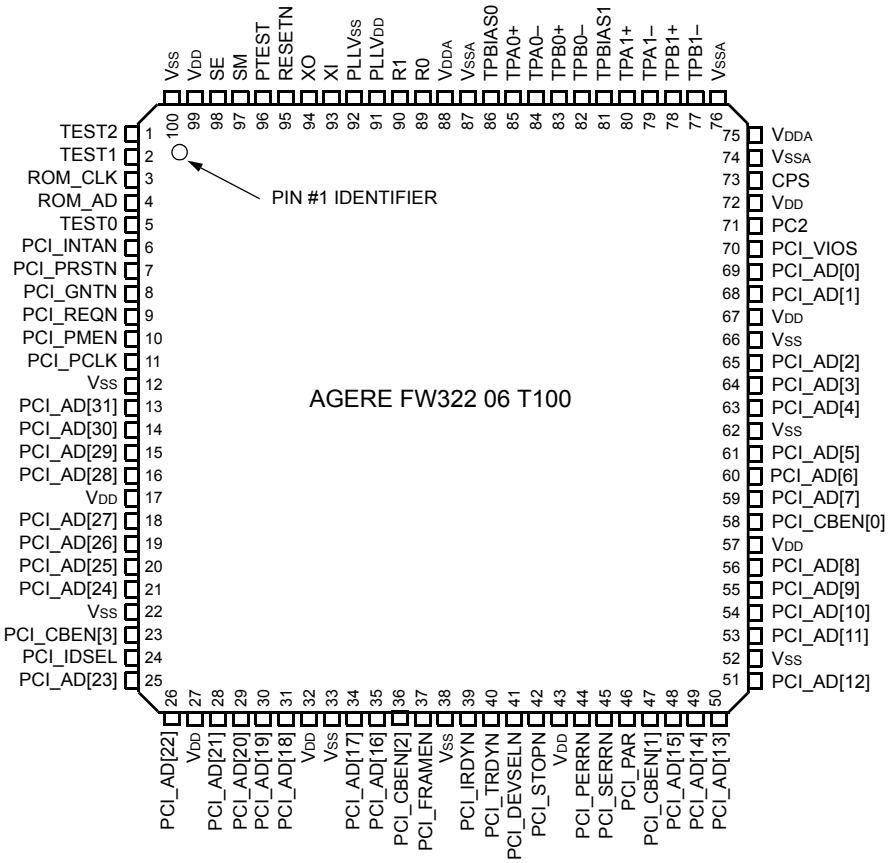
Note: All gap counts on all nodes of a *1394* bus must be identical. The software accomplishes this by issuing PHY core configuration packets (see Section 4.3.4.3 of *IEEE 1394*-1995 and *1394*a-2000 standards) or by issuing two bus resets, which resets the gap counts to the maximum level (3Fh).

The internal link power status (LPS) signal works with the internal LKON signal to manage the LLC power usage of the node. The LPS signal indicates if the LLC of the node is powered up or down. If LPS is inactive for more than 1.2 μs and less than 25 μs, the internal PHY/link interface is reset.

If LPS is inactive for greater than 25 μs, the PHY will disable the internal PHY/link interface to save power. The FW322 continues its repeater function even when the PHY/link interface is disabled. If the PHY then receives a link-on packet, the internal LKON signal is activated to output a 6.114 MHz signal, which can be used by the LLC to power itself up. Once the LLC is powered up, the internal LPS signal communicates this to the PHY and the internal PHY/link interface is enabled. The internal LKON signal is turned off when the LCtrl bit is set.

Six of the FW322 pins are used to set up various test conditions used only during the device manufacturing process. These pins are SE, SM, TEST0, TEST1, TEST2, and PTEST.

Pin Information



5-7338 (F)r.2

Note: Active-low signals within this document are indicated by an N following the symbol names.

Figure 6. Pin Assignments for the FW322 06 T100

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol*	Type	Description
1	TEST2	I	**Test.** Used by Agere for device manufacturing testing. This pin has an internal pull-up resistor so it can be left floating (or tied high) for normal operation. Do not tie this pin to VSS.
2	TEST1	I	**Test.** Used by Agere for device manufacturing testing. Tie to VSS for normal operation.
3	ROM_CLK	I/O	**ROM Clock.**
4	ROM_AD	I/O	**ROM Address/Data.**
5	TEST0	I	**Test.** Used by Agere for device manufacturing testing. Tie to VSS for normal operation.
6	PCI_INTAN	O	**PCI Interrupt (Active-Low).**
7	PCI_PRSTN	I	**PCI Reset (Active-Low).**
8	PCI_GNTN	I	**PCI Grant Signal (Active-Low).**
9	PCI_REQN	O	**PCI Request Signal (Active-Low).**
10	PCI_PMEN	O	**PCI Power Management Event (Active-Low).** A PCI power management event will be indicated if this signal is low.
11	PCI_PCLK	I	**PCI Clock Input.** 33 MHz.
12	VSS	—	**Digital Ground.**
13	PCI_AD[31]	I/O	**PCI Address/Data Bit.**
14	PCI_AD[30]	I/O	**PCI Address/Data Bit.**
15	PCI_AD[29]	I/O	**PCI Address/Data Bit.**
16	PCI_AD[28]	I/O	**PCI Address/Data Bit.**
17	VDD	—	**Digital Power.**
18	PCI_AD[27]	I/O	**PCI Address/Data Bit.**
19	PCI_AD[26]	I/O	**PCI Address/Data Bit.**
20	PCI_AD[25]	I/O	**PCI Address/Data Bit.**
21	PCI_AD[24]	I/O	**PCI Address/Data Bit.**
22	VSS	—	**Digital Ground.**
23	PCI_CBEN[3]	I/O	**PCI Command/Byte Enable (Active-Low).**
24	PCI_IDSEL	I	**PCI ID Select.**
25	PCI_AD[23]	I/O	**PCI Address/Data Bit.**
26	PCI_AD[22]	I/O	**PCI Address/Data Bit.**
27	VDD	—	**Digital Power.**
28	PCI_AD[21]	I/O	**PCI Address/Data Bit.**
29	PCI_AD[20]	I/O	**PCI Address/Data Bit.**
30	PCI_AD[19]	I/O	**PCI Address/Data Bit.**
31	PCI_AD[18]	I/O	**PCI Address/Data Bit.**
32	VDD	—	**Digital Power.**
33	VSS	—	**Digital Ground.**
34	PCI_AD[17]	I/O	**PCI Address/Data Bit.**
35	PCI_AD[16]	I/O	**PCI Address/Data Bit.**
36	PCI_CBEN[2]	I/O	**PCI Command/Byte Enable Signal (Active-Low).**
37	PCI_FRAMEN	I/O	**PCI Frame Signal (Active-Low).**

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
38	VSS	—	**Digital Power.**
39	PCI_IRDYN	I/O	**PCI Initiator Ready Signal (Active-Low).**
40	PCI_TRDYN	I/O	**PCI Target Ready Signal (Active-Low).**
41	PCI_DEVSELN	I/O	**PCI Device Select Signal (Active-Low).**
42	PCI_STOPN	I/O	**PCI Stop Signal (Active-Low).**
43	VDD	—	**Digital Power.**
44	PCI_PERRN	I/O	**PCI Parity Error Signal (Active-Low).**
45	PCI_SERRN	I/O	**PCI System Error Signal (Active-Low).**
46	PCI_PAR	I/O	**PCI Parity Signal.**
47	PCI_CBEN[1]	I/O	**PCI Command/Byte Enable Signal (Active-Low).**
48	PCI_AD[15]	I/O	**PCI Address/Data Bit.**
49	PCI_AD[14]	I/O	**PCI Address/Data Bit.**
50	PCI_AD[13]	I/O	**PCI Address/Data Bit.**
51	PCI_AD[12]	I/O	**PCI Address/Data Bit.**
52	VSS	—	**Digital Ground.**
53	PCI_AD[11]	I/O	**PCI Address/Data Bit.**
54	PCI_AD[10]	I/O	**PCI Address/Data Bit.**
55	PCI_AD[9]	I/O	**PCI Address/Data Bit.**
56	PCI_AD[8]	I/O	**PCI Address/Data Bit.**
57	VDD	—	**Digital Power.**
58	PCI_CBEN[0]	I/O	**PCI Command/Byte Enable Signal (Active-Low).**
59	PCI_AD[7]	I/O	**PCI Address/Data Bit.**
60	PCI_AD[6]	I/O	**PCI Address/Data Bit.**
61	PCI_AD[5]	I/O	**PCI Address/Data Bit.**
62	VSS	—	**Digital Ground.**
63	PCI_AD[4]	I/O	**PCI Address/Data Bit.**
64	PCI_AD[3]	I/O	**PCI Address/Data Bit.**
65	PCI_AD[2]	I/O	**PCI Address/Data Bit.**
66	VSS	—	**Digital Ground.**
67	VDD	—	**Digital Power.**
68	PCI_AD[1]	I/O	**PCI Address/Data Bit.**
69	PCI_AD[0]	I/O	**PCI Address/Data Bit.**
70	PCI_VIOS	—	**PCI Signaling Indicator.** For PCI applications that use a universal expansion board (see *PCI Local Bus Specification*, Rev. 2.2, Section 4.1.1), connect this pin to the VI/O pin. For other cases, connect this pin to 3.3 V for PCI buses using 3.3 V signaling or to 5 V for PCI buses using 5 V signaling.

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
71	PC2	I	**Power-Class Indicator.** On hardware reset (RESETN), this input sets the default value of the least significant bit in the Power Class field (**Pwr**) in the SelfID packet (see Section 4.3.4.1 of the *1394a-2000 Specification*). This bit can be tied to VDD (high) or to VSS (low) as required for particular power consumption and source characteristics. The two most significant **Pwr** bits in the SelfID are internally set to zero. As an example, for a **Pwr** field value of 001, PC2 = 1.
72	VDD	—	**Digital Power.**
73	CPS	I	**Cable Power Status.** CPS is normally connected to the cable power through a 400 kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This information is maintained in one internal register and is available to the LLC by way of a register read (see *IEEE 1394a*-2000, *Standard for a High Performance Serial Bus*, Sections 4.2.2.7 and 5B.1). **Note:** This pin can be left unconnected for applications that do not use *1394* bus power (VP). When this pin is grounded, the PWR_FAIL bit in PHY register 0101_2 will set.
74	VSSA	—	**Analog Circuit Ground.** All VSSA signals should be tied together to a low-impedance ground plane.
75	VDDA	—	**Analog Circuit Power.** VDDA supplies power to the analog portion of the device.
76	VSSA	—	**Analog Circuit Ground.** All VSSA signals should be tied together to a low-impedance ground plane.
77	TPB1–	Analog I/O	**Port 1, Port Cable Pair B.** TPB1± is the port B connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector. When the FW322's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
78	TPB1+		
79	TPA1–	Analog I/O	**Port 1, Port Cable Pair A.** TPA1± is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector. When the FW322's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
80	TPA1+		

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
81	TPBIAS1	Analog I/O	**Port 1, Twisted-Pair Bias.** TPBIAS1 provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes. When the FW322's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
82	TPB0–	Analog I/O	**Port 0, Port Cable Pair B.** TPB0± is the port B connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector. When the FW322's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
83	TPB0+		
84	TPA0–	Analog I/O	**Port 0, Port Cable Pair A.** TPA0± is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector. When the FW322's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
85	TPA0+		
86	TPBIAS0	Analog I/O	**Port 0, Twisted-Pair Bias.** TPBIAS0 provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes. When the FW322's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
87	V_{SSA}	—	**Analog Circuit Ground.** All V_{SSA} signals should be tied together to a low-impedance ground plane.
88	V_{DDA}	—	**Analog Circuit Power.** V_{DDA} supplies power to the analog portion of the device.
89	R0	I	**Current Setting Resistor.** An internal reference voltage is applied to a resistor connected between R0 and R1 to set the operating current and the cable driver output current. A low temperature-coefficient resistor (TCR) with a value of 2.49 kΩ ± 1% should be used to meet the *IEEE 1394*-1995 standard requirements for output voltage limits.
90	R1		
91	$PLLV_{DD}$	—	**Power for PLL Circuit.** $PLLV_{DD}$ supplies power to the PLL circuitry portion of the device.
92	$PLLV_{SS}$	—	**Ground for PLL Circuit.** $PLLV_{SS}$ is tied to a low-impedance ground plane.

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
93	XI	Analog I/O	**Crystal Oscillator.** XI and XO connect to a 24.576 MHz parallel resonant fundamental mode crystal. Although when a 24.576 MHz clock source is used, it can be connected to XI with XO left unconnected. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used. It is necessary to add an external series resistor to the XO pin. The value of the resistor is nominally 400 Ω. Note that it is very important to place the crystal as close as possible to the XO and XI pins, i.e., within 0.5 in./ 1.27 cm. For more important details regarding the crystal, refer to the *FW323/FW322 Hardware Implementation Design Guideline* Application Note.
94	XO		
95	RESETN	I	**Reset (Active-Low).** When RESETN is asserted low (active), a *1394* bus reset condition is set on the active cable ports and the FW322 is reset to the reset start state. To guarantee that the PHY will reset, this pin must be held low for at least 2 ms. An internal pull-up resistor, connected to VDD, is provided, so only an external delay capacitor (0.1 μF) and resistor (510 kΩ), in parallel, are required to connect this pin to ground. This circuitry will ensure that the capacitor will be discharged when PHY power is removed. The input is a standard logic buffer and can also be driven by an open-drain logic output buffer. Do not leave this pin unconnected. This pin is also used with the EEPROM interface. It is the powerup reset pin. This pin is asserted low (active) to indicate a powerup reset. Refer to the *FW322 06/FW323 06 EEPROM Interface and Start-up Behavior* Application Note sections titled Initiation of EEPROM Load and Initial Powerup.
96	PTEST	I	**Test.** Used by Agere for device manufacturing testing. Tie to VSS for normal operation.
97	SM	I	**Test Mode Control.** SM is used during Agere's manufacturing test and should be tied to VSS for normal operation.
98	SE	I	**Test Mode Control.** SE is used during Agere's manufacturing test and should be tied to VSS for normal operation.
99	VDD	—	**Digital Power.**
100	VSS	—	**Digital Ground.**

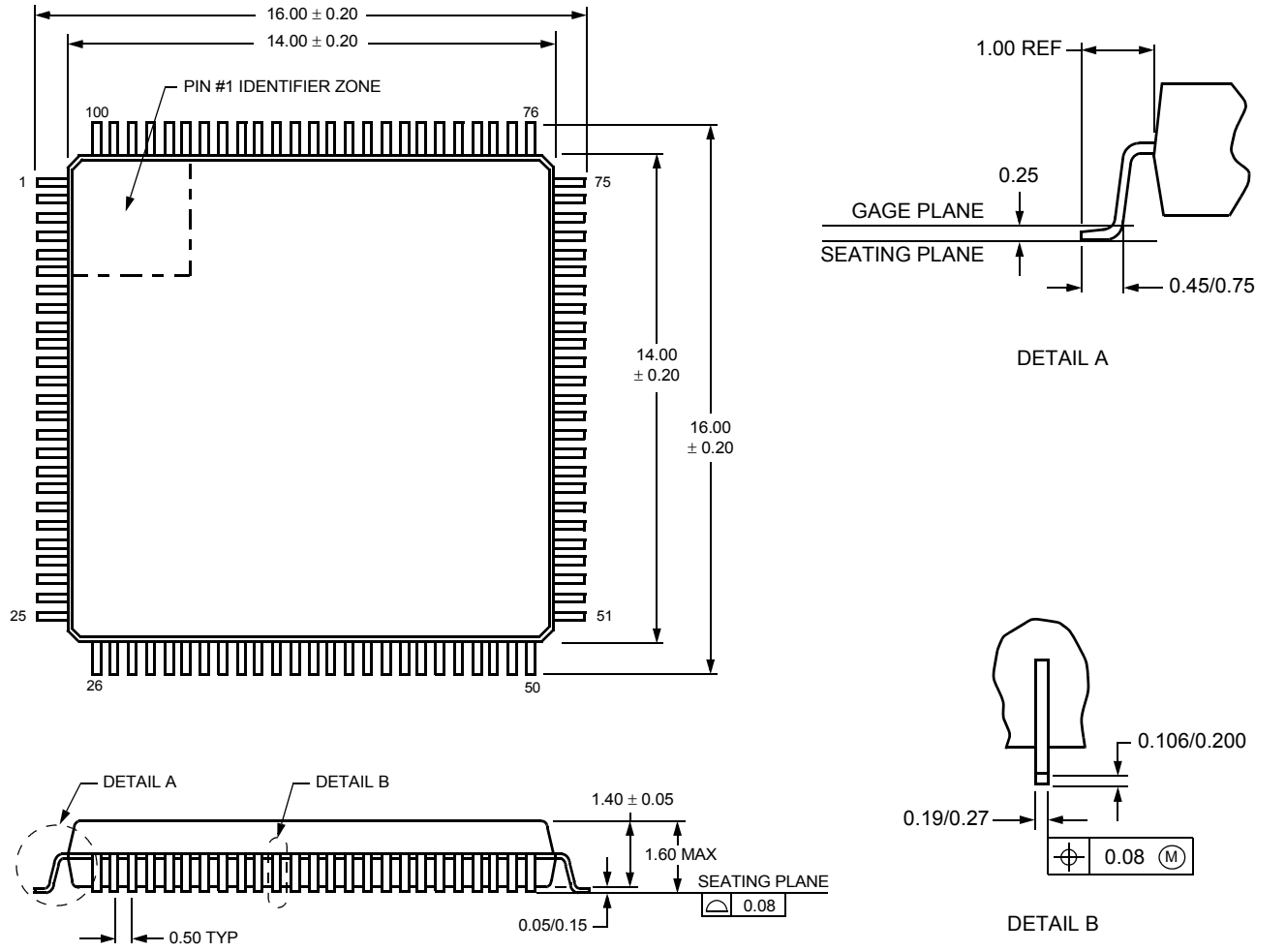
* Active-low signals within this document are indicated by an N following the symbol names.

Note: For those applications when one or more FW322 ports are not wired to a connector, those unused ports may be left unconnected without normal termination. When a port does not have a cable connected, internal connect-detect circuitry will keep the port in a disconnected state.

Outline Diagrams

100-Pin TQFP

Dimensions are in millimeters.



5-2146 (F)

Microsoft and *Windows* are registered trademarks of Microsoft Corporation.
The *FireWire* logo is a trademark and *MacOS* is a registered trademark of Apple Computer, Inc.
1394 is a trademark and *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
Mini PCI is a registered trademark of PCI-SIG, Inc.

For additional information, contact your Agere Systems Account Manager or the following:

INTERNET:	**http://www.agere.com**
E-MAIL:	**docmaster@agere.com**
N. AMERICA:	Agere Systems Inc., Lehigh Valley Central Campus, Room 10A-301C, 1110 American Parkway NE, Allentown, PA 18109-9138 **1-800-372-2447**, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA:	CHINA: **(86) 21-54614688** (Shanghai), **(86) 755-25881122** (Shenzhen) JAPAN: **(81) 3-5421-1600** (Tokyo), KOREA: **(82) 2-767-1850** (Seoul), SINGAPORE: **(65) 6778-8833**, TAIWAN: **(886) 2-2725-5858** (Taipei)
EUROPE:	**Tel. (44) 1344 296 400**

December 2004
PB05-005CMPR (Replaces PB04-086CMPR)