LXT1000

Gigabit Ethernet Transceiver

Datasheet

The LXT1000 transceiver supports Gigabit Ethernet over copper twisted-pair connections and supplies all of the physical layer (PHY) functions needed to interface a Gigabit Ethernet controller to a 100-meter CAT5 twisted-pair connection. The device incorporates Intel's high-efficiency Optimal Signal Processing (OSP™) technology, combining the best properties of digital and analog signal processing to produce a truly optimal device.

Featuring a GMII interface, 4DPAM5 encoder, scrambler, and 8B/10B encoder, Viterbi Decision Feedback Equalizer (DFE), DSP filtering for echo cancellation, equalization, and near- and far-end crosstalk elimination, as well as gain control and timing recovery, the LXT1000 also includes an internal hybrid circuit combining the transmit and receive paths on each pair, allowing simple 1:1 turns ratio magnetics. LXT1000 complies with applicable portions of 802.3.

Product Features

- IEEE 802.3ab compliant.
- GMII and Ten-Bit Interface (TBI) MAC interface configurations.
- Integrated 10/100 transceiver with fallback support.
- Provides 802.3ab auto-negotiation for resolution of Master/Slave and flow-control (802.3x).
- MII management, QuickStatus, 7 LEDs, Interrupt.
- Supports 10 KB Jumbo Frames (full duplex).
- Supports carrier extension and packet bursting (half duplex).
- JTAG support.
- 3.3V power supply.
- Packaging: 492-Lead PBGA.
- Commercial Temperature Range, 0-55° C.

Applications

- NICs
- Switches

Related Documents

- *LXT1000 Gigabit Ethernet Transceiver Design and Layout Guide*

As of January 15, 2001, this document replaces the Level One document *LXT1000 Gigabit Ethernet Transceiver*.

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Contents

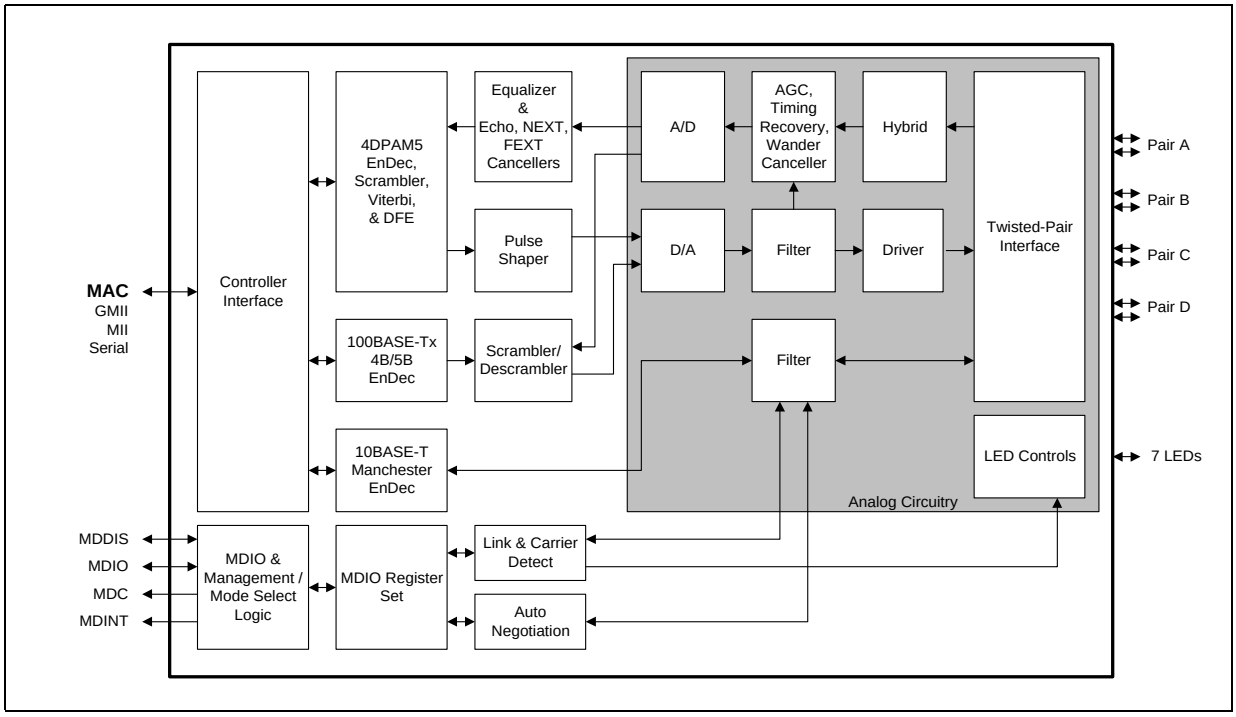
Figures

Tables

Revision History

Revision	Date	Page #	Description
002	July 2001	28	Add “Test Loopback” to the Functional Description section.
		71	Add footnote to Table 27 in the Applications Information section referring to return loss test conditions.
		75	Add a footnote to Table 29 and Table 30 in the Test Specifications section referring to LXT1000 Application Note Thermal Design Considerations Application Note for further detail.
		76	Changed Output Set-up Time and Output Hold Time values from Maximums to Minimums in Table 32.
		93	Add a footnote to Table 58 and Table 68 in the Register Set section referring to Auto-Negotiation and Registers 4 and 9.
		106	Add Appendix A, “Ordering Information”.

Figure 1. LXT1000 Block Diagram



1.0 Ball Assignments and Signal Descriptions

Figure 2. LXT1000 PBGA Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	A
B	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	rxd5	vccd	rxd7	vccd	gbias	gnd	rx_clk	gnd	gtx_clk	gnd	p/d	gnd	master	gnd	gnd	gnd	gnd	gnd	B
C	gnd	gnd	gnd	gnd	gnd	gnd	gnd	rxd3	gnd	rxd6	gnd	rx_dv	gnd	gbias	gnd	vccd	gnd	tx_er	gnd	txd7	gnd	qstat	gnd	gnd	gnd	gnd	C
D	gnd	gnd	gnd	p/d	gnd	p/d	rxd1	gnd	gbias	gnd	gbias	gbias	gnd	gnd	gnd	gnd	tx_clk	gnd	qclk	gnd	txd5	gnd	gnd	gnd	gnd	gnd	D
E	gnd	gnd	gnd	gnd	gnd	rxd0	vccd	rxd2	gnd	rxd4	gnd	gbias	rx_er	gnd	col	crs	gnd	tx_en	gnd	txd6	gnd	gnd	gnd	gnd	gnd	gnd	E
F	gnd	gnd	gnd	p/d	gnd	vccd	vccd	vccd	vccd	vccd							vccd	vccd	vccd	vccd	vccd	gnd	txd3	gnd	gnd	gnd	F
G	gnd	mdc	gnd	speed 0	gnd	vccd															vccd	txd4	gnd	gnd	gnd	gnd	G
H	gnd	gnd	speed 2	gnd	speed 1	vccd															vccd	gnd	txd2	gnd	gnd	gnd	H
J	gnd	p/d	gnd	gnd	mdio	vccd															vccd	txd1	gnd	txd0	gnd	gnd	J
K	gnd	gnd	mdint	gnd	an_en	vccd															vccd	gnd	nc2	gnd	gnd	gnd	K
L	gnd	an_rstrt	gnd	gnd	mddis						gnd	gnd	gnd	gnd	gnd	gnd						gnd	nc1	gnd	gnd	gnd	L
M	gnd	gnd	gnd	tms	gnd						gnd	gnd	gnd	gnd	gnd	gnd						ser10	gnd	anisol	gnd	gnd	M
N	gnd	gnd	tdi	gnd	tck						gnd	gnd	gnd	gnd	gnd	gnd						gnd	reset	gnd	gnd	gnd	N
P	gnd	trst	gnd	tdo	gnd						gnd	gnd	gnd	gnd	gnd	gnd						vcca	gnd	gnd	gnd	gnd	P
R	gnd	gnd	gnd	gnd	gnd						gnd	gnd	gnd	gnd	gnd	gnd						gnd	smart_spd	gnd	gnd	gnd	R
T	gnd	gnd	gnd	gnd	gnd						gnd	gnd	gnd	gnd	gnd	gnd						cross	vcca	gnd	gnd	gnd	T
U	gnd	gnd	gnd	ledl	ledt	vcca															vcca	pwrdwn	gnd	tbi	gnd	gnd	U
V	gnd	gnd	gnd	vcca	gnd	gnd															gnd	vcca	gnd	gnd	gnd	gnd	V
W	gnd	gnd	gnd	ledr	gnd	ledf															vcca	gnd	gnd	gnd	gnd	gnd	W
Y	gnd	gnd	gnd	gnd	vcca	leds															gnd	duplex/tx_tclkn	gnd	gnd	gnd	gnd	Y
AA	gnd	gnd	gnd	ledc	ledg	vcca	gnd	gnd	gnd	vcca							gnd	gnd	gnd	gnd	vcca	pause/tx_tclkp	gnd	xo	gnd	gnd	AA
AB	gnd	gnd	gnd	gnd	vcca	gnd	gnd	gnd	gnd	gnd	gnd	vcca	gnd	rbias	gnd	gnd	vcca	gnd	gnd	gnd	vcca	gnd	gnd	gnd	gnd	gnd	AB
AC	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	vcca	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	xi	gnd	gnd	gnd	AC
AD	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	vcca	vcca	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	AD
AE	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	vcca	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	AE
AF	gnd	gnd	gnd	vcca	tpap	tpan	vcca	vcca	tpbn	tpbp	vcca	gnd	gnd	gnd	vcca	tpcp	tpcn	vcca	vcca	tpdn	tpdp	vcca	gnd	gnd	gnd	gnd	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Table 1. Signal Type Abbreviations

Symbol	Signal Type	Definition
I	Input	Standard input-only signal.
LHR	Input Latched, L-H Reset	Latched on Low-to-High edge of RESET; ignored thereafter.
MD	Input, Latched, MDDIS	Latched on Low-to-High edge of RESET; used thereafter only if Manual Control mode (MDDIS) = 1.
O	Output	Standard output-only signal.
I/O	Bidirectional	Input and output signal.
A	Analog	Current source signal.
PD	Pull Down	Pull down signal. Tie Low.
PU	Pull Up	Pull up signal.
N/C	No Connect	Do not connect.

Table 2. LXT1000 GMII Signal Descriptions

Ball #	Symbol	Type[1]	Description
MAC Data Interface[2]- 1000/100/10 Operation			
C20 E20 D21 G22 F23 H23 J22 J24	TXD7 TXD6 TXD5 TXD4 TXD3 TXD2 TXD1 TXD0	I	**Transmit Data Bus**. The width of this synchronous input bus varies with the speed/ mode: 1000: All 8 bits are used. 100 or 10 MII: TXD<3:0> are used; TXD<7:4> are ignored. 10 Serial: TXD<0> is monitored; TXD<7:1> are ignored.
E18	TX_EN	I	**Transmit Enable.** This synchronous input indicates that valid data is being driven on the TXD bus.
D17	TX_CLK	O	**Transmit Clock**. All transmit inputs must be synchronized to this output clock during 10/100 operation. It is provided as a utility clock during 1000 operation. Its frequency depends on the link speed/mode: 100/1000 Mbps: 25 MHz 10 MII and Auto-negotiation: 2.5 MHz 10 Serial: 10 MHz
B17	GTX_CLK	I	**Gigabit Transmit Clock**. 125 MHz input clock; all transmit inputs must be synchronized to this clock during 1000 operation.
C18	TX_ER	I	**Transmit Coding Error.** This synchronous input causes the transmission of error symbols in 1000/100 links. For half-duplex 1000 links, it will cause the generation of carrier-extension symbols when properly synchronized with TX_EN (refer to 1000 Mbps operation section).

1. I/O Column Coding: I = Input, O = Output
2. Complies with IEEE 802.3, Clauses 35.(GMII) and 22 (MII); Modes 1000 (GMII), 100 (MII), 10 (MII or Serial), Auto-negotiation.
3. Complies with IEEE 802.3, Clause 36. NOTE: This section is an alternate listing of previously described pins.

Table 2. LXT1000 GMII Signal Descriptions (Continued)

Ball #	Symbol	Type[1]	Description
B11 C10 B9 E10 C8 E8 D7 E6	RXD7 RXD6 RXD5 RXD4 RXD3 RXD2 RXD1 RXD0	O	**Receive Data Bus**. The width of this synchronous output bus varies with speed/mode: 1000: All 8 bits are driven. 100 and 10 MII mode: RXD<3:0> are driven; RXD<7:4> are held Low. 10 Serial: RXD<0> is driven; RXD<7:1> are held Low.
C12	RX_DV	O	**Receive Data Valid.** This synchronous output is asserted when valid data is driven on RXD.
E13	RX_ER	O	**Receive Error**. For 1000 operation, this output is asserted when error symbols or carrier-extension symbols are received. For 100 operation, it is asserted when error symbols are received. For 10 operation, it is not asserted. It is always synchronous to RX_CLK.
B15	RX_CLK	O	**Receive Clock**. This output clock is used to synchronize the receive output signals. Its frequency depends upon the link speed: 1000: 125 MHz 100: 25 MHz (35/65 duty cycle) 10 MII or Auto-negotiation: 2.5 MHz 10 Serial: 10 MHz
E15	COL	O	**Collision.** This asynchronous output is asserted when a collision is detected (applies to half-duplex links only). In full-duplex mode, this output is forced Low.
E16	CRS	O	**Carrier Sense.** This asynchronous output is asserted when data is detected at the twisted-pair interface.
MAC Data Interface - TBI Configuration[3] - 1000-Only Operation			
C20, E20, D21, G22, F23, H23, J22, J24, E18, C18	TXD<9:0>	I	**Transmit Data Bus**. This input bus must be synchronized to GTX_CLK.
D17	TX_CLK	O	**Transmit Clock**. 25 MHz output. Not used; provided as a utility.
B17	GTX_CLK	I	**Gigabit Transmit Clock**. 125 MHz input clock
B11, C10, B9, E10, C8, E8, D7, E6, C12, E13	RXD<9:0>	O	**Receive Data Bus**. This output data bus is synchronized to RBC0/RBC1.
B15, E15	RBC0, RBC1	O	**Receive Clocks**. Two 62.5 MHz output clocks are provided at these outputs. RBC0 is 180 degrees (8 ns = 1/2 period delay) with respect to RBC1.
E16	COMDET	O	**Comma Detect**. Toggles when comma sequence is detected in the receive data stream.

1. I/O Column Coding: I = Input, O = Output
2. Complies with IEEE 802.3, Clauses 35.(GMII) and 22 (MII); Modes 1000 (GMII), 100 (MII), 10 (MII or Serial), Auto-negotiation.
3. Complies with IEEE 802.3, Clause 36. NOTE: This section is an alternate listing of previously described pins.

Table 2. LXT1000 GMII Signal Descriptions (Continued)

Ball #	Symbol	Type[1]	Description
GMII Control Interface			
G2	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 2.5 MHz.
J5	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for communication between the PHY and the management function.

1. I/O Column Coding: I = Input, O = Output
2. Complies with IEEE 802.3, Clauses 35.(GMII) and 22 (MII); Modes 1000 (GMII), 100 (MII), 10 (MII or Serial), Auto-negotiation.
3. Complies with IEEE 802.3, Clause 36. NOTE: This section is an alternate listing of previously described pins.

Table 3. LXT1000 Twisted-Pair Interface Signal Descriptions

Ball #	Symbol	Type[1]	Description
AF5, AF6, AF10,AF9 AF16,AF17, AF21, AF20	TPAP, TPAN TPBP, TPBN TPCP, TPCN TPDP, TPDN	I/O I/O I/O I/O	**Twisted-Pair A - D, Positive and Negative**. For 1000BASE-T operation, all four pair are both input and output at the same time. For 100BASE-TX and 10BASE-T operation, only TPAP/TPAN and TPBP/TPBN are used. The device automatically configures input and output pairs.

1. I/O Column Coding: I = Input, O = Output

Table 4. LXT1000 Configuration Signal Descriptions

Ball #	Symbol	Type[1]	Description[2]
H3 H5 G4	SPEED2 SPEED1 SPEED0	I, MD	**Speed Select.** These inputs determine the LXT1000's operating speed. When the MAC Interface is used in a TBI configuration, they must be set as follows: High, Low, Low (advertise 1000BASE-T only). When the MAC Interface is used in a GMII configuration, their function varies depending on whether auto-negotiation is enabled. When auto-negotiation is enabled, each signal, when High, enables advertising of a specific speed via the corresponding bits in the MII Registers: SPEED<2> = 1000 (9.9, 9.8) SPEED<1> = 100 (4.7, 4.8) SPEED<0> = 10 (4.5, 4.6) When auto-negotiation is disabled by tying AN_EN Low, SPEED<0> forces the speed via MII Bit 0.13 to either 10 (= 0) or 100 (=1). SPEED<2:1> should be tied Low.
K5	AN_EN	LHR	**Auto Negotiation Enable.** This input sets the power-on state of MII Register Bit 0.12, which controls Auto-Negotiation. Normally, this input should be tied High. When High, auto-negotiation is enabled. When Low, auto-negotiation is disabled.

1. I/O Column Coding: LHR = Input, Latched on Low-to-High edge of RESET (ignored thereafter); I, MD = Input, Latched on Low-to-High edge of RESET, used thereafter only if Manual Control mode (MDDIS = 1).
2. MAC Interface Operating modes: GMII (1000 Mbps), MII (10 or 100 Mbps), Serial (10 Mbps).

Table 4. LXT1000 Configuration Signal Descriptions (Continued)

Ball #	Symbol	Type[1]	Description[2]
Y22	DUPLEX/ TX_TCLKN	I, MD	**Duplex Mode.** When 21.15 = 0 (default), this input controls the duplex state of the link. Its exact function varies depending on the state of AN_EN. For TBI configurations, this input should be tied High. When AN_EN is High, this bit enables advertising of full-duplex capabilities. (Bits 9.9, 4.8, and 4.6 are set High if the corresponding SPEED is also High). When AN_EN is Low, this bit directly forces duplex state through MII bit 0.8; Low = half duplex; High = full duplex.
		O	**TX_TCLKN (Transmit Jitter Test Clock)**. The internal 125 MHz clock used to transmit data is output as a differential signal on Y22 and AA22 when 21.15 = 1.
L2	AN_RSTRT	I, MD	**Restart Auto Negotiation.** A positive edge on AN_RSTRT restarts the Auto-negotiation process. This signal controls the MII Control Register bit 0.9. AN_RSTRT is relevant only when AN_EN is High.
R23	SMART_SPD	LHR	**Smart Speed Select.** When High, this input enables SmartSpeed control. SMART_SPD drives bit 16.7 (see "SmartSpeed" on page 43).
AA22	PAUSE/ TX_TCLKP	I, MD	**Pause Configuration**. When 21.15 = 0 (default), this input determines the settings of Pause (4.10) and ASM_DIR (4.11) during auto-negotiation. If this input is High, both bits are set High; if Low, both are disabled.
		O	**TX_TCLKP (Transmit Jitter Test Clock)**. The internal 125 MHz clock used to transmit data is output as a differential signal on Y22 and AA22 when 21.15 = 1.
B21	MASTER	I, MD	**Master/Slave Configuration**. This configuration sets Port Type bit 9.10, which indicates the Gigabit Master/Slave configuration. The default configuration, bit 9.12, interprets this setting as the preferred, but not required, mode. High = Master (multi-port) configuration (Transmitter driven from local clock source). Low = Slave (single-port) configuration. (Transmitter driven from recovered clock).
T22	CROSS	I, MD	**Crossover Selection.** Determines TPAP/N and TPBP/N operation during auto-negotiation and 10/100 operation. Crossover Selection is not used during 1000 operation. When High, TPAP/N is an input; TPBP/N is an output (Switch configuration). When Low, TPAP/N is an output; TPBP/N is an input (NIC/DTE configuration). When set to mid-level voltage or left open, the device automatically determines correct operation. Changing the state of this input generates an internal reset, resulting in a new auto-negotiation cycle.
M24	ANISOL	LHR	**Auto Negotiate Isolate.** When ANISOL is High, the auto-negotiation isolate feature is enabled (refer to "Auto-Negotiate Isolation" on page 44). ANISOL drives 16.2.
M22	SER10	LHR	**Serial Mode.** Applies when the MAC interface is used in the GMII configuration. Determines how 10 Mbps links are handled and setting of bit 16.3: GMII Configuration: High = Serial mode (1 bit x 10 MHz) Low = MII mode (4 bits x 2.5 MHz). TBI Configuration: For TBI configuration, pull Low.
U24	TBI CONFIGURATION	LHR	**Ten-Bit Interface (TBI) Mode.** Determines MAC interface configuration and setting of bit 16.1. High = TBI Configuration Low = GMII configurations.

1. I/O Column Coding: LHR = Input, Latched on Low-to-High edge of RESET (ignored thereafter); I, MD = Input, Latched on Low-to-High edge of RESET, used thereafter only if Manual Control mode (MDDIS = 1).
2. MAC Interface Operating modes: GMII (1000 Mbps), MII (10 or 100 Mbps), Serial (10 Mbps).

Table 5. LXT1000 LED Indicator Configuration Signal Descriptions

Ball #	Symbol	Type[1]	Description
AA5	LEDG	I/O	**Gigabit LED.** This active High output is asserted when a Gigabit link is established. Pull Low through a resistor/LED. (Refer to "PHY Address Determination" on page 36.)
Y6	LEDS	I/O	**Speed LED.** This active high output is asserted when a 100 Mbps link is established. Pull Low through a resistor/LED. (Refer to "PHY Address Determination" on page 36.)
AA4	LEDC/ADD4	I/O[3]	**Collision LED[2].** After reset, this is a LED output indicating collision. The LXT1000 automatically determines whether this output is active High or active Low. In full-duplex Gigabit mode, the LEDC output goes active whenever packets are simultaneously transmitted and received. **MDIO Address 4.** During power-up or reset, this ball is read to determine bit 4 of the LXT1000's MDIO Address.
W6	LEDF/ADD3	I/O[3]	**Duplex LED[2].** After reset, this ball is a LED output indicating duplex state. The LXT1000 automatically determines whether this output is active High or active Low. **MDIO Address 3.** During power-up or reset, this ball is read to determine bit 3 of the LXT1000's MDIO Address.
W4	LEDR/ADD2	I/O	**Receive LED[2].** After reset, this LED output indicates receive activity at the twisted-pair (not indicated in Loopback operation). The LXT1000 automatically determines whether this output is active High or active Low. **MDIO Address 2.** During power-up or reset, this ball is read to determine bit 2 of the LXT1000's MDIO Address.
U5	LEDT/ADD1	I/O	**Transmit LED[2].** After reset, this ball is an LED output indicating transmit activity at the twisted-pair (not indicated in Loopback operation). The LXT1000 automatically determines whether this output is active High or active Low. **MDIO Address 1.** During power-up or reset, this ball is read to determine bit 1 of the LXT1000's MDIO Address.
U4	LEDL/ADD0	I/O	**Link LED[2].** After reset, this ball is an LED output indicating link establishment at any speed. The LXT1000 automatically determines whether this output is active High or active Low. **MDIO Address 0.** During power-up or reset, this ball is read to determine bit 0 of the LXT1000's MDIO Address.

1. I/O Column Coding: I = Input, O = Output.
2. Polarity of LEDs is automatically set during the initial configuration.
3. The Input function, however, is not used.

Table 6. LXT1000 Miscellaneous Signal Descriptions

Ball #	Symbol	Type[1]	Description
C22	QSTAT	O, PU	**Quick Chip Status.** Link-state monitoring. See Section 2.3.8, "Quick Status Interface" on page 34.
D19	QCLK	I	**Quick Clock.** Clock input used for QSTAT feature. Maximum frequency is 25 MHz. (There is no minimum.)
L5	MDDIS	I	**Management Disable**. When MDDIS is High, read and write operations on the MDIO are disabled and most hardware control balls have continuous control over their respective functions (some balls are read only at reset or power-up). When MDDIS is Low, the MDIO supports read and write operations, and hardware control balls establish only the initial values of their respective functions.
K3	MDINT	O	**Management Data Interrupt**. When bit 18.1 = 1, an Active Low output indicates status change. Interrupt is cleared by reading Register 19.
AC23 AA24,	XI XO	I O	**Crystal Input and Output**. A 25 MHz clock must be supplied at this input, either by placing a 25 MHz crystal across XI and XO, or by driving a 25 MHz signal directly into XI. Refer to Functional Description on page 20 for detailed requirements.
AB14	RBIAS	AI	**Bias Control.** A 10.7 kΩ, 1% resistor must be tied from this ball to ground.
D9, D11, D12, E12, C14, B13	GBIAS	AI	**GMII Bias.** Tie these balls together, and then to the anode of a 0.1 µf capacitor. Tie the cathode of the capacitor to ground.
N23	RESET	I	**Reset.** This active Low input is OR'ed with the control register Reset bit (0.15). The LXT1000 reset cycle is extended 258 µs (nominal) after Reset is de-asserted. The transmitter is held disabled until the transmit clock frequency is within specification.
U22	PWRDWN	I	**Power Down.** When High, PWRDWN forces the LXT1000 into hardware power down mode, de-activating all functions and interfaces. This ball is OR'ed with the Power Down bit 0.11.
Pull Down (P/D)			
F4	P/D	-	**Pull-down.** Tie Low. ***Note:*** Tie independently to ground or through its own resistor.
J2	P/D	-	**Pull-down.** Tie Low.
B19	P/D	-	**Pull-down.** Tie Low.
D6	P/D	-	**Pull-down.** Tie Low.
D4	P/D	-	**Pull-down.** Tie Low.
No Connect (N/C)			
L23	N/C1	-	**No Connect.** Let ball float; do not connect to anything.
K23	N/C2	-	**No Connect.** Let ball float; do not connect to anything.
1. I/O Column Coding: I = Input, O = Output, A = Analog, PU = Pull Up (Internal)			

Table 7. LXT1000 Boundary Scan Signal Descriptions

Ball #	Name	I/O	Description
N5	TCK	I	**Test Clock.** Test clock input sourced by the ATE.
N3	TDI	I	**Test Data Input.** Test data sampled with respect to the rising edge of TCK.
P4	TDO	O	**Test Data Output.** Test data driven with respect to the falling edge of TCK.
M4	TMS	I	**Test Mode Select.**
P2	TRST	I	**Test Mode Reset.**
1. I/O Column Coding: I = Input, O = Output			

Table 8. LXT1000 Power Supply Signal Descriptions

Ball #	Name	I/O	Description
U6, U21, V4, V22, W21, Y5, AA6, AA10, AA21, AB5, AB12, AB17, AB21, AC13, AD13, AD14, AE13, AF4, AF7:8, AF11, AF15, AF18, AF19, AF22, P22, T23	VCCA	-	**Analog Power Supply** (+3.3V)
B10, B12, C16, E7, F6:10, F17:21, G6, G21, H6, H21, J6, J21, K6, K21	VCCD	-	**Digital Power Supply** (+3.3V)
A1:26, B1:8, 14, 16, 18, 20, B22:26, C1:7, 9, 11, 13, C15, 17, 19, 21, 23:26 D1:3, 5, 8, 10,13:16, 18, D20, 22:26 E1:5, 9, 11, 14, 17, 19, E21:26 F1:3, 5, 22, 24:26 G1, 3, 5, 23:26 H1, 2, 4, 22, 24:26 J1, 3, 4, 23, 25, 26 K1,2,4, 22, 24:26 L1, 3, 4, 11:16, 22, 24:26 M1:3, 5, 11:16, 23, 25, 26 N1, 2, 4, 11:16, 22, 24:26 P1, 3, 5, 11:16, 23:26 R1:5, 11:16, 22, 24:26 T1:5,11:16, 24:26 U1:3, 23, 25, 26 V1:3, 5, 6, 21, 23:26 W1:3, 5, 22:26 Y1:4, 21, 23:26 AA1:3, 7:9, 17:20, 23, 25, AA26 AB1:4, 6:11, 13, 15:16, AB18:20, 22:26 AC1:12,14:22, 24:26 AD1:12, 15:26 AE1:12, 14:26 AF1:3, 12:14, 23:26	GND	-	**Ground**

2.0 Functional Description

2.1 Introduction

The LXT1000 is an IEEE 802.3-compliant transceiver for Gigabit Ethernet over copper twisted-pair connections. The LXT1000 supplies all of the physical layer (PHY) functions needed to interface a Gigabit Ethernet controller to a 100-meter CAT5 twisted-pair connection. The following paragraphs introduce the functional description sections that follow.

2.1.1 Network Interface

The LXT1000 uses a single, common network interface to support 1000BASE-T, 100BASE-TX, and 10BASE-T. This physical interface consists of four signal pairs that are used for 1000 Mbps transmission. (Only two pairs are needed for 10/100 Mbps.) Each signal pair consists of two bidirectional balls that transmit and receive at the same time. Crossover Control allows the twisted-pair interface to be configured for switch or DTE/NIC applications. Automatic Crossover Detection allows the LXT1000 to automatically detect which pair is transmit and which pair is receive and configure itself accordingly. (See “Interface Descriptions” on page 24.)

2.1.2 MAC Interface

The LXT1000 Media Access Controller (MAC) Interface supports several industry standards, which facilitate system integration. This interface has two basic configurations, one of which must be chosen as part of the basic design. See “MAC Data Interface” on page 25 for a more complete discussion.

GMII Configuration (1000/100/10)

This configuration complies with the IEEE 802.3 standard, Clause 35, intended for “copper” applications. It provides support for 1000BASE-T links, with fallback to 10/100 operation. For 10/100 operation, the interface defaults to an MII interface, complying with Clause 22 of the standard. For 10M operation, a serial option is also available.

TBI Configuration (1000 only)

This configuration complies with the IEEE 802.3 standard, Clause 36, and is intended to interface to Gigabit MACs originally developed for fiber applications. It supports 1000M-only operation.

2.1.3 MDIO/MDC Interface (Management)

The LXT1000 provides the IEEE-compliant Management Data Input/Output (MDIO) Interface, which allows upper-layer devices to monitor and control the state of the LXT1000. See “MDIO/MDC Management Interface” on page 31.

2.1.4 Hardware Control Interface

The LXT1000 is configurable at power up or hardware reset. Configuration options and operational settings of the device include such variables as link establishment, MAC interface operation and control, and physical address of the device. See “Hardware Control Interface” on page 33.

2.1.5 JTAG Boundary Scan Interface

The LXT1000 includes an IEEE JTAG1149.1 boundary scan test port for board level testing.

2.1.6 Initialization

Re-initialization and re-configuration functions are identical for power-up and hardware reset. (An external hardware reset circuit is not required.)

2.1.7 Link

The LXT1000 continuously monitors link state, and indicates to upper management the state (up or down), speed (1000, 100, 10), and duplex state (full, half) of the link.

2.1.8 Auto Negotiation

The LXT1000 provides full IEEE 802.3ab-compliant auto-negotiation, with automatic next-page generation. It also provides an option for manual next-page generation.

2.2 LXT1000 Applications

The LXT1000 supports NIC and switch applications. It provides half- and full-duplex operation at 1000 Mbps, 100 Mbps and 10 Mbps. Refer to Figure 3 for typical applications and Figure 4, which shows the LXT1000 Block Diagram.

Figure 3. LXT1000 Applications

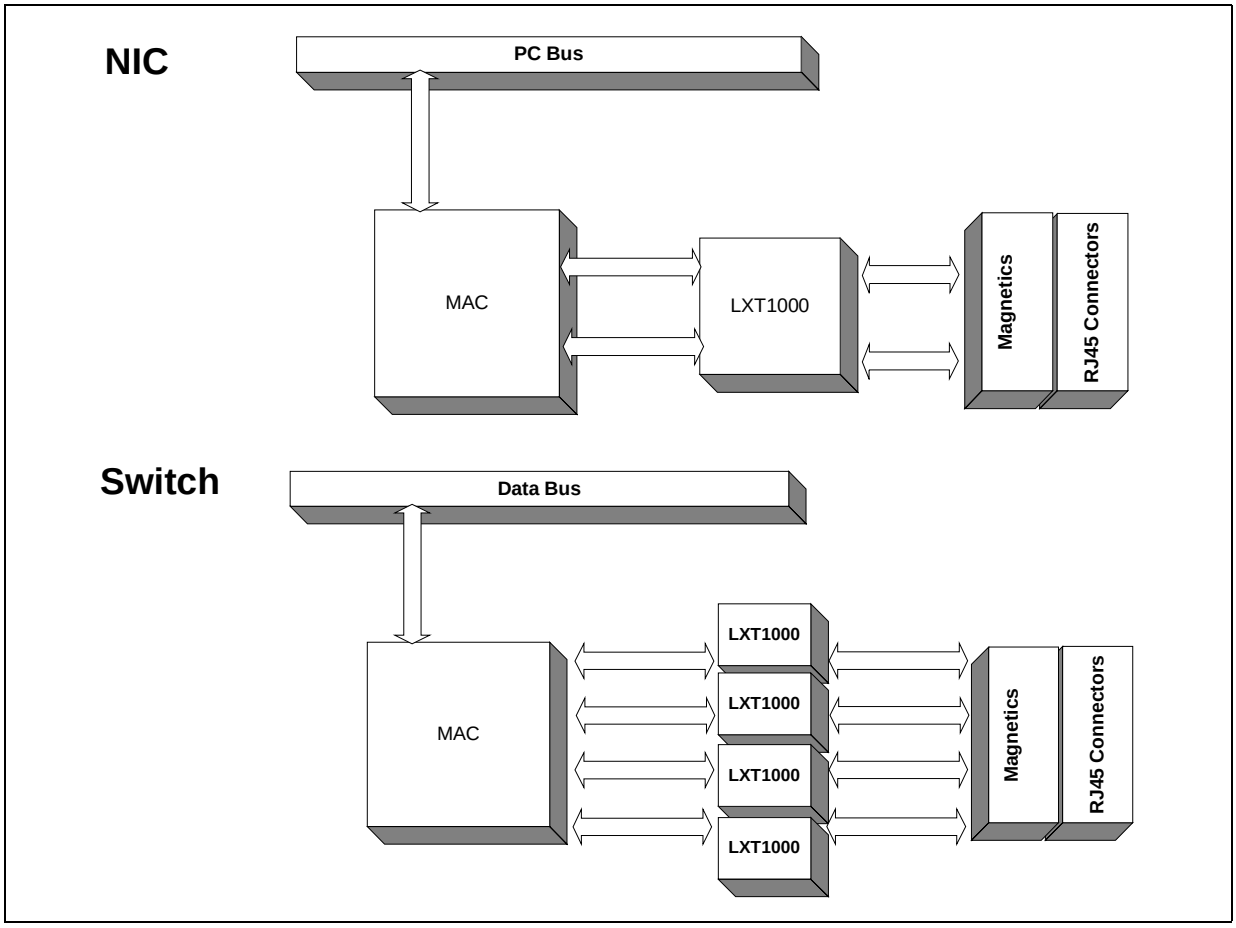
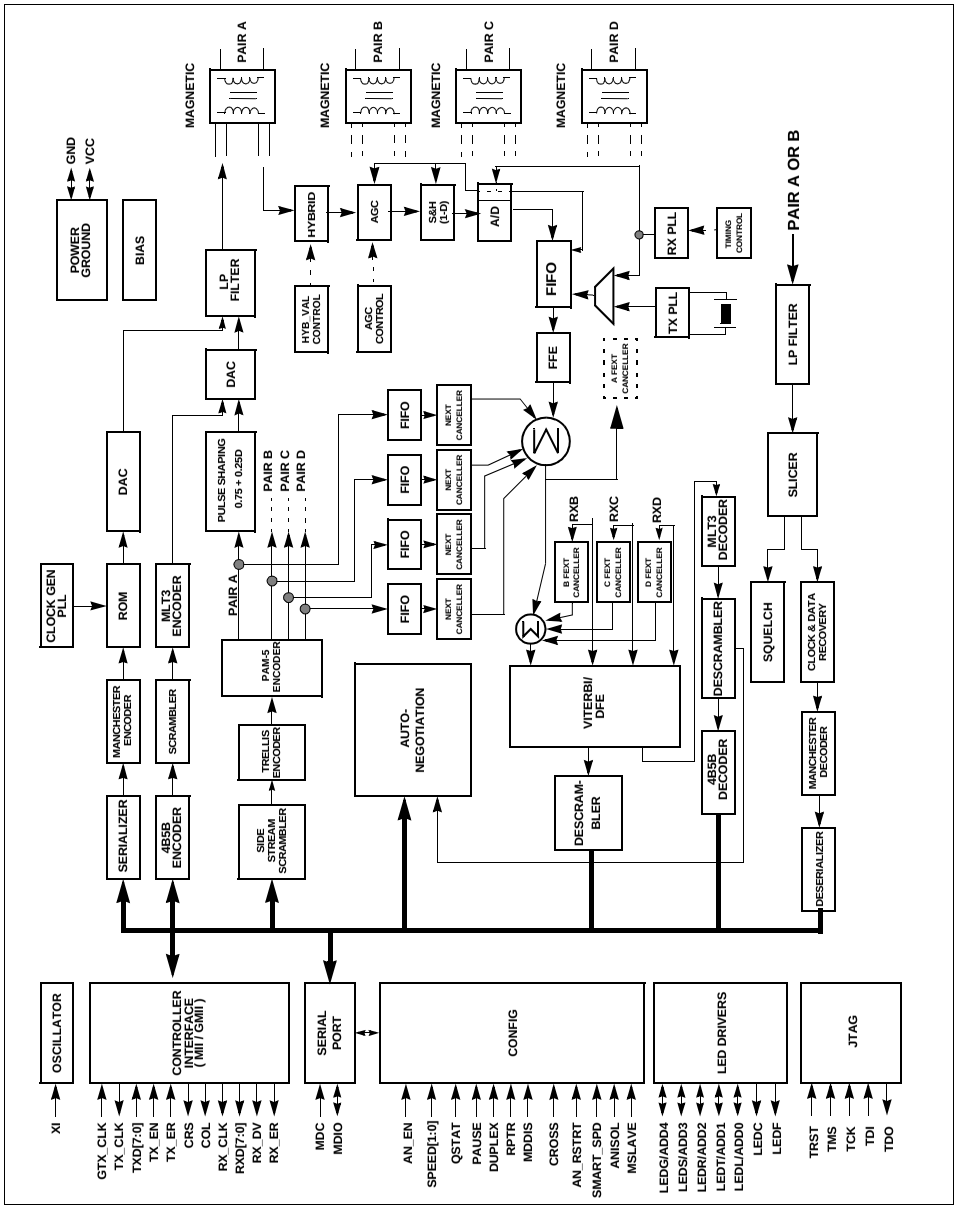


Figure 4. LXT1000 Block Diagram



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2.3 Interface Descriptions

2.3.1 Network Interface

The LXT1000 uses a single common network interface to support 1000BASE-T, 100BASE-TX, and 10BASE-T. This interface consists of four signal pairs—A, B, C, and D. Each signal pair consists of two bidirectional balls that can transmit and receive at the same time. The network physical interface consists of passive devices and magnetics. For 1000BASE-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used. Table 9 shows the mapping between the pairs and the RJ-45 signals. Refer to "Application Information" on page 66 for more details.

Table 9. Mapping of Twisted-Pair Outputs to RJ-45s

Pair	RJ-45s
A	1 and 2
B	3 and 6
C	4 and 5
D	7 and 8

2.3.1.1 MDI/MDIX Configuration

For 1000BASE-T links, pair identification is determined automatically in accordance with the standard.

The LXT1000 has an Automatic Crossover Detection function. If the crossover ball is left open, the LXT1000 automatically detects which application is being used and configures itself accordingly. If the CROSS ball is tied Low, the LXT1000 configures itself as a classic MDI (DTE/NIC) device with Pair A as transmit and pair B as receive. If the CROSS ball is tied High, the LXT1000 configures itself as an MDIX device (repeater/switch), with Pair B as transmit and Pair A as receive (refer to Figure 5 and Table 10).

Figure 5. Crossover Function

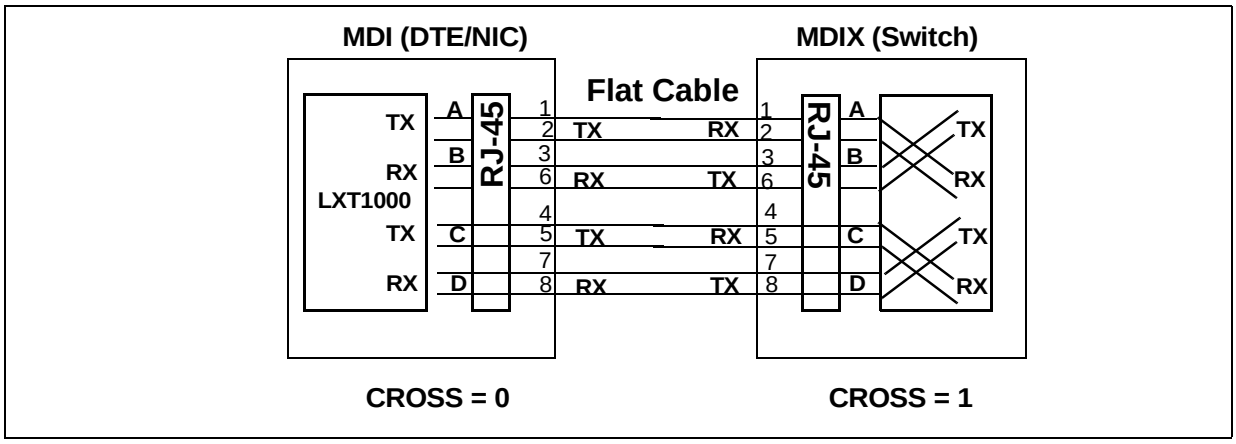


Table 10. Crossover Control and Automatic Detection

Crossover Input	Application	Transmit Pair	Receive Pair
CROSS = Low	DTE/NIC	Pair A - 1, 2	Pair B -3, 6
CROSS = High	Switch	Pair B - 3, 6	Pair A -1, 2
CROSS = Open	Automatic	Configured Accordingly	

2.3.2 MAC Data Interface

The MAC Data Interface has two basic configurations as selected by the TBI configuration pin:

- GMII - supports 1000/100/10 links (TBI Configuration = Low)
- TBI - supports 1000 only links (TBI Configuration = High)

2.3.2.1 Modes of Operation

For the GMII configuration, the interface varies according to the speed of the link:

- 1000 - GMII interface. 8 bits x 125 MHz
- 100 - MII interface. 4 bits x 25 MHz
- 10 - MII (4 bits x 2.5 MHz) or Serial (1bit x 10 MHz) as selected by the SER10 configuration ball.

For the TBI Configuration, the interface is 10 bits x 125 MHz (supports 1000 only).

When no link is established (during auto-negotiation), clocks on the interface operate the same as they do for the 10M MII mode.

Table 11. MAC Interface Modes of Operation

Configuration/ Purpose	Speed	Mode/Standard	Width	How selected
GMII Copper MACs	1000	GMII (IEEE 802.3, Ch. 35)	8 Bits x 125 MHz	TBI = Low
	100	MII (IEEE 802.3, Ch. 22)	4 Bits x 25 MHz	
	10	MII (IEEE 802.3, Ch. 22)	4 Bits x 2.5 MHz	TBI, SER10 = Low
		Serial (No standard)	1 Bit x 10 MHz	TBI = Low, SER10 = High
TBI Fiber “802.3z” MACs	1000	TBI (IEEE 802.3, Ch. 36)	10 Bits x 125 MHz	TBI = High

Table 12. MAC Interface Transmit Signal Mapping

MAC Interface Ball #	GMII				TBI
	1000BASE-T GMII Mode (8B)	100BASE-TX MII Mode (4B)	10BASE-T MII (4B)	10BASE-T Serial (1B)	1000BASE-T TBI Mode (10B)
D17	25 MHz ref.	TX_CLK			-
B17	GTX_CLK	Ignored			REFCLK
C18	TX_ER		Ignored		TXD<9>
E18	TX_EN				TXD<8>
C20	TXD<7>	Ignored			TXD<7>
E20	TXD<6>	Ignored			TXD<6>
D21	TXD<5>	Ignored			TXD<5>
G22	TXD<4>	Ignored			TXD<4>
F23	TXD<3>			Ignored	TXD<3>
H23	TXD<2>			Ignored	TXD<2>
J22	TXD<1>			Ignored	TXD<1>
J24	TXD<0>			TXD	TXD<0>

Table 13. MAC Interface Receive Signal Mapping

	GMII				TBI
MAC Interface Ball #	1000BASE-T GMII Mode (8B)	100BASE-TX MII Mode (4B)	10BASE-T MII (4B)	10BASE-T Serial (1B)	1000BASE-T TBI Mode (10B)
E15	COL				RBC1
E16	CRS				COMDET
B15	RX_CLK				RBC0
E13	RX_ER		No Function		RXD<9>
C12	RX_DV				RXD<8>
B11	RXD<7>	Held Low			RXD<7>
C10	RXD<6>	Held Low			RXD<6>
B9	RXD<5>	Held Low			RXD<5>
E10	RXD<4>	Held Low			RXD<4>
C8	RXD<3>			Held Low	RXD<3>
E8	RXD<2>			Held Low	RXD<2>
D7	RXD<1>			Held Low	RXD<1>
E6	RXD<0>			RXD	RXD<0>

2.3.2.2 GMII Mode (1000 BASE-T)

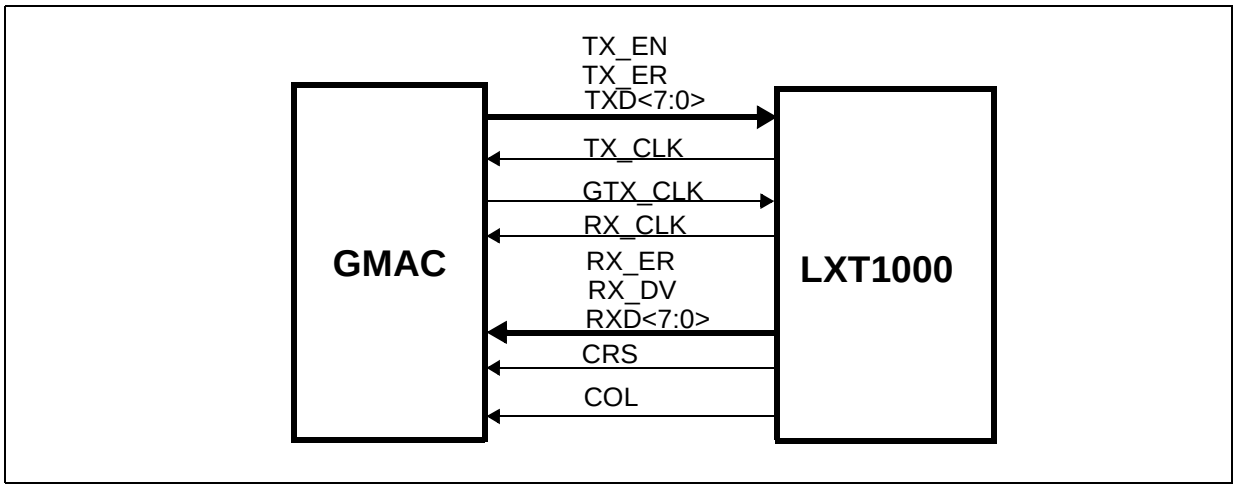
In GMII Mode, the LXT1000 supplies the following:

- RX_CLK (125 MHz)
- Eight receive data bits
- Carrier sense
- Collision detect
- Receive error signal

The MAC supplies a 125 MHz GTX clock, eight transmit data bits, and a transmit error signal. In the GMII mode, the LXT1000 drives a 25 MHz reference clock on its TX_CLK output ball for use, such as the MAC state machines. See Figure 6, which shows a GMII configuration.

The GMII mode supports carrier extension and packet concatenation in both the transmit and receive directions. These functions are enabled through the TX_ER and RX_ER balls. Refer to "1000 Mbps Operation" on page 46.

Figure 6. GMII Data Interface



2.3.2.3 MII Mode (10/100BASE-T)

The MII mode provides fallback support for 10/100 links when the GMII configuration of the MAC interface is selected. In this mode, the LXT1000 provides four receive data bits, 25 or 2.5 MHz transmit and receive clocks, and an error flag for received data. It also provides a carrier sense signal and a collision detect signal. The LXT1000 drives unused balls on the receive bus to ground. The transmit clock is driven on the TX_CLK ball, and GTX_CLK is ignored and can be left open. The MAC drives four transmit data bits and a transmit error ball.

2.3.2.4 Serial Mode (10BASE-T)

The Serial 10M mode supports legacy MACs when the link speed falls back to 10 Mbps. This mode is selected by setting the SER10 input High (otherwise MII mode is chosen for 10 operation), and is only available when the GMII configuration of the MAC interface is selected. The interface consists of a single data bit in each direction, 10 MHz transmit and receive clocks driven by the LXT1000, carrier sense, and collision detect (see Figure 7).

The relationship between 10 Mbps Serial Interface and the 10 Mbps MII Interface is shown in Figure 8.

Figure 7. Serial Interface

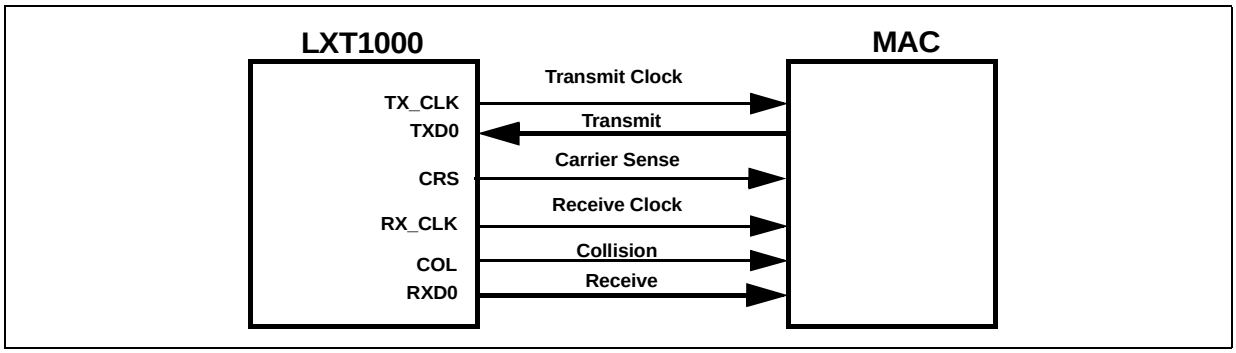
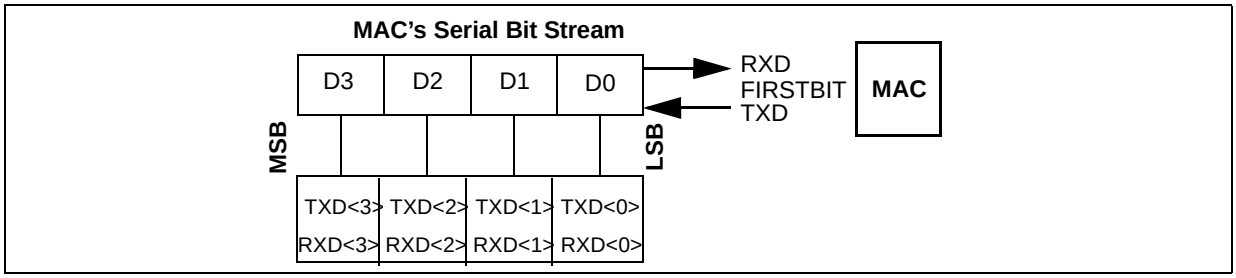


Figure 8. Relationship between 10 Mbps Serial Interface and 10 Mbps MII Interface



2.3.2.5 Test Loopback

During test loopback the twisted-pair interface is disabled, and data transmitted by the MAC is internally looped back by the LXT1000 and returned to the MAC. Test loopback is available for 10 Mbps, 100 Mbps, and 1000 Mbps modes of operation. The desired mode of operation for test loopback is enabled by setting the following register address bits as shown in Table 14 for each mode.

Table 14. Test Loopback Operation

Mode of Operation	Bit					
	16.14	0.14	0.13	0.12	0.8	0.6
10 Mbps	0	1	0	0	1	0
100 Mbps	0	1	1	0	1	0
1000 Mbps	1	1	0	0	1	1

2.3.3 TBI Configuration (1000BASE-T Only)

The LXT1000 provides a Ten-Bit Interface (TBI) for applications where a 1000BASE-T copper interface needs to be integrated with a MAC originally designed for Gigabit-Ethernet over fiber applications (1000BASE-LX/SX). In this mode, the LXT1000 drives the following:

- 10-bit-wide data bus
- COMDET signal

- Two 62.5 MHz clock (RBC0 and RBC1) in the receive direction
- 10-bit-wide interface
- 125 MHz clock on the GTX_CLK pin in the transmit direction

The LXT1000's TBI Mode does not support the signals SIGDET, EN_WRAP, or EN_COMDET.

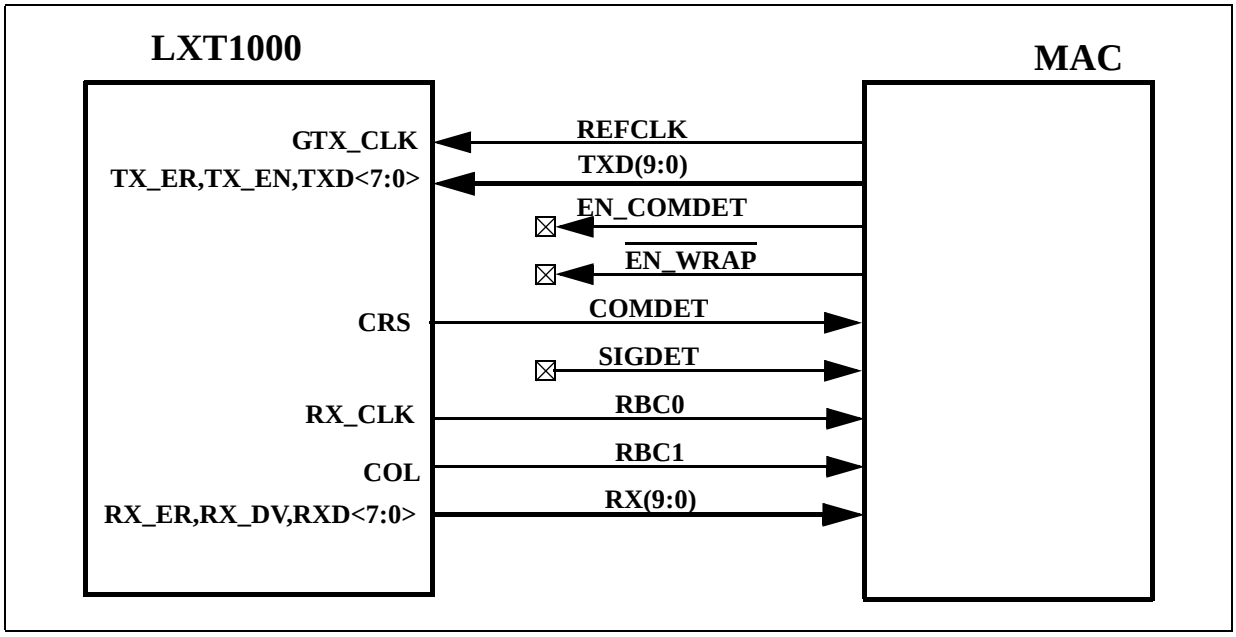
All 10-bit I/Os are multiplexed onto the GMII lines as shown in Table 12 and Table 13. The 10-Bit Interface is configured via the TENBIT pin.

When using this mode, the LXT1000 must be configured as shown below:

- AN_EN set High
- DUPLEX set High
- SPEED<2:0> set High, Low, Low, respectively

MAC auto-negotiation functions should be disabled. The MAC determines link status and its partners abilities via the MDIO interface and the LXT1000 MII Registers.

Figure 9. 10-Bit Interface (TBI)

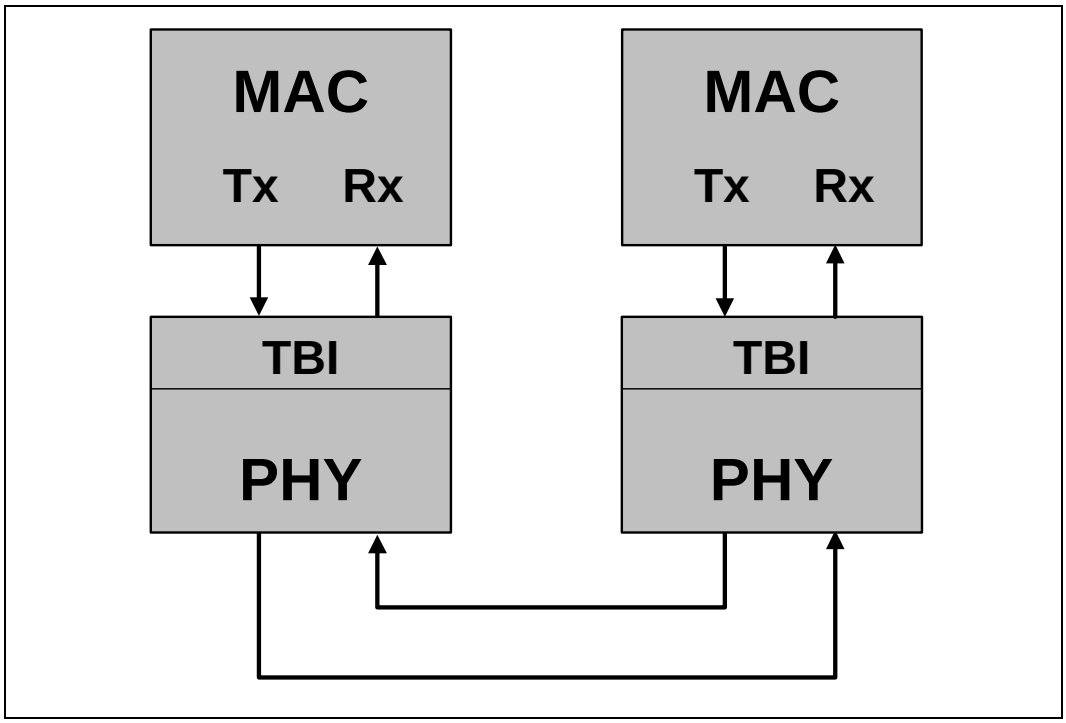


2.3.4 TBI Communication Between MAC and PHY

The Ten-Bit Interface (TBI) is included in the IEEE 802.3z specification and was developed to operate over fiber media. When used to operate over twisted-pair media, TBI displays inconsistencies between the IEEE 802.3z and IEEE 802.3ab specifications. For example, the physical- coding sublayer (PCS) appends a single, additional /R/ to the code-group stream to ensure that the subsequent /I/ is aligned on an even-numbered, code-group boundary for data transmission from the PHY to the MAC. (See IEEE 802.3z Clause 36.2.4.15.1 for more information.) This action results in the addition of a one-byte carrier extend, which the MAC may interpret as an error in approximately half of the transmitted frames.

Figure 10 shows the direction of data flow between the MAC and PHY. Transmit data traffic is data transmitted from the MAC through the PHY and onto the twisted-pair. Receive data traffic is data received from on the twisted-pair to the PHY and passed on to the receiving MAC.

Figure 10. Data Flow Between PHY and Mac



2.3.4.1 Transmit Mode – Data Traffic from MAC to PHY

Each frame transmitted from the MAC to the PHY begins on an arbitrarily designated even byte, and each byte thereafter alternates between odd and even. In full duplex operation, the MAC appends a single additional /R/ code group to the code-group stream to ensure that the subsequent /I/ is aligned on an even-numbered code-group boundary and the end-of-packet delimiter is complete according IEEE 802.3z Clause 36.2.4.14.1 (i.e., frames must end on an odd byte and the next even byte starts the subsequent /I/).

2.3.4.1.1 Frames Ending on an Even Byte

The PHY interprets the frames correctly but must realign itself so that they end on an even code group. When the PHY resets or realigns, it changes the even and odd byte designations. The data are then serialized and passed onto the twisted-pair for transmission.

2.3.4.1.2 Frames Ending on an Odd Byte

Frames that end on an odd byte comply with the IEEE 802.3z standard and are transmitted from the MAC to the PHY without additional byte assertion. The data are then serialized and passed onto the twisted-pair for transmission to the receiving device.

2.3.4.2 Receive Mode – Data Traffic from PHY to MAC

The MAC receives encapsulated data from the PHY-TBI interface according to the IEEE 802.3z specification. The PHY appends a single, additional /R/ to the code-group stream to all frames that end in an even byte. This action ensures that the subsequent /I/ is aligned on an even-numbered code-group boundary for data transmission from the PHY to the MAC and results in the addition of a one-byte carrier extend.

2.3.5 MAC Data Interface Control

The MAC Interface can be controlled via Tristate Condition and Auto-Negotiation Isolation:

- **Tri-state Condition.** Setting the Isolate Bit (0.10 = 1) forces the LXT1000 to tri-state all the MAC Interface signals that it drives, including TX_CLK and RX_CLK. In this mode, the MDIO and MDINT outputs are not tri-stated, so that the LXT1000 can continue to respond to MAC management requests and send interrupts.
- **Auto-Negotiation Isolation.** If the Auto-Negotiation Isolation feature is enabled (via Bit 16.2 = 1), the LXT1000 disables the MAC Interface when the link drops and then re-negotiates to a different speed. The LXT1000 holds all data transfers to/from the MAC until the MAC writes bit 16.2 = 0. (Refer to “Auto-Negotiate Isolation” on page 44.)

2.3.6 MDIO/MDC Management Interface

The LXT1000 supports the IEEE compliant Management Data Input/Output (MDIO) Interface, which allows the MAC or management control function to manage the LXT1000 by accessing its internal control and status registers (herein referred to as the “MII Registers”).

The MII register set is a block of 32 registers, each 16 bits wide. The MDIO interface provides access to individual registers within the set. Certain registers are defined by the IEEE 802.3 and are required for compliance (0-10, 15). Other registers are left open for vendor-specific implementation. The LXT1000 implements all the required registers, and additional registers (16-21) for device-specific enhancements.

The basic physical interface consists of two signals: the bidirectional data line (MDIO) and a clock line (MDC), driven by the MAC or management function. This interface allows the MAC to manage up to 32 PHYs. All transfers are initiated by the MAC. The MDIO protocol provides both read and write operations (see Figure 11 and Figure 12). During a write operation, the MAC drives the MDIO line for the entire frame. For a read operation, a turn-around time is inserted in the frame to allow the PHY to drive data back to the MAC. The LXT1000 supports a maximum frequency on MDC of 2.5 MHz.

The MDIO frame structure starts with a 32-bit preamble, which is required by the LXT1000. It includes a start-of-frame marker, an op-code, a 10-bit address field, and a 16-bit data field. The address field is divided into two 5-bit segments. The first segment identifies the PHY and the second identifies the register being accessed. The PHY address that the LXT1000 responds to is configured via the Hardware Control Interface (refer to “PHY Address Determination” on page 36).

The LXT1000 provides two enhancements to the basic MDIO interface: a disable function and an external interrupt. The MDDIS input controls MDIO interface operation. Pulling MDDIS High disables read and write operations on the MDIO. When pulled Low, both read and write operations are allowed.

Figure 11. MDIO Read Frame Format

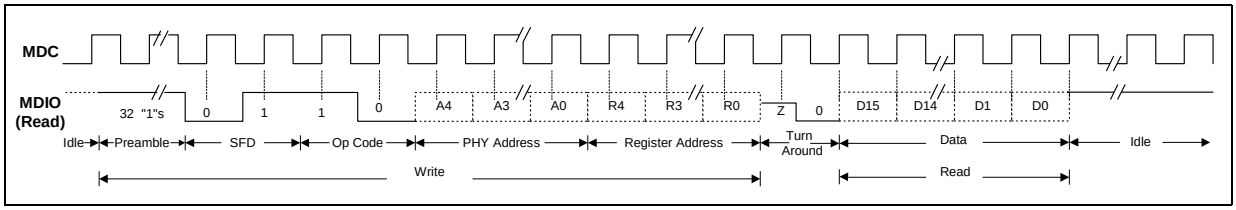
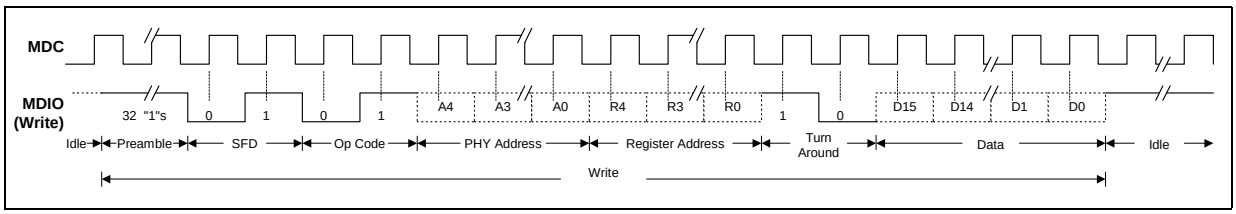


Figure 12. MDIO Write Frame Format



2.3.6.1 Interrupts

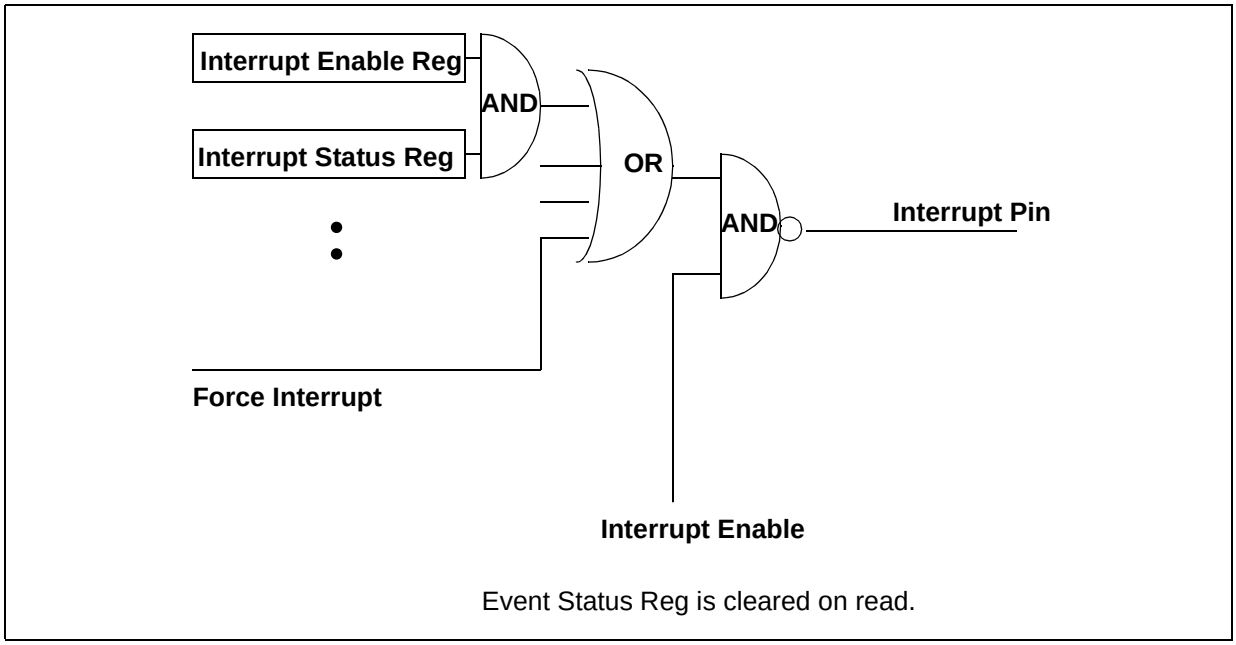
The LXT1000 signals an interrupt using the MDINT signal as shown in Figure 13. The Interrupt Enable Register (Register 18) enables the Interrupt, and the Interrupt Status Register (Register 19) identifies the Interrupt.

The LXT1000 drives active Low signal on the MDINT ball when there is an interrupt pending, which is indicated by the Interrupt Status Register bit (19.2).

2.3.6.1.1 Interrupt Options

- Speed
- Link Status
- Duplex Status
- Isolate Status
- Crossover Status
- Polarity
- Smartspeed Select
- Error Counters Full
- Auto-negotiation

Figure 13. Interrupt Handling



2.3.7 Hardware Control Interface

Configuration options and operational settings of the device include such variables as link establishment, MAC interface operation and control, and physical address of the device. Individual chip addressing allows multiple LXT1000 devices to share the GMII in either mode. Table 15 lists all hardware selectable configurations. Some configuration bits are read only at hardware reset.

For hardware-only applications, the Hardware Control Interface provides continuous control of the LXT1000. This mode is selected by driving the MDDIS input High.

In this setting, read and write operations on the MDIO interface are disabled; use is solely monitoring applications.

For software or MAC-managed applications, the Hardware Control Interface provides initial settings of the MII Register bits. This mode is selected by driving MDDIS Low.

Table 15. Configuring the LXT1000 via Hardware Control Interface

Desired Configuration	Hardware Settings
Link Configurations	
A/N to any speed, duplex	Speed <2:0> = 111, AN_EN = High, Duplex = High
A/N to Gigabit-only, full or half duplex	Speed <2:0> = 100, AN_EN = High, Duplex = High
A/N to Gigabit, half duplex only	Speed <2:0> = 100, AN_EN = High, Duplex = Low
Master/Slave Configurations[1]	
Multi-port Device (Master preferred)	MASTER = High
Single-port Device (Slave preferred)	MASTER = Low
Pause/ASM Pause[2]	
Enable Pause / ASM Pause	PAUSE = High
Disable Pause / ASM Pause	PAUSE = Low
PHY MDIO Address	
PHY MDIO Address	Set via ADD balls (shared with LED balls)
MAC Configuration	
GMII Configuration (1000/100/10)	TENBIT = Low
TBI Configuration (1000 only)	TENBIT = High
Select MII mode for 10 Mbps links	SER10 = Low
Select Serial mode for 10 Mbps links	SER10 = High
Advanced Functions	
Crossover - MDIX configuration	CROSS = High
Crossover – MDI configuration	CROSS = Low
Crossover – auto-configuration	CROSS = Float
Enable Smart Speed	SMART_SPEED = High
Disable Smart Speed	SMART_SPEED = Low
Enable A/N Isolate	ANISOL = High
Disable A/N Isolate	ANISOL = Low

1. Settings may be overridden during the auto-negotiation process. Use register bits to force these settings,
2. Individual control of ASM and Pause is only available through register bits.

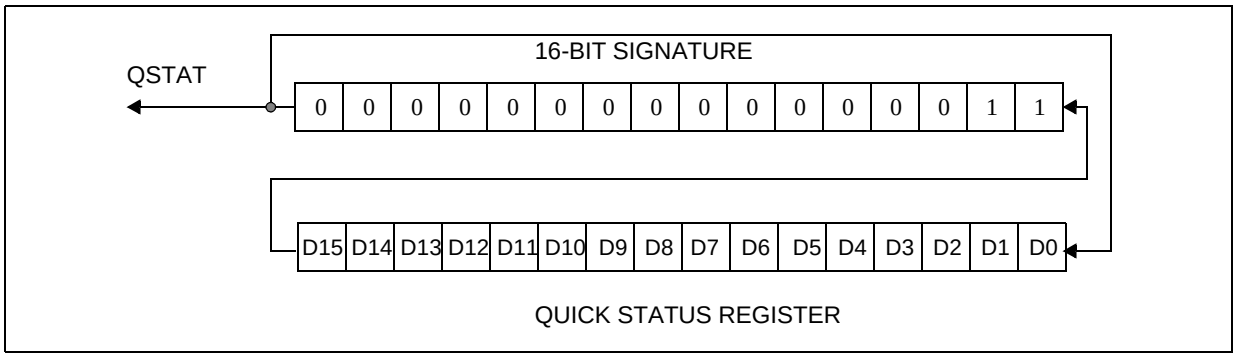
2.3.8 Quick Status Interface

The LXT1000 provides an additional Quick Status Interface for link-state monitoring. The LXT1000 sends out 32 bits (16 data bits, 16 signature bits) of continuous information about the current link state on the Quick Status data ball (QSTAT). Utilizing this single ball allows the MAC to be constantly aware of what operations the PHY is performing. A separate, 25 MHz clock input line (QCLK) provides synchronization for the data ball. Thus, an ASIC can monitor multiple PHY devices using a single clock.

A simple signature is used to delineate the start of the QSTAT register (Address 17) information, allowing a very simple interface to be designed. The contents of the Quick Status register are output on QSTAT. (See Table 67 on page 100 for Quick Status bits definition and description.) The 16-bits of the Quick Status Register are separated by a signature (0000000000000011). The LXT1000 sources this status information on the falling edge of QCLK.

This information provides a continuous status update of several different attributes and modes of the PHY, and can be used to sense RX, TX, and COL as well as to monitor the status and speed of the auto-negotiation process. The information is provided on an unsolicited basis, without having to issue read requests, which is ideal for hardware applications that require constant monitoring of link status with minimal interaction.

Figure 14. Quick Status Register



2.3.9 LED Functions

The LXT1000 provides seven status indicator LEDs.

2.3.9.1 Link Up

When the link is up, these LEDs report link status as follows:

- Transmission
- Receive
- 1000 Operation
- 10/100 Operation
- Duplex (Full- or Half-duplex)
- Link
- Collision (Half-duplex only) During full-duplex Gigabit operation, this LED is asserted whenever packets are simultaneously transmitted and received.

2.3.9.2 Link Down

When the link is down, these LEDs report the status of the DSPs for the four channels, as shown in Table 16 on page 36.

Table 16. LED Status Indication / PHY Addressing

LED Ball	LED Function	Initialization Function	Link Down Function
LEDL	**Link LED.** Link status.	PHY Address bit 0	Off
LEDT	**Transmit LED.** Transmitting packets.	PHY Address bit 1	Channel A DSP Lock
LEDR	**Receive LED.** Receiving packets.	PHY Address bit 2	Channel B DSP Lock
LEDF	**Duplex LED.** Full-duplex mode selection.	PHY Address bit 3	Channel D DSP Lock
LEDC	**Collision LED.** Collision indication.	PHY Address bit 4	Channel C DSP Lock
LEDG	**Gigabit LED.** 1000 operation selection.	None. Tie Low	No Function
LEDS	**Speed LED.** 10/100 operation selection.	None. Tie Low	No Function

2.3.9.3 LED Options

Individual LEDs can be set to turn on solid, turn off, or blink. If enabled, the blink period is 512 ms. LED events can be “activity stretched” to 100 ms (from the default 30 ms) by setting bit 20.0 = 1. Pulse stretching also can be disabled, if desired, by setting bit 20.1 = 1. This may be useful to indicate events for a management engine. In addition, turning LEDs on and off via MDIO management control may be useful for diagnostic purposes.

2.3.9.4 PHY Address Determination

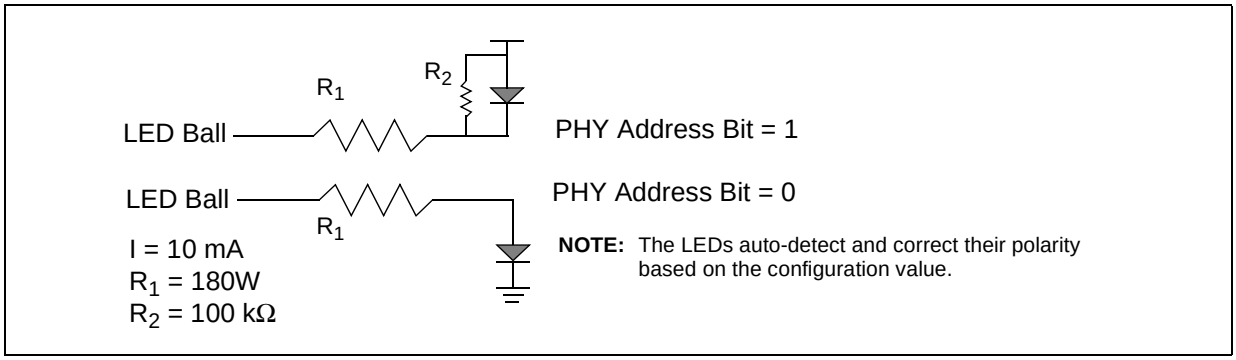
Five of the seven LED balls (LEDR, LEDT, LEDL, LEDF, and LEDC) also determine the PHY address. At power-up and reset, these five LED balls define the GMII PHY address of the LXT1000. After power-up and reset, the same balls become LED status indicators (see Table 16).

The configuration of the LED components depends on the actual value used for the individual PHY address bits. Refer to Figure 15. When a “1” value is desired, the LED and resistor are connected between the LED ball VCC. When a “0” value is desired, the LED and resistor are connected between the LED ball and ground. The polarity of the LEDs is automatically detected and corrected.

If LEDs are not required for the application, only a resistor is required to set the PHY address.

The LED balls are designed to drive 10 mA. They will be open drain/source depending on the external circuit configuration. This will allow the user to tie several configuration balls together (with a single resistor) if LEDs are not desired, assuming that all ports will be set to the same value.

Figure 15. PHY Address Determination via LED balls



2.3.10 JTAG Boundary Scan Interface

The LXT1000 includes an IEEE JTAG1149.1 boundary scan test port for board level testing. All digital I/O balls are accessible. The physical interface consists of five balls (TRST, TMS, TDI, TDO, and TCK), and includes a state machine, data register array, and instruction register. Pull each of these balls High except TRST, which is pulled Low.

2.3.10.1 State Machine

The TAP controller is a 16 state machine driven by the TCK and TMS balls. Upon reset by TRST the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS and TDI are High for a period of five TCK periods.

2.3.10.2 Instruction Register

After the state machine resets, the IDCODE instruction is always invoked. The decode logic ensures correct data flow to the Data registers according to the current instruction (see Table 17).

Table 17. Boundary Scan Supported Instructions

Name	Code	Description	Mode	Data Register
EXTEST	FFE8	External Test	Test	BSR
IDCODE	FFFEH	ID Code Inspection	Normal	ID REG
SAMPLE	FFF8H	Sample Boundary	Normal	BSR
HIGHZ	FFCFH	Force Float	Normal	Bypass
CLAMP	FFEFH	Control Boundary to 1/0	Test	Bypass
BYPASS	FFFFH	Bypass Scan	Normal	Bypass

2.3.10.3 Boundary Scan Register

Each BSR cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. There are four modes of operation (see Table 18).

Table 18. BSR Mode of Operation

Mode	Operation
1	Capture
2	Shift
3	Update
4	System Function

Table 19. JTAG ID Register

31:28 Version	27:12 Part ID	11:8 JEDEC Continuation Characters	7:1 JEDEC ID[1]	0 Reserved
xxxx	3E8	0000	111 1110	1

1. The JEDEC ID is an 8-bit identifier. And the MSB is for parity and is ignored. Intel's JEDEC ID is FE (1111 1110) which becomes 111 1110.

2.4 Initialization

2.4.1 Power-Up

At power-up, the LXT1000 initializes all internal PLLs and analog functions and reads its hardware configuration balls. Internal logic holds the device in reset for approximately 300 ms after VCC reaches 3.xV.

2.4.2 Hardware Reset

The LXT1000 does not require an external hardware reset circuit. The device can be reset by pulling the RESET ball Low. Hardware reset causes the same re-initialization and reconfiguration function that occurs at power-up. TX_CLK and RX_CLK are not available and the MII registers are not accessible until the external reset function completes.

2.4.3 Software Reset

Software reset, which is invoked by setting bit 0.15 = 1 causes all internal digital state machines to reset and causes the external hardware configuration to be re-read, but does not cause re-initialization of the PLLs or other analog functions. RX_CLK and TX_CLK, and the MII registers continue to be available. Table 20 summarizes the various modes

2.4.4 Hardware Power-Down

Hardware power-down mode is entered when PWRDWN is High. In power-down mode, all functions are disabled. When the LXT1000 exits power-down mode (PWRDWN is Low), it re-initializes all analog functions and configuration settings.

2.4.5 Software Power-Down

Software power-down is entered by setting 0.11 = 1. In software power-down, all functions and RX_CLK and TX_CLK are disabled except for the MII Registers and MDIO interface. When the LXT1000 exits software power-down (0.11 = 0), it re-initializes all analog functions, but retains its previous configuration settings.

Table 20. Initialization Modes

Mode	Initializes PLL and Analog Functions	Initializes Digital Functions and State Machines	RX_CLK and TX_CLK	MII Registers Access	Re-Read H/W Configuration Balls
Power-Up	Yes	Yes	No	No	Yes
H/W Reset	Yes	Yes	No	No	Yes
H/W Power-Down Recovery	Yes	Yes	No	No	Yes
S/W Power-Down Recovery	Yes	Yes	Yes	Yes	No
S/W Reset	No	Yes	Yes	Yes	Yes

2.4.6 Determining Link State

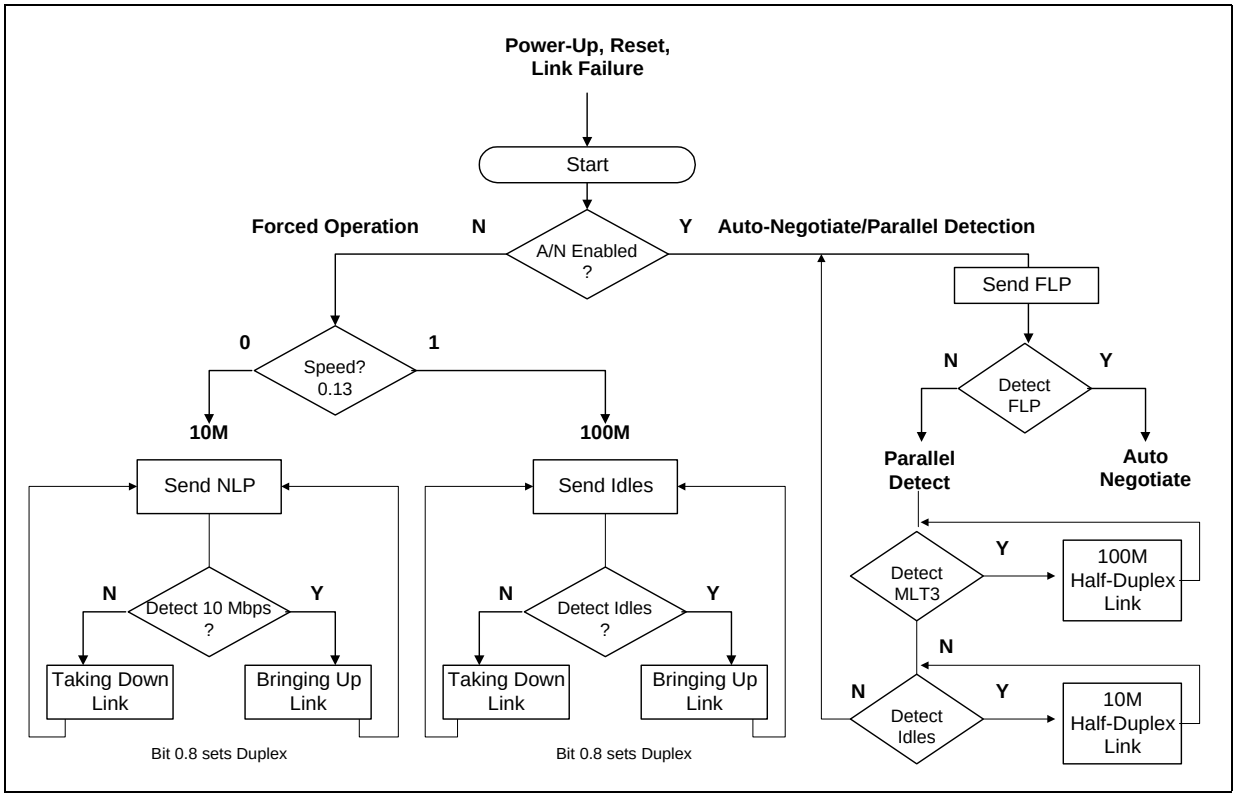
The LXT1000 and its link partner determine the type of link established through one of three methods:

- Auto-Negotiation
- Parallel Detection
- Forced Operation

Auto-negotiation is the only method allowed by the 802.3ab standard for establishing a 1000BASE-T link, although forced operation can be used for test purposes. (See "Test Information" on page 70.) For 10/100 links, any of the three methods can be used. Following sections discuss each in greater detail.

Figure 16 provides an overview of link establishment. First the LXT1000 checks if auto-negotiation is enabled. If not, the LXT1000 forces operation as directed. If auto-negotiation is enabled, the LXT1000 begins transmitting Fast Link Pulses (FLPs) and receiving FLPs from its link partner. If FLPs are received by the LXT1000, auto-negotiation proceeds. It also can receive 100BASE-TX MLT3 and 10BASE-T Normal Link Pulses (NLPs). If either MLT3 or NLPs are received, it aborts FLP transmission and immediately brings up the corresponding half-duplex link.

Figure 16. Overview of Link Establishment



2.4.6.1 False Link

The LXT1000 does not falsely establish link with a partner operating at a different speed. For example, the LXT1000 does not establish a Gigabit or 10M link with a 100M link partner.

2.4.6.2 Auto-Negotiation

Auto-negotiation allows the LXT1000 and its link partner to determine:

- Link speed (1000, 100 or 10)
- Link duplex state (full or half)
- Flow-control support (PAUSE and ASM_DIR)
- Master-Slave relationship for Gigabit links

During auto-negotiation, the LXT1000 and its link partner exchange configuration information using Fast Link Pulses (FLPs). This exchange of information allows them to determine the highest common ability, and set the link state accordingly. The information exchanged is static; it is determined before auto-negotiation begins and is not modified during the process. This process ensures that each side clearly understands the other's ability. The information to be sent is loaded into MII Registers 4 and 9 before auto-negotiation begins. Once auto-negotiation completes, the information received from the other side is placed in MII Registers 5 and 10. Each side then compares its capabilities to its link partner's to determine the link state.

Link information is exchanged in 16-bit words called “Pages”. 10/100 auto-negotiation requires only one page, which is called the “Base Page” and is exchanged through Registers 4 and 5. 1000 auto-negotiation requires four pages: a base page and three next pages. The base page originates from Register 4, and is identical to the one used for 10/100 auto-negotiation, except that Bit 15 (Next Page) = 1 for 1000 auto-negotiation, and Bit 15 = 0 for 10/100 auto-negotiation. The other three pages are generated by the LXT1000 from information in Register 9; with the corresponding information from the link partner loaded into Register 10.

Auto-negotiation is the only method recognized in the IEEE standard for bringing up a 1000BASE-T link, although forced operation can be used for test purposes. Auto-negotiation is necessary to determine the master-slave relationship, which is required for echo cancellation and signal recovery. (Refer to “Master/Slave Relationship Details” on page 68.)

2.4.6.2.1 A Special Note for TBI Applications

When interfacing the LXT1000 to MACs intended for Gigabit/fiber applications, turn off the MACs auto-negotiate function if possible; the LXT1000 cannot support it. Program the LXT1000 for auto-negotiation, full-duplex, and speed = 1000 only.

2.4.6.2.2 Controlling Auto-Negotiation

Control

When auto-negotiation is controlled by software, the following steps are recommended:

- After power-up, power-down, or reset, the power-down recovery time must be completed before attempting to program the MII Registers.
- Use MII Registers 4 and 9 to configure the device.
- Enable auto-negotiation by setting MDIO bit 0.12 = 1.

Monitoring

MII Register 17 provides a convenient place to monitor link status following auto-negotiation. The contents of this register are also output on the QuickStatus ball. (Refer to “Quick Status Interface” on page 34 for more information):

- Bit 17.10 is set to 1 once the link is established.
- Bits 17.15:14 can be used to determine the link operating speed (1000, 100, or 10 Mbps).
- Bit 17.9 can be used to determine the duplex mode (half or full).

2.4.6.3 Parallel Detection

Parallel detection can only be used to establish 10 and 100 links. It occurs when the LXT1000 tries to negotiate (transmit FLPs to its link partner), but instead of sensing FLPs from the link partner, it senses 100BASE-TX MLT3 code or 10BASE-T Normal Link Pulses (NLPs) instead. In this case, the LXT1000 immediately stops auto-negotiation (terminates transmission of FLPs) and immediately brings up whatever link corresponds to what it has sensed (MLT3 or NLPs).

With parallel detection, it is impossible to determine the true duplex state of the link partner, and the IEEE standard requires the LXT1000 to assume a half-duplex link. Parallel detection also does not allow exchange of flow-control ability (PAUSE and ASM_DIR) or Master/Slave relationship required by 1000BASE-T. This is why parallel detection cannot be used to establish Gigabit Ethernet links.

2.4.6.4 Forced Operation

Forced operation can be used to establish 10 and 100 links, and 1000 links for test purposes. In this method, auto-negotiation is disabled completely, and the link state of the LXT1000 is determined by MII Register 0. At reset, the state of this register is determined by the Hardware Configuration balls, and if MDIO/MDC operation is enabled, it can by updated via software at any time.

In forced operation, the user sets the link speed (10, 100, or 1000) and duplex state (full or half). For Gigabit (1000) links, the user must explicitly designate one side as the Master and the other as the Slave.

Note the paradox (per the Standard): If one side of the link is forced to full-duplex operation and the other side has auto-negotiation enabled, the auto-negotiating partner parallel-detects to a half-duplex link while the forced side operates as directed in full-duplex mode. The result is spurious, unexpected collisions on the side configured to auto-negotiate.

Table 21 summarizes link establishment procedures.

Table 21. Determining Duplex State via Parallel Detection

Configuration	Result
Both sides set for auto-negotiate	Link is established via auto-negotiation.
Both sides set for forced operation	No problem as long as duplex settings match.
One side set for auto-negotiation and the other for forced, half-duplex	Link is established via parallel detect.
One side set for auto-negotiation and the other for forced full-duplex	Link is established; however, sides disagree, resulting in transmission problems. (Forced side will be full-duplex, auto-negotiation side will be half-duplex.)

2.4.7 Establishing and Maintaining the Link

Once the link state is determined—via auto-negotiation, parallel detection or forced operation—the LXT1000 and its link partner bring up the link.

2.4.7.1 1000BASE-T

For 1000BASE-T links, the LXT1000 and its link partner enter a training phase. They exchange idle symbols and use the information gained to set their adaptive filter coefficients. These coefficients are used to equalize the incoming signal, as well as eliminate signal impairments such as echo and crosstalk.

Either side indicates completion of the training phase to its link partner by changing the encoding of the idle symbols it transmits. When both sides so indicate, the link is up. Each side continues sending idle symbols whenever it has no data to transmit. The link is maintained as long as valid idle, data, or carrier extension symbols are received.

2.4.7.2 100BASE-TX

For 100BASE-TX links, the LXT1000 and its link partner immediately begin transmitting idle symbols. Each side continues sending idle symbols whenever it has no data to transmit. The link is maintained as long as valid idle symbols or data is received.

2.4.7.3 10BASE-T

For 10BASE-T links, the LXT1000 and its link partner begin exchanging Normal Link Pulses (NLPs). The LXT1000 transmits an NLP every 16 ms, and expects to receive one every 10 to 20 ms. The link is maintained as long as normal link pulses are received.

2.4.8 Taking Down the Link

The LXT1000 takes down an established link when the required conditions are met. For 100/1000 links, this occurs some time after valid idle codes are not received. For 10 links, this occurs after a sufficient number of Normal Link Pulses (NLPs) are not sensed.

When link is down, transmission of data is halted until the link is re-established. *What* is transmitted depends on whether auto-negotiation is enabled or not. If auto-negotiation is enabled, the LXT1000 re-enters the auto-negotiation phase and begins transmitting Fast Link Pulses (FLPs). If auto-negotiation is disabled, the LXT1000 continues to transmit idle symbols (100/1000) or NLPs, but inhibits transmission of data. For 1000TX links, the LXT1000 re-enters the training phase.

Table 22 summarizes these relationships.

Table 22. Transmission Pattern If Link Is Down

Speed	Link Established By	What Happens When Link Goes Down	
		A/N Disabled	A/N Enabled
1000 A/N	4DPAM5 stream	Return to training phase	Return to Auto-Negotiation
100 A/N	MLT3 stream	Continue transmitting idle	
10 A/N	Normal Link Pulses (NLPs)	Continue transmitting NLPs	

2.4.9 Link Enhancements

The LXT1000 offers three enhanced link functions, each of which are discussed in the sections that follow:

- SmartSpeed
- Auto-Negotiate Isolation
- Flow Control

2.4.9.1 SmartSpeed

SmartSpeed is an enhancement to auto-negotiation that allows the LXT1000 to react intelligently to network conditions that prohibit establishment of a 1000BASE-T link, such as cable problems. Such problems may allow auto-negotiation to complete, but then inhibit completion of the training phase. Normally, if a 1000BASE-T link fails, the LXT1000 returns to the auto-negotiation state with the same speed settings indefinitely. With SmartSpeed enabled, after three failed attempts, the LXT1000 automatically downgrades the highest ability it advertises to the next lower speed: from 1000 to 100 to 10. Once a link is established, and if it is later broken, the LXT1000 automatically upgrades the capabilities advertised to the original setting. This allows the LXT1000 to automatically recover once the cable plant is repaired.

2.4.9.1.1 Using SmartSpeed

Smartspeed is enabled by pulling SMART_SPD High or by setting 16.7 = 1. When SmartSpeed downgrades the LXT1000 advertised capabilities, it sets bit 18.9. When link is established, its speed is indicated in 17.15:14. SmartSpeed automatically resets the highest-level auto-negotiation abilities advertised, if link is established and then lost for more than 2 seconds.

2.4.9.2 Auto-Negotiate Isolation

Auto-Negotiate Isolation functions whenever the link drops unexpectedly and is re-established at a different speed. Auto-Negotiate Isolation is enabled when the ANISOL input is set High. Then, when a link speed change occurs, the LXT1000 sets bit 16.2 and holds all data transfers to or from the MAC until 16.2 is cleared. The LXT1000 indicates the changes in link state through its Interrupt function (Register 18), which operates independently of Auto-Negotiate Isolation.

When activated, the auto-negotiate isolation function is asynchronous to the MAC Interface. It may cause the abrupt termination of a packet as well as setup and hold violations on the receive signals output by the MAC Interface.

2.4.9.3 Flow Control

Flow control is a function which is described in Clause 31 of the IEEE 802.3 standard. It allows congested nodes to pause traffic. Flow control is essentially a MAC-to-MAC function. MACs indicate their ability to implement flow control during auto-negotiation. This ability is communicated through two bits in the auto-negotiation registers (4.10 and 4.11).

The LXT1000 transparently supports MAC-to-MAC advertisement of flow control through its auto-negotiation process. Prior to auto-negotiation, the MAC indicates its flow control capabilities via 4.10 (Pause) and 4.11 (ASM_DIR). After auto-negotiation, the link partner’s flow control capabilities are indicated in 5.10 and 5.11.

There are two forms of flow control that can be established via auto-negotiation: symmetric and asymmetric. Symmetric flow control is for point-to-point links; asymmetric for hub-to-end-node connections. Symmetric flow control allows either node to flow-control the other. Asymmetric flow control allows a repeater or switch to flow-control a DTE, but not vice versa.

Table 23 shows intended operation for the various settings of ASM_DIR and Pause. This information is provided for reference only, it is the responsibility of the MAC to implement the correct function. The LXT1000 merely allows the two MACs to communicate their abilities to each other.

Table 23. Pause and Asymmetric Pause Settings

ASM_DIR settings Local (4.11) and Remote (5.10)	Pause Setting - Local (4.10)	Pause Setting - Remote (5.10)	Result
Both ASM_DIR = 1	1	1	Symmetric - Either side can flow control the other
	1	0	Asymmetric - Remote can flow control local only
	0	1	Asymmetric - Local can flow control remote
	0	0	No flow control
Either or both ASM_DIR = 0	1	1	Symmetric - Either side can flow control the other
	Either or both = 0		No flow control

2.4.10 Link Speed Changes

The LXT1000 is designed with glitch-free muxing logic, which guarantees that the two output clocks, TX_CLK and RX_CLK, do not glitch during a speed change, for example, from Gigabit operation to auto-negotiation. The changeover takes no more than three clock cycles of the slowest clock (whether switching to or from). No clock pulse is shorter than the half-duty cycle of the fastest clock (4 ns). During the transition phase, legitimate clock pulses of either speed may appear on the outputs. There also may be no activity on the output for the entire duration of the transition.

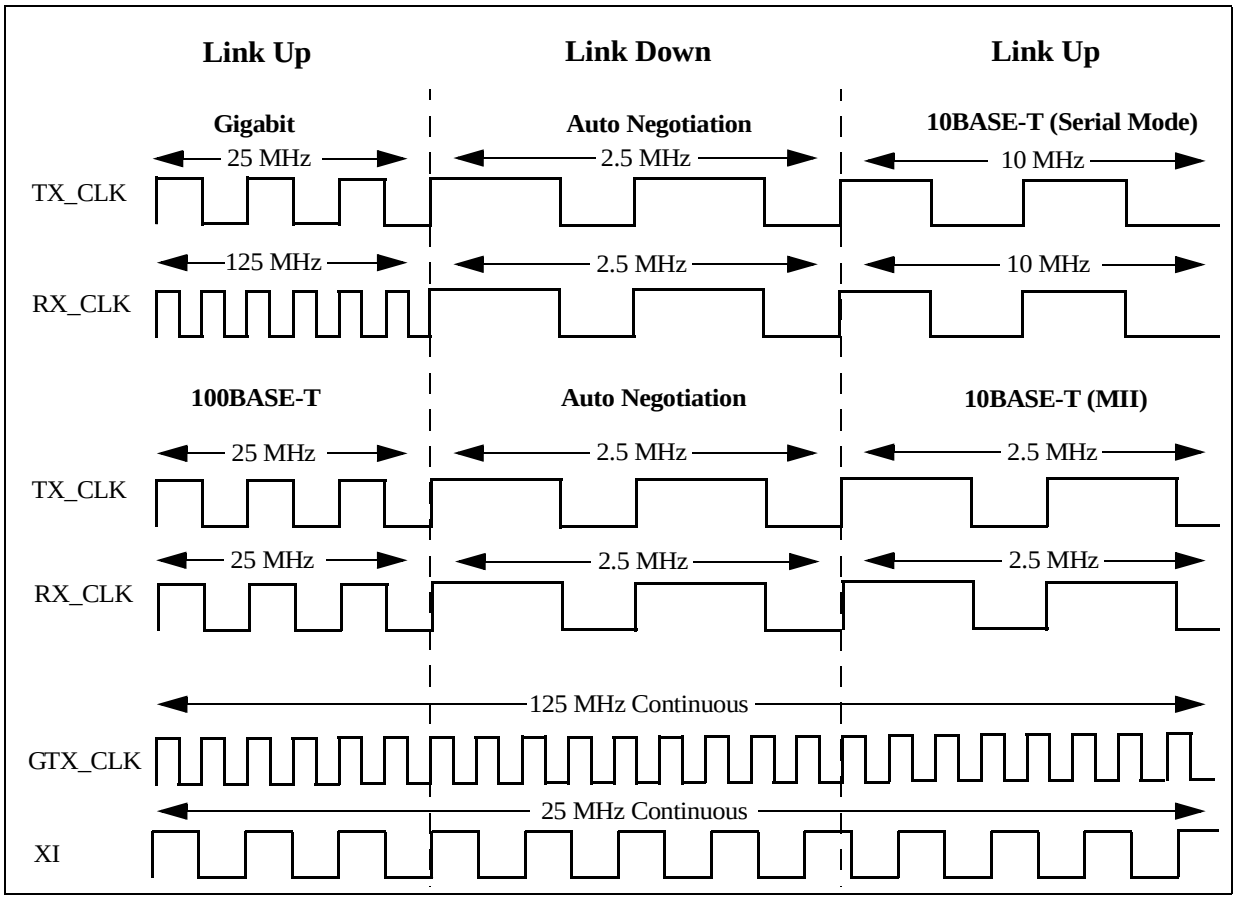
2.4.10.1 How Link Speed Changes Affect MAC Interface Clock Signals

Whenever link speed changes occur, the frequencies of the MAC interface clock (TX_CLK and RX_CLK) change accordingly. Figure 17 shows two link speed changes and the corresponding clock frequency changes: Gigabit to auto-negotiation to 10BASE-T (Serial mode), and 100BASE-T to auto-negotiation to 10BASE-T (MII mode). Many other link speed/clock changes are possible; these only serve as examples.

Notes: 1. RX_CLK and TX_CLK do not change frequency when the link state changes from auto-negotiation to 10BASE-T and the MAC Interface is configured for 10 MII mode.

2. The crystal clock (XI) and the GTX_CLK are continuous. Both are input signals.

Figure 17. Link Speed and Corresponding Clock Frequency Changes



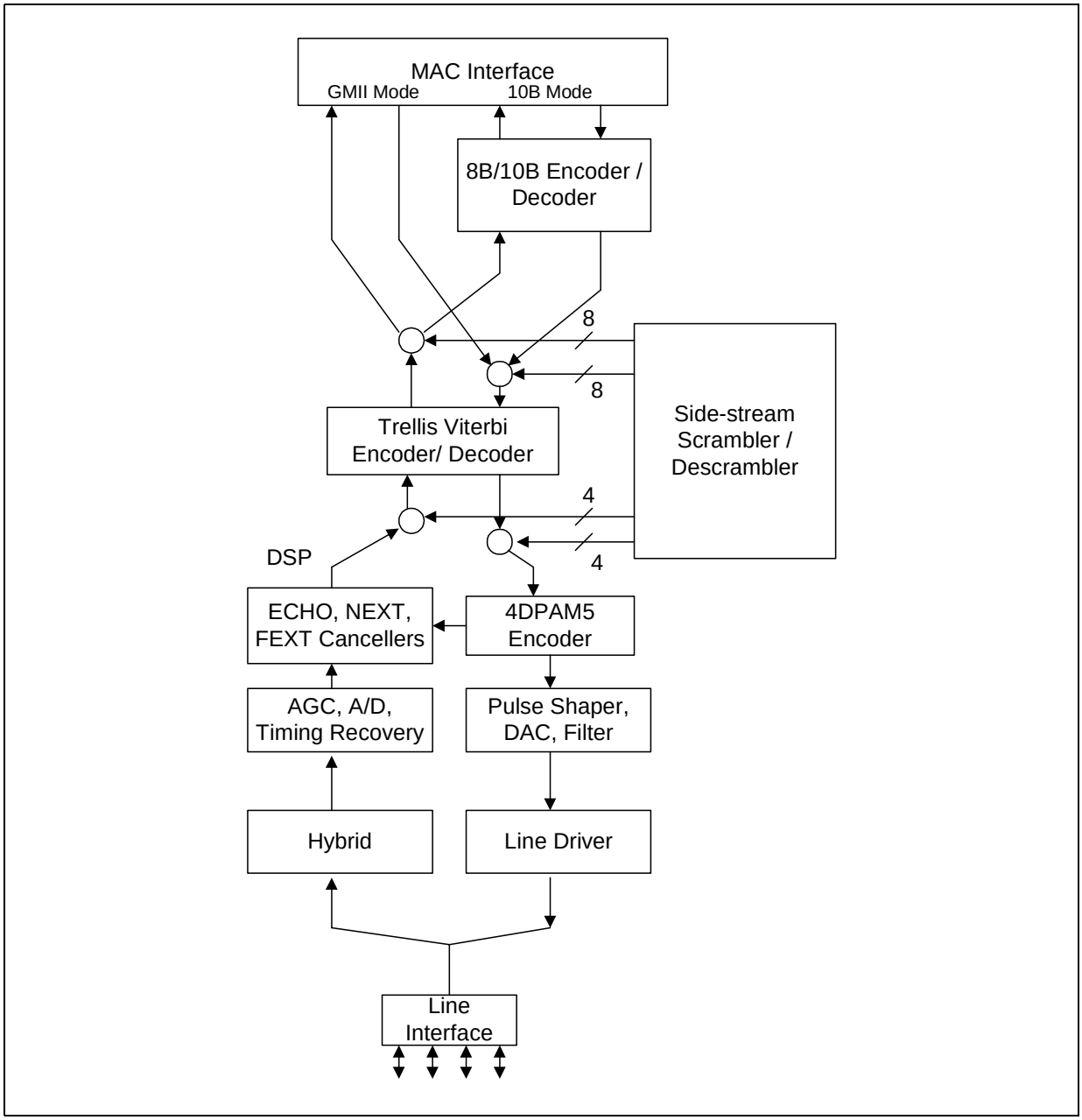
2.5 1000 Mbps Operation

2.5.1 Introduction

Figure 18 provides an overview of 1000BASE-T functions, followed by discussion and review of the internal functional blocks shown in the diagram.

A following sections describes the various Gigabit transmit and receive operations from the point of view of the MAC. These operations include normal transmit/receive, false carrier and collision detection, and carrier extension/packet concatenation with/without errors. (Refer to "Supported Operations" on page 51.)

Figure 18. 1000BASE-T Functions Overview



2.5.2 Transmit Functions

This section describes functions used when the Media Access Controller (MAC) transmits data through the LXT1000 and out onto the twisted-pair connection (see Figure 19 on page 49).

2.5.2.1 8B/10B Decoder

The 8B/10B is used only when the MAC interface is configured for TBI mode. In that case, it converts 10B codes transmitted by the MAC into 8B (GMII) data. Note that only data codes are decoded; non-data codes are ignored.

2.5.2.2 Scrambler

The scrambler randomizes the transmitted data. The purpose of scrambling is twofold:

- Scrambling eliminates repeating data patterns, also known as “spectral lines” from the 4DPAM5 waveform in order to reduce EMI.
- Each channel (A, B, C, D) has a unique signature that the receiver uses for identification.

The scrambler is driven by a 33-bit Linear Feedback Shift Register (LFSR), which is randomly loaded at power-up. The LFSR function used by the Master differs from that used by the Slave, giving each direction its own unique signature. The LFSR, in turn, generates twelve mutually uncorrelated outputs. Eight of these are used to randomize the inputs to the 4DPAM5 and Trellis encoders. The remaining four outputs randomize the sign of the 4DPAM5 outputs.

2.5.2.3 Transmit FIFO

The transmit FIFO re-synchronizes data transmitted by the MAC to the transmit reference used by the LXT1000. The FIFO is large enough to support a frequency differential of up to +/- 1000 ppm over a packet size of 10 KB (jumbo frame).

2.5.2.4 Transmit Phase-Locked Loop PLL

This function generates the 125 MHz timing reference used by the LXT1000 to transmit 4DPAM5 symbols. When the LXT1000 is the Master side of the link, the XI input is the reference for the transmit PLL. When the LXT1000 is the Slave side of the link, the recovered receive clock is the reference for the transmit PLL.

2.5.2.5 Trellis Encoder

The Trellis Encoder uses the two high-order bits of data and its previous output to generate a ninth bit, which determines if the next 4DPAM5 pattern should be even or odd. For data, this function is: $Trellis_n = Data7_{n-1}$ XOR $Data6_{n-2}$ XOR $Trellis_{n-3}$ This provides forward error correction and enhances the signal-to-noise (SNR) ratio by a factor of 6dB.

2.5.2.6 4DPAM5 Encoder

The 4DPAM5 encoder translates 8B codes transmitted by the MAC into 4DPAM5 symbols. The encoder operates at 125 Mhz, which is both the frequency of the MAC interface and the baud rate used by 1000BASE-T.

Each 8B code represents one of 2^8 or 256 data patterns. Each 4DPAM5 symbol consists of one of five signal levels (-2,-1,0,1,2) on each of the four twisted-pair (A,B,C,D) representing 5^4 or 625 possible patterns per baud period. Of these, 113 patterns are reserved for control codes, leaving 512 patterns for data. These data patterns are divided into two groups of 256 even and 256 odd data patterns. Thus, each 8B octet has two possible 4DPAM5 representations—one even and one odd pattern.

2.5.2.7 Spectral Shaper

This function causes the 4DPAM5 waveform to have a spectral signature that is very close to that of the MLT3 waveform used by 100BASE-TX. This allows 1000BASE-T to take advantage of infrastructure (cables, magnetics) designed for 100BASE-TX.

The shaper works by transmitting 75% of a 4DPAM5 code in the current baud period, and adding the remaining 25% into the next baud period.

2.5.2.8 Low-Pass Filter

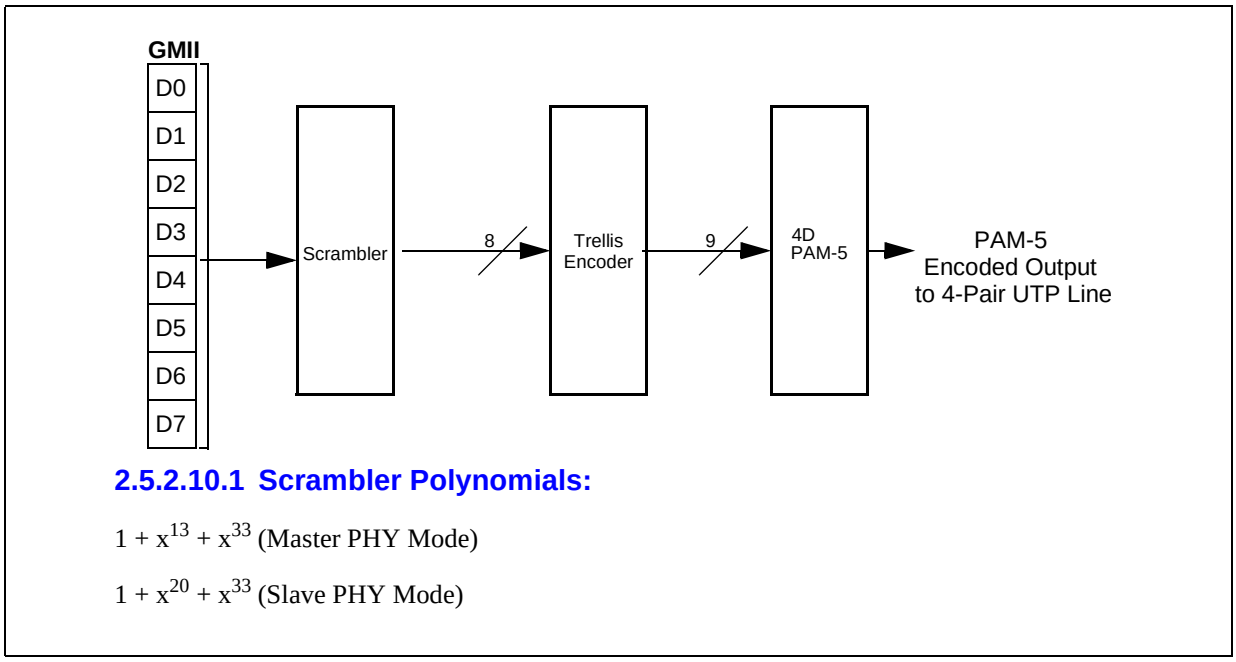
To aid with EMI, this filter attenuates signal components more than 180 MHz. In 1000BASE-T, the fundamental symbol rate is 125 MHz.

2.5.2.9 Line Driver

The line driver drives the 4DPAM5 waveforms onto the four twisted-pair channels (A, B, C, D), adding them onto the waveforms that are simultaneously being received from the link partner.

2.5.2.10 Transmit/Receive Flow

Figure 19. 1000BASE-T Transmit Flow and Line Coding Scheme

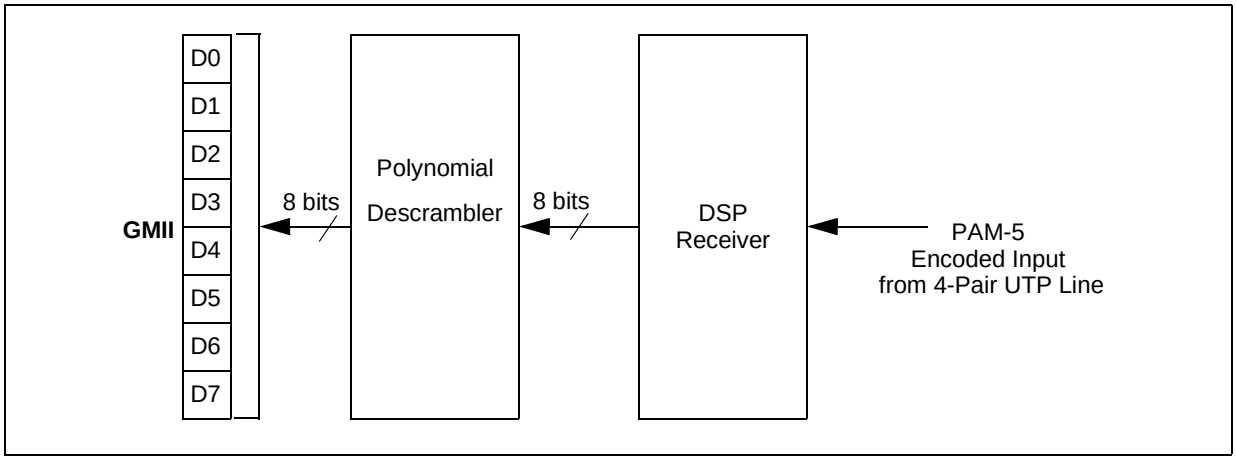


2.5.2.10.1 Scrambler Polynomials:

$1 + x^{13} + x^{33}$ (Master PHY Mode)

$1 + x^{20} + x^{33}$ (Slave PHY Mode)

Figure 20. 1000BASE-T Receive Flow



2.5.3 Receive Functions

This section describes functions which are used when the LXT1000 receives data from the twisted-pair interface and passes it back to the MAC (see Figure 18 and Figure 20).

2.5.3.1 Hybrid

The hybrid subtracts the transmitted signal from the input signal, allowing the use of simple 100BASE-TX compatible magnetics.

2.5.3.2 Automatic Gain Control

The Automatic Gain Control (AGC) normalizes the amplitude of the received signal, adjusting for the attenuation produced by the cable.

2.5.3.3 Timing Recovery

This function re-generates a receive clock from the incoming data stream which is used to sample the data. On the Slave side of the link, this clock is also used to drive the transmitter.

2.5.3.4 Analog-to-Digital Converter

The Analog-to-Digital (ADC) function converts the incoming data stream from an analog waveform to digitized samples for processing by the DSP core.

2.5.3.5 Digital Signal Processor

The Digital Signal Processor (DSP) provides per-channel adaptive filtering, which eliminates various signal impairments including:

- Inter-symbol interference (equalization).
- Echo caused by impedance mismatch of the cable.
- Near-end crosstalk (NEXT) between adjacent channels (A, B, C, D).

- Far-end crosstalk (FEXT)
- Propagation delay variations between channels of up to 120 ns.
- Extraneous tones that have been coupled into the receive path.

The adaptive filter coefficients are initially set during the training phase. They are continuously adjusted (“adaptive equalization”) during operation through the decision-feedback loop.

2.5.3.6 Descrambler

The descrambler identifies each channel by its characteristic signature, removing the signature and re-routing the channel internally. In this way, the receiver can correct for channel swaps and polarity reversals. The descrambler uses the same base 33-bit LFSR used by the transmitter on the other side of the link.

The descrambler automatically loads the seed value from the incoming stream of scrambled idle symbols. The descrambler requires approximately 15 µs to lock, normally accomplished during the training phase.

2.5.3.7 Viterbi Decoder/Decision Feedback Equalizer (DFE)

The Viterbi decoder generates clean 4DPAM5 symbols from the output of the DSP. The Viterbi decoder simultaneously looks at the received data over several baud periods. For each baud period, it predicts whether the symbol received should be even or odd, and compares that to the actual symbol received. The 4DPAM5 code is organized in such a way that a single level error on any channel changes an even code to an odd one and vice versa. In this way, the Viterbi decoder can detect single-level coding errors, effectively improving the signal-to-noise (SNR) ratio by a factor of 6dB. When an error occurs, this information is quickly fed back into the equalizer to prevent future errors.

2.5.3.8 4DPAM5 Decoder

The 4DPAM5 decoder generates 8B data from the output of the Viterbi decoder.

2.5.3.9 8B/10B Encoder

The 8B/10B encoder converts 8B data into 10B codes and is used when the MAC interface is configured in TBI mode. (This function is not used when the MAC interface is configured for GMII mode.)

2.5.4 Supported Operations

The LXT1000 Gigabit functions include:

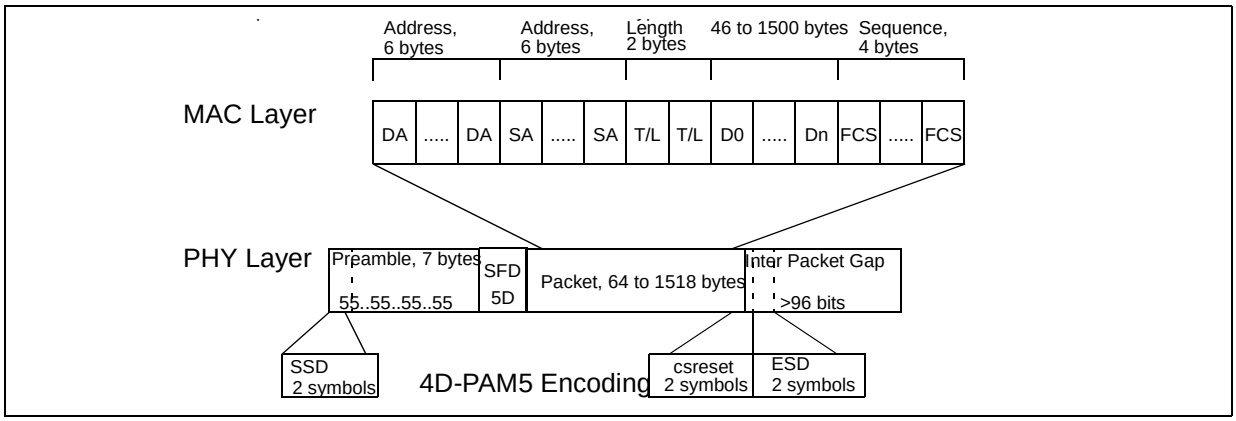
- **Link detection.**
- **Normal packet operation.** Generation of SSD, ESD, csreset, idle, error handling, and false carrier detection.
- **Collision detection** for half-duplex operation.
- **Carrier extension** with/without errors, supporting frame bursting.

- **Packet concatentation**, which allows MACs in half-duplex applications to concatenate packet up to a maximum length of 8 KB. Gaps between packets are filled using a special symbol allowing the PHY to maintain ownership of the link.
- **Jumbo frames.** For full-duplex operations, the LXT1000 allows jumbo frames up to 10 KB, with up to +/- 200 ppm of frequency tolerance on any clock.

2.5.4.1 Operation Details

Figure 21 introduces the following sections and accompanying figures, which provide further detail of all 1000 Mbps supported operations.

Figure 21. 1000BASE-T Frame Structure



2.5.4.1.1 Transmitting/Receiving (Normal)

To transmit, the MAC asserts TX_EN and immediately begins driving preamble octets on TX_D. The LXT1000 asserts CRS back to the MAC, and drives two SSD symbols on the line. The SSD symbols overwrite the first two octets transmitted by the MAC, which are normally preamble octets “55”. After transmitting the SSD, the LXT1000 begins transparent scrambling/encoding of the stream. After the last Frame Check Sequence octet, the MAC de-asserts TX_EN, and the LXT1000 responds by driving two symbols of convolutional reset (csreset) and two ESD symbols before driving idle symbols. The csreset symbols return the Viterbi encoder to a default state during the inter-packet gap.

As a receiver, the LXT1000 asserts CRS and RX_DV in response to receiving an SSD, and immediately begins driving RX_D. Preamble octets “55 55” are substituted for the SSD, after that the LXT1000 transparently decodes the received stream. The LXT1000 de-asserts RX_DV and CRS when it receives the first csreset.

Figure 22. 1000BASE-T Transmission (No Errors, No Collision, No Carrier Extension)

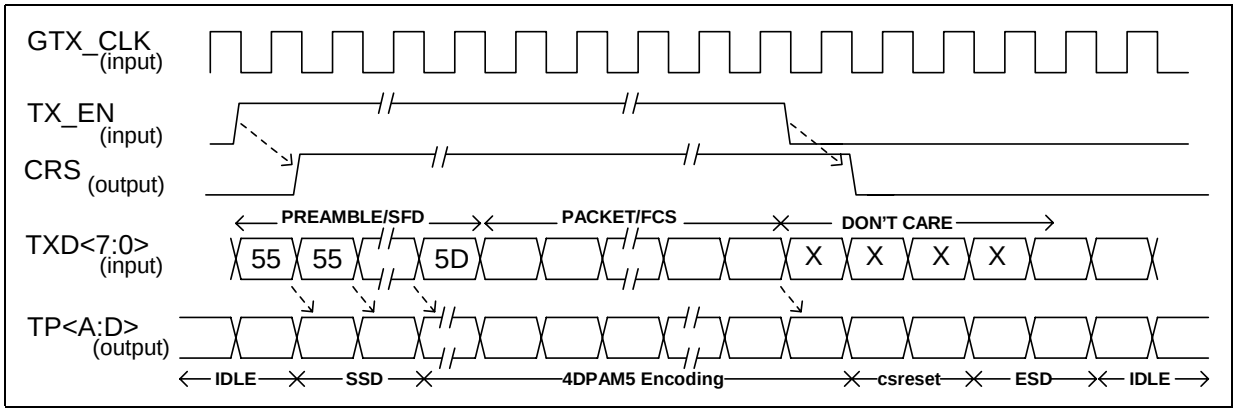
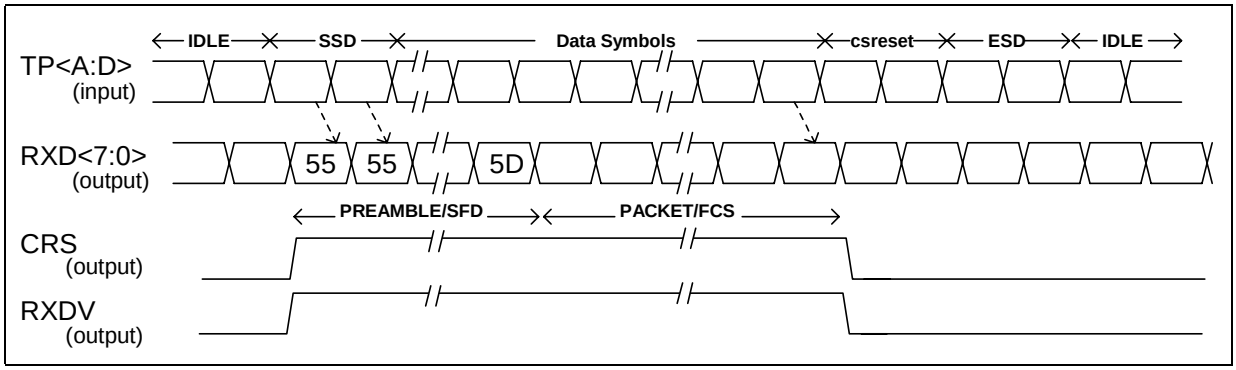


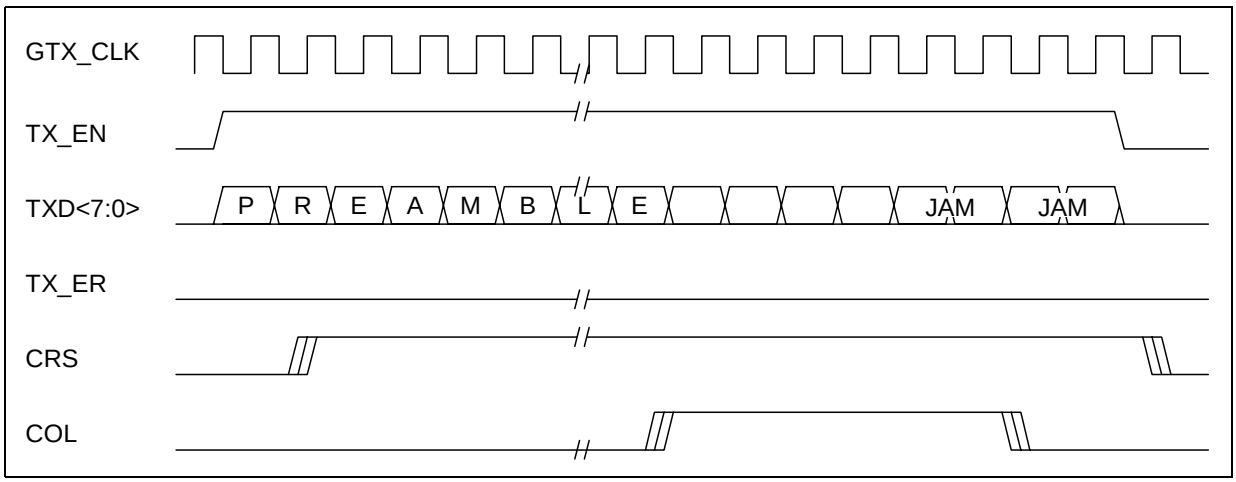
Figure 23. 1000BASE-T Reception (No Errors, No Collision, No Carrier Extension)



2.5.4.1.2 Collision Detection

If the link is configured as a half-duplex connection, and a collision occurs (defined as TX_EN active and the link partner not idle at the same time) the LXT1000 responds by asserting the COL signal and driving a “jam” pattern “55” on the RX_D lines.

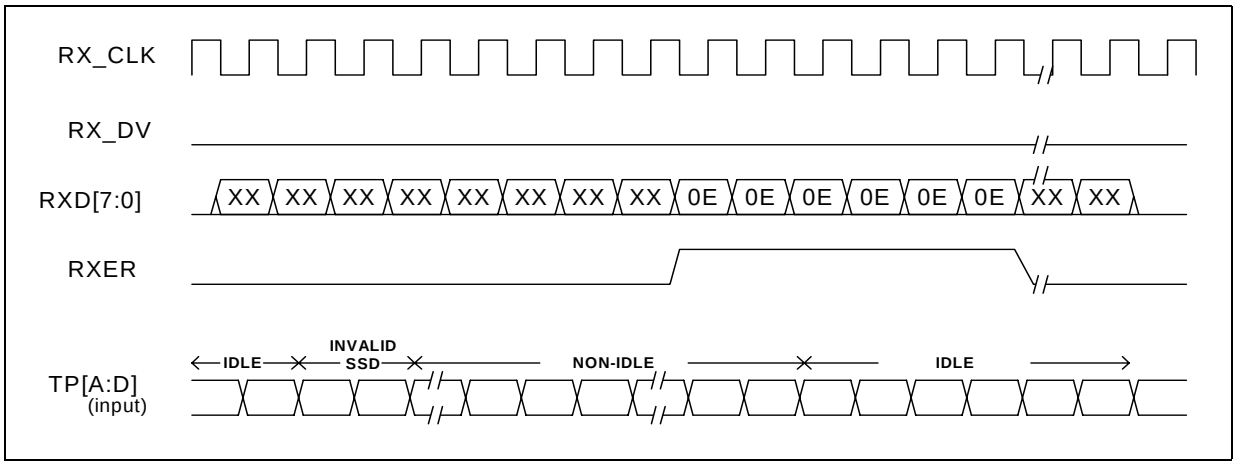
Figure 24. 1000BASE-T Transmission with Collision



2.5.4.1.3 False Carrier Detection

If the LXT1000 receives a false carrier, defined as a packet that does not have an SSD, it responds by asserting RX_ER and driving an “0E” on the RX_D lines.

Figure 25. 1000BASE-T False Carrier Detection



2.5.4.1.4 Error Handling

To drive an error, the MAC asserts TX_ER while TX_EN is active. The LXT1000 responds by immediately terminating normal transmit activities, and driving error codes on the line. While TX_ER is asserted, data on TX_D is ignored. As soon as TX_ER is de-asserted, the LXT1000 resumes normal transmission activities. If the LXT1000 receives error codes while receiving a packet, it asserts the RX_ER signal to the MAC for as many symbol periods as the error is received. When the LXT1000 stops receiving error codes from the line, it resumes normal receive activities.

Figure 26. 1000BASE-T Transmission with Error

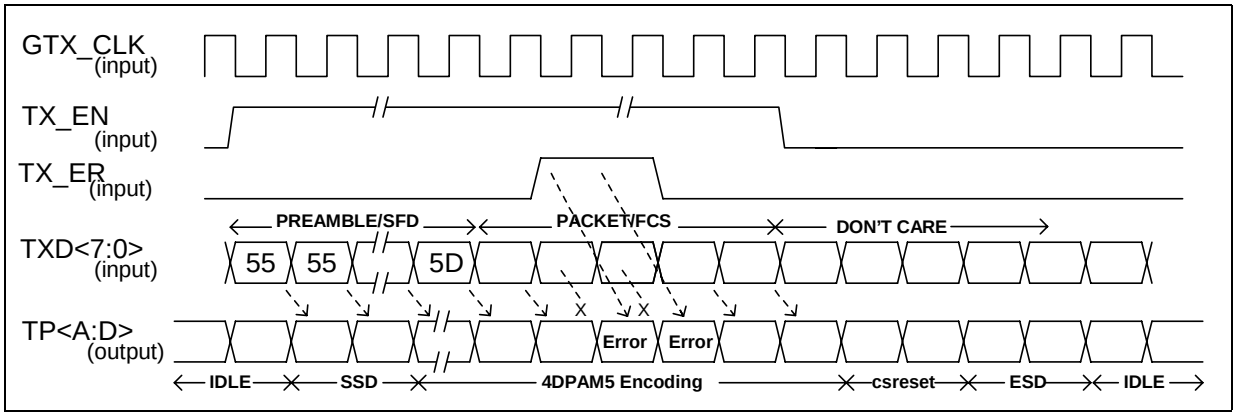
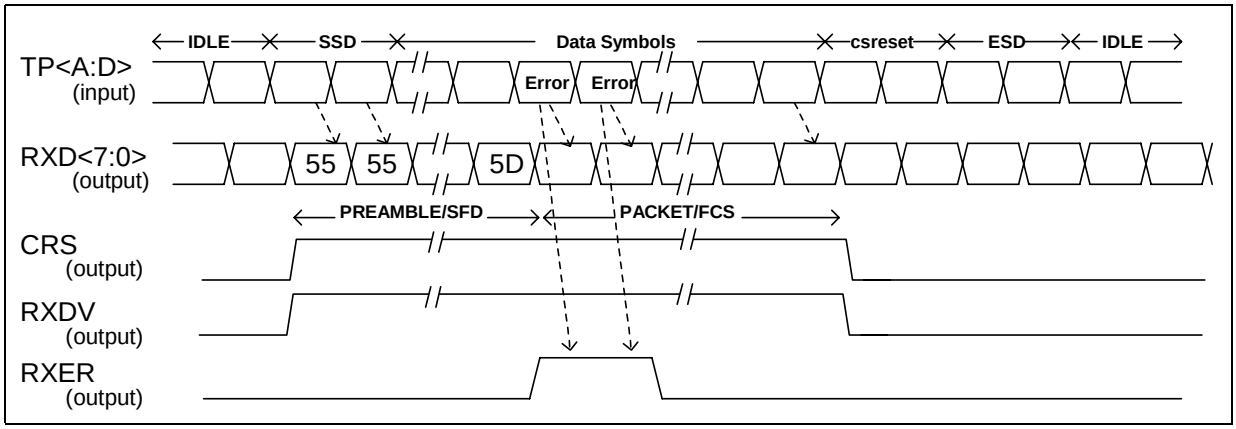


Figure 27. 1000BASE-T Reception with Error



2.5.4.1.5 Carrier Extend/Packet Concatenation

To extend carrier at the end of a packet, the MAC asserts TX_ER as it simultaneously de-asserts TX_EN at the very end of the packet. At the same time, it drives a “0F” octet on the TX_D lines. The LXT1000 responds by terminating the packet with csreset and ESD, and then sends “Carrier Extend” symbols on the line.

If the MAC ends the event by simply dropping TX_ER (carrier extension), the LXT1000 responds by immediately driving idle symbols on the line. If the MAC re-asserts TX_EN at the same time it de-asserts TX_ER (packet concatenation), the LXT1000 immediately drives SSD on the line and then begins transmitting the packet. The LXT1000 leaves CRS asserted for the entire time that either TX_EN or TX_ER remain asserted. If TX_EN goes High during this process, it first must finish sending the “crsreset” and “ESD” symbols on the line, then generate SSD and continue with normal packet encoding.

In the receive direction, the LXT1000 performs the inverse function, dropping RX_DV and asserting RX_ER when it detects Carrier-Extend symbols on the line. The LXT1000 asserts CRS while RX_DV or RX_ER are asserted. During carrier extend, the LXT1000 drives “0F” on the RX_D lines.

Figure 28. 1000BASE-T Transmission, Carrier Extend and Packet Concatenation

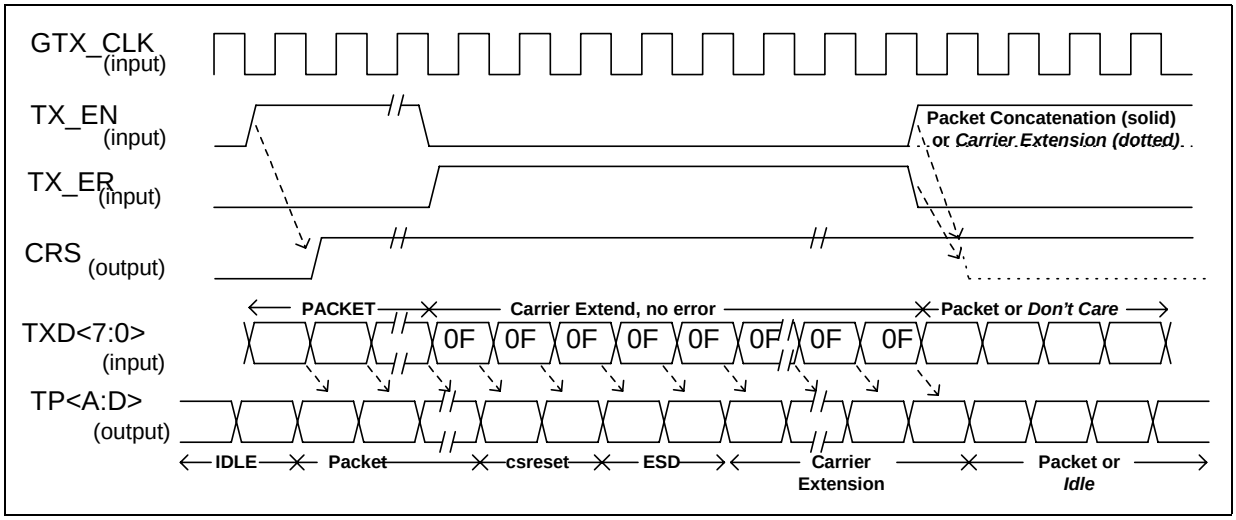
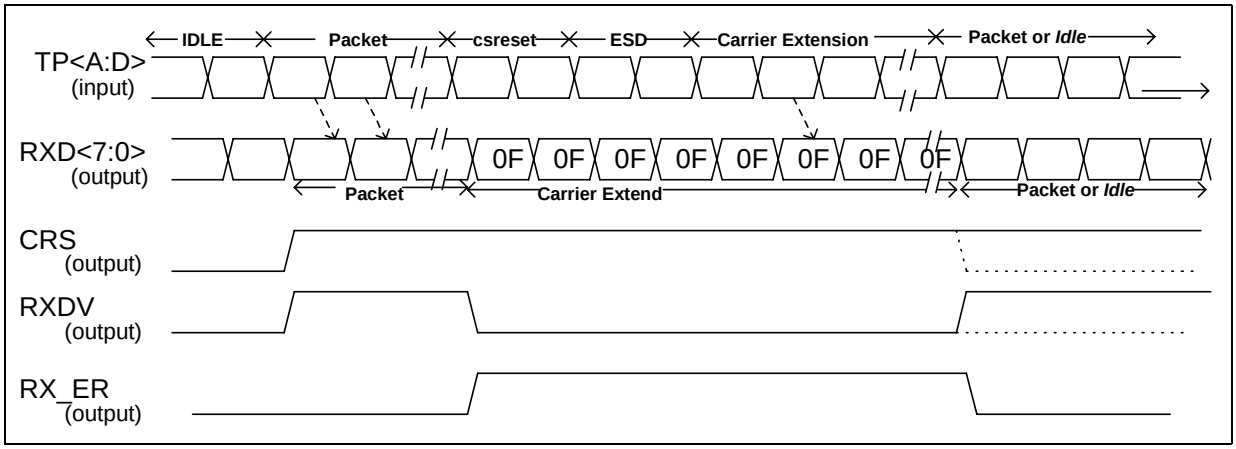


Figure 29. 1000BASE-T Reception, Carrier Extension and Packet Concatenation



2.5.4.1.6 Carrier Extend/Packet Concatenation with Errors

Carrier Extension and Packet Concatenation with errors are shown in Figure 30 on page 57 and Figure 31 on page 57. The sequence of events is identical to the simple carrier extend case with two exceptions:

- If the MAC transmits other than “0F” on the TX_D lines while it drives TX_ER, the LXT1000 responds by sending csreset, ESD and carrier-extend-with error symbols.
- If the LXT1000 receives carrier-extend-with-error, it asserts RX_ER and CRS and drives “1F” on the RX_D lines.

Figure 30. 1000BASE-T Transmission Extend - Packet Concatenation and Carrier Extension, with Errors

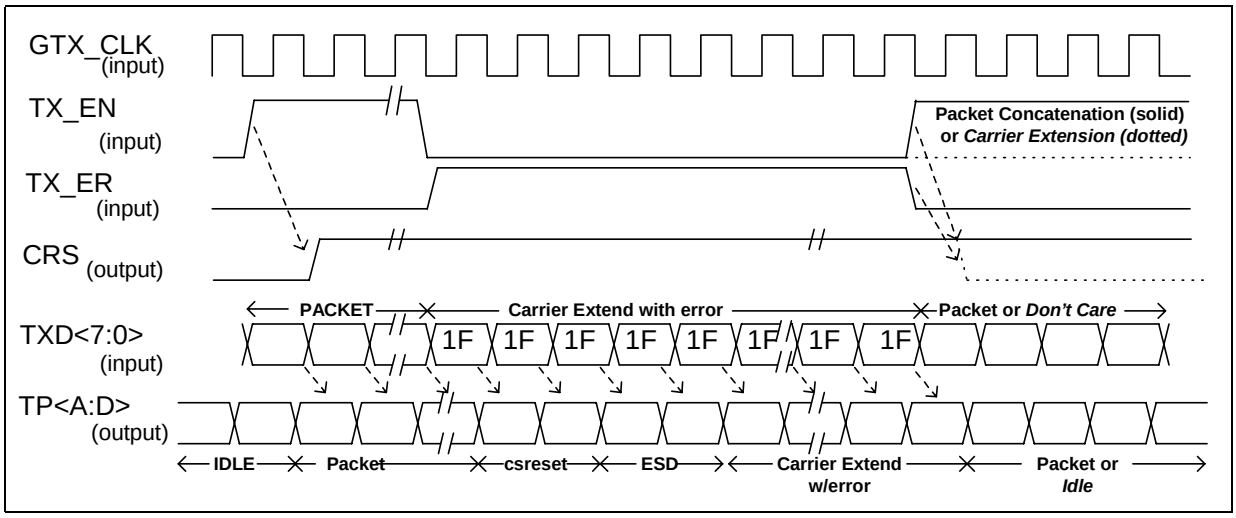
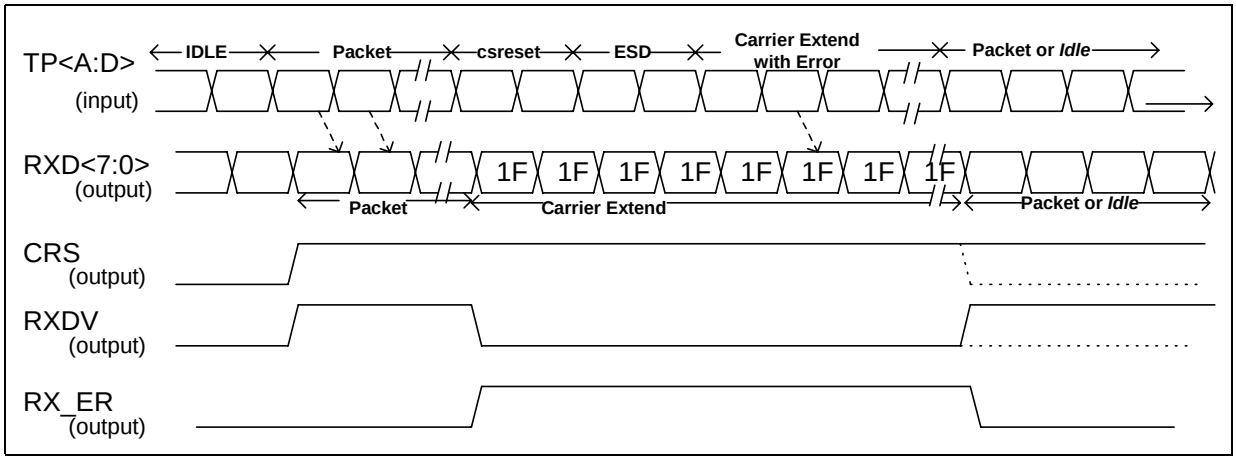


Figure 31. 1000BASE-T Reception Extend - Packet Concatenation and Carrier Extension, with Errors

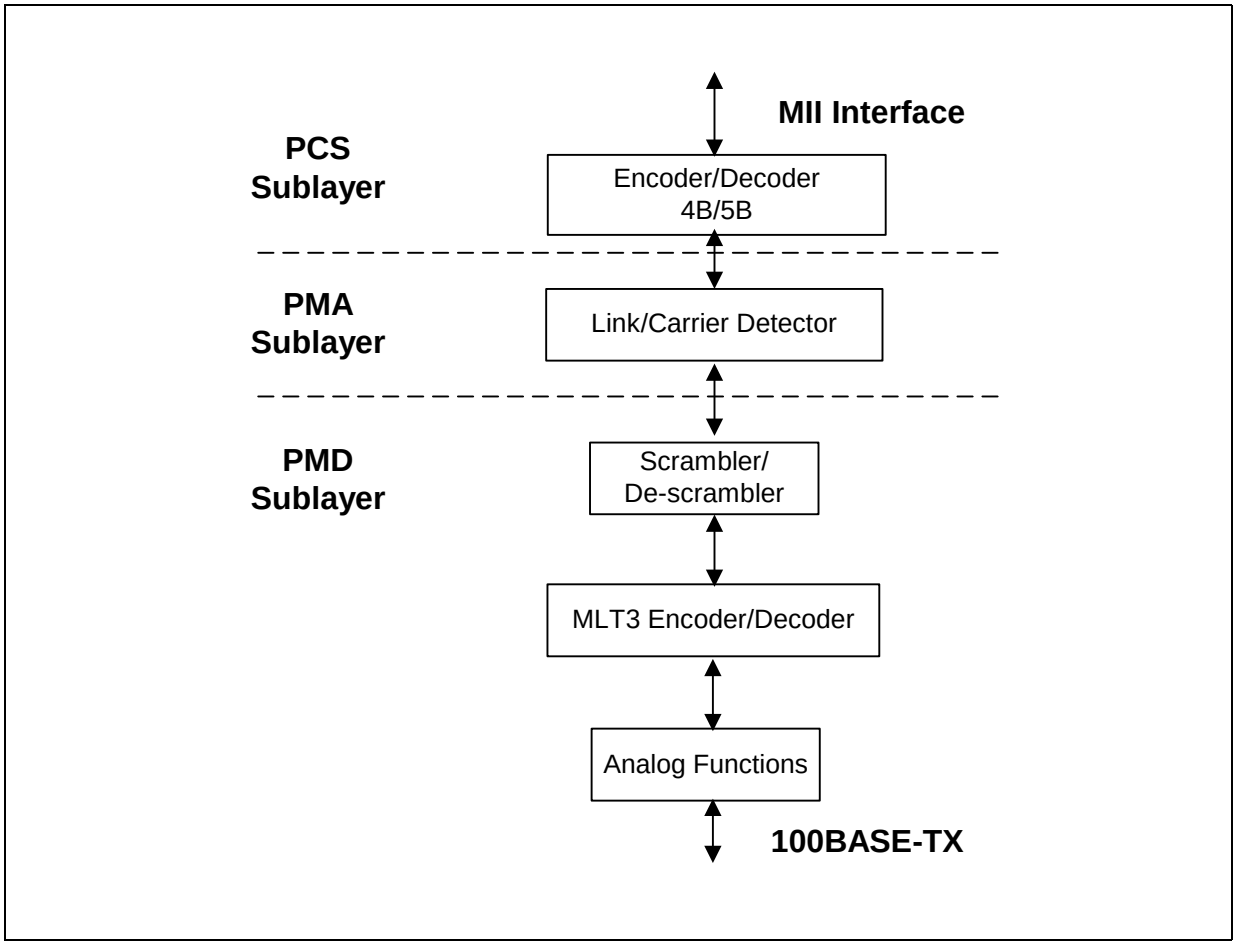


2.6 100 Mbps Operation

2.6.1 Protocol Support

Figure 32 shows the protocol sublayers and associated functions, each of which are discussed individually in the proceeding sections.

Figure 32. Protocol Sublayers and Associated Functions



2.6.2 Digital Functions

2.6.2.1 4B/5B Encoder

The 4B/5B encoder translates 4B data nibbles to one of 32 5B symbols. Of the 32 5B symbols, 16 are used to represent data and 6 are used for control. The other 10 symbols are unused and are considered “invalid”. 100BASE-TX data flow is shown as Figure 34 on page 60. See “4B/5B Coding” on page 60.

2.6.2.2 Scrambler

The scrambler is an 11-bit Linear Feedback Shift Register (LFSR). It creates a random pattern that is “XORed” with the data before it is transmitted. The scrambler randomizes the data and reduces harmonics to improve EMI performance. The receiver automatically detects the seed for the descrambler from the transmitted pattern assuming that scrambled idle was transmitted. Thus an inter-packet gap is all that is required for the descrambler to initially lock. Once locked, the descrambler remains locked as long as it receives at least 12 Idle symbols within 2 ms.

2.6.2.3 MLT3 Encoder

The MLT3 encoder translates the encoded, scrambled data into an MLT3 waveform, which uses three signal levels (+1, 0, -1) that follow each other in an infinitely repeating loop (+1 -> 0 -> -1 -> 0 -> +1). A “1” baud causes a transition to the next level in the sequence, a “0” baud causes the sequence to remain at its present value. In order for the receive PLLs to function properly, a minimum density of “1s” is needed. 5B symbols with excessive numbers of “0s” (generally invalid) are avoided.

2.6.2.4 Link and Carrier Detector

The LXT1000 establishes a link whenever the scrambler becomes locked and remains locked for approximately 50 ms. Whenever the scrambler loses lock (not receiving 12 idle symbols during a 2 ms window), the link is taken down. The result is a very robust operation, filtering out any small noise “hits” that would otherwise disrupt the link. Furthermore, 100 Mbps idle patterns will not bring up a 10 Mbps link.

2.6.2.5 Baseline Wander Correction

The LXT1000 provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). If uncorrected, this wander can cause receiver errors, particularly at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent. “Killer Packets” have been created that exhibit worst case baseline wander characteristics. The LXT1000 baseline wander correction characteristics allow the LXT1000 to recover error-free data, even at long line lengths.

2.6.3 Analog Functions

On the transmit side, the analog functions consist of a DAC and a filter. On the receiver, they consist of an A/D, timing recovery, and AGC.

2.6.3.1 Transmitting/Receiving

The MAC asserts TX_EN and begins driving data on the TXD balls at the same time. The LXT1000 substitutes a start-of-stream delimiter (/J/K symbol pair) for the first two nibbles sent by the MAC (which are normally preamble - “55”). Then, it transparently encodes and scrambles the rest of the frame until the MAC de-asserts TX_EN at the end of the packet. In response, the LXT1000 drives an end-of-stream marker, /T/R, followed by idles, /I/I... (see Figure 35 on page 62).

The LXT1000 receives a valid start-of-stream delimiter, asserts CRS and RX_DV to the MAC, and immediately begins driving receive data on RXD<3:0>. It substitutes “55” (preamble) for the first two bytes of SSD. It then continues to continuously descramble and decode the packet until it encounters an end-of-stream marker, /T/R, at which point it de-asserts RX_DV and CRS (see Figure 36 on page 62).

Normal data transmission is implemented in 4-bit-wide (4B) nibbles to the MAC. If the 4B/5B encoder is bypassed, 5B symbol data (instead of 4B nibbles) is passed to the MAC. RX_ER, RX_DV, COL, and CRS signals continue to function as in normal 4B mode.

2.6.3.2 Collision Detection

If the LXT1000 is in half-duplex, and it sends and receives a packet at the same time, it asserts its collisions (COL) output (see Figure 37 on page 62).

2.6.3.3 False Carrier Detection

If the LXT1000 detects a false carrier, it asserts RX_ER and drives an “E” (4B) or “0E” (5B) on the bus.

2.6.3.4 Error Handling

When the MAC wants to transmit an error, it asserts TX_ER while TX_EN is asserted. The LXT1000 responds by driving “error” symbols /H/H on the line. If the LXT1000 receives error symbols on the line in the middle of a packet, it asserts RX_ER and drives an “E” (4B) or “OE” (5B) on the bus.

Figure 33. 100BASE-TX Frame Structure

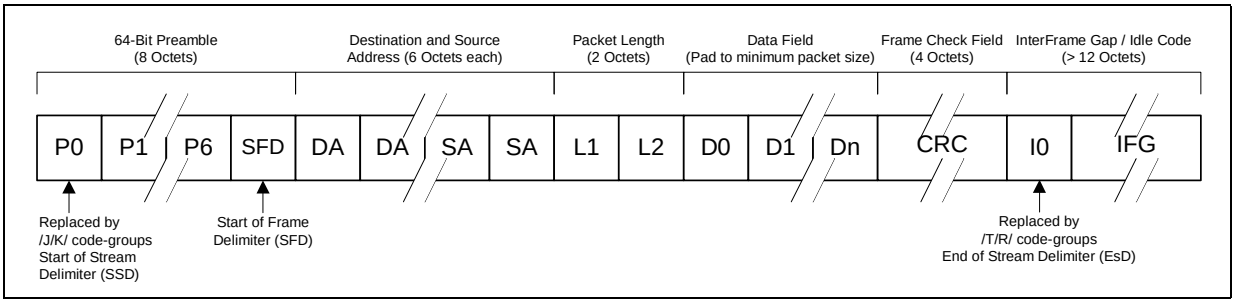


Figure 34. 100BASE-TX Data Flow

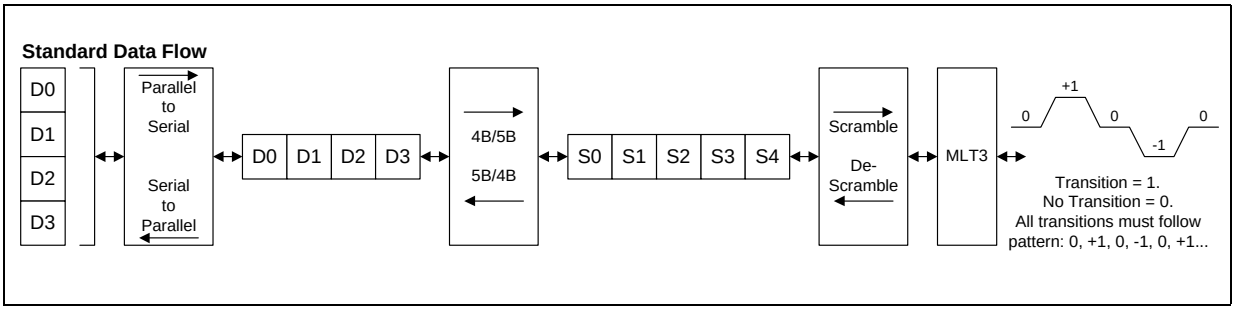


Table 24. 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Symbol 4 3 2 1 0	Interpretation
	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2

1. The /I/ (Idle) code-group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code-groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code-groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code-group is used to signal an error condition.

Table 24. 4B/5B Coding (Continued)

Code Type	4B Code 3 2 1 0	Name	5B Symbol 4 3 2 1 0	Interpretation
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
DATA	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 1 1	Idle. Used as inter-stream fill code
	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
CONTROL	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (SSD), part 1 of 2
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (SSD), part 2 of 2
	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
INVALID	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code-group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code-groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code-groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code-group is used to signal an error condition.

Figure 35. 100BASE-T Transmission (No Errors, No Collision, No Carrier Extension)

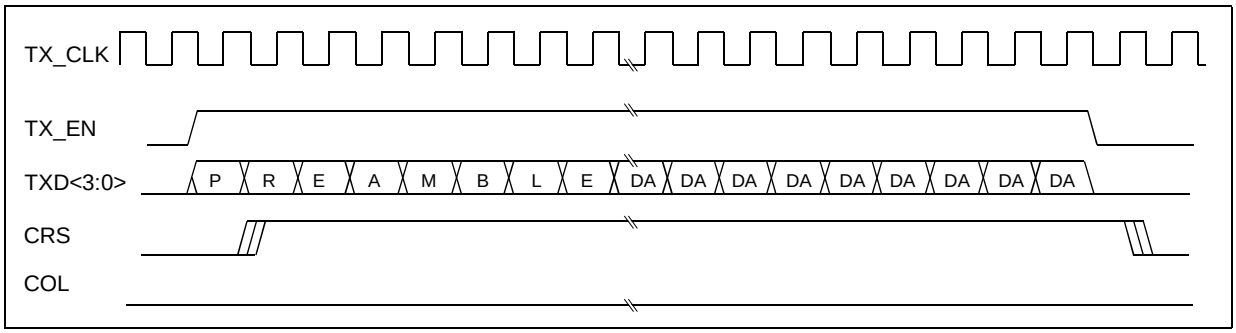


Figure 36. 100BASE-T Reception (No Errors, No Collision, No Carrier Extension)

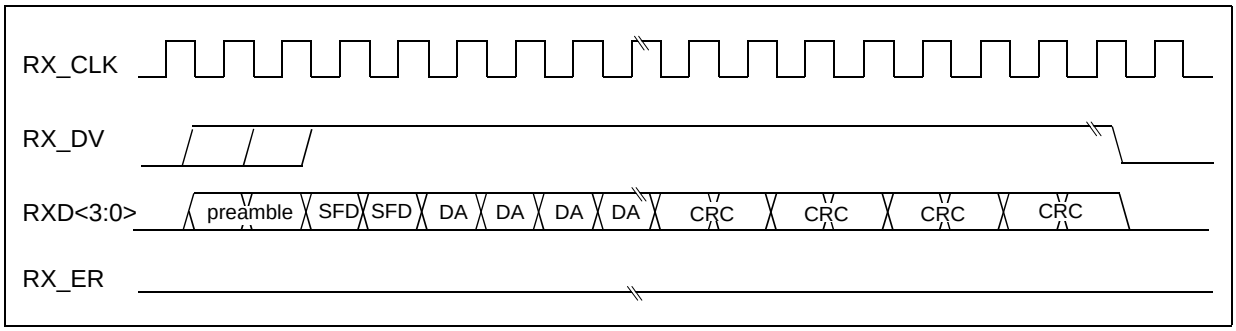
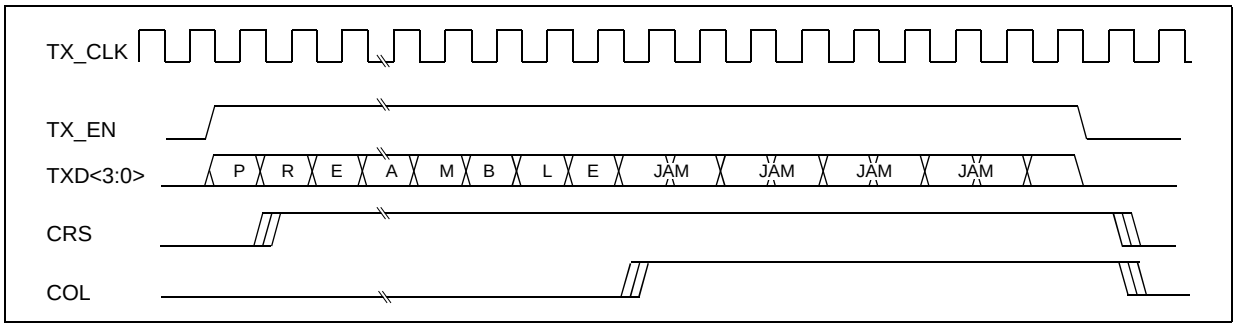


Figure 37. 100BASE-TX Transmission with Collision



2.7 10 Mbps Operation

The LXT1000 also operates as a 10BASE-T transceiver. The 10 Mbps MAC interface supports either MII mode 4B (4 bits x 2.5 MHz) or Serial mode (1 bit x 10 MHz) operations. The 10BASE-T transceiver includes a serializer/deserializer and Manchester encoder.

2.7.1 Transmitting/Receiving

In 10 Mbps mode, when the receiver detects preamble, it always asserts CRS immediately. Its next action depends on the state of bit 16.5. If 16.5 = 1, the LXT1000 strips the entire 10 Mbps preamble, asserting RX_DV starting with the start-of-frame marker “5D”. The first data driven on the RXD lines is the Ethernet Destination Address of the packet. If 16.5 = 0, the LXT1000 asserts RX_DV at the same time as CRS, and drives preamble on the lines.

Because 10 Mbps Ethernet uses a non-continuous carrier, the first preamble octets may be lost while the LXT1000 is synchronizing its receiver to the incoming packet. In addition, the LXT1000 may have to insert an additional octet of preamble when the SFD occurs in order to byte-synchronize the incoming data packet. For both these reasons, there exact number of preamble+SFD octets (8) may not be duplicated at the MAC Interface.

In either case, the LXT1000 continues asserting RX_DV and CRS and driving data onto the RXD balls until it detects an end-of-frame marker. At this point, it de-asserts RX_DV and CRS and the RXD signals.

The LXT1000 RX_CLK switches phase before a 10BASE-T packet is received. While the line is idle, the internal PLL that generates RX_CLK idles at the last known phase of the previous packet. When carrier is detected, the phase is adjusted in a glitch-free manner to match the incoming signal.

2.7.2 Polarity Correction

The LXT1000 automatically detects and corrects for the condition where the receive signal is inverted. Reversed polarity is detected if 8 inverted link pulses, or 4 inverted end-of-frame markers, are received consecutively. If link pulses or data are not received for 96-128 ms, the polarity state is reset to a non-inverted state.

2.7.3 Link Test

In 10 Mbps mode, the LXT1000 always transmit link pulses. If the link test function is enabled, it monitors the connection for link pulses. Once link pulses are detected, data transmission will be enabled and will remain enabled as long as either the link pulses or data transmission continue. If the link pulses stop, the data transmission will be disabled.

If auto-negotiation is disabled, the link will re-establish after a packet or four link pulses are received. If auto-negotiation is enabled, re-negotiation occurs.

2.7.4 Link Failure

Link failure occurs if Link Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT1000 returns to the auto-negotiation phase if auto-negotiation is enabled.

2.7.5 SQE (Heartbeat)

By default, the SQE (heartbeat) function is disabled on the LXT1000. To enable this function, set bit 16.9 = 1. When this function is enabled, the LXT1000 will assert its COL output for 5-15 Bit Times (BT) after each packet.

2.7.6 Jabber

If MAC transmission exceeds the jabber timer, the LXT1000 will disable the transmit and loopback functions and assert the COL ball. The LXT1000 automatically exits jabber mode 250-750 ms after the MAC ends transmission. The Jabber function can be disabled by setting bit 16.10 = 1.

2.7.7 Preamble Generation Mode

If preamble enable is enabled by setting bit 16.5 to a logical ‘1’, the MII RXD<3:0> bits will be set to the preamble value, x’5’ whenever a preamble is received. If the preamble enable mode is disabled, the RXD<3:0> bits will remain zero until the SFD is received. This mode may slightly increase the latency. In 10BASE-T serial mode, the preamble is always transferred to the RXD0 ball.

2.8 LXT1000 Operating Requirements

2.8.1 Power

While operating, the LXT1000 requires a 3.3V, 1.5A power supply to all VCC balls. Apply power to *all* VCC balls simultaneously. (Brief power-up transients to individual balls may be acceptable.) Drive input balls *only when power is supplied* to the device. When power is supplied, all input balls are 5V tolerant. Logic inputs, however, must meet the low and high voltage levels specified in this data sheet (see “Test Specifications” on page 75).

The MDIO/MDC interface cannot be powered separately from the rest of the MII interface.

2.8.2 Clock

A 25 MHz master clock source is required. The recommended means is to place a fundamental-mode, parallel-resonant, 25 MHz crystal with 100 ppm (or better) stability across the XI/XO balls.

As an alternative, a 25 MHz clock can be provided to the XI ball, provided it meets certain requirements (see Table 34 on page 77).

- Frequency error of no more than +/- 100 ppm
- Jitter of no more than 50 ps
- Rise-time no slower than 6 ns

2.8.3 RBIAS

A 10.7 kΩ, 1% resistor is required between the RBIAS input and ground. This resistor should be as close to the device as possible, and the traces as short as possible. Keep all high-speed signals away from the RBIAS ball. Use the traces from GND ball immediately adjacent to the RBIAS ball to enclose the resistor and ball, forming a shielded area between the RBIAS connection and the switching signals on the PCB.

2.8.4 GBIAS

Tie the GBIAS balls together, then tie to the anode of a 0.1µf capacitor, and the cathode of this capacitor to ground.

3.0 Application Information

3.1 Design Recommendations

3.1.1 Device Placement

The LXT1000 should be placed as close to the magnetics and RJ-45 connector as is possible, and no more than 6 to 9 inches away from the MAC or ASIC it is interfacing to.

The RBIAS resistor, GBIAS capacitor and MAC Interface series resistors should be placed as close to the LXT1000 as possible. Avoid high-speed signals in the vicinity of the RBIAS resistor. Pull-up and pull-down resistors and LEDs are less critical, and can be placed farther away.

3.1.2 Ground Plane Layout

The LXT1000 uses a single common logic ground plane for all digital and analog functions. Put as many ground-plane layers as is possible in the design. If possible, sandwich high-speed signals between two ground planes for better impedance control and for better EMI performance. Design the ground plane system to be as large and as quiet as possible, especially near the twisted-pair signals.

Be cognizant of the split between chassis ground (used for terminating external cables) and logic/ circuit ground. Keep the two planes completely separate (single-point ground) or thoroughly tie them together (multi-point ground). If the former, follow these rules:

- Run the split between the chassis ground and circuit ground directly under the magnetics.
- Reference the cables, chassis and line-side of the magnetics to chassis ground. Reference all devices, decoupling and bypass capacitors on the device side of the magnetics to circuit ground.
- Do not run any signals in the chassis ground region unless absolutely necessary (LEDs, for example).

In either case, the following always apply:

- Never run a high-speed signal across a break in a ground plane. Maintain continuous ground plane presence near all high-speed signals.
- Never loop ground planes.

3.1.3 Power Plane Layout and Filtering

A split analog/digital power plane is recommended for the LXT1000. For designs using multiple LXT1000s, one common digital VCC plane and one common analog VCC plane can be used for all devices.

The digital and analog VCC planes should be connected by one or more ferrite beads. The cumulative current rating of all beads should be the number of LXT1000 devices times 1.0A. Bulk capacitors (2.2, 4.7, or 10 µF) must be placed on each side of each ferrite.

3.1.3.1 Decoupling Capacitors

A decoupling capacitor must be placed near each LXT1000 VCC ball. A 0.01 µF value is recommended. Liberal and extensive use of decoupling capacitors throughout the design is highly recommended. The self-resonant frequency of the decoupling capacitors should be at least 125 MHz.

3.1.4 RBIAS and GBIAS Requirements

For RBIAS and GBIAS requirements, see "LXT1000 Operating Requirements" on page 64.

3.1.5 Twisted-Pair Layout

Each of the four signal pairs should be laid out differentially. The two traces must be kept close together, with no intervening traces or components other than the passive termination network. Layer changes should be avoided if at all possible. Keep traces short as possible, and shielded above and below with a quiet ground plane if possible.

The device-side center-tap of each winding must be supplied with the same 3.3V used to supply the analog VCC balls of the LXT1000. Each center-tap should be supplied with its own 0.01 µf decoupling capacitor to circuit ground.

Transformer isolation voltage should be rated at 2 kV to protect circuitry from static voltages across connectors and cables. Each line-side center-tap should have its own decoupling cap to chassis ground. Line-side center-taps must not be DC-shorted together.

3.1.6 MAC Interface Layout

Keep the signal lines as short as possible - no more than 6 to 9 inches; avoid "teeing" if at all possible. Note that the 802.3 specification does not support the use of any external connectors on the GMII Interface. The LXT1000's GMII pads are designed to drive a 50Ω trace with a single 5 pf load on the end.

Design the MAC Interface using external 42 Ω series terminations. Place the series terminations as close to the LXT1000 as is possible.

3.1.7 5V Tolerance Considerations

The inputs of the LXT1000 are 5V-compliant. These inputs tolerate 5V signal levels, even though the device is powered to 3.3V. This applies to all digital input balls, and the inputs on the GMII interface. Driving the GMII pads with 5V logic, however, may affect set-up and hold times, which must be calculated at the 1.5V threshold of the GMII. The output balls on the MAC Interface meet the electrical requirements for both the GMII and MII interfaces. The typical high output voltage (2.6V) may not meet the switching requirements of some CMOS 5V logic.

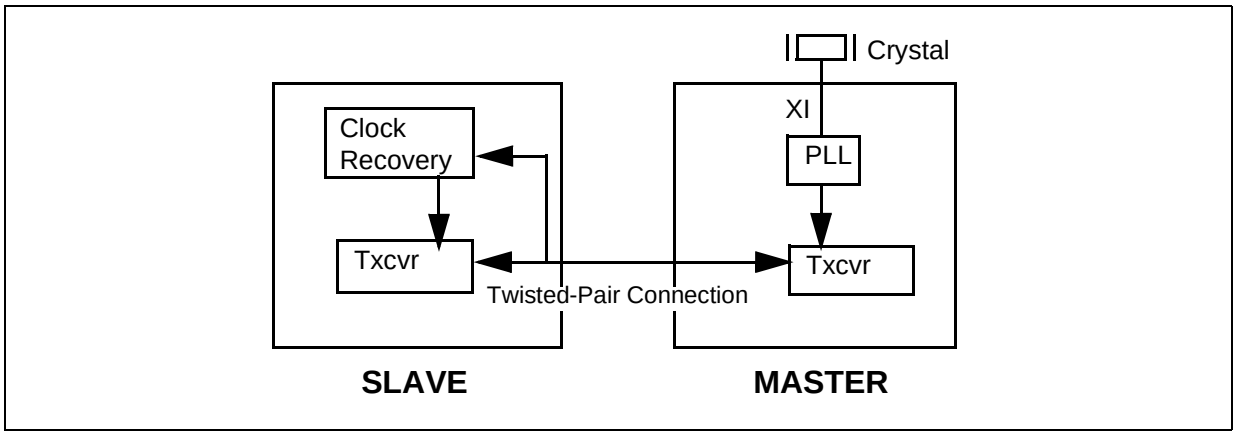
3.1.8 Master/Slave Relationship Details

Resolution of the Master-Slave relationship is a key part of gigabit auto-negotiation. As shown in Figure 38, every Gigabit link has a “Master” side and a “Slave” side. The Master synchronizes transmission to a local clock, while. the Slave synchronizes transmission to a clock that is recovered from the link. This keeps the transmitters on both sides of the link phase-locked to each other, which is necessary for echo cancellation.

In connections between multi-port devices (switches, for example) and single-port devices (NICs, for example), the typical preference is that the multi-port device be the Master and the single-port device be the Slave. For point-to-point links there is no preference.

The Master/Slave settings are configured prior to auto-negotiation. This can be done via software or hardware. Software configuration involves setting certain MII bits. Hardware configuration, which provides more limited capabilities, is done via external configuration balls on the LXT1000.

Figure 38. Master/Slave Relationship



3.1.8.1 Configuring Master/Slave in Software

Three MII Register bits (9.12, 9.11, 9.10) are used to configure the Master/Slave setting:

Bit 9.12

Bit 9.12 decides whether bit 9.11 or bit 9.10 is used to specify the Master/Slave setting.

If bit 9.12 = 0, then bit 9.10 is used.
If bit 9.12 = 1, then bit 9.11 is used.

Bit 9.11 is used when the Master/Slave setting is mandatory. If both sides use bit 9.11 and set it to the same value, a deadlock results (no link can be established). Bit 9.10 is used when the Master/ Slave setting is not mandatory. If both sides use bit 9.10 and set it to the same value, the conflict is resolved via a random number. If one side uses bit 9.11 and the other side uses bit 9.10, bit 9.11 takes precedence. The default state for bit 9.12 is 0 (select 9.10).

Bit 9.11

Bit 9.11 is used only when bit 9.12 = 1.

If bit 9.11 = 1, this node must be the master.
If bit 9.11 = 0, this node must be the slave.

Bit 9.11= 0 is the default state. By default, bit 9.11 is not used.

Bit 9.10

Bit 9.10 is used only when bit 9.12 = 0. The initial state of bit 9.10 is set by the Master/Slave configuration ball.
If bit 9.10 = 1, this node should be master.
If bit 9.10 = 0, this node should be slave.

3.1.8.2 Configuring Master/Slave in Hardware

The Master/Slave ball sets the default state of bit 9.10, which by default is the bit used to determine whether this node is a master or a slave. If the Master/Slave ball is High, the device indicates that it wants to be the master; if Low, the device indicates that it wants to be a slave.

Table 25. Configuring Master/Slave Relationship

Preference	Software Settings	Hardware Settings
Manual Master	9.12 = 1, 9.11 = 1	None
Multi-port Device	9.12 = 0, 9.10 = 1	Master = High
Single-port Device	9.12 = 0, 9.10 = 0	Master = Low
Manual Slave	9.12 = 1, 9.11 = 0	None

3.1.8.3 Resolution of the Master/Slave Relationship

The multi-port and single-port settings guarantee resolution of the Master/Slave relationship, but not a specific outcome. If both sides choose the same setting, a winner is randomly picked. In contrast, the manual settings result either in the specified setting or a deadlock. Manual settings take precedence over single-port and multi-port settings. Identical manual settings result in a deadlock. Identical single-port or multi-port settings are resolved by a random number. These relationships are summarized in Table 26.

Table 26. Master/Slave Preferences/Outcomes

Preferences		Outcome	
LXT1000	Link Partner	LXT1000	Link Partner
Manual Master	Manual Master	Deadlock - link doesn't come up.	
Manual Master	Any other setting	Master	Slave
Multi-port Device	Manual Master	Slave	Master
Multi-port Device[1]	Multi-port Device	Resolved by a random number.	
Multi-port Device	Manual Slave or Single-Port Device	Master	Slave
Single-port Device[1]	Manual Master or Multi-port Device	Slave	Master

1. If both sides choose "Multi-port Device" or "Single-Port Device", they exchange random numbers, and the side with the higher number prevails.

Table 26. Master/Slave Preferences/Outcomes

Preferences		Outcome	
LXT1000	Link Partner	LXT1000	Link Partner
Single-port Device	Single-port Device	Resolved by a random number.	
Single-port Device	Manual Slave	Master	Slave
Manual Slave	Any other setting	Slave	Master
Manual Slave	Manual Slave	Deadlock - link doesn't come up.	

1. If both sides choose "Multi-port Device" or "Single-Port Device", they exchange random numbers, and the side with the higher number prevails.

3.2 Test Information

3.2.1 Forced Gig Operation

For test purposes, Gigabit links may be brought up in forced mode, bypassing auto-negotiation that is normally required to bring up the link. To bring up a forced link:

- Disable auto-negotiation by tying the AN_EN input Low, or setting MII Register bit 0.12 = 0.
- Force the speed to 1000 Mbps by setting the SPEED<2:0> balls to "100" or setting MII bits 0.13 and 0.8 = 0 and 0.6 = 1.
- Set one side to "Master" by setting the MASTER input ball High, or setting MII bits 9.12 and 9.11 = 1.
- Set the other side to "Slave" by setting the MASTER input ball Low, or setting MII bit 9.12 = 1 and 9.11 = 0.

3.2.2 Gigabit Transmit Test Clock

The PAUSE and DUPLEX inputs may be re-configured as output balls that drive a differential 125 MHz transmit test clock. This test clock is required by the 802.3 standard, and is used to verify that the device meets jitter requirements. This test mode is enabled by setting bit 21.15 = 1. When used in this mode, the two clock outputs should be terminated by 50Ω tied to VCC. Refer to the *LXT1000 Design and Layout Guide* for more details.

3.2.3 Scrambler/Encoder Disable (100M)

For testing purposes, the 100 Megabit scrambler and encoder can be independently disabled. Disabling the encoder causes the MII interface to operate as a 5-bit symbol mode interface, rather than the normal 4-bit mode transmission. RXD4 and TXD4 accommodate MACs accepting 5-bit symbols. In this "5B" mode, the MAC is responsible for generating all PHY layer encoding, including SFD, EFD, and idle code.

To disable the encoder when a 100M link has been established, set bit 16.11 = 1. To disable the 100M scrambler, set bit 16.12 = 1. To return to normal 100M operation, set 16.11 = 0 and 16.12 = 0.

3.3 Magnetics Information

The LXT1000 features a simple 1:1 turns ratio requirement for connection to the transmission line. The hybrid is integrated into the LXT1000 and is not required in the magnetic. Refer to Table 27 for transformer requirements.

Transformers meeting these requirements are available from various manufacturers. Designers should test and validate all magnetics before using them in production.

Table 27. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Turns Ratio	–	1:1	–	–	–
Insertion Loss	0.0	–	1.1	dB	0.1 - 1 MHz
	–	–	0.5	dB	1 - 60 MHz
	–	–	1.0	dB	60 - 100 MHz
	–	–	1.2	dB	100 - 125 MHz
Primary Inductance	350	–	–	µH	
Transformer Isolation	–	1.5	–	kV	
Differential to common mode rejection	42	–	–	dB	0.1 - 30 MHz
	37	–	–	dB	30 - 60 MHz
	33	–	–	dB	60 - 100 MHz
Common to common mode rejection	30	–	–	dB	0.1 - 100 MHz
Return Loss[1]	16	–	–	dB	0.1 - 30 MHz
	12.5	–	–	dB	30 - 40 MHz
	11.5	–	–	dB	40 - 50 MHz
	10.0	–	–	dB	50 - 100 MHz
Crosstalk	40	–	–	dB	0.1 - 30 MHz
	38	–	–	dB	30 - 60 MHz
	33	–	–	dB	60 - 100 MHz
Rise Time	–	1.6	1.8	ns	10% to 90%

1. Return loss for transmit fails the IEEE 802.3 template for 100BASE-TX and 1000BASE-T with 115Ω load at 40 MHz corner. Does not fail if cable is IEEE-compliant.

3.4 Component Manufacturers

Table 28. Component Manufacturers

Component	Manufacturer	Part Number
Magnetics	Pulse Engineering	H5007
Magnetics	Bel Fuse Inc	S558-5999-M9
Magnetics	Halo	TG1G-3506NZ

3.5 Typical Application Circuitry

3.5.1 Typical NIC Application

Figure 39 shows the typical MII/GMII Interface. A typical application of the LXT1000,

Figure 40 on page 73 groups similar signals; it does not portray the actual chip pin out. The MII is at the upper left and Hardware Control Interface at center left.

Figure 41 on page 74 details the twisted-pair interface of a typical NIC application.

Figure 39. Typical MII/GMII Interface

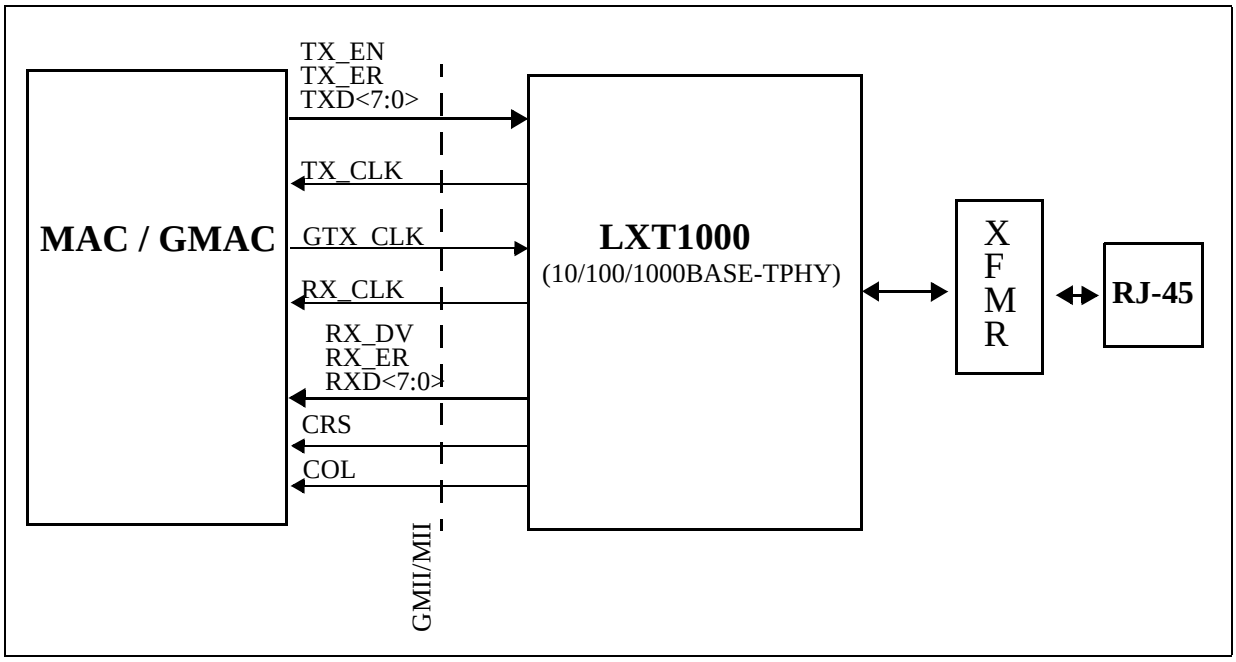


Figure 40. Typical Configuration - GMII Interface

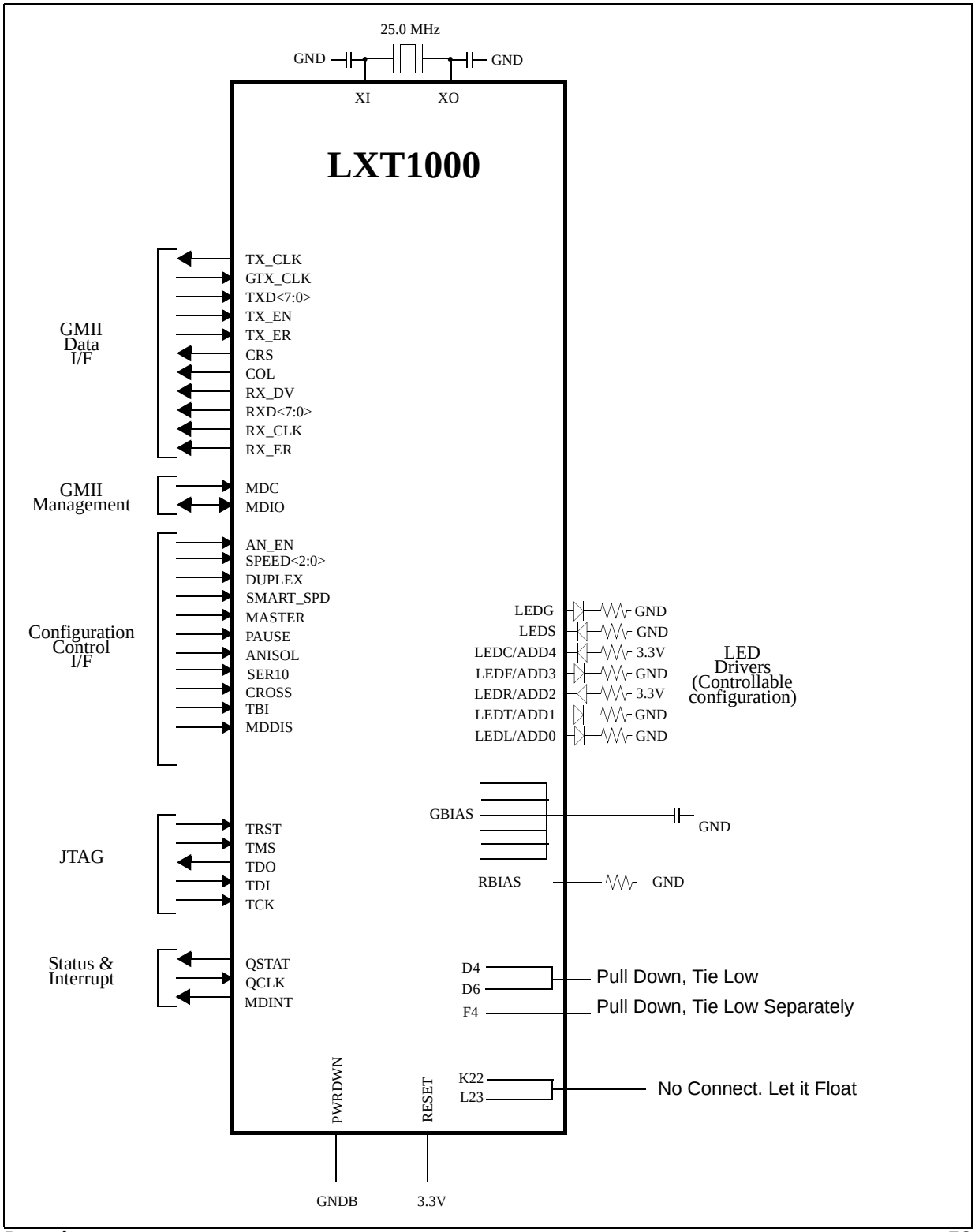
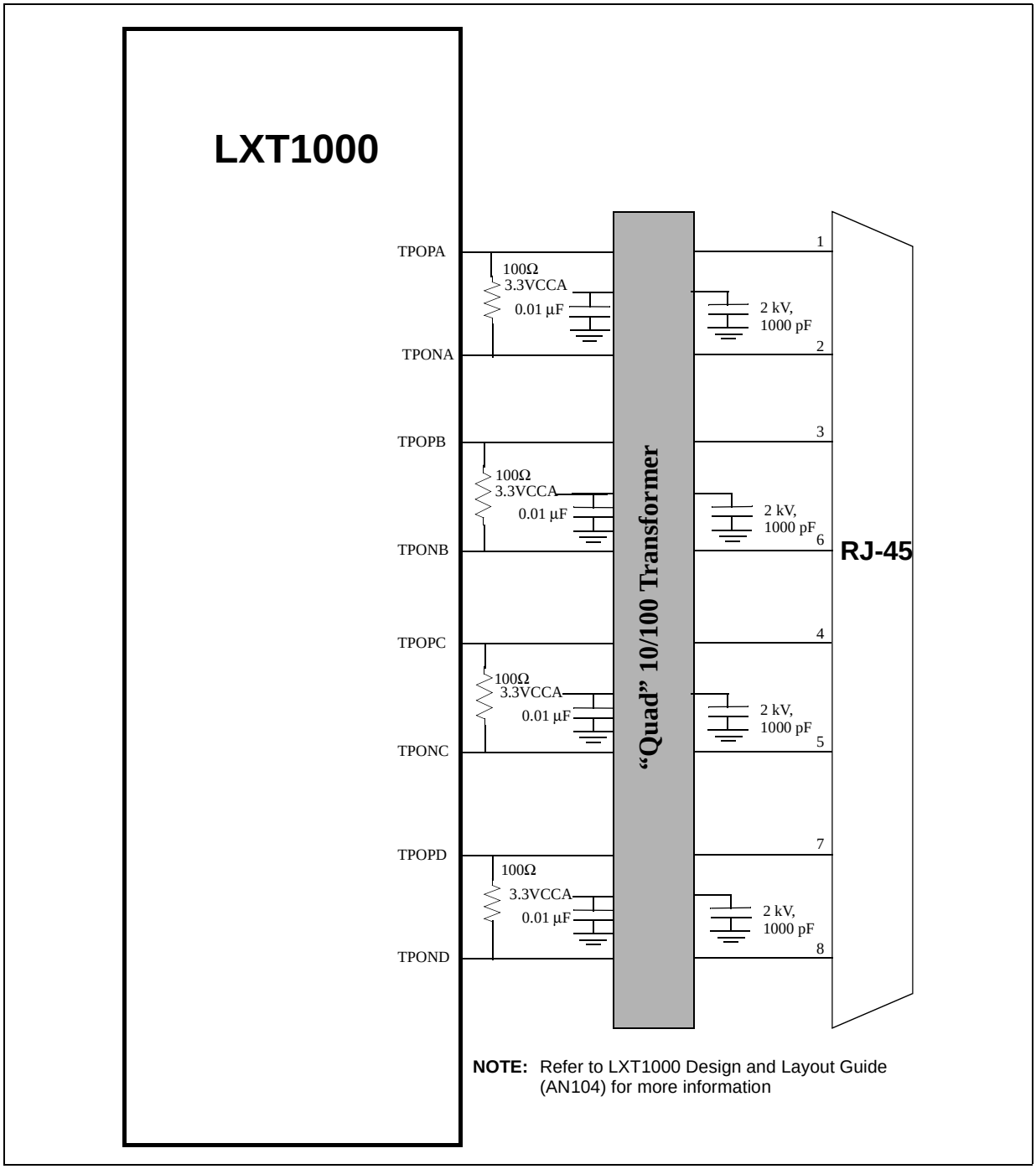


Figure 41. NIC Application - Twisted-Pair Interface



NOTE: Refer to LXT1000 Design and Layout Guide (AN104) for more information

4.0 Test Specifications

Note: Table 29 through Table 52 and Figure 42 through Figure 57 represent the design specifications of the LXT1000 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 30 through Table 52 are guaranteed over the recommended operating conditions specified in Table 30.
(Test Specifications remain under development.)

Table 29. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
Supply Voltage	VCC	-0.3	3.6	V
Operating Temperature[1]	TOP	0	+55	ºC
Storage Temperature	TST	-65	+150	ºC
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.				
1. Refer to LXT1000 Thermal Design Considerations Application Note for operating temperature clarification.				

Table 30. Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units
Recommended Supply Voltage		VCC	3.15	3.3	3.45	V
Recommended Operating Temperature[2]		TOP				
Vcc Current	1000BASE-T	ICC		1.75		A
	100BASE-TX	ICC		0.45		A
	10BASE-T	ICC		0.25		A
	Auto-Negotiation	ICC		0.45		A
	Power-down mode	ICC	–	–		mA
1. Typical values are at 25° C and are for design aid only. Not guaranteed or production tested. 2. Refer to LXT1000 Thermal Design Considerations Application Note for operating temperature clarification.						

Table 31. GMII DC Specifications

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output High Voltage	Voh	2.40	2.60	3.60	V	Ioh = -1.0 mA, VCC = Min
Output Low Voltage	Vol	GND		0.50	V	Iol = 1.0 mA, VCC = Min
Input High Voltage	Vih	1.70		-	V	
Input Low Voltage	Vil	-		0.90	V	
Input Low Current	Iih	-		40	uA	VCC = MAX, Vin = 2.0V
Input High Current	Iil	-600		-	uA	VCC = Max, Vin = 0.4V
Output Source Impedance			8-12		ohms	
1. Typical values are at 25° C and are for design aid only. Not guaranteed or production tested.						

Table 32. GMII General AC Specifications

Parameter	Symbol	Min	Max	Units	Conditions
Clock Rise Time	tR	-	1.00	ns	Vil_ac(max) to Vih_ac(min), 5pf load
Clock Fall Time	tF	-	1.00	ns	
Clock Slew Rate	-	0.6	-	V/ns	Vil_ac(max) to Vih_ac(min) or Vih_ac(min) to Vil_ac(max)
Input Low Voltage AC	Vil_ac	--	0.70	V	--
Input High Voltage AC	Vih_ac	1.90	--	V	--
GTX_CLK Frequency		125 -100 ppm	125 +100 ppm	MHz	
GTX_CLK, RX_CLK Time High		0.6		ns	
GTX_CLK, RX_CLK Time Low		0.6		ns	
Output Set-up Time RXD, RX_DV, RX_ER setup to ↑ RX_CLK		2.5		ns	
Output Hold time RXD, RX_DV, RX_ER hold from ↑ RX_CLK		0.50		ns	
Input Set-up time TXD, TX_EN, TX_ER setup to ↑ GTX_CLK		2.00		ns	
Input Hold time (receiver) TXD,TX_EN,TX_ER hold from ↑ GTX_CLK		0.00		ns	

Table 33. Other Digital I/O Characteristics[1]

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage[3]	V_{IL}	–	–	0.8	V	–
Input High voltage[3]	V_{IH}	2.0	–	–	V	–
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage[4]	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage[4]	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Applies to all digital balls except GMII balls.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. Does not apply to XI, QCLK, or TCK.
4. The LEDs are capable of sourcing/sinking up to 10 mA drive, but do not meet the listed V_{OL}/V_{OH} characteristics.

Table 34. Required Clock Characteristics

Parameter	Min	Nom	Max	Units	Test Condition
Frequency	–	25.0	–	MHz	
Frequency Stability	-100	–	+100	ppm	-40 – 85°C
Effective Series Resistance			50	ohms	At 25 MHz. Applies to crystals only
Rise Time			6	ns	Applies to oscillators only
Jitter			50	ps	>5 kHz, applies to oscillators only

Table 35. 1000BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VOP	0.67		0.82	V	802.3ab Test Mode 1
Signal amplitude symmetry	Vss			1	%	802.3ab Test Mode 1
Signal scaling	Vsc			2	%	From 1/2 of average Vop; Test Mode 1
Output Droop	Vod	73.1			%	Test Mode 1
Transmitter Distortion				10	mV	802.3ab Distortion Processing
Peak-to-Peak Transmitter Timing Jitter Measurements[2]						
Ref. to MASTER Tx TCLK				1.4	ns	peak-to-peak
MASTER-to-Transmit Output	T_a			0.30	ns	5 kHz HPF
MASTER-to-SLAVE Tx TCLK				1.4	ns	peak-to-peak
SLAVE-to-Transmit Output				T_a +0.4	ns	32 kHz HPF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Filter specifications are listed in section 40.6.1.2.5 of IEEE 802.3 standard, typically single-pole, high-pass filters (HPF)

Table 36. 100BASE-TX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VOP	0.95		1.05	V	
Signal amplitude symmetry	Vss	98		102	%	
Signal rise/fall time	TRF	3.0		5.0	ns	
Rise/fall time symmetry	TRFS				ns	
Duty cycle distortion	DCD			±0.5	ns	
Overshoot/Undershoot	VOS			5	%	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 37. 10BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VOP	2.2	2.5	2.8	V	With transformer, line replaced by 100 Ω resistor
Transition timing jitter added by the MAU and PLS sections	-	0	2	11	ns	After line model specified by IEEE 802.3 for 10BASE-T MAU
Receiver						
Receive Input Impedance	ZIN	-	3.6	-	kΩ	
Differential Squelch Threshold	VDS	300	420	585	mV	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 38. 10BASE-T Link Integrity Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Time Link Loss Receive	TLL	50		150	ms	
Link Pulse	TLP	2		7	Link Pulses	
Link Min Receive Timer	TLR MIN	2		7	ms	
Link Max Receive Timer	TLR MAX				ms	
Link Transmit Period	Tlt	8	16	24	ms	
Transmit Link Pulse Width	Tlpw	60		150	ns	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

4.1 1000BASE-T Timing Parameters

Figure 42. 1000BASE-T GMII Transmit Timing

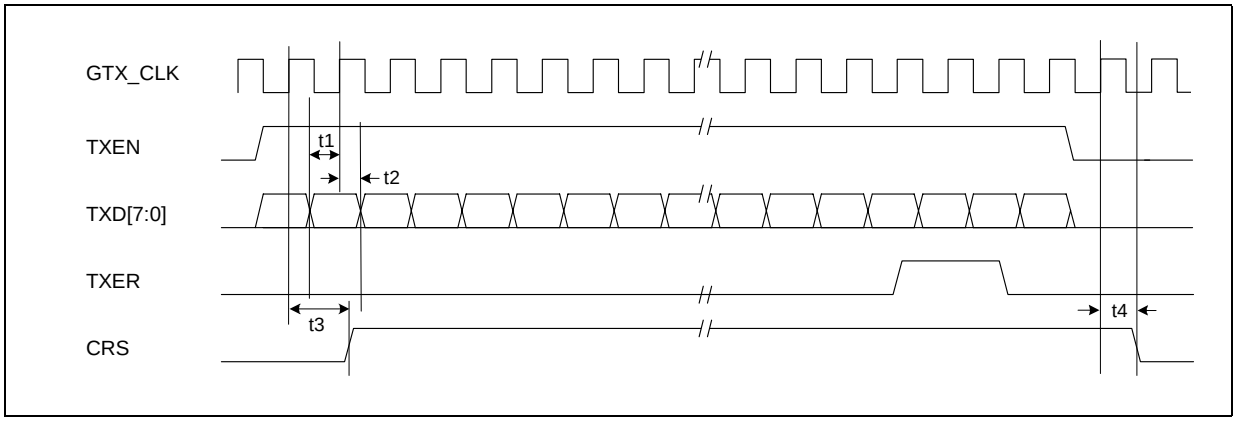


Table 39. 1000BASE-T GMII Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]
TXD<7:0>, TX_EN, TX_ER Setup to GTX_CLK High	t1	2.00			ns
TXD<7:0>, TX_EN, TX_ER Hold from GTX_CLK High	t2	0.00			ns
TX_EN sampled to CRS asserted	t3			16	BT
TX_EN sampled to CRS de-asserted	t4			16	BT
TX_EN sampled to twisted-pair out (Transmit latency)				84	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 1000BASE-T = 10^{-9} or 1 ns.

Figure 43. 1000BASE-T GMII Receive Timing

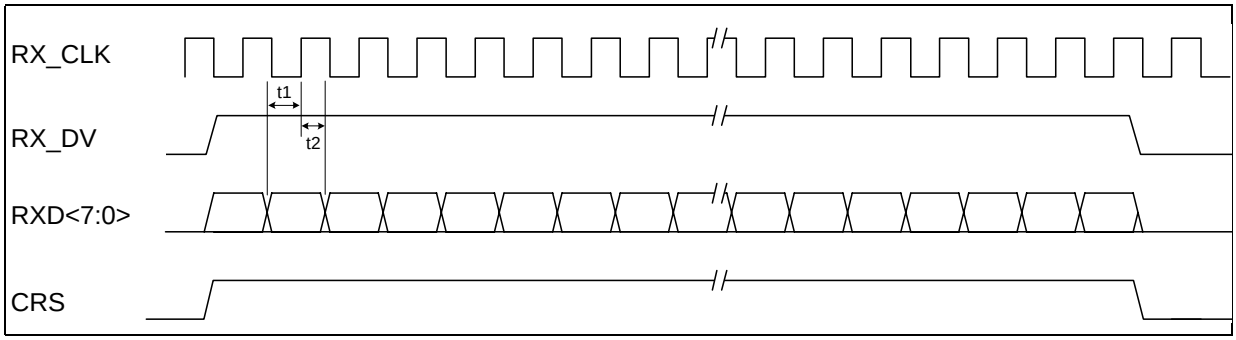


Table 40. 1000BASE-T GMII Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	2.50			ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	0.50			ns
Receive start of MDI input[3] to CRS asserted				244	BT
Receive start of MDI input[4] to CRS deasserted				244	BT
Receive start of MDI input[3] to COL asserted				244	BT
Receive start of MDI input[4] to COL deasserted				244	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 1000BASE-T = 10^{-9} or 1 ns
3. MDI input is first symbol of SSD.
4. MDI input is first symbol of CSReset.

4.2 100BASE-TX Timing Parameters

Figure 44. 100BASE-TX Transmit Timing

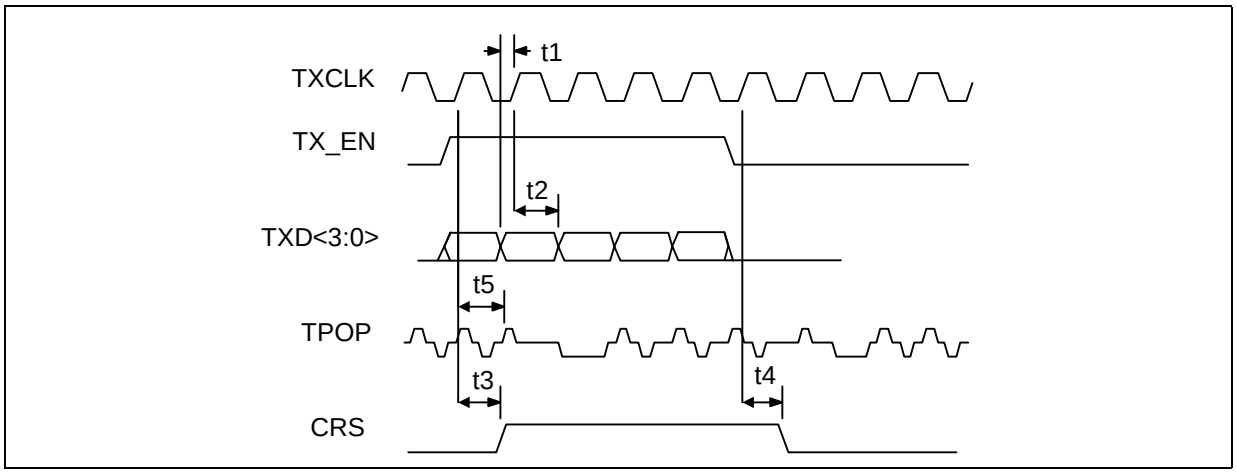


Table 41. GMII - 100BASE-TX Transmit Timing Parameters / 4B Mode

Parameter	Sym	Min	Typ[1]	Max	Units[2]
TXD<3:0>, TX_EN, TX_ER Setup to TX_CLK High	t1	10			ns
TXD<3:0>, TX_EN, TX_ER Hold from TX_CLK High	t2	0			ns
TX_EN sampled to CRS asserted	t3	0		4	BT
TX_EN sampled to CRS de-asserted	t4	0		16	BT
TX_EN sampled to TPO out (Transmit latency)	t5	6		14	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} or 10 ns.

Figure 45. 100BASE-TX Receive Timing

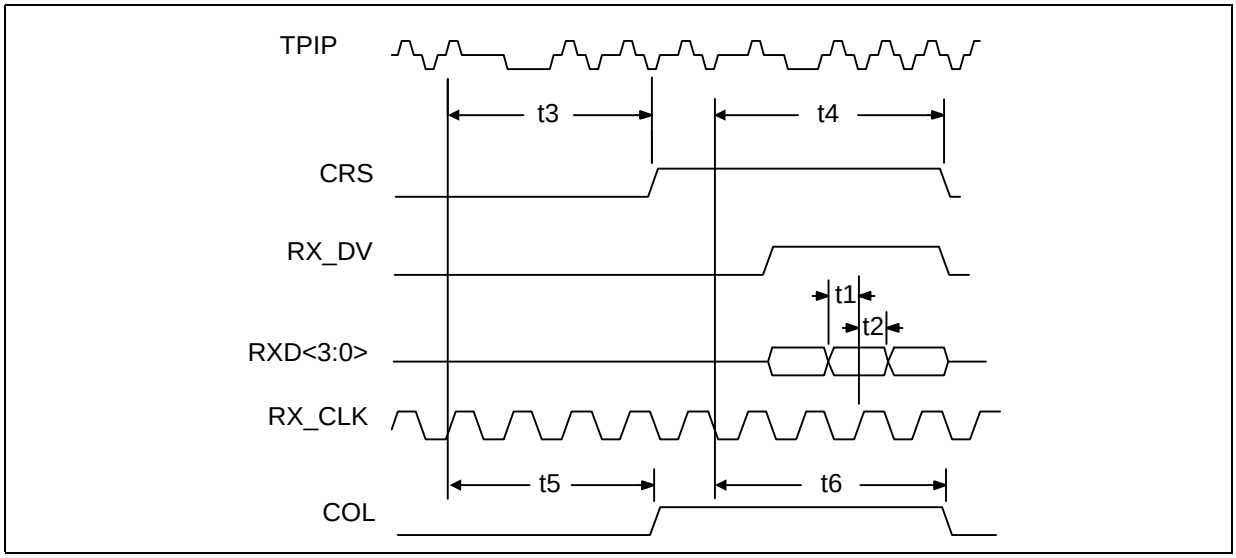


Table 42. GMII - 100BASE-TX Receive Timing Parameters / 4B Mode

Parameter	Sym	Min	Typ[1]	Max	Units[2]
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10			ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5			ns
Receive start of “J” to CRS asserted	t3			20	BT
Receive start of “T” to CRS de-asserted	t4	13		24	BT
Receive start of “J” to COL asserted	t5			20	BT
Receive start of “T” to COL de-asserted	t6	13		24	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} or 10 ns.

4.3 10BASE-T Timing Parameters

Figure 46. 10BASE-T MII Transmit Timing

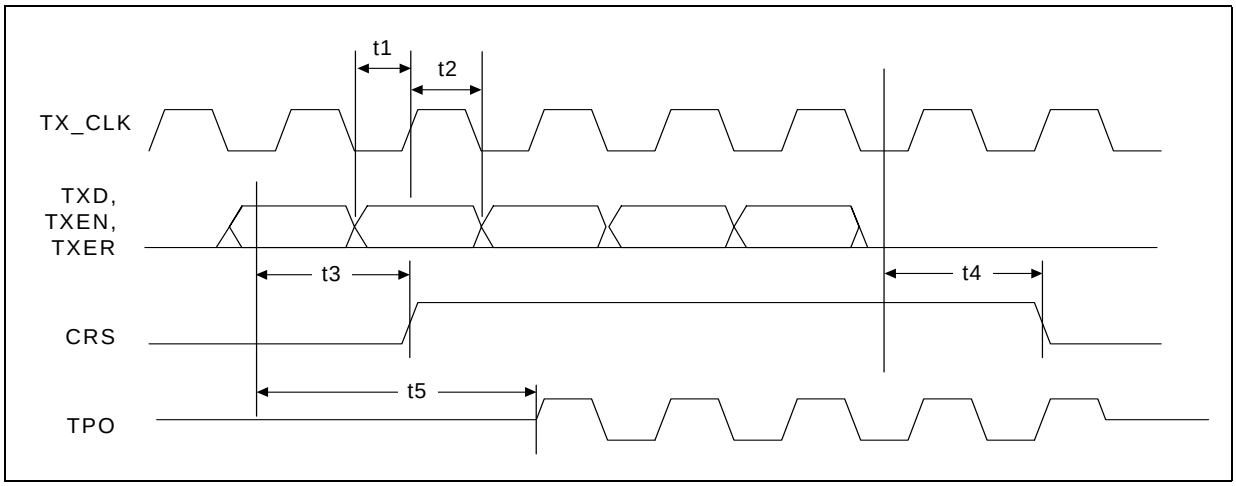


Table 43. GMII - 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]
TXD, TX_EN, TX_ER Setup to TX_CLK High	t1	10			ns
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2	0			ns
TX_EN sampled to CRS asserted	t3	0		4	BT
TX_EN sampled to CRS de-asserted	t4	0		16	BT
TX_EN sampled to TPO out (Tx latency)	t5	6		14	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 10BASE-T = 10^{-7}or 100 ns.

Figure 47. 10BASE-T Receive Timing

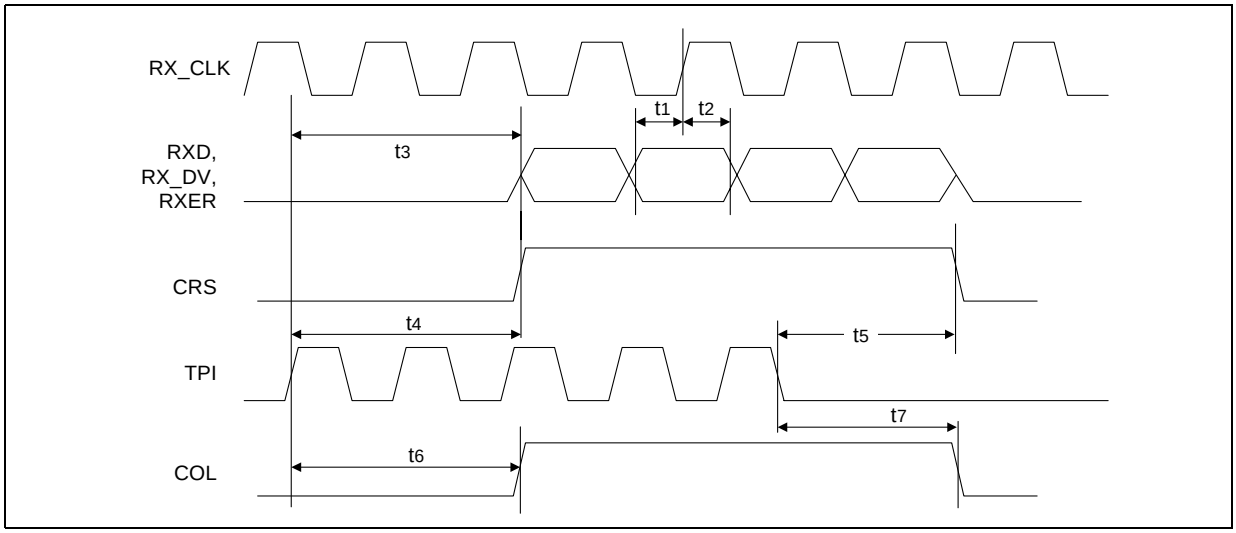


Table 44. GMII - 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10			ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5			ns
TPI in to RXD out (Rx latency)	t3			14	BT
TPI in to CRS asserted	t4			20	BT
TPI quiet to CRS de-asserted	t5	13		24	BT
TPI in to COL asserted	t6			20	BT
TPI quiet to COL de-asserted	t7	13		24	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 10BASE-T = 10^{-7}or 100 ns.

Figure 48. 10BASE-T SQE (Heartbeat) Timing

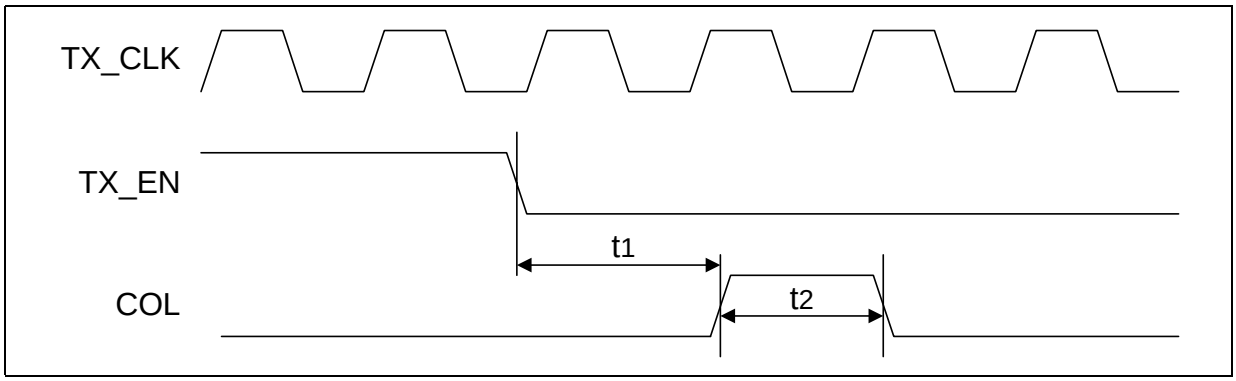


Table 45. 10BASE-T SQE (Heartbeat) Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units
COL (SQE) Delay after TX_EN off	t1	0.65		1.6	µs
COL (SQE) Pulse duration	t2	0.5		1.5	µs
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.					

Figure 49. 10BASE-T Jab and Unjab Timing

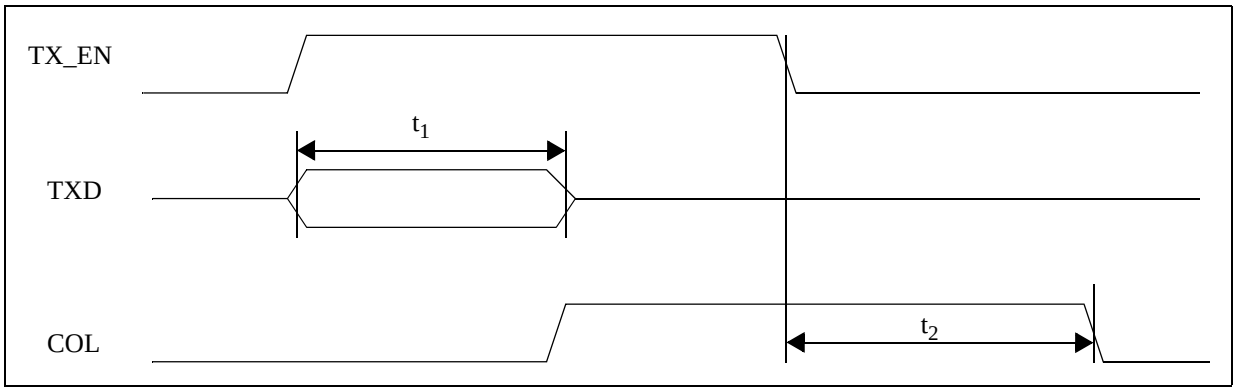


Table 46. 10BASE-T Jab and Unjab Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units
Maximum Transmit time	t1	20		150	ms
Unjab time	t2	250		750	ms
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.					

Figure 50. 10BASE-T Serial Transmit Timing

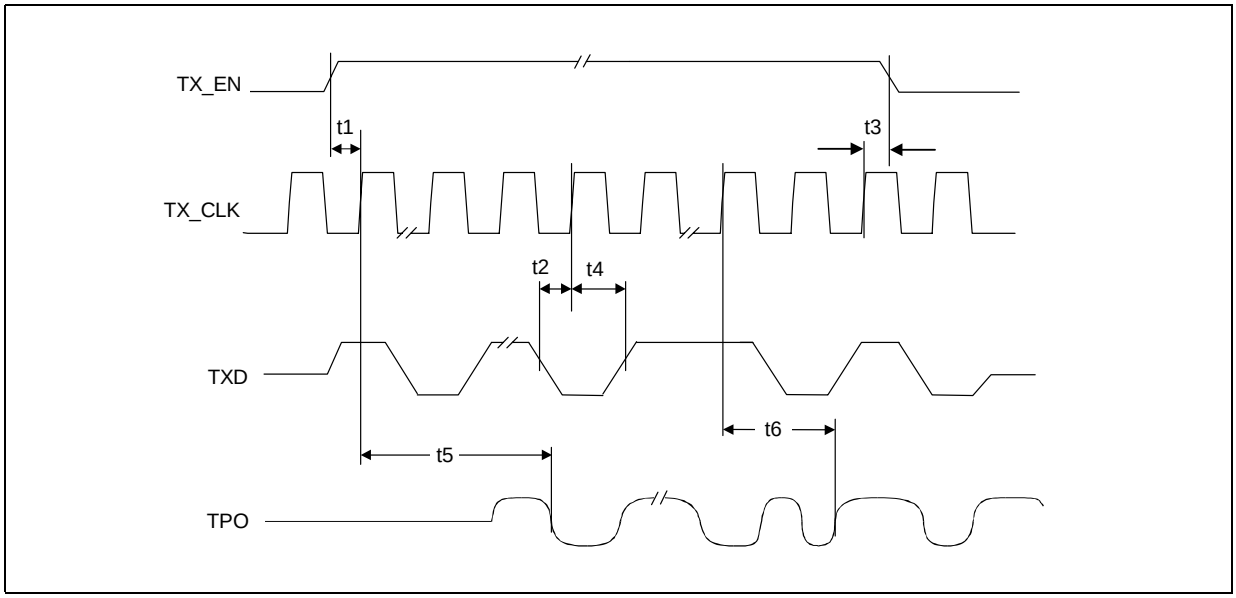


Table 47. 10BASE-T Serial Transmit Timing

Parameter	Symbol	Min	Typ[1]	Max	Units
TX_EN setup from TX_CLK	t1	22			ns
TXD<0> setup from TX_CLK	t2	22			ns
TX_EN hold after TX_CLK	t3	5			ns
TXD<0> hold after TX_CLK	t4	5			ns
Transmit Start-up delay	t5		430	450	ns
Transmit Latency	t6		300	350	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 51. 10BASE-T Serial Start-of-Frame Timing

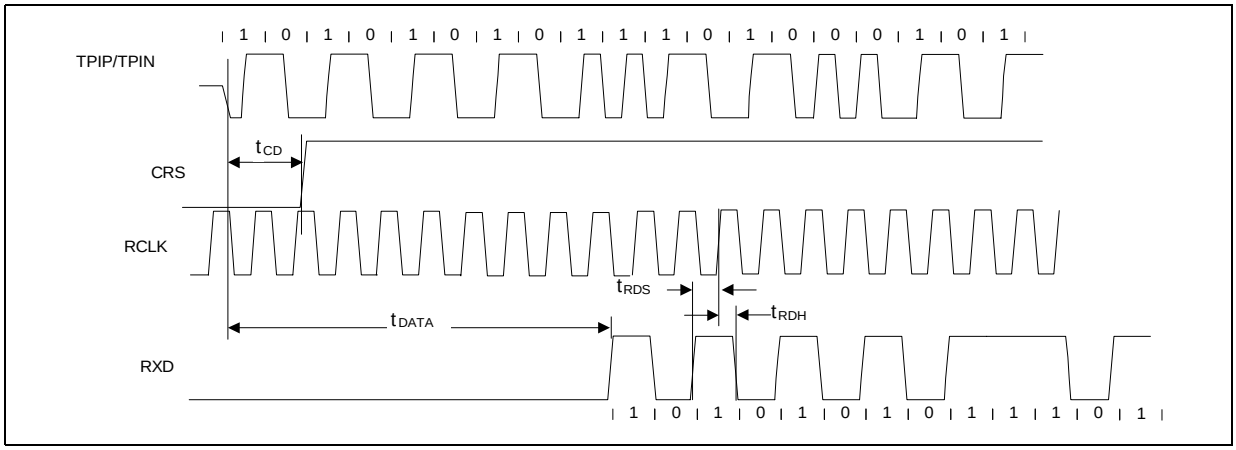


Table 48. 10BASE-T Serial Start-of-Frame Timing

Parameter	Symbol	Min	Typ[1]	Max	Units
Decoder Acquisition Time	tDATA	-	1900	3000	ns
CRS turn-on delay	tCD	-	425	550	ns
RXD setup from RX_CLK	tRDS	30	45	-	ns
RXD hold from RX_CLK	tRDH	30	45	-	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 52. 10BASE-T Serial End-of-Frame Timing

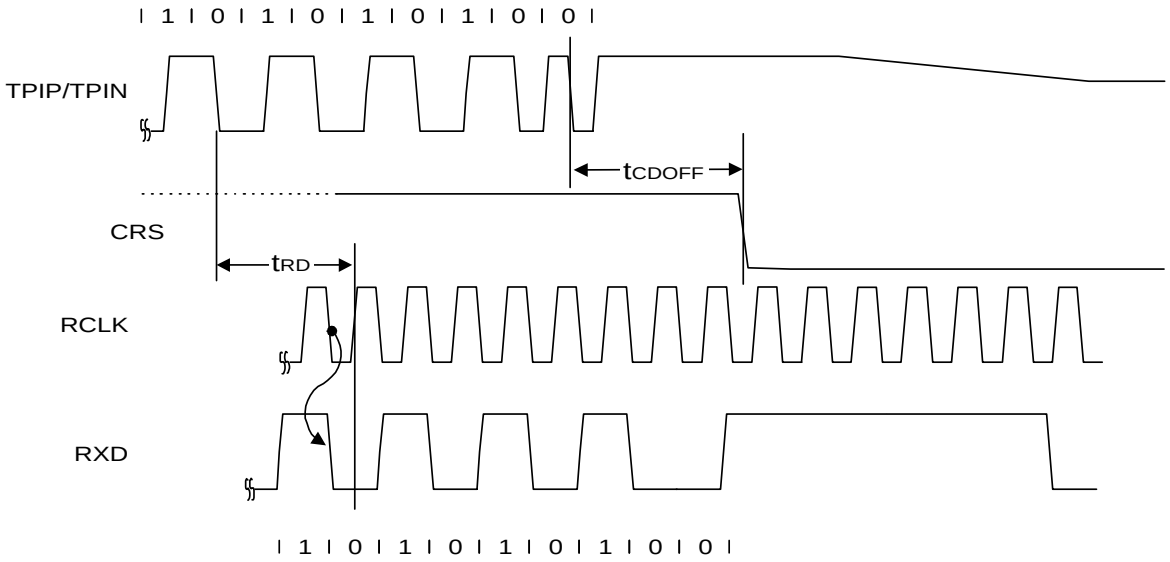


Table 49. 10BASE-T Serial End-of-Frame Timing

Parameter	Symbol	Min	Typ[1]	Max	Units[2]
RX_CLK after CRS off		5	-	-	BT
Receive latency	tRD	-	-	400	ns
CRS turn off delay	tCDOFF	-	-	530	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 10BASE-T = 10^{-7} or 100 ns.

4.4 Auto-Negotiation Timing Parameters

Figure 53. Fast Link Pulse Timing

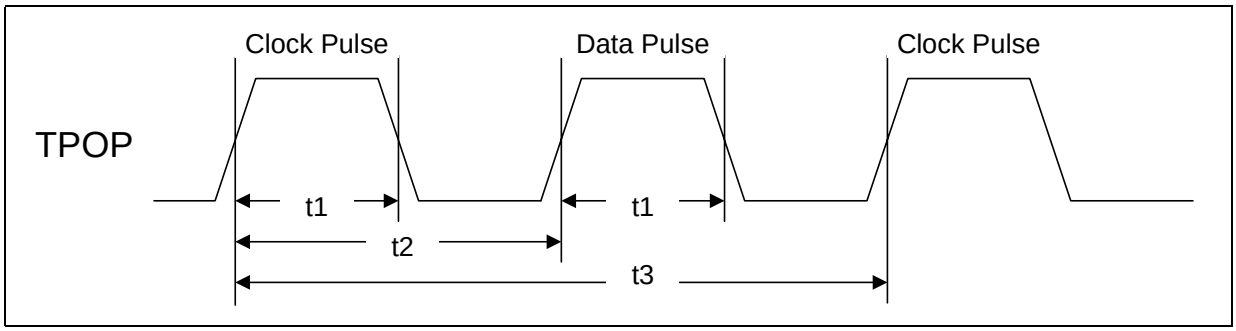


Figure 54. FLP Burst Timing

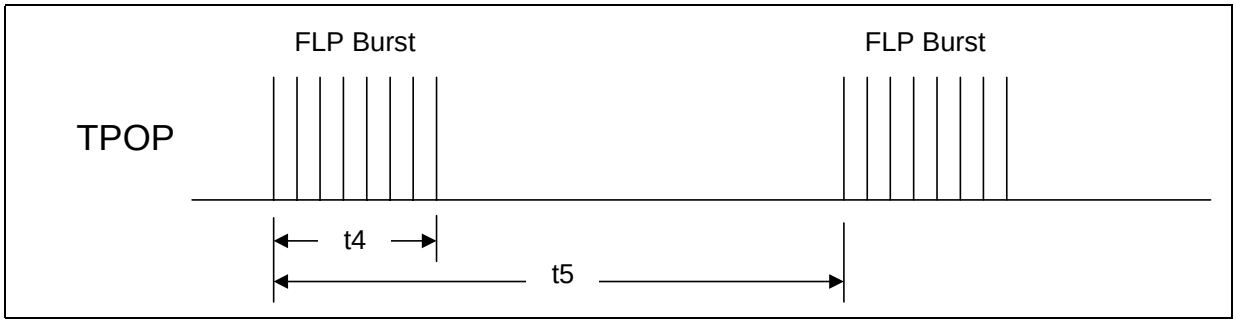


Table 50. Fast Link Pulse Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	–	100	ns	–
Clock pulse to Data pulse	t2	55.5	–	69.5	µs	–
Clock pulse to Clock pulse	t3	111	–	139	µs	–
FLP burst width	t4	–	–	2	ms	–
FLP burst to FLP burst	t5	8	–	24	ms	–
Clock/Data pulses per burst	–	17	–	33	ea	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

4.5 MDIO Timing Parameters

Figure 55. MDIO Write Timing

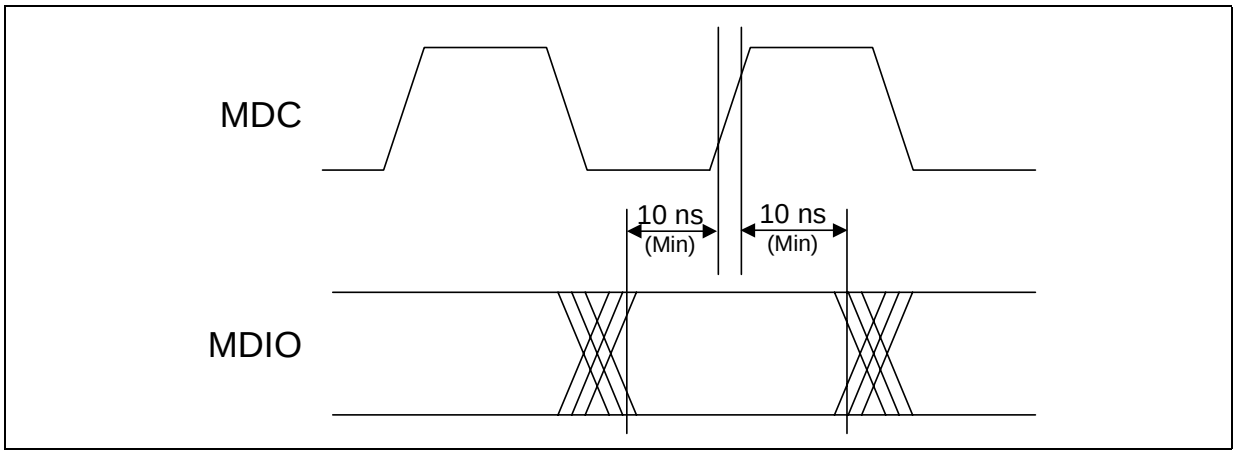


Figure 56. MDIO Read Timing

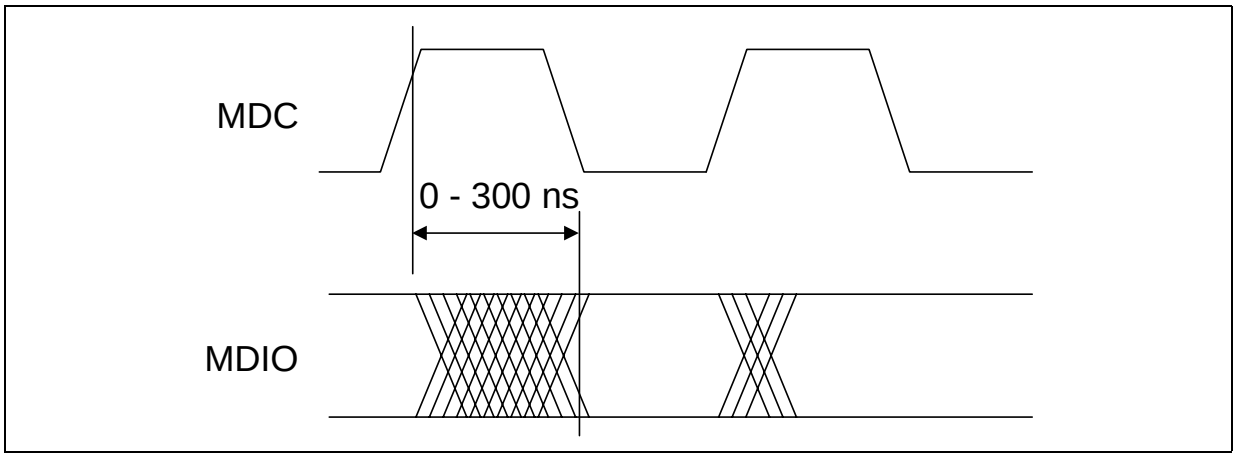


Table 51. MDIO Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO Setup before MDC		10		-	ns	When sourced by STA
MDIO Hold after MDC		10		-	ns	When sourced by STA
MDC to MDIO Output delay		10		300	ns	When sourced by PHY
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.						

4.6 QSTAT Timing Parameters

Figure 57. QSTAT Write Timing

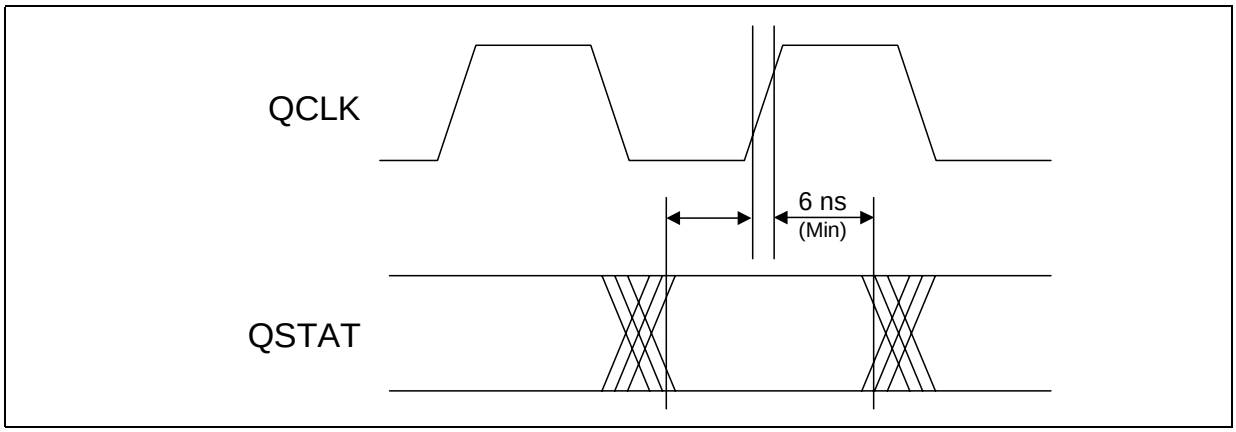


Table 52. QSTAT Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
QCLK to QSTAT Output delay		6.0	9.0	12.0	ns	
QCLK Frequency				25	MHz	
QCLK Duty Cycle		35		65	%	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

5.0 Register Set

Refer to Table Table 53 for a complete register listing.

- Base registers (0 through 10 and 15) are defined in accordance with the “Reconciliation Sublayer and Media Independent Interface” and “Physical Layer Link Signalling for 10/100/1000 Mbps Auto-Negotiation” sections of the IEEE 802.3.
- Additional registers (16 through 22) are defined in accordance with the IEEE 802.3 specification for adding unique chip functions.

Table 53. Register Set

Address	Register Name	Bit Assignments
0	Control Register	(Table 54 on page 91)
1	Status Register	(Table 55 on page 92)
2	PHY Identification Register 1	(Table 56 on page 92)
3	PHY Identification Register 2	(Table 57 on page 93)
4	A/N Advertisement Register	(Table 58 on page 93)
5	A/N Link Partner Base Page Ability Register	(Table 59 on page 94)
6	A/N Expansion Register	(Table 60 on page 95)
7	A/N Next Page Transmit Register	(Table 61 on page 96)
8	A/N Link Partner Rec’d Next Page Register	(Table 62 on page 96)
9	1000BASE-T/100BASE-T2 Control Register	(Table 63 on page 97)
10	1000BASE-T/100BASE-T2 Status Register	(Table 64 on page 98)
15	Extended Status Register	(Table 65 on page 98)
16	Port Configuration Register	(Table 66 on page 99)
17	Quick Status Register	(Table 67 on page 100)
18	Interrupt Enable Register	(Table 68 on page 101)
19	Interrupt Status Register	(Table 69 on page 102)
20	LED Configuration Register	(Table 70 on page 103)
21	Port Control Register	(Table 71 on page 104)
22	Reserved	
23	Reserved	
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Reserved	
29	Reserved	
30	Reserved	
31	Reserved	

Table 54. Control Register (Address 0)

Bit	Name	Description	Type [1]	Default
0.15	Reset	1 = PHY reset 0 = Normal operation	R/W SC	0
0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W	0
0.13	Speed Selection	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (manual mode not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	Note 2
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process This bit must be enabled for 1000BASE-T operation.	R/W	Note 3
0.11	Power Down	1 = Power down 0 = Normal operation	R/W	0
0.10	Isolate	1 = Electrically isolate PHY from GMII 0 = Normal operation	R/W	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = Normal operation	R/W SC	Note 4
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W	Note 5
0.7	Collision Test	1 = Enable COL signal test 0 = Disable COL signal test	R/W	Note 6
0.6	Speed Selection 1000 Mb/s	0.6 (Speed<1>) 0.13 (Speed<0>) 1 1 = Reserved 1 0 = 1000 Mbps (manual mode not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	Note 2
0.5:0	Reserved	Write as 0, ignore on Read	R/W	00000

1. R/W = Read/Write, RO = Read Only, SC = Self Clearing
2. If auto-negotiation is enabled, this bit is ignored. If auto-negotiation is disabled, the default value of bits 0.13 and 0.6 are determined by the SPEED<2:0> balls.
3. The default value of bit 0.12 is determined by ball AN_EN.
4. If auto-negotiation is enabled, the default value of bit 0.9 is determined by ball AN-RSTRT. If auto-negotiation is disabled, the default value of bit 0.9 = 0.
5. If auto-negotiation is enabled, this bit is ignored. If auto-negotiation is disabled, the default value of bit 0.8 is determined by ball DUP.
6. This bit is ignored unless loopback is enabled (0.14 = 1).

Table 55. Status Register (Address 1)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO	0
1.14	100BASE-X Full Duplex	1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X	RO	1
1.13	100BASE-X Half Duplex	1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X	RO	1
1.12	10 Mbps Full Duplex	1 = PHY able to operate at 10 Mbps in full-duplex mode 0 = PHY not able to operate at 10 Mbps full-duplex mode	RO	1
1.11	10 Mbps Half Duplex	1 = PHY able to operate at 10 Mbps in half-duplex mode 0 = PHY not able to operate at 10 Mbps in half-duplex	RO	1
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full-duplex 100BASE-T2 0 = PHY not able to perform full-duplex 100BASE-T2 (Not supported)	RO	0
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half-duplex 100BASE-T2 0 = PHY not able to perform half-duplex 100BASE-T2 (Not supported)	RO	0
1.8	Extended Status	1 = Extended status information in register 15 0 = No extended status information in register 15	RO	1
1.7	Reserved	1 = ignore when read	RO	0
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO	0
1.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault condition detected 0 = No remote fault condition detected	RO/LH	0
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detected 0 = Jabber condition not detected	RO/LH	0
1.0	Extended Capability	1 = Extended register capabilities 0 = Extended register capabilities	RO	1

1. R/W = Read/Write, RO = Read Only
2. LL = Latch Low, clear on read
3. LH = Latch High, clear on read

Table 56. PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI	RO	0013 hex

1. R0 = Read Only

Table 57. PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier composed of bits 19 through 24 of the OUI	RO	011110
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number **NOTE:** For devices prior to Revision C1: When read, the value returned is 03H.	RO	001100
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number Rev B7 5 C2 6 C3 7 C4 8		XXXX

1. R0 = Read Only

Figure 58. PHY Identifier Bit Mapping

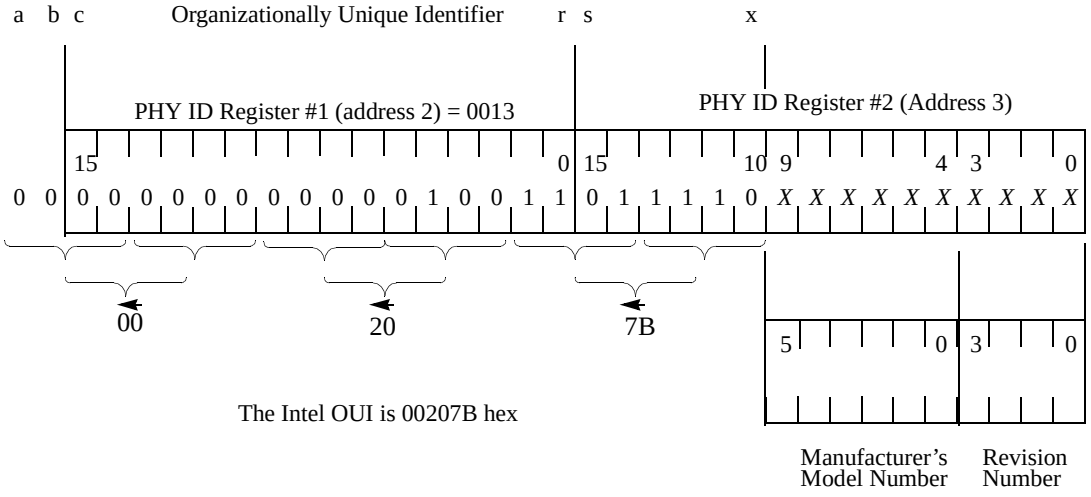


Table 58. Auto-Negotiation Advertisement Register (Address 4)[1]

Bit	Name	Description	Type [2]	Default
4.15	Next Page	1 = Manual Control of Next Page (Software) 0 = Device Control of Next Page (Auto)	R/W	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0

1. Restart auto-negotiation, bit 0.9=1, whenever Register 4 or Register 9 are written or modified.
2. R/W = Read/Write, RO = Read Only
3. The default value of bits 4.10 and 4.11 are determined by the PAUSE ball.
4. The default value of bit 4.8 is determined by the DUP and SPEED1 balls.
5. The default value of bit 4.7 is determined by the DUP and SPEED1 balls.
6. The default value of bit 4.6 is determined by the DUP and SPEED0 balls.
7. The default value of bit 4.5 is determined by the DUP and SPEED balls

Table 58. Auto-Negotiation Advertisement Register (Address 4)[1]

Bit	Name	Description	Type [2]	Default
4.12	Reserved		R/W	0
4.11	ASM_DIR	Advertise Asymmetric Pause direction bit. This bit is used in conjunction with PAUSE.	R/W	Note 3
4.10	Pause	Advertise to Partner that Pause operation as defined in 802.3x is desired.	R/W	Note 3
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT1000 does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
4.8	100BASE-TX Full Duplex	1 = DTE is 100BASE-TX full-duplex capable. 0 = DTE is not 100BASE-TX full-duplex capable.	R/W	Note 4
4.7	100BASE-TX	1 = DTE is 100BASE-TX capable. 0 = DTE is not 100BASE-TX capable.	R/W	Note 5
4.6	10BASE-T Full Duplex	1 = DTE is 10BASE-T full-duplex capable. 0 = DTE is not 10BASE-T full-duplex capable.	R/W	Note 6
4.5	10BASE-T	1 = DTE is 10BASE-T capable. 0 = DTE is not 10BASE-T capable.	R/W	Note 7
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations should not be transmitted.	R/W	00001

1. Restart auto-negotiation, bit 0.9=1, whenever Register 4 or Register 9 are written or modified.
2. R/W = Read/Write, RO = Read Only
3. The default value of bits 4.10 and 4.11 are determined by the PAUSE ball.
4. The default value of bit 4.8 is determined by the DUP and SPEED1 balls.
5. The default value of bit 4.7 is determined by the DUP and SPEED1 balls.
6. The default value of bit 4.6 is determined by the DUP and SPEED0 balls.
7. The default value of bit 4.5 is determined by the DUP and SPEED balls

Table 59. Auto-Negotiation Link-Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type [1]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages. 0 = Link Partner has no ability to send multiple pages.	RO	N/A
5.14	Acknowledge	1 = Link Partner has received Link Code Word from LXT1000. 0 = Link Partner has not received Link Code Word from LXT1000.	RO	N/A
5.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	RO	N/A
5.12	Reserved		RO	N/A

1. RO = Read Only
2. Per 802.3xy-1997, Register 8 will store the Auto-negotiation Link Partner Received Next Pages. Register 5 will NOT be used to store Next Pages; it will contain the information from the last Base Page correctly received.

Table 59. Auto-Negotiation Link-Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type [1]	Default
5.11	LP ASM_DIR	Advertise Asymmetric Pause direction bit. This bit is used in conjunction with PAUSE. 1 = Link Partner is capable of asymmetric pause. 0 = Link Partner is not capable of asymmetric pause.	RO	N/A
5.10	Pause	Link Partner wants to utilize Pause Operation as defined in 802.3x	RO	N/A
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO	N/A
5.8	100BASE-TX Full Duplex	1 = Link Partner is 100BASE-TX full duplex capable. 0 = Link Partner is not 100BASE-TX full duplex capable.	RO	N/A
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO	N/A
5.6	10BASE-T Full Duplex	1 = Link Partner is 10BASE-T full-duplex capable. 0 = Link Partner is not 10BASE-T full-duplex capable.	RO	N/A
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO	N/A
5.4:0	Selector Field S[4:0]	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations shall not be transmitted.	RO	N/A

1. RO = Read Only
2. Per 802.3xy-1997, Register 8 will store the Auto-negotiation Link Partner Received Next Pages. Register 5 will NOT be used to store Next Pages; it will contain the information from the last Base Page correctly received.

Table 60. Auto-Negotiation Expansion Register (Address 6)

Bit	Name	Description	Type [1]	Default
6.15:6	Reserved	Ignore.	RO	0
6.5	Base Page	This bit indicates the status of the autonegotiation variable, base page. It flags synchronization with the autonegotiation state diagram allowing detection of interrupted links. This bit is only used if bit 21.13 (Alternate NP feature) is set. 1 = base_page = true 0 = base_page = false	RO/ LH	0
6.4	Parallel Detection Fault	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link partner is next page able. 0 = Link partner is not next page able.	RO	0

1. R/W = Read/Write, RO = Read Only, LH = Latch High, clear on read

Table 60. Auto-Negotiation Expansion Register (Address 6)

Bit	Name	Description	Type [1]	Default
6.2	Next Page Able	1 = Local device is next page able 0 = Local device is not next page able	RO	1
6.1	Page Received	Indicates that a new page has been received as and the received code word has been loaded into register 5 (base pages) or register 8 (next pages) as specified in clause 28 of 802.3. This bit clears on read. If bit 21.13 is set, the Page Received bit also clears when mr_page_rx = false or transmit_disable = true.	RO/ LH	0
6.0	Link Partner Auto Neg Able	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.	RO	0
1. R/W = Read/Write, RO = Read Only, LH = Latch High, clear on read				

Table 61. Auto-Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type [1]	Default
7.15	Next Page (NP)	1 = Additional next pages follow 0 = Last page	R/W	0
7.14	Reserved	Write as 0, ignore on read	RO	0
7.13	Message Page (MP)	1 = Message page 0 = Unformatted page	R/W	0
7.12	Acknowledge 2 (ACK2)	1 = Will comply with message 0 = Can not comply with message	R/W	0
7.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	R0	0
7.10:0	Message/ Unformatted Code Field		R/W	0
1. R/W = Read/Write, RO = Read Only				

Table 62. Auto-Negotiation Link Partner Received Next Page Ability Register (Address 8)

Bit	Name	Description	Type [1]	Default
8.15	Next Page (NP)	1 = Link Partner has additional next pages to send 0 = Link Partner has no additional next pages to send	RO	0
8.14	Acknowledge (ACK)	1 = Link Partner has received Link Code Word from the LXT1000 0 = Link Partner has not received Link Code Word from the LXT1000	RO	0
8.13	Message Page (MP)	1 = Page sent by the Link Partner is a Message Page 0 = Page sent by the Link Partner is an Unformatted Page	RO	0
1. RO = Read Only				

Table 62. Auto-Negotiation Link Partner Received Next Page Ability Register (Address 8)

Bit	Name	Description	Type [1]	Default
8.12	Acknowledge 2 (ACK2)	1 = Link Partner complies with the message 0 = Link Partner cannot comply with the message	RO	0
8.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	RO	0
8.10:0	Message/ Unformatted Code Field		RO	0

1. RO = Read Only

Table 63. 1000BASE-T/100BASE-T2 Control Register (Address 9)[1]

Bit	Name	Description	Type[2]	Default
9.15:13	Test Mode		R/W	000
9.12	Master/Slave Config Enable	1 = Enable MASTER-SLAVE Manual configuration value 0 = Disable MASTER-SLAVE Manual configuration value	R/W	0
9.11	Master/Slave Config Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one.	R/W	Note 3
9.10	Port Type	1 = Multi-port Device (MASTER) 0 = Single-port (SLAVE) This bit is only used when 9.12 is set to logical zero.	R/W	Note 3
9.9	1000T Full Duplex	1 = DTE is 1000BASE-T full-duplex capable. 0 = DTE is not 1000BASE-T full-duplex capable. This bit is used by Smart Negotiation.	R/W	Note 4
9.8	1000T Half Duplex	1 = DTE is 1000BASE-T capable 0 = DTE is not 1000BASE-T capable. This bit is used by Smart Negotiation.	R/W	Note 4
9.7	Reserved	-	R/W	-
9.6	Reserved	Reserved-Enable Bypass selection, auto-negotiate bypass mode	R/W	0
9.5	Reserved	Reserved	R/W	0
9.4:0	Reserved	Reserved	R/W	0

1. Restart auto-negotiation, set bit 0.9=1, whenever Register 4 or Register 9 are written or modified.
2. R/W = Read/Write
3. The default value of bits 9.11 and 9.10 are determined by the MASTER ball.
4. The default values of bits 9.9 and 9.8 are determined by the DUP and SPEED2 bits.

Table 64. 1000BASE-T/100BASE-T2 Status Register (Address 10)

Bit	Name	Description	Type [1]
10.15	Master/Slave config fault	1 = MASTER-SLAVE manual configuration fault detected 0 = No MASTER-SLAVE manual configuration fault detected	RO/LH
10.14	Master/Slave resolution	1 = Configuration resolved to MASTER 0 = Configuration resolved to SLAVE	RO Note 2
10.13	Local Receiver Status	1 = Local Receiver OK 0 = Local Receiver not OK	RO
10.12	Remote Receiver Status	1 = Remote Receiver OK 0 = Remote Receiver not OK	RO
10.11	LP 1000T FD	1 = Link Partner is capable of 1000BASE-T full duplex 0 = Link Partner is not capable of 1000BASE-T full duplex	RO Note 2
10.10	LP 1000T HD	1 = Link Partner is capable of 1000BASE-T half duplex 0 = Link Partner is not capable of 1000BASE-T half duplex	RO Note 2
10.9	Reserved		RO
10.8	Reserved	Reserved-Indicates Link Partners bypass mode when bit 9.6 set	RO
10.7:0	Idle Error Count	Idle Error counter Value	RO/SC

1. RO = Read Only; LH = Latch High; SC = Self Clearing
2. Valid after auto-negotiation complete (bit 1.5)

Table 65. Extended Status Register (Address 15)

Bit	Name	Description	Type [1]	Default
15.15	1000BASE-X Full Duplex	1 = PHY able to perform full-duplex 1000BASE-X 0 = PHY not able to perform full-duplex 1000BASE-X	RO	0
15.14	1000BASE-X Half Duplex	1 = PHY able to perform half-duplex 1000BASE-X 0 = PHY able to perform half-duplex 1000BASE-X	RO	0
15.13	1000BASE-T Full Duplex	1 = PHY able to perform full-duplex 1000BASE-T 0 = PHY not able to perform full-duplex 1000BASE-T	RO	1
15.12	1000BASE-T Full Duplex	1 = PHY able to perform half-duplex 1000BASE-T 0 = PHY able to perform half-duplex 1000BASE-T	RO	1
15.11:0	Reserved	Ignore when read	RO	0

1. RO = Read Only

Table 66. Port Configuration Register (Address 16)

Bit	Name	Description	Type [1]	Default
16.15	Reserved	Always set to 0.	R/W	0
16.14	Reserved	Always set to 0.	R/W	0
16.13	Transmit Disable	1 = Disable twisted-pair transmitter 0 = Normal Operation	R/W	0
16.12	Bypass Scrambler (100BASE-TX)	1 = Bypass Scrambler and Descrambler 0 = Normal Operation	R/W	Note 2
16.11	Bypass 4B/5B (100BASE-TX)	1 = Bypass 4B/5B encoder and decoder 0 = Normal Operation	R/W	Note 3
16.10	Jabber (10BASE-T)	1 = Disable Jabber 0 = Normal operation	R/W	0
16.9	SQE (10BASE-T)	1 = Enable Heart Beat 0 = Disable Heart Beat	R/W	0
16.8	TP Loopback (10BASE-T)	1 = Disable TP loopback during half-duplex operation 0 = Normal Operation	R/W	0
16.7	Smart Speed Selection	1 = Smart Speed Selection enabled 0 = Smart Speed Selection disabled	R/W	Note 4
16.6	Reserved	Always set to 0.	R/W	0
16.5	PRE_EN	Preamble Enable. 0 = Set RX_DV High coincident with SFD 1 = Set RX_DV High and RXD = preamble when CRS is asserted	R/W	0
16.4	Reserved	Always set to 0.	R/W	0
16.3	10 Mbps Serial	1 = If in 10BASE-T, the serial output interface is used. 10 Mbps data is driven on RXD<0> in this mode. 0 = Utilize normal GMII mode	R/W	Note 5
16.2	ANIsolate	1 = For read operation, indicates that the port has been isolated due to a speed change. Writing a 1 has no effect. 0 = When written to 0, un-isolates the port, when read as 0 indicates that the port is not isolated. ***Note:*** NOTE: Isolation only applies when AN_EN = 1.	R/W	N/A
16.1	TENbit	10-bit interface mode enable. Only active for 1000 Mbps. 1 = Use TBI configuration for MAC Interface 0 = Use GMII configuration for MAC Interface	R/W	Note 6
16.0	Reserved	Always set to 0.	RO	0

1. R/W = Read/Write, RO = Read Only
2. The default value of bit 16.12 is determined by the BYPSCR/LEDG ball.
3. The default value of bit 16.11 is determined by the BYPENC/LEDS ball.
4. The default value of bit 16.7 is determined by the SMART_SPD ball.
5. The default value of bit 16.3 is determined by the SER10 ball.
6. The default value of bit 16.1 is determined by the TBI ball.

Table 67. Quick Status Register (Address 17)

Bit	Name	Description	Type [1]	Default[2]
17.15:14	Data Rate	17.15 17.14 0 0 LXT1000 operating in 10BASE-T Serial mode 0 1 LXT1000 operating in 10BASE-T MII mode 1 0 LXT1000 operating in 100BASE-T mode 1 1 LXT1000 operating in 1000BASE-T mode	RO	11
17.13	Transmit Status	1 = LXT1000 is transmitting a packet 0 = LXT1000 is not transmitting a packet	RO	0
17.12	Receive Status	1 = LXT1000 is receiving a packet 0 = LXT1000 is not receiving a packet	RO	0
17.11	Collision Status	1 = Collision is occurring 0 = No collision	RO	0
17.10	Link	1 = Link is up 0 = Link is down	RO	0
17.9	Duplex Mode	1 = Full duplex 0 = Half duplex	RO	0
17.8	Auto-Negotiation	1 = LXT1000 is Auto-Negotiate enabled 0 = LXT1000 is in manual mode (only for 10/100)	RO	0
17.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
17.6:4	Line Length Estimation	000 = Line length is 0 Meters 001 = Line Length is 20 Meters 010 = Line Length is 40 Meters 011 = Line Length is 60 Meters 100 = Line Length is 80 Meters 101 = Line Length is 100 Meters 110 = Line Length is 120 Meters 111 = Line length is above 120 Meters Line length estimation is only valid for 100 and 1000 modes.	RO	000
17.3	Pause	Pause ability advertised by link partner	RO	0
17.2	Asymmetric Pause	Asymmetric pause ability advertised by link partner	RO	0
17.1	Reserved	-	RO	0
17.0	Event	1 = Event has occurred (Smart Speed, Error Condition) 0 = No event has occurred	RO	0

1. RO = Read Only
2. The default is overridden by appropriate ball or auto-negotiation result when applicable.

Table 68. Interrupt Enable Register (Address 18)

Bit	Name	Description	Type [1]	Default
18.15:14	Reserved	Write as 0; ignore on read.	R/W	N/A
18:13	AN_FAULT	Mask for auto-negotiation fault. 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.12	Reserved	-	R/W	N/A
18.11	CROSSMSK	Mask for Cross Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.10	POLARITY	Mask for Polarity Event 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.9	SMRTMSK	Mask for Smart Speed 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.8	CNTRMSK	Mask for Counter Full 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.7	ANMSK	Mask for Auto-Negotiate Complete 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.6	SPEEDMSK	Mask for Speed Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.5	DUPLEXMSK	Mask for Duplex Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.4	LINKMSK	Mask for Link Status Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.3	Reserved	-	R/W	0
18.2	Reserved	Write as 0; ignore on read.	R/W	N/A
18.1	INTEN	1 = Enable interrupts 0 = Disable interrupts	R/W	0
18.0	TINT	1 = If interrupts are enabled, force interrupt on MDINT 0 = Normal operation	R/W	0

1. R/W = Read/Write

Table 69. Interrupt Status Register (Address 19)

Bit	Name	Description	Type [1]
19.15:14	Reserved	Ignore	RO
19.13	AN_FAULT	Auto-negotiation Fault Event occurred. 1 = Indicates fault detected 0 = Indicates no an_fault occurred.	RO/SC
19.12	Reserved	-	-
19.11	CROSSCHG	Crossover Event Status Change 1 = Indicates crossover (MDIX) mode is in effect 0 = Indicates that straight (MDI) mode is in effect	RO
19.10	POLARITY	Polarity Correction Status Change 1 = The polarity is reversed 0 = The polarity is normal	RO
19.9	SMRTSPD	Smart Speed Status 1 = The smart speed feature was utilized to downgrade the link 0 = The smart speed feature was not utilized	RO/SC
19.8	Reserved	-	RO
19.7	ANCHG	Auto-Negotiation Status Change 1= Auto Negotiation has completed 0= Auto Negotiation has not completed	RO/SC
19.6	SPEEDCHG	Speed Change Status 1 = Indicates that a Speed Change has occurred since last reading this register 0 = Indicates that a Speed Change has not occurred since last reading this register	RO/SC
19.5	DUPLEXCHG	Duplex Change Status 1 = Indicates that a Duplex Change has occurred since last reading this register 0 = Indicates that a Duplex Change has not occurred since last reading this register	RO/SC
19.4	LINKCHG	Link Change Status 1 = Indicates that a Link Change has occurred since last reading this register 0 = Indicates that a Link Change has not occurred since last reading this register	RO/SC
19.3	Reserved	-	RO
19.2	MDINT	Interrupt. (This bit is NOT masked by 18.1) 1 = Indicates MII interrupt pending 0 = Indicates no MII interrupt pending	RO/SC
19.1	Reserved	Ignore	RO
19.0	Reserved	Ignore	RO

1. RO = Read Only, SC = Self Clearing

Table 70. LED Configuration Register (Address 20)

Bit	Name	Description	Type [1]	Default
20.15:14	LEDC Programming bit	00 = Collision indication 01 = Blink 10 = On 11 = Off	R/W	00
20.13:12	LEDR Programming bit	00 = Receive indication 01 = Blink 10 = On 11 = Off ***Note:*** Not indicated in Loopback Operation.	R/W	00
20.11:10	LEDT Programming bit	00 = Transmit indication 01 = Blink 10 = On 11 = Off ***Note:*** Not indicated in Loopback Operation.	R/W	00
20.9:8	LEDG Programming bit	00 = Gigabit mode indication 01 = Gigabit Transmit or Receive activity 10 = On 11 = Off	R/W	00
20.7:6	LEDS Programming bit	00 = 10/100 mode indication 01 = 10/100 Transmit or Receive activity 10 = On 11 = Off	R/W	00
20.5:4	LEDL Programming bit	00 = Link indication 01 = Blink 10 = On 11 = Off	R/W	00
20.3:2	LEDF Programming bit	00 = Full-Duplex indication 01 = Blink 10 = On 11 = Off	R/W	00
20.1	PULSESTRETCH	0 = Disable pulse stretching of all LEDs 1 = Enable pulse stretching of all LEDs	R/W	1
20.0	LEDFREQ	0 = Stretch LED events to 30 ms 1 = Stretch LED events to 100 ms	R/W	0

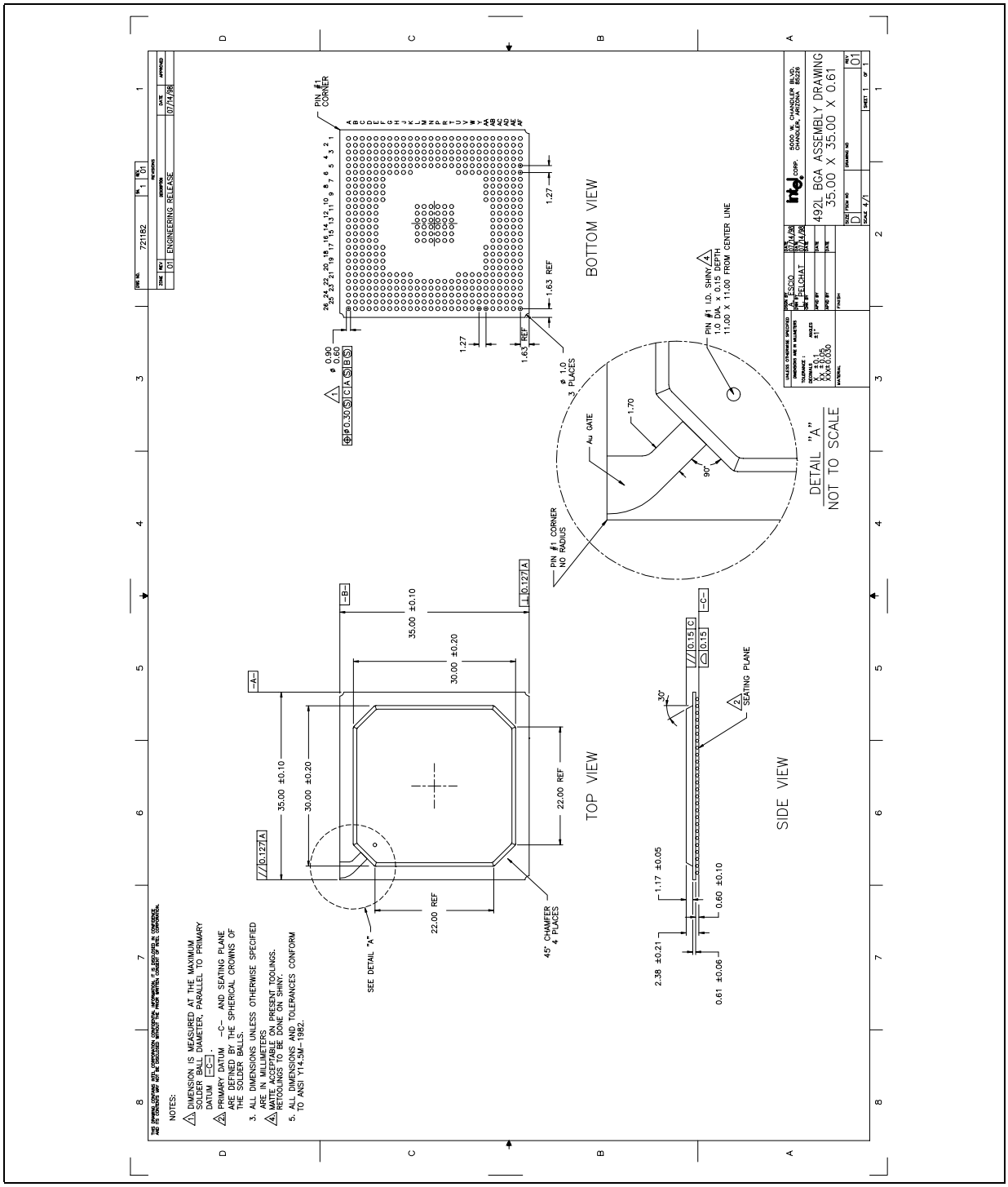
1. R/W = Read/Write

Table 71. Port Control Register (Address 21)

Bit	Name	Description	Type [1]	Default
21.15	TX_TCLK	Enables TX_TCLK outputs for jitter testing. The output signal appears at the PAUSE/TX_TCLKP and DUPLEX/TX__TCLKN balls. ***Note:*** Must be measured with a differential probe.	R/W	0
21.14	Reserved	-	R/W	0
21.13	Alternate NP feature	1 = Enable alternate auto-negotiate next page feature 0 = Disable alternate auto-negotiate next page feature	R/W	0
21.12	Reserved	-	R/W	0
21.11:0	Reserved	-	R/W	0
1. R/W = Read/Write				

6.0 Mechanical Specification

Figure 59. Preliminary PBGA Package Specification



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Appendix A Ordering Information

Table 72. Product Information

Number	Revision	Qualification	Tray MM	Tape & Reel MM
FLLXT1000BA.C4	C4	S	837274	—

Figure 60. Ordering Information - Sample