LXT901/907

Universal 10BASE-T and AUI Transceivers

Datasheet

The LXT901 and LXT907 Universal 10BASE-T and AUI Transceivers are designed for IEEE 802.3 physical layer applications. They provide all the active circuitry to interface most standard IEEE 802.3 controllers to either the 10BASE-T media or Attachment Unit Interface (AUI). In addition to standard 10 Mbps Ethernet, they also support full-duplex operation at 20 Mbps.

The LXT901 and LXT907 are identical except for the function of one pin. The LXT901 offers selectable termination impedance to allow the use of either shielded or unshielded twisted-pair cable. The LXT907 offers a signal quality error (SQE) disable function.

Common LXT901 and LXT907 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing, and reversed polity detection/correction. Integrated filters simplify the design work required for FCC-compliance EMI performance.

Applications

- Access devices (DSL, Cable Modems, and Set-Top Boxes).
- Routers/Bridges/Switches/Hubs
- Telecom Backplane
- USB to Ethernet Converters

Product Features

Functional Features

- Integrated Manchester Encoder/Decoder
- 10BASE-T Transceiver
- AUI Transceiver
- Full-Duplex Capable (20 Mbps)

Diagnostic Features

- Four LED Drivers
- AUI/RJ-45 Loopback
- Remote Signaling of Link-Down and Jabber conditions

Convenience Features

- Automatic/Manual AUI/RJ-45 Selection
- Automatic Polarity Correction
- SQE Disable function (*LXT907 only*)
- Programmable Impedance Driver (*LXT901 only*)
- Power-Down Mode and four loopback modes
- LXT901 available in 64-pin LQFP and 44-pin PLCC
- LXT907 available in 44-pin PLCC

For technical assistance on this product, please call 1-800-628-8686, or send an e-mail to support@mailbox.intel.com.

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Contents

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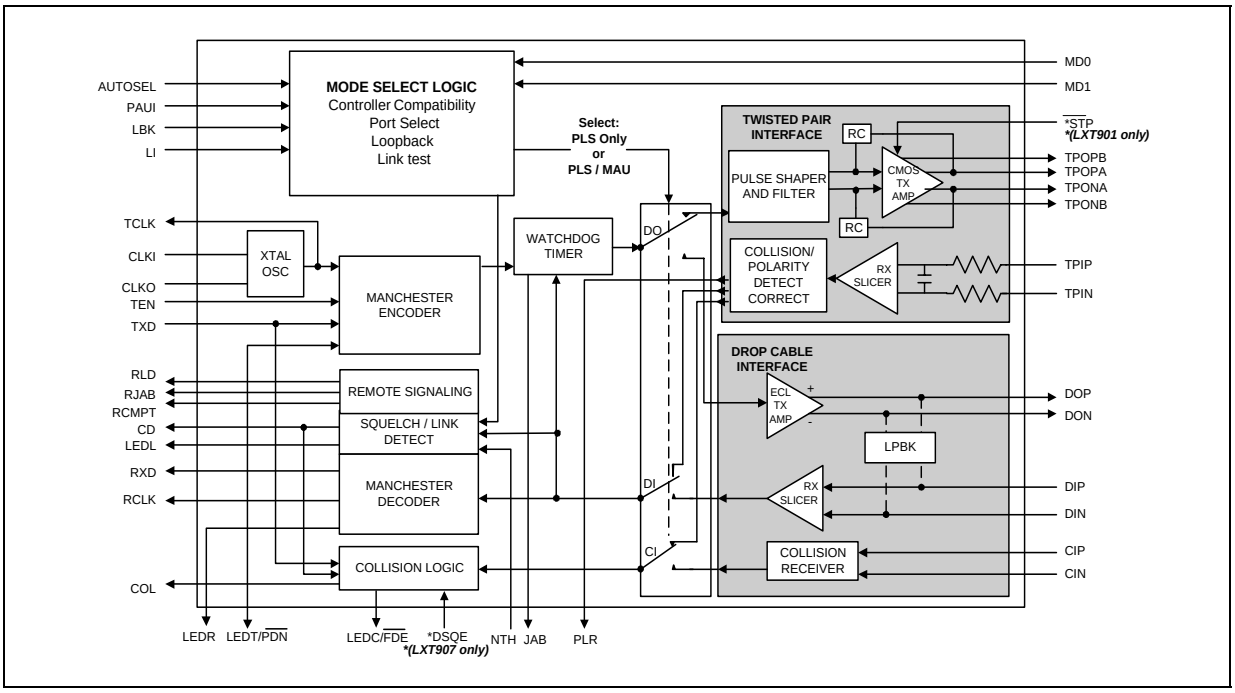
Revision History

Date	Revision	Page #	Description
June 2001	002	20	Table 3: Changed Nom frequency from “25.0” to “20.0.”
		23	Added 0.1 µF label to capacitor at bottom of Figure 9 graphic.
		24	Added 0.1 µF label to capacitor at bottom of Figure 10 graphic.
		25	Added 0.1 µF label to capacitor at bottom of Figure 11 graphic
		26	Added 0.1 µF label to capacitor at bottom of Figure 12 graphic
		27	Added 0.1 µF label to capacitor at bottom of Figure 13 graphic
		31	Added 2nd para under “Test Specifications”: Quality & Reliability issues.
		31	Removed “Ambient operating temperature” from Absolute Maximum Ratings table.
		45	Added Appendix: Product Ordering Information

Figure 1. LXT901/907 Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT901/907 Pin Assignments

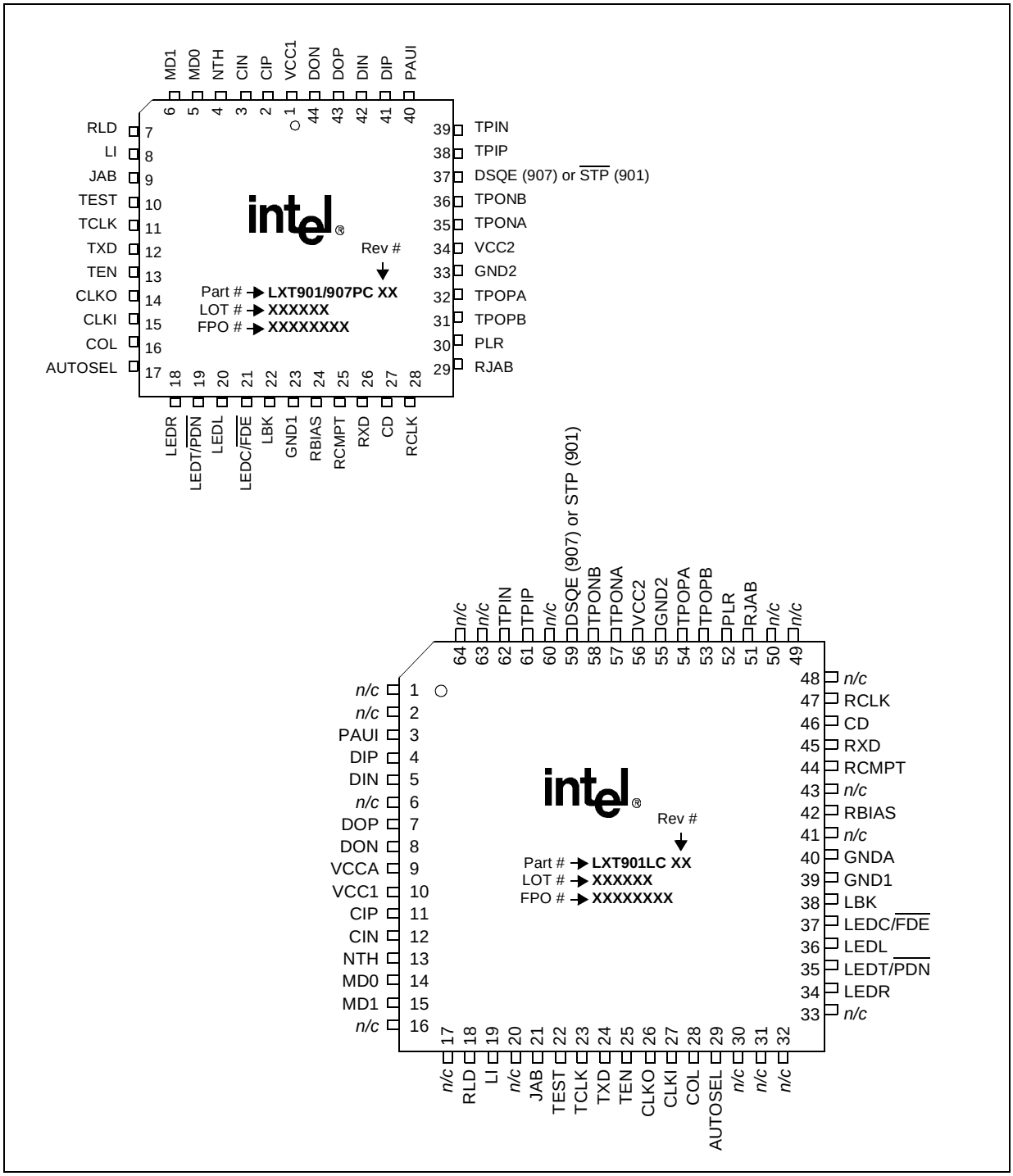


Table 1. LXT901/907 Signal Descriptions

PLCC	LQFP	Symbol	I/O	Description
1 34 -	10 56 9	VCC1 VCC2 VCCA	I I I	**Power Inputs.** Power supply inputs of +5 volts. (LQFP Only)
2 3	11 12	CIP CIN	I I	**AUI Collision Pair.** Differential input to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	13	NTH	I	**Normal Threshold.** Selects normal or reduced threshold. When NTH is High, the normal twisted-pair squelch threshold is in effect. When NTH is Low, the normal twisted-pair squelch threshold is reduced by 4.5 dB.
5 6	14 15	MD0 MD1	I I	**Mode Select 0 (MD0), Mode Select 1 (MD1).** Mode select pins determine the controller compatibility mode in accordance with Table 2.
7	18	RLD	O	**Remote Link Down.** Output goes high to signal to the controller that the remote port is in link down condition.
8	19	LI	1	**Link Test Enable.** Controls Link Integrity Test; enabled when LI = High, disabled when LI = Low
9	21	JAB	O	**Jabber Indicator.** Output goes High to indicate Jabber state.
10	22	TEST	I	**Test.** For Intel internal use only. It is recommended to tie this pin High externally.
11	23	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
12	24	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. Connect TXD directly to the transmit data output of the controller.
13	25	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Test Specifications for details).
14 15	26 27	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	28	COL	O	**Collision Detect.** Output which drives the collision detect input of the controller.
17	29	AUTOSEL	I	**Automatic Port Select.** When High, automatic port selection is enabled (the 901/907 defaults to the AUI port only if twisted-pair link integrity = Fail). When Low, manual port selection is enabled (the PAUI pin determines the active port).
18	34	LEDR	OD	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive.
19	35	LEDT/ $\overline{\text{PDN}}$	OD I	**Transmit LED (LEDT)/Power-Down ($\overline{\text{PDN}}$).** Open drain driver for the transmit indicator. Output is pulled Low during transmit. **Do not allow this pin to float. If unused, tie High.** If externally pulled Low, the LXT901/907 goes to power-down state.
20	36	LEDL	OD I	**Link LED.** Open drain driver for link integrity indicator. Output is pulled Low during link test pass. If externally tied Low, internal circuitry is forced to “Link Pass” state and the 901/907 will transmit link test pulses continuously.
1. I/O Column Coding: I = Input, O = Output, OD = Open Drain				

Table 1. LXT901/907 Signal Descriptions (Continued)

PLCC	LQFP	Symbol	I/O	Description
21	37	LEDC/ $\overline{\text{FDE}}$	OD I	**Collision LED (LEDC)/Full Duplex Enable ($\overline{\text{FDE}}$).** Open drain driver for the collision indicator pulls Low during collision. LED "On"(i.e., Low output) time is extended by approximately 100 ms. If externally tied Low, the LXT901/907 enables full duplex operation by disabling the internal twisted-pair loopback and collision detection circuits in anticipation of external twisted-pair loopback or full duplex operation. If this pin is not used, tie high or directly to VCC.
22	38	LBK	I	**Loopback.** Enables internal loopback mode. Refer to Functional Descriptions for details.
23 33 –	39 55 40	GND1 GND2 GNDA	– – –	**Ground Returns.** Grounds (LQFP Only)
24	42	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
25	44	RCMPT	O	**Remote Compatibility.** Output goes High to signal the controller that the remote port is compatible with the LXT901/LXT907 remote signaling features.
26	45	RXD	O	**Receive Data.** Connect RXD directly to the receive data input of the controller.
27	46	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network.
28	47	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data. Connect to the controller receive clock input.
29	51	RJAB	O	**Remote Jabber.** Output goes High to indicate the remote port is in Jabber condition.
30	52	PLR	O	**Polarity Reverse.** Output goes High to indicate reversed polarity at the twisted-pair input.
31 36 32 35	53 58 54 57	TPOPB TPONB TPOPA TPONA	O O O O	**Twisted-Pair Transmit Pairs A & B.** Two differential driver pair outputs (A and B) to the twisted-pair cable. The outputs are pre-equalized. Each pair must be shorted together and tied to the transformer with a 24.9Ω 1% series resistor to match impedance of 100Ω. Refer to Figure 16 in the Applications Section for information on 150Ω configurations.
37	59	$\overline{\text{STP}}$ **(LXT901)**	I	**$\overline{\text{STP}}$ Select (LXT901 only).** When $\overline{\text{STP}}$ is Low, 150Ω termination for shielded twisted-pair is selected. When $\overline{\text{STP}}$ is High, 100Ω termination for unshielded twisted-pair is selected. LXT907 is designed for 100Ω UTP termination (not selectable).
		DSQE **(LXT907)**	I	**Disable SQE (LXT907 only).** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE must be disabled for normal operation in Hub/Switch applications. LXT901operates with SQE enabled (not selectable).
38 39	61 62	TPIP TPIN	I I	**Twisted-Pair Receive Pair.** A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. No external filters are required.
40	3	PAUI	I	**Port/AUI Select.** In Manual Port Select mode (AUTOSEL Low), PAUI selects the active port. When PAUI is High, the AUI port is selected. When PAUI is Low, the twisted-pair port is selected. In Auto Port Select mode, PAUI must be tied to ground.
1. I/O Column Coding: I = Input, O = Output, OD = Open Drain				

Table 1. LXT901/907 Signal Descriptions (Continued)

PLCC	LQFP	Symbol	I/O	Description
41 42	4 5	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	7 8	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.
–	1, 2, 6, 16, 17, 20, 30, 31, 32, 33, 41, 43, 48, 49, 50, 60, 63, 64	N/C	–	No Connect (Internally tied to ground).
1. I/O Column Coding: I = Input, O = Output, OD = Open Drain				

2.0 Functional Description

The LXT901/907 Universal 10BASE-T and AUI Transceivers perform the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. They function as PLS-only devices (for use with 10BASE-2 or 10BASE-5 coaxial cable networks), or as Integrated PLS/MAU devices (for use with 10BASE-T twisted-pair networks). In addition to standard 10 Mbps operation, they also support full-duplex 20 Mbps operation. Unless otherwise noted, all the information in this data sheet applies to both the LXT901 and LXT907.

The LXT901/907 interfaces a back-end controller to either an AUI drop cable or a twisted-pair cable. The controller interface includes transmit and receive clocks and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI), and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT901/907 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back-end controller side of the interface. The Transmit function refers to data transmitted by the back-end to the AUI cable (PLS-only mode), or to the twisted-pair network (Integrated PLS/MAU mode). The Receive function refers to data received by the back-end from the AUI cable (PLS-only), or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT901/907 performs all required MAU functions defined by the IEEE 802.3 10BASE–T specification, such as collision detection, link integrity testing, signal quality error messaging, jabber control, and loopback. In the PLS-only mode, the LXT901/907 receives incoming signals from the AUI DI circuit with ± 18 ns of jitter and drives the AUI DO circuit.

2.1 Controller Compatibility Modes

The LXT901/907 ia compatible with most industry standard controllers, including devices produced by Motorola, AMD, Intel, Fujitsu, National Semiconductor, Seeq, and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine controller compatibility modes as listed in Table 2. Refer to Test Specifications for a complete set of timing diagrams for each mode.

Table 2. Controller Compatibility Modes

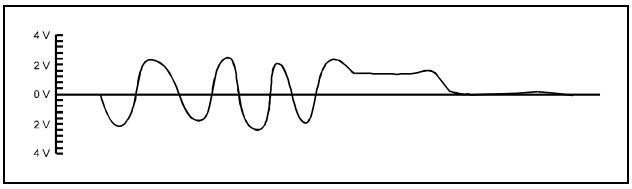
Controller Mode	Setting	
	MD1	MD0
Mode 1 For Motorola 68EN360, MPC860, Advanced Micro Devices AM7990, or compatible controllers	Low	Low
Mode 2 For Intel 82596 or compatible controllers[1]	Low	High
Mode 3 For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[2]	High	Low
Mode 4 For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	High	High

1. Refer to Intel Application Note 51 when designing with Intel controllers.
2. SEEQ controllers require inverters on CLKI, LBK, RCLK and COL.

2.2 Transmit Function

The LXT901/907 receives NRZ data from the controller at the TXD input, as shown in Figure 1, “LXT901/907 Block Diagram” on page 7, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (DO circuit) or the twisted-pair network (TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, as shown in Figure 3. The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT901/907 transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated, PLS/ MAU mode is selected). External resistors control the termination impedance for the LXT907. External resistors and the $\overline{\text{STP}}$ pin control termination impedance on the LXT901.

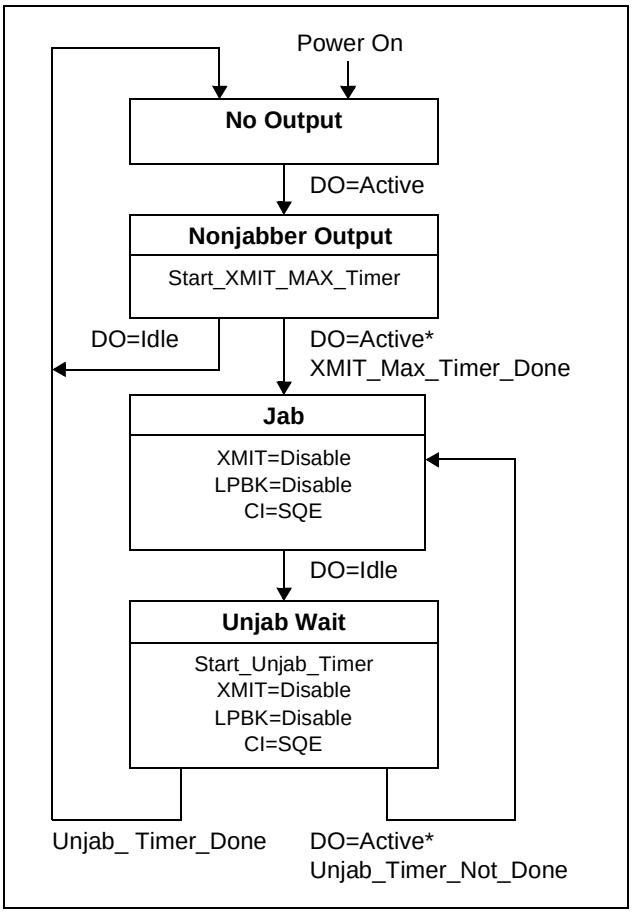
Figure 3. LXT901/907 TPO Output Waveform



2.2.1 Jabber Control Function

Figure 4 is a state diagram of the LXT901/907 Jabber control function. The on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT901/907 is in the jabber state, the TXD circuit must remain idle for a period of 250 to 750 ms before it will exit the jabber state.

Figure 4. Jabber Control Function



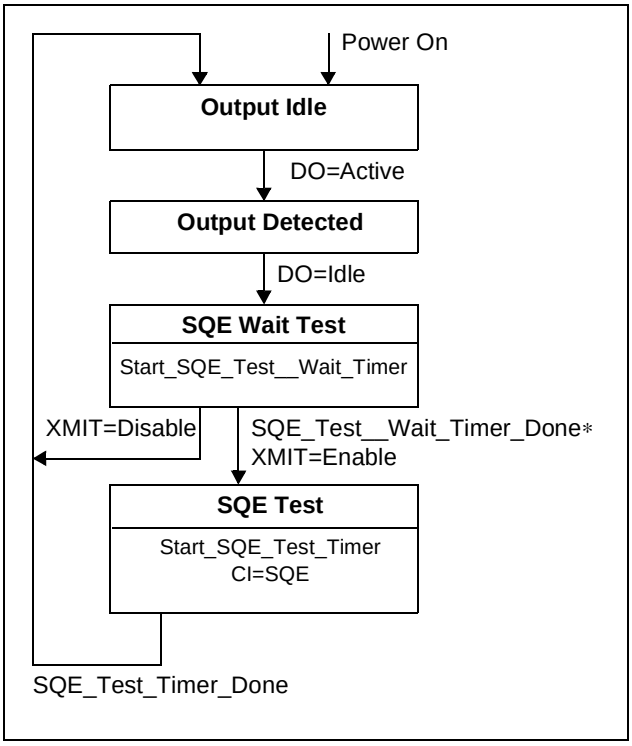
2.2.2 SQE Function

In the integrated PLS/MAU mode, the LXT901/907 supports the signal quality error (SQE) function, as shown in Figure 5 on page 14. After every successful transmission on the 10BASE-T network when SQE is enabled, the LXT901/907 transmits the SQE signal for 10BT ± 5BT over the internal CI circuit which is indicated on the COL pin of the device. When using the 10BASE-2 port of the LXT901/907, the SQE function is determined by the external MAU attached.

2.2.2.1 SQE Disable Function (LXT907 only)

SQE must be disabled for normal operation in hub and switch applications. The LXT907 offers an SQE disable function. The SQE function is disabled when DSQE is set High, and enabled when DSQE is Low.

Figure 5. SQE Function



2.3 Receive Function

The LXT901/907 receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder, then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75 percent of the threshold level (unsquelched) for 8 bit times (typical), the LXT901/907 receive function enters the Idle state. If the polarity of the TPI circuit is reversed, LXT901/907 detects the polarity reverse and reports it via the PLR output. The LXT901/907 automatically corrects reversed polarity.

2.3.1 Polarity Reverse Function

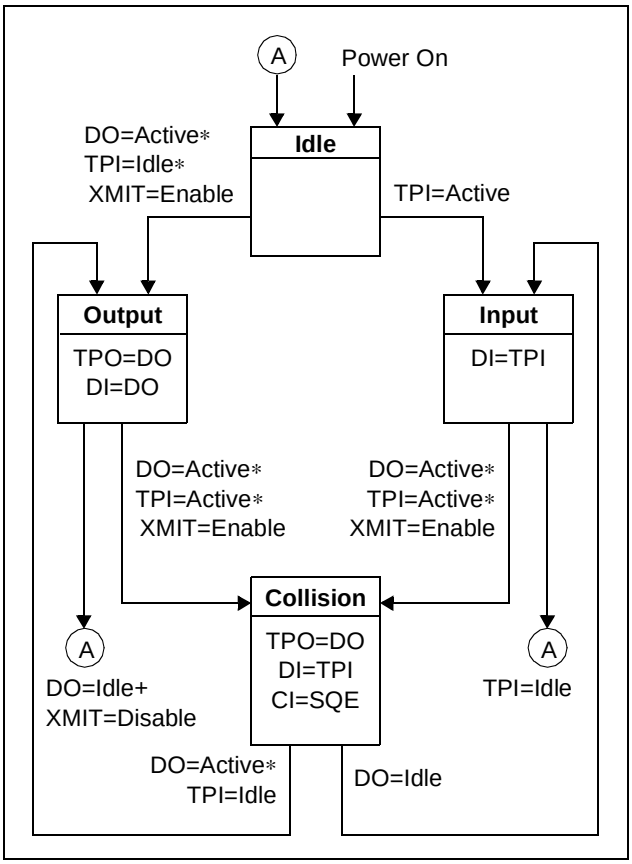
The LXT901/907 polarity reverse function uses both link pulses and End-of-Frame data to determine the polarity of the received signal. If Link Integrity Testing is disabled, polarity detection is based only on received data. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT901/907 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. Polarity correction is always enabled.

2.3.2 Collision Detection Function

The collision detection function operates on the twisted pair side of the interface. For standard (half-duplex) 10BASE-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT901/907 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 6 is a state diagram of the LXT901/907 collision detection function. Refer to Test Specifications for collision detection and COL/CI output timing.

Note: For full-duplex operation on twisted-pair and AUI ports, the collision detection circuitry must be disabled.)

Figure 6. Collision Detection Function



2.4 Loopback Functions

2.4.1 Standard Twisted-Pair Loopback

The LXT901/907 provides the standard loopback function defined by the 10BASE-T specification for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT901/907 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This standard loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Standard loopback is also disabled during link fail and jabber states. The LXT901/907 also provides three additional loopback functions.

2.4.2 External Loopback

An external loopback mode, useful for system-level testing, is controlled by the LEDC pin. When LEDC is tied Low, the LXT901/907 disables the collision detection and internal loopback circuits to allow external loopback. External loopback mode can be set on either twisted-pair or AUI ports.

2.4.3 Forced Twisted-Pair Loopback

"Forced" twisted-pair loopback is controlled by the LBK pin. When the twisted-pair port is selected and LBK is High, twisted-pair loopback is "forced", overriding collisions on the twisted-pair circuit. When LBK is Low, normal loopback is in effect.

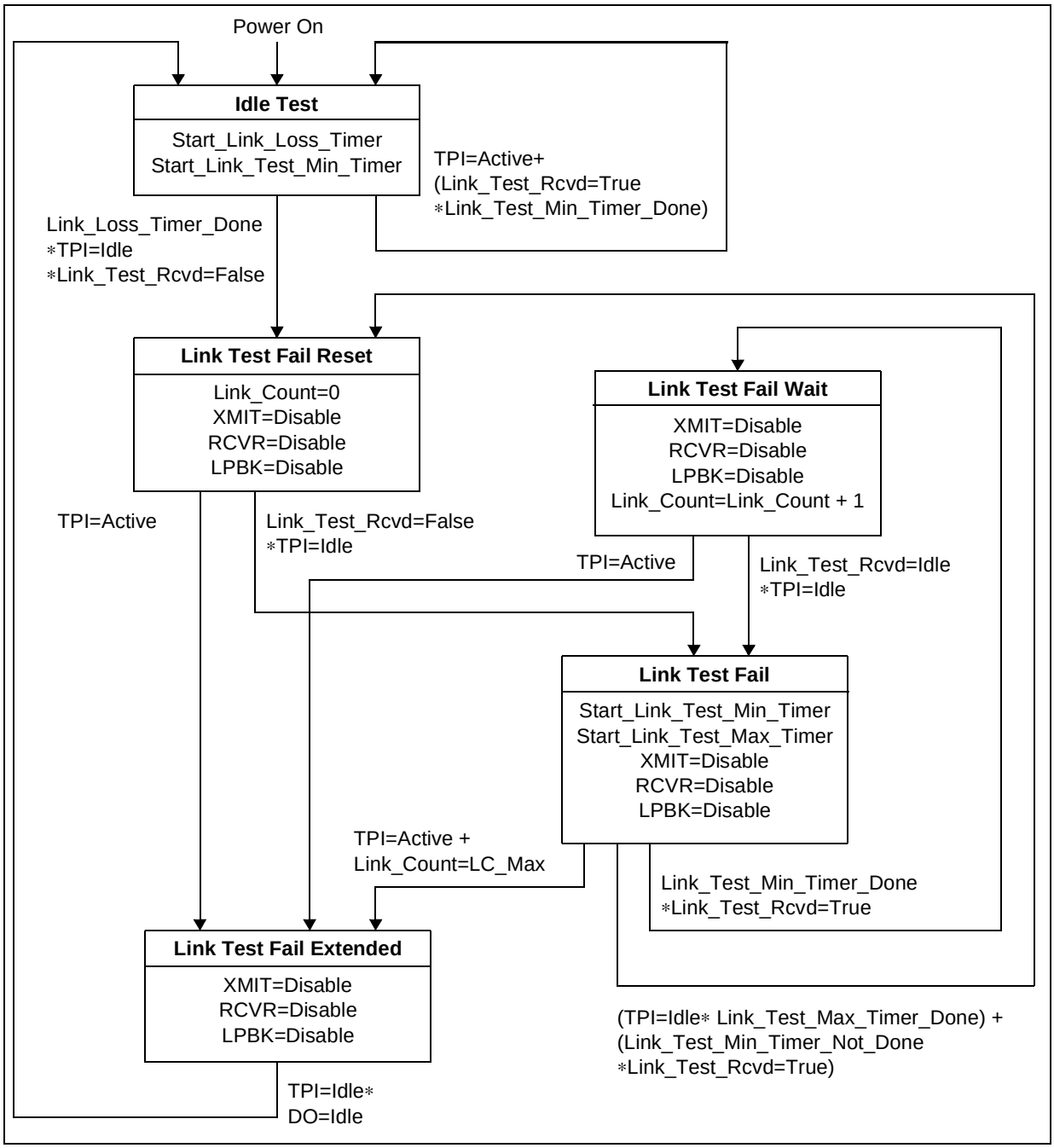
2.4.4 AUI Loopback

AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

2.5 Link Integrity Test Function

Figure 7 on page 18 is a state diagram of the LXT901/907 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when the LI pin is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT901/907 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT901/907 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

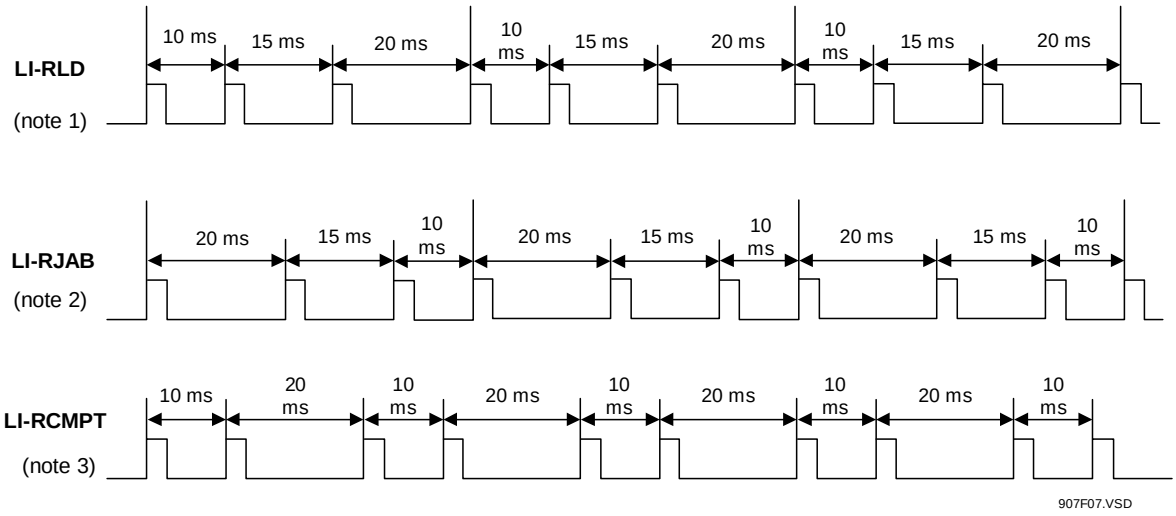
Figure 7. Link Integrity Test Function



2.5.1 Remote Signaling

The LXT901/907 transmits standard link pulses which meet the IEEE 802.3 10BASE-T specification. However, the LXT901/907 encodes additional status information into the link pulse by varying the link pulse timing. This is referred to as remote signaling. Using alternate pulse intervals, the LXT901/907 can signal three local conditions: link down, jabber, and remote signaling compatibility. Figure 8 shows the interval variations used to signal local status to the other end of the line. The LXT901/907 also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are reported to the controller over the RLD, RJAB and RCMPT output pins.

Figure 8. Remote Signaling Link Integrity Pulse Timing



NOTES:
1. For Remote Link-Down (RLD) signaling, the interval between LI pulses increments from 10 ms to 15 ms, and then the cycle starts over.
2. For Remote Jabber (RJAB) signaling, the interval between LI pulses decrements from 20 ms to 15 ms to 10 ms, and then the cycle starts over.
3. For Remote Compatibility (RCMPT) signaling, the interval between LI pulses continually switches between 10 ms and 20 ms.

3.0 Application Information

3.1 Twisted-Pair Impedance Matching

Resistors must be installed on each input and output pair to match impedance of the network media being used. The LXT907 is configured with 100Ω termination for Unshielded Twisted-Pair (UTP). In this case, the positive and negative sides of both output pairs are shorted together (TPOPA/TPOPB and TPONA/TPONB) and tied to the transformer through a 24.9Ω 1% series resistor.

The LXT901 is designed with an $\overline{\text{STP}}$ Select pin that allows the device to match both 100Ω and 150Ω media. A dual resistor combination can be configured to accommodate either line termination, as shown in Figure 16 on page 30. When 100Ω termination is selected, both A and B pairs are driven in parallel. When 150Ω termination is selected, the B pair is tri-stated and only the A pair is driven.

3.2 Crystal Information

Designers should test and validate crystals to system requirements before committing to a specific component. Crystal specifications for the LXT901/907 are shown in Table 3. Based on limited evaluation, Table 4 lists some suitable crystals.

Table 3. Crystal Specifications

Parameter	Min	Nom	Max	Units
Frequency	–	20.0	–	MHz
Frequency[1] Stability	–	–	+/-80	ppm
1. Test condition = -40 - 85°C				

Table 4. Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

3.3 Magnetics Information

The LXT901 and LXT907 require a 1:1 ratio for the receive transformer and a 1:$\sqrt{2}$ ratio for the transmit transformer on the twisted-pair interface. The AUI Interface requires a 1:1 ratio for both the transmit and receive transformers. Designers should test and validate magnetics for system requirements before committing to a specific component. Table 5 lists some suitable magnetics.

Table 5. Suitable Magnetics

	Manufacturer	Part Number
Twisted-Pair	Fil-Mag	23Z128
		23Z128SM
	Valor	PT4069
		ST7011
	Belfuse	A553-0716
		S553-0716
	HALO	TD42-2006Q
		TG42-1406N1
AUI	Fil-Mag	23Z90
		23Z90SM
	Valor	LT6032
		ST7032
	HALO	TD01-0756K
		TG01-0756N

3.4 Typical Applications

Figure 9 on page 23 through Figure 16 on page 30 show typical LXT901/907 applications.

3.4.1 Auto Port Select with External Loopback Control

Figure 9 on page 23 is a typical LXT901/907 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT901/907 pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

Programmable option pins are grouped center left. The PAUI pin is tied Low and all other option pins are tied High. This set-up selects the following options:

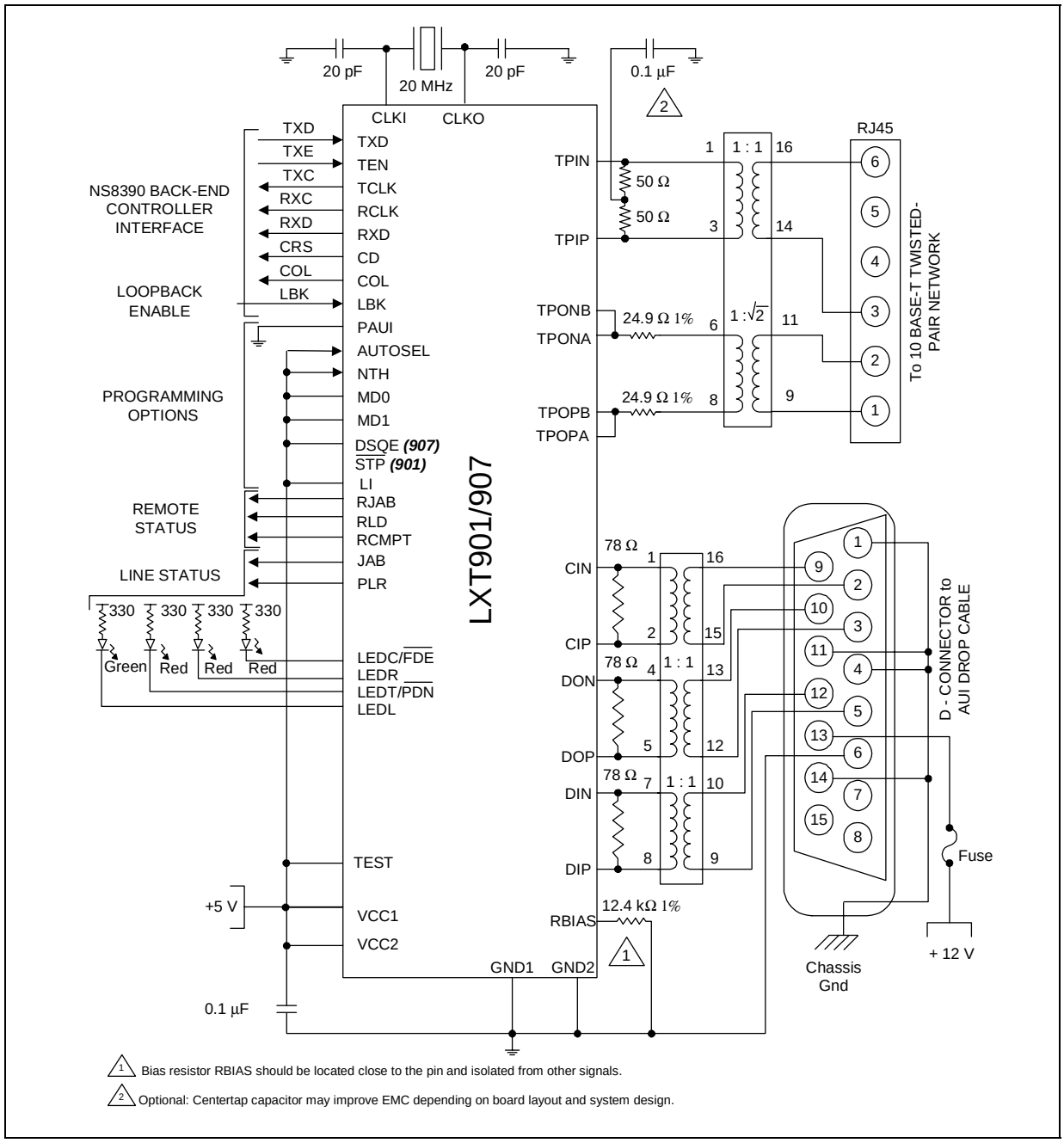
- Automatic Port Selection
  (PAUI Low and AUTOSEL High)
- Normal Receive Threshold (NTH High)
- Mode 4, compatible with National NS8390 controllers (MD0 High, MD1 High)
- SQE Disabled (DSQE High on LXT907 only)
- 100Ω termination UTP cable ($\overline{\text{STP}}$ High on LXT901 only)
- Link Testing Enabled (LI High)

Status outputs are grouped at lower left. Local status outputs drive LED indicators and remote status indicators are available as required.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground busses.

The twisted-pair and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors for 100Ω UTP are installed in each I/O pair but no external filters are required.

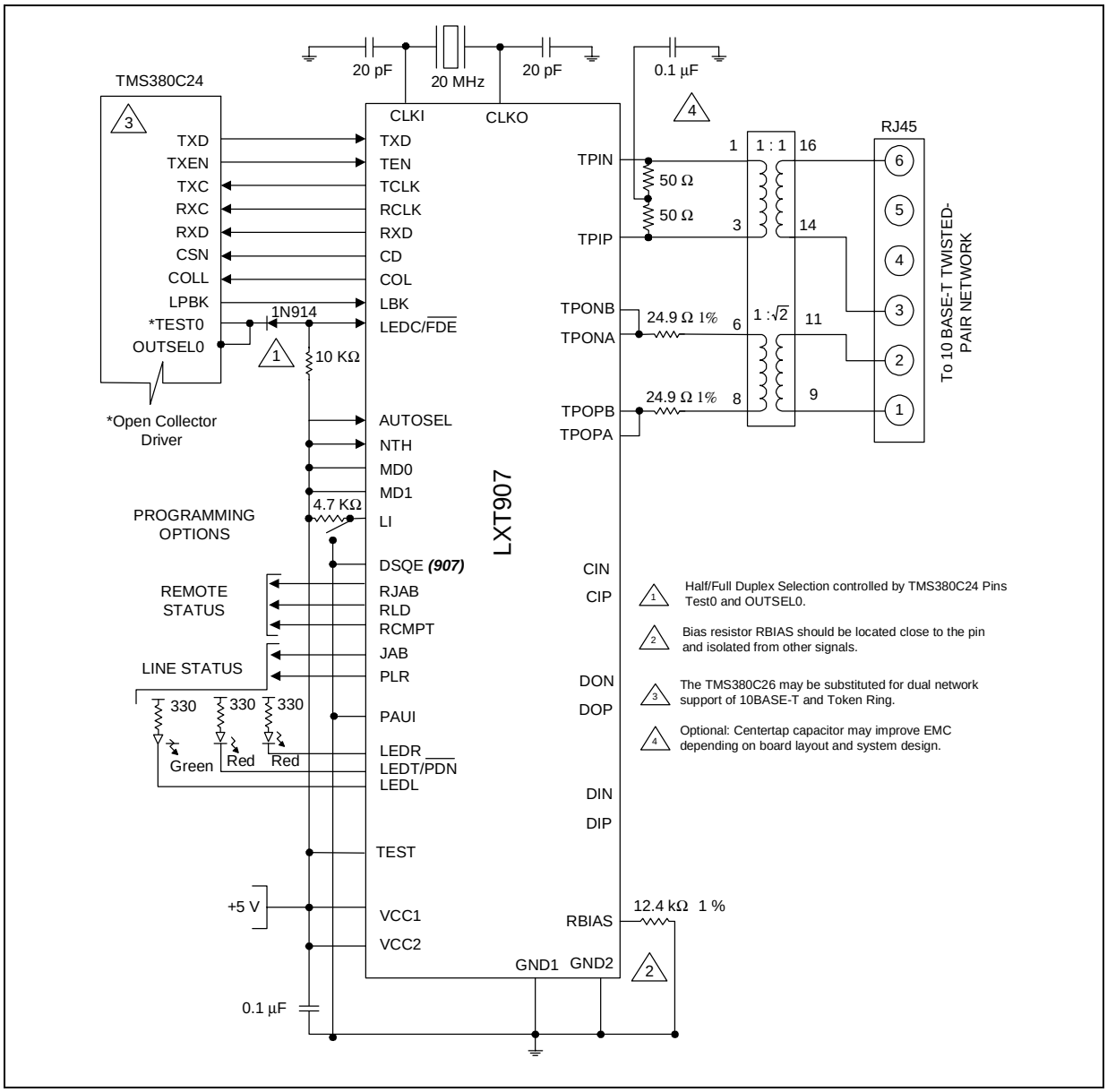
Figure 9. LAN Adapter Board - Auto Port Select with External LPBK Control



3.4.2 Full-Duplex Support

Figure 10 shows the LXT907 with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C24 or other full-duplex-capable controllers, the LXT907 supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application, the SQE function is enabled (DSQE is tied Low) and the AUI port is not used.

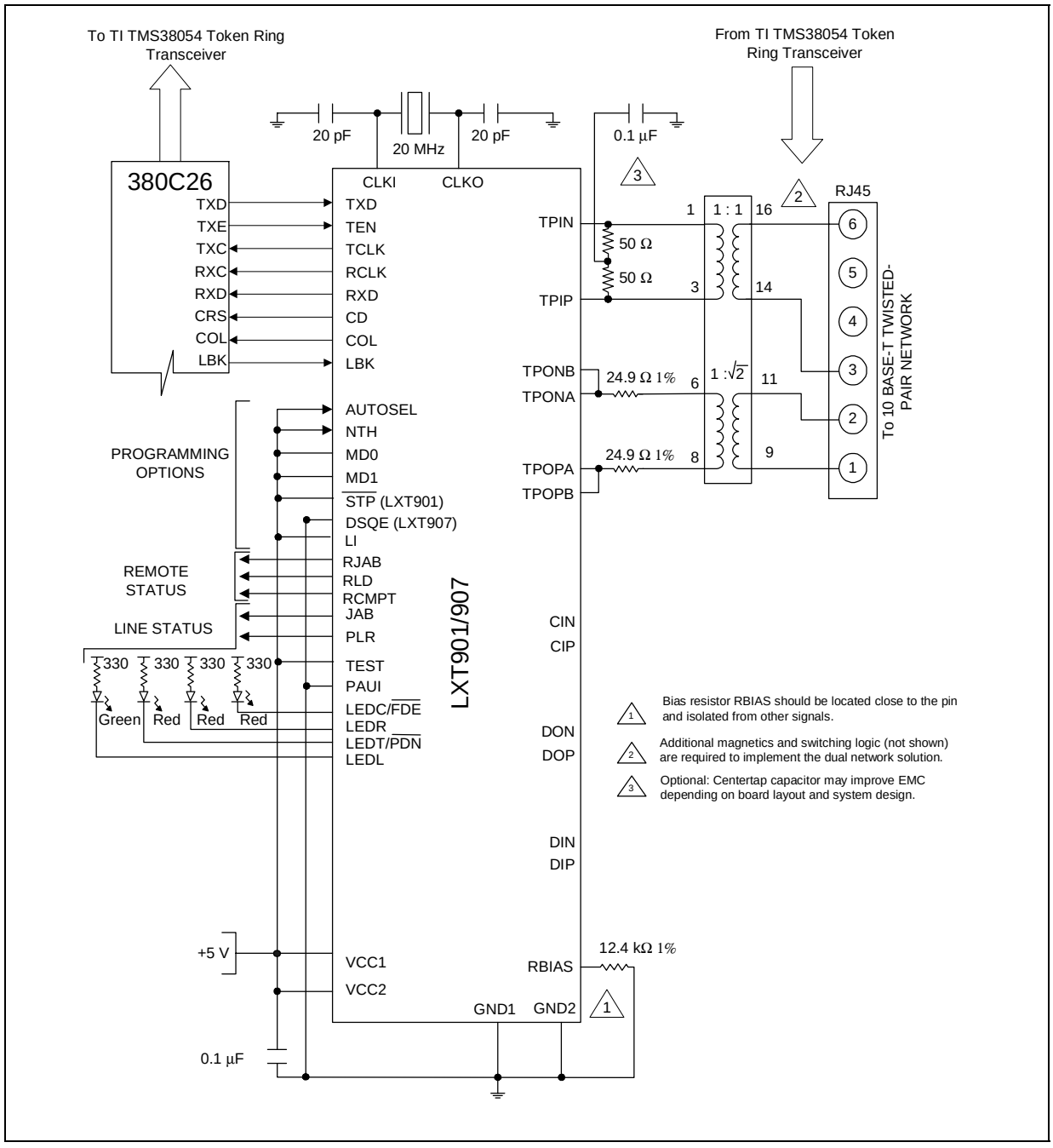
Figure 10. Full-Duplex Operation



3.4.3 Dual Network Support - 10Base-T and Token Ring

Figure 11 shows the LXT901/907 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C26, both the LXT901/907 and a TMS38054 Token Ring transceiver can be tied to a single RJ-45 allowing dual network support from a single connector. The LXT901/907 AUI port is not used. The LXT901 $\overline{STP}$ is High and the LXT907 DSQE is Low.

Figure 11. 380C26 Interface for Dual Network Support of 10BASE-T and Token Ring



3.4.4 Manual Port Select with Link Test Function

With MD0 tied Low and MD1 tied High, the LXT901/907 logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and Seeq 8005 controllers). Figure 12 shows the setup for Fujitsu controllers. Figure 13 on page 27 shows the four inverters required to interface with the Seeq 8005 controller. As in Figure 9 on page 23, both these Mode 3 applications show the LI pin tied High, enabling Link Testing; and the $\overline{STP}$ (LXT901 only) and NTH pins are both tied High, selecting the standard receiver threshold and 100Ω termination for unshielded twisted-pair cable. However, in these applications, AUTOSEL is tied Low, allowing external port selection through the PAUI pin. The remote status outputs are inverted to drive LED indicators.

Figure 12. LAN Adapter Board - Manual Port Select with Link Test Function

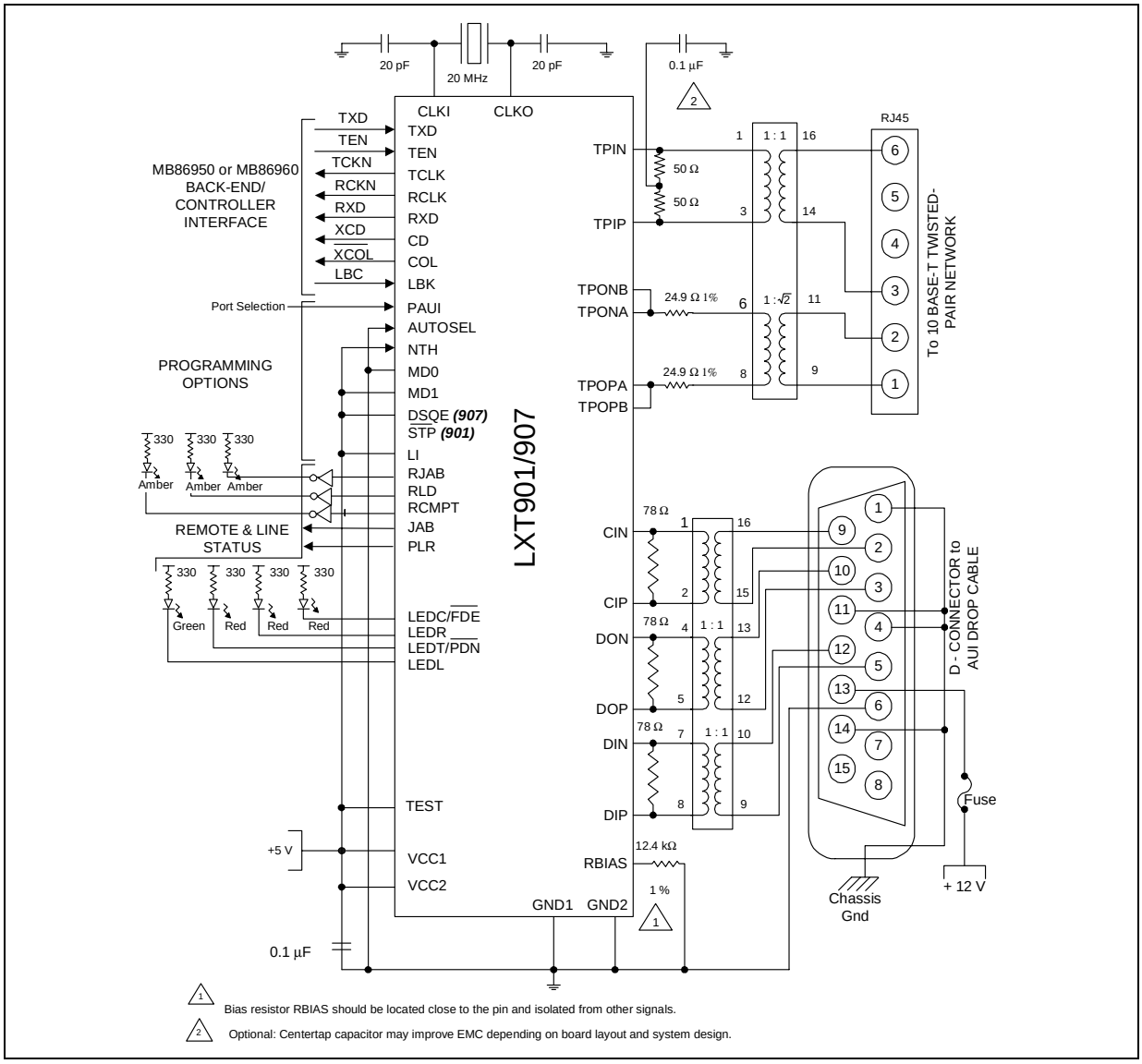
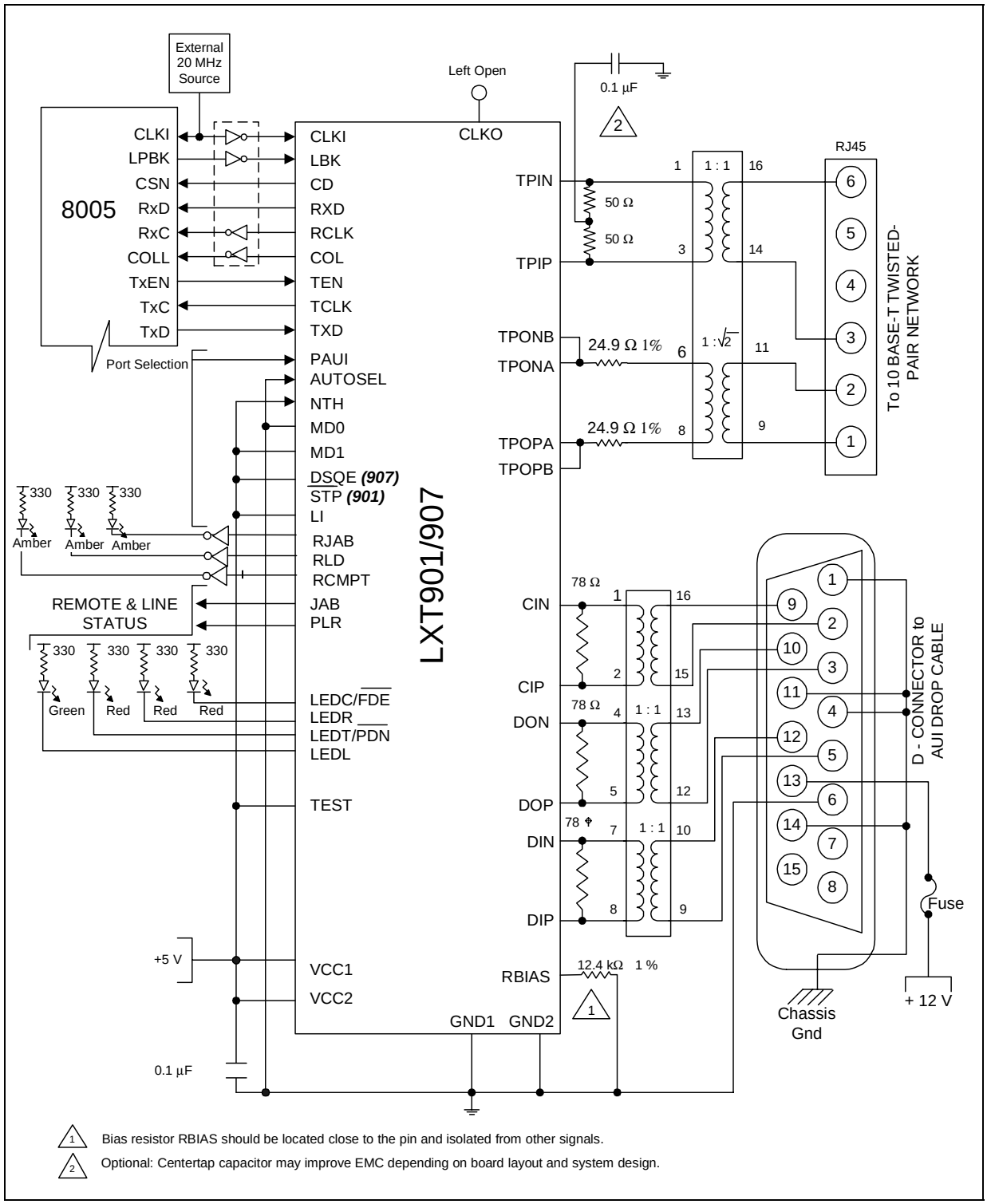


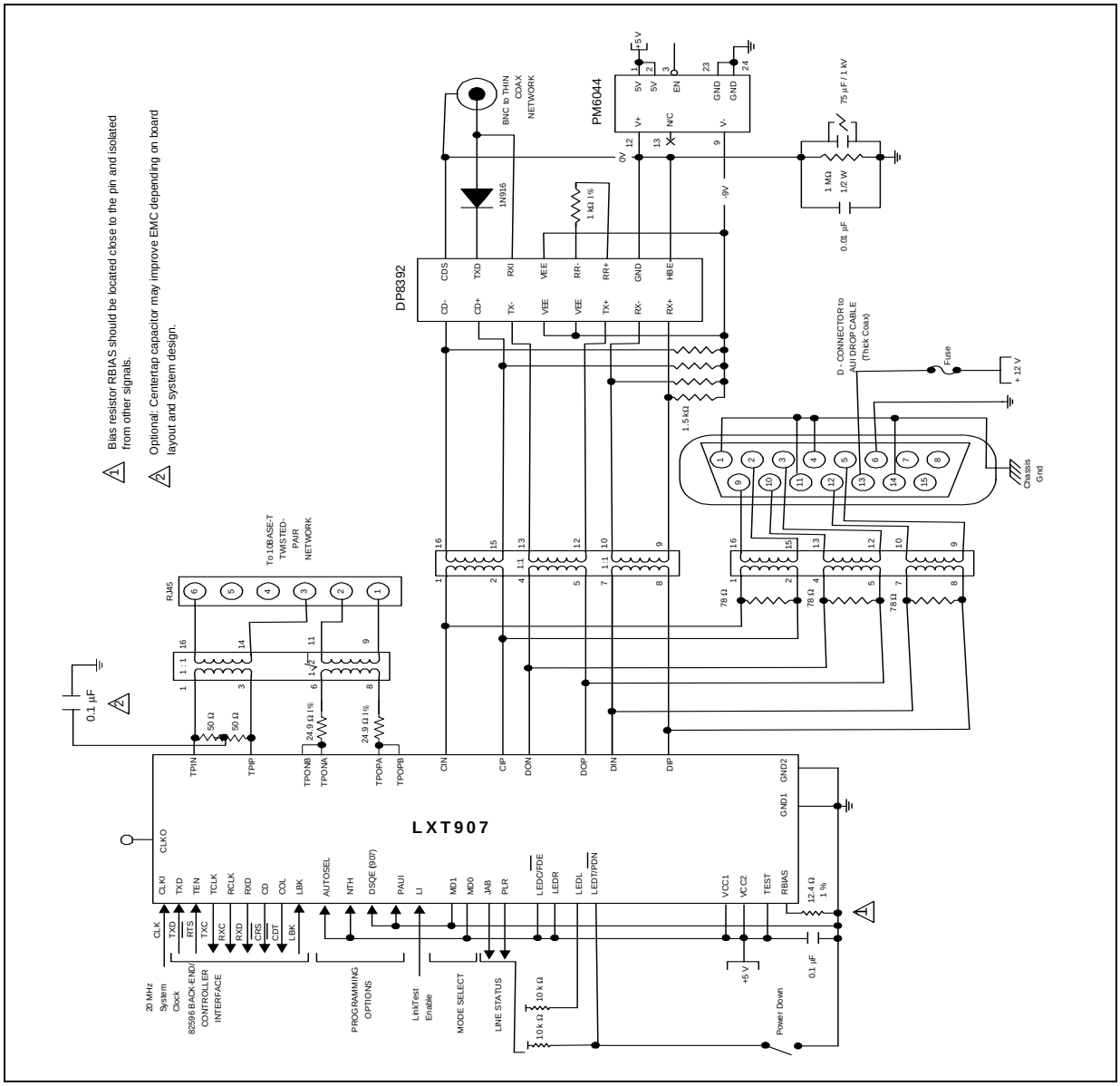
Figure 13. Manual Port Select with Seeq 8005 Controller



3.4.5 Three Media Application

Figure 14 shows the LXT907 in Mode 2 (compatible with Intel 82596 controllers) with additional media options for the AUI port. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. (A DP8392 coax transceiver with PM6044 power supply is required to drive the thin coax network through the BNC.)

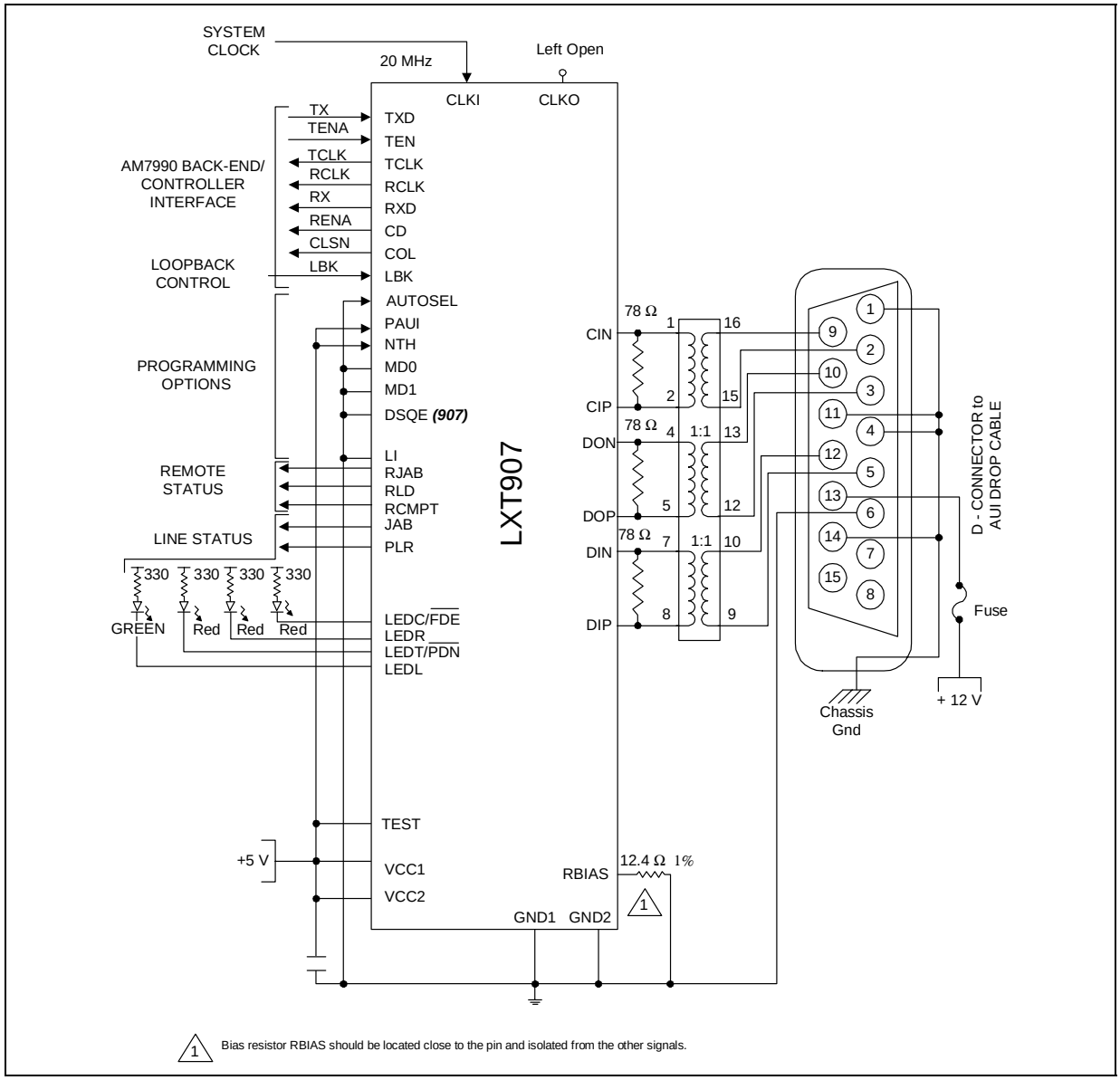
Figure 14. Three Media Application



3.4.6 AUI Encoder/Decoder ONLY

In Figure 15, the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied Low and PAUI is tied High, manually selecting the AUI port. The twisted-pair port is not used. With MD1 and MD0 both tied Low, the logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LI pin is tied Low, disabling the link test function. The DSQE pin is also tied Low, enabling the SQE function on the LXT907. The LBK input controls loop back. A 20 MHz system clock is supplied at CLK1, with CLK0 left open.

Figure 15. AUI Encoder/Decoder Only Application

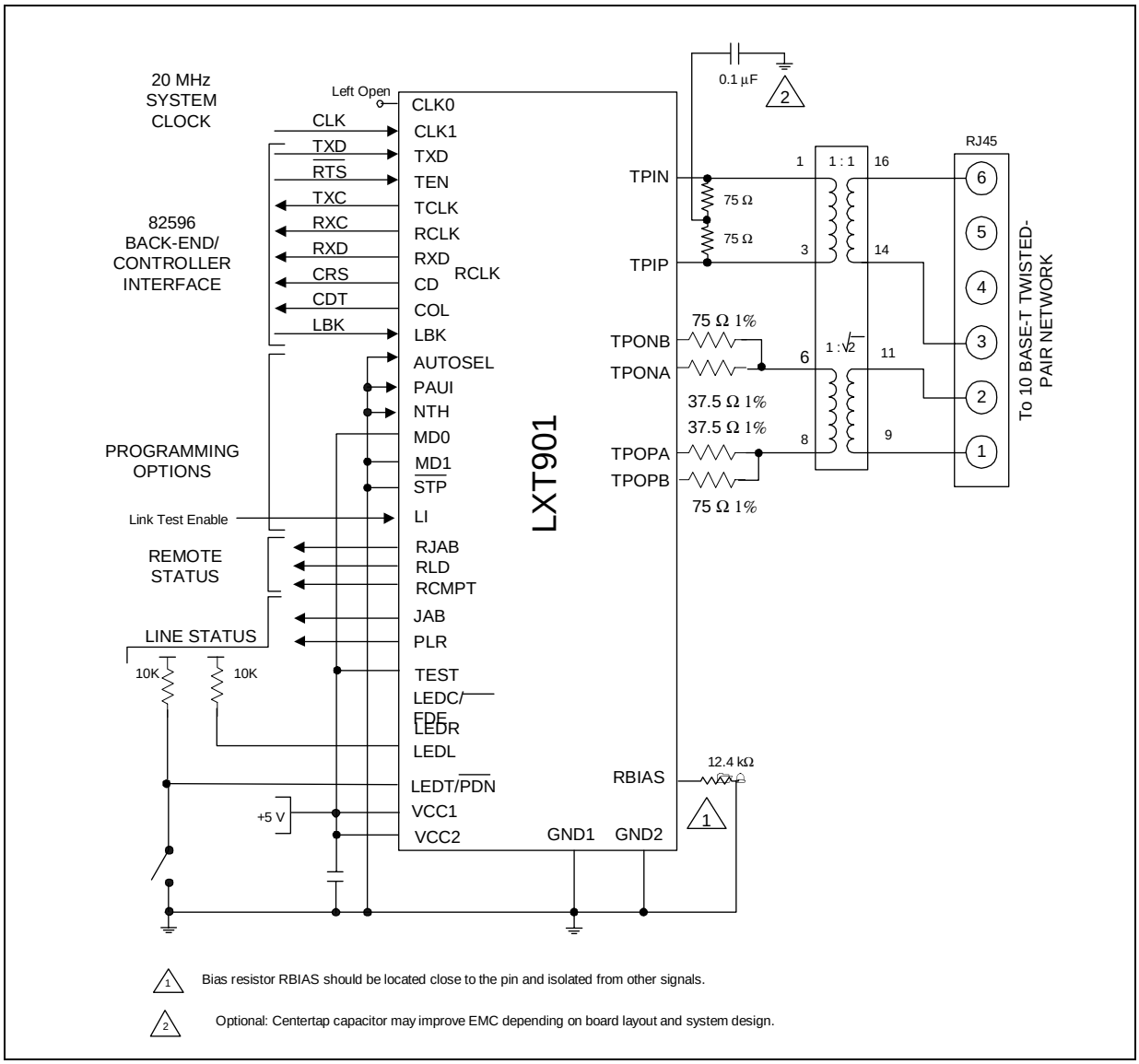


3.4.7 150Ω Shielded Twisted-Pair Only (LXT901 only)

Figure 16 shows the LXT901 in a typical twisted-pair only application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ-45 connector. (The AUI port is not used). With MD0 tied High and MD1 tied Low, the LXT901 logic and framing are set to Mode 2 (compatible with Intel 82596 controllers).

A 20 MHz system clock input at CLK1 is used in place of the crystal oscillator. (CLK0 is left open). The L1 pin externally controls the link test function. The UTP/$\overline{\text{STP}}$ and NTH pins are both tied Low, selecting the reduced receiver threshold and 150Ω termination for shielded twisted-pair cable. The switch at LEDT/PDN manually controls the power-down mode.

Figure 16. 150 Ω Shielded Twisted-Pair Only Application (LXT901)



1 Bias resistor RBIAS should be located close to the pin and isolated from other signals.

2 Optional: Centertap capacitor may improve EMC depending on board layout and system design.

4.0 Test Specifications

Note: Table 6 through Table 15 and Figure 17 through Figure 42 represent the performance specifications of the LXT901/907. These specifications are guaranteed by test except where noted "by design." Minimum and maximum values listed in Table 8 through Table 15 apply over the recommended operating conditions specified in Table 7.

For all Quality and Reliability issues (for example, parts packaging and thermal specifications), please send your questions to Intel at the following e-mail address: qr.requests@intel.com.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{CC}	-0.3	6	V
Storage temperature	T_{STG}	-65	+150	°C
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.				

Table 7. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage[1]	V_{CC}	4.75	5.0	5.25	V
Recommended operating temperature	T_{OP}	0	–	70	°C
1. Voltages with respect to ground unless otherwise specified. Power supply should be filtered to suppress high frequency transients, consistent with good PCB design.					

Table 8. I/O Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage[2]	V_{IL}	–	–	0.8	V	–
Input high voltage[2]	V_{IH}	2.0	–	–	V	–
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
	V_{OL}	–	–	10	%V_{CC}	I_{OL} < 10 µA
Output low voltage (Open drain LED driver)	V_{OLL}	–	–	0.7	%V_{CC}	I_{OLL} = 10 mA
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
	V_{OH}	90	–	–	%V_{CC}	I_{OH} < 10 µA
1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing. 2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.						

Table 8. I/O Electrical Characteristics (Continued)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output rise time TCLK & RCLK	CMOS	–	–	3	12	ns	C_{LOAD} = 20 pF
	TTL	–	–	2	8	ns	–
Output fall time TCLK & RCLK	CMOS	–	–	3	12	ns	C_{LOAD}= 20 pF
	TTL	–	–	2	8	ns	–
CLKI rise time (externally driven)		–	–	–	10	ns	–
CLKI duty cycle (externally driven)		–	–	50/50	40/60	%	–
Supply current	Normal Mode	I_{CC}	–	65	85	mA	Idle Mode
		I_{CC}	–	90	110	mA	Transmitting on twisted-pair
		I_{CC}	–	70	90	mA	Transmitting on AUI
	Power-Down Mode	I_{CC}	–	0.75	2	mA	–

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 9. AUI Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	I_{IL}	–	–	-700	µA	–
Input High current	I_{IH}	–	–	500	µA	–
Differential output voltage	V_{OD}	±550	–	±1200	mV	–
Differential squelch threshold	V_{DS}	150	250	350	mV	5 MHz square wave input

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 10. Twisted-Pair Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	–
Transmit timing jitter addition	–	–	±3.3	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections	–	–	±3.3	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 10. Twisted-Pair Electrical Characteristics (Continued)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive input impedance		ZIN	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential Squelch Threshold	Normal Threshold; NTH = High	VDS	300	400	585	mV	5 MHz square wave input
	Reduced Threshold; NTH = Low	VDS	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 11. Switching Characteristics

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10	24	ms

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 12. RCLK/Start-of-Frame Timing

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	tDATA	–	900	1100	ns
	Twisted-Pair	tDATA	–	1200	1500	ns
CD turn-on delay	AUI	tCD	–	25	200	ns
	Twisted-Pair	tCD	–	425	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2, 3 and 4	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2, 3 and 4	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (LXT907 only; Mode 3)		tsws	–	±90	–	ns

1. Typical values are at 25°C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 13. RCLK/End-of-Frame Timing

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Min	t_{RC}	5	1	27	5	bt
Rcv data throughput delay	Max	t_{RD}	400	375	375	375	ns
CD turn off delay[2]	Max	t_{CDOFF}	500	475	475	475	ns
Receive block out after TEN off	Typ[1]	t_{IFG}	5	50	–	–	bt
RCLK switching delay after CD off (LXT907 only; Mode 3)	Typ[1]	t_{SWE}	–	–	120(±80)	–	ns

1. Typical values are at 25° C and are for design aid only, are not guaranteed, and are not subject to production testing.
2. CD turn-off delay measured from middle of last bit: timing specification is unaffected by the value of the last bit.

Table 14. Transmit Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	t_{EHCH}	22	–	–	ns
TXD setup from TCLK	t_{DSCH}	22	–	–	ns
TEN hold after TCLK	t_{CHEL}	5	–	–	ns
TXD hold after TCLK	t_{CHDU}	5	–	–	ns
Transmit start-up delay - AUI	t_{STUD}	–	220	450	ns
Transmit start-up delay - Twisted-Pair	t_{STUD}	–	430	450	ns
Transmit through-put delay - AUI	t_{TPD}	–	–	300	ns
Transmit through-put delay - Twisted-Pair	t_{TPD}	–	300	350	ns

1. Typical values are at 25° C and are for design aid only, are not guaranteed, and are not subject to production testing.

Table 15. Collision, COL/CI Output and Loopback Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL turn-on delay	t_{COLD}	–	40	500	ns
COL turn-off delay	t_{COLOFF}	–	420	500	ns
COL (SQE) Delay after TEN off	t_{SQED}	0.65	1.2	1.6	µs
COL (SQE) Pulse Duration	t_{SQEP}	500	1000	1500	ns
LBK setup from TEN	t_{KHEH}	10	25	–	ns
LBK hold after TEN	t_{KHEL}	10	0	–	ns

1. Typical values are at 25° C and are for design aid only, are not guaranteed, and are not subject to production testing.

4.1 Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low) Figures 17 - 22

Figure 17. Mode 1 RCLK/Start-of-Frame Timing

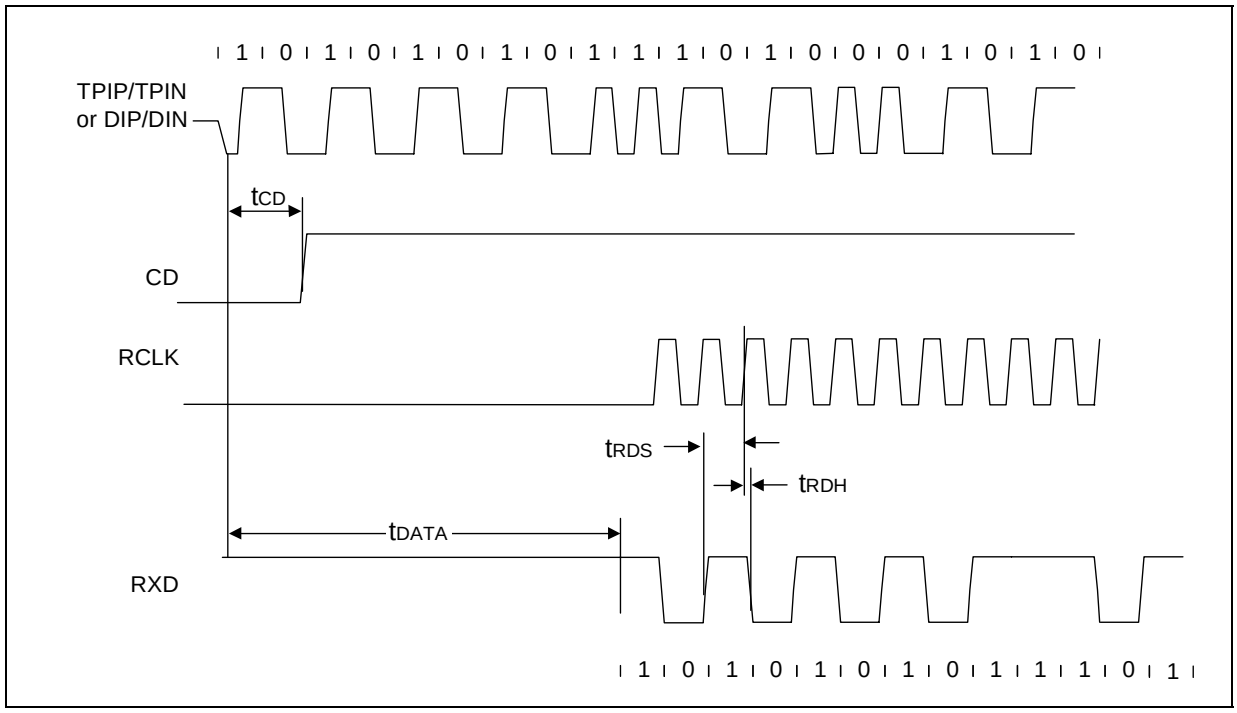


Figure 18. Mode 1 RCLK/End-of-Frame Timing

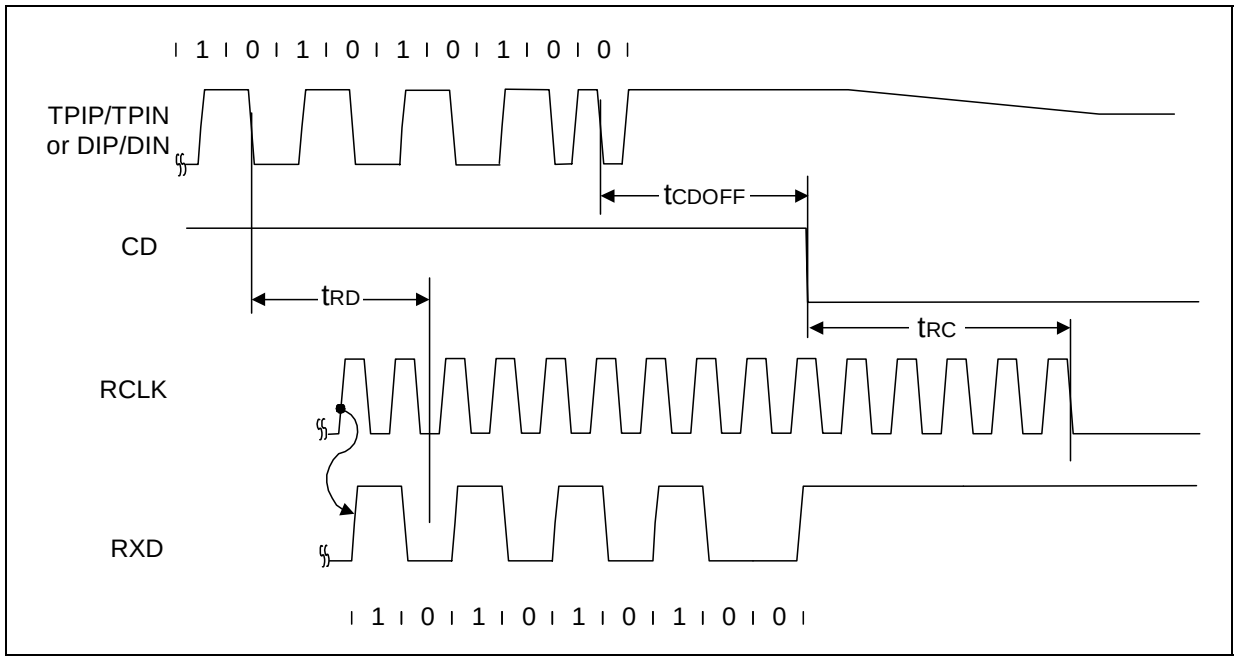


Figure 19. Mode 1 Transmit Timing

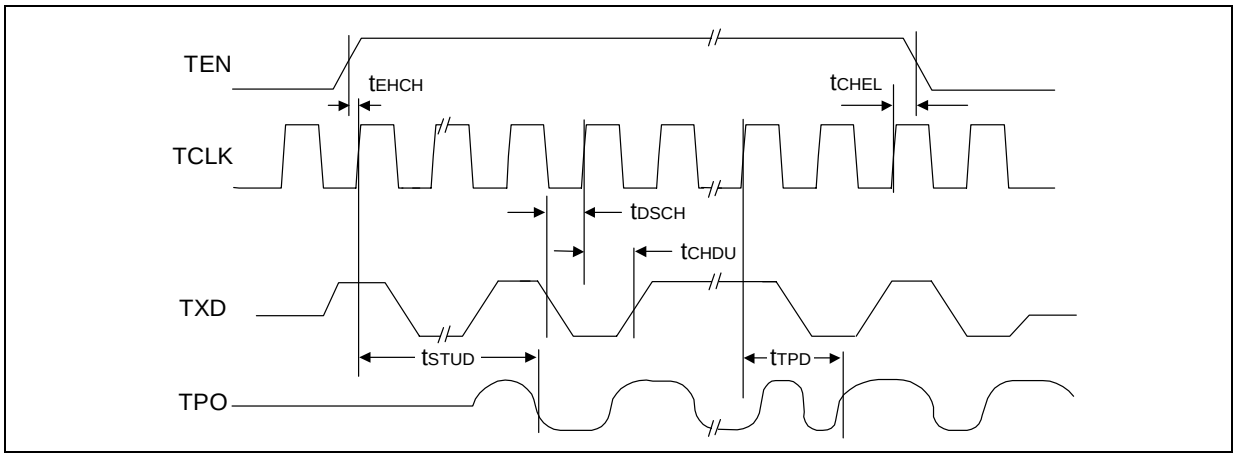


Figure 20. Mode 1 Collision Detect Timing

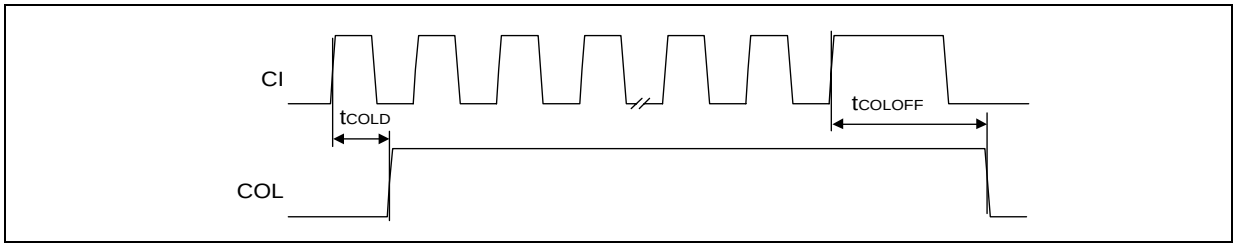


Figure 21. Mode 1 COL/CI Output Timing

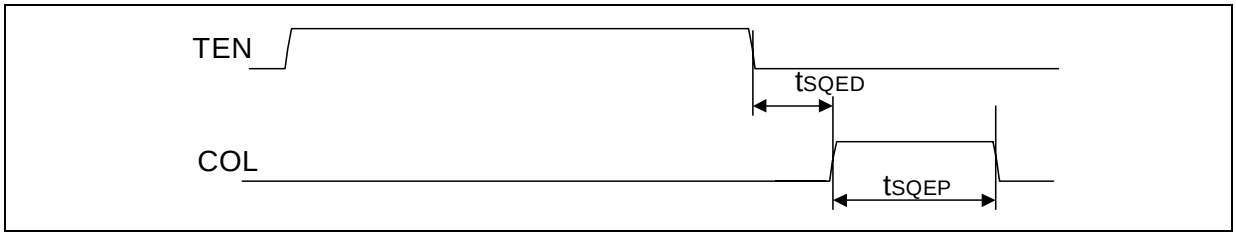
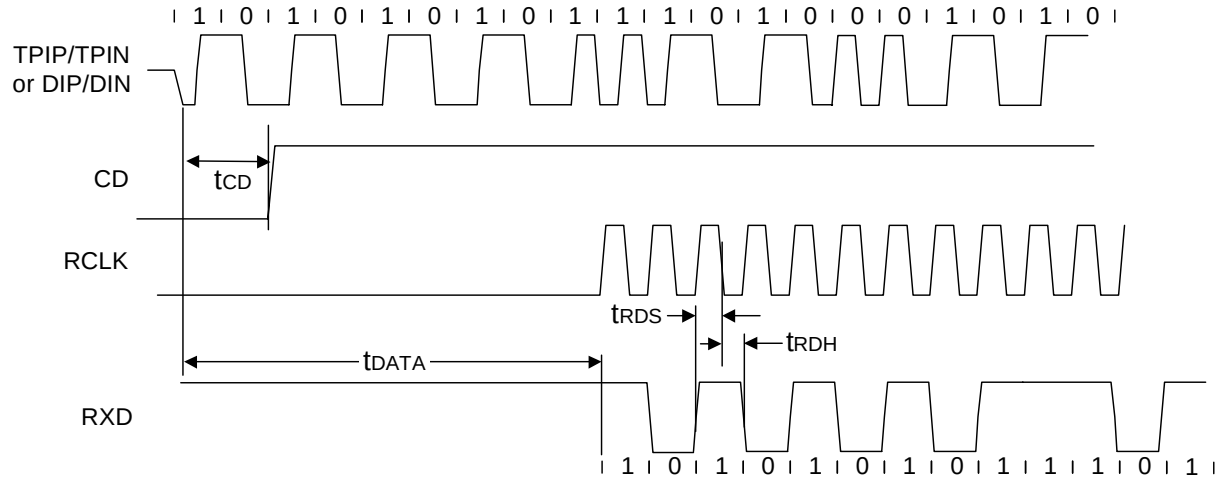


Figure 22. Mode 1 Loopback Timing

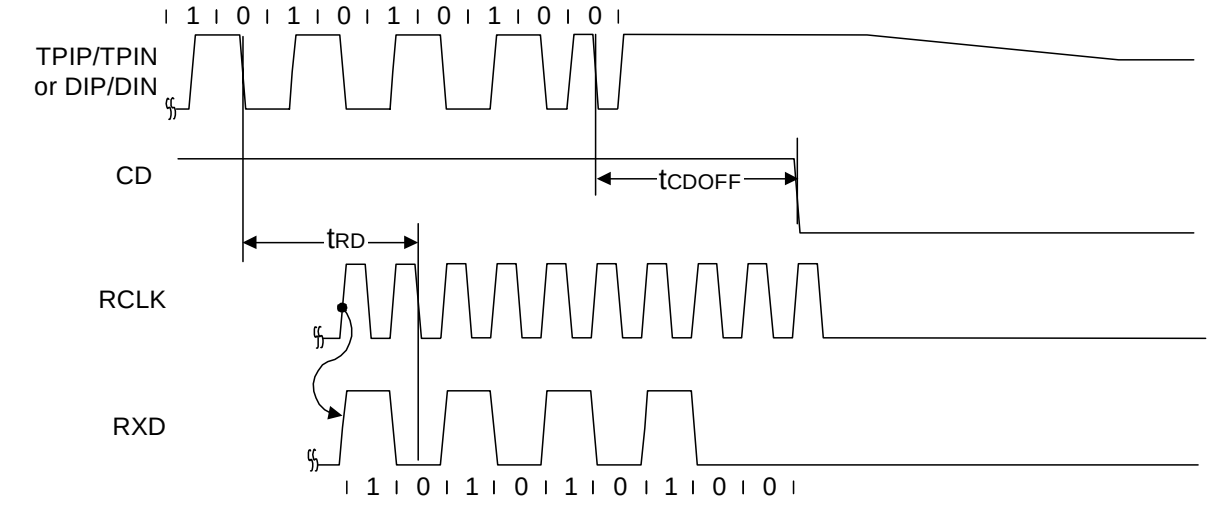
4.2 Timing Diagrams for Mode 2 (MD1=Low, MD0=High) Figures 23 - 28

Figure 23. Mode 2 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 24. Mode 2 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 25. Mode 2 Transmit Timing

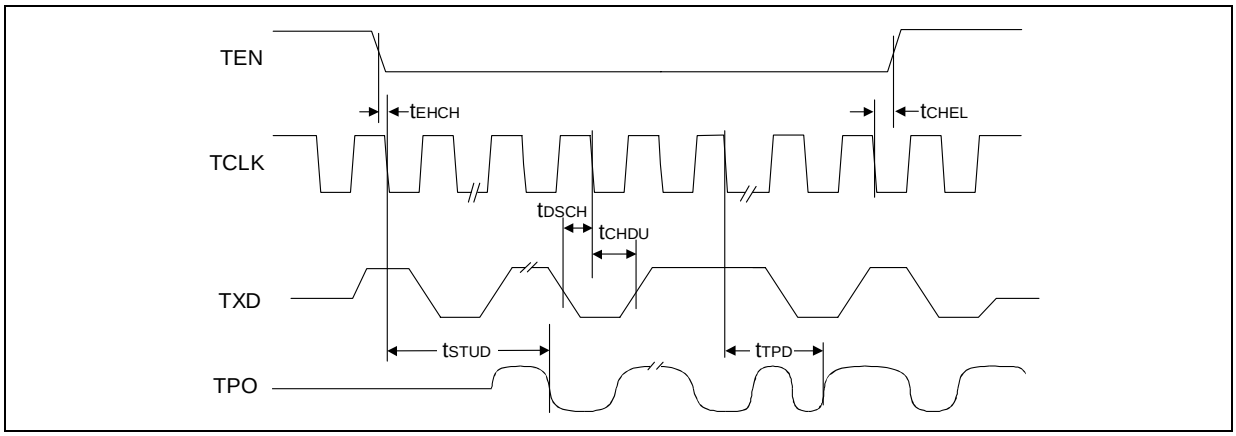


Figure 26. Mode 2 Collision Detect Timing

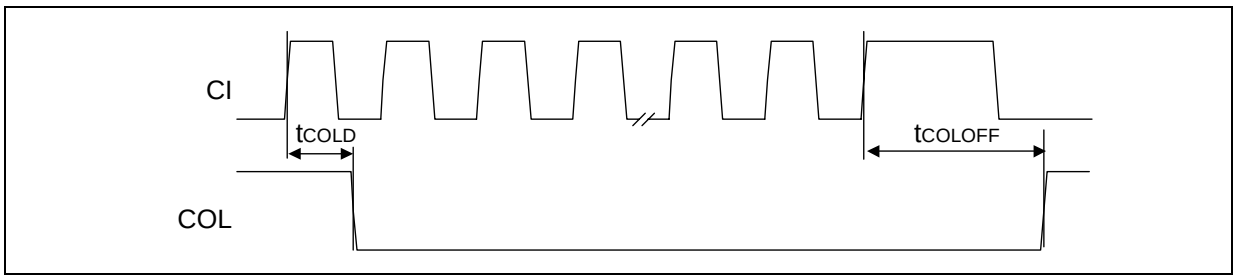


Figure 27. Mode 2 COL/CI Output Timing

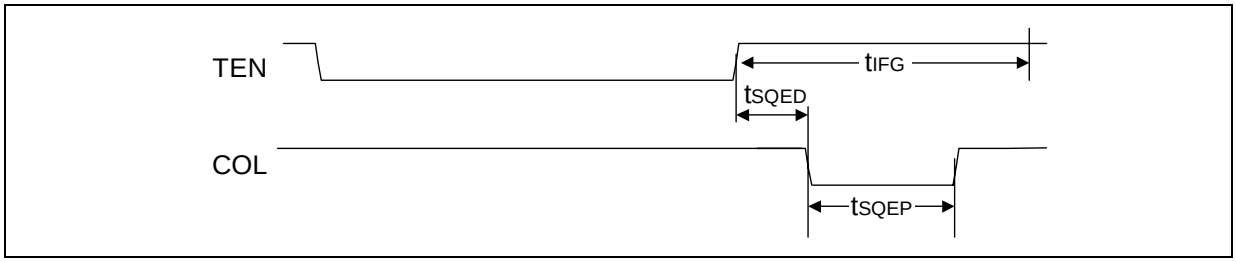
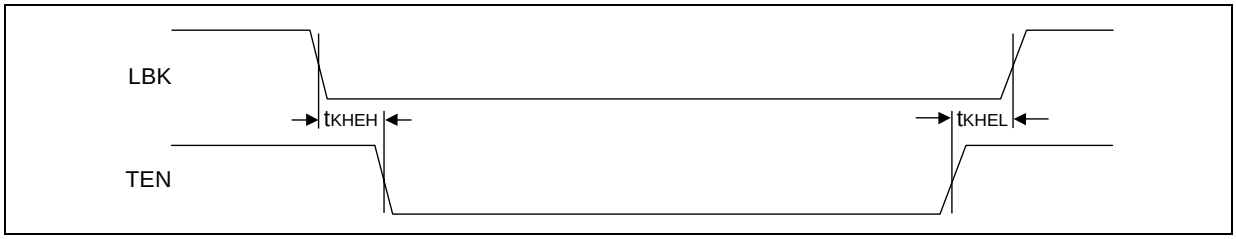
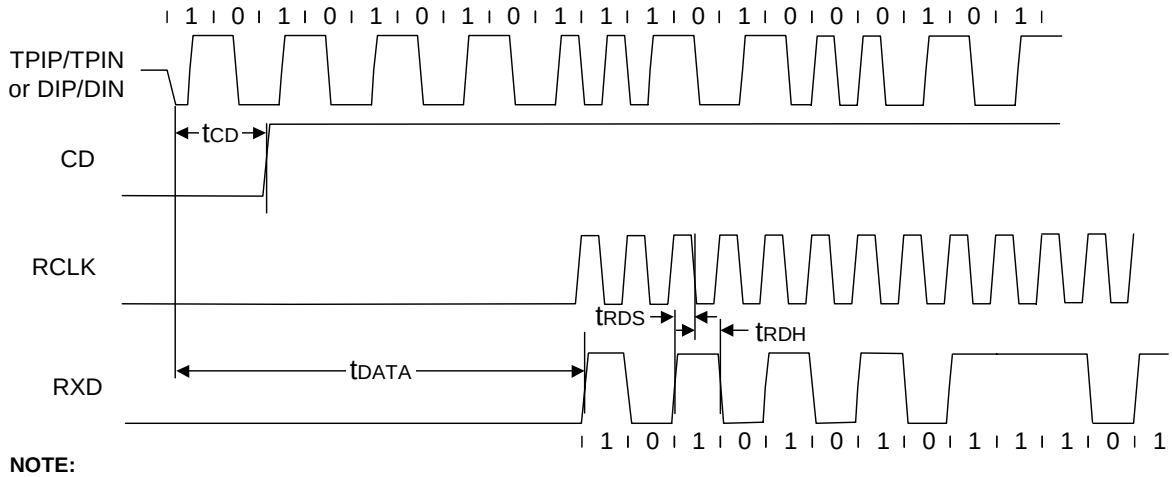


Figure 28. Mode 2 Loopback Timing



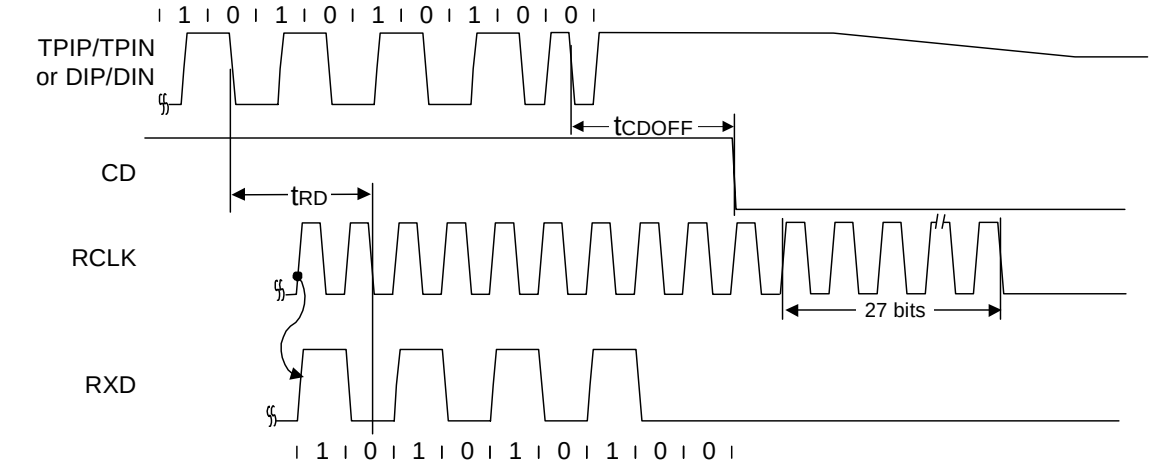
4.3 Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low) Figures 29 - 36

Figure 29. Mode 3 RCLK/Start-of-Frame Timing (LXT901 only)



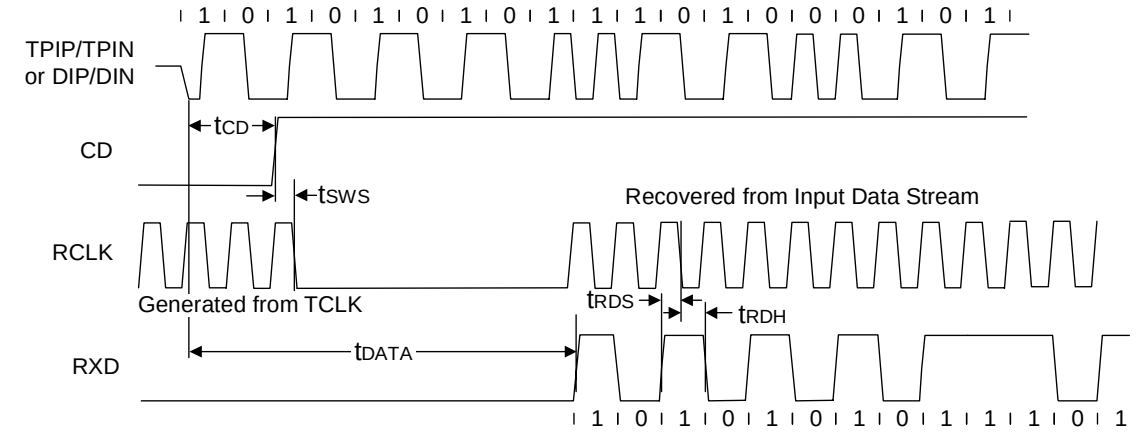
NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 30. Mode 3 RCLK/End-of-Frame Timing (LXT901 only)



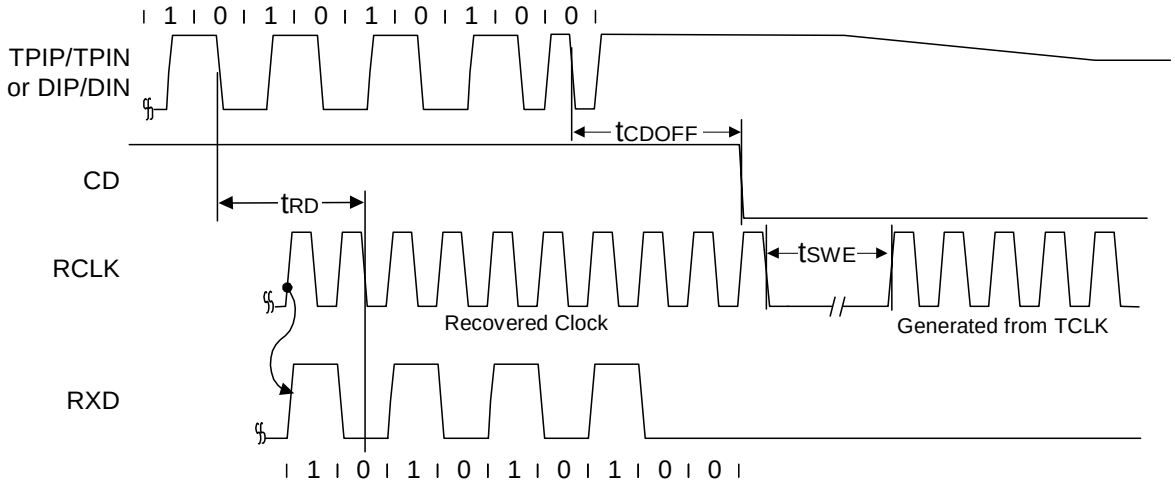
NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 31. Mode 3 RCLK/Start-of-Frame Timing (LXT907 only)



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 32. Mode 3 RCLK/End-of-Frame Timing (LXT907 only)



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 33. Mode 3 Transmit Timing

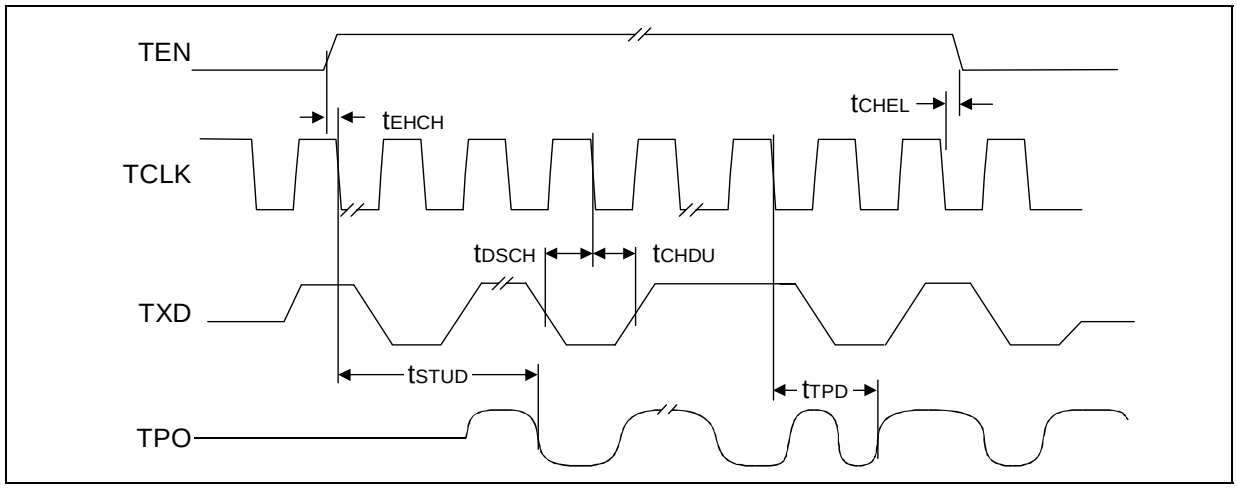


Figure 34. Mode 3 Collision Detect Timing

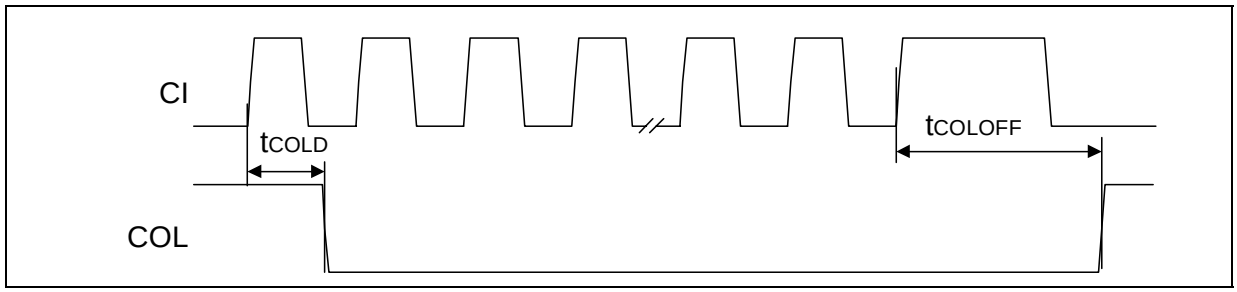
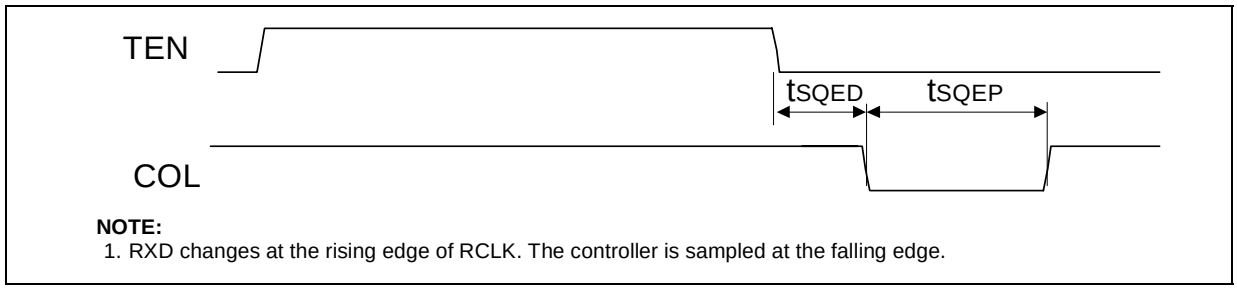


Figure 35. Mode 3 COL/CI Output Timing

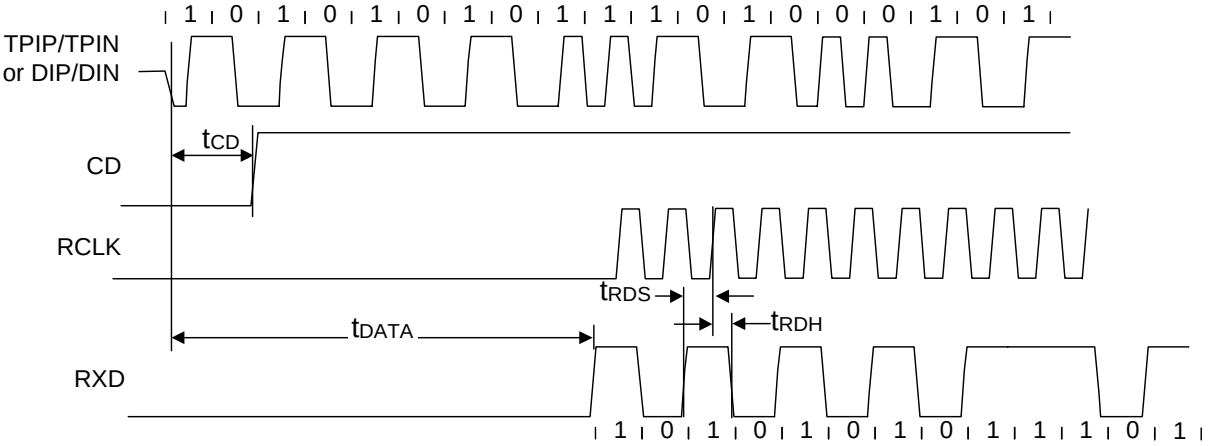


NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 36. Mode 3 Loopback Timing

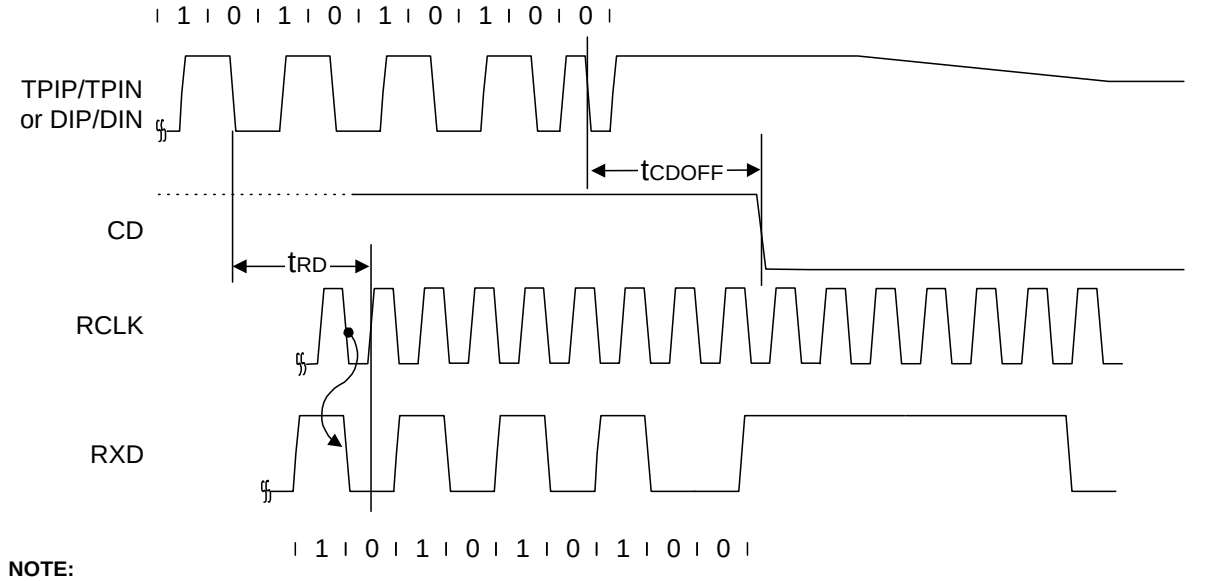
4.4 Timing Diagrams for Mode 4 (MD1 = High, MD0 = High) Figures 37 - 42

Figure 37. Mode 4 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 38. Mode 4 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 39. Mode 4 Transmit Timing

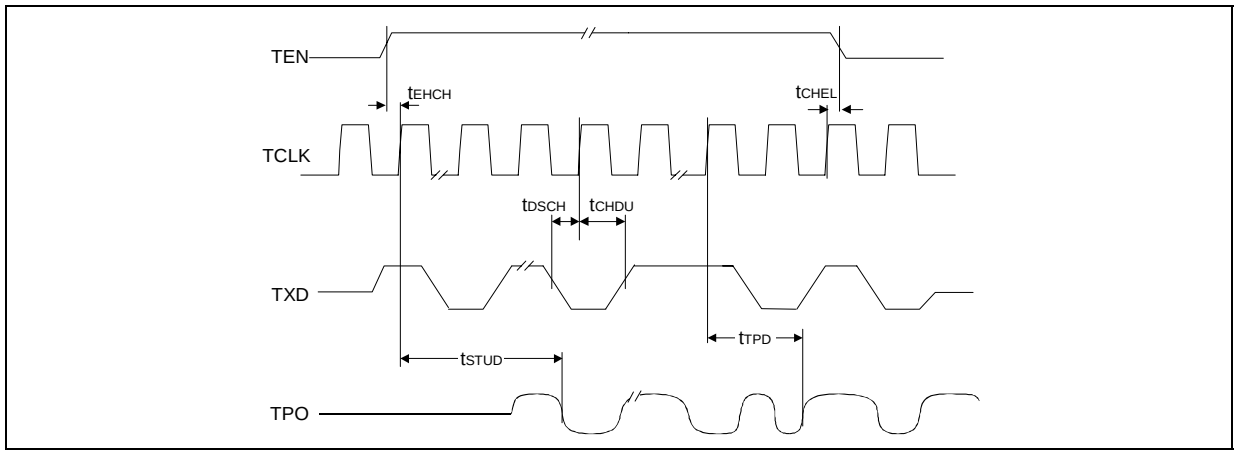


Figure 40. Mode 4 Collision Detect Timing

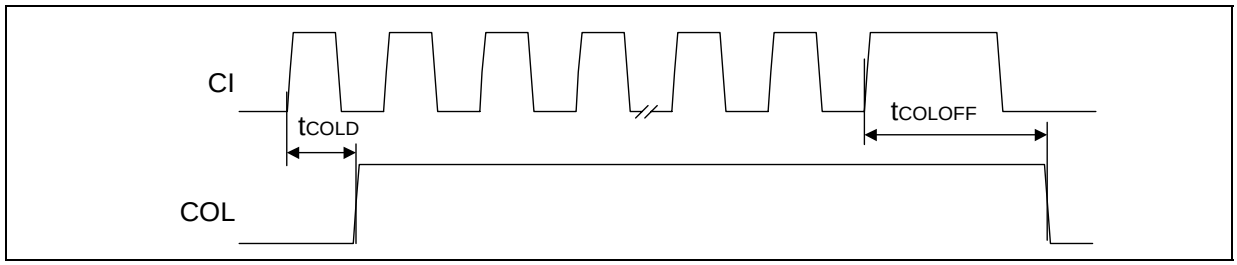


Figure 41. Mode 4 COL/CI Output Timing

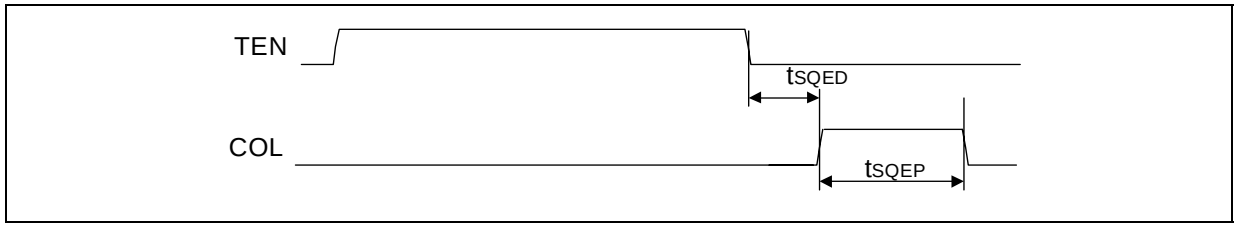
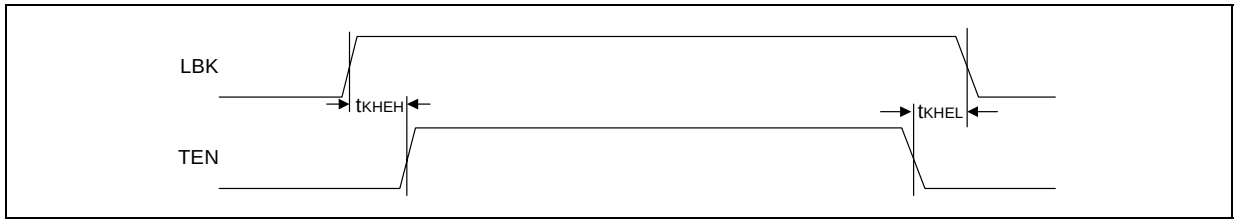


Figure 42. Mode 4 Loopback Timing

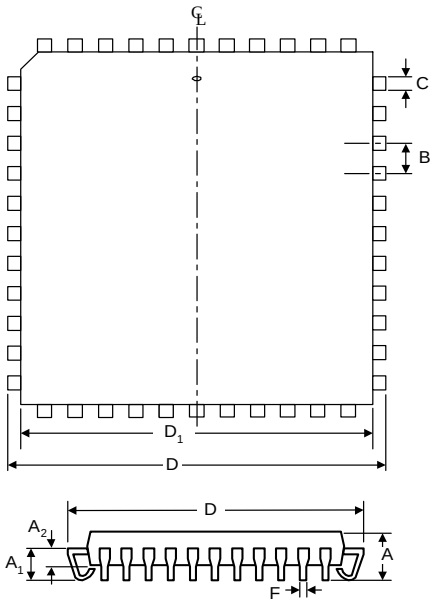


5.0 Mechanical Specifications

Figure 43. LXT901/907 Package Specifications

44-Pin PLCC

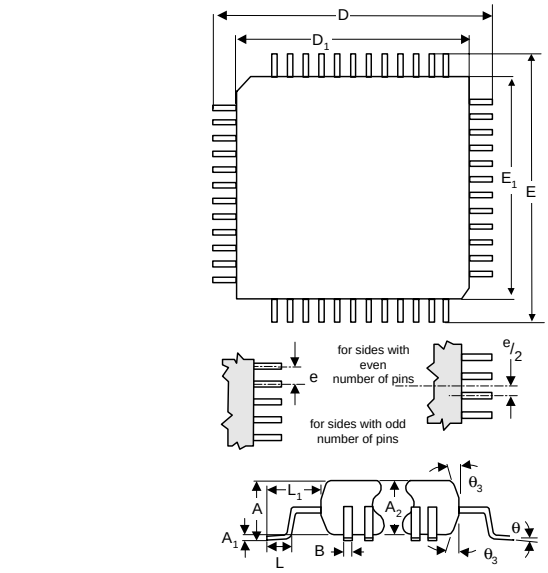
- Part Number LXT901PC and LXT907PC
- Commercial Temp Range (0°C to 70°C)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	0.685	0.695	17.399	17.653
D1	0.650	0.656	16.510	16.662
F	0.013	0.021	0.330	0.533

64-Pin LQFP

- Part Number LXT901LC
- Commercial Temp Range (0°C to 70°C)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.063	–	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	.011	0.17	0.27
D	0.472 BSC		12.00 BSC	
D1	0.394 BSC		10.00 BSC	
E	0.472 BSC		12.00 BSC	
E1	0.394 BSC		10.00 BSC	
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
L1	0.039 REF		1.00 REF	
θ3	11°	13°	11°	13°
θ	0°	7°	0°	7°

Appendix A Ordering Information

Table 16. Product Information

Number	Revision	Qualification	Tray MM	Tape & Reel MM
DJLXT901LC.E2	E2	S	831686	831803
NLXT901PC.E2	E2	S	831657	831813
NLXT907PC.E2	E2	S	831666	831822

Figure 44. Ordering Information - Sample