Product Brief

FW801A/FW801BF

Low-Power PHY One-Cable Transceiver/Arbiter Devices

FEATURES

- Compliant with IEEE® Standard 1394a-2000, IEEE Standard for a High Performance Serial Bus Amendment 1.
- Supports extended BIAS_HANDSHAKE time for enhanced interoperability with camcorders.
- While unpowered and connected to the bus, will not drive TPBIAS on a connected port even if receiving incoming bias voltage on that port.
- Does not require external filter capacitors for PLL.
- Does not require a separate 5 V supply for 5 V link controller interoperability.
- Interoperable across 1394 cable with 1394 physical layers (PHY) using 5 V supplies.
- Interoperable with 1394 link-layer controllers using 5 V supplies.
- Powerdown features to conserve energy in battery powered applications include the following:
  - — Device powerdown ball.
  - — Link interface disable using LPS.
  - — Inactive ports powerdown.
  - — Automatic micro-low-power sleep mode during suspend.
- Interface to link-layer controller supports Annex J electrical isolation as well as bus-keeper isolation.
- Provides one fully compliant cable port at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s.
- Fully supports 1394 Open HCI requirements.
- Supports arbitrated short bus reset to improve utilization of the bus.
- Supports ack-accelerated arbitration and fly-by concatenation.
- Supports connection debounce.
- Supports multispeed packet concatenation.
- Supports PHY pinging and remote PHY access packets.
- Fully supports suspend/resume.
- Supports PHY-link interface initialization and reset.
- Supports 1394a-2000 register set.
- Supports LPS/link-on as a part of PHY-link interface.
- Supports provisions of IEEE 1394-1995 Standard for a High Performance Serial Bus.
- Fully interoperable with FireWire® and i.LINK® implementations of IEEE 1394-1995.
- Reports cable power fail interrupt when voltage at CPS ball falls below 7.5 V.
- Provides separate cable bias and driver termination voltage supply for port. Other Features

OTHER FEATURES

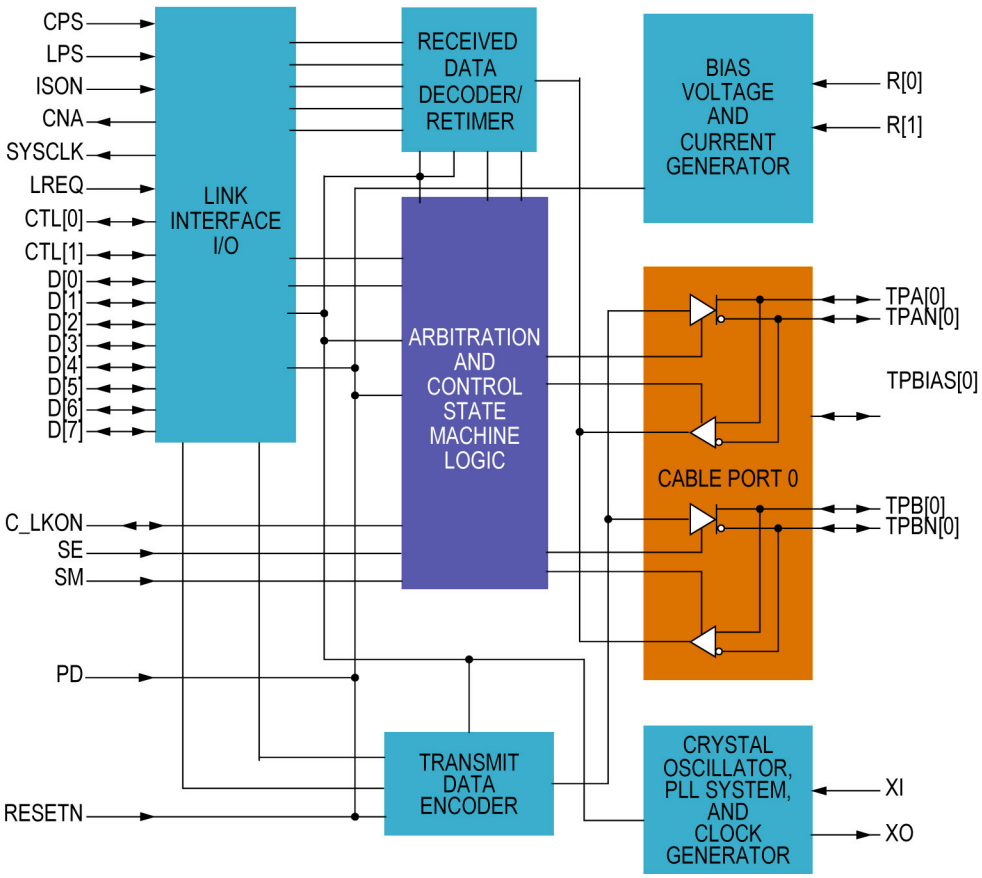
- 48-pin TQFP and 48-ball VTFSBGAC packages.
- Single 3.3 V supply operation.
- Data interface to link-layer controller provided through 2/4/8 parallel lines at 50 Mbits/s.
- 25 MHz crystal oscillator and PLL provide a 50 MHz link-layer controller clock as well as transmit/receive data at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s.
- Multiple separate package signals provided for analog and digital supplies and grounds.

FW801 Functional Overview

The LSI FW801 devices provide the analog physical layer functions needed to implement a one-port node in a cable-based IEEE 1394-1995 and IEEE 1394a-2000 network.

The cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The PHY is designed to interface with a link-layer controller (LLC).

Functional Block Diagram



ORDERING INFORMATION:		
Device	Comcode	Package
FW801A-DB	108698374	48-Pin TQFP
L-FW801A-DB*	7000795450	48-Pin TQFP
FW801BF-09-DB	7000482230	48-Ball VTFSBGAC
L-FW801BF-DB*	700077706	48-Ball VTFSBGAC

* Lead-free: No intentional addition of lead, and less than 1000 ppm. LSI lead-free devices are fully compliant with the Restriction of Hazardous Substances (RoHS) directive that restricts the content of six hazardous substances in electronic equipment in the European Union. Beginning July 1, 2006, electronic equipment sold in the European Union must be manufactured in accordance with the standards set by the RoHS directive.

FireWire

For more information and sales office locations, please visit the LSI web sites at: lsi.com lsi.com/contacts

June 2006
PB06-052CMPR