Si3050 + Si3011

FCC/TBR21 VOICE DAA

Features

- PCM highway data interface
- μ-law/A-law companding
- SPI control interface
- GCI interface
- 80 dB dynamic range TX/RX
- Line voltage monitor
- Loop current monitor
- +6 dBm TX/RX level mode
- Parallel handset detection
- 3 μA on-hook line monitor current
- Overload detection
- Programmable ac termination
- TIP/RING polarity detection
- Integrated codec and 2- to 4-wire analog hybrid
- Programmable digital hybrid for near-end echo reduction
- Polarity reversal detection
- Programmable digital gain in 0.1 dB increments
- Integrated ring detector
- Type I and II caller ID support
- Pulse dialing support
- 3.3 V power supply
- Daisy-chaining for up to 16 devices
- Greater than 5000 V isolation
- Patented isolation technology
- Ground start and loop start support
- Available in Pb-free RoHS-compliant packages

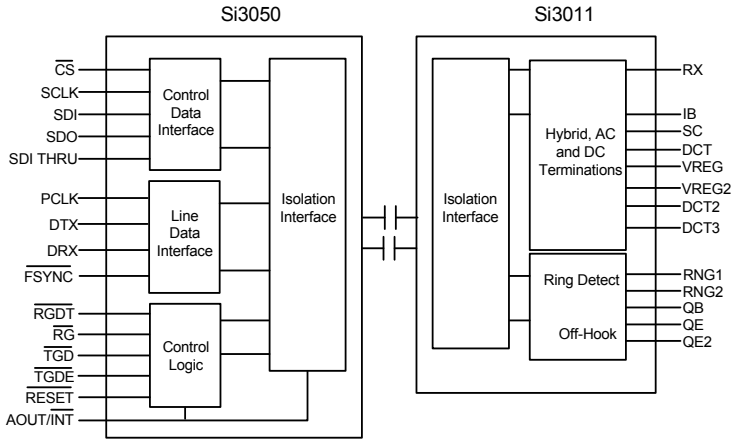
Applications

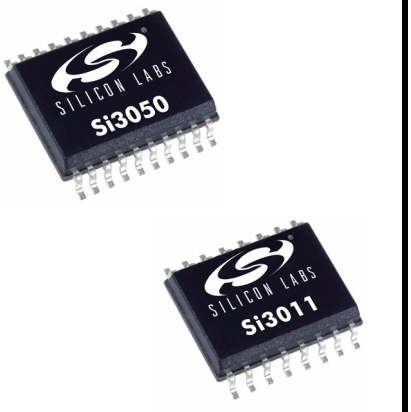
- DSL IADs
- VoIP gateways
- PBX and IP-PBX systems
- Voice mail systems

Description

The Si3050+Si3011 Voice DAA chipset provides a highly-programmable foreign exchange office (FXO) analog interface that is ideal for DSL IADs, PBXs, IP-PBXs, and VoIP gateway products. The solution implements Silicon Laboratories' patented isolation capacitor technology, which eliminates the need for costly isolation transformers, relays, or opto-isolators, while providing superior surge immunity for robust field performance. The Voice DAA is available in one 20-pin TSSOP (Si3050) and one 16-pin TSSOP/SOIC (Si3011) and requires minimal external components. The Si3050 interfaces directly to standard telephony PCM interfaces.

Functional Block Diagram



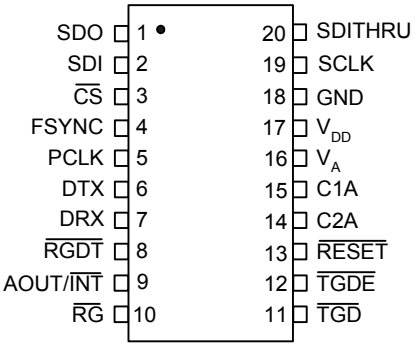


Ordering Information

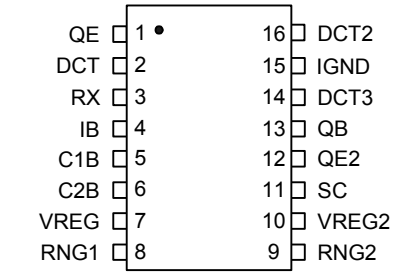
See page 96.

Pin Assignments

Si3050



Si3011



US Patent# 5,870,046
US Patent# 6,061,009
Other Patents Pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions and Thermal Information

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	F-Grade	0	25	70	°C
		G-Grade	–40	25	85	
Si3050 Supply Voltage, Digital	V_D		3.0	3.3	3.6	V
Thermal Resistance (Si3011)[3]	θ_{JA}	SOIC-16	—	77	—	°C/W
		TSSOP-16	—	89	—	°C/W
Thermal Resistance (Si3050)[3]	θ_{JA}	TSSOP-20	—	84	—	°C/W

Notes:
1. The Si3050 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si3050 and any Si3011 are used. See "2. Typical Application Schematic" on page 17 for the typical application circuit.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. Operation above 125 °C junction temperature may degrade device reliability.

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, see Figure 1 on page 6)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 1 DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 1 DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ILIM = 1 DCR = 0	—	—	40	V
On-Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	5	µA
Operating Loop Current	I_{LP}	ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	ILIM = 1	10	—	60	mA
DC Ring Current		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT2 = 0	13.5	15	16.5	V_{rms}
Ring Frequency	F_R		13	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

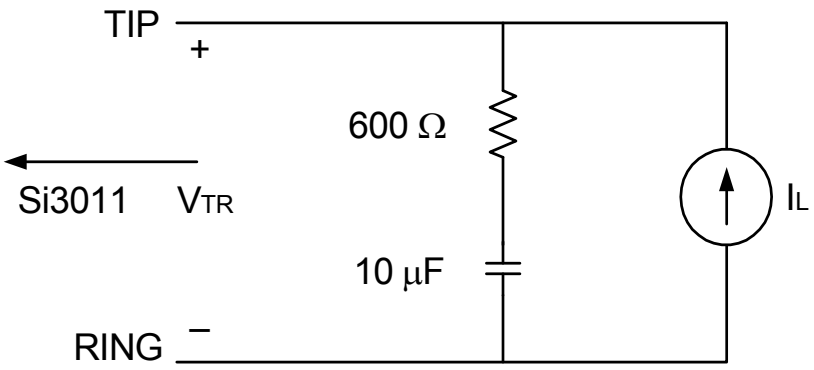


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F/K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage[1]	V_{IH}		2.0	—	—	V
Low Level Input Voltage[1]	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
AOUT High Level Voltage	V_{AH}	I_O = 10 mA	2.4	—	—	V
AOUT Low Level Voltage	V_{AL}	I_O = 10 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Digital[2]	I_D	V_D pin	—	8.5	10	mA
Total Supply Current, Sleep Mode[2]	I_D	PDN = 1, PDL = 0	—	5.0	6.0	mA
Total Supply Current, Deep Sleep[2,3]	I_D	PDN = 1, PDL = 1	—	1.3	1.5	mA

Notes:

1. V_{IH}/V_{IL} do not apply to C1A/C2A.
2. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs are held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
3. $\overline{\text{RGDT}}$ is not functional in this state.

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F/K-Grade, Fs = 8000 Hz, see "2. Typical Application Schematic" on page 17)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		8	—	16	kHz
PCLK Input Frequency	PCLK		256	—	8192	kHz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	—	200	—	Hz
Transmit Full-Scale Level[1]	V_{FS}	FULL2 = 1 (+6.0 dBm)[2]	—	2.16	—	V_{PEAK}
Receive Full-Scale Level[1,3]	V_{FS}	FULL2 = 1 (+6.0 dBm)[2]	—	2.16	—	V_{PEAK}
Dynamic Range[4,5,6]	DR	ILIM = 1, FULL2 = 0 DCR = 0, I_L = 20, 50, 100 mA	—	80	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ILIM = 1, FULL2 = 0 DCR = 0, I_L = 20, 50 mA	—	–78	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ILIM = 1, FULL2 = 0 DCR = 0, I_L = 100 mA	—	–72	—	dB
Dynamic Range (Caller ID mode)[8]	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	62	—	dB
Caller ID Full-Scale Level[8]	V_{CID}		—	1.5	—	V_{PEAK}
Gain Accuracy[6,9]		2-W to DTX, TXG2, RXG2, TXG3, and RXG3 = 0000	–0.5	0	0.5	dB
Transhybrid Balance[10]		300–3.4 kHz, $Z_{ACIM} = Z_{LINE}$	20	—	—	dB
Transhybrid Balance[10]		1 kHz, $Z_{ACIM} = Z_{LINE}$	—	30	—	dB
Two-Wire Return Loss		300–3.4 kHz, all ac terminations	25	—	—	dB
Two-Wire Return Loss		1 kHz, all ac terminations	—	32	—	dB

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1 on page 6.
2. With FULL2 = 1, the transmit and receive full-scale level of +6.0 dBm can be achieved with a 600 Ω termination. In this mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
3. Receive full-scale level produces –0.9 dBFS at DTX.
4. DR = 20 x log (RMS V_{FS}/RMS Vin) + 20 x log (RMS V_{in}/RMS noise). The RMS noise measurement excludes harmonics. Here, V_{FS} is the 0 dBm full-scale level per Note 1 above.
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
6. Vin = 1 kHz, –3 dBFS.
7. THD = 20 x log (RMS distortion/RMS signal).
8. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log (RMS V_{IN}/RMS noise). V_{CID} is the 1.5 V full-scale level with the enhanced caller ID circuit. With the typical CID circuit, the V_{CID} full-scale level is 6 V peak, and the DR_{CID} decreases to 50 dB.
9. Refer to Tables 10–11 for relative gain accuracy characteristics (passband ripple).
10. Analog hybrid only. Z_{ACIM} controlled by ACIM in Register 30.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 3.6	V
Input Current, Si3050 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Ambient Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage can occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.

Table 6. Switching Characteristics—General Inputs

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Min	Typ	Max	Unit
Cycle Time, PCLK	t_p	0.12207	—	3.90625	µs
PCLK Duty Cycle	t_{dty}	40	50	60	%
PCLK Jitter Tolerance	t_{jitter}	—	—	2	ns
Rise Time, PCLK	t_r	—	—	25	ns
Fall Time, PCLK	t_f	—	—	25	ns
PCLK Before $\overline{\text{RESET}}$ ↑[2]	t_{mr}	10	—	—	cycles
$\overline{\text{RESET}}$ Pulse Width[3]	t_{rl}	250	—	—	ns
$\overline{\text{CS}}$, SCLK Before $\overline{\text{RESET}}$↑	t_{mxr}	20	—	—	ns
Rise Time, Reset	t_r	—	—	25	ns

Notes:

1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC/PCLK relationship must be fixed after $\overline{\text{RESET}}$↑.
3. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250 ns or 10 PCLK cycle times.

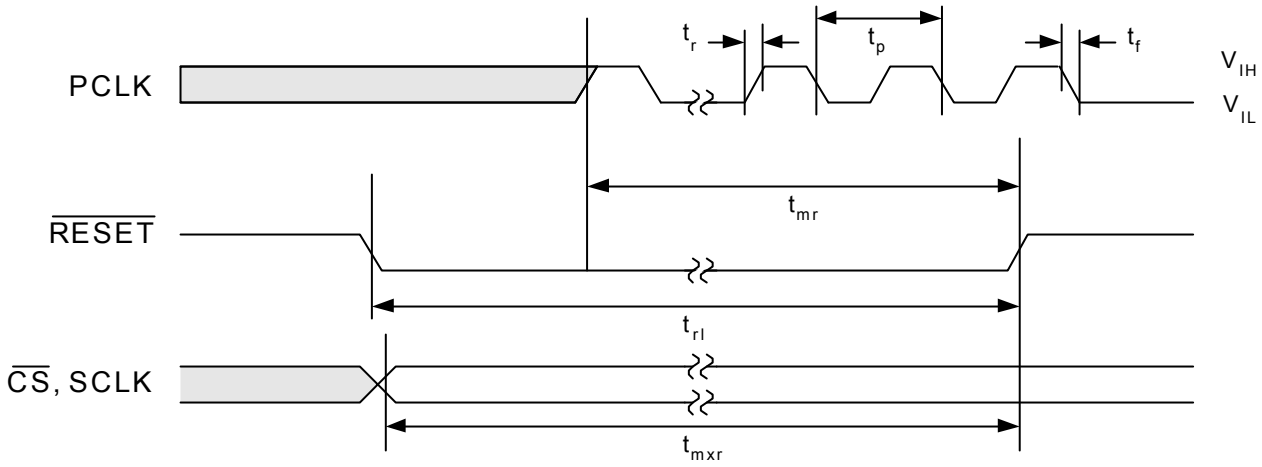


Figure 2. General Inputs Timing Diagram

Table 7. Switching Characteristics—Serial Peripheral Interface

(V_{IO} = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter*	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		61.03	—	—	ns
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, $\overline{CS}$ to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, SCLK to $\overline{CS}$ Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SCLK Rise to SDI Transition	t_{h2}		20	—	—	ns
Delay time between chip selects	t_{cs}		220	—	—	ns
Propagation Delay, SDI to SDITHRU			—	6	—	ns

***Note:** All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.

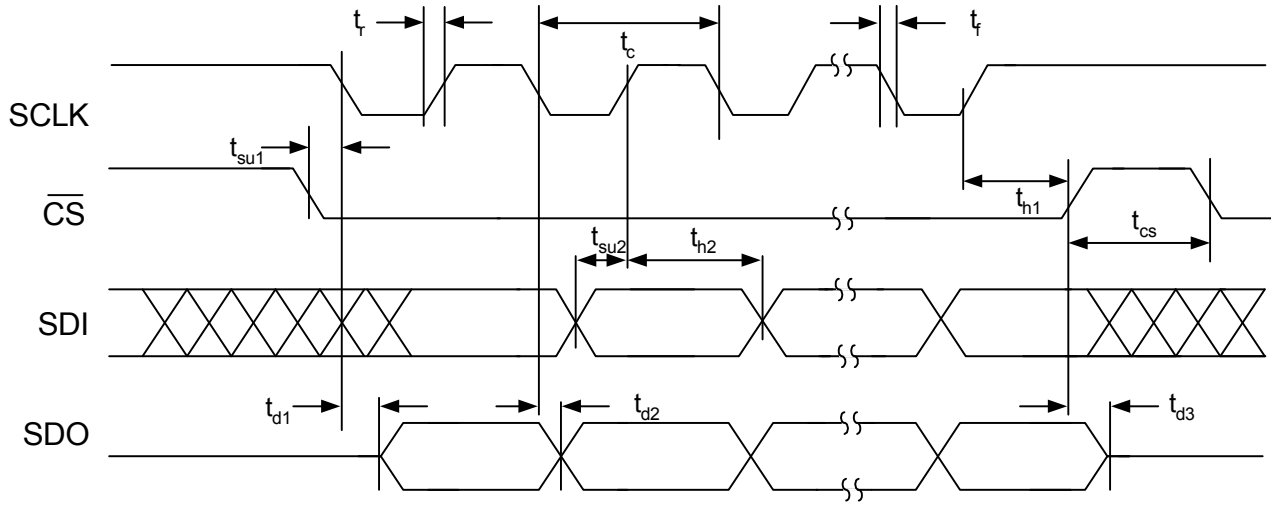


Figure 3. SPI Timing Diagram

Table 8. Switching Characteristics—PCM Highway Serial Interface

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Units
Cycle Time PCLK	t_p		122	—	3906	ns
Valid PCLK Inputs			— — — — — — — —	256 512 768 1.024 1.536 2.048 4.096 8.192	— — — — — — — —	kHz kHz kHz MHz MHz MHz MHz MHz
FSYNC Period[2]	t_{fp}		—	125	—	µs
PCLK Duty Cycle	t_{dty}		40	50	60	%
PCLK Jitter-Tolerance	t_{jitter}		—	—	2	ns
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-State[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC Rise to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, PCLK Fall to FSYNC Fall	t_{h1}		20	—	—	ns
Setup Time, DRX Transition to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCLK Falling to DRX Transition	t_{h2}		20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_O - 0.4$ V, V_{IL} = 0.4 V, rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC must be 8 kHz under all operating conditions.
3. Specification applies to PCLK fall to DTX tri-state when that mode is selected.

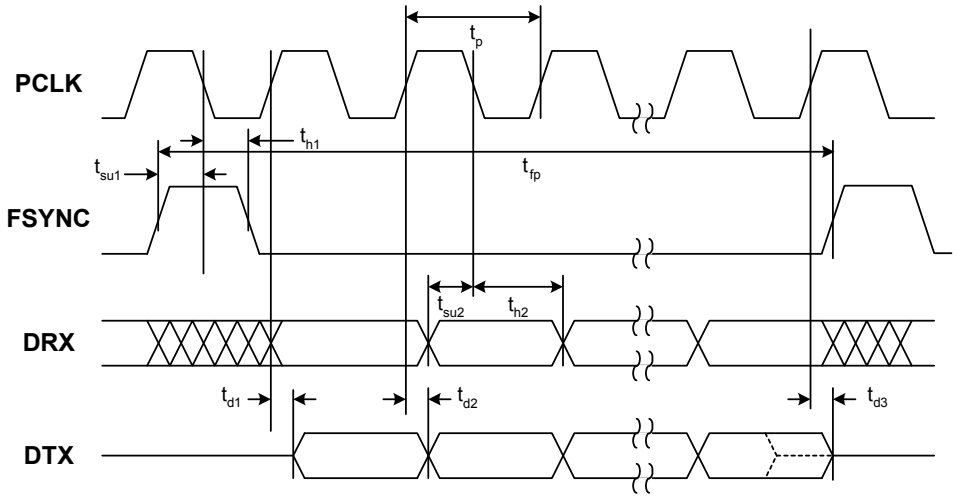


Figure 4. PCM Highway Interface Timing Diagram (RXS = TXS = 1)

Table 9. Switching Characteristics—GCI Highway Serial Interface
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Units
Cycle Time PCLK (Single Clocking Mode)	t_p		—	488	—	ns
Cycle Time PCLK (Double Clocking Mode)	t_p		—	244	—	ns
Valid PCLK Inputs			— —	2.048 4.096	— —	MHz MHz
FSYNC Period[2]	t_{fp}		—	125	—	µs
PCLK Duty Cycle	t_{dty}		40	50	60	%
PCLK Jitter Tolerance	t_{jitter}		—	—	2	ns
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-State[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC Rise to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, PCLK Fall to FSYNC Fall	t_{h1}		20	—	—	ns
Setup Time, DRX Transition to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCLK Falling to DRX Transition	t_{h2}		20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_O - 0.4$ V, V_{IL} = 0.4 V, rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC must be 8 kHz under all operating conditions.
3. Specification applies to PCLK fall to DTX tri-state when that mode is selected.

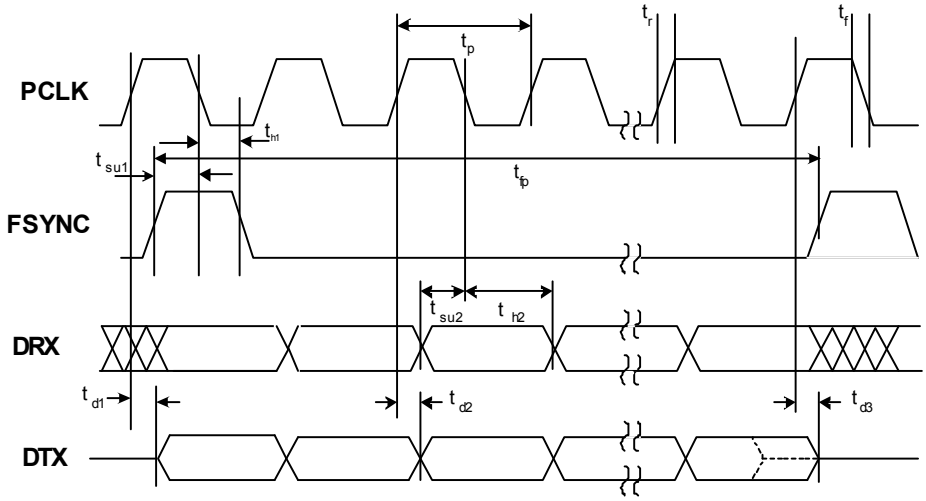


Figure 5. GCI Highway Interface Timing Diagram (1x PCLK Mode)

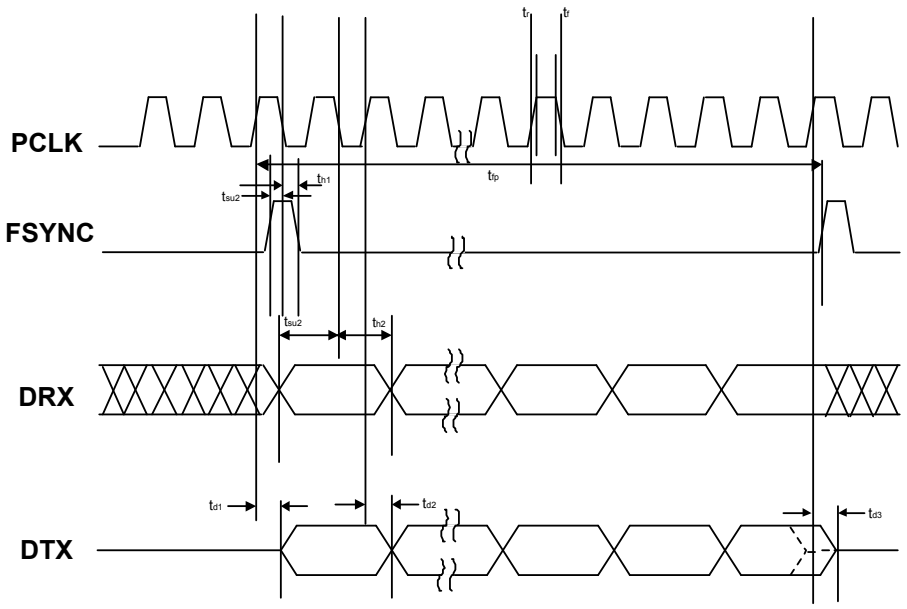


Figure 6. GCI Highway Interface Timing Diagram (2x PCLK Mode)

Table 10. Digital FIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	s
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 7, 8, 9, and 10.					

Table 11. Digital IIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	s
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 11, 12, 13, and 14. Figures 15 and 16 show group delay versus input frequency.					

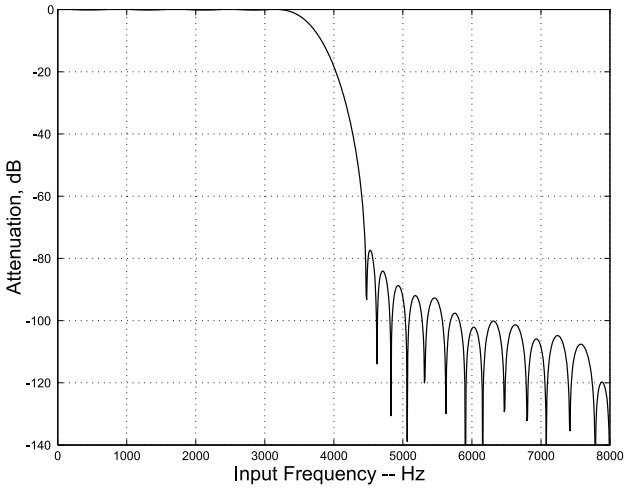


Figure 7. FIR Receive Filter Response

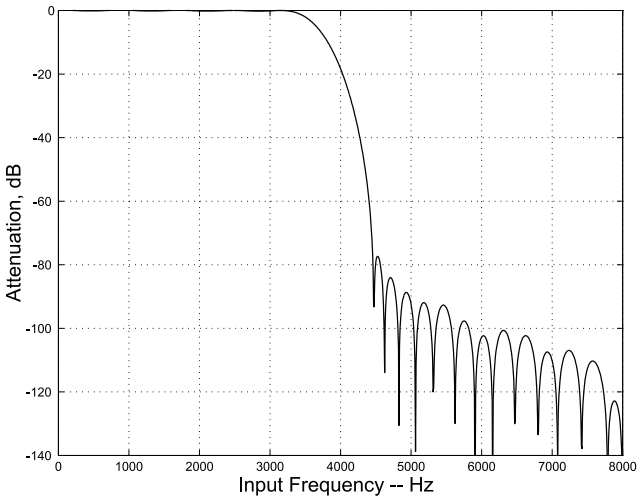


Figure 9. FIR Transmit Filter Response

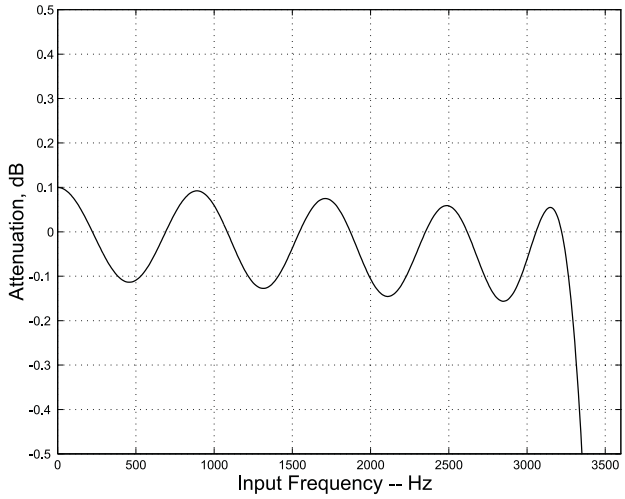


Figure 8. FIR Receive Filter Passband Ripple

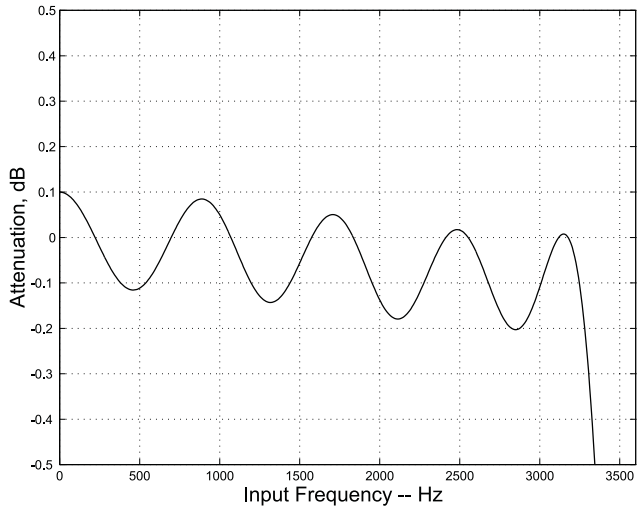


Figure 10. FIR Transmit Filter Passband Ripple

For Figures 7–10, all filter plots apply to a sample rate of Fs = 8 kHz.

For Figures 11–14, all filter plots apply to a sample rate of Fs = 8 kHz.

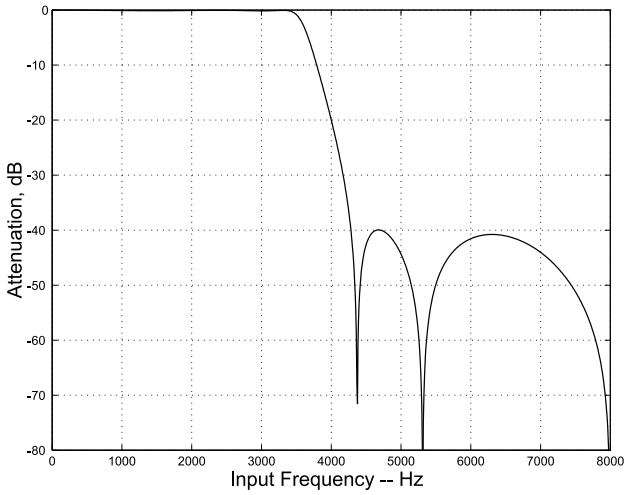


Figure 11. IIR Receive Filter Response

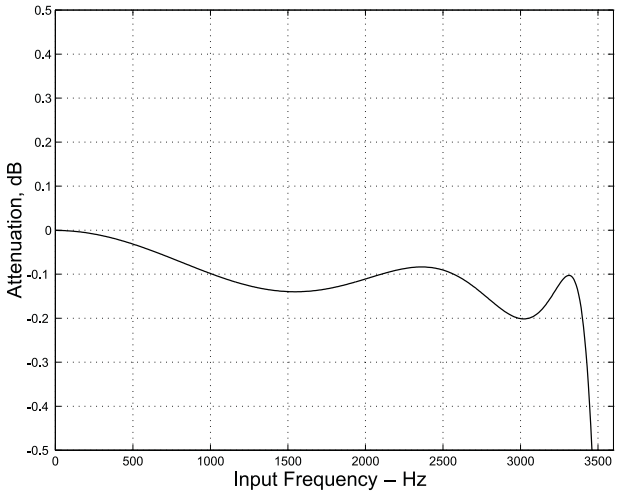


Figure 14. IIR Transmit Filter Passband Ripple

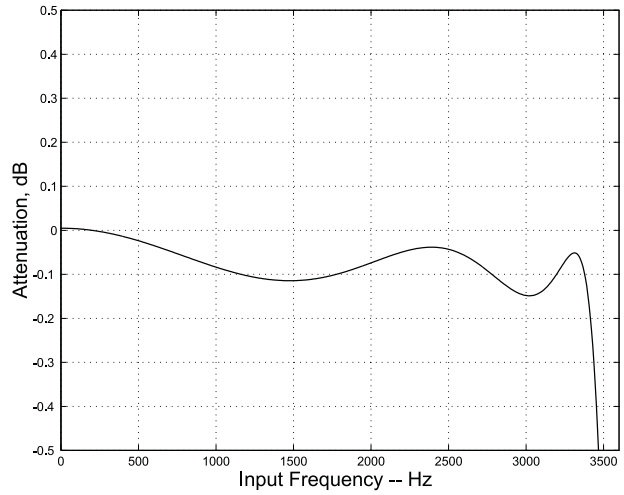


Figure 12. IIR Receive Filter Passband Ripple

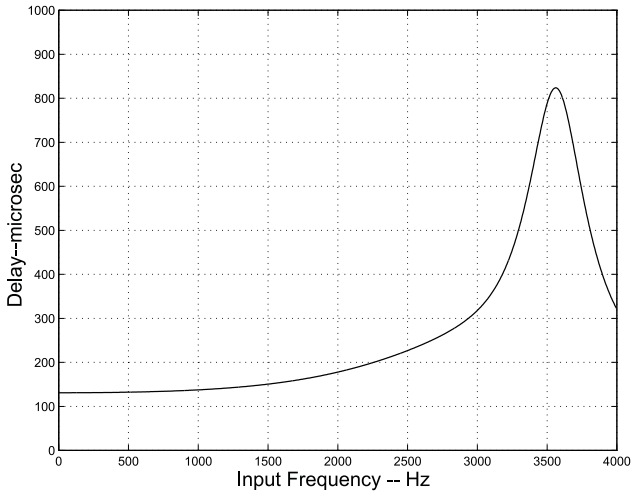


Figure 15. IIR Receive Group Delay

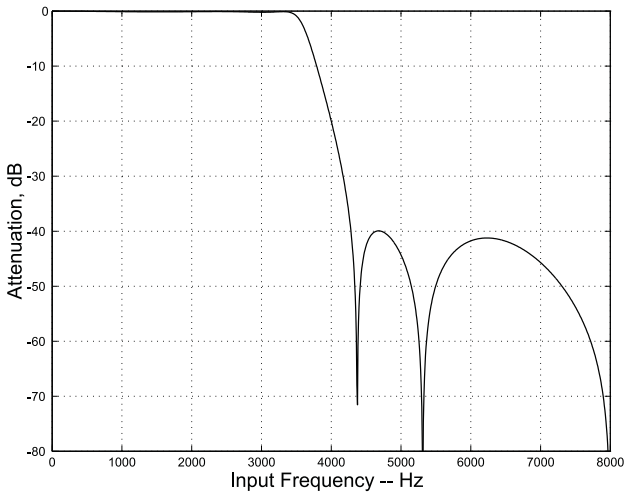


Figure 13. IIR Transmit Filter Response

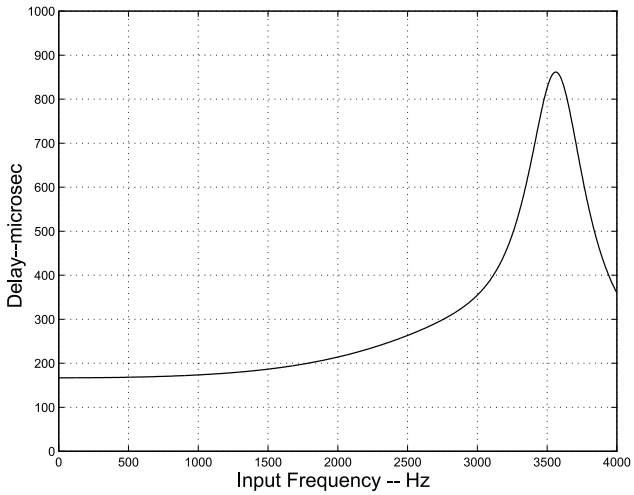


Figure 16. IIR Transmit Group Delay

2. Typical Application Schematic

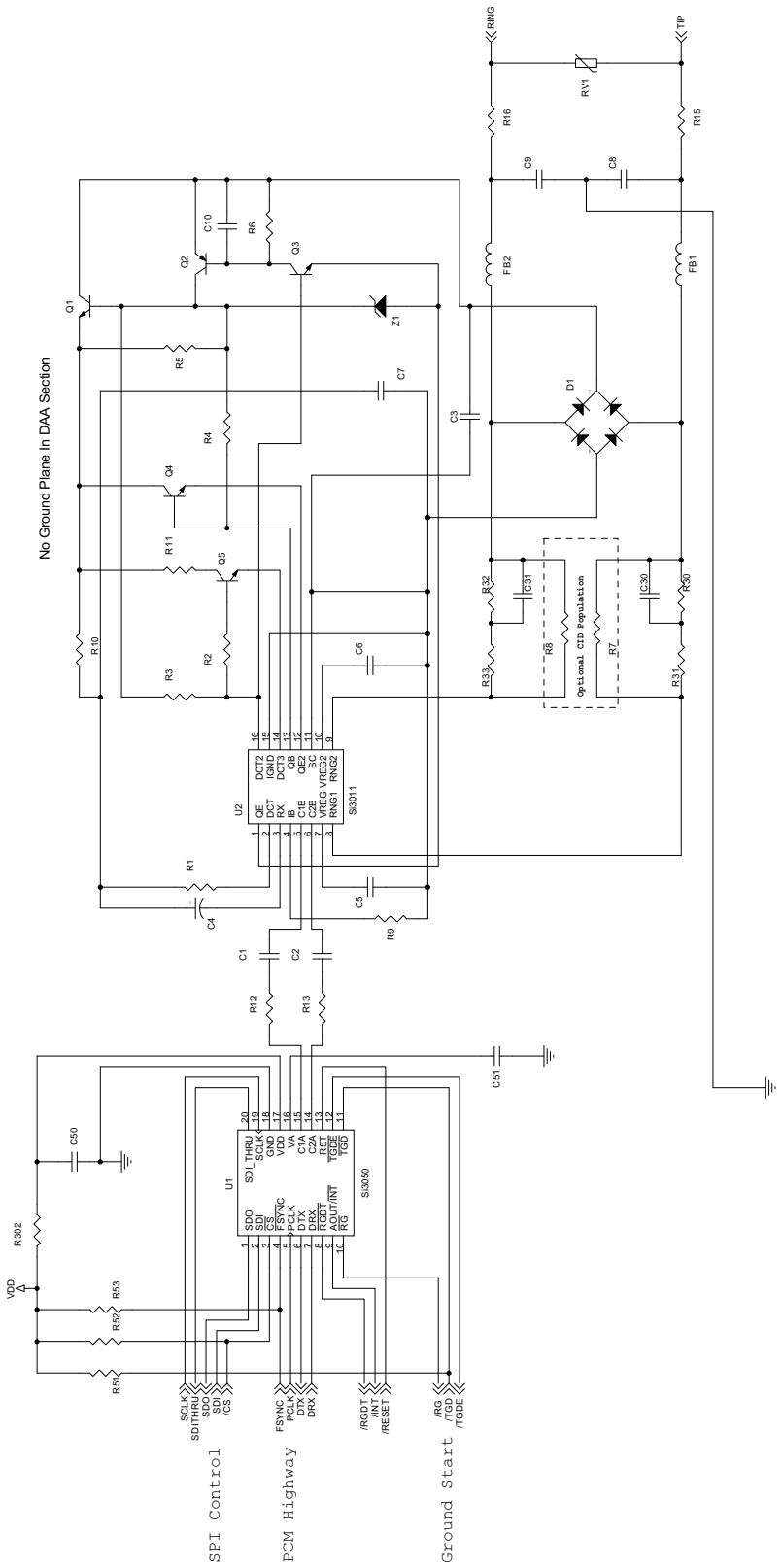


Figure 17. Typical Application Circuit for the Si3050 and Si3011
(Refer to "AN67: Si3050/52/54/56 Layout Guidelines" for Recommended Layout Guidelines)

3. Bill of Materials

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3[1]	3.9 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C51	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 µF, 16 V, X7R, ±20%	Venkel, SMEC
C30, C31[1]	120 pF, 250 V, X7R, ±10%	Venkel, SMEC
D1, D2[2]	Dual Diode, 225 mA, 300 V, (CMPD2004S)	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM18AG601SN1	Murata
Q1, Q3	NPN, 300 V, MMBTA42	Central OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	Central OnSemi, Fairchild
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	Central OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Diodes Inc., Shindengen
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8[1]	Not Installed, 20 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonic
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13[3]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R15, R16[4]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R30, R32[1]	15 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R31, R33[1]	5.1 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R51, R52, R53	4.7 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
U1	Si3050	Silicon Labs
U2	Si3011	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W	General Semi, On Semi, Diodes Inc.

Notes:

1. R7–R8 may be substituted for R30–R33 and C30–C31 for lower cost, but reduced CID performance.
2. Several diode bridge configurations are acceptable. Parts, such as a single HD04, a DF-04S, or four 1N4004 diodes, may be used (suppliers include General Semiconductor, Diodes Inc., etc.).
3. 56 Ω, 1/16, 1% resistors may be substituted for R12–R13 (0 Ω) to decrease emissions. (See AN81.)
4. Murata BLM18AG601SN1 may be substituted for R15–R16 (0 Ω) to decrease emissions. (See AN81.)

4. AOUT PWM Output

Figure 18 illustrates an optional circuit to support the pulse width modulation (PWM) output capability of the Si3050 for call progress monitoring purposes.To enable this mode, the INTE bit (Register 2) should be set to 0, the PWME bit (Register 1) set to 1, and the PWMM bits (Register 2) set to 00.

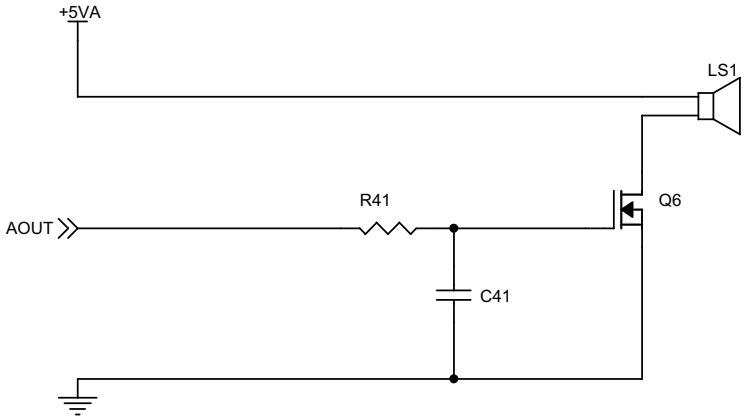


Figure 18. AOUT PWM Circuit for Call Progress

Table 12. Component Values—AOUT PWM

Component	Value	Supplier
LS1	Speaker BRT1209PF-06	Intervox
Q6	NPN KSP13	Fairchild
C41	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
R41	150 Ω, 1/10 W, ±5%	Venkel, SMEC, Panasonic

Registers 20 and 21 allow the receive and transmit paths to be attenuated linearly. When these registers are set to all 0s, the transmit and receive paths are muted. These registers affect the call progress output only and do not affect transmit and receive operations on the telephone line.

The PWMM[1:0] bits (Register 1, bits 5:4) select one of three different PWM output modes for the AOUT signal, including a delta-sigma data stream, a 32 kHz return to 0 PWM output, and a balanced 32 kHz PWM output.

5. Functional Description

The Si3050 is an integrated direct access arrangement (DAA) providing a programmable line interface that meets global telephone line requirements. The Si3050 implements Silicon Laboratories' patented isolation capacitor technology, which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with two highly-integrated ICs.

The Si3050+Si3011 chipset is software programmable and designed to meet FCC and TBR21 specifications. In addition, the Si3050 meets the most stringent global requirements for out-of-band energy, emissions, immunity, high-voltage surges, and safety, including FCC Parts 15 and 68, EN55022, EN55024, and many other standards.

5.1. Line-Side Device Support

Three different line-side devices are available for use with the Si3050 system-side device. This data sheet covers the Si3011, which has been optimized for TBR21 and FCC-compliant countries. For information on a globally-compliant solution, refer to the Si3050-Si3018/19 data sheet.

5.2. Power Supplies

The Si3050 operates from a 3.3 V power supply. The Si3050 input pins can only accept 3.3 V CMOS signal levels. If support of 5 V signal levels is necessary, a level shifter is required. The Si3011 derives its power from two sources: the Si3050 and the telephone line. The Si3050 supplies power over the patented isolation capacitor link between the two devices, allowing the Si3011 to communicate with the Si3050 while on-hook and perform other on-hook functions, such as line voltage monitoring. When off-hook, the Si3011 also derives power from the line current supplied from the telephone line. This feature is exclusive to DAAs from Silicon Labs and allows the most cost-effective implementation for a DAA while still maintaining robust performance over all line conditions.

5.3. Initialization

Each time the Si3050 is powered up, assert the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is deasserted, the registers have default values to guarantee the line-side device (Si3011) is powered down without the possibility of loading the line (i.e., off-hook). An example initialization procedure follows:

1. Power up and de-assert $\overline{\text{RESET}}$.
2. Wait until the PLL is locked. This time is less than 1 ms from the application of PCLK.
3. Enable PCM (Register 33) or GCI (Register 42) mode.
4. Set the desired line interface parameters (i.e., ILIM, DCR, ACIM, OHS2, TGA2, and TXG2[3:0]).
5. Set the FULL2 and IIRE bits as required.
6. Write a 0x00 into Register 6 to power up the line-side device.

When this procedure is complete, the Si3011 is ready for ring detection and off-hook operation.

5.4. Isolation Barrier

The Si3050 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' patented signal processing techniques. Differential capacitive communication eliminates signal degradation from capacitor mismatches, common mode interference, or noise coupling. As shown in the "2. Typical Application Schematic" on page 17, the C1, C2, C8, and C9 capacitors isolate the Si3050 (system-side) from the Si3011 (line-side). Transmit, receive, control, ring detect, and caller ID data are passed across this barrier.

The communications link is disabled by default. To enable it, the PDL bit (Register 6, bit 4) must be cleared. No communication between the Si3050 and Si3011 can occur until this bit is cleared. Allow the PLL to lock to the PCLK and FSYNC input signals before clearing the PDL bit.

5.5. Power Management

The Si3050 supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full powerdown mode. The power management modes are controlled by the PDN and PDL bits (Register 6).

On powerup, or following a reset, the Si3050 is in reset operation. The PDL bit is set, and the PDN bit is cleared. The Si3050 is operational, except for the communications link. No communication between the Si3050 and line-side device (Si3011) can occur during reset operation. Bits associated with the line-side device are invalid in this mode.

In typical applications, the DAA will predominantly be operated in normal mode. In normal mode, the PDL and PDN bits are cleared. The DAA is operational and the communications link passes information between the Si3050 and the Si3011.

The Si3050 supports a low-power sleep mode that supports ring validation and wake-up-on-ring features. To enable the sleep mode, the PDN bit must be set.

When the Si3050 is in sleep mode, the PCLK signal must remain active. In low-power sleep mode, the Si3050 is non-functional except for the communications link and the RGDT signal. To take the Si3050 out of sleep mode, pulse the reset pin (RESET) low.

In summary, the powerdown/up sequence for sleep mode is as follows:

1. Ensure the PDL bit (Register 6, bit 4) is cleared.
2. Set the PDN bit (Register 6, bit 3).
3. The device is now in sleep mode. PCLK must remain active.
4. To exit sleep mode, reset the Si3050 by pulsing the RESET pin.
5. Program registers to desired settings.

The Si3050 also supports an additional Powerdown mode. When both the PDN (Register 6, bit 3) and PDL (Register 6, bit 4) bits are set, the chipset enters a complete powerdown mode and draws negligible current (deep sleep mode). In this mode, the Si3050 is non-functional. The RGDT pin does not function and the Si3050 will not detect a ring. Normal operation can be restored using the same process for taking the Si3050 out of sleep mode.

5.6. Calibration

The Si3050 initiates two auto-calibrations by default when the device goes off-hook or experiences a loss of line power. A 17 ms resistor calibration is performed to allow circuitry internal to the DAA to adjust to the exact line conditions present at the time of going off-hook. This resistor calibration can be disabled by setting the RCALD bit (Register 25, bit 5). A 256 ms ADC calibration is also performed to remove offsets that might be present in the on-chip A/D converter, which could affect the A/D dynamic range. The ADC auto-calibration is initiated after the DAA dc termination stabilizes and the resistor calibration completes. Due to the large variation in line conditions and line card behavior presented to the DAA, it might be beneficial to use manual ADC calibration instead of auto-calibration.

Manual ADC calibration should be executed as close as possible to 256 ms before valid transmit/receive data is expected.

The following steps should be taken to implement manual ADC calibration:

1. The CALD bit (auto-calibration disable—Register 17) must be set to 1.
2. The MCAL bit (manual calibration) must be toggled to one and then 0 to begin and complete the calibration.
3. The calibration is completed in 256 ms.

5.7. In-Circuit Testing

The Si3050's advanced design provides the designer with an increased ability to determine system functionality during production line tests and support for end-user diagnostics. Six loopback modes allow increased coverage of system components. For four of the test modes, a line-side power source is needed. While a standard phone line can be used, the test circuit in Figure 1 on page 6 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side device.

For the start-up loopback test mode, no line-side power is necessary, and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Register 6, bit 4) is set (the default case), the line side is in a powerdown mode, and the system-side is in a digital loopback mode. In this mode, data received on DRX passes through the internal filters and is transmitted on DTX. This path introduces approximately 0.9 dB of attenuation on the DRX signal received. The group delay of both transmit and receive filters exists between DRX and DTX. Clearing the PDL bit disables this mode, and the DTX data switches to the receive data from the line side. When the PDL bit is cleared, the FDT bit (Register 12, bit 6) becomes active to indicate that successful communication between the line side and system side is established. This provides verification that the communications link is operational.

The digital data loop-back mode offers a way to input data on the DRX pin and have the identical data output on the DTX pin through bypassing the transmit and receive filters. Setting the DDL bit (Register 10, bit 0) enables this mode, which provides an easy way to verify communication between the host processor/DSP and the DAA. No line-side power or off-hook sequence is required for this mode.

The remaining test modes require an off-hook sequence to operate. The following sequence lists the off-hook requirements:

1. Powerup or reset.
2. Allow the internal PLL to lock on PCLK and FSYNC.
3. Enable line-side by clearing PDL bit.
4. Issue an off-hook command.
5. Delay 402.75 ms for calibration to occur.
6. Set desired test mode.

The communications link digital loopback mode allows the host processor to provide a digital input test pattern on DRX and receive that digital test pattern back on DTX. To enable this mode, set the IDL bit (Register 1, bit 1). The communications link is tested in this mode. The digital stream is delivered across the isolation capacitors, C1 and C2, of the "2. Typical Application

Schematic" on page 17, to the line-side device and returned across the same path. In this digital loopback mode, the 0.9 dB attenuation and filter group delays also exist.

The PCM analog loopback mode extends the signal path of the analog loopback mode. In this mode, an analog signal is driven from the line into the line-side device. This analog signal is converted to digital data and then passed across the communications link to the system-side device. The data passes through the receive filter, through the transmit filter, and is then passed across the communications link and sent back out onto the line as an analog signal. Set the PCML bit (Register 33, bit 7) to enable this mode.

With the final testing mode, internal analog loopback, the system can test the operation of the transmit and receive paths on the line-side device and the external components in the "2. Typical Application Schematic" on page 17. The host provides a digital test waveform on DRX. Data passes across the isolation barrier, is transmitted to and received from the line, passes back across the isolation barrier, and is presented to the host on DTX. Clear the HBE bit (Register 2, bit 1) to enable this mode.

When the HBE bit is cleared, it produces a dc offset that affects the signal swing of the transmit signal. Silicon Laboratories recommends that the transmit signal be 12 dB lower than normal transmit levels. A lower level eliminates clipping from the dc offset that results from disabling the hybrid. It is assumed in this test that the line ac impedance is nominally 600 Ω.

Note: All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

5.8. Exception Handling

The Si3050 can determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling DSP can read several status bits. The bit of highest importance is the frame detect bit (FDT, Register 12, bit 6) which indicates that the system-side (Si3050) and line-side (Si3011) devices are communicating. During normal operation, the FDT bit can be checked before reading the bits that indicate information about the line side. If FDT is not set, the following bits related to the line side are invalid—RDT, RDTN, RDTP, LCS[4:0], LSID[1:0], REVB[3:0], LVS[7:0], LCS2[7:0], ROV, BTD, DOD, and OVL; the RGDT operation is also non-functional.

Following powerup and reset, the FDT bit is not set because the PDL bit (Register 6 bit 4) defaults to 1. In this state, the ISOcap is not operating and no information about the line side can be determined. The user must provide a valid PCLK and FSYNC to the system and clear the PDL bit to activate the ISOcap link. Communication with the line-side device takes less than 10 ms to establish.

5.9. Revision Identification

The Si3050 provides information to determine the revision of the Si3050 and/or the Si3011. The REVA[3:0] bits (Register 11) identify the revision of the Si3050, where 0101b denotes revision E. The REVB[3:0] bits (Register 13) identify the revision of the line-side device, where 0110b denotes revision F.

5.10. Transmit/Receive Full-Scale Level

The Si3050 supports programmable maximum transmit and receive levels. The default signal level supported by the Si3050 is 0 dBm into a 600 Ω load. The Si3050+Si3011 chipset supports an enhanced full-scale mode that can be enabled by setting the FULL2 bit in Register 30. With FULL2 = 1, the full-scale signal level increases to +6.0 dBm into a 600 Ω load or 1.5 dBV into all reference impedances. The full-scale and enhanced full-scale modes provide the ability to trade off TX power and TX distortion for a peak signal. By using the programmable digital gain registers in conjunction with the enhanced full-scale signal level mode, a specific power level (+3.2 dBm for example) can be achieved across all ACT settings.

5.11. Parallel Handset Detection

The Si3050 can detect a parallel handset going off-hook. When the Si3050 is off-hook, the loop current can be monitored with the LCS or LCS2 bits. A significant drop in loop current signals a parallel handset going off-hook. If a parallel handset going off-hook causes the loop current to drop to 0, the LCS and LCS2 bits will read all 0s. Additionally, the Drop-Out Detect (DOD) bit will fire (and generate an interrupt if the DODM bit is set) indicating that the line-derived power supply has collapsed.

The LVS bits also can be read when on- or off-hook to determine the line voltage. Significant drops in line voltage can signal a parallel handset. For the Si3050 to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination to support two off-hook DAAs on the same line. Improved parallel handset operation can be achieved by changing the dc impedance from 50 Ω to 800 Ω.

5.12. Line Voltage/Loop Current Sensing

The 5-bit LCS[4:0] register reports loop current measurements when off-hook. An additional register is available to report loop current to a finer resolution (LCS2[7:0]). The LVS[7:0] register can be read when the chipset is on or off hook. These registers can be used to help determine the following line conditions:

- When on-hook, detect if a line is connected.
- When on-hook, detect if a parallel phone is off-hook.
- When off-hook, detect if a parallel phone goes on or off-hook.
- Detect if enough loop current is available to operate.
- When used in conjunction with the OPD bit, detect if an overload condition exists. (See "5.26. Overload Detection" on page 31.)

5.12.1. Line Voltage Measurement

The Si3050 reports line voltage with the LVS[7:0] bits (Register 29) in both on- and off-hook states with a resolution of 1 V per bit. The accuracy of these bits is approximately ±10%. Bits 0 through 7 of this 8-bit signed number indicate the value of the line voltage in 2s complement format. Bit 7 indicates the polarity of the TIP/RING voltage.

If the INTE bit (Register 2, bit 7) and the POLM bit (Register 3, bit 0) are set, a hardware interrupt is generated on the AOUT/$\overline{\text{INT}}$ pin when Bit 7 of the LVS register changes state. The edge-triggered interrupt is cleared by writing 0 to the POLI bit (Register 4, bit 0). The POLI bit is set each time bit 7 of the LVS register changes state, and must be written to 0 to clear it. The default state of the LVS register forces the LVS[7:0] bits to 0 when the line voltage is 3 V or less. The LVFD bit (Register 31, bit 0) disables this force-to-zero function and allows the LVS register to display non-zero values of 3 V and below. This register may display unpredictable values at line voltages between 0 to 2 V. At 0 V, the LVS register displays all 0s.

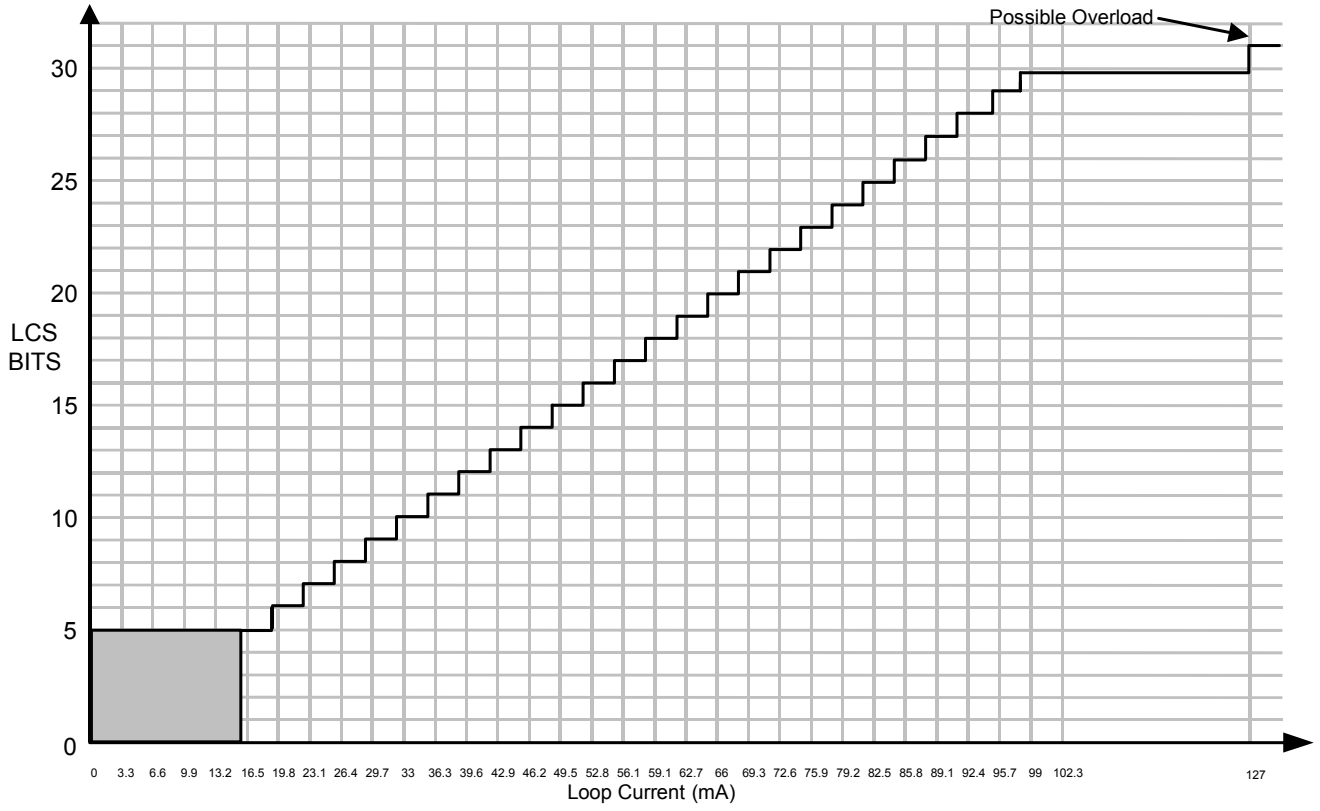


Figure 19. Typical Loop Current LCS Transfer Function (ILIM = 0)

5.12.2. Loop Current Measurement

When the Si3050 is off-hook, the LCS[4:0] bits measure loop current in 3.3 mA/bit resolution. With the LCS[4:0] bits, a user can detect another phone going off-hook by monitoring the dc loop current. The line current sense transfer function is shown in Figure 19 and is detailed in Table 13. The LCS and LCS2 bits report loop current down to the minimum operating loop current for the DAA. Below this threshold, the reported value of loop current is unpredictable. The minimum operating loop current of the Si3050+Si3011 chipset is 10 mA.

When the LCS bits reach max value, the Loop Current Sense Overload Interrupt bit (Register 4) fires. LCSOI firing however, does not necessarily imply that an overcurrent situation has occurred. An overcurrent situation in the DAA is determined by the status of the OPD bit (Register 19). After the LCSOI interrupt fires, the OPD bit should be checked to determine if an overcurrent situation exists. The OPD bit indicates an overcurrent situation when loop current exceeds either 160 mA (ILIM = 0) or 60 mA (ILIM = 1), depending on the setting of the ILIM bit (Register 26).

Table 13. Loop Current Transfer Function

LCS[4:0]	Condition
00000	Insufficient line current for normal operation. Use the DOD bit (Register 19, bit 1) to determine if a line is still connected.
00100	Minimum line current for normal operation.
11111	Loop current may be excessive. Use the OPD bit to determine if an overload condition exists.

The LCS2 register also reports loop current in the off-hook state. This register has a resolution of 1.1 mA per bit.

5.13. Off-Hook

The communication system generates an off-hook command by setting the OH bit (Register 5, bit 0). This off-hook state seizes the line for incoming/outgoing calls. It also can be used for pulse dialing.

With the OH bit at logic 0, negligible dc current flows through the hookswitch. When a logic 1 is written to the OH bit, the hookswitch transistor pair, Q1 and Q2, turn on. A termination impedance across TIP and RING is applied and causes dc loop current to flow. The termination impedance has both an ac and a dc component.

Several events occur in the DAA when the OH bit is set. There is a 250 µs latency for the off-hook command to be communicated to the line-side device. When the line-side device goes off-hook, an off-hook counter forces a delay to allow line transients to settle before transmission or reception can occur. The off-hook counter time is controlled by the FOH[1:0] bits (Register 31, bits 6:5). The default setting for the off-hook counter time is 128 ms, but can be adjusted up to 512 ms or down to 64 or 8 ms.

After the off-hook counter expires, a resistor calibration is performed for 17 ms to allow the DAA internal circuitry to adjust to the exact conditions present at the time of going off-hook. This resistor calibration can be disabled by setting the RCALD bit (Register 25, bit 5).

After the resistor calibration is performed, an ADC calibration is performed for 256 ms. This calibration helps to remove offset in the A/D sampling the telephone line. ADC calibration can be disabled by setting the CALD bit (Register 17, bit 5). See "5.6. Calibration" on page 21 for more information on automatic and manual calibration.

Silicon Laboratories recommends that the resistor and the ADC calibrations not be disabled except when a fast response is needed after going off-hook, such as when responding to a Type II Caller-ID signal. See "5.25. Caller ID" on page 29 for detailed information.

To calculate the total time required to go off-hook and start transmission or reception, include the digital filter delay (typically 1.5 ms with the FIR filter) in the calculation.

5.14. Ground Start Support

The Si3050 DAA supports loop-start applications by default. It can also support ground-start applications with the RG, TGD, and TGDE pins and the schematic shown in Figure 20. The component values are listed in Table 14.

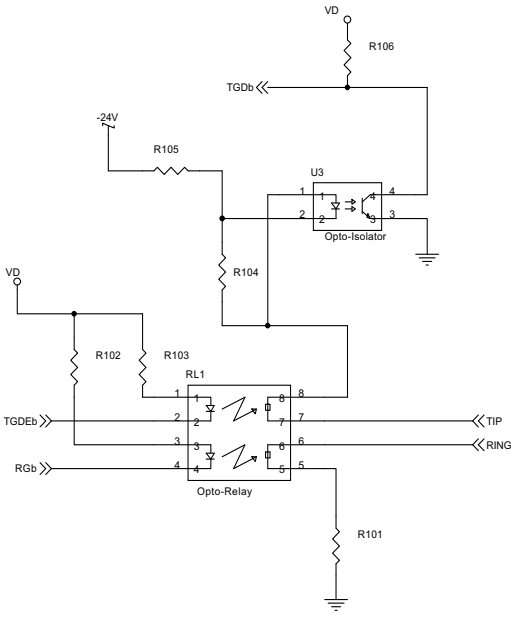


Figure 20. Typical Application Circuit for Ground Start Support on the SI3050

Table 14. Component Values for the Ground Start Support Schematic

Symbol	Value	Supplier(s)
R101	200 Ω, 2 W, ±5%	Venkel, SMEC, Panasonic
R102, R103, R106	1 kΩ, 1/10 W, ±5%	Venkel, SMEC, Panasonic
R104	1.5 kΩ, 1/10 W, ±5%	Venkel, SMEC, Panasonic
R105	10 kΩ, 1/2 W, ±5%	Venkel, SMEC, Panasonic
RL1	AQW210S	Aromat, NEC
U3	PS2501L-1	NEC, Fairchild

5.14.1. Ground Start Idle

Ensure the relay in series with TIP is closed by clearing the TGOE bit (Register 32, bit 1). This enables the DAA to sense if the CO grounds TIP. Set RG to 1 (Register 32, bit 0) so that no current flows through the relay connecting RING to ground.

5.14.2. DAA Requests Line Seizure

With TGOE set to zero, seize the line by closing the relay in series with RING (clear the RG bit, Register 32, bit 0). The CO detects this current flowing on RING and grounds TIP. This sets the TGD bit (Register 32, bit 2). The DAA may then be taken off-hook and the relay in series with RING opened (clear the RG bit). The call continues as in loop-start mode.

5.14.3. CO Requests Line Seizure

In a normal on-hook state, the relay in series with TIP should be closed, connecting the –24 V isolated supply. The CO grounds TIP to request line seizure, causing current to flow. The opto-isolator U3 (see Figure 20 on page 25) detects this current and sets the TGD bit (Register 32, bit 2). This bit remains high as long as current is detected. The TGDI bit (Register 4, bit 1) is a sticky bit, and remains high until cleared. A hardware interrupt on the AOUT/$\overline{\text{INT}}$ can be made to occur when TIP current begins to flow by enabling the TGDM bit (Register 3, bit 1). Clear the interrupt by writing 0 to the TGDI bit (Register 4 bit 1). The DAA may then be taken off-hook and the call continued as in loop-start mode.

5.15. Interrupts

The AOUT/$\overline{\text{INT}}$ pin can be used as a hardware interrupt pin by setting the INTE bit (Register 2, bit 7). When this bit is set, the analog output used for call progress monitoring is not available. The default state of this interrupt output pin is active low, but active high operation can be enabled by setting the INTP bit (Register 2, bit 6). This pin is an open-drain output when the INTE bit is set and requires a 4.7 kΩ pullup or pulldown for correct operation. If multiple $\overline{\text{INT}}$ pins are connected to a single input, the combined pullup or pulldown resistance should equal 4.7 kΩ. Bits 7–0 in Register 3 and bit 1 in Register 44 can be set to enable hardware interrupt sources. When one or more of these bits is set, the AOUT/$\overline{\text{INT}}$ pin goes into an active state and stays active until the interrupts are serviced. If more than one hardware interrupt is enabled in Register 3, use software polling to determine the cause of the interrupts. Register 4 and bit 3 of Register 44 contain sticky interrupt flag bits. Clear these bits after servicing the interrupt.

Registers 43 and 44 contain the line current/voltage threshold interrupt. This interrupt is triggered when the measured line voltage or current in the LVS or LCS2 registers, as selected by the CVS bit (Register 44, bit 2), crosses the threshold programmed into the CVT[7:0] bits. With the CVP bit, the interrupt can be programmed to occur when the measured value rises above or falls below the threshold. Only the magnitude of the measured value is used for comparison to the threshold programmed into the CVT[7:0] bits. Therefore, only positive numbers should be used as a threshold.

5.16. DC Termination

The Si3050+Si3011 chipset has programmable settings for the dc impedance and current limit. The dc impedance of the DAA is normally represented with a 50 Ω slope as shown in Figure 21, but can be changed to an 800 Ω slope by setting the DCR bit. This higher dc termination presents a higher resistance to the line as loop current increases.

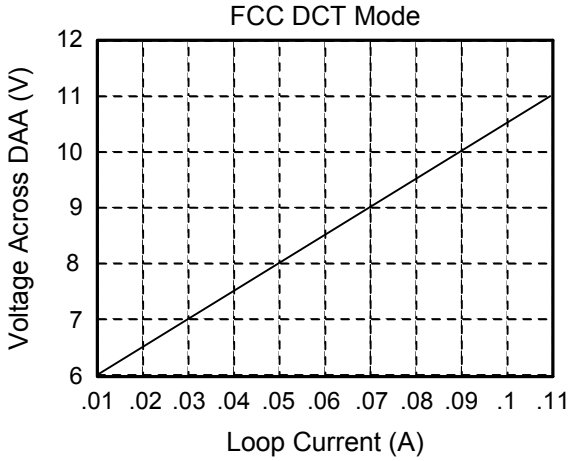


Figure 21. FCC Mode I/V Characteristics

For applications requiring current limiting per the TBR21 standard, the ILIM bit may be set to select this mode. In this mode, the dc I/V curve is changed to a 2000 Ω slope above 40 mA, as shown in Figure 22. This allows the DAA to operate with a 50 V, 230 Ω feed, which is the maximum linefeed specified in the TBR21 standard.

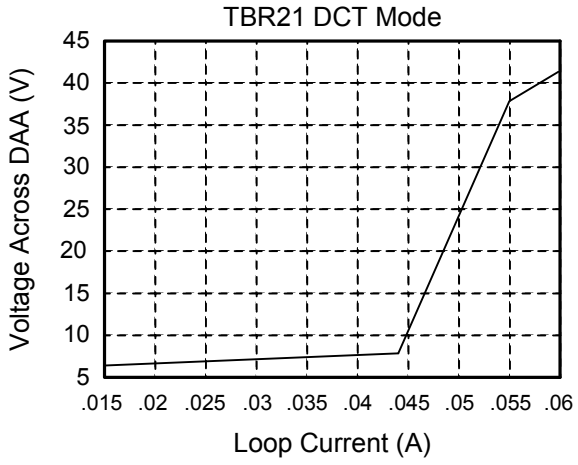


Figure 22. TBR21 Mode I/V Characteristics

5.17. AC Termination

The Si3050+Si3011 chipset provides two ac termination impedances. The ACIM bit in Register 30 is used to select the ac impedance setting. The two available settings for the Si3050+Si3011 chipset are listed in Table 15. The programmable digital hybrid can be used to further reduce near-end echo for each of the four listed ac termination settings. See "5.28. Transhybrid Balance" on page 32 for details.

Table 15. AC Termination Settings

ACIM	AC Termination
0	600 Ω
1	210 Ω + (750 Ω || 150 nF) and 275 Ω + (780 Ω || 150 nF)

5.18. Ring Detection

The ring signal is resistively coupled from TIP and RING to the RNG1 and RNG2 pins. The Si3050 supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal of the ring signal. See “5.25.Caller ID” on page 29. The ring detection threshold is programmable with the RT2 bit (Register 17, bit 4). The ring detector output can be monitored in three ways. The first method uses the $\overline{\text{RGDT}}$ pin. The second method uses the register bits, RDTP, RDTN, and RDT (Register 5). The final method uses the DTX output.

The ring detector mode is controlled by the RFWE bit (Register 18, bit 1). When the RFWE bit is 0 (default mode), the ring detector operates in half-wave rectifier mode. In this mode, only positive ring signals are detected. A positive ring signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. Conversely, a negative ring signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2. When the RFWE bit is 1, the ring detector operates in full-wave rectifier mode. In this mode, both positive and negative ring signals are detected.

The first method to monitor ring detection output uses the $\overline{\text{RGDT}}$ pin. When the $\overline{\text{RGDT}}$ pin is used, it defaults to active low, but can be changed to active high by setting the RPOL bit (Register 14, bit 1). This pin is an open-drain output, and requires a 4.7 kΩ pullup or pulldown for correct operation. If multiple $\overline{\text{RGDT}}$ pins are connected to a single input, the combined pullup or pulldown resistance should equal 4.7 kΩ.

When the RFWE bit is 0, the $\overline{\text{RGDT}}$ pin is asserted when the ring signal is positive, which results in an output signal frequency equal to the actual ring frequency. When the RFWE bit is 1, the $\overline{\text{RGDT}}$ pin is asserted when the ring signal is positive or negative.

The output then appears to be twice the frequency of the ring waveform.

The second method to monitor ring detection uses the ring detect bits (RDTP, RDTN, and RDT). The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. When the signal on RNG1-RNG2 is above the positive ring threshold, the RDTP bit is set. When the signal on RNG1-RNG2 is below the negative ring threshold, the RDTN bit is set. When the signal on RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFWE bit is 0, a positive ring signal sets the RDT bit for a period of time. When the RFWE bit is 1, a positive or negative ring signal sets the RDT bit.

The RDT bit acts like a one shot. When a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter reaching 0, then the RDT bit clears. The length of this count is approximately 5 seconds. The RDT bit is reset to 0 by an off-hook event. If the RDTM bit (Register 3, bit 7) is set, a hardware interrupt occurs on the AOUT/INT pin when RDT is triggered. This interrupt can be cleared by writing to the RDTI bit (Register 4, bit 7). When the RDI bit (Register 2, bit 2) is set, an interrupt occurs on both the beginning and end of the ring pulse as defined by the RTO bits (Register 23, bits 6:3). Ring validation may be enabled when using the RDI bit.

The third method to monitor detection uses the DTX data samples to transmit ring data. If the ISOcap is active (PDL=0) and the device is not off-hook or in on-hook line monitor mode, the ring data is presented on DTX. The waveform on DTX depends on the state of the RFWE bit.

When RFWE is 0, DTX is –32768 (0x8000) while the RNG1-RNG2 voltage is between the thresholds. When a ring is detected, DTX transitions to +32767 when the ring signal is positive, then goes back to –32768 when the ring is near 0 and negative. Thus a near square wave is presented on DTX that swings from –32768 to +32767 in cadence with the ring signal.

When RFWE is 1, DTX sits at approximately +1228 while the RNG1-RNG2 voltage is between the thresholds. When the ring becomes positive, DTX transitions to +32767. When the ring signal goes near 0, DTX remains near 1228. As the ring becomes negative, the DTX transitions to –32768. This repeats in cadence with the ring signal.

To observe the ring signal on DTX, watch the MSB of the data. The MSB toggles at the same frequency as the ring signal independent of the ring detector mode. This method is adequate for determining the ring frequency.

5.19. Ring Validation

Ring validation prevents false triggering of a ring detection by validating the ring parameters. Invalid signals, such as a line-voltage change when a parallel handset goes off-hook, pulse dialing, or a high-voltage line test are ignored. Ring validation can be enabled during normal operation and in low-power sleep mode when a valid external PCLK signal is supplied.

The ring validation circuit operates by calculating the time between alternating crossings of positive and negative ring thresholds to validate that the ring frequency is within tolerance. High and low frequency tolerances are programmable in the RAS[5:0] and RMX[5:0] fields. The RCC[2:0] bits define how long the ring signal must be within tolerance.

Once the duration of the ring frequency is validated by the RCC bits, the circuitry stops checking for frequency tolerance and begins checking for the end of the ring signal, which is defined by a lack of additional threshold crossings for a period of time configured by the RTO[3:0] bits. When the ring frequency is first validated, a timer defined by the RDLY[2:0] bits is started. If the RDLY[2:0] timer expires before the ring timeout, then the ring is validated and a valid ring is indicated. If the ring timeout expires before the RDLY[2:0] timer, a valid ring is not indicated.

Ring validation requires the following five parameters:

- Timeout parameter to place a lower limit on the frequency of the ring signal (the RAS[5:0] bits in Register 24). The frequency is measured by calculating the time between crossings of positive and negative ring thresholds.
- Minimum count to place an upper limit on the frequency (the RMX[5:0] bits in Register 22).
- Time interval over which the ring signal must be the correct frequency (the RCC[2:0] bits in Register 23).
- Timeout period that defines when the ring pulse has ended based on the most recent ring threshold crossing.
- Delay period between when the ring signal is validated and when a valid ring signal is indicated to accommodate distinctive ringing.

The RNGV bit (Register 24, bit 7) enables or disables the ring validation feature in both normal operating mode and low-power sleep mode.

Ring validation affects the behavior of the RDT status bit, the RDTI interrupt, the $\overline{\text{INT}}$ pin, and the $\overline{\text{RGDT}}$ pin.

1. When ring validation is enabled, the status bit seen in the RDT read-only bit (r5.2), represents the detected envelope of the ring. The ring validation parameters are configurable so that this envelope may remain high throughout a distinctive-ring sequence.
2. The RDTI interrupt fires when a validated ring occurs. If RDI is zero (default), the interrupt occurs on the rising edge of RDT. If RDI is set, the interrupt occurs on both rising and falling edges of RDT.
3. The $\overline{\text{INT}}$ pin follows the RDTI bit with configurable polarity.
4. The RGDT pin can be configured to follow the ringing signal envelope detected by the ring validation circuit by setting RFWE to 0. If RFWE is set to 1, the RGDT pin follows an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately 5 seconds. (This information is shown in Register 18).

5.20. Ringer Impedance

The ring detector in a typical DAA is ac coupled to the line with a large 1 µF, 250 V decoupling capacitor. The ring detector on the Si3011 is resistively coupled to the line. This coupling produces a high ringer impedance to the line of approximately 20 MΩ to meet FCC and TBR21 specifications.

5.21. Pulse Dialing

Pulse dialing is accomplished by going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have strict specifications for pulse fidelity including make and break times, make resistance, and rise and fall times. In a traditional, solid-state dc holding circuit, there are a number of issues in meeting these requirements.

The Si3050 dc holding circuit has active control of the on- and off-hook transients to maintain pulse dialing fidelity.

To ensure proper operation of the DAA during pulse dialing, disable the automatic resistor calibration that is performed each time the DAA enters the off-hook state by setting the RCALD bit (Register 25, bit 5).

5.22. Receive Overload Detection

The Voice DAA chipset is capable of monitoring and reporting receive overload conditions on the line. Billing tones, parallel phone off-hook events, polarity reversals and other disturbances on the line may trigger multiple levels of overload detection as described below.

Transient events less than 1.1 V_{PK} on the line are filtered out by the low-pass digital filter on the Si3050+Si3011 chipset. The ROV and ROVI bits are set when the received signal is greater than 1.1 V_{PK}. Both bits will continue to indicate an overload condition until a zero is written to clear. The OVL mirrors the function of the ROV and ROVI bits but it automatically clears after the overload condition has been removed. When the OVL bit returns to 0, the DAA initiates an auto-calibration sequence that must complete before data can be transmitted. An external interrupt can optionally be triggered by the ROVI bit by setting the ROVM and INTE bits.

Certain events such as billing tones can be sufficiently large to disrupt the line-derived power supply of the Voice DAA line side device. To ensure that the device maintains the off-hook line state during these events, the BTE bit should be set. If such an event occurs while the BTE bit is set, the BTD and BTDI bits will be asserted. A zero must be written to the BTE bit to clear the BTD and BTDI bits. An external interrupt can optionally be triggered by the BTDI bit by setting the BTDM and INTE bits.

In the event that a line disturbance causes the loop current to collapse below the minimum required operating current of the Voice DAA, the DOD and DODI bits will be set. An external interrupt can optionally be triggered by the DODI bit by setting the DODM and INTE bits.

5.23. Billing Tone Filter (Optional)

Optionally, a billing tone filter may be inserted between the line and the voice DAA to minimize disruptions caused by large billing tones. The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are expensive and few countries utilize billing tones, this filter is typically placed in an external dongle or added as a population option. Figure 23 shows a billing tone filter example. Table 16 gives the component values.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 kHz and 16 kHz.

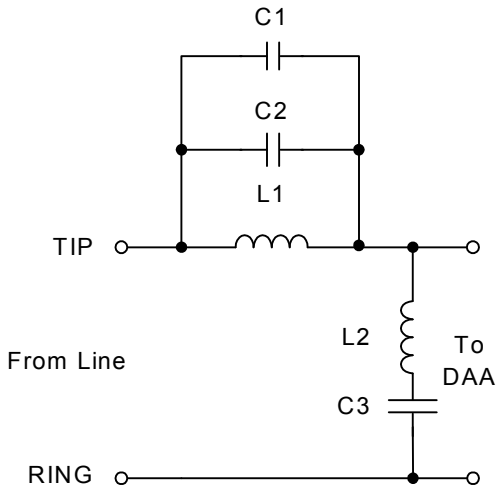


Figure 23. Billing Tone Filter

Table 16. Component Values—Optional Billing Tone Filters

Component	Value
C1,C2	0.027 µF, 50 V, ±10%
C3	0.01 µF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 Ω, ±10%
L2	10 mH, >40 mA, <10 Ω, ±10%

The billing tone filter affects the DAA's ac termination and return loss.

5.24. On-Hook Line Monitor

The on-hook line monitor mode allows the Si3050 to receive line activity when in an on-hook state. This mode is typically used to detect caller ID data (see "5.25.Caller ID") and is enabled by setting the ONHM bit (Register 5, bit 3). Caller ID data can be gained up or attenuated using the receive gain control bits in Registers 39 and 41.

5.25. Caller ID

The Si3050 can pass caller ID data from the phone line to a caller ID decoder connected to the DAA.

5.25.1. Type I Caller ID

Type I Caller ID sends the CID data when the phone is on-hook.

In systems where the caller ID data is passed on the phone line between the first and second rings, utilize the following method to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in "5.18. Ring Detection" on page 26, determine when the first ring is complete.
2. Assert the ONHM bit (Register 5, bit 3) to enable caller ID data detection. The caller ID data is passed across the RNG 1/2 pins and presented to the host via the DTX pin.
3. Clear the ONHM bit after the caller ID data is received.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, use the following method to capture the caller ID data:

1. Enable full wave rectified ring detection (RFWE, Register 18, bit 1).
2. Monitor the RDTP and RDTN register bits or the POLI bit to identify if a polarity reversal or a ring signal has occurred. A polarity reversal trips either the RDTP or RDTN ring detection bits, therefore the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; so, if a battery reversal occurs, the DSP should wait a minimum of 40 ms to verify that the event is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Assert the ONHM bit (Register 5, bit 3) to enable caller ID data detection. The caller ID data is passed across the RNG 1/2 pins and presented to the host via the DTX pin.
4. Clear the ONHM bit after the caller ID data is received.

5.25.2. Type II Caller ID

Type II Caller ID sends the CID data while the phone is off-hook. This mode is often referred to as caller ID/call waiting (CID/CW). To receive the CID data when off-hook, use the following procedure (also see Figure 24):

1. The Caller Alert Signal (CAS) tone is sent from the central office (CO) and is digitized along with the line data. The host processor detects the presence of this tone.
2. The DAA must check if there is another parallel device on the same line, which is accomplished by briefly going on-hook, measuring the line voltage, and returning to an off-hook state.
   a. Set the CALD bit (Register 17, bit 5) to disable the calibration that automatically occurs when going off-hook.
   b. Set the RCALD bit (Register 25, bit 5) to disable the resistor calibration that automatically occurs when going off-hook
   c. Set the FOH[1:0] bits (Register 31 bits 6:5) to 11

to reduce the time period for the off-hook counter to 8 ms allowing compliance to the Type II CID timing requirements.

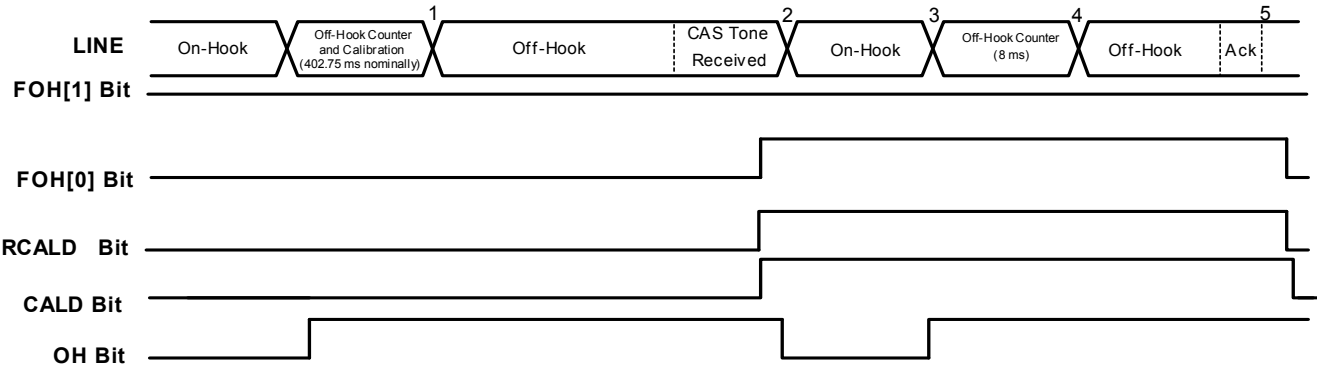
d. Clear the OH bit (Register 5, bit 0). This puts the DAA into an on-hook state. The RXM bit (Register 15, bit 3) also can be set to mute the receive path.

e. Read the LVS bits to determine the state of the line. If the LVS bits read the typical on-hook line voltage, then there are no parallel devices active on the line, and CID data reception can be continued. If the LVS bits read well below the typical on-hook line voltage, then there are one or more devices present and active on the same line that are not compliant with Type II CID. Do not continue CID data reception.

f. Set the OH bit to return to an off-hook state. Immediately after returning to an off-hook state, the off-hook counter must be allowed to expire. This allows the line voltage to settle before transmitting or receiving data. After 8 ms normal data transmission and reception can begin. If a non-compliant parallel device is present, then a reply tone is not sent by the host tone generator and the CO does not send the CID data. If all devices on the line are Type II CID compliant, then the host must mute its upstream data output to avoid the propagation of its reply tone and the subsequent CID data. When muting its upstream data output, the host processor should return an acknowledgement (ACK) tone to the CO requesting transmission of CID data.

3. The CO then responds with CID data after receiving the CID data, the host processor unmutes the upstream data output and continues with normal operation.
4. The muting of the upstream data path by the host processor mutes the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.
5. The CALD and the RCALD bits can be cleared to re-enable the automatic calibrations when going off-hook. The FOH[1:0] bits also can be programmed to 01 to restore the default off-hook counter time.

Because of the nature of the low-power ADC, the data presented on DTX can have up to a 10% dc offset. The caller ID decoder must either use a high-pass or a band-pass filter to accurately retrieve the caller ID data.



Notes:

1. The off-hook counter and calibrations prevent transmission or reception of data for 402.75 ms (default) for the line voltage to settle.
2. The caller alert signal (CAS) tone transmits from the CO to signal an incoming call.
3. The device is taken on-hook to read the line voltage in the LVS bits to detect parallel handsets. In this mode, no data is transmitted on the DTX pin.
4. When the device returns off-hook, the normal off-hook counter is reduced to 8 ms. If the CALD and RCALD bits are set, then the automatic calibrations are not performed.
5. After allowing the off-hook counter to expire (8 ms), normal transmission and reception can continue. If CID data reception is required, send the appropriate signal to the CO at this time.

Figure 24. Implementing Type II Caller ID on the Si3050+Si3011

5.26. Overload Detection

The Si3050 can be programmed to detect an overload condition that exceeds the normal operating power range of the DAA circuit. To use the overload detection feature, the following steps should be followed:

1. Set the OH bit (Register 5, bit 0) to go off-hook, and wait 25 ms to allow line transients to settle.
2. Enable overload detection by then setting the OPE bit (Register 17, bit 3).

If the DAA senses an overload situation it automatically presents an 800 Ω impedance to the line to reduce the hookswitch current. At this time, the DAA also sets the OPD bit (Register 19, bit 0) to indicate that an overload condition exists. The line current detector within the DAA has a threshold that is dependent on the ILIM bit (Register 26). When ILIM = 0, the overload detection threshold equals 160 mA. When ILIM = 1, the overload detection threshold equals 60 mA. The OPE bit should always be cleared before going off-hook.

5.27. Gain Control

The Si3050 supports multiple levels of gain and attenuation for the transmit and receive paths.

The TXG2 and RXG2 bits (Registers 38–39) enable gain or attenuation in 1 dB increments for the transmit and receive paths (up to 12 dB gain and 15 dB attenuation). The TGA2 and RGA2 bits select either gain or attenuation. The TXG3 and RXG3 bits (Registers 40–41) enable gain or attenuation in 0.1 dB increments up to 1.5 dB for the transmit and receive paths. The TGA3 and RGA3 bits select either gain or attenuation. The transmit and receive paths can be individually muted with the TXM and RXM bits (Register 15). The signal flow through the Si3050 and the Si3011 is shown in Figures 25–26.

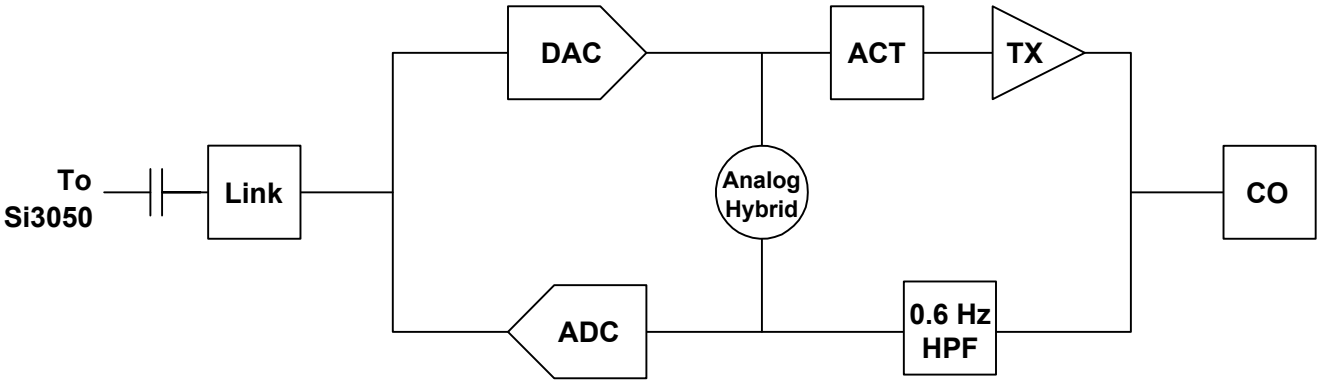


Figure 25. Si3011 Signal Flow Diagram

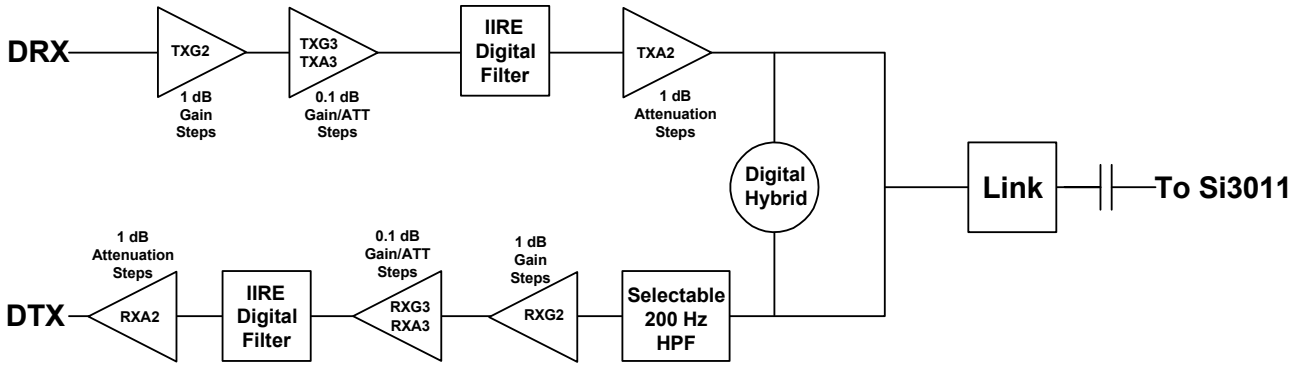


Figure 26. Si3050 Signal Flow Diagram

5.28. Transhybrid Balance

The Si3050 contains an on-chip analog hybrid that performs the 2- to 4-wire conversion and near-end echo cancellation. This hybrid circuit is adjusted for each ac termination setting selected to achieve a minimum transhybrid balance of 20 dB when the line impedance matches the impedance set by ACIM.

The Si3050 also offers a digital hybrid stage for additional near-end echo cancellation. For each ac termination setting, the eight programmable hybrid registers (Registers 45–52) can be programmed with coefficients to increase cancellation of real-world line impedances. This digital filter can produce 10 dB or greater of near-end echo cancellation in addition to the trans-hybrid loss from the analog hybrid circuitry. Coefficients are 2s complement, where unity is represented as binary 0100 0000b, the maximum value as binary 0111 1111b, and the minimum value as binary 1000 000b. See AN84 for a more detailed description of the digital hybrid and how to use it.

5.29. Filter Selection

The Si3050 supports additional filter selections for the receive and transmit signals as defined in Tables 10 and 11. The IIRE bit (Register 16, bit 4) selects between the IIR and FIR filters. The IIR filter provides a shorter, but non-linear, group delay alternative to the default FIR filter, and only operates with an 8 kHz sample rate. The FILT bit (Register 31, bit 1) selects a –3 dB low frequency pole of 5 Hz when cleared and a –3 dB low frequency pole of 200 Hz (per EIA/TIA 464) when set. The FILT bit affects the receive path only.

5.30. Clock Generation

The Si3050 generates the necessary internal clock frequencies from the PCLK input. PCLK must be synchronous to the 8 kHz FSYNC clock and run at one of the following rates: 256 kHz, 512 kHz, 768 kHz, 1.024 MHz, 1.53 MHz, 2.048 MHz, 4.09 MHz, or 8.192 MHz. The ratio of the PCLK rate to the FSYNC rate is determined internally by the DAA and is transferred into internal registers after a reset. These internal registers are not accessible through register reads or writes. Figure 27 shows the operation of the Si3050 clock circuitry.

The PLL clock synthesizer settles quickly after powerup. However, the settling time depends on the PCLK frequency and it can be approximately predicted by the following equation:

$$T_{settle} = 64/F_{PCLK}$$

For all valid PCLK frequencies listed above, the default line sample rate is 8 kHz. This sample rate can be increased to 16 kHz by setting the HSSM bit (Register 7, bit 3). Regardless of the sample rate frequency, the serial data communication rate of the PCM and GCI highways remains 8 kHz. When the 16 kHz sample rate is selected, additional timeslots in the PCM or GCI highway are used to transfer the additional data.

5.31. Communication Interface Mode Selection

The Si3050 supports two communication interface protocols:

- PCM/SPI mode where data and control information transmission/reception occurs across separate buses (PCM highway for data, and SPI port for control).
- GCI mode where data and control information is multiplexed and transmission/reception occurs across the GCI highway bus.

A pin-strapping method (specifically, the state of SCLK on power-up [reset]) is used to select between the two communication interface protocols. Tables 16 and 17 specify how to select a communication mode, and how the various pins are used in each mode.

When operating in PCM/SPI mode, the GCI control register should not be written (i.e., Register 42 must each remain set at 0000_0000 when using the PCM/SPI highway mode). Similarly, when operating in GCI highway mode the PCM registers should not be written (i.e., Registers 33–37 must remain set to 0000_0000 when using the GCI highway mode).

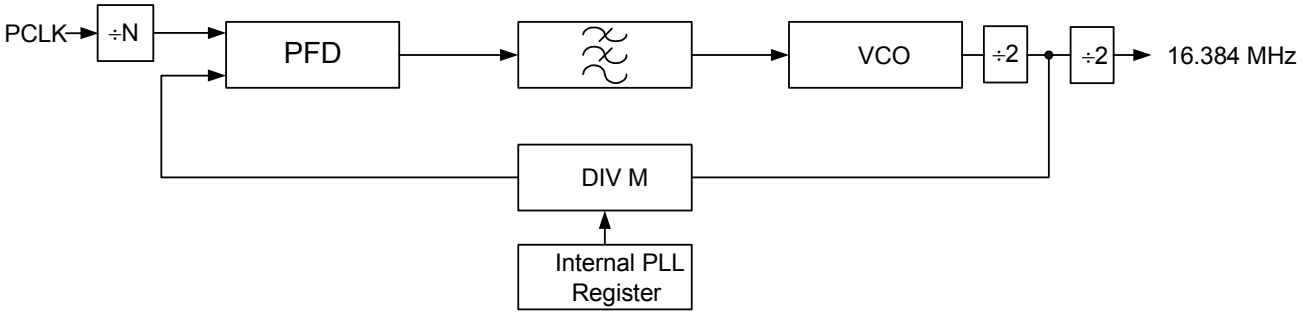


Figure 27. PLL Clock Synthesizer

Table 17. PCM or GCI Highway Mode Selection

SCLK	SDI	Mode Selected
1	X	PCM Mode
0	0	GCI Mode, B2 Channel used
0	1	GCI Mode, B1 Channel used
Note: Values shown are the states of the pins at the rising edge of RESET.		

Table 18. Pin Functionality in PCM or GCI Highway Mode

Pin Name	PCM Mode	GCI Mode
SDI_THRU	SPI Data Throughput pin for Daisy Chaining Operation (Connects to the SDI pin of the subsequent device in the daisy chain)	Sub-frame Selector, bit 2
SCLK	SPI Clock Input	PCM/GCI Mode Selector
SDI	SPI Serial Data Input	B1/B2 Channel Selector
SDO	SPI Serial Data Output	Sub-frame Selector, bit 1
CS	SPI Chip Select	Sub-frame Selector, bit 0
FSYNC	PCM Frame Sync Input	GCI Frame Sync Input
PCLK	PCM Input Clock	GCI Input Clock
DTX	PCM Data Transmit	GCI Data Transmit
DRX	PCM Data Receive	GCI Data Receive
Note: This table denotes pin functionality after the rising edge of RESET and mode selection.		

5.32. PCM Highway

The Si3050 contains a flexible programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled via the PCLK and FSYNC inputs, the PCM Transmit and Receive Start Count registers (Registers 34–37), and the PCM Mode Select register (Register 33). The interface can be configured to support from 4 to 128 8-bit timeslots in each frame, which corresponds to PCLK frequencies of 256 kHz to 8.192 MHz in power of 2 increments. Time slot assignment and data delay from FSYNC edge are handled via the TXS and RXS registers. These 10-bit values are programmed with the number of PCLK cycles following the rising edge of FSYNC until the data transfer begins. Because the Si3050 looks for the rising edge of FSYNC, both long and short FSYNC pulse widths can be accommodated. A value of 0 in the PCM Transmit and Receive Start Count registers signifies that the MSB of the data should occur in the same cycle as the rising edge of FSYNC.

By setting the correct starting point of the data, the Si3050 can operate with buses having multiple devices requiring different time slots. The DTX pin is high impedance except during transmission of an 8-bit PCM sample. DTX returns to high impedance either on the negative edge of PCLK during the LSB or on the positive edge of PCLK following the LSB. This behavior is based on the setting of the TRI bit in the PCM Mode Select register. Tristating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots without the risk of driver contention. In addition to 8-bit data modes, a 16-bit linear mode is also provided. This mode can be activated via the PCMF bits in the PCM Mode Select register. Double-clocked timing also is supported in which the duration of a data bit is two PCLK cycles. This mode is activated via the PHCF bit in the PCM Mode Select register. Setting the TXS or RXS registers greater than the number of PCLK cycles in a sample period stops data transmission or reception. Figures 28–31 illustrate the usage of the PCM highway interface to adapt to common PCM standards.

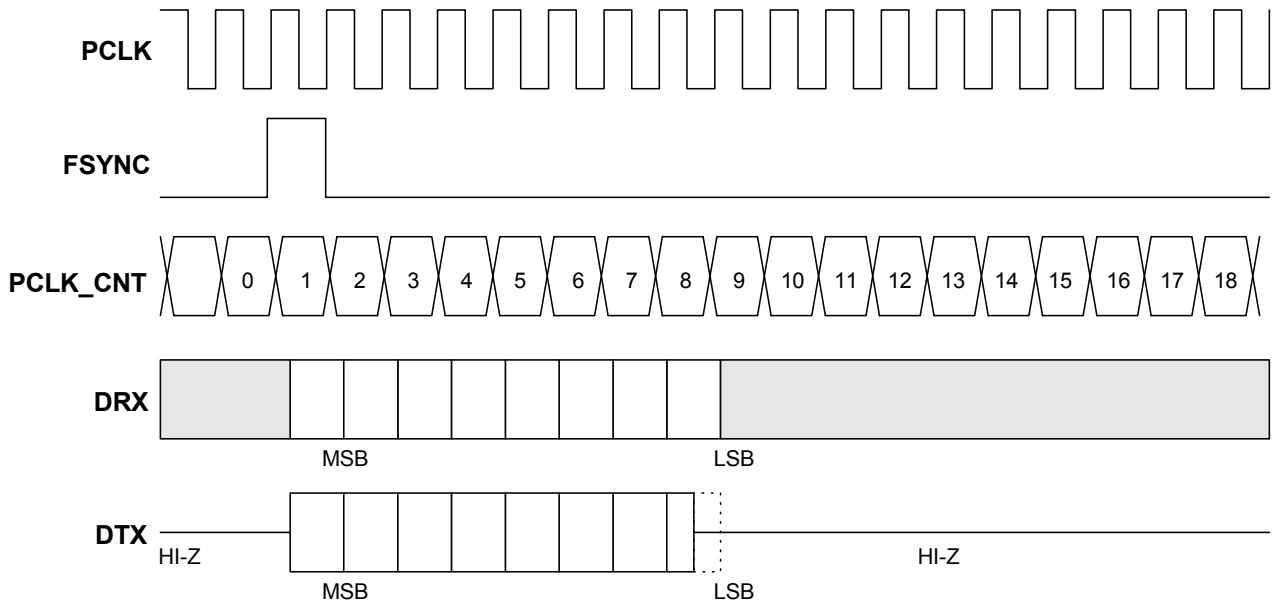


Figure 28. PCM Highway Transmission, Short FSYNC, Single Clock Cycle Delayed Transmission (TXS = RXS = 0, PHCF = 0, TRI = 1)

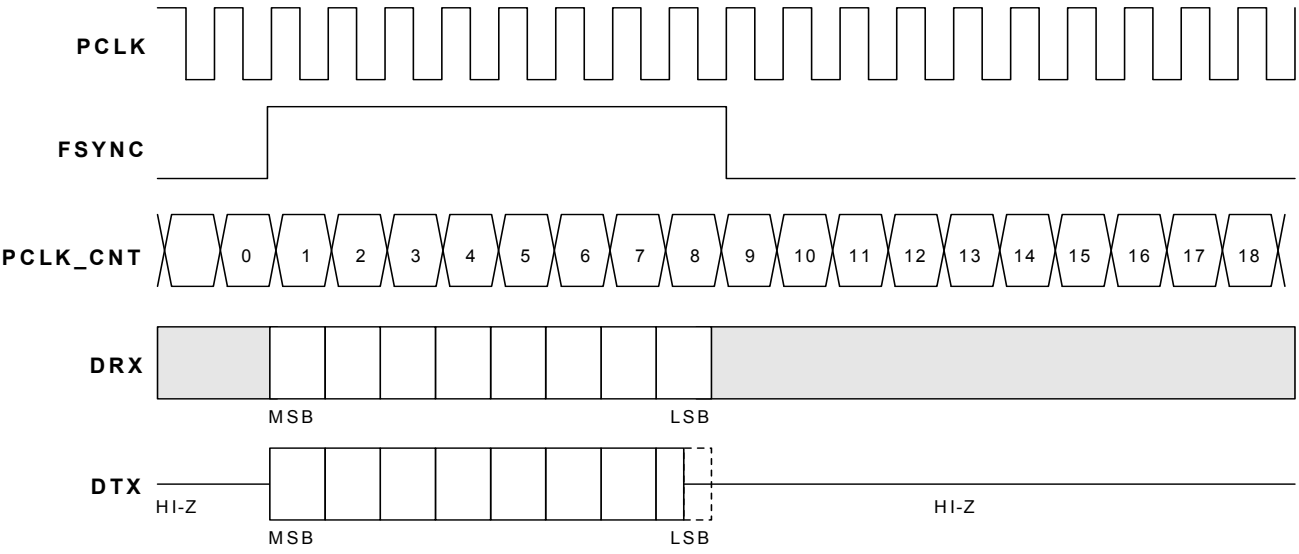


Figure 29. PCM Highway Transmission, Long FSYNC (TXS = RXS = 0, PHCF = 0, TRI = 1)

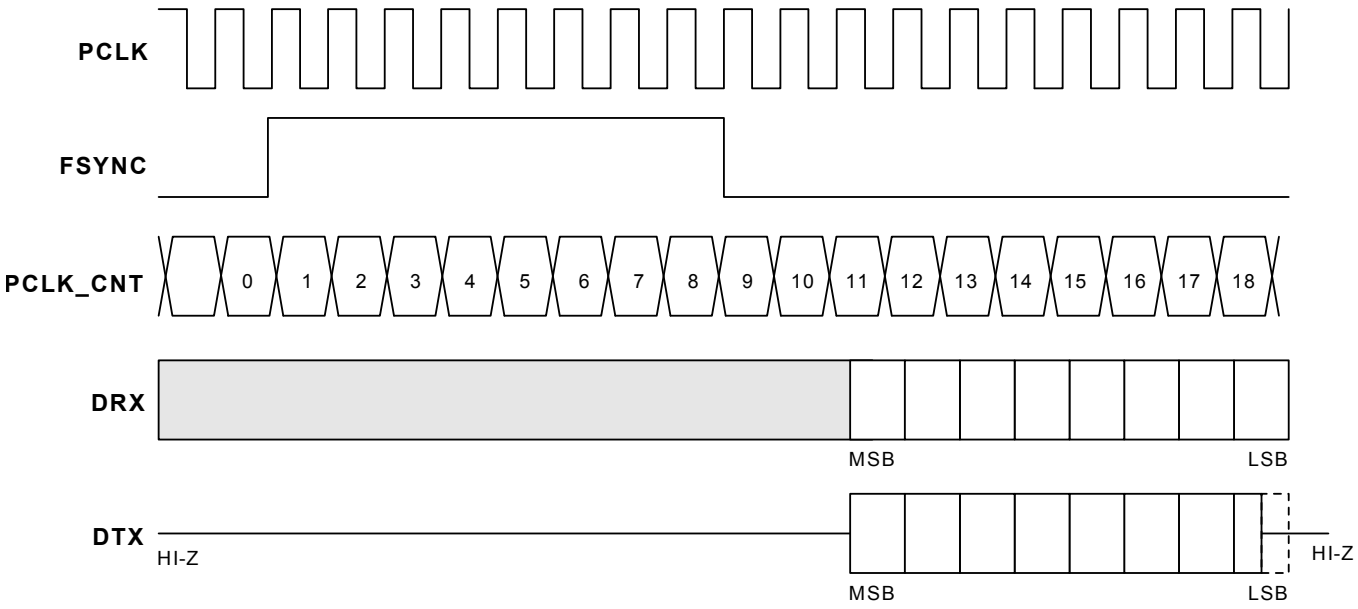


Figure 30. PCM Highway Transmission, Long FSYNC, Delayed Data Transfer (TXS = RXS = 10, PHCF = 0, TRI = 1)

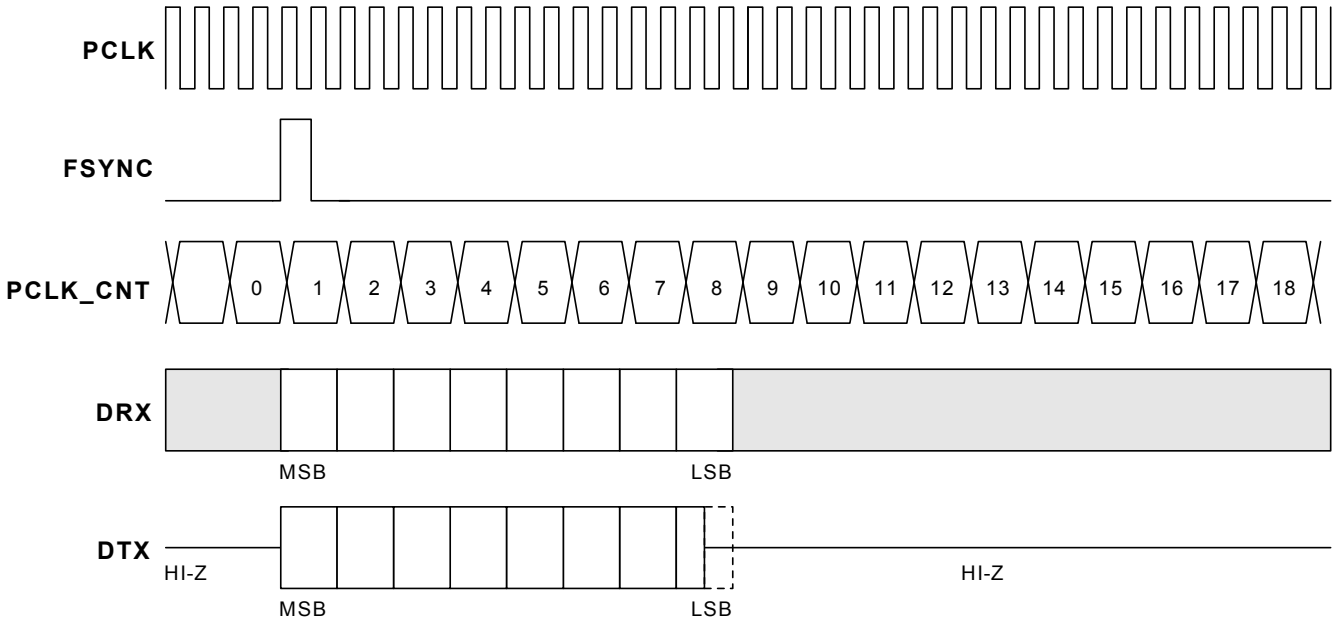


Figure 31. PCM Highway Double Clocked Transmission, Short FSYNC (TXS = RXS = 0, PHCF = 1, TRI = 1)

5.33. Companding in PCM Mode

The Si3050 supports both µ-Law and A-Law companding formats in addition to 16-bit linear data. The 8-bit companding schemes follow a segmented curve formatted as a sign bit, three chord bits, and four step bits. µ-Law is commonly used in North America and Japan, while A-Law is primarily used in Europe. Data format is selected via the PCMF bits (Register 33). Table 19 on page 38 and Table 20 on page 39 define the µ-Law and A-Law encoding formats. If linear mode is used the resulting 16-bit data is transmitted in two consecutive 8-bit PCM highway timeslots as shown in Figure 32.

5.34. 16 kHz Sampling Operation in PCM Mode

The Si3050 can be configured to support a 16 kHz sampling rate and transmit the data on an 8 kHz PCM or GCI highway bus. By setting the HSSM bit (Register 7, bit 3) to 1, the DAA changes its sampling rate, Fs, to 16 kHz if it was originally configured for an 8 kHz sampling rate. If µ-law or A-law companding is used, the resulting 8-bit samples are transmitted in two consecutive 8-bit PCM highway timeslots. If linear mode is used, the resulting 16-bit samples are transmitted in four consecutive 8-bit PCM highway timeslots as shown in Figure 33.

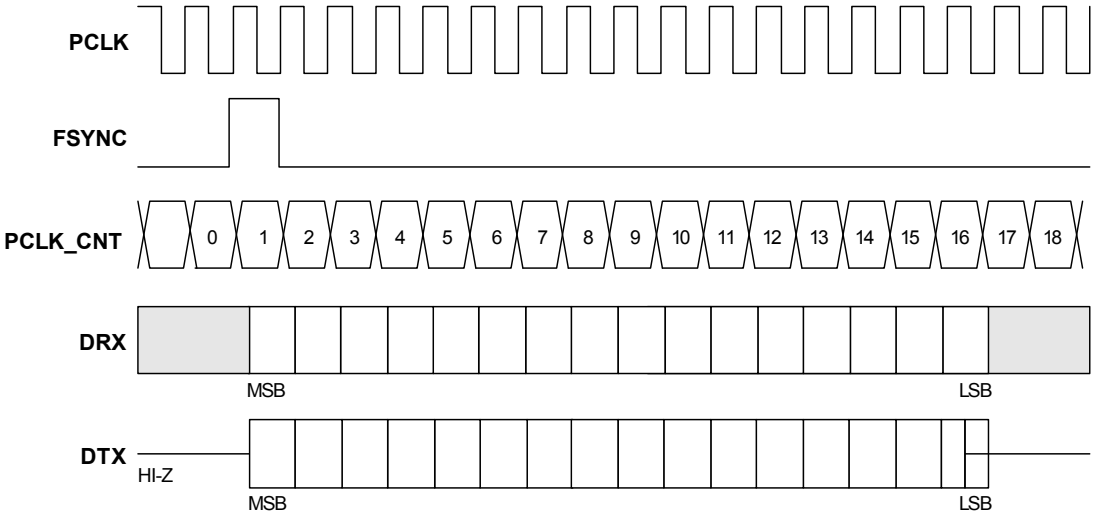


Figure 32. PCM Highway Transmission, Single Clock Cycle, 16-bit linear mode (TXS = RXS = 0, PHCF = 0, TRI = 1, PCMF = 11)

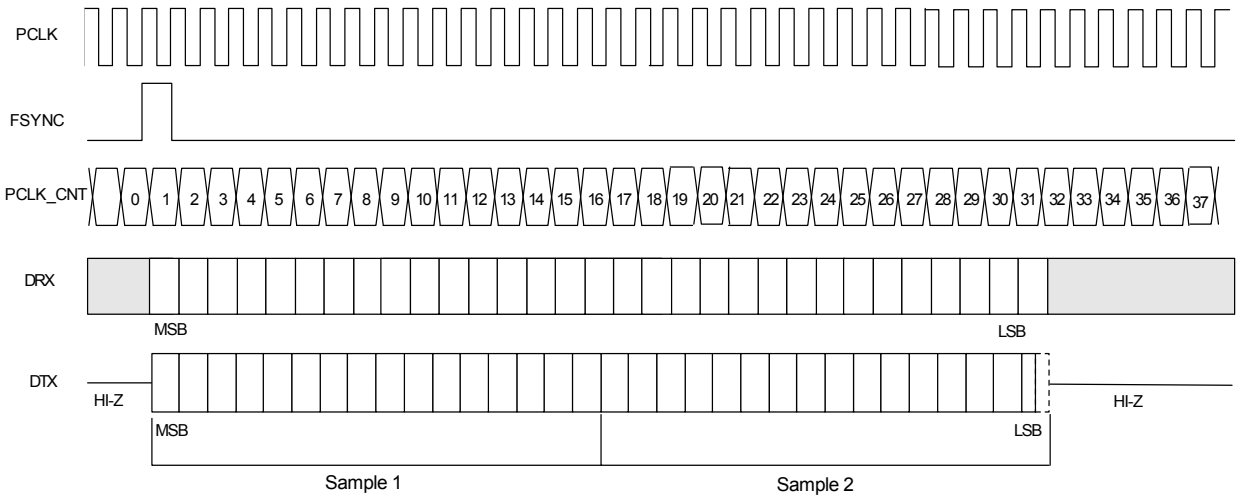


Figure 33. PCM Highway Transmission, Single Clock Cycle, 16-bit linear mode (TXS = RXS = 0, PHCF = 0, TRI = 1, PCMF = 11, HSSM = 1)

Table 19. µ-Law Encode-Decode Characteristics[1,2]

Segment Number	#Intervals x Interval Size	Value at Segment Endpoints	Digital Code	Decode Level
8	16 x 256	8159 . . . 4319 4063	10000000b 10001111b	8031 4191
7	16 x 128	. . . 2143 2015	 10011111b	 2079
6	16 x 64	. . . 1055 991	 10101111b	 1023
5	16 x 32	. . . 511 479	 10111111b	 495
4	16 x 16	. . . 239 223	 11001111b	 231
3	16 x 8	. . . 103 95	 11011111b	 99
2	16 x 4	. . . 35 31	 11101111b	 33
1	15 x 2 1 x 1	. . . 3 1 0	 11111110b 11111111b	 2 0

Notes:
1. Characteristics are symmetrical about analog 0 with sign bit = 1 for negative analog values.
2. Digital code includes inversion of both sign and magnitude bits.

Table 20. A-Law Encode-Decode Characteristics[1,2]

Segment Number	#Intervals x interval size	Value at segment endpoints	Digital Code	Decode Level
7	16 x 128	4096 3968 . . 2143 2015	10101010b 10100101b	4032 2112
6	16 x 64	. . . 1055 991	 10110101b	 1056
5	16 x 32	. . . 511 479	 10000101b	 528
4	16 x 16	. . . 239 223	 10010101b	 264
3	16 x 8	. . . 103 95	 11100101b	 132
2	16 x 4	. . . 35 31	 11110101b	 66
1	32 x 2	. . . 2 0	 11010101b	 1

Notes:
1. Characteristics are symmetrical about analog 0 with sign bit = 1 for negative analog values.
2. Digital code includes inversion of all even numbered bits.

5.35. SPI Control Interface

The control interface to the Si3050 is a 4-wire interface modeled on commonly available micro-controller and serial peripheral devices. The interface consists of four pins: clock (SCLK), chip select ($\overline{CS}$), serial data input (SDI), and serial data output (SDO). In addition, the Si3050 includes a serial data through output pin (SDITHRU) to support daisy chain operation of up to 16 devices. The device can operate with 8-bit and 16-bit SPI controllers. Each SPI operation consists of a control byte, an address byte (of which only the six LSBs are used internally), and either one or two data bytes depending on the width of the controller. Bytes are transmitted MSB first.

There are a number of variations of usage on this four-wire interface as follows:

- Continuous clocking. During continuous clocking, assertion of the $\overline{CS}$ pin controls the data transfers. The $\overline{CS}$ pin must be asserted before the falling edge of SCLK on which the first bit of data is expected during a read cycle, and must remain low for the duration of the 8-bit transfer (command/address or data), going high after the last rising edge of SCLK after the transfer.
- Clock only during transfer. The clock is active during the actual byte transfers only. Each byte transfer consists of eight clock cycles in a return to 1 format.
- SDI/SDO wired operation. Independent of the clocking options described, the SDI and SDO pins can be treated as two separate lines or wired together if the master can tri-state its output during the data byte transfer of a read operation.

The SPI state machine resets when the $\overline{CS}$ pin is asserted during an operation on an SCLK cycle that is not a multiple of eight. This provides a mechanism for the controller to force the state machine to a known state in the case where the controller and the device are not synchronized.

The control byte has the following structure and is presented on the SDI pin MSB first.

7	6	5	4	3	2	1	0
BRCT	R/W	1	0	CID[0]	CID[1]	CID[2]	CID[3]

The bits are defined as follows:

7	BRCT	Indicates a broadcast operation that is intended for all devices in the daisy chain. This is only valid for write operations as it causes contention on the SDO pin during a read.
6	R/W	**Read/Write Bit.** 1 = Read operation. 0 = Write operation.
5	1	This bit must be 1 at all times.
4	0	This bit must be 0 at all times.
3:0	CID[0:3]	This field indicates the channel that is targeted by the operation. The 4-bit channel value is provided LSB first. The devices reside on the daisy chain such that device 0 is nearest to the controller and device 15 is furthest away in the SDI/SDITHRU chain. See Figure 34. As the CID information propagates down the daisy chain, each channel decrements the CID by 1. The device that receives a value of 0 in the CID field responds to the SPI transaction. See Figure 35. If a broadcast to all devices connected to the chain is requested, the CID do not decrement. In this case, the same 8- or 16-bit data is presented to all channels regardless of the CID values.

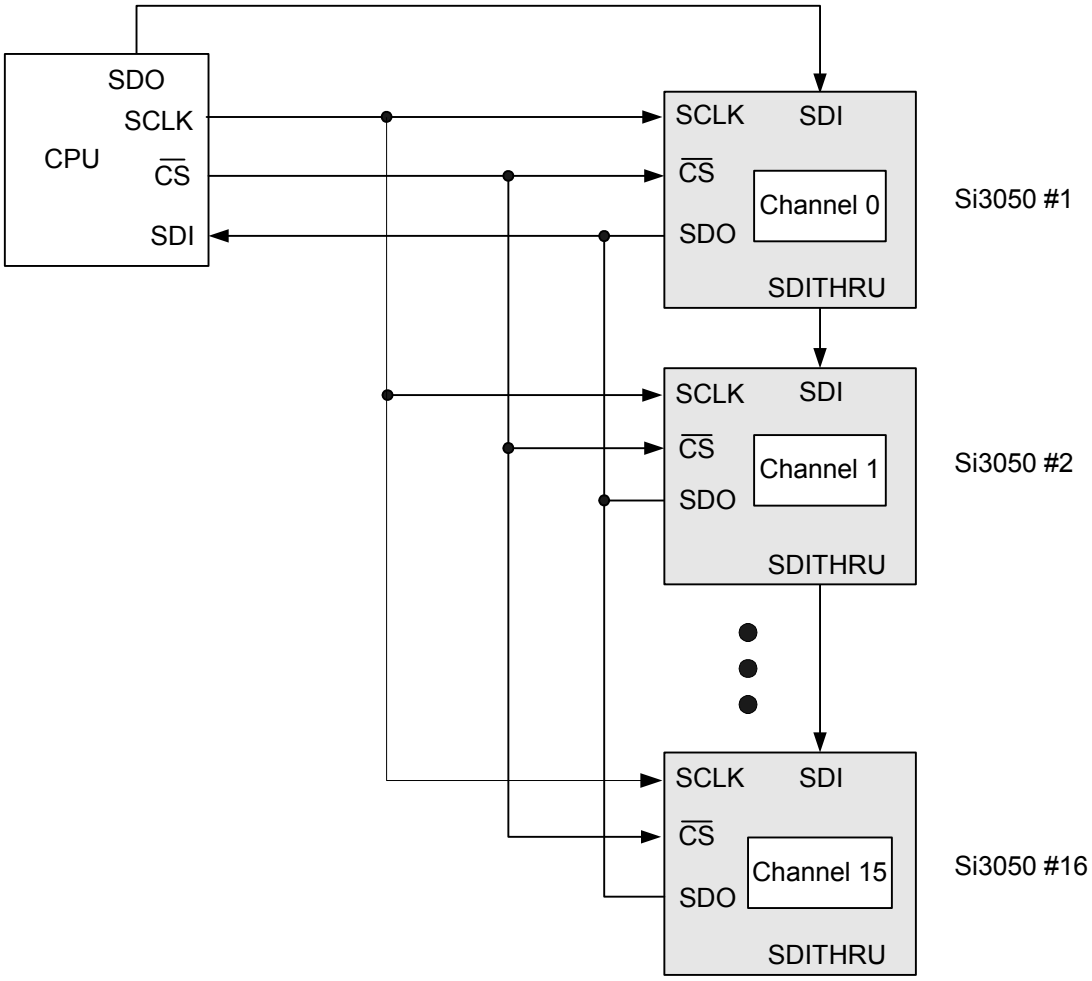


Figure 34. SPI Daisy Chain Control Architecture

SPI Control Byte

	BRCT	R/W	1	0	CID[0]	CID[1]	CID[2]	CID[3]
SDI0	0	0 or 1	1	0	0	0	0	0
SDI1	0	0 or 1	1	0	1	0	0	0
SDI2	0	0 or 1	1	0	0	1	0	0
SDI3	0	0 or 1	1	0	1	1	0	0
SDI14	0	0 or 1	1	0	0	1	1	1
SDI15	0	0 or 1	1	0	1	1	1	1

Figure 35. Sample SPI Control Byte to Access Channel 0

Figure 36. Sample SPI Control Byte for Broadcast Mode (Write Only)

In Figure 35 the CID field is 0. As this field is decremented in LSB to MSB order, the value decrements for each SDI down the line. The BRCT and R/W bits remain unchanged as the control word passes through the entire chain. A unique CID is presented to each device, and the device receiving a CID value of 0 is the target of the operation (channel 0 in this case). Figure 36 illustrates that in broadcast mode, all bits pass through the chain without permutation.

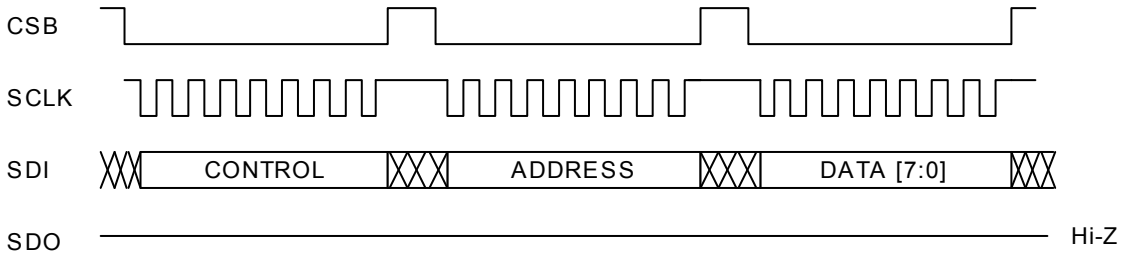


Figure 37. Write Operation via an 8-bit SPI Port

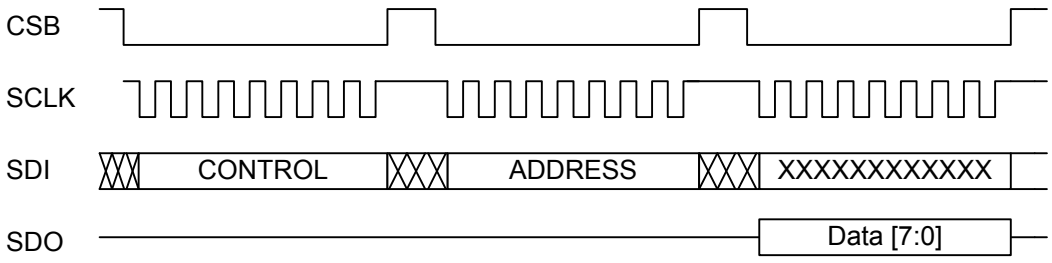


Figure 38. Read Operation via an 8-bit SPI Port

Figure 37 and Figure 38 illustrate WRITE and READ operations via an 8-bit SPI controller. Each of these operations are performed as a 3-byte transfer. The $\overline{CS}$ pin is asserted between each byte. The $\overline{CS}$ pin must be asserted before the first falling edge of SCLK after the DATA byte to indicate to the state machine that only one byte should be transferred. The state of the SDI pin is ignored during the DATA byte of a read operation.

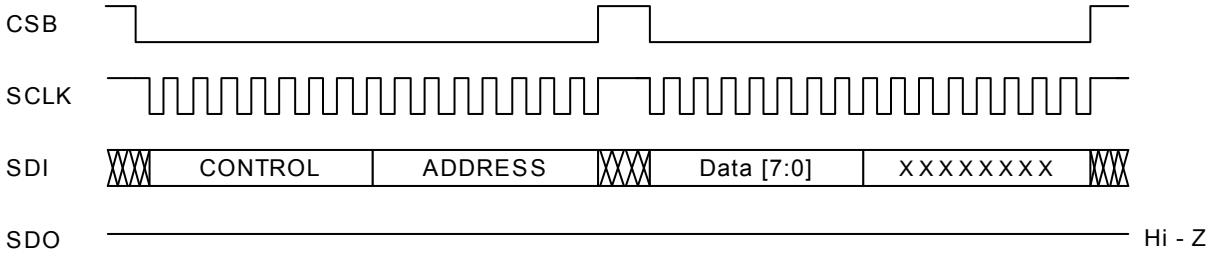


Figure 39. Write Operation via a 16-bit SPI Port

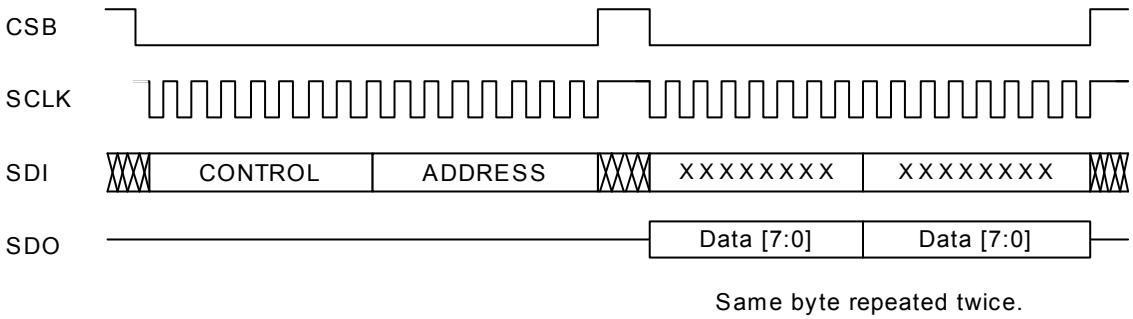


Figure 40. Read Operation via a 16-bit SPI Port

Figures 39 and 40 illustrate WRITE and READ operations via a 16-bit SPI controller. These operations require a 4-byte transfer arranged as two 16-bit words. The $\overline{CS}$ pin does not go high when the eighth bit of data is received, which indicates to the SPI state machine that eight more SCLK pulses follow to complete the operation. In the case of a WRITE operation, the last eight bits are ignored. In a read operation, the 8-bit data value is repeated so that the data may be captured during the last half of a data transfer if required by the controller. The Si3050 autodetects the SPI mode (16-bit or 8-bit mode).

5.36. GCI Highway

The Si3050 contains an alternate communication interface to the SPI and PCM highway control and data interface. The general circuit interface (GCI) can be used for the transmission and reception of control and data information onto a GCI highway bus. The PCM and GCI highways are 4-wire interfaces and share the same pins. The SPI control interface is not used as a communication interface in the GCI highway mode, but rather as hardwired channel selector pins.

When GCI mode is selected, the sub-frame selection pins must be tied to the correct state to select one of eight sub-frame timeslots in the GCI frame (Table 21). These pins must remain in this state when the Si3050 is operating. Selecting a particular subframe automatically causes that individual Si3050 to transmit and receive on the appropriate sub-frame in the GCI frame, which is initiated by an FSYNC pulse. No more register settings are needed to select which sub-frame a device uses, and the sub-frame for a particular device cannot be changed when in operation. Only one Si3050 DAA can be assigned per sub-frame, which allows a total of eight DAAs to be connected to the same GCI highway bus.

GCI mode supports a 1x and a 2x PCLK rate as shown in Figures 5 and 6 on pages 13 and 14, respectively. The PCLK rate is autodetected and no internal register settings are needed to support either 1x or 2x PCLK mode.

Table 21. GCI Mode Sub-Frame Selection

	SDI_THRU	SDO	$\overline{CS}$
GCI Subframe 0 Selected (Voice channels 1–2)	1	1	1
GCI Subframe 1 Selected (Voice channels 3–4)	1	1	0
GCI Subframe 2 Selected (Voice channels 5–6)	1	0	1
GCI Subframe 3 Selected (Voice channels 7–8)	1	0	0
GCI Subframe 4 Selected (Voice channels 9–10)	0	1	1
GCI Subframe 5 Selected (Voice channels 11–12)	0	1	0
GCI Subframe 6 Selected (Voice channels 13–14)	0	0	1
GCI Subframe 7 Selected (Voice channels 15–16)	0	0	0

The GCI highway requires either a 2.048 or 4.096 MHz clock frequency on the PCLK pin, and an 8 kHz frame sync input on the FSYNC pin. The overall unit of data used to communicate on the GCI highway is a frame, which is 125 µs in length. Each frame is initiated by a pulse on the FSYNC pin and the rising edge signifies the beginning of the next frame. In 2x PCLK mode, there are twice as many PCLK cycles during each 125 µs frame versus 1x PCLK mode. Each frame consists of eight fixed timeslot sub-frames that are assigned using the Sub-Frame Select pins as described in Table 18 on page 34 (SDI_THRU, SDO, and $\overline{CS}$). Within each sub-frame are four channels (bytes) of data, including the two voice data channels (B1 and B2), one Monitor channel (M) for initialization and setup of the device, and one Signaling and Control channel (SC) for communicating status of the device and for initiating commands. Within the SC channel are six Command/Indicate (C/I) bits and two handshaking bits (MR and MX). The C/I bits are used for status and command communication, whereas the handshaking bits Monitor Receive (MR) and Monitor Transmit (MX) are used for data exchanges in the Monitor channel. Figure 41 illustrates the contents of a GCI highway frame.

5.37. Companding in GCI Mode

The Si3050 supports µ-Law and A-Law companding formats in addition to 8-bit or 16-bit linear data. The 8-bit companding schemes are described in "5.33. Companding in PCM Mode" on page 37 and are shown in Table 19 and Table 20. If 16-bit linear mode is used, the resulting 16-bit samples are transmitted in both the B1 and B2 channels of a single subframe. For proper operation, select all Si3050 DAAs to use the B1 channel with only one DAA per subframe.

5.38. 16 kHz Sampling Operation in GCI Mode

The Si3050 can be configured to support a 16 kHz sampling rate (as described in "5.34. 16 kHz Sampling Operation in PCM Mode" on page 37) and transmit the data on an 8 kHz GCI Highway bus. If 8-bit samples are used with a 16 kHz sample rate, the samples are transmitted in both the B1 and B2 channels of a single subframe. If 16-bit linear mode is used, the resulting 16-bit samples are transmitted in both the B1 and B2 channels of two consecutive subframes. In this case, assign one DAA per two subframes.

5.39. Monitor Channel

The Monitor channel is used for initialization and setup of the Si3050. It also can be used for general communication with the Si3050 by allowing read and write access to the Si3050's registers. Use of the monitor channel requires manipulation of the MR and MX handshaking bits, located in bits 1 and 0 of the SC channel described below. For purposes of this specification, "downstream" is identified to be the data sent by a host to the Si3050. "Upstream" is identified to be the data sent by the Si3050 to a host.

Figure 41 illustrates the Monitor channel communication protocol. For successful communication with the Si3050, the transmitter should anticipate the falling edge of the receiver's acknowledgement. This also maximizes communication speed. Because of the handshaking protocol required for successful communication, the data transfer rate using the Monitor channel is less than 8 kbytes/second.

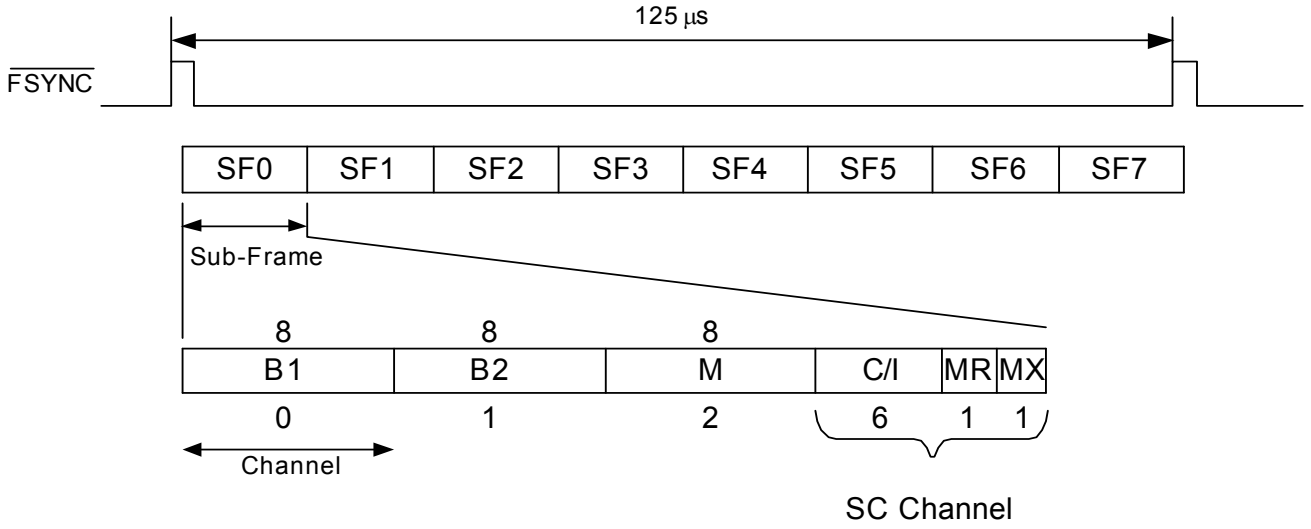


Figure 41. Time-Multiplexed GCI Highway Frame Structure

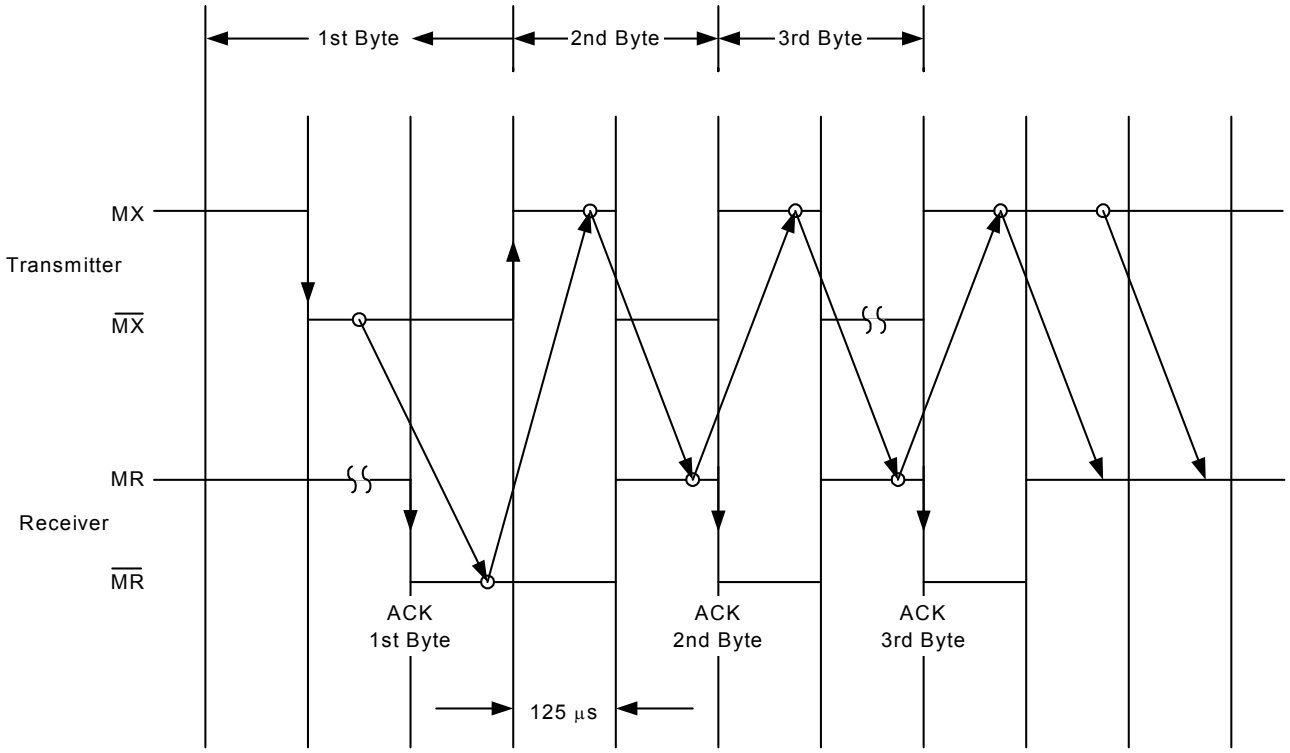


Figure 42. Monitor Handshake Timing

The Idle state is achieved by the MX and MR bits being held inactive (signal is high) for two or more frames. When a transmission is initiated by a host device, an active state (signal is low) is present on the downstream MX bit. This signals to the Si3050 that a transmission has begun on the Monitor channel and the Si3050 should begin accepting data from host device. The Si3050, after reading the data on the Monitor channel, acknowledges the initial transmission by placing the upstream MR bit in an active state. The data is received and the upstream MR becomes active in the frame immediately following the downstream MX becoming active. The upstream MR then remains active until either the next byte is received or an end of message is detected. The end of message is signaled by the downstream MX being held inactive for two or more consecutive frames. Receipt of initial data is signaled by the upstream MR bit's transitioning from an inactive to an active state. Upon receiving acknowledgement from the Si3050 that the initial data is received, the host device places the downstream MX bit in the inactive state for one frame and then either transmit another byte by placing the downstream MX bit in an active state again, or signal an end of message by leaving the downstream MX bit inactive for a second frame.

When the host is performing a write command, the host only manipulates the downstream MX bit, and the Si3050 only manipulates the upstream MR bit. If a read command is performed, the host initially manipulates the downstream MX bit to communicate the command, but then manipulates the downstream MR bit in response to the Si3050 responding with the requested data. Similarly, the Si3050 initially manipulates its upstream MR bit to receive the read command, and then manipulates its upstream MX bit to respond with the requested data. If the host is transmitting data, the Si3050 always transmits a $FF value on its Monitor data byte. While the Si3050 is transmitting data, the host should always transmit a $FF value on its Monitor byte. If the Si3050 is transmitting data and detects a value other than a $FF on the downstream Monitor byte, the Si3050 signals an Abort.

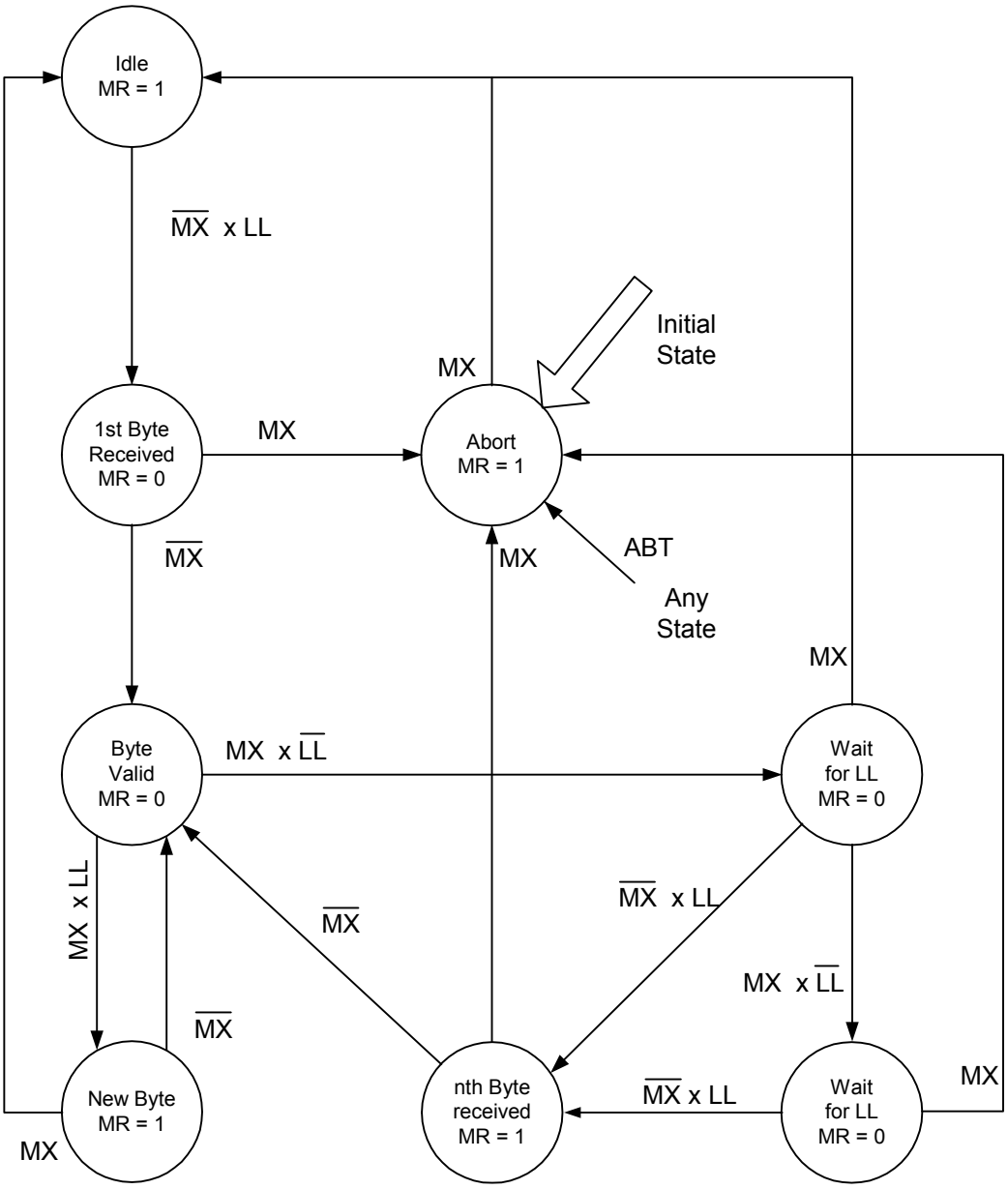
For read and write commands, an initial address must be specified. The Si3050 responds to a read or a write command at this address, and then subsequently increment this address after every register access.

In this manner, multiple consecutive registers can be read or written in one transmission sequence. By correctly manipulating the MX and MR bits, a transmission sequence can continue from the beginning specified address until an invalid memory location is reached. To end a transmission sequence, the host processor must signal an end-of-message (EOM) by placing the downstream MX and MR bits inactive for two consecutive frames. The transmission also can be stopped by the Si3050 by signaling an Abort. This is signaled by placing the upstream MR bit inactive for at least two consecutive cycles in response to the downstream MX bit going active. An abort is signaled by the Si3050 for the following reasons:

- A read or write to an invalid memory address is attempted
- An invalid command sequence is received
- A data byte was not received for at least two consecutive frames
- A collision occurs on the Monitor data bytes while the Si3050 is transmitting data

When the Si3050 aborts because of an invalid command sequence, the state of the Si3050 does not change. If a read or write to an invalid memory address is attempted, all previous reads or writes in that transmission sequence are valid up to the read or write to the invalid memory address. If an EOM is detected before a valid command sequence is communicated, the Si3050 returns to the idle state and remains unchanged.

The data presented to the Si3050 in the downstream Monitor bits must be present for two consecutive frames to be considered valid data. The Si3050 checks to ensure it receives the same data in two consecutive frames. If not, it does not acknowledge receipt of the data byte and waits until it does receive two consecutive identical data bytes before acknowledging to the transmitter that it received the data. If the transmitter attempts to signal transmission of a subsequent data byte by placing the downstream MX bit in an inactive state while the Si3050 is still waiting to receive a valid data byte transmission of two consecutive identical data bytes, the Si3050 signals an abort and ends the transmission. Figure 43 shows a state diagram for the Receiver Monitor channel for the Si3050. Figure 44 on page 48 shows a state diagram for the Transmitter Monitor channel for the Si3050.



MR: MR bit calculated and transmitted on DTX line.
MX: MX bit received data downstream (DRX line).
LL: Last look of monitor byte received on DRX line.
ABT: Abort indication to internal source.

Figure 43. Si3050 Monitor Receiver State Diagram

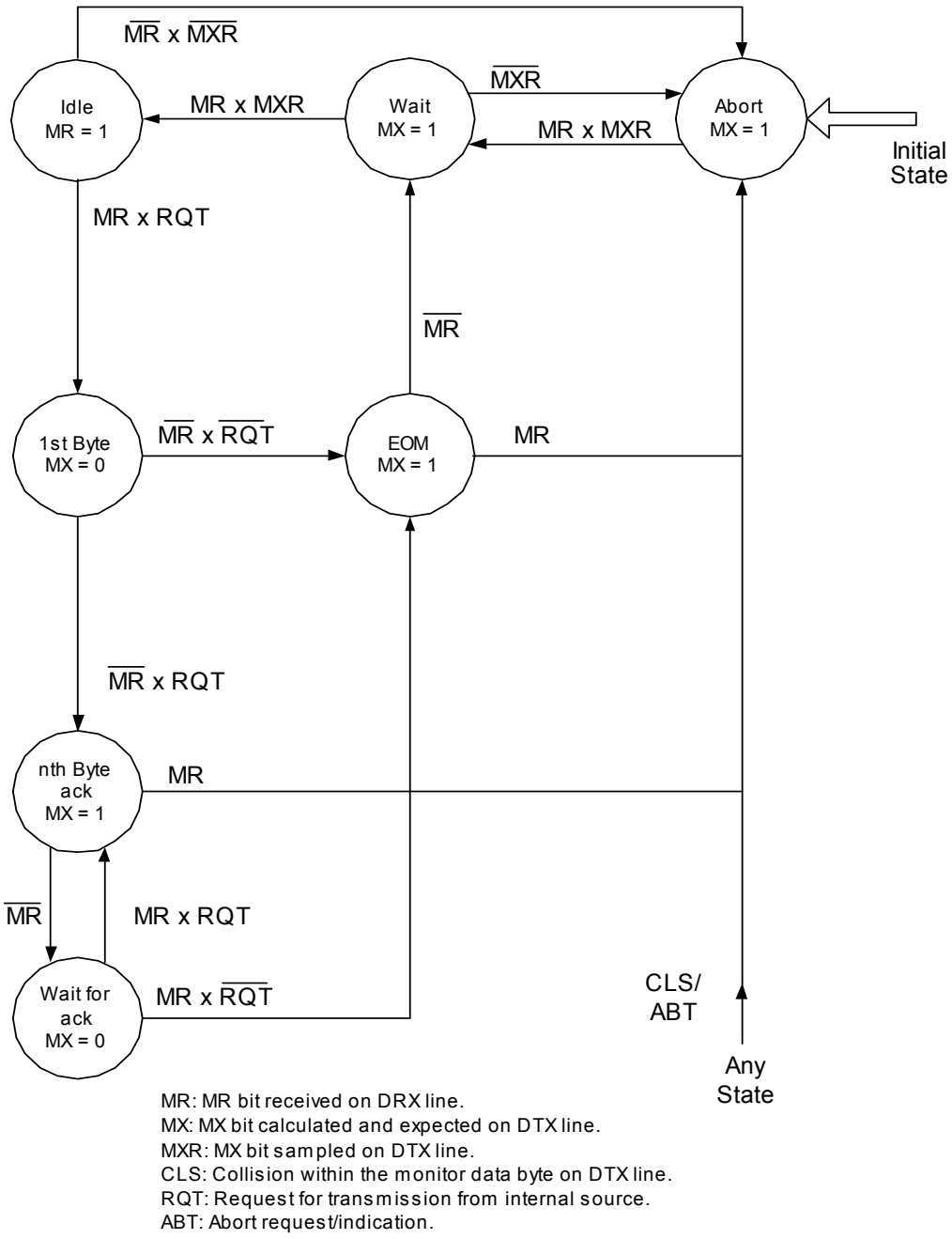


Figure 44. Si3050 Monitor Transmitter State Diagram

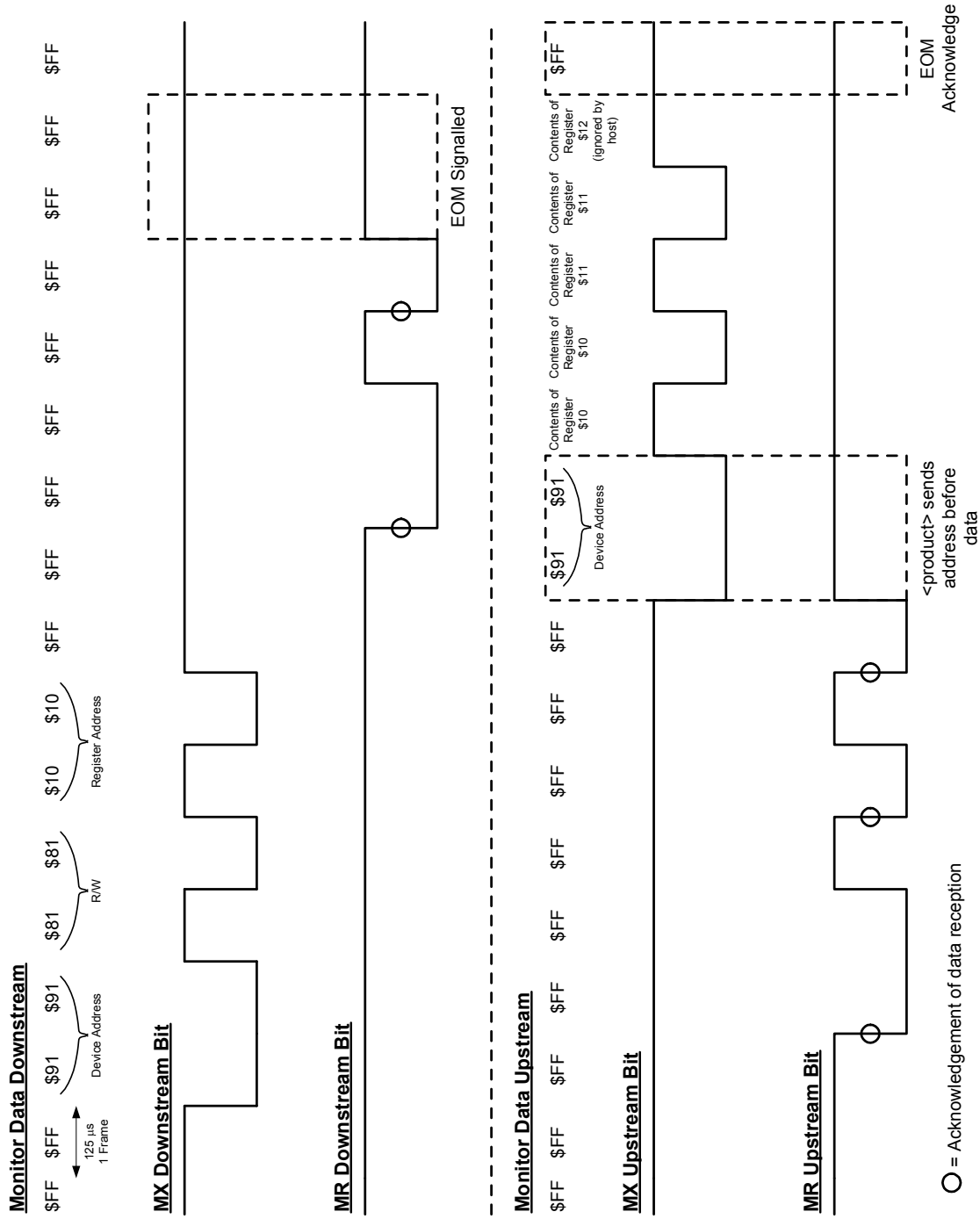


Figure 45. Example Read of Registers $10 and $11 in Subframe 0 of the Si3050

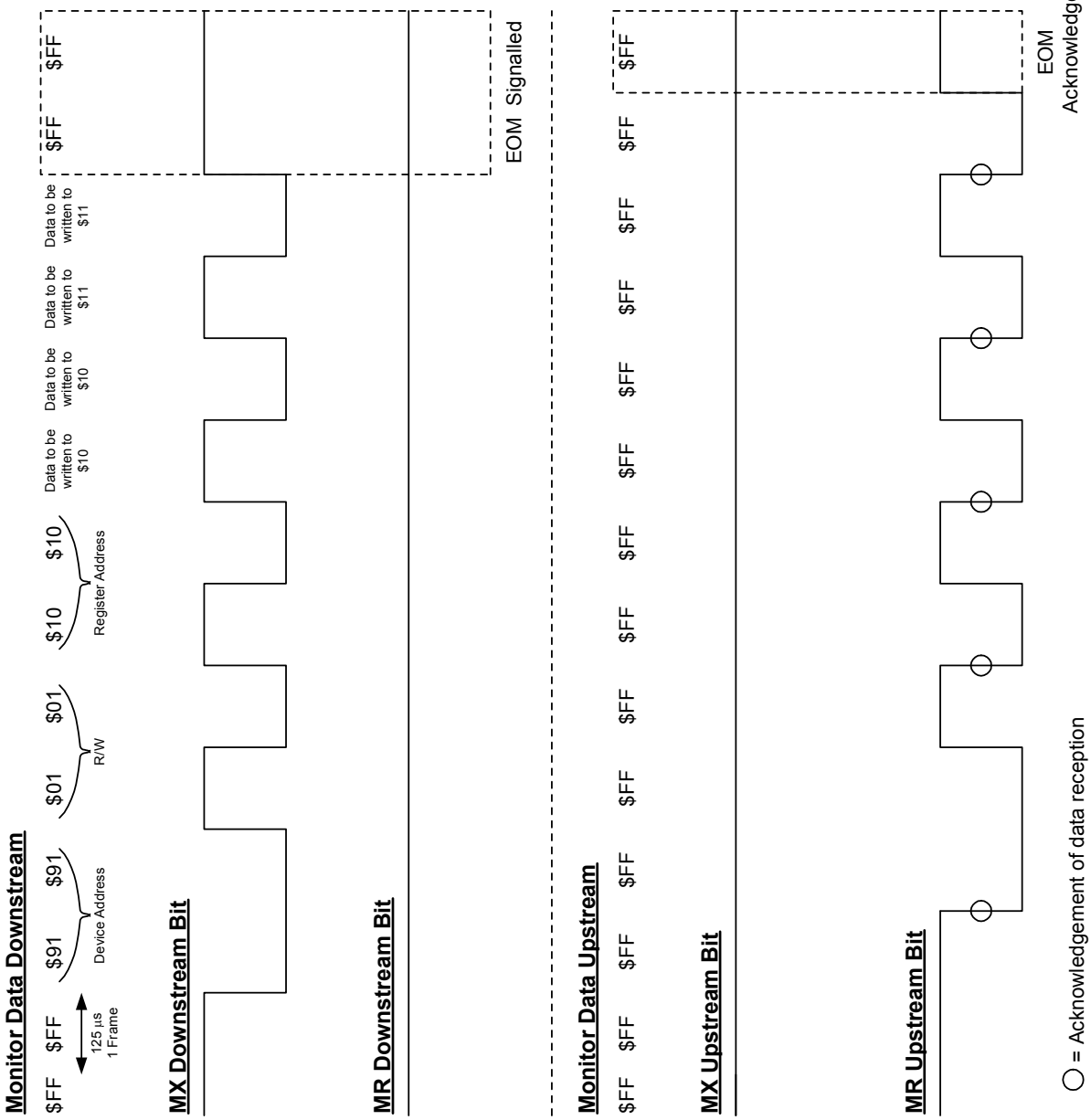


Figure 46. Example Write to Registers $10 and $11 in Subframe 0 of the Si3050

5.40. Summary of Monitor Channel Commands

Communication with the Si3050 should be in the following format:

Byte 1: Device Address Byte

Byte 2: Command Byte

Byte 3: Register Address Byte

Bytes 4-n: Data Bytes

Bytes n+1, n+2: EOM

5.41. Device Address Byte

The Device Address byte identifies which device connected to the GCI highway receives the particular message. This address should be the first byte sent to the Si3050 at the beginning of every transmission sequence. For Read commands, the address sent to the Si3050 is the first byte transmitted in response to the Read command before register data is transmitted. This Device Address byte has the following structure:

1	0	0	A	B	0	0	C

The lowest programmable bit, C, has a special function. This bit enables a register read or write, or enables a special Channel Identification Command (CID).

C = 1: Normal command follows.

C = 0: Channel Identification Command.

The CID is a special command to identify themselves by software. For this special command, the subsequent command byte transmitted by the host processor must be $00 (binary), and have no address or data bytes. The Si3050 in turn responds with a fixed 2-byte identification code:

1	0	0	A	0	0	0	0
1	0	1	1	1	1	1	0

Upon sending the 2-byte identification code, the Si3050 sends an EOM (MR = MX = 1) for two consecutive frames. When A = 0, B must be 0 or the Si3050 signals an abort due to an invalid command. In this mode, bit C is the only other programmable bit.

A = 0: Response to CID command from the device using channel B1 is placed in Monitor Data.

A = 1: Response to CID command from the device using channel B2 is placed in Monitor Data.

When C = 1, bits A and B are channel enable bits. When these bits are set to 1, the individual corresponding channels receives the command in the next command byte. The channels whose corresponding bits are set to 0 ignores the subsequent command byte.

A = 1: Channel B1 receives the command.

A = 0: Channel B1 does not receive the command.

B = 1: Channel B2 receives the command.

B = 0: Channel B2 does not receive the command.

5.42. Command Byte

The Command byte has the following structure:

RW	CMD[6:0]

The RW bit is a register read/write bit.

RW = 0: A write is performed to the Si3050's register.

RW = 1: A read is performed on the Si3050's register.

The CMD[6:0] bits specify the actual command to be performed.

CMD[6:0] = 0000001: Read or write a register on the Si3050.

CMD[6:0] = 0000010 – 1111111: Reserved.

5.43. Register Address Byte

The Register Address byte has the following structure:

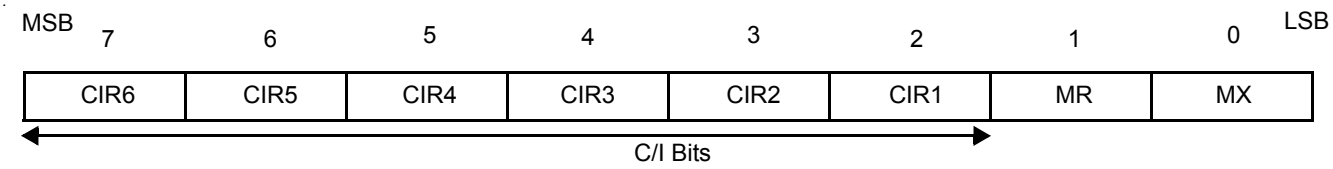
ADDRESS[7:0]

This byte contains the actual 8-bit address of the register to be read or written.

5.44. SC Channel

The SC channel consists of six C/I bits and two handshaking bits, MR and MX. One of these channels is contained in every 4-byte sub-frame and is transmitted every frame. The handshaking bits are described in the above Monitor Channel section. The definition of the six C/I bits depends on the direction the bits are being sent, either transmitted to the GCI highway bus via the DTX pin or received from the GCI highway bus via the DRX pin.

5.45. Receive SC Channel



These bits are defined as follows:

CIR6: Reserved

CIR5: Reserved

CIR4: ONHM

CIR3: TGDE

CIR2: RG

CIR1: OH

Data that is received must be consistent and match for at least two consecutive frames to be considered valid. When a new command or status is communicated via the C/I bits, the data must be sent for at least two consecutive frames to be recognized by the Si3050. The following steps describe the protocol of how C/I bits are stored, detected, and validated. This is illustrated in Figure 47.

1. The current state of the C/I bits are stored in a primary register P. If the received C/I bits are identical to this current state, no action is taken.
2. Upon receipt of an SC channel with C/I bits that differ from the current state, these new C/I bits are immediately latched into a secondary register S.
3. The C/I bits in the SC channel received in the frame immediately after the SC channel just stored in S are compared with the C/I bits in the S register.
   a. If the C/I bits in these two channels are identical, then the C/I bits in the S register are loaded into the P register and are considered a valid change of C/I bits. The Si3050 then responds accordingly to the changed C/I bits.
   b. If a set of C/I bits is latched into the S register and the subsequent set of C/I bits received does not match either the S or P registers, then the newly received set of C/I bits are latched into the S register. This continues to occur as long as the subsequent set of C/I bits received differs from the C/I bits in the S and P registers.
   c. If the C/I bits in the SC channel received immediately after the SC channel just stored in S do not match the C/I bits stored in S, but DO match the C/I bits stored in P, then the single set of C/I bits stored in the S latch are invalidated, and the current state of the C/I bits in P remains unchanged.

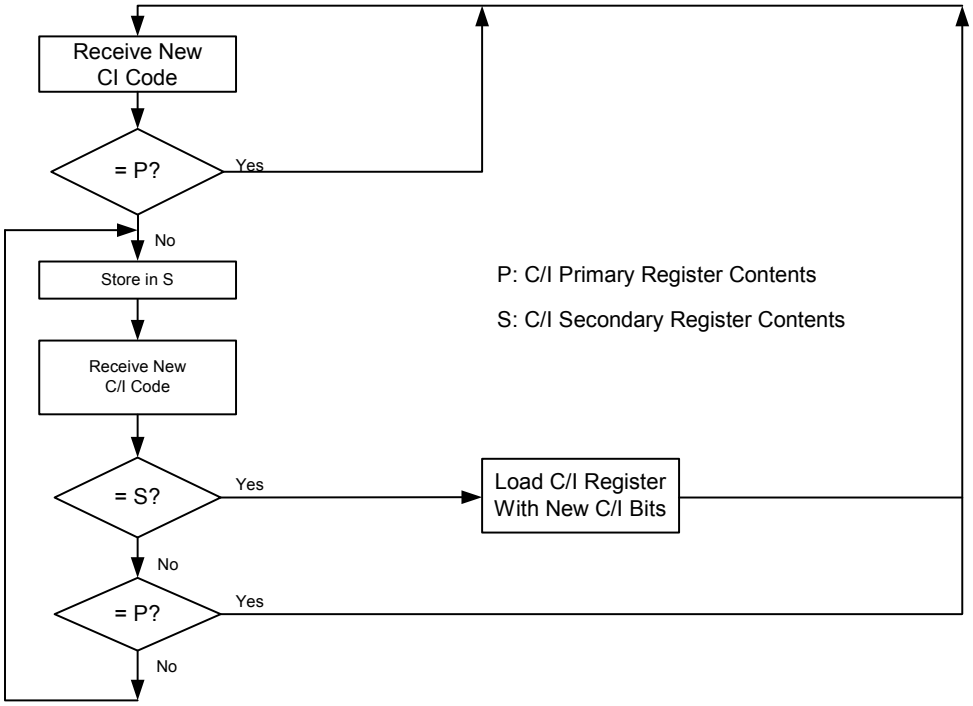
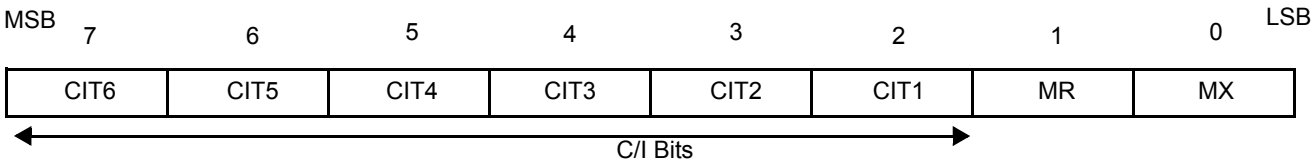


Figure 47. Protocol for Receiving C/I Bits in the Si3050

5.46. Transmit SC Channel

The following diagram shows the definition of the transmitted SC channel, which is transmitted MSB first.



These bits are defined as follows:

CIT6: Reserved

CIT5: CVI

CIT4: DOD

CIT3: INT (represents the state of the $\overline{\text{INT}}$ pin)

CIT2: Battery Reversal (represents the state of bit 7 of the LVS register)

CIT1: TGD

6. Control Registers

Note: Registers not listed here are reserved and must not be written.

Table 22. Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR		PWMM[1:0]		PWME		IDL	
2	Control 2	INTE	INTP		WDTEN		RDI	HBE	RXE
3	Interrupt Mask	RDTM	ROVM	FDTM	BTDM	DODM	LCSOM	TGDM	POLM
4	Interrupt Source	RDTI	ROVI	FDTI	BTDI	DODI	LCSOI	TGDI	POLI
5	DAA Control 1		RDTN	RDTP		ONHM	RDT		OH
6	DAA Control 2				PDL	PDN			
7	Sample Rate Control					HSSM			
8	Reserved								
9	Reserved								
10	DAA Control 3								DDL
11	System- and Line-Side Device Revision	LSID[3:0]				REVA[3:0]			
12	Line-Side Device Status		FDT		LCS[4:0]				
13	Line-Side Device Revision		1	REVB[3:0]					
14	DAA Control 4							RPOL	
15	TX/RX Gain Control 1	TXM				RXM			
16	International Control 1				IIRE				
17	International Control 2	CALZ	MCAL	CALD		OPE	BTE	ROV	BTD
18	International Control 3							RFWE	
19	International Control 4						OVL	DOD	OPD
20	Call Progress RX Attenuation	ARM[7:0]							
21	Call Progress TX Attenuation	ATM[7:0]							
22	Ring Validation Control 1	RDLY[1:0]		RMX[5:0]					
23	Ring Validation Control 2	RDLY[2]	RTO[3:0]				RCC[2:0]		
24	Ring Validation Control 3	RNGV		RAS[5:0]					
25	Resistor Calibration	RCALS	RCALM	RCALD		RCAL[3:0]			
26	DC Termination Control					0	0	ILIM	DCR
27	Reserved								
28	Loop Current Status	LCS2[7:0]							
29	Line Voltage Status	LVS[7:0]							
30	AC Termination Control				FULL2			ACIM	
31	DAA Control 5		FOH[1:0]		0	OHS2	0	FILT	LVFD
32	Ground Start Control						TGD	TGDE	RG
33	PCM/SPI Mode Select	PCML		PCME	PCMF[1:0]		0	PHCF	TRI
34	PCM Transmit Start Count—Low Byte	TXS[7:0]							
35	PCM Transmit Start Count—High Byte							TXS[1:0]	
36	PCM Receive Start Count—Low Byte	RXS[7:0]							
37	PCM Receive Start Count—High Byte							RXS[1:0]	
38	TX Gain Control 2				TGA2	TXG2[3:0]			
39	RX Gain Control 2				RGA2	RXG2[3:0]			
40	TX Gain Control 3				TGA3	TXG3[3:0]			
41	RX Gain Control 3				RGA3	RXG3[3:0]			
42	GCI Control					GCIF[1:0]		B2D	B1D
43	Line Current/Voltage Threshold Interrupt	CVT[7:0]							
44	Line Current/Voltage Threshold Interrupt Control					CVI	CVS	CVM	CVP
45–52	Programmable Hybrid Register 1–8	HYB1–8[7:0]							
53–58	Reserved								
59	RX Gain Control 1						RG1	GCE	

Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR		PWMM[1:0]		PWME		IDL	
Type	R/W		R/W		R/W		R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset.** 0 = Enables the DAA for normal operation. 1 = Sets all registers to their reset value. **Note:** Bit automatically clears after being set.
6	Reserved	Read returns zero.
5:4	PWMM[1:0]	**Pulse Width Modulation Mode.** Used to select the type of signal output on the call progress AOUT pin. 00 = PWM output is clocked at 16.384 MHz as a delta-sigma data stream. A local density of 1s and 0s tracks the combined transmit and receive signals. Use this setting with the optional call progress circuit shown in Figure 18 on page 19. 01 = Balanced conventional PWM output signal has high and low portions of the modulated pulse that are centered on the 16 kHz sample clock. 10 = Conventional PWM output signal returns to logic 0 at regular 32 kHz intervals and rises at a time in the 32 kHz period proportional to its instantaneous amplitude. 11 = Reserved.
3	PWME	**Pulse Width Modulation Enable.** 0 = Pulse width modulation mode disabled (AOUT). 1 = Enable pulse width modulation mode for the call progress analog output (AOUT). This mode sums the transmit and receive audio paths and presents this as a CMOS digital-level output of PWM data. The circuit in Figure 18 on page 19 should be used.
2	Reserved	Read returns zero.
1	IDL	**Isolation Digital Loopback.** 0 = Digital loopback across the isolation barrier is disabled. 1 = Enables digital loopback mode across the isolation barrier. The line-side device must be enabled and off-hook prior to setting this mode. The data path includes the TX and RX filters.
0	Reserved	Read returns zero.

Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INTE	INTP		WDTEN		RDI	HBE	RXE
Type	R/W	R/W		R/W		R/W	R/W	R/W

Reset settings = 0000_0011

Bit	Name	Function
7	INTE	**Interrupt Pin Enable.** 0 = The AOUT/$\overline{\text{INT}}$ pin functions as an analog output for call progress monitoring purposes. 1 = The AOUT/$\overline{\text{INT}}$ pin functions as a hardware interrupt pin.
6	INTP	**Interrupt Polarity Select.** 0 = The AOUT/$\overline{\text{INT}}$ pin, when used in hardware interrupt mode, is active low. 1 = The AOUT/$\overline{\text{INT}}$ pin, when used in hardware interrupt mode, is active high.
5	Reserved	Read returns zero.
4	WDTEN	**Watchdog Timer Enable.** 0 = Watchdog timer disabled. 1 = Watchdog timer enabled. When set, this bit can be cleared only by a hardware reset. The watchdog timer monitors register access. If no register access occurs within a 4 s window, the DAA is put into an on-hook state. A read or write of a DAA register restarts the watchdog timer counter. If the watchdog timer times out, the OH bit is cleared, placing the DAA into an on-hook state. Setting the OH bit places the DAA back into an off-hook state.
3	Reserved	Read returns zero.
2	RDI	**Ring Detect Interrupt Mode.** This bit operates in conjunction with the RDTM and RDTI bits. This bit selects whether one or two interrupts are generated for every ring burst. 0 = An interrupt is generated at the beginning of every ring burst. 1 = An interrupt is generated at the beginning and end of every ring burst. The interrupt at the beginning of the ring burst must be serviced (by writing 0 to the RDTI bit) before the end of the ring burst in order for both interrupts to occur.
1	HBE	**Hybrid Enable.** 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable.** 0 = Receive path disabled. 1 = Enables receive path.

Register 3. Interrupt Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTM	ROVM	FDTM	BTDM	DODM	LCSOM	TGDM	POLM
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RDTM	**Ring Detect Mask.** 0 = A ring signal does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A ring signal causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
6	ROVM	**Receive Overload Mask.** 0 = A receive overload does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A receive overload causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
5	FDTM	**Frame Detect Mask.** 0 = The ISOcap losing frame lock does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = The ISOcap losing frame lock causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
4	BTDM	**Billing Tone Detect Mask.** 0 = A detected billing tone does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A detected billing tone causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
3	DODM	**Drop Out Detect Mask.** 0 = A line supply dropout does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A line supply dropout causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
2	LCSOM	**Loop Current Sense Overload Mask.** 0 = An interrupt does not occur when the LCS bits are all 1s. 1 = An interrupt occurs when the LCS bits are all 1s.
1	TGDM	**TIP Ground Detect Mask.** 0 = The TGD bit going active does not cause an interrupt on the AOUT/INT pin. 1 = The TGD bit going active causes an interrupt on the AOUT/INT pin.
0	POLM	**Polarity Reversal Detect Mask.** This interrupt is generated from bit 7 of the LVS register. When this bit transitions, it indicates that the polarity of TIP and RING is switched. 0 = A polarity change on TIP and RING does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A polarity change on TIP and RING causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.

Register 4. Interrupt Source

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTI	ROVI	FDTI	BTDI	DODI	LCSOI	TGDI	POLI
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RDTI	**Ring Detect Interrupt.** 0 = A ring signal is not occurring. 1 = A ring signal is detected. If the RDTM bit (Register 3) and INTE bit (Register 2) are set, a hardware interrupt occurs on the AOUT/INT pin. This bit must be written to a 0 to be cleared. The RDI bit (Register 2) determines if this bit is set only at the beginning of a ring pulse, or at the both the beginning and end of a ring pulse. This bit should be cleared after clearing the PDL bit (Register 6) as powering up the line-side device can cause this interrupt to be triggered.
6	ROVI	**Receive Overload Interrupt.** 0 = Normal operation. 1 = An excessive input level on the receive pin is detected. If the ROVM bit (Register 3) and INTE bit (Register 2) are set, a hardware interrupt occurs on the AOUT/INT pin. This bit must be written to 0 to clear it. This bit is identical in function to the ROV bit (Register 17) and clearing this bit also clears the ROV bit.
5	FDTI	**Frame Detect Interrupt.** 0 = Frame detect is established on the ISOcap link. 1 = This bit is set when the ISOcap link does not have frame lock. If the FDTM bit (Register 3) and INTE bit (Register 2) are set, a hardware interrupt occurs on the AOUT/INT pin. When set, this bit must be written to 0 to be cleared.
4	BTDI	**Billing Tone Detect Interrupt.** 0 = Normal operation. 1 = The line-side power supply has been disrupted. If the BTDM bit (Register 3) and INTE bit (Register 2) are set, a hardware interrupt occurs on the AOUT/INT pin. This bit must be written to 0 to clear it.
3	DODI	**Drop Out Detect Interrupt.** 0 = Normal operation. 1 = The line-side power supply has collapsed. (The DOD bit in Register 19 has fired.) If the DODM bit (Register 3) and INTE bit (Register 2) are set, a hardware interrupt occurs on the AOUT/INT pin. This bit must be written to 0 to be cleared. This bit should be cleared after clearing the PDL bit (Register 6) as powering up the line-side device can cause this interrupt to be triggered.
2	LCSOI	**Loop Current Sense Overload Interrupt.** 0 = Normal operation. 1 = The LCS bits have reached max value. If the LCSOM bit (Register 3) and the INTE bit are set, a hardware interrupt occurs on the AOUT/INT pin. This bit must be written to 0 to clear it. **Note:** LCSOI does not necessarily imply that an overcurrent situation has occurred. An overcurrent situation in the DAA is determined by the status of the OPD bit (Register 19). After the LCSOI interrupt fires, the OPD bit should be checked to determine if an overcurrent situation exists.

Bit	Name	Function
1	TGDI	**TIP Ground Detect Interrupt.** This bit is reverse logic as compared to the TGD bit. 0 = The CO has not grounded TIP causing current to flow. 1 = The CO has grounded TIP, causing current to flow. Once set, this bit must be written to 0 to clear it. If the TDGM bit (Register 3) and INTE bit (Register 3) are set, a hardware interrupt occurs on the AOUT/INT pin. To clear the interrupt, write this bit to 0.
0	POLI	**Polarity Reversal Detect Interrupt.** 0 = Bit 7 of the LVS register has not changed states. 1 = Bit 7 of the LVS register has transitioned from 0 to 1, or from 1 to 0, indicating the polarity of TIP and RING is switched. If the POLM bit (Register 3) and INTE bit (Register 2) are set, a hardware interrupt occurs on the AOUT/INT pin. To clear the interrupt, write this bit to 0.

Register 5. DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RDTN	RDTP		ONHM	RDT		OH
Type		R	R		R/W	R		R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	RDTN	**Ring Detect Signal Negative.** 0 = No negative ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	**Ring Detect Signal Positive.** 0 = No positive ring signal is occurring. 1 = A positive ring signal is occurring.
4	Reserved	Read returns zero.
3	ONHM	**On-Hook Line Monitor.** 0 = Normal on-hook mode. 1 = Enables low-power on-hook monitoring mode allowing the host to receive line activity without going off-hook. This mode is used for caller-ID detection.
2	RDT	**Ring Detect.** 0 = Reset 5 seconds after last positive ring is detected or when the system executes an off-hook. Only a positive ring sets this bit when RFWE = 0. When RFWE = 1, either a positive or negative ring sets this bit. 1 = Indicates a ring is occurring.
1	Reserved	Read returns zero.
0	OH	**Off-Hook.** 0 = Line-side device on-hook. 1 = Causes the line-side device to go off-hook.

Register 6. DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PDL	PDN			
Type				R/W	R/W			

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	PDL	**Powerdown Line-Side Device.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Places the line-side device in lower power mode.
3	PDN	**Powerdown System-Side Device.** 0 = Normal operation. 1 = Powers down the system-side device. A pulse on $\overline{\text{RESET}}$ is required to restore normal operation.
2:0	Reserved	Read returns zero.

Register 7. Sample Rate Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					HSSM			
Type					R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	HSSM	**High-Speed Sampling Mode.** 0 = Sample Rate is 8 kHz. 1 = Sample Rate is 16 kHz. The PCM or the GCI highway continues to be at 8 kHz; thus, twice as many samples are generated per device timeslot. Samples are transmitted in adjacent timeslots.
2:0	Reserved	Read returns zero.

Register 8-9. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 10. DAA Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								DDL
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	DDL	**Digital Data Loopback.** 0 = Normal operation. 1 = Takes data received on DRX and loops it back out to DTX before the TX and RX filters. Output data is identical to the input data.

Register 11. System-Side and Line-Side Device Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LSID[3:0]				REVA[3:0]			
Type	R				R			

Reset settings = xxxx_xxxx

Bit	Name	Function
7:4	LSID[3:0]	**Line-Side ID Bits.** The line-side bits corresponding to the Si3011 are 0100.
3:0	REVA[3:0]	**System-Side Revision.** Four-bit value indicating the revision of the Si3050 (system-side) device.

Register 12. Line-Side Device Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FDT		LCS[4:0]				
Type	R			R				

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	FDT	**Frame Detect.** 0 = Indicates ISOcap link has not established frame lock. 1 = Indicates ISOcap link frame lock is established.
5	Reserved	Read returns zero.
4:0	LCS[4:0]	**Off-Hook Loop Current Monitor (3.3 mA/bit).** 00000 = Loop current is less than required for normal operation. 00100 = Minimum loop current for normal operation. 11111 = Loop current is >127 mA, and an overload condition may exist.

Register 13. Line-Side Device Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		1	REVB[3:0]					
Type	R		R					

Reset settings = xxxx_xxxx

Bit	Name	Function
7	Reserved	Read returns zero.
6	Reserved	This bit always reads a one.
5:2	REVB[3:0]	**Line-Side Device Revision.** Four-bit value indicating the revision of the line-side device.
1:0	Reserved	Read returns zero.

Register 14. DAA Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RPOL	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1	RPOL	**Ring Detect Polarity.** 0 = The $\overline{\text{RGDT}}$ pin is active low. 1 = The $\overline{\text{RGDT}}$ pin is active high.
0	Reserved	Read returns zero.

Register 15. TX/RX Gain Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM				RXM			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute.** 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	Reserved	Read returns zero.
3	RXM	**Receive Mute.** 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	Reserved	Read returns zero.

Register 16. International Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				IIRE				
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	These bits may be written to a zero or one.
4	IIRE	**IIR Filter Enable.** 0 = FIR filter enabled for transmit and receive filters. (See Figures 7–10 on page 15.) 1 = IIR filter enabled for transmit and receive filters. (See Figures 11–16 on page 16.)
3:0	Reserved	These bits may be written to a zero or one.

Register 17. International Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALZ	MCAL	CALD	0	OPE	BTE	ROV	BTD
Type	R/W	R/W	R/W		R/W	R/W	R/W	R

Reset settings = 0000_0000

Bit	Name	Function
7	CALZ	**Clear ADC Calibration.** 0 = Normal operation. 1 = Clears the existing ADC calibration data. This bit must be written back to 0 after being set.
6	MCAL	**Manual ADC Calibration.** 0 = No calibration. 1 = Initiate manual ADC calibration.
5	CALD	**Auto-Calibration Disable.** 0 = Enable auto-calibration. 1 = Disable auto-calibration.
4	Reserved	Always write this bit to zero.
3	OPE	**Overload Protect Enable.** 0 = Disabled. 1 = Enabled. The OPE bit should always be cleared before going off-hook.
2	BTE	**Billing Tone Detect Enable.** The DAA can detect events, such as billing tones, that can cause a disruption in the line-side power supply. When this bit is set, the device will maintain off-hook during such events. If a billing tone is detected, the BTD bit (Register 17, bit 0) is set to indicate the event. Writing this bit to zero clears the BTD bit. 0 = Billing tone detection disabled. The BTD bit is not functional. 1 = Billing tone detection enabled. The BTD bit is not functional.
1	ROV	**Receive Overload.** This bit is set when the receive input has an excessive input level (i.e., receive pin goes below ground). Writing a 0 to this location clears this bit and the ROVI bit (Register 4, bit 6). 0 = Normal receive input level. 1 = Excessive receive input level.
0	BTD	**Billing Tone Detected.** This bit is set if an event, such as a billing tone, causes a disruption in the line-side power supply. Writing a zero to BTE clears this bit. 0 = No billing tone detected. 1 = Billing tone detected.

Register 18. International Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RFWE	
Type							R/W	

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	Reserved	This bit may be written to a zero or one.
1	RFWE	**Ring Detector Full-Wave Rectifier Enable.** When RNGV (Register 24) is disabled, this bit controls the ring detector mode and the assertion of the RGDT pin. When RNGV is enabled, this bit configures the RGDT pin to either follow the ringing signal detected by the ring validation circuit, or to follow an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately 5 seconds. **RNGV** **RFWE** **RGDT** 0 0 Half-Wave 0 1 Full-Wave 1 0 Validated Ring Envelope 1 1 Ring Threshold Crossing One-Shot
0	Reserved	Read returns zero.

Register 19. International Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						OVL	DOD	OPD
Type						R	R	R

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	OVL	**Receive Overload Detect.** This bit has the same function as ROV (Register 17), but clears itself after the overload is removed. See “5.22.Receive Overload Detection” on page 28. This bit is only masked by the off-hook counter and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
1	DOD	**Recal/Dropout Detect.** When the line-side device is off-hook, it is powered from the line itself. This bit will read 1 when loop current is not flowing. For example, if this line-derived power supply collapses, such as when the line is disconnected, this bit is set to 1. Additionally, when on-hook, and the line-side device is enabled, this bit is set to 1. 0 = Normal operation. 1 = Line supply dropout detected when off-hook.
0	OPD	**Overload Protect Detect.** This bit is used to indicate that the DAA has detected a loop current overload. The detector firing threshold depends on the setting of the ILIM bit (Register 26). **OPD** **ILIM** **Overcurrent Threshold** **Overcurrent Status** 0 0 160 mA No overcurrent condition exists 0 1 60 mA No overcurrent condition exists 1 0 160 mA Overcurrent condition has been detected 1 1 60 mA Overcurrent condition has been detected

Register 20. Call Progress RX Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ARM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT receive path signal used for call progress monitoring. Setting the bits to all 0s mutes the AOUT receive path. Attenuation = 20 log(ARM[7:0]/64) 1111_1111 = +12 dB (gain) 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB ... 0000_0000 = Mute

Register 21. Call Progress TX Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ATM[7:0]	**AOUT Transmit Path Attenuation.** When decremented from the default settings, these bits linearly attenuate the AOUT transmit path signal used for call progress monitoring. Setting the bits to all 0s mutes the AOUT transmit path. Attenuation = 20 log(ATM[7:0]/64) 1111_1111 = +12 dB (gain) 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB ... 0000_0000 = Mute

Register 22. Ring Validation Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[1:0]		RMX[5:0]					
Type	R/W		R/W					

Reset settings = 1001_0110

Bit	Name	Function
7:6	RDLY[1:0]	**Ring Delay Bits 1 and 0.** These bits, in combination with the RDLY[2] bit (Register 23), set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms ... 1 11 1792 ms
5:0	RMX[5:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field and if it exceeds the value in RMX[5:0] then the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/ (2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms}, RMX \leq RAS$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.

Register 23. Ring Validation Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[2]	RTO[3:0]				RCC[2:0]		
Type	R/W	R/W				R/W		

Reset settings = 0010_1101

Bit	Name	Function
7	RDLY[2]	**Ring Delay Bit 2.** This bit, in combination with the RDLY[1:0] bits (Register 22), sets the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms ... 1 11 1792 ms
6:3	RTO[3:0]	**Ring Timeout.** These bits set when a ring signal is determined to be over after the most recent ring threshold crossing. **RTO[3:0] Ring Timeout** 0000 DO NOT USE THIS SETTING 0001 128 ms 0010 256 ms ... 1111 1920 ms
2:0	RCC[2:0]	**Ring Confirmation Count.** These bits set the amount of time that the ring frequency must be within the tolerances set by the RAS[5:0] bits and the RMX[5:0] bits to be classified as a valid ring signal. **RCC[2:0] Ring Confirmation Count Time** 000 100 ms 001 150 ms 010 200 ms 011 256 ms 100 384 ms 101 512 ms 110 640 ms 111 1024 ms

Register 24. Ring Validation Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV		RAS[5:0]					
Type	R/W		R/W					

Reset settings = 0001_1001

Bit	Name	Function
7	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. 1 = Ring validation feature is enabled in both normal operating mode and low-power mode.
6	Reserved	Always write these bits to zero.
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. If a second or subsequent TIP/RING event occurs after the timer has timed out then the frequency of the ring is too low and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RAS[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $RAS[5:0] \geq \frac{1}{2 \times f\_min \times 2\ ms}$

Register 25. Resistor Calibration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RCALS	RCALM	RCALD		RCAL[3:0]			
Type	R	R/W	R/W		R/W			

Reset settings = xx0x_xxxx

Bit	Name	Function
7	RCALS	**Resistor Auto Calibration.** 0 = Resistor calibration is not in progress. 1 = Resistor calibration is in progress.
6	RCALM	**Manual Resistor Calibration.** 0 = No calibration. 1 = Initiate manual resistor calibration. (After a manual calibration has been initiated, this bit must be cleared within 1 ms.)
5	RCALD	**Resistor Calibration Disable.** 0 = Internal resistor calibration enabled. 1 = Internal resistor calibration disabled.
4	Reserved	This bit can be written to a 0 or 1.
3:0	RCAL[3:0]	Always write back the value read.

Register 26. DC Termination Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					0	0	ILIM	DCR
Type							R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	These bits may be written to a zero or one.
3:2	Reserved	Always write these bits to zero.
1	ILIM	**Current Limiting Enable.** 0 = Current limiting mode disabled. 1 = Current limiting mode enabled. This mode limits loop current to a maximum of 60 mA per the TBR21 standard.
0	DCR	**DC Impedance Selection.** 0 = 50 Ω dc termination is selected. This mode should be used for all standard applications. 1 = 800 Ω dc termination is selected.

Register 27. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Do not write to these register bits.

Register 28. Loop Current Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCS2[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	LCS2[7:0]	**Loop Current Status.** Eight-bit value returning the loop current. Each bit represents 1.1 mA of loop current. 0000_0000 = Loop current is less than required for normal operation.

Register 29. Line Voltage Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LVS[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	LVS[7:0]	**Line Voltage Status.** Eight-bit value returning the loop voltage. Each bit represents 1 V of loop voltage. This register operates in on- and off-hook modes. Bit seven of this register indicates the polarity of the TIP/RING voltage. When this bit changes state, it indicates that a polarity reversal has occurred. The value returned is represented in 2s complement format. 0000_0000 = No line is connected.

Register 30. AC Termination Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				FULL2	0	0	ACIM	0
Type	R/W						R/W	

Reset settings = 0000_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5	Reserved	This bit may be written to a zero or one.
4	FULL2	Enhanced Full Scale (2x) Transmit and Receive Mode. 0 = Default 1 = Transmit/Receive 2x Full Scale This bit changes the full scale of the ADC and DAC from 0 min to +6 dBm into 600 Ω load (or 1.5 dBV into all reference impedances). When this bit is set, low loop currents may result in increased distortion.
3:2	Reserved	Always write these bits to zero.
1	ACIM	**AC Impedance Selection.** The off-hook ac termination is selected from the following: 0 = 600 Ω 1 = 270 Ω + (750 Ω || 150 nF) and 275 Ω + (780 Ω || 150 nF)
0	Reserved	Always write this bit to zero.

Register 31. DAA Control 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	FOH[1:0]		0	OHS2	0	FILT	LVFD
Type	RW				R/W		R/W	R/W

Reset settings = 0010_0000

Bit	Name	Function
7	Reserved	Always write this bit to zero.
6:5	FOH[1:0]	**Fast Off-Hook Selection.** These bits determine the length of the off-hook counter. The default setting is 128 ms. 00 = 512 ms 01 = 128 ms 10 = 64 ms 11 = 8 ms
4	Reserved	Always write this bit to zero.
3	OHS2	**On-Hook Speed 2.** This bit sets the on-hook transition speed. On-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS2 Mean On-Hook Speed** 0 Less than 0.5 ms 1 3 ms ±10% (meets ETSI standard)
2	Reserved	Always write these bits to zero.
1	FILT	**Filter Pole Selection.** 0 = The receive path has a low –3 dBFS corner at 5 Hz. 1 = The receive path has a low –3 dBFS corner at 200 Hz.
0	LVFD	**Line Voltage Force Disable.** 0 = Normal operation. 1 = The circuitry that forces the LVS register (Register 29) to all 0s at 3 V or less is disabled. The LVS register may display unpredictable values at voltages between 0 to 2 V. All 0s are displayed if the line voltage is 0 V.

Register 32. Ground Start Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						TGD	TGDE	RG
Type						R	W	W

Reset settings = 0000_0x11

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	TGD	**TIP Ground Detect.** 0 = The CO has grounded TIP, causing current to flow. When current ceases to flow, this bit returns to a one. 1 = The CO has not grounded TIP causing current to flow.
1	TGDE	**TIP Ground Detect Enable.** 0 = The external relay connecting TIP to an isolated supply is closed, enabling current to flow in TIP if the CO grounds TIP. 1 = The external relay connecting TIP to an isolated supply is open. In this state, the DAA is unable to determine if the CO has grounded TIP.
0	RG	**Ring Ground.** 0 = The external relay connecting RING to ground is closed, causing current to flow in RING. 1 = The external relay connecting RING to ground is open, not allowing current to flow in RING.

Register 33. PCM/SPI Mode Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PCML		PCME	PCMF[1:0]		0	PHCF	TRI
Type	R/W	R/W	R/W	R/W		R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	PCML	**PCM Analog Loopback.** 0 = Normal operation. 1 = Enables analog data to be received from the line, converted to digital data and transmitted across the ISOcap link. The data passes through the RX filter and is looped back through the TX filter and is transmitted back out to the line.
5	PCME	**PCM Enable (Registers 34–37 should be set before PCM transfers are enabled).** 0 = Disable PCM transfers. 1 = Enable PCM transfers.
4:3	PCMF[1:0]	**PCM Data Format.** 00 = A-Law. Signed magnitude data format (refer to Table 20 on page 39). 01 = µ-Law. Signed magnitude data format (refer to Table 19 on page 38). 10 = 8-bit linear. The top 8-bits of the 16-bit linear signal are transferred, and the bottom 8-bits are discarded (2s complement data format). 11 = 16-bit linear (2s complement data format).
2	Reserved	Always write this bit to zero.
1	PHCF	**PCM Highway Clock Format.** 0 = 1 PCLK per data bit. 1 = 2 PCLKs per data bit.
0	TRI	**Tri-state Bit 0.** 0 = Tri-state bit 0 on positive edge of PCLK. 1 = Tri-state bit 0 on negative edge of PCLK.

Register 34. PCM Transmit Start Count—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXS[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	TXS[7:0]	**PCM Transmit Start Count.** PCM Transmit Start Count equals the number of PCLKs following FSYNC before data transmission begins.

Register 35. PCM Transmit Start Count—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							TXS[1:0]	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1:0	TXS[1:0]	**PCM Transmit Start Count.** PCM Transmit Start Count equals the number of PCLKs following FSYNC before data transmission begins.

Register 36. PCM Receive Start Count—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXS[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RXS[7:0]	**PCM Receive Start Count.** PCM Receive Start Count equals the number of PCLKs following FSYNC before data reception begins.

Register 37. PCM Receive Start Count—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RXS[1:0]	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1:0	RXS[1:0]	**PCM Receive Start Count.** PCM Receive Start Count equals the number of PCLKs following FSYNC before data reception begins.

Register 38. TX Gain Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				TGA2	TXG2[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	TGA2	**Transmit Gain or Attenuation 2.** 0 = Incrementing the TXG2[3:0] bits results in gaining up the transmit path. 1 = Incrementing the TXG2[3:0] bits results in attenuating the transmit path.
3:0	TXG2[3:0]	**Transmit Gain 2.** Each bit increment represents 1 dB of gain or attenuation, up to a maximum of +12 dB and –15 dB respectively. For example: **TGA2 TXG2[3:0] Result** X 0000 0 dB gain or attenuation is applied to the transmit path. 0 0001 1 dB gain is applied to the transmit path. 0 : 0 11xx 12 dB gain is applied to the transmit path. 1 0001 1 dB attenuation is applied to the transmit path. 1 : 1 1111 15 dB attenuation is applied to the transmit path.

Register 39. RX Gain Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				RGA2	RXG2[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	RGA2	**Receive Gain or Attenuation 2.** 0 = Incrementing the RXG2[3:0] bits results in gaining up the receive path. 1 = Incrementing the RXG2[3:0] bits results in attenuating the receive path.
3:0	RXG2[3:0]	**Receive Gain 2.** Each bit increment represents 1 dB of gain or attenuation, up to a maximum of +12 dB and –15 dB respectively. For example: **RGA2** **RXG2[3:0]** **Result** X 0000 0 dB gain or attenuation is applied to the receive path. 0 0001 1 dB gain is applied to the receive path. 0 : 0 11xx 12 dB gain is applied to the receive path. 1 0001 1 dB attenuation is applied to the receive path. 1 : 1 1111 15 dB attenuation is applied to the receive path.

Register 40. TX Gain Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				TGA3	TXG3[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	TGA3	**Transmit Gain or Attenuation 3.** 0 = Incrementing the TGA3[3:0] bits results in gaining up the transmit path. 1 = Incrementing the TGA3[3:0] bits results in attenuating the transmit path.
3:0	TXG3[3:0]	**Transmit Gain 3.** Each bit increment represents 0.1 dB of gain or attenuation, up to a maximum of 1.5 dB. For example: **TGA3 TXG3[3:0] Result** X 0000 0 dB gain or attenuation is applied to the transmit path. 0 0001 0.1 dB gain is applied to the transmit path. 0 : 0 1111 1.5 dB gain is applied to the transmit path. 1 0001 0.1 dB attenuation is applied to the transmit path. 1 : 1 1111 1.5 dB attenuation is applied to the transmit path.

Register 41. RX Gain Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				RGA3	RXG3[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	RGA3	**Receive Gain or Attenuation 2.** 0 = Incrementing the RXG3[3:0] bits results in gaining up the receive path. 1 = Incrementing the RXG3[3:0] bits results in attenuating the receive path.
3:0	RXG3[3:0]	**Receive Gain 3.** Each bit increment represents 0.1 dB of gain or attenuation, up to a maximum of 1.5 dB. For example: **RGA3** **RXG3[3:0]** **Result** X 0000 0 dB gain or attenuation is applied to the receive path. 0 0001 0.1 dB gain is applied to the receive path. 0 : 0 1111 1.5 dB gain is applied to the receive path. 1 0001 0.1 dB attenuation is applied to the receive path. 1 : 1 1111 1.5 dB attenuation is applied to the receive path.

Register 42. GCI Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					GCIF[1:0]		B2D	B1D
Type					R/W		R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:2	GCIF[1:0]	**GCI Data Format.** 00 = A-Law. 01 = µ-Law. 10 = 8-bit linear. The top 8-bits of the 16-bit linear signal are transferred, and the bottom 8-bits are discarded. 11 = 16-bit linear. B1 and B2 channels are used for the 16-bits of data. Regardless of whether the DAA is set to transmit and receive in the B1 or B2 channel, both channels are used to send and receive the 16-bit linear data.
1	B2D	**Channel B2 Enable.** 0 = Channel B2 transfers are disabled. 1 = Channel B2 transfers are enabled. If 16-bit linear data format is chosen, disabling the B2 channel results in only the top 8 bits of line data being sent and received in the B1 channel.
0	B1D	**Channel B1 Enable.** 0 = Channel B1 transfers are disabled. 1 = Channel B1 transfers are enabled. If 16-bit linear data format is chosen, disabling the B1 channel results in only the bottom 8 bits of line data being sent and received in the B2 channel.

Register 43. Line Current/Voltage Threshold Interrupt

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CVT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	CVT[7:0]	**Current/Voltage Threshold.** These bits determine the threshold at which an interrupt is generated from either the LCS or LVS register. This interrupt can be generated to occur when the line current or line voltage rises above or drops below the value in the CVT[7:0] register.

Register 44. Line Current/Voltage Threshold Interrupt Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CVI	CVS	CVM	CVP
Type					R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	CVI	**Current/Voltage Interrupt.** 0 = The current/voltage threshold has not been crossed. 1 = The current/voltage threshold is crossed. If the CVM and INTE bits are set, a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. Once set, this bit must be written to 0 to be cleared.
2	CVS	**Current/Voltage Select.** 0 = The line current shown in the LCS2 register is used to generate an interrupt. 1 = The line voltage shown in the LVS register is used to generate an interrupt.
1	CVM	**Current/Voltage Interrupt Mask.** 0 = The current/voltage threshold being triggered does not cause a hardware interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = The current/voltage threshold being triggered causes a hardware interrupt on the AOUT/$\overline{\text{INT}}$ pin.
0	CVP	**Current/Voltage Interrupt Polarity.** 0 = The current/voltage threshold is triggered by the absolute value of the number in either the LCS2 or LVS register falling below the value in the CVT[7:0] register. 1 = The current/voltage threshold is triggered by the absolute value of the number in either the LCS2 or LVS register rising above the value in the CVT[7:0] register.

Register 45. Programmable Hybrid Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB1[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB1[7:0]	**Programmable Hybrid Register 1.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 46. Programmable Hybrid Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB2[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB2[7:0]	**Programmable Hybrid Register 2.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the second tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 47. Programmable Hybrid Register 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB3[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB3[7:0]	**Programmable Hybrid Register 3.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the third tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 48. Programmable Hybrid Register 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB4[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB4[7:0]	**Programmable Hybrid Register 4.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the fourth tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 49. Programmable Hybrid Register 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB5[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB5[7:0]	**Programmable Hybrid Register 5.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the fifth tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 50. Programmable Hybrid Register 6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB6[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB6[7:0]	**Programmable Hybrid Register 6.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the sixth tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 51. Programmable Hybrid Register 7

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB7[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB7[7:0]	**Programmable Hybrid Register 7.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the seventh tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 52. Programmable Hybrid Register 8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB8[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB8[7:0]	**Programmable Hybrid Register 8.** These bits can be programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the eighth tap in the eight-tap filter. When this register is set to all 0s, this filter stage does not have an effect on the hybrid response. See the section entitled "5.28. Transhybrid Balance" on page 32 for more information on selecting coefficients for the programmable hybrid.

Register 53-58. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Do not write to these register bits.

Register 59. RX Gain Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	RG1	GCE	0
Type						R/W	R/W	

Reset settings = xxxx_xxxx

Bit	Name	Function
7:3	Reserved	Always write these bits to zero.
2	RG1	**Receive Gain 1.** This bit enables receive path gain adjustment. 0 = No gain applied to hybrid, full scale RX on line = 0 dBm. 1 = 1 dB of gain applied to hybrid, full scale RX on line = –1 dBm.
1	GCE	**Guarded Clear Enable.** This bit (in conjunction with the R2 bit set to 1) enables the Si3050 to meet BT's Guarded Clear Spec (B5 6450, Part 1: 1993, Section 15.4.3.3). With these bits set, the DAA will draw approximately 2.5 mA of current from the line while on-hook. 0 = Default, DAA does not draw loop current. 1 = Guarded Clear enabled, DAA draws 2.5 mA while on-hook to meet Guarded Clear requirement.
0	Reserved	Always write this bit to zero.

APPENDIX—IEC/UL60950 3RD EDITION

Introduction

Although designs using the Si3011 comply with IEC/UL60950 3rd Edition and pass all overcurrent and overvoltage tests, there are still several issues to consider.

Figure 48 shows two designs that can pass the IEC/UL60950 overvoltage tests and electromagnetic emissions. The top schematic shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 48 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, it is important to remember that compliance to IEC/UL60950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage tests applies to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, must be considered during the design stages. Consult with your professional testing agency during the design of the product to determine which tests apply to your system.

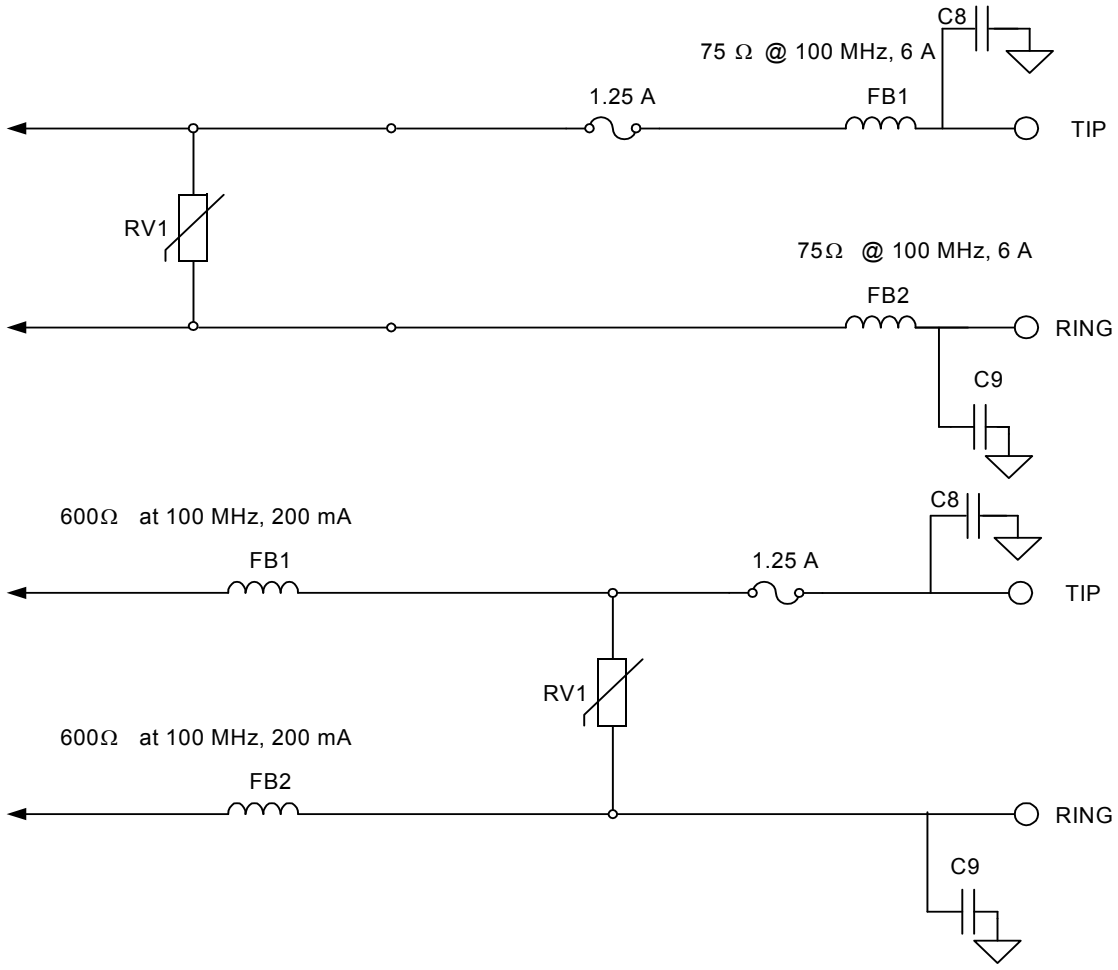


Figure 48. Circuits that Pass All Overvoltage Tests

7. Pin Descriptions: Si3050

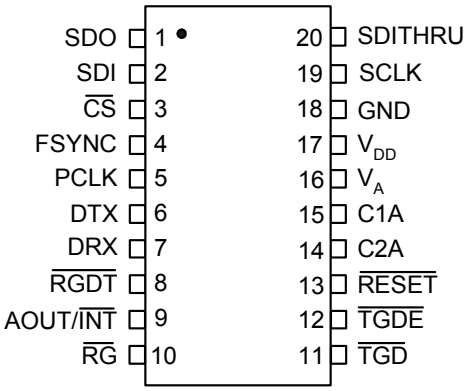


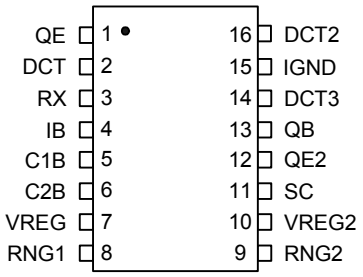
Table 23. Si3050 Pin Descriptions

Pin #	Pin Name	Description
1	SDO	**Serial Port Data Output.** Serial port control data output.
2	SDI	**Serial Port Data Input.** Serial port control data input.
3	$\overline{CS}$	**Chip Select Input.** An active low input control signal that enables the SPI Serial port. When inactive, SCLK and SDI are ignored and SDO is high impedance.
4	FSYNC	**Frame Sync Input.** Data framing signal that is used to indicate the start and stop of a communication/data frame.
5	PCLK	**Master Clock Input.** Master clock input.
6	DTX	**Transmit PCM or GCI Highway Data Output.** Outputs data from either the PCM or GCI highway bus.
7	DRX	**Receive PCM or GCI Highway Data Input.** Receives data from either the PCM or GCI highway bus.
8	$\overline{RGDT}$	**Ring Detect Output.** Produces an active low rectified version of the ring signal.
9	AOUT/$\overline{INT}$	**Analog Speaker Output/Interrupt Output.** Provides an analog output signal for driving a call progress speaker in AOUT mode. Alternatively, this pin can be set to provide a hardware interrupt signal.
10	$\overline{RG}$	**Ring Ground Output.** Control signal for ring ground relay. Used to support ground start applications.

Table 23. Si3050 Pin Descriptions (Continued)

Pin #	Pin Name	Description
11	$\overline{\text{TGD}}$	**TIP Ground Detect Input.** Used to detect current flowing in TIP for supporting ground start applications.
12	$\overline{\text{TGDE}}$	**TIP Ground Detect Enable Output.** Control signal for the ground detect relay. Used to support ground start applications.
13	$\overline{\text{RESET}}$	**Reset Input.** An active low input that is used to reset all control registers to a defined, initialized state. Also used to bring the Si3050 out of sleep mode.
14	C2A	**Isolation Capacitor 2A.** Connects to one side of the isolation capacitor C2. Used to communicate with the line-side device.
15	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor C1. Used to communicate with the line-side device.
16	V_A	**Regulator Voltage Reference.** This pin connects to an external capacitor and serves as the reference for the internal voltage regulator.
17	V_{DD}	**Digital Supply Voltage.** Provides the 3.3 V digital supply voltage to the Si3050.
18	GND	**Ground.** Connects to the system digital ground.
19	SCLK	**Serial Port Bit Clock Input.** Controls the serial data on SDO and latches the data on SDI.
20	SDITHRU	**SDI Passthrough Output.** Cascaded SDI output signal to daisy-chain the SPI interface with additional devices.

8. Pin Descriptions: Si3011



Pin #	Pin Name	Description
1	QE	**Transistor Emitter.** Connects to the emitter of Q3.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	RX	**Receive Input.** Serves as the receive side input from the telephone network.
4	IB	**Internal Bias.** Provides a bias voltage to the device.
5	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side device.
6	C2B	**Isolation Capacitor 2B.** Connects to one side of isolation capacitor C2. Used to communicate with the system-side device.
7	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
8	RNG1	**Ring 1.** Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the DAA.
9	RNG2	**Ring 2.** Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the DAA.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	SC	**SC Connection.** Enables external transistor network. Should be tied through a 0 Ω resistor to I_{GND}.
12	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
13	QB	**Transistor Base.** Connects to the base of transistor Q4.

Pin #	Pin Name	Description
14	DCT3	**DC Termination 3.** Provides dc termination to the telephone network.
15	IGND	**Isolated Ground.** Connects to ground on the line-side interface.
16	DCT2	**DC Termination 2.** Provides dc termination to the telephone network.

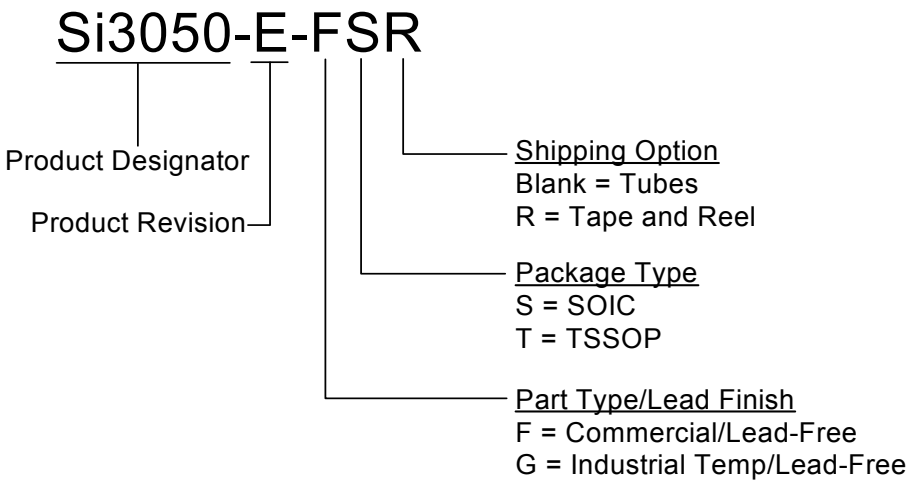
9. Ordering Guide

Chipset	Region	System-side (TSSOP)	Line-side (SOIC)	Line-side (TSSOP)	Pb-Free and RoHS-Compliant	Temperature
Si3050+Si3011	FCC/TBR21	Si3050-E-FT	Si3011-F-FS	Si3011-F-FT	Yes	0 to +70 °C
Si3050+Si3011	FCC/TBR21	Si3050-E-GT	Si3011-F-GS	Si3011-F-GT	Yes	–40 to +85 °C
Note: Refer to "10. Product Identification" on page 96 for more information on part naming conventions.						

10. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



11. Package Outline: 20-Pin TSSOP

Figure 49 illustrates the package details for the Si3050. Table 24 lists the values for the dimensions shown in the illustration.

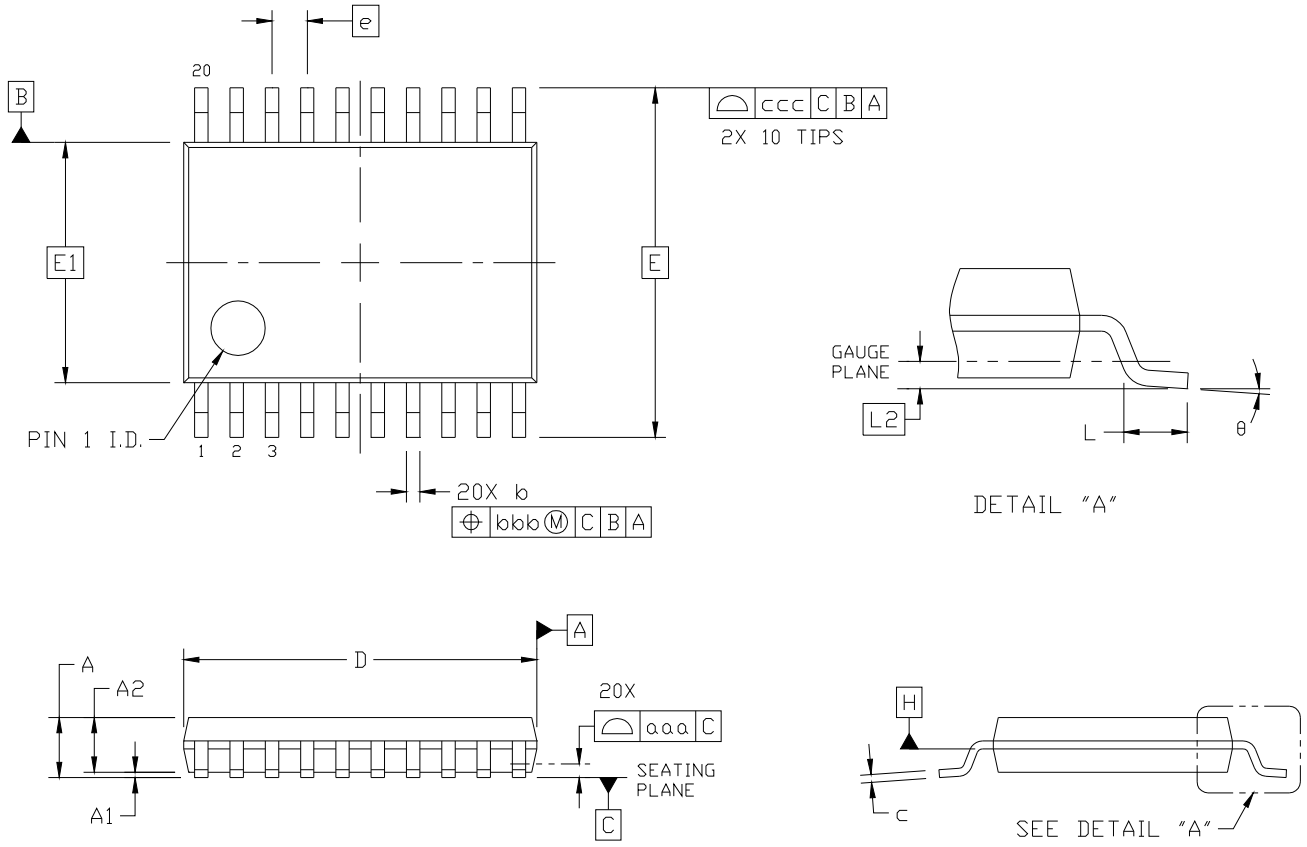


Figure 49. 20-Pin Thin Shrink Small Outline Package (TSSOP)

Table 24. 20-Pin TSSOP Package Diagram Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	6.40	6.50	6.60
E		6.40 BSC	
E1	4.40	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L2		0.25 BSC	
θ	0°	—	8°
aaa		0.10	
bbb		0.10	
ccc		0.20	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

12. Package Outline: 16-Pin SOIC

Figure 50 illustrates the package details for the Si3011. Table 25 lists the values for the dimensions shown in the illustration.

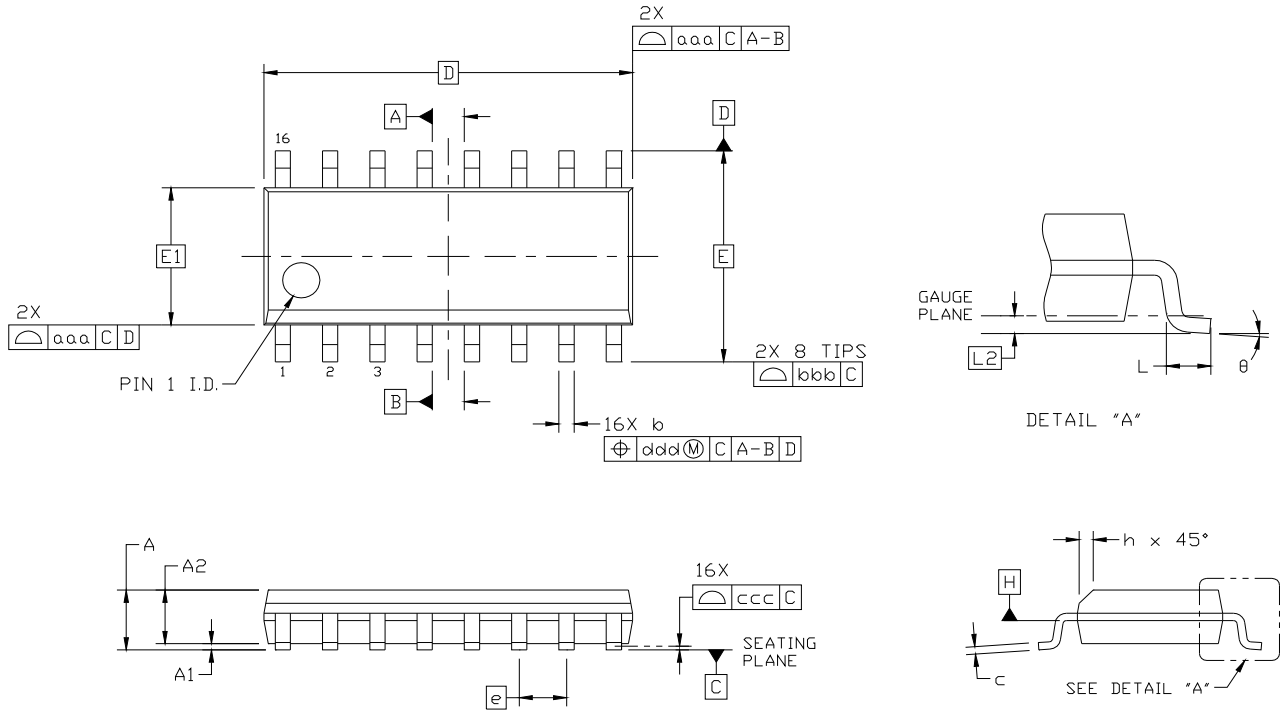


Figure 50. 16-Pin Small Outline Integrated Circuit (SOIC) Package

Table 25. 16-Pin SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

13. Package Outline: 16-Pin TSSOP

Figure 51 illustrates the package details for the Si3011. Table 26 lists the values for the dimensions shown in the illustration.

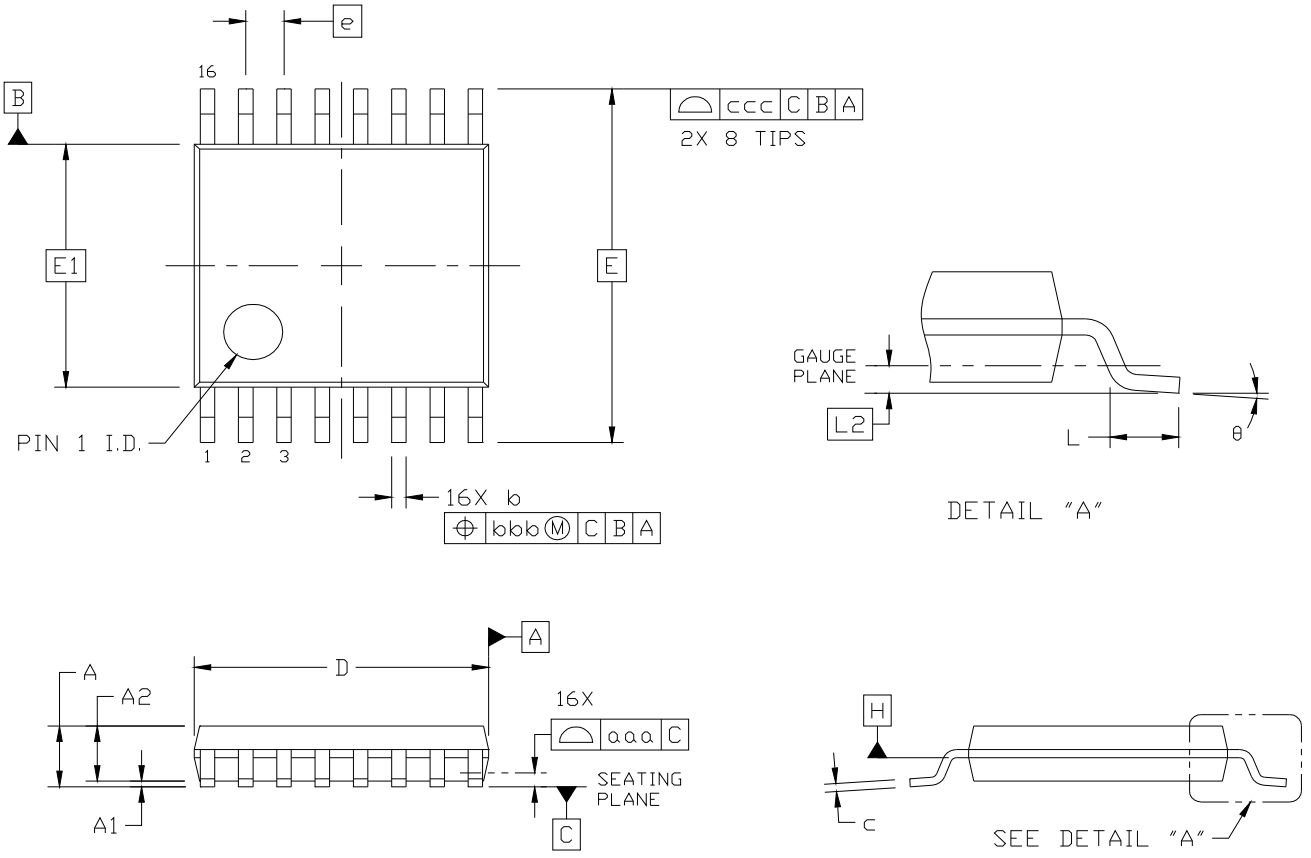


Figure 51. 16-Pin Thin Shrink Small Outline Package (TSSOP)

Table 26. 16-Pin TSSOP Package Diagram Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E	6.40 BSC		
E1	4.40	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.20		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

SILICON LABS Si3050 SUPPORT DOCUMENTATION

- AN16: Multiple Device Support
- AN17: Designing for International Safety Compliance
- AN30: Ground Start Implementation with Silicon Laboratories' DAAs
- AN67: Layout Guidelines
- AN72: Ring Detection/Validation with the Si305x DAAs
- AN77: Silicon DAA Software Guidelines (Si3050)
- AN81: Emissions Design Considerations
- AN84: Digital Hybrid with the Si305x DAAs

Note: Refer to www.silabs.com for a current list of support documents for this chipset.

NOTES:

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

- Updated Deep Sleep Total Supply Current from 1.0 to 1.3 mA typical
- Updated package pictures
- Removed all SPIM references (SPIM bit is never present in any Si3050 device).
- Removed SnPb package options
- Minor typo corrections

Revision 1.1 to Revision 1.11

- The internal System-Side Revision value (REVA[3:0] in Register 11) has been incremented by one for Si3050 revision E.

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