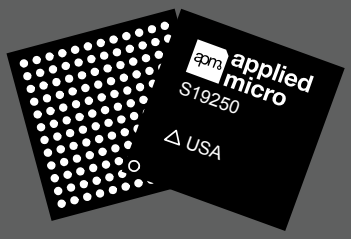
S19250 | Serial OC-192 - to - 16bit Transceiver

PRODUCT BRIEF



The S19250 MUX/DeMux chip is a fully integrated serialization/de-serialization SONET STS-192/10 GB Ethernet/Fiber Channel transceiver with Electronic Dispersion Compensation (EDC). This device can be used to compensate channel impairments caused by Single Mode Fiber (SMF) and copper medium. The chip performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/SDH, 10 Gigabit Ethernet (10 GbE) and 10 Gigabit Fibre Channel (10 G FC) transmission standards. The first figure shows a typical network application. The other application block diagrams are shown in the remaining figures

Features

- Operational from 9.9 Gbps to 11.32 Gbps
- Built-In Self Test (BIST) with Error Counter
- On-chip High-Frequency PLLs for Clock Recovery and Clock Gen.
- 16-bit LVDS Parallel Data Path
- TX and RX Lock Detect Indicators
- Reference Loop Timing Modes
- Line and Diagnostic Loopback Mode for Faulty Node Identification
- -40°C to 85°C Industrial Temperature Range
- Supports MDIO, I2C and SPI serial interface
- Complies with applicable OIF SFI-4 Phase 1, Telcordia/ITU-T, 300-pin MSA, IEEE 802.3ae and XFP MSA Standards
- 2000 V ESD rating, 1500 V on high speed inputs
- 17 x 17 mm, 1.0 mm pitch package with RoHS compliant lead free option. Pin Compatible with S19235/S19237.
- 1.1 W typical
- JTAG support

Applications

- SONET/SDH and 10GbE-Based Transmission Systems & Modules
- Section Repeaters
- Add Drop Multiplexers (ADM)
- Broad-Band Cross-Connects
- Fiber Optic Test Equipment

Overview

On-chip clock synthesis PLL components are contained in the S19250 chip, allowing the use of a slower external transmit clock reference. The chip can be used with 155.52 MHz or 622.08 MHz (or equivalent FEC/10 GbE/10 G FC rates) reference clocks, in support of existing system clocking schemes. The low-jitter LVDS interface guarantees compliance with the bit-error rate requirements of the Telcordia and ITU-T standards.

The S19250 transceiver incorporates SONET/SDH/10 GbE/10 G Fibre Channel serialization and deserialization functions. This chip can be used to implement the front end of SONET/10 GbE/10 G Fibre Channel equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial, and serial-to-parallel conversion and system timing.

Transmitter Features

- Reference Clock Frequency Selection: Divide by 16, 64 or 66 of the TX rate; for example (644.53 MHz, 161.13 MHz or 156.25 MHz) for 10GE TX rate
- Internal, Self-Initializing FIFO to Decouple Transmit Clocks
- Programmable TSD Output Differential Swing
- Duo Binary Encoding
- Transmitter De-Emphasis

Receiver Features

- LOS/RSSI
- ISI compensation. Tolerates additional 350 ps/nm of chromatic dispersion with an OSNR penalty of 1.0dB over a traditional demux
- Tolerates up to 34" of Standard FR-4 Material
- Adaptive Post-Amplifier Offset Adjust
- Phase Adjust of -0.11 to +0.085 UI
- Reference Clock Frequency Selection: Divide by 16, 64 or 66 of the RX rate; for example (644.53 MHz, 161.13 MHz or 156.25 MHz) for 10GE RX rate
- Capability to Interface with Single-Ended or Differential TIAs (Center Tap Option)
- Input Sensitivity of 10 mV p-p (one wire or two wire) at 10^{-12} BER

S19250 System Block Diagram

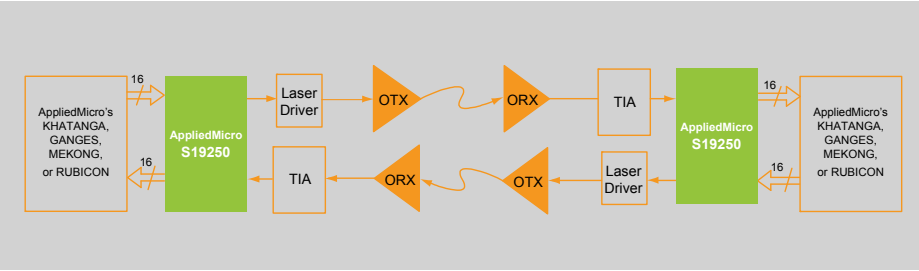


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Figure 1. Mid-Plane Application Block Diagram

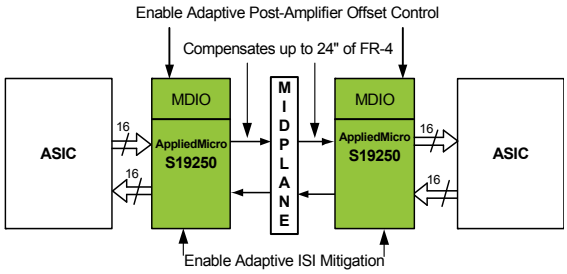

Figure 2. XFP Application Block Diagram

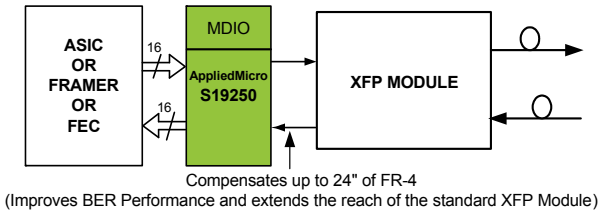

Figure 3. 300 MSA Application Block Diagram