

The **S3485** SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET multi-rate interface device. The AppliedMicro receives a scrambled Non-Return-to-Zero (NRZ) signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with the SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 transmission standards. The device is suitable for SONET-based WDM applications. The diagram in figure below shows a typical network application.

Features

- 345 mW typical power
- CMOS 0.13 micron technology
- Complies with Telecordia specifications
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports the following rates:
 - OC-48 with or w/o FEC (2.488-2.67 Gbps)
 - OC-24 with or w/o FEC (1.244-1.335 Gbps)
 - OC-12 with or w/o FEC (622.8-667.5 Mbps)
 - OC-3 with or w/o FEC (155.52-166.87 Mbps)
 - HDTV (1.485 Gbps)
 - D1 Video (1.38 Gbps)
 - Fibre Channel (1062.5 Mbps)
 - Fibre Channel/4 (265.5 Mbps)
 - 2 x Fibre Channel (2.125 Gbps)
 - Gigabit Ethernet (1.25 Gbps)
 - DTV (143.18 Mbps)
 - ESCON (200 Mbps)
- Reference frequency of 155.52 MHz (for OC-48)
- Interface to LVDS and LVCMOS logic
- 4-bit LVDS data path
- 121 pin PBGA package with Green/RoHS compliant lead free option
- Diagnostic and line loopback mode
- Supports line timing
- Lock detect Output/Signal Detect Inputs
- Dual 1.2 V and 1.8 V supply
- Built-in self test

Applications

- Wavelength Division Multiplexing (WDM)
- SONET/SDH-transmission systems
- Section Tepeaters & ADMs
- Broad-band cross-connects
- Fiber optic terminators/test equipment

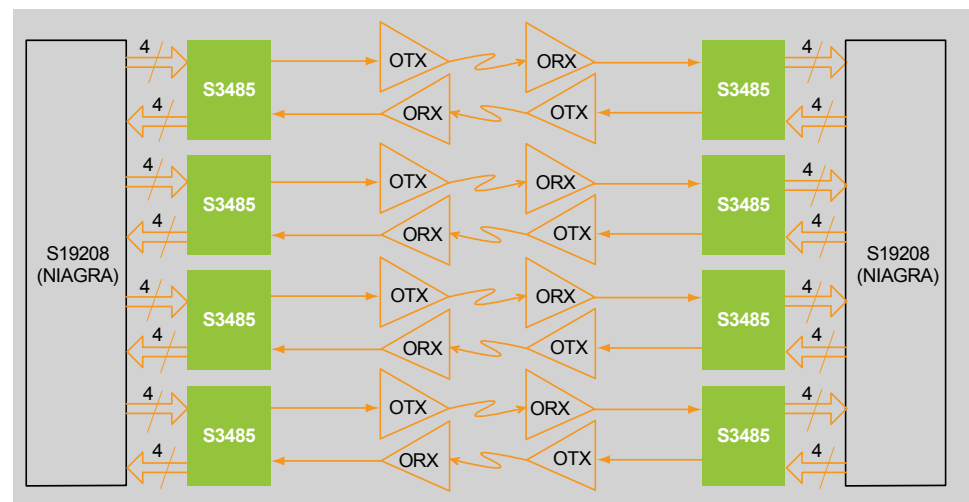
Overview

On-chip clock synthesis is performed by the high-frequency Phase-Lock Loop (PLL) on the S3485 transceiver chip, allowing the use of a slower external transmit clock reference. The chip can be used with a divide by 16 reference clock in support of existing system clocking schemes.

The low-jitter parallel LVDS interface is compliant with the bit-error rate requirements of the Telecordia and ITU-T standards. The S3485 is packaged in a 121 PBGA offering designers a small package outline.

The S3485 transceiver implements SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 serialization/deserialization and transmission functions. This chip can be used to implement the front end of SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of data stream management and clock distribution throughout the front end.

S3485 System Block Diagram



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