1+1 Protection without Relays Using Cortina Systems® LXT380/1/4/6/8 Hitless Protection Switching

Application Note

10 August 2007

Document Number 249464

Revision 2.0

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Revision History

Revision 2.0 Revision Date: 10 August 2007
First release of this document from Cortina Systems, Inc.

Revision 001 Revision Date: August 2001
Initial release.

1.0 Introduction - 1+1 Hitless Protection Switching

Today's telecommunications customers and international regulatory bodies demand an extremely high quality of service with little or no periods of service failure or down time. If your goal is to provide your customers with equipment that has an extremely high availability, then 1+1 protection is the method to use for T1/E1/J1 line interface cards.

In a 1+1 protection scheme, each primary line card has a backup (or protection) board that can be switched into the circuit path while the primary line card is isolated in case the primary line card fails. This is accomplished by having a control circuit card that constantly monitors each primary line card and preforms switching tasks when necessary. Switching takes place in a protection switching matrix traditionally constructed with mechanical relays as switching elements.

From an architectural standpoint, the relay switching matrix is easy to visualize but comes with some inherent drawbacks:

- **Parts Count**

  As an example, if each line card has 8 T1/E1/J1 bidirectional ports and is implemented with a 1+1 protection scheme, a total of 8*2 = 16 DPDT relays would be required.

- **Space**

  The typical size for a DPDT telco signal relay is 15 x 7.5 mm. This requires a board area of 3600 sq. mm. at a parts density of 50%.

- **Switching Speed**

  The typical switching time for a telco relay, including debounce time, is about 3.5 ms. On a T1 link running at 1.544 MHz, this corresponds to over 5000 bits of data. This is well over the time required to cause a loss of frame sync. On E1 links running at 2.048 MHz, the problem is even worse. Since re-framing can take up to 193 frames, a significant degradation in performance is realized.

- **Power**

  Eliminating the need for 16 relays and the associated driver circuitry reduces the power requirements for the system.

As can be seen from the previous discussion, relay based protection schemes give rise to a number of issues. The following sections introduce a scheme designed around Cortina Systems® LIUs with fast tri-stating transmit drivers utilizing Hitless Protection Switching (HPS). HPS protects the system from single board failures by utilizing on-chip fast solid state tri-state drivers to switch in the back-up board before a loss of frame sync. This eliminates the need for mechanical relays and enhances the overall reliability of the system.

2.0 1+1 Implementation

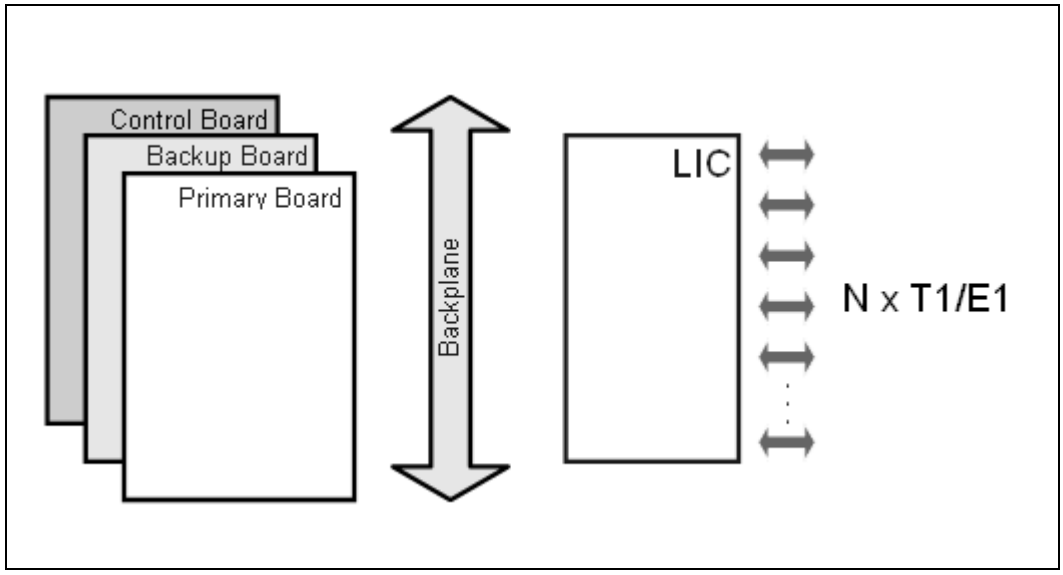
2.1 Architecture

Figure 1 represents the typical architecture found in most T1/E1/J1 systems with redundancy protection. This approach is common in rack based systems where several boards share a common backplane. The primary and back-up boards are identical in function and have access to the same data and control signals. A separate Line Interface Card (LIC) houses the shared connectors and passive interface components between primary and back-up boards. This LIC approach reduces the system cost by reducing the number of total system components through avoiding duplication. It also offers a simple mechanism for supporting different connector and line impedance options. An independent control board supervises the system operation and selects the primary or back-up board for use. Other boards may also exist depending on system functionality.

In a redundancy protection application it is essential that the board in standby mode does not alter the T1/E1/J1 signal from its design standard. Performance requirements such as pulse shape and return loss must still be met.

The LXT38x LIU series of T1/E1/J1 LIUs include several features that ease the design of redundancy protection systems. These features guarantee excellent analog performance and minimize switching errors and bit errors.

Figure 1 Redundancy Protection



2.1.1 LXT38x T1/E1/J1 LIU Family

The LXT38x LIU family of 3.3 V T1/E1/J1 LIUs is comprised of the following members:

- LXT380 LIU: Octal E1 analog front-end with clock and data recovery and hardware or software modes.
- LXT381 LIU: Octal E1 analog front-end with data recovery mode only. Only hardware mode is available.

- LXT384 LIU: Octal T1/E1/J1 LIU with digital jitter attenuation. Both hardware and software modes are available.
- LXT386 LIU: Quad T1/E1/J1 LIU with digital jitter attenuation. Both hardware and software modes are available.
- LXT388 LIU: Dual T1/E1/J1 LIU with dual digital jitter attenuation. Both hardware and software modes are available.

Some features available in these devices ease the development of redundant protection systems:

- Output tristating by freezing the TCLK signal
- Fast output tristating by using the OE pin
- Software controllable output driver tristate by using the OE register
- High receiver input impedance of 70 kΩ typ
- Constant delay jitter attenuator (LXT384/6/8 LIUs only)

The driver tristate feature allows the designer to connect the redundant driver output in parallel with the primary driver when one of them is tristated. Similarly, because the receiver impedance is very high, two receivers can be connected in parallel.

The following sections will describe the “standard” HPS 3-board solution, an HPS solution with one of the boards unpowered, a 2-board HPS solution and a hot swappable HPS solution.

All of the circuits described in this Application Note were built and tested using the evaluation boards for the LXT38x LIU.

2.1.2 Design Considerations

This section contains some design considerations to account for in all LIU designs.

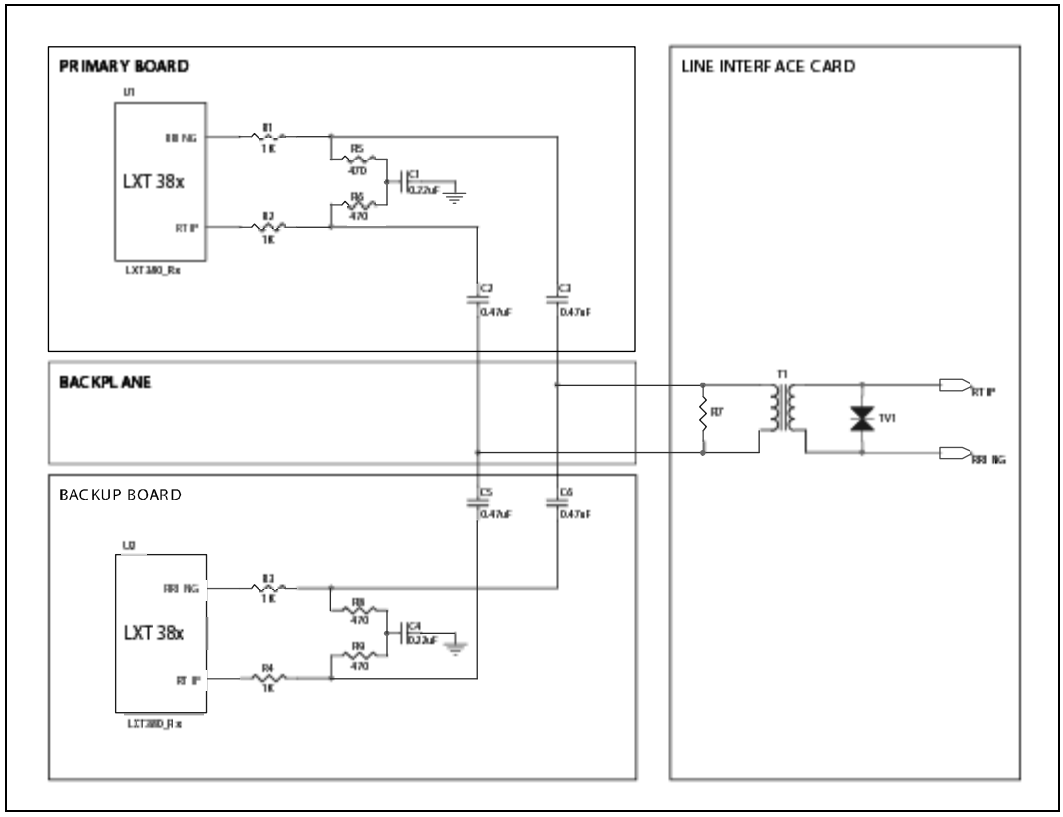
- **Minimize trace/cable lengths.** Long cable lengths may reduce the output amplitude. In the experiments conducted, the cable connecting the primary, back-up and LIC boards did not exceed 25 cm. If longer cables are to be used, the transmit series resistors (R10 – R13) may need to be reduced to compensate for the loss in amplitude.
- **Minimize parasitic capacitance.** High parasitic capacitance will affect both the pulse shape and the return loss performance. The protection components chosen for this Application Note have a very low capacitance at the nominal operating voltage. Note that long cable lengths also add to the total parasitic capacitance. In some cases, the transmit capacitor (C4) may have to be adjusted to optimize pulse shape and return loss performance.
- **Surge immunity.** The protection elements recommended in Figure 2 and Figure 3 are sufficient for compliance with IEC 61000-4-5 (EN-6100-4-5) with up to 24 A peak current on a 1.2/50 µsec surge. If additional protection is required, a different line TVS may be necessary.
- **Place the TVS close to the connector.** Surge protection should be placed as close as possible the source of the disturbance, that is, the connector.
- **Include TVS protection in the power supply.** The protection diodes (D1 – D8) will couple current to the power supply (TVcc) in the event of a lightning surge. To protect other circuits on the board, a 3.3 V TVS should be included in the power supply. A TVS suitable for this application is the SMLVT 3V3. A similar device for 5 V should be selected if TVcc is 5 V.

- **Avoid routing transmit and receive signals parallel to each other.** This layout practice minimizes cross-talk. If you must cross these signals, do it at right angles.
- **Avoid routing digital signals near analog signals.** This is especially important near the receiver inputs as the cross-talk can induce bit errors.
- **EMI filtering.** Some designs may require EMI filtering to meet emissions standards. In these applications, common mode chokes may be added near the connectors.
- **When the back-up board is powered down.** Ensure that the OE pin is held low.
- **When hot swapping boards.** Ensure linear tracking of VCC and TVCC supplies during power up. Use a Schottky diode to maintain VCC - TVCC tracking. See Figure 21.

2.2 Receive Line Interface

Figure 2 shows the recommended receive configuration for redundancy protection. Only one channel is shown for simplicity.

Figure 2 Receive Interface Circuit



The Line Interface Card (LIC) contains T1, the receive transformer, the termination resistor R7 and a transient voltage suppressor TV1. The transient voltage suppressor is recommended in applications where there are stringent surge immunity requirements. In the primary and back-up boards, the series 1 kΩ resistors further improve the surge and ESD immunity. The primary and back-up boards are connected through the backplane. Table 1 and Table 2 lists the components that were used in tests for both Coaxial and Twisted Pair Cable (TWP).

Table 1 Component List (LXT380/1 LIU)

Component	Coax Cable (75 Ω)	TWP Cable (120 Ω)
R7	90.9 Ω ± 1%	162 Ω ± 1%
TV1	LC03-6, Semtech* (or equivalent)	
T1	S553-6500-55, Belfuse* (or equivalent) 1:1	

Table 2 Component List (LXT384/6/8 LIU)

Component	T1 TWP Cable	E1 Coax Cable	E1 TWP Cable
R7	26.1 Ω ± 1%	19.6 Ω ± 1%	32.4 Ω ± 1%
TV1	LC03-6, Semtech* (or equivalent)		
T1	S553-6500-55, Belfuse* 1:2 (or equivalent)		

2.3 Transmit Line Interface

Figure 3 LXT38x LIU Transmit Interface Circuit

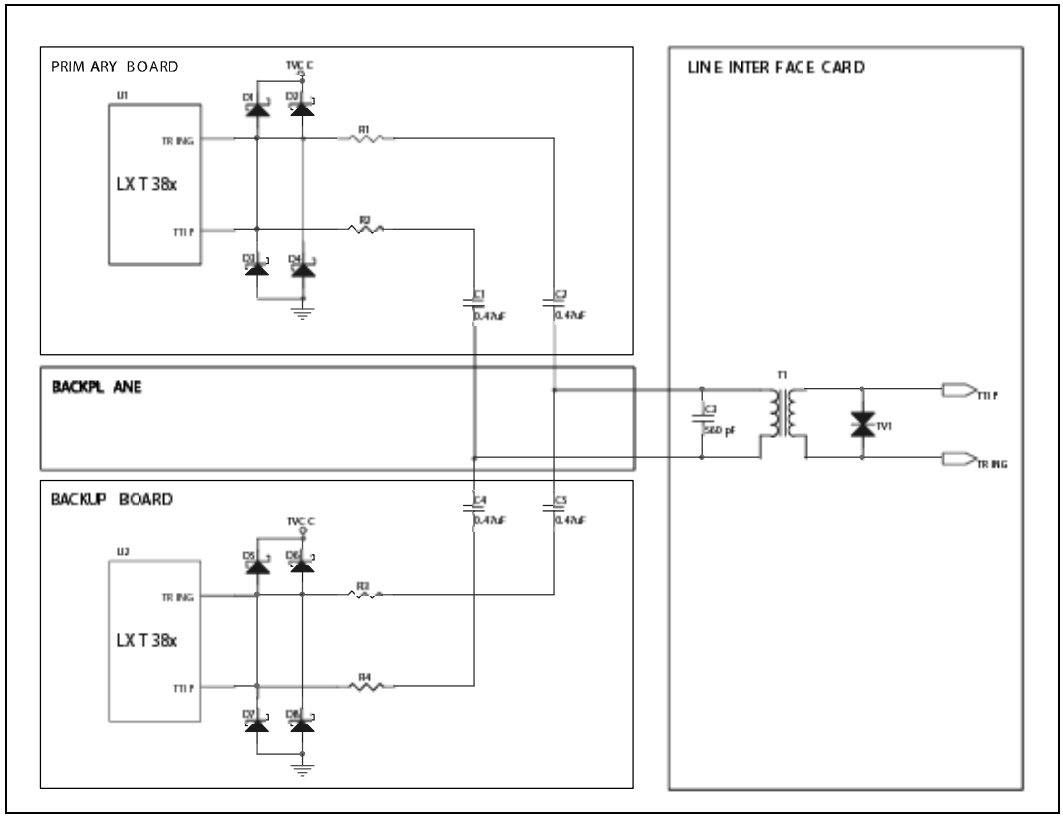


Figure 3 represents the recommended transmit line interface. The LIC contains the 1:2 transmit transformer and 560 pF pulse shaping capacitor. TV1 is included as a first level of surge (lightning) protection complimented by D1-8. Resistors R1-4 are the same value for both coaxial and TWP operation. Primary and backup boards are connected in the backplane and are capacitively coupled.

When tristated, the output driver impedance is very high and will not affect the pulse shaping in the primary board.

Table 3 lists the components that were used in tests for both E1 75 Ω coaxial and 120 Ω TWP cable and for T1 100 Ω TWP Cable.

Table 3 Component List (LXT380/1/4/6/8 LIU)

Component	E1 (Coax Cable or TWP Cable)	T1 (TWP Cable)
D1 – D8	MBR0540T1, Motorola (or equivalent)	
TV1	LC03-6, Semtech* (or equivalent)	
T1	S553-6500-55, Belfuse* (or equivalent) 1:2	
R1-4	11 Ω ± 1%	9.1 Ω ± 1% (see note 1)

Note: 1. Resistor values shown for T1 (100 Ω termination) are for TVCC at 5.0 V. For TVCC at 3.3 V, R1-4 are 0 Ω

3.0 Test Results

The circuits in Figure 2 and Figure 3 were tested using the LXD380/1 and the LXD384/6/8 demo boards. The following performance parameters were tested for both coaxial and twisted pair cable where applicable:

- Receiver sensitivity per ITU-T G703
- Pulse template per ITU-T G703
- Receive return loss per ITU-T G703
- Transmit return loss per ETSI ETS 300 166

3.1 LXT380/1 LIU Test Results

3.1.1 Receiver Sensitivity

The devices were able to correctly recover data with cable attenuation up to 12 dB at 1.024 MHz, exceeding the 6 dB minimum limit set by ITU-T G703.

3.1.2 Pulse Template

Figure 4 and Figure 5 represent the output pulses obtained for twisted pair and coaxial cable. During the tests, the backup boards were powered and the output drivers set to tristate mode.

Figure 4 Twisted Pair cable Output

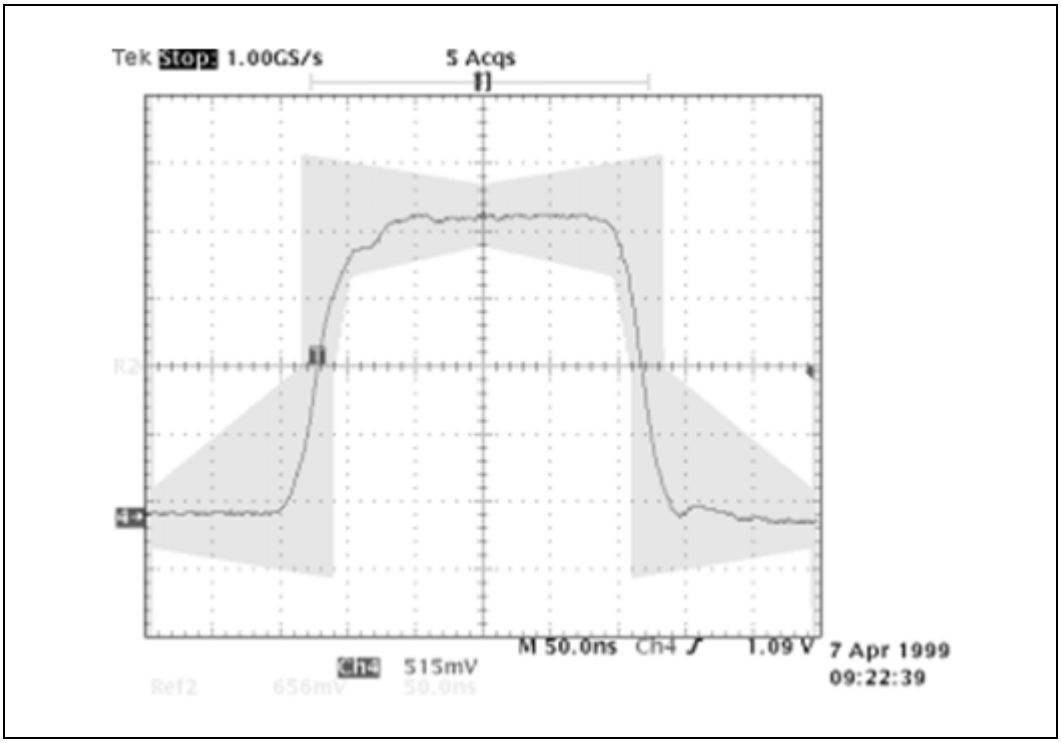
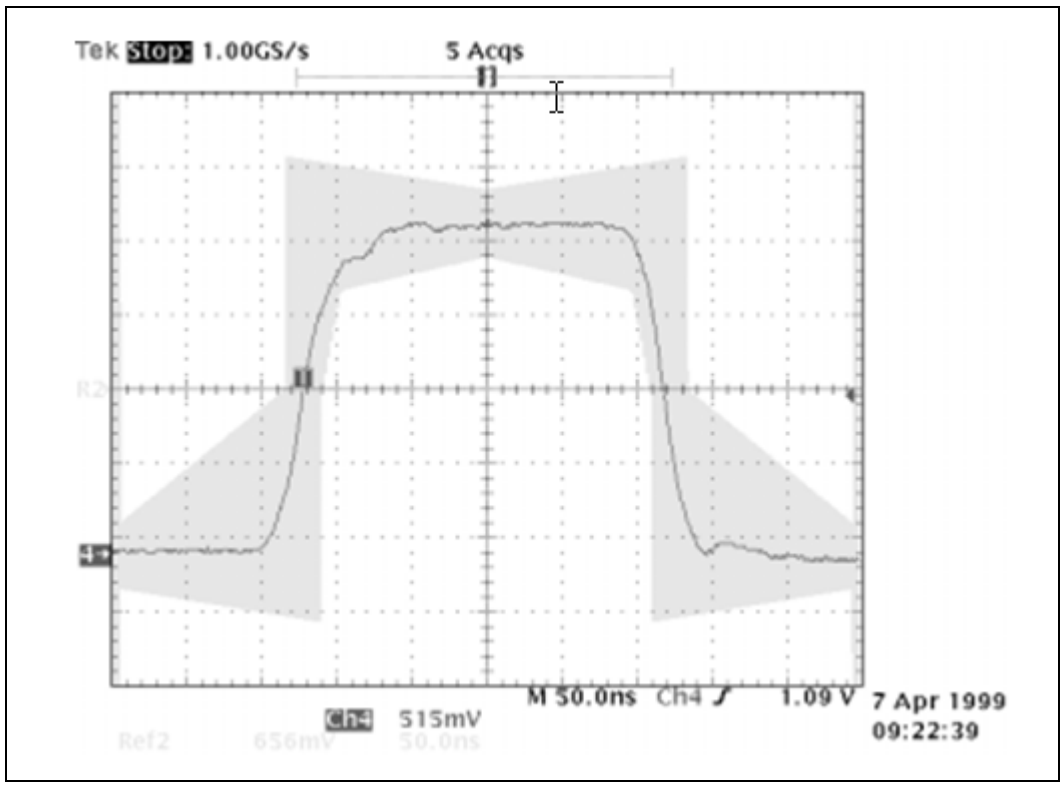


Figure 5 Coaxial Cable Output



3.1.3 Receive Return Loss

Figure 6 and Figure 7 show the measured receiver return loss for both coaxial and twisted pair cable. The results are compared against G703 minimum requirements.

Figure 6 LXT380/1 LIU Rx Return Loss, Twisted Pair Cable

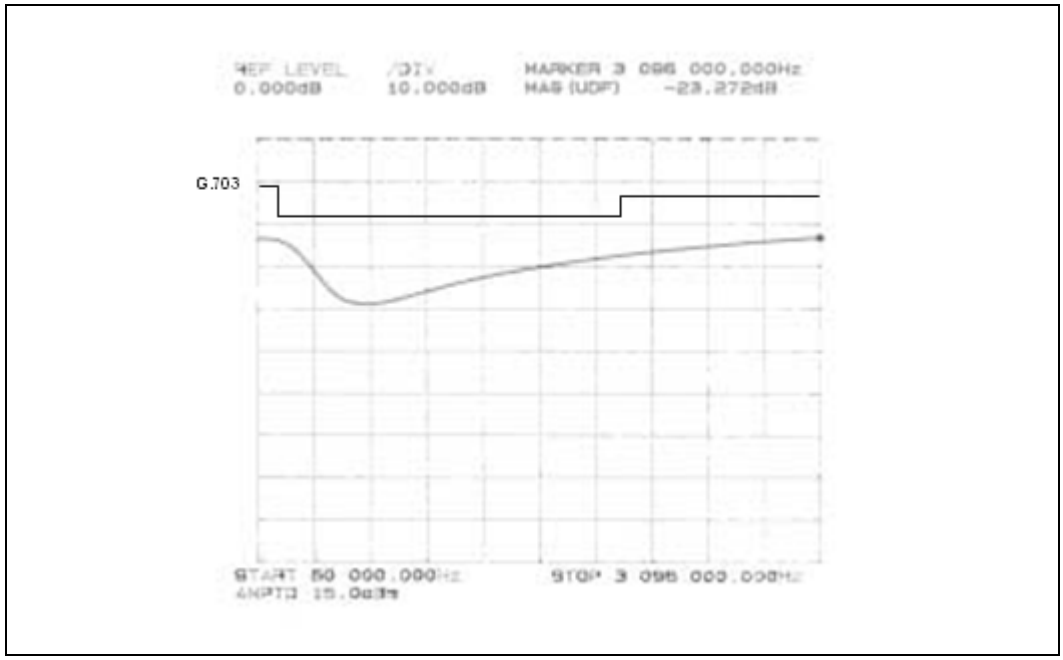
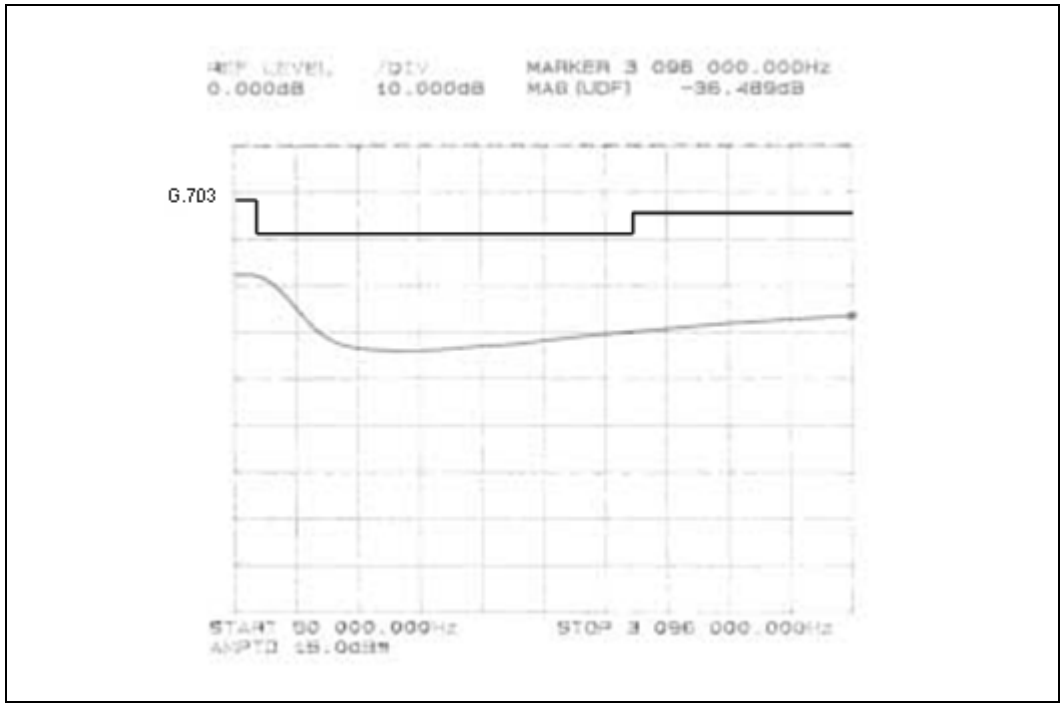


Figure 7 LXT380/1 LIU Rx Return Loss, Coaxial Cable



3.1.4 Transmit Return Loss

Figure 8 and Figure 9 show the measured transmit return loss for both coaxial and twisted pair cable.

The results are compared against ETSI ETS 300 166 requirements.

Figure 8 LXT380/1 LIU Tx Return Loss, Twisted Pair Cable

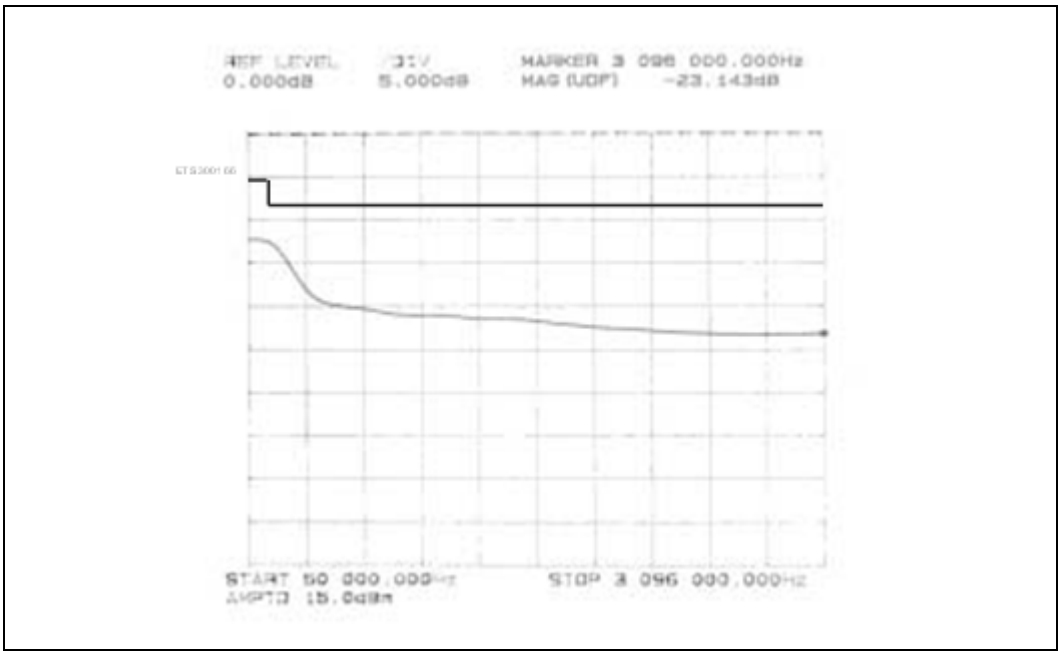
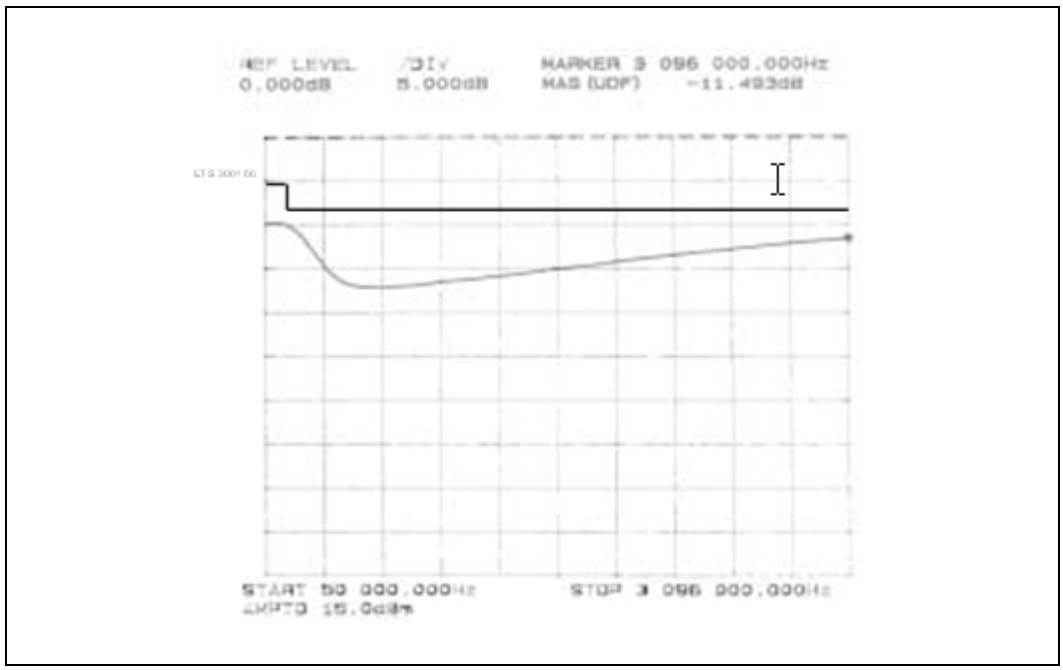


Figure 9 LXT380/1 LIU Tx Return Loss, Coaxial Cable



3.2 LXT384/6/8 LIU Test Results

3.2.1 Receiver Sensitivity

The devices were able to correctly recover data with cable attenuation up to 12 dB at 772 kHz for T1 and 1024 kHz for E1. For T1, this figure exceeds the requirements in ANSI T1.102 of 3 dB (655 feet of cable) at 772 kHz. For E1, the figure exceeds the 6 dB minimum limit set (at 1024 kHz) by ITU-T G703.

3.2.2 Pulse Template

3.2.2.1 E1 Mode

Figure 10 and Figure 11 represent the output pulses obtained for twisted pair and coaxial cable. During the tests, the backup boards were powered and the output drivers set to tristate mode.

Figure 10 E1 Twisted Pair Cable Output

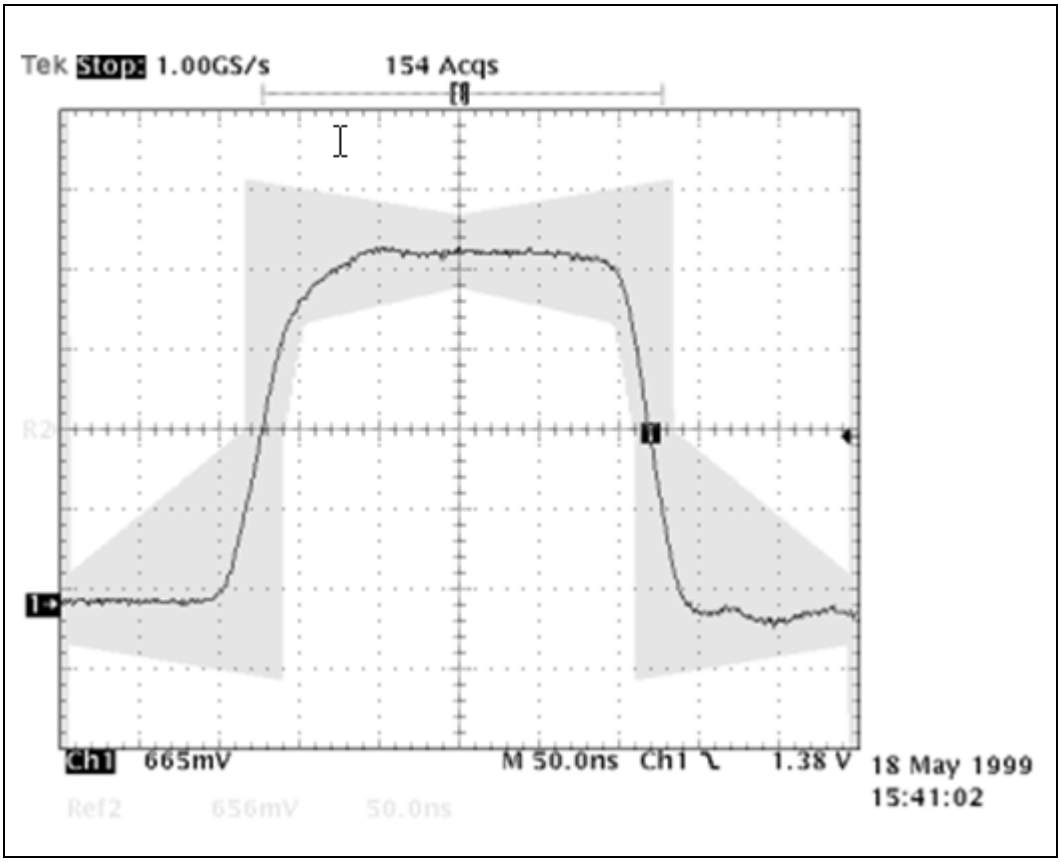
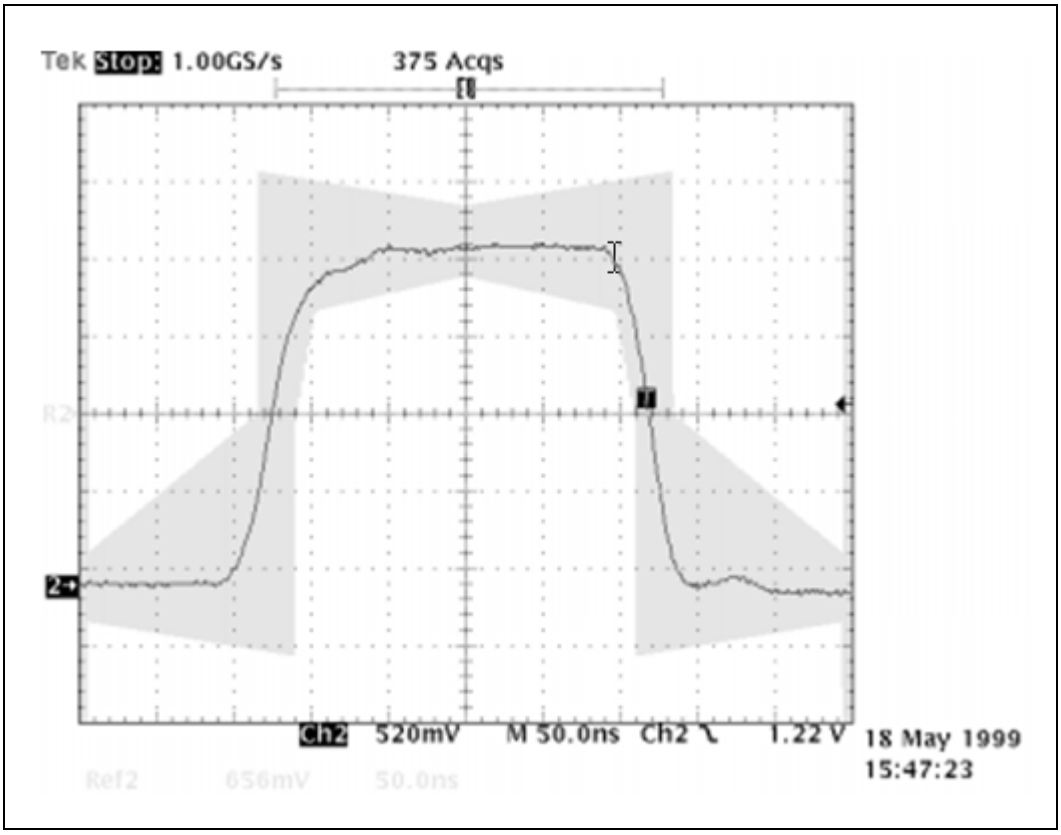


Figure 11 E1 Coaxial Cable Output



3.2.2.2 T1 Mode

The configuration shown in Figure 12 was successfully tested for all possible cable lengths. Figure 12 and Figure 13 show the test results for the two most extreme cases: no cable and maximum cable length.

Figure 12 T1 Output with 0 ft. of Cable

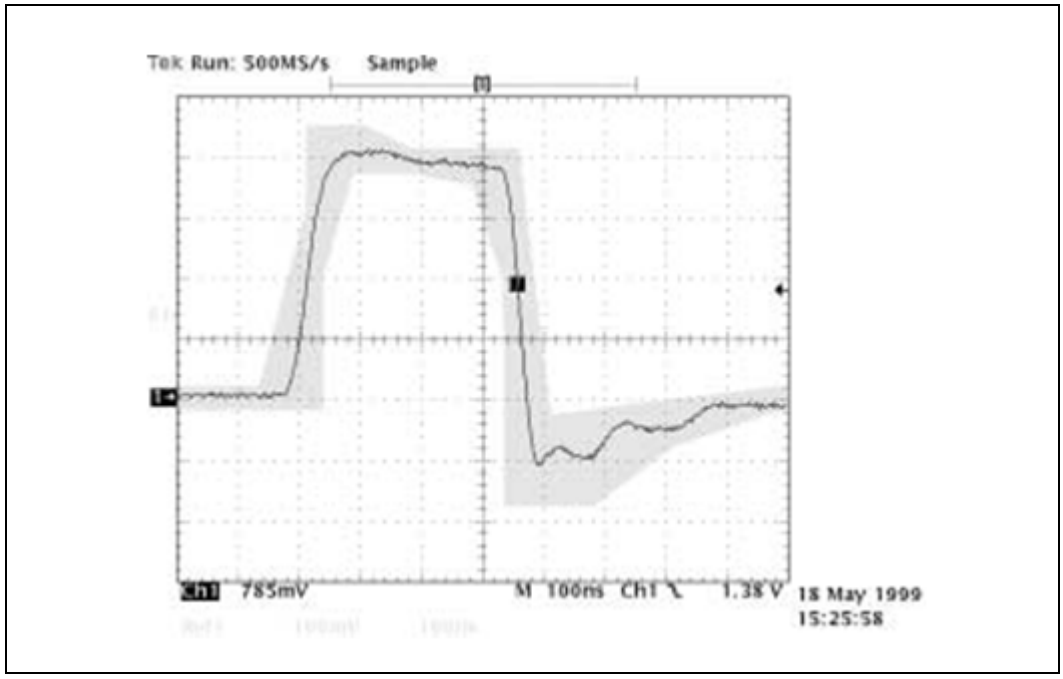
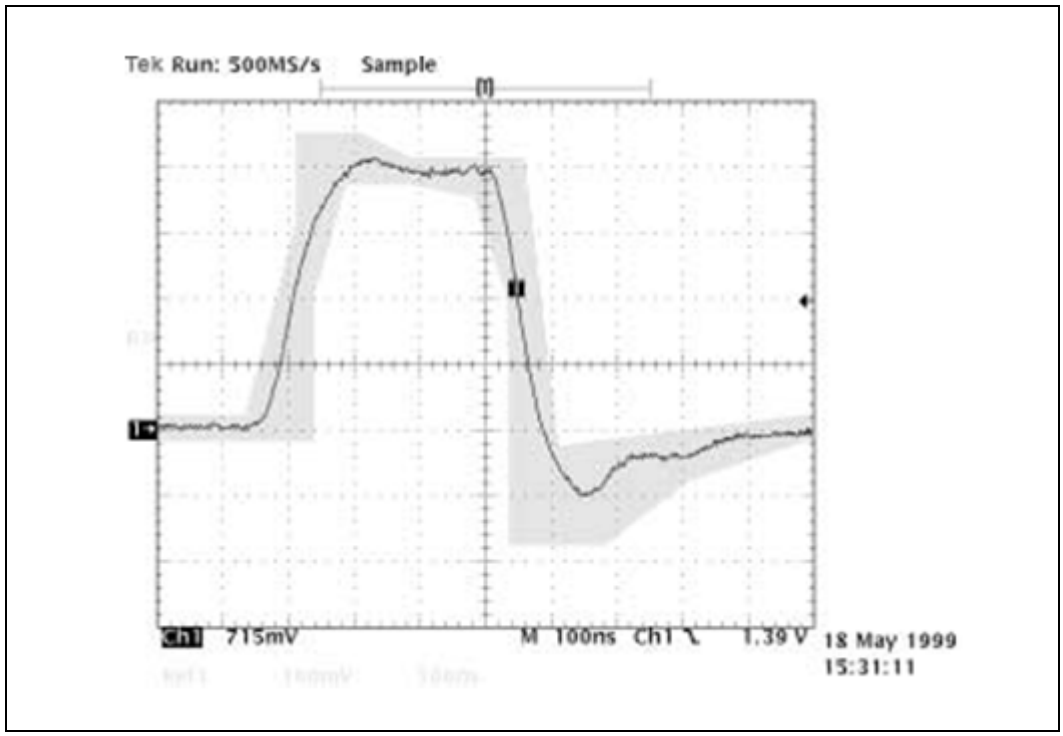


Figure 13 T1 Output with 655 ft. of Cable



3.2.3 Receive Return Loss

Figure 14 through Figure 16 represent the measured receive return loss for T1 and E1. Although there are no receive return loss requirements for T1, the results are compared against G.703 minimum requirements.

Figure 14 LXT384 LIU Rx Return Loss, E1 Twisted Pair Cable

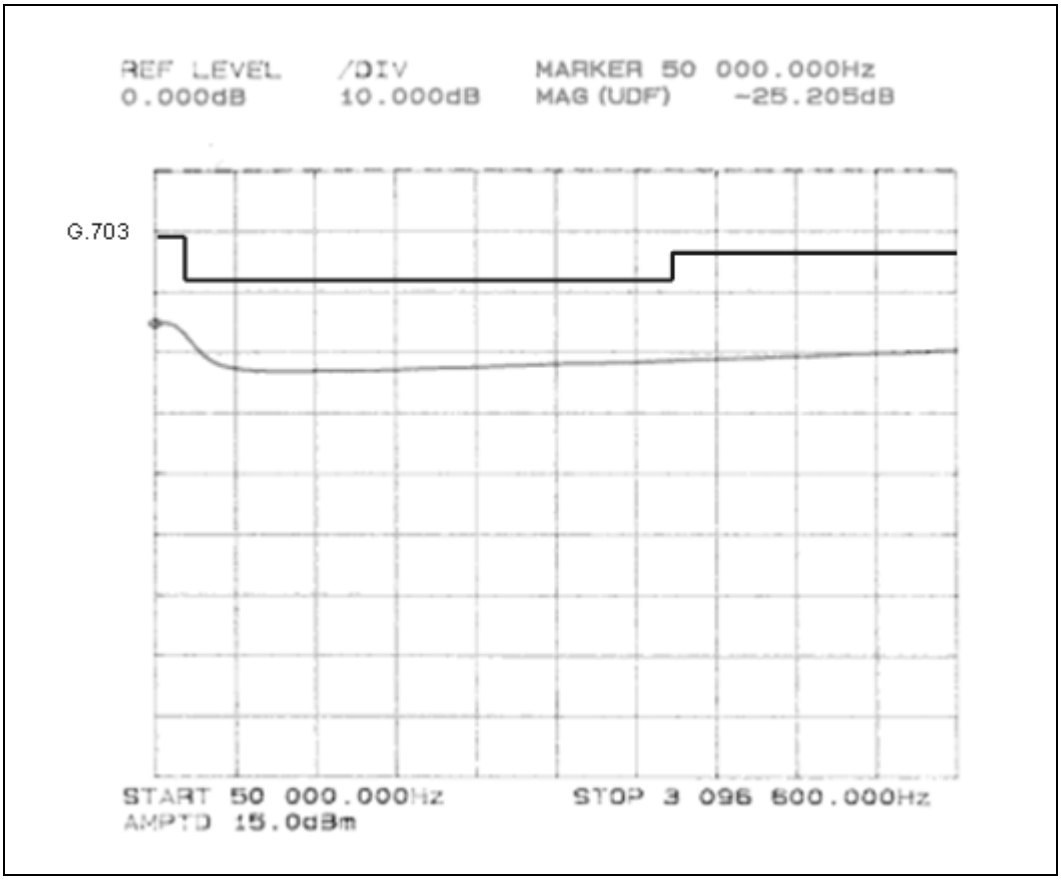


Figure 15 LXT384 LIU Rx Return Loss, E1 Coaxial Cable

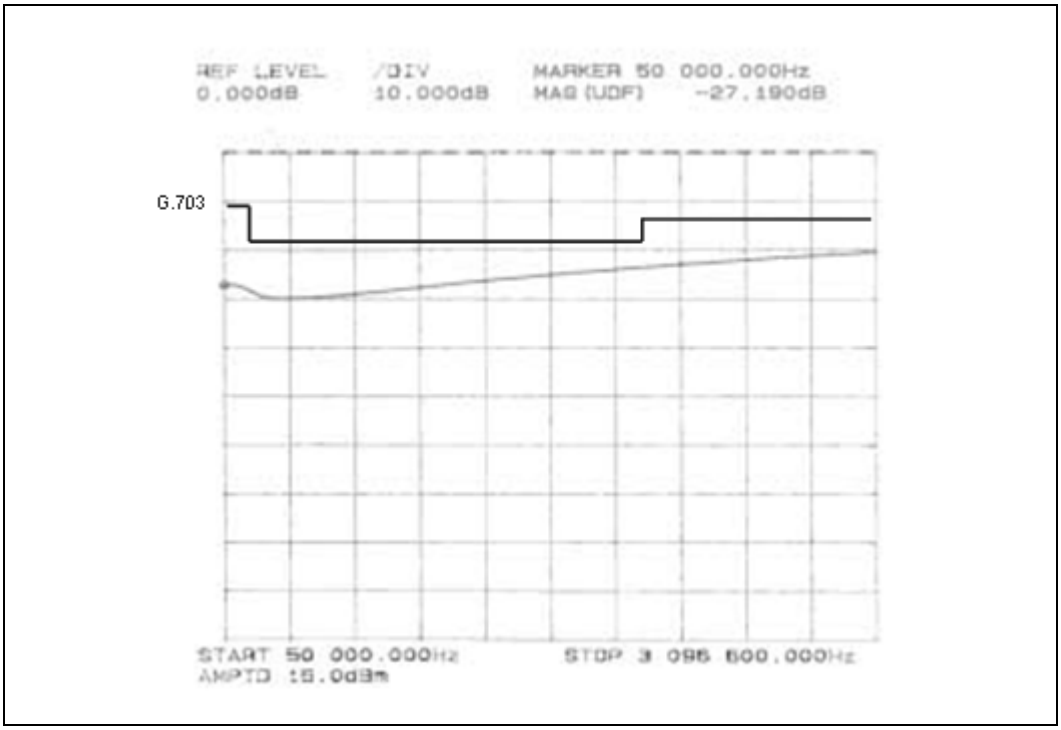
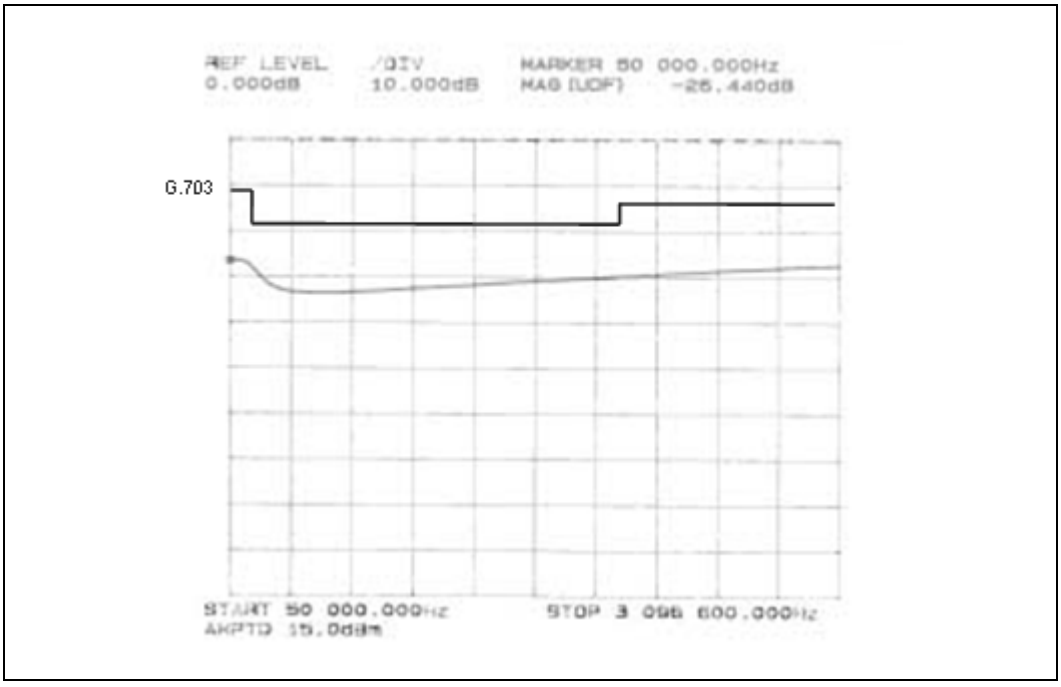


Figure 16 LXT384 LIU Rx Return Loss, T1 Twisted Pair Cable



3.2.4 Transmit Return Loss

Figure 17 through Figure 19 represent the measured transmit return loss for T1 and E1. Although there are no transmit return loss requirements for T1, the results are compared against ETSI ETS 300 166 minimum requirements.

Figure 17 LXT384 LIU Tx Return Loss, E1 Twisted Pair Cable

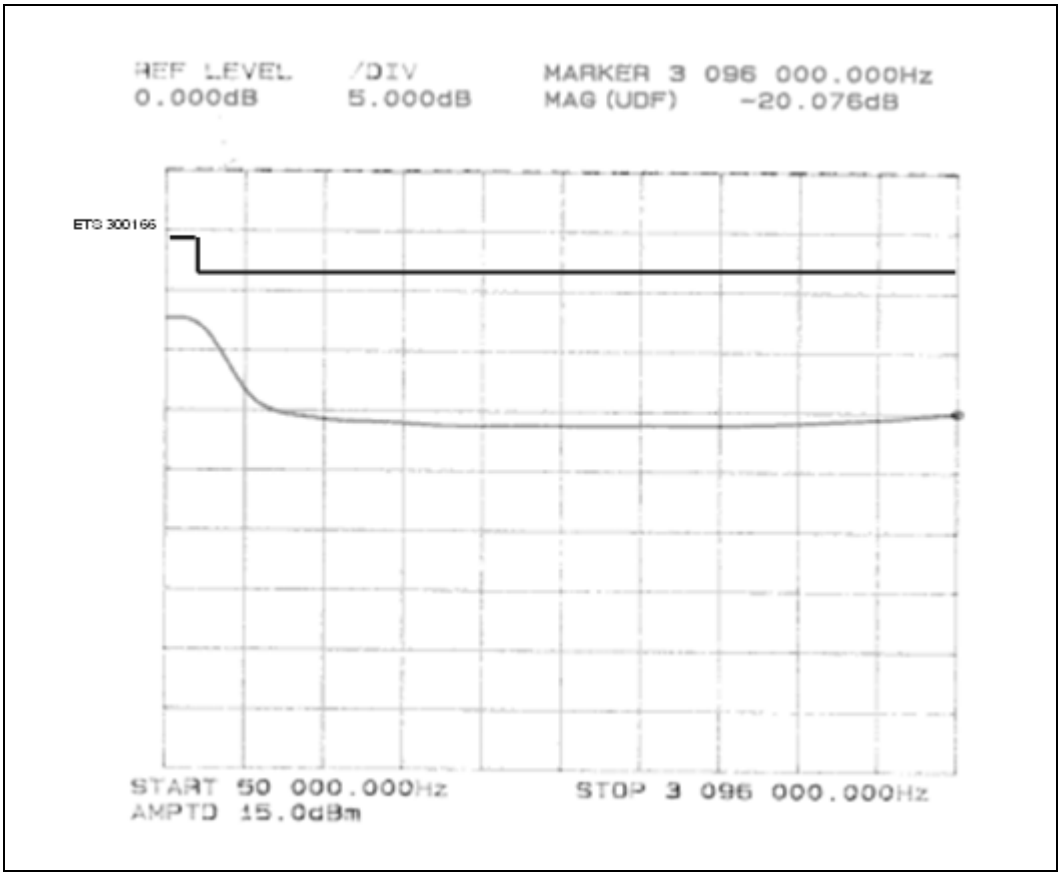


Figure 18 LXT384 LIU Tx Return Loss, E1 Coaxial Cable

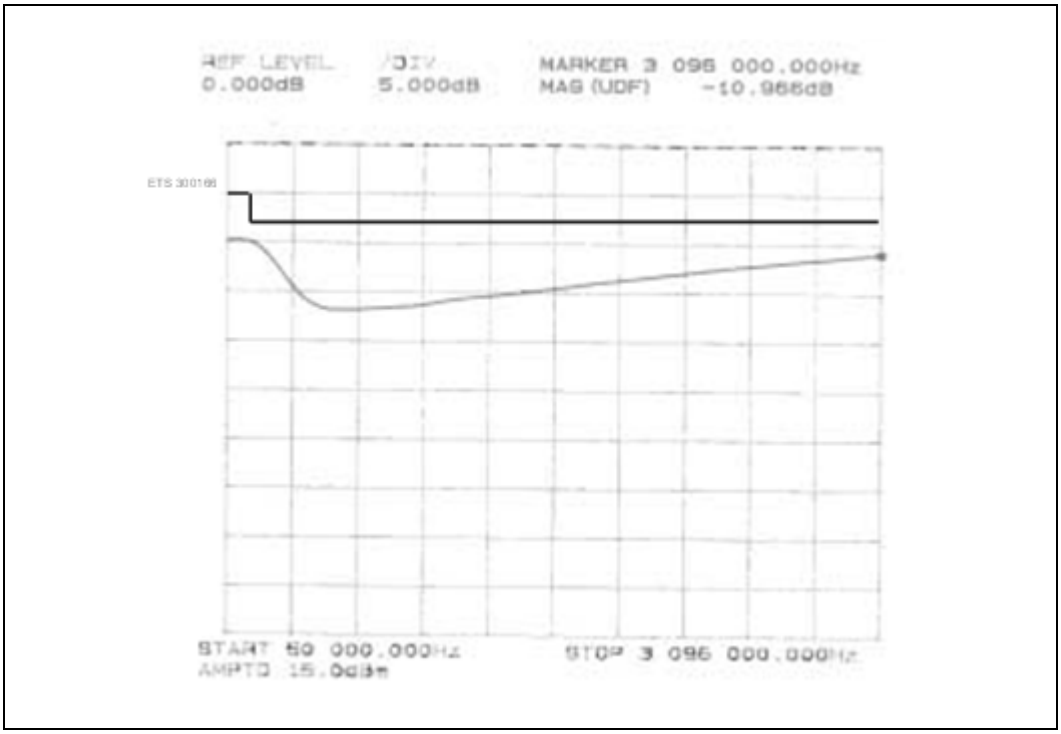
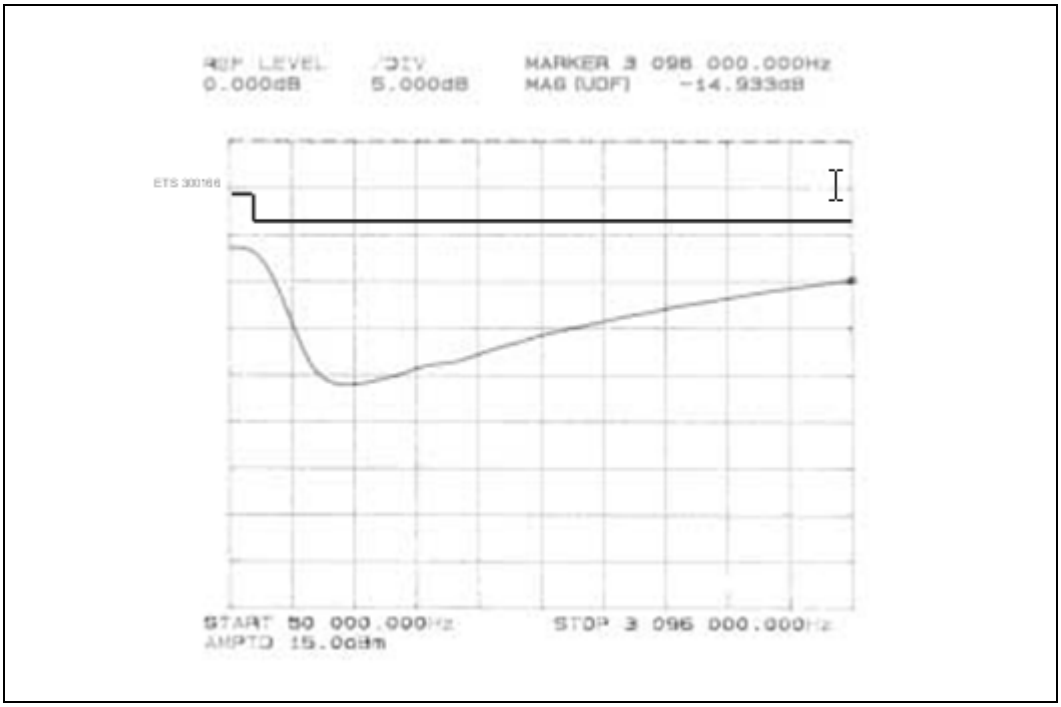


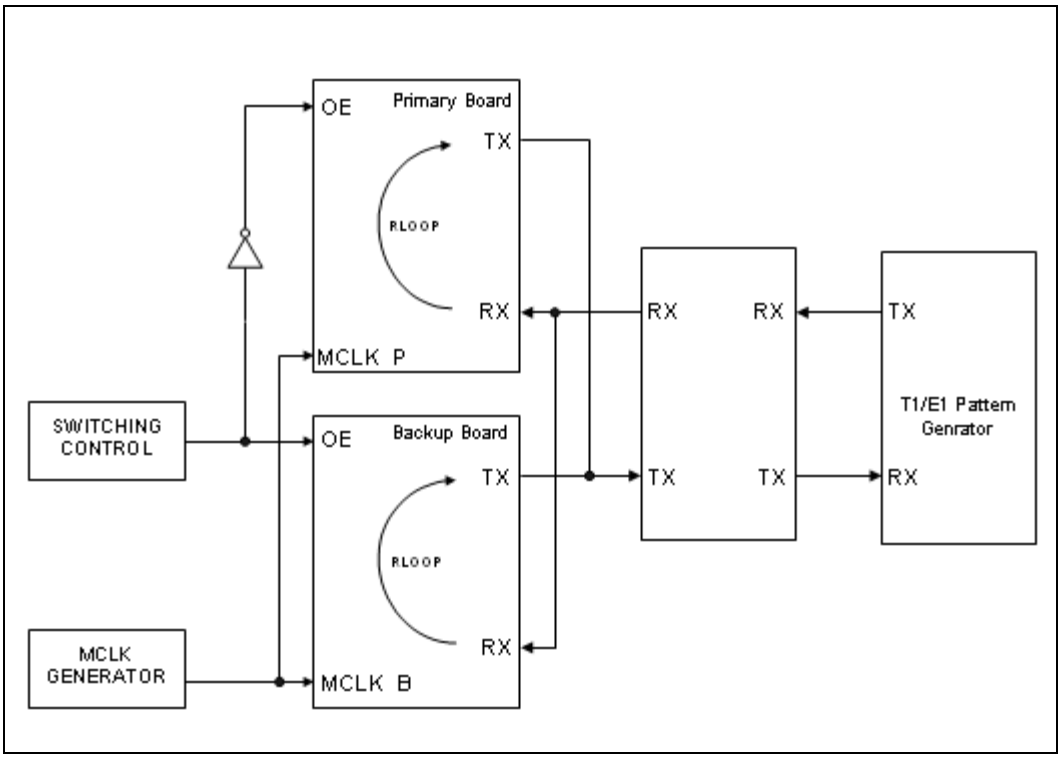
Figure 19 LXT384 LIU Tx Return Loss, T1 Twisted Pair Cable HPS Test Set-up



3.2.5 Test Setup

Figure 20 represents the setup used for hitless switching testing. A standard T1/E1/J1 pattern generator/analyzer transmits a framed pseudo-random pattern (215-1 for E1 and 220-1 for T1). Both the primary and the backup boards receive this pattern. The boards were set to retransmit the signals (remote loopback). A clock generator was used to provide MCLK references to the LXT384 LIUs.

Figure 20 HPS Test Set-up



One of the boards is active while the other board's driver is tristated (OE=Low). The "switching control" block, in this case a clock generator, determines which board is active. In order to obtain statistics on the number of bit errors caused by a switching event, the switch control block was set to generate a 50 Hz clock, effectively generating 100 switching events per second.

The pattern analyzer was used to keep track of the number of bit errors and to verify frame synchronization.

3.2.6 Test Conditions

- Input frequency range: +/- 50 ppm
- MCLK frequency range: +/- 100 ppm
- Room temperature
- Nominal supply voltage
- Jitter attenuator enabled in the LXT384 LIU. Since the board was set to remote loopback it is not relevant whether the jitter attenuator is placed in the transmit or receive path.

- Jitter added to the input signal. The input T1 and E1 input signals were modulated with sinusoidal jitter. The tests were performed at the jitter frequency/amplitude points listed in Table 4.

Table 4 Jitter Test Points

Jitter Frequency	Jitter Amplitude
1 Hz	10 UI
10 Hz	10 UI
100 Hz	10 UI
1 kHz	2 UI
10 kHz	0.5 UI
100 kHz	0.3 UI

3.2.7 Test Results

Standard frame synchronization algorithms require errors in two or more consecutive frame alignment words in order to declare loss of frame synchronization. Since the number of errors is limited to one, frame loss will not be declared.

The following results were obtained using the setup in Figure 22 for both T1 and E1 operation:

- Maximum number of errors per switching event: 1 error
- Probability of an error during a switching event: 50%
- No frame synchronization loss

4.0 Frequently Asked Questions

Question 1 **What is redundancy?**

Answer In the telecom industry, redundancy means having a back-up board in the system in the event the primary board fails. Redundancy is the most common method to ensure reliable and continuous service.

Question 2 **What is HPS 1+1 Protection?**

Answer 1+1 protection is when every primary board has a back-up board. In this configuration the equipment is protected from single board failures. Hitless Protection Switching means having the ability, in the event of a board failure, to be able to switch in the back-up board before a loss of frame sync.

Question 3 **Why do you need HPS?**

Answer Currently, most manufacturers are doing 1+1 protection using relays to switch from the primary to the back-up board. There are a number of reasons to use Cortina's HPS scheme rather than relays. Because the transmitters of the LXT38x family of Line Interface Units (LIU) can be fast tri-stated and contain constant delay jitter attenuation, the transmitters and receivers of the primary and back-up boards can be tied together. On an octal T1/E1/J1 interface card, this saves 8 transformers, 16 mechanical relays and 8 sets of protection devices. This, in turn, saves money and board space making the end product more marketable and reliable.

Question 4 **Can I make the primary and back-up boards hot swappable?**

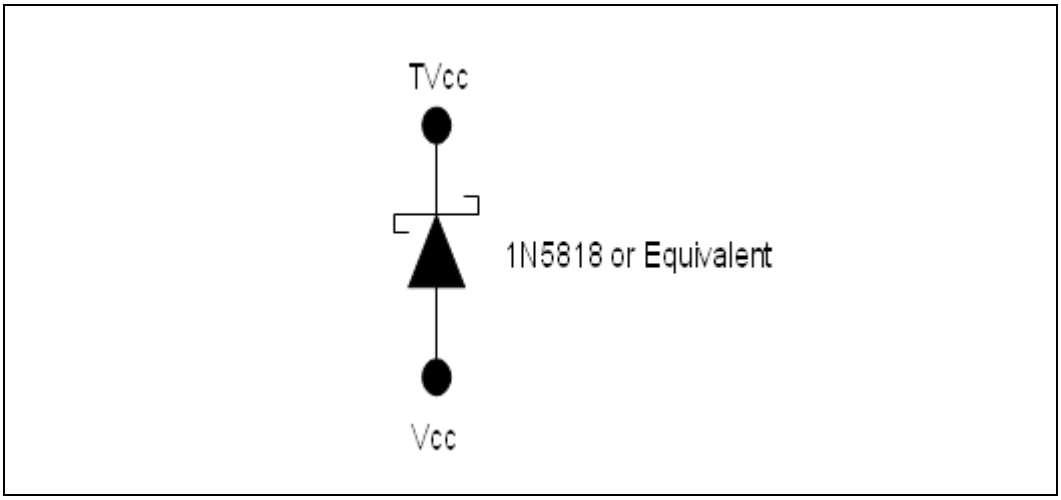
Answer Yes. The high impedance of the receiver and the tristated transmitter allow for this. Hot swapping requires special design considerations.

A system issue for HPS applications is to have the ability to change out a failed card without taking the system off-line. This means that either the slot be switched and isolated or simply removed and replaced. A scheme has been tested for doing the latter, saving the switching and isolation circuitry.

The answer is twofold. First install a Schottky diode between VCC and TVCC ensuring that both supply pins come up at the same time. The second item is to etch the GND and OE fingers on the card edge connector longer than the signal pins and to etch the VCC and TVCC fingers to a length in between the GND/OE and signal pins. If the card is mounted in a rack and cannot be inserted crooked, the second item is irrelevant.

Figure 21 shows the orientation of the Schottky diode between the power pins.

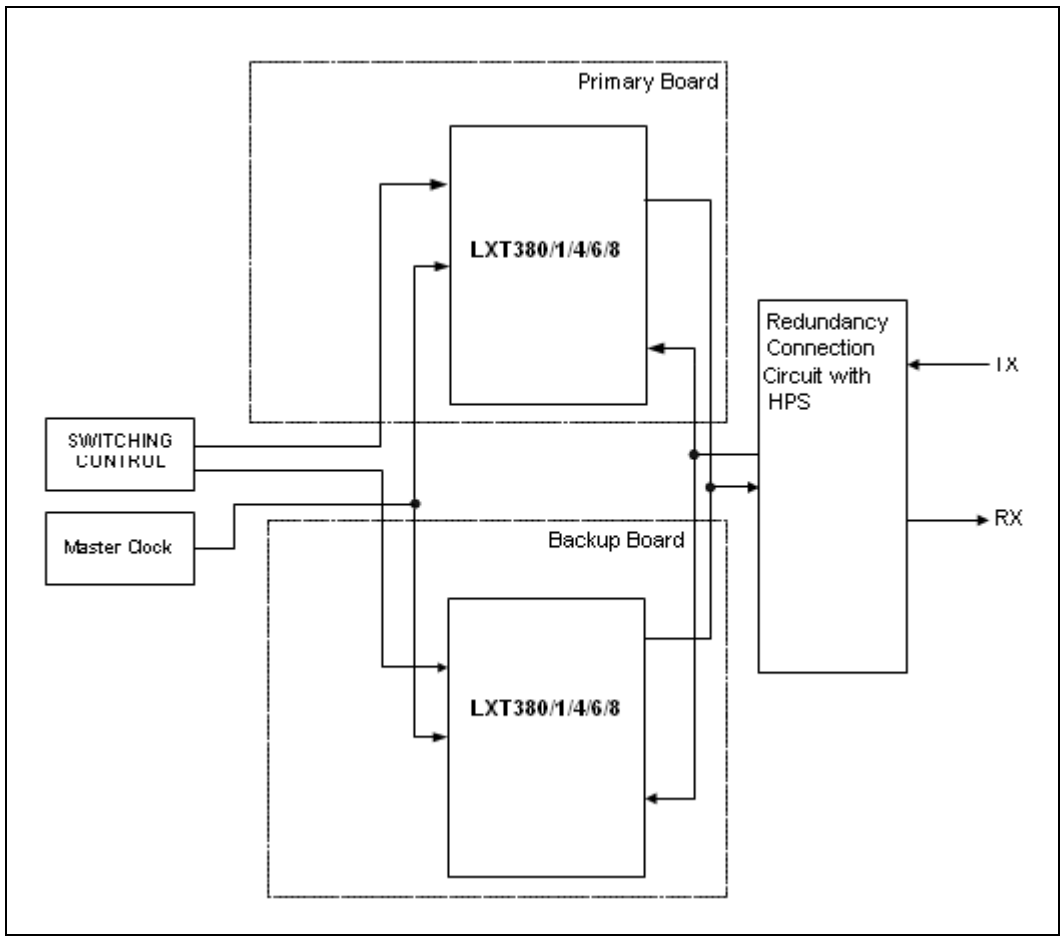
Figure 21 Diode Orientation



Question 5 **Can I power down the back-up board during normal operation?**

Answer This version of 1+1 Redundancy Protection without relays deals with leaving the backup board powered down or due to loss of board power or power supply failure while the system is running on the primary board. The scheme shown in Figure 22 works well whether or not power is applied to the backup board.

Figure 22 Block Diagram of Redundancy Circuit with Back-up Supply Voltage Removed



Features

Features for this solution include the following:

- Highly integrated octal LIU with small footprint
- Removing sixteen double pole relays while retaining octal redundancy
- Preserving electrical performance without frame hits during switchover
- Saving power by removing supply voltage to the backup board
- Primary and back-up boards are independent

Powering Down the Back-up

A powered down LIU will siphon power from a 1+1 protection interface if the power down sequence is not done correctly. There is a way to prevent this with the LXT38x LIU family by using the following sequence:

1. Ground the Output Enable (OE) pin.
2. Remove VCC and TVCC from the LIU on the board being powered down.

Following this procedure assures that the active LIU remains unaffected.

Question 6 **How can HPS help my equipment's reliability?**

Answer Not using redundancy can cause down time due to equipment failure. It could be hours for a technician to get to the site and replace a failed board. Using 1+1 redundancy with mechanical relays also causes down time. Due to the relay switching time, over 6,000 bit errors will be produced. It only takes a few bit errors out of 1,344 consecutive bits to cause a loss of frame sync forcing the system to reacquire frame sync. This means a potential loss of almost 38,000 bits.

Using HPS will eliminate down time because the switch-over is accomplished in less than 1 µSec.

Question 7 **In the event of an electrical surge, won't the back-up board get hit too?**

Answer Your first line of defense against electrical surges and lightning strikes is the front-end protection circuitry (transient surge protection, fuses, etc.). Any residual transients that make it past will not affect the back-up board due to the high impedance of the transmit drivers and Schottky diodes.

5.0 Conclusions

The results presented in this Application Note demonstrate that the LXT38x LIU series save space and power and operate successfully with the backup board powered down in T1/E1 1+1 protection systems.

Other options are available, such as a cabling solution for 1+1 protection, instead of the backplane design presented here. Please contact Cortina Applications Engineering for more information.

Contact Information

Cortina Systems, Inc.
840 W. California Ave
Sunnyvale, CA 94086

408-481-2300

sales@cortina-systems.com

apps@cortina-systems.com

www.cortina-systems.com

To provide comments on this document:

documentation@cortina-systems.com

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