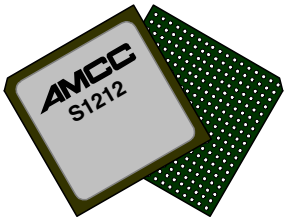

Description

The S1212 device consists of four CDR modules. Each of the modules can independently run at the OC-12 or OC-3 data rate. The S1212 can also be provisioned to mix and match OC-3 and OC-12 data streams within the same device. The S1212 can be configured in MII (Media Independent Interface) mode or in Non-MII mode.

The S1212 minimizes the external components on the board:
no external loop filter component,
internally biased outputs,
internally provided common mode bias for AC input, and internally provided bias for external LVPECL driver.

The S1212 offers significant advantages in power and real estate with high integration, low power, and a small package.

Overview

The function of the S1212 clock and data recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S1212 receives either an OC-12 or an OC-3 scrambled NRZ signal and recovers the clock from the data stream. The device outputs a differential bit clock and retimed data. Figure 1 shows a typical network application.

The Low Voltage Differential Signaling (LVDS) or LVPECL interfaces guarantee compliance with the bit-error rate requirements of the Telecordia and ITU-T standards.

AMCC Suggested Interface Devices

AMCC	S4805 DANUBE	SONET/SDH Mapper STS-48/STM-16, 4 x STS-12/STM-4 x STS-3/STM-1
AMCC	S4806 OHIO	0C-48/4 x OC-12 SONET/SDH Framer and channelized ATM/POS Mapper
AMCC	S1208 EVROS	STS-12/STM-4 DS3/E3/DS1 E1/VT/TU SONET/SDH Mapper
Agilent	HFBR-5908E	Optical Transceiver
Infineon	V23818-H18	Optical Transceiver
Agere	1417G4A	Optical Transceiver
Sumitomo	SCM7101-XC	Optical Transceiver
OCP	DTR-156-5M	Optical Transceiver

– At a Glance –

General Features

- CMOS 0.13 micron technology
- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer, and jitter generation
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports Data Rates of 155.52 Mbps (OC-3) and 622.08 Mbps (OC-12)
- LVDS or LVPECL differential serial interface
- Internal termination of the optic's LVPECL driver renders a seamless power saving connection
- Typical 350 mW power in LVDS I/O mode
- Directly compatible with 2.5 V or 3.3 V LVDS, 3.3 V LVPECL (DC and AC)
- 196 Ball Grid Array Package
- 1.2 V and 3.3 V/2.5 V Power supply

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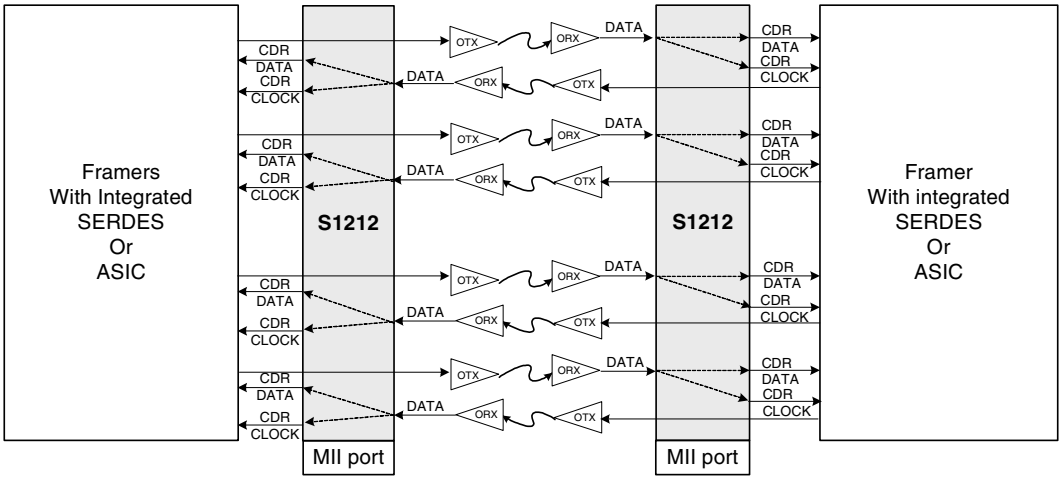

Figure 1. System Block Diagram

The sequence of operations is as follows for each Channel:

1. Serial data input
2. Serial Data and recovered clock outputs

Internal clocking and control functions are transparent to the user.

Prefix	Device	Package	Revision
S - Integrated Circuit	1212	PB -196 PBGA	20

X	XXXX	XX	XX
Prefix	Device	Package	Revision

Figure 2. S1212 Ordering Information

- Receiver lock detect output for each channel
- Signal detect input on each channel
- Selectable reference frequencies of 19.44, 77.76 or 155.52 MHz
- Quad configuration, mixed Mode OC-3/OC-12
- Independent power down of unused channels

Applications

- SONET/SDH OC-3/OC-12
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

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