TM

Envoy-CE2 Device

SPI-3 to Ethernet Controller
TXC-06880

PRELIMINARY **DATA SHEET**

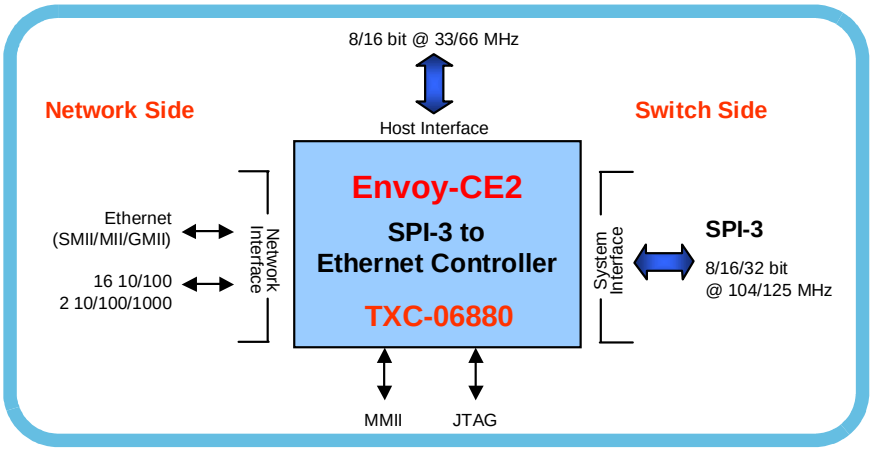
TXC-06880-MB, Ed. 4
February 2005

FEATURES

- 2 Configurable Media Access Controllers (MACs)
- Each MAC is configurable as 8 Fast Ethernet ports (10/100 Mbit/s), 2 Fast Ethernet ports with extended buffers or 1 Gigabit Ethernet port (10/100/1000 Mbit/s)
- SPI-3 interface configurable in Link or PHY layer mode, operating at 125 MHz
- Support for Jumbo frames (9600 Bytes) and Super Jumbo frames (12000 Bytes)
- Full and Half Duplex (CSMA/CD) operation (Half Duplex only supported for Fast Ethernet)
- Programmable SPI-3 burst size from 64 to 1024 bytes
- Frame integrity verification (FCS and Frame length checks) and generation
- Packet statistics and Performance monitoring support for RMON per port
- PAUSE frame flow control for Full Duplex mode
- "Raise Carrier" flow control for Half Duplex mode
- Programmable high and low FIFO watermarks for flow control trigger
- Automatic PAUSE frame generation and termination
- Filtering of PAUSE frames in Ethernet Ingress or Egress
- Port aggregation from Ethernet to SPI-3, using routing tag encapsulation
- 8/16 bit Microprocessor interface, selectable between Intel or Motorola
- JTAG Boundary Scan (IEEE 1149.1 Standard)
- 580-lead Plastic Ball Grid Array (PBGA) package, 27 mm x 27 mm

APPLICATIONS

- Metro Edge Routers and Switches
- Ethernet over SONET/SDH Multi-Service Provisioning Platforms (MSPPs)
- IP DSLAMs
- 3G Wireless Base Stations
- 3G Radio Network Controllers (RNCs)
- Multi-Service Access Platforms (MSAPs)



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LIST OF FIGURES

LIST OF DATA SHEET CHANGES

Section A:

This Section A change list identifies those areas within previous released Envoy-CE2 device Data Sheet **Edition 3, January 2005** that have significant differences relative to the second previous released Envoy-CE2 Data Sheet **Edition 2, November 2004**.:

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
3-5	Updated Table of Contents and List of Figures.
6	Added 'List of Data Sheet Changes' section.
11	Modified Section 2.1.1.
19	Modified Section 2.1.9.
49	Modified Max value of "MDC frequency" for table Figure 17.
50	Modified last row for table Figure 18.
57	Modified last column of Symbols "T2", "T3" and "T4" for table Figure 23.
58	Modified last column of Symbols "T3" and "T4" for table Figure 24.
63	Modified Section 6.2.1.1 and added Section 6.2.1.2.
81	Modified Description for Address "0040".
87	Modified Description for Addresses "2014" and "2040". **Changed "STPA Violation Frame Error Enable" to "Reserved. Must be set to 0 for normal operation." in Description for Address** "2018"**.**
87	**Changed "SPI-3 Input Overflow Packet Violation Counter" to "Reserved" in Description and modified "RC" to "RO" in Mode for Address** "2068".
117	Modified and added new Part Number. Removed two Related Product devices.

Section B:

This Section B change list identifies those areas within this updated Envoy-CE2 device Data Sheet that have significant differences relative to the previous and now superseded Envoy-CE2 Data Sheet:

Updated Envoy-CE2 device Data Sheet: *PRELIMINARY* Edition 4, February 2005

Previous Envoy-CE2 device Data Sheet: *PRODUCT PREVIEW* Edition 3, January 2005

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date. Changed *Product Preview* to *Preliminary*.
3-5	Updated Table of Contents and List of Figures.
6	Updated 'List of Data Sheet Changes' section.
50	Modified table Parameter column for Figure 18.
59	Modified Section 6.1.2.1, Section 6.1.2.2 and Section 6.1.2.3.
60	Modified Section 6.1.2.4 and Section 6.1.2.5.
63	Modified Section 6.2.1.1 and Section 6.2.1.2.
67	Modified Section 6.2.4.7.
84	Modified rows for register "2008", "200C", "2014" and "2014".
86	Modified Description for Bit Range 7-0 of Address "2008".
87	Modified Description for Bit Range 7-0 of Address "200C", "2014" and "2014".
101	Modified Bit Range 15-8 Description for Address "4008".
106	Modified Bit "2" Description for Address "4084".
107	Modified Bit "24", "25", "26" and "27" Descriptions for Address "4084".

1.0 OVERVIEW

1.1 DEVICE DESCRIPTION

The Envoy™-CE2 is the next generation of powerful Ethernet to SPI-3 Controllers for carrier-class networks. The Envoy-CE2 incorporates two configurable Media Access Controllers (MACs). Each MAC can be configured as a single Gigabit Ethernet (10/100/1000 Mbit/s), dual Fast Ethernet with extended buffers or octal Fast Ethernet (10/100 Mbit/s) interface and is programmable for either full-duplex or half-duplex operation. The Envoy-CE2 supports Super Jumbo (12 KBytes) packets on both Fast Ethernet and Gigabit Ethernet interfaces.

The Envoy-CE2 is designed to interface directly with SPI-3 compliant devices, such as network processors. The support for master mode on the SPI-3 allows glueless interface with standard SPI-3 based GFP/VCAT framers and mappers. On the Ethernet side, the Envoy-CE2 interfaces directly with standard Fast Ethernet and Gigabit Ethernet PHY/SerDes devices via the SMII and GMII. The Envoy-CE2 incorporates on-chip buffering to promote high performance without congestion or loss of data and provides backpressure support on both the Ethernet and SPI-3 interfaces.

1.2 APPLICATION EXAMPLE

Ethernet is emerging as the Layer 2 Protocol of choice in Enterprise, Access and Metro Networks. This is due to its cost effectiveness, wide spread acceptance and ease of use. The Envoy-CE2 provides a means to connect a cost efficient, switching protocol interface in Ethernet to a Telecom based interface, the OIF SPI-3. Current network processing devices that traditionally have a packet based interface the OIF SPI-3 interface, can now interface to Ethernet based devices using the Envoy-CE2.

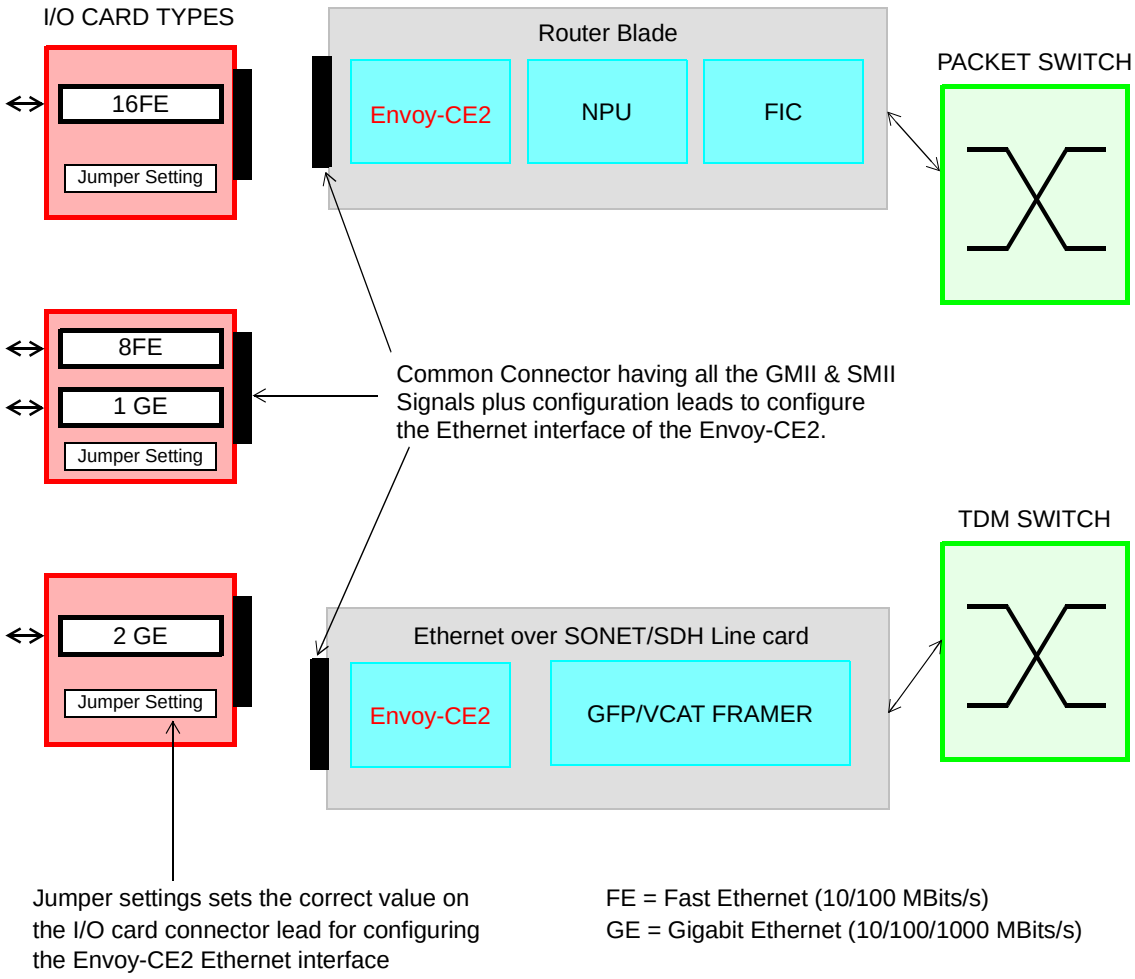
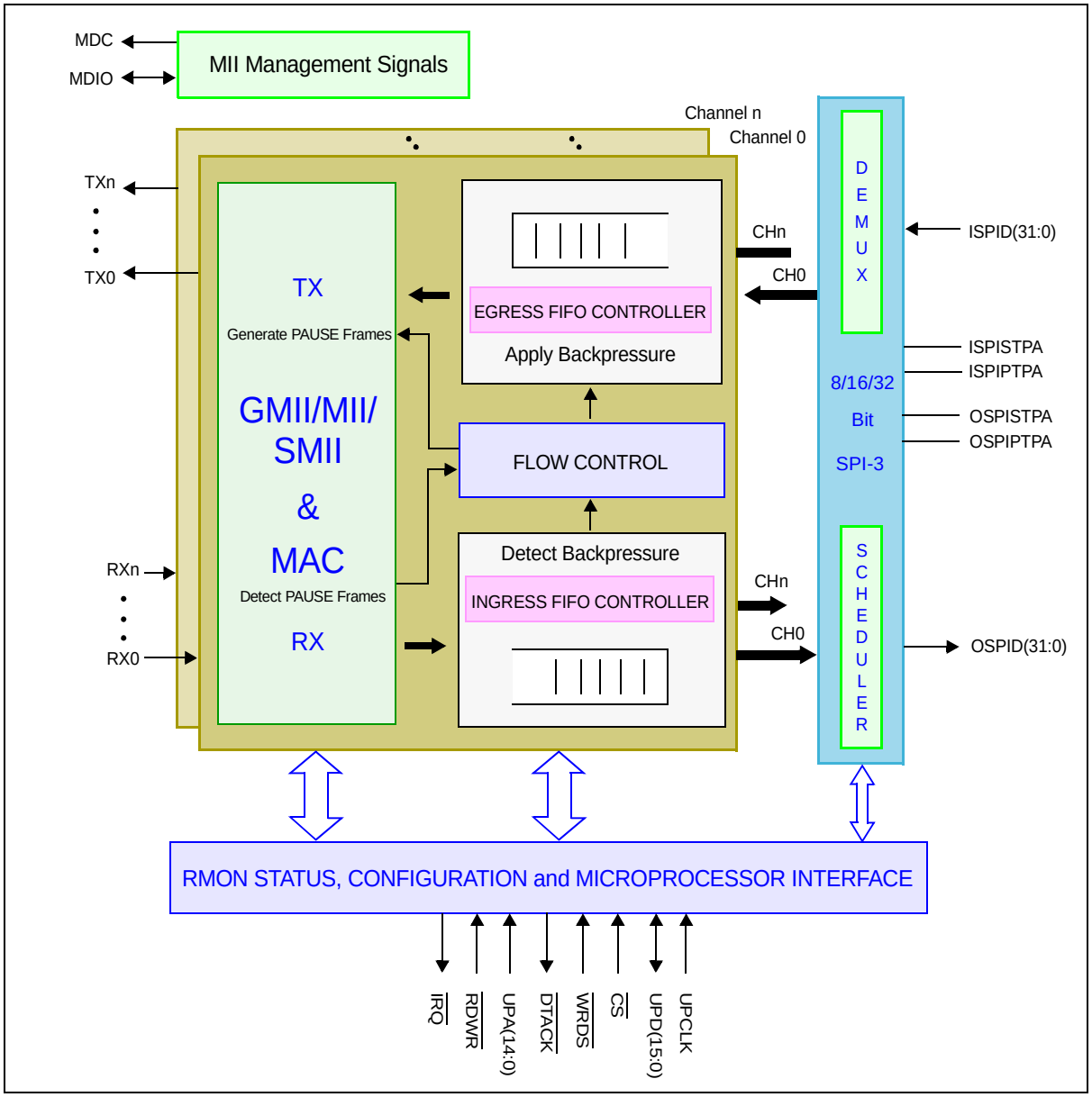


Figure 1. Flexible Architecture for Ethernet Over SONET/SDH & Router Application

2.0 FUNCTIONAL DESCRIPTION

2.1 BLOCK DIAGRAM



Note: Each MAC is configurable as 8 Fast Ethernet Ports (10/100 Mbit/s), 2 Fast Ethernet Ports with Extended Buffers, or 1 Gigabit Ethernet Port (10/100/1000 Mbit/s)

Figure 2. Functional Block Diagram of the Envoy-CE2

2.1.1 Media Access Controller (MAC)

The Envoy-CE2 has 2 Configurable Media Access Controllers (MACs):

- Configurable MAC A services ports 0 to 7
- Configurable MAC B services ports 8 to 15

Each MAC can be configured as:

- 8 Fast Ethernet ports with 7.75 KBytes of Ingress buffering and 4 KBytes of Egress buffering per port supporting 10/100 Mbit/s data rates via SMII.

OR

- 1 Gigabit Ethernet port with 62 KBytes of Ingress buffering and 32 KBytes of Egress buffering per port supporting 10/100/1000 Mbit/s data rates via GMII/MII.

OR

- 2 Fast Ethernet ports with 31 KBytes of Ingress buffering and 16 KBytes of Egress buffering per port supporting 10/100 Mbit/s data rates via SMII. (Extended SMII Mode).

Possible Envoy-CE2 Configurations:

- 16 Fast Ethernet Ports
- 2 Gigabit Ethernet Ports
- 8 Fast Ethernet Ports and 1 Gigabit Ethernet Port
- 4 Fast Ethernet Ports (Extended SMII Mode) with larger buffers (31 KBytes of Ingress Buffering and 16 KBytes of Egress Buffering per port).

The main features supported by each Configurable MAC are:

- Compliant to IEEE 802.3, 802.3i, 802.3u, 802.3x, 802.3z
- Full Duplex and Half Duplex (CSMA/CD) operation per configurable MAC
- Connection to standard 10/100 Mbit/s Fast Ethernet PHY devices via SMII interface
- Connection to Multi-rate 10/100/1000 Mbit/s Gigabit Ethernet PHY devices via GMII/MII interface
- Frame Integrity Verification (FCS and length checks)
- Errored Frames can be configured to be filtered
- Programmable Inter-Packet Gap (IPG) between Ethernet frames
- Programmable maximum frame length
  - Minimum frame size = 64 bytes
  - Maximum frame size = 12 KBytes
- Support for VLAN tagged frame transmission
- Programmable High and Low FIFO watermarks for space and frame/chunk availability generation
- MAC control sublayer provides support for control frames including PAUSE frames
- Automatic PAUSE Frame Generation and Termination
- 62 KByte ingress FIFO per Configurable MAC
- 32 KByte egress FIFO per Configurable MAC
- Far end switch side loopback for diagnostic capability
- Packet statistics and performance monitoring support for Remote Network Monitoring (RMON)

2.1.2 Serial Media Independent Interface (SMII)

The Serial Media Independent Interface (SMII) is capable of operating at 10/100 Mbit/s mixed mode. The SMII is configurable to operate in either Full Duplex or Half Duplex mode.

Control and Data are transported across the Tx and Rx signals in 10 bit segments. The segments are synchronized using the SYNC signal. From the 10 bits, 2 bits are control and the other 8 bits are data. In 100 Mbit/s mode, every 10 bit segment transfers a new byte of data. In 10 Mbit/s mode, each 10 bit segment is repeated ten times. Please refer to the SMII specification for further details.

Each SMII port is comprised of:

- Two serial data signals (Tx and Rx) per port
- 125 MHz reference clock signal (Clock) per Configurable MAC
- Synchronization signal (SYNC) per Configurable MAC

2.1.3 Gigabit Media Independent Interface (GMII) & Media Independent Interface (MII)

The GMII interface of the Envoy-CE2 is capable of operating at 1 Gbit/s. When configured in MII mode, the interface is capable of operating at 10/100 Mbit/s. The GMII/MII ports allow the Envoy-CE2 to connect to Multi-rate Gigabit Ethernet PHY devices.

When configured as GMII, each port is comprised of:

- Two data buses, Transmit and Receive, each 8 bits wide
- Two clock signals, 1 per direction
    - The transmit clock is an output and the receive clock is an input
    - An input pad is provided to source the transmit clock from an external oscillator
- Two network status signals (Rx Error and Tx Error)
- Two control signals (Rx Data Valid and Tx Enable)
- All signals are synchronous to the clock
- Note: The GMII is a 3.3 V interface that will only work with a 3.3 V PHY device.

Note: The GMII is a 3.3 V interface that will only work with a 3.3 V PHY device.

When configured as MII, each port is comprised of:

- Two data buses, Transmit and Receive, each 4 bits wide
    - Uses Least Significant Nibble of the GMII bus
- Two clock signals, 1 per direction
    - Both the transmit and receive clocks are inputs to the Envoy-CE2
- Four Status signals (Rx Data Valid, Tx Enable, Carrier sense, and Collision detect)

Note: The GMII signal pins are muxed with the SMII signal pins.

The following sequence needs to be performed when switching from GMII mode to MII mode and vice versa:

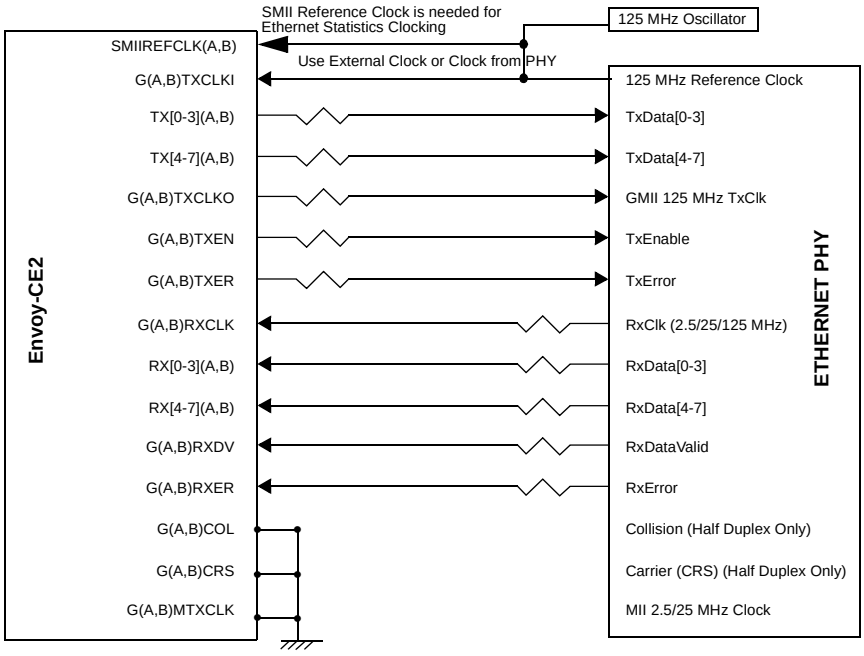
- Enable Soft Reset for the MAC (Register 0x4000 Bit 31 for Port 0)
- Reprogram Interface Mode Register (Register 0x4004 Bits 8-9)
- Remove Soft Reset

2.1.4 Ethernet Interface Description For Different Modes

The Envoy-CE2 has 16 Ethernet Ports: Ports 0 to 15. Ports 0 to 7 are assigned to Configurable MAC A (CMAC A) and Ports 8 to 15 are assigned to Configurable MAC B (CMAC B). Each CMAC can be configured as 8 SMII ports, 2 Extended SMII ports (larger buffers) or 1 triple speed GMII/MII port. Device pins CFGCMACA(1:0) and CFGCMACB(1:0) are used to configure CMAC A and CMAC B, respectively.

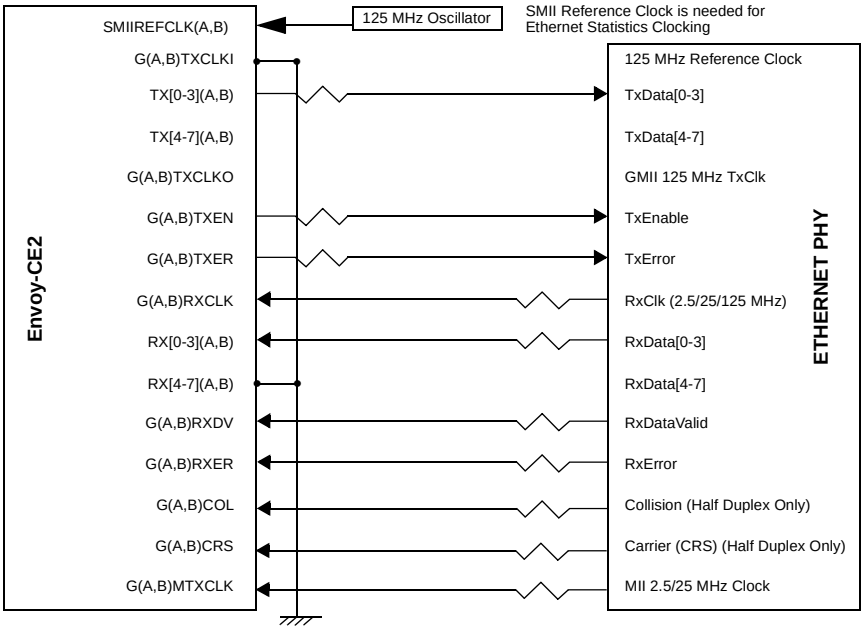
When CMAC A is configured in GMII/MII mode (CFGCMACA = 01), port 0 will be in GMII or MII mode (MII mode is based on programmable bits “Interface Mode”: register 4004 bits 8-9) and ports 1 to 7 are inactive. When CMAC A is configured in Extended SMII mode (CFGCMACA = 10), ports 0 and 4 will be in extended SMII mode and ports 1, 2, 3, 5, 6, and 7 are inactive. When CMAC A is configured in SMII mode (CFGCMACA = 11), ports 0 to 7 will be in SMII mode.

When CMAC B is configured in GMII/MII mode (CFGCMACB = 01), port 8 will be in GMII or MII mode (MII mode is based on programmable bits “Interface Mode”: register 4804 bits 8-9) and ports 9 to 15 are inactive. When CMAC B is configured in Extended SMII mode (CFGCMACB = 10), ports 8 and 12 will be in extended SMII mode and ports 9, 10, 11, 13, 14, and 15 are inactive. When CMAC B is configured in SMII mode (CFGCMACB = 11), ports 8 to 15 will be in SMII mode.



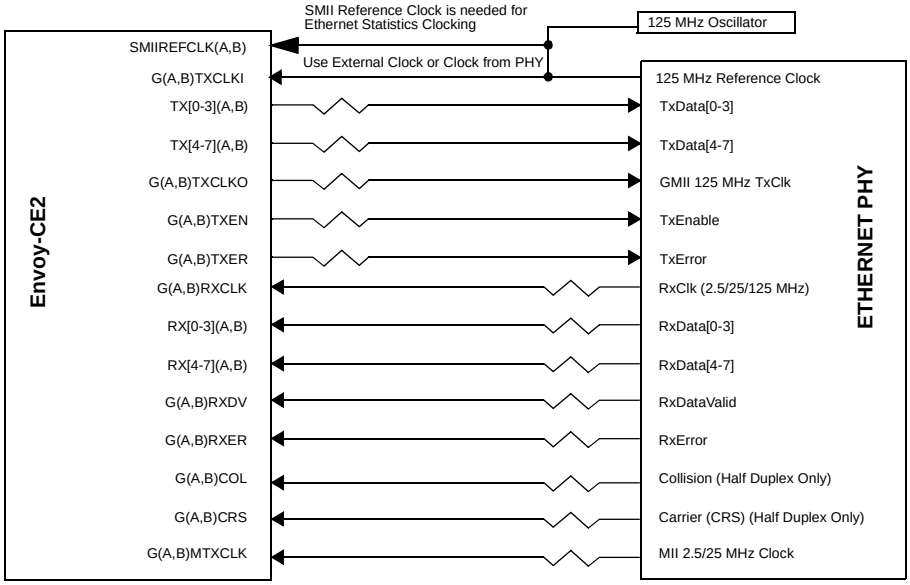
Note: Series termination resistor values are dependent on the selection of the Ethernet PHY. Please consult the specification of the Ethernet PHY for series termination resistor values

Figure 3. GMII (1000 Mbit/s) Only Interface Connection



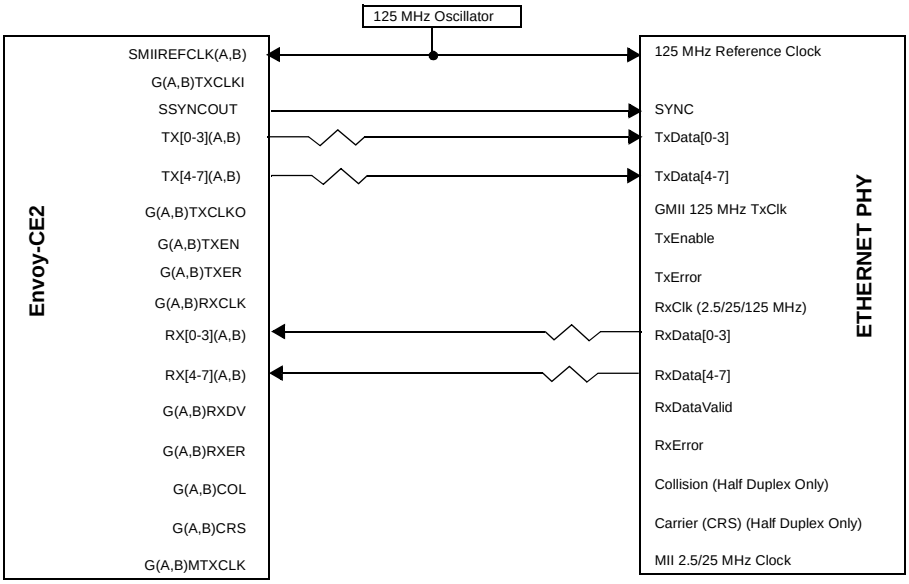
Note: Series termination resistor values are dependent on the selection of the Ethernet PHY. Please consult the specification of the Ethernet PHY for series termination resistor values

Figure 4. MII (10/100 Mbit/s) Only Interface Connection



Note: Series termination resistor values are dependent on the selection of the Ethernet PHY. Please consult the specification for the Ethernet PHY to determine the series termination resistor values

Figure 5. GMII/MII (10/100/1000 Mbit/s) Interface Connection



Note: Series termination resistor values are dependent on the selection of the Ethernet PHY.
Please consult the specification for the Ethernet PHY to determine the series termination resistor values

Figure 6. SMII (10/100 Mbit/s) Interface Connection

2.1.5 Management Media Independent Interface (MMII) Port

The MMII port on the Envoy-CE2 is used to configure and retrieve status from the Ethernet PHYs connected to the Envoy-CE2. Multiple PHY devices (up to 32) are programmable via this interface. The Envoy-CE2 MMII interface is compliant to the Management interface outlined in IEEE 802.3u. The device can be configured for preamble suppression at the MMII interface. The frequency of the output clock of the MMII port (MDC) is programmable to UPCLK/n (n = 4, 6, 8, 10, 14, 20, or 28). All data transfers are synchronous to the clock signal and provide support for up to 32 PHYs.

Two additional functions performed by the interface are the Scan function and the Automatic PHY address Increment function. In Scan mode, multiple back-to-back reads can be performed from a particular PHY. When Scan mode and Auto PHY address increment are enabled, back-to-back reads can be performed with the PHY address being incremented after each read. Hence, the PHYs are scanned.

Note: When Scan mode and Auto PHY address increment are enabled, the range of addresses scanned will be between “PHY Address” (Register 0x0048 Bits(8-12)) and PHY number 31.

Notes:

1. When Scan mode and Auto PHY address increment are enabled, the range of addresses scanned will be between “PHY Address” (Register 0x0048 Bits 8-12) and PHY number 31.
2. Envoy’s Management Media Independent Interface (MMII) is in Master mode.

2.1.6 Ingress & Egress Buffering Mechanism

Two buffering mechanisms are provided: **Store and Forward** and **Streaming**. In Store and Forward mode, a complete frame is stored in the Ingress and Egress buffers, before it is transmitted across the SPI-3 and Ethernet interfaces, respectively. In Streaming mode, a programmable number of bytes are stored in the Ingress and Egress buffers, before the frame is transmitted across the SPI-3 and Ethernet interfaces, respectively. Hence for low latency applications, streaming mode provides a solution to transport large frames with smaller buffer space. The Ingress and Egress buffers can be programmed separately.

2.1.7 System Packet Interface Level 3 (SPI-3)

The SPI-3 interface operates using an 8, 16, or 32 bit wide pin configurable data bus (TDAT(31-0) and RDAT(31-0)). The minimum clock (TFCLK and RFCLK) rate is 50 MHz and the maximum clock rate is 125 MHz. The device can be pin configured to operate as a Link (Master) or a PHY (Slave) layer device. Multi-PHY (MPHY) and Single-PHY (SPHY) modes of operation are supported (programmable). Packet level transfer mode is supported in Multi-PHY mode only and Byte level transfer mode is supported in both Single-PHY and Multi-PHY modes. On the output interface, chunking is supported where a configured number of bytes (chunk) are transferred by a port from the PHY device to the Link device. Programmable packet available thresholds are provided on the input interface. The SPI-3 interface is divided into the SPI-3 input and the SPI-3 output.

The SPI-3 interface assigns an 8 bit port address with an address range of 0 to 255. The Envoy-CE2 allows programming of an offset base address for the SPI-3 port address assignment. The base address is a 3-bit programmable value and is assigned to the most significant 3 bits of the 8 bit SPI-3 address. Individual SPI-3 port addresses are calculated by adding the (base address x 32) to the logical Ethernet port number. For example, the SPI-3 address of port 11 with a base address of 3 will give a SPI-3 port address of (11 + (3x32)) =107.

2.1.7.1 PHY Mode

In PHY layer mode, the following SPI-3 interface naming convention is used, per the OIF SPI-3 specification. Packets received at the Ethernet receive interface, are stored in the Ingress FIFO and **transmitted** on the **SPI-3 Rx** interface (SPI-3 output for Envoy-CE2). Packets **received** at the **SPI-3 Tx** interface (SPI-3 input for Envoy-CE2), are stored in the Egress FIFO and transmitted on the Ethernet transmit interface.

In PHY layer mode, space availability per channel for Transmit Interface (PTPA/STPA) is asserted when a programmable number of bytes or more, are available for storage in the Egress FIFO. The de-assertion of space availability is also programmable and is indicated when a programmed number of bytes are available for storage in the Egress FIFO (near-full condition). For PTPA, the programmable values for the assertion and de-assertion of the signal are 8 to 2040 bytes. For STPA, the programmable values for assertion and de-assertion are 2 to 255 bytes in 8-bit SPI-3 mode, 4 to 510 bytes in 16-bit SPI-3 mode, and 8 to 1020 bytes in 32-bit SPI-3 mode. In the Receive direction (SPI-3 output), one of the channels will be selected for frame transfer, based on a round robin algorithm. Packet data may be transferred across the Receive Interface in chunks, programmable from 8 to 2040 bytes, in 8 byte increments. In the Receive direction (SPI-3 output), the time between consecutive transfers (pause) is programmable to 0 or 2 cycles.

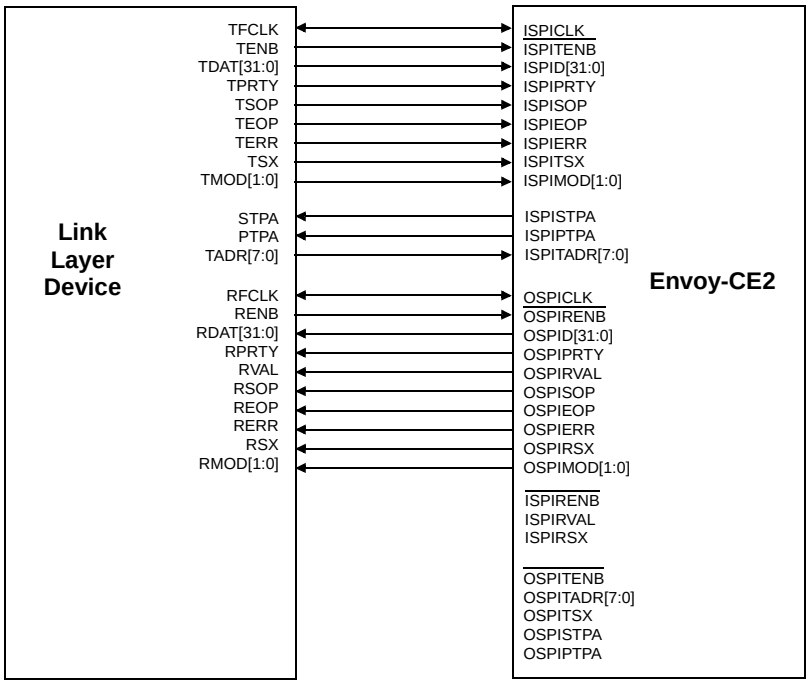


Figure 7. Envoy-CE2 in PHY Layer Mode

2.1.7.2 Link Mode

In Link layer mode, the following SPI-3 interface naming convention is used, per the OIF SPI-3 specification. Packets received at the Ethernet receive interface, are stored in the Ingress FIFO and **transmitted** on the **SPI-3 Tx** interface (SPI-3 output for Envoy-CE2). Packets **received** at the **SPI-3 Rx** interface (SPI-3 input for Envoy-CE2), are stored in the Egress FIFO and transmitted on the Ethernet transmit interface.

At the Transmit Interface (SPI-3 output) in Link layer mode, the device monitors the STPA and PTPA signals for indication of buffer space availability in the PHY device. In the event the PHY device indicates FIFO buffer availability by asserting its Transmit Packet available status signal and there is packet data available for transfer to the port, then Envoy-CE2 will transfer packet data to the PHY port. The transfer may be chunk-based or packet-based. In chunk mode, a specified number of bytes (chunk) is transferred to a PHY device port, before the Envoy-CE2 selects another PHY port for packet data transfer. If an end of packet is encountered, a reselection also occurs. Chunk sizes are programmable from 8 to 2040 bytes, in 8 byte increments. In packet based transfer, Envoy-CE2 will transfer the complete packet to a PHY port and will pause data transmission when the PHY device port indicates its FIFO is almost full by de-asserting its Transmit Packet available signal. Selection of another PHY port is done once a complete packet has been sent to the current PHY port. Port selection is accomplished using the first come, first serve, round robin algorithm. At the Receive interface (SPI-3 input), the PHY device will transfer packet data to the Envoy-CE2, which will globally backpressure the PHY device when any Port's Egress FIFO becomes almost full.

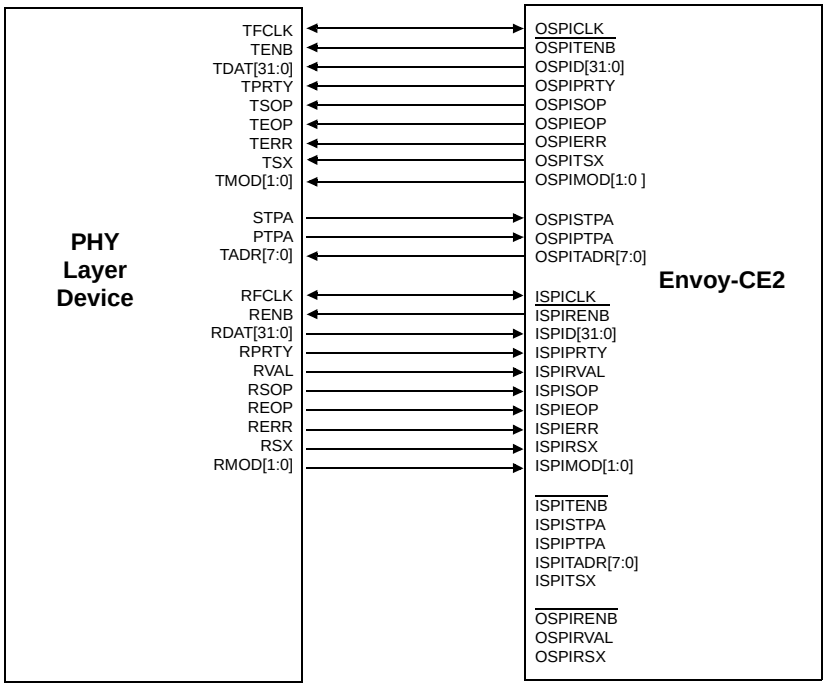


Figure 8. Envoy-CE2 in Link Layer Mode

2.1.8 Microprocessor Interface

The Envoy-CE2 configuration, status, and device management is performed via its microprocessor interface. The interface has a 15 bit wide address bus UPA(14-0) and a pin configurable 8 or 16 bit wide data bus UPD(15-0). It is compatible with standard Intel/ Motorola micro-controllers. The interface operates from a minimum clock (UPCLK) frequency of 33 MHz to a maximum clock frequency of 66 MHz.

The following table shows the Pin description for the Host interface in Intel and Motorola modes:

Envoy-CE2 Pin Name	Intel Mode Description	Motorola Mode Description
Microprocessor Clock (UPCLK)	Host Interface Clock	Host Interface Clock
Microprocessor Data Bus (UPD)	Host Data Bus	Host Data Bus
Microprocessor Address Bus (UPA)	Host Address Bus	Host Address Bus
Chip Select (CS)	Device Chip Select	Device Chip Select
Write/Transfer Start (WRDS)	Write Strobe (Active Low)	Active Low Transfer Start
Transfer Acknowledge ($\overline{\text{DTACK}}$)	Ready	Active Low Transfer Acknowledge
Read/Write (RDWR)	Read Strobe (Active Low)	Read/$\overline{\text{Write}}$ Strobe
Interrupt ($\overline{\text{IRQ}}$)	Interrupt Pin	Interrupt Pin

All internal registers (control and status) are 32 bits wide. In order to complete a write operation, all 32 bits must be written. All accesses require writing or reading the complete 32 bits. Hence, when performing a write when the Microprocessor Interface is configured as an 8 bit wide bus, it is required to do 4 writes to write to the internal register. Similarly, when doing a read when the bus is configured as an 8 bit wide bus, 4 reads need to be performed to access the register. The diagrams in Figure 21, Figure 22, Figure 23, and Figure 24 illustrate the bus accesses in Motorola and Intel modes for both read and write operations. The minimum $\overline{\text{CS}}$ to $\overline{\text{DTACK}}$ time is 6 UPCLK cycles and the maximum $\overline{\text{CS}}$ to $\overline{\text{DTACK}}$ time is 22 UPCLK cycles.

2.1.9 JTAG Boundary Scan

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in Figure 9, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register path bordering the input and output leads. The boundary scan test bus interface consists of four input signals and an output signal. The four input signals are Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and

Test Mode Reset ($\overline{\text{TRST}}$). The output signal is Test Data Output (TDO). In addition to the TAP, a pin is provided ($\overline{\text{DEVHIZ}}$) to place the output buffers in a high impedance state for systems that do not support the IEEE 1149.1 standard. Boundary scan signal timing is shown in Figure 20.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 9.

The boundary scan function can be reset and disabled by holding lead $\overline{\text{TRST}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the Envoy-CE2 device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

2.1.9.1 Boundary Scan Operation

The Envoy-CE2 supports the following boundary scan test instructions:

The EXTEST test instruction provides the ability to test the connectivity of the Envoy-CE2 device to external circuitry.

The SAMPLE/PRELOAD test instruction provides the ability to examine the values of the Input and Output pins without interfering with device operation, and to initialize the Boundary Scan Register with new values for the next operation.

The BYPASS test instruction provides the ability to bypass the Envoy-CE2 boundary scan and instruction registers.

The IDCODE test instruction provides a unique device identification for the Envoy-CE2 device.

The HIGHZ test instruction provides the ability to drive all 3-state outputs and bidirectional pins to their high impedance state.

The CLAMP test instruction provides the ability to drive the component pins of the chip from the boundary scan register, while the bypass register is selected as the serial path between TDI and TDO. The component pins will not switch while the CLAMP instruction is selected.

2.1.9.2 Boundary Scan Reset

Specific control of the $\overline{\text{TRST}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the Envoy-CE2. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value should be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the Input, Output and Input/Output Parameters section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

2.1.9.3 Boundary Scan Schematic

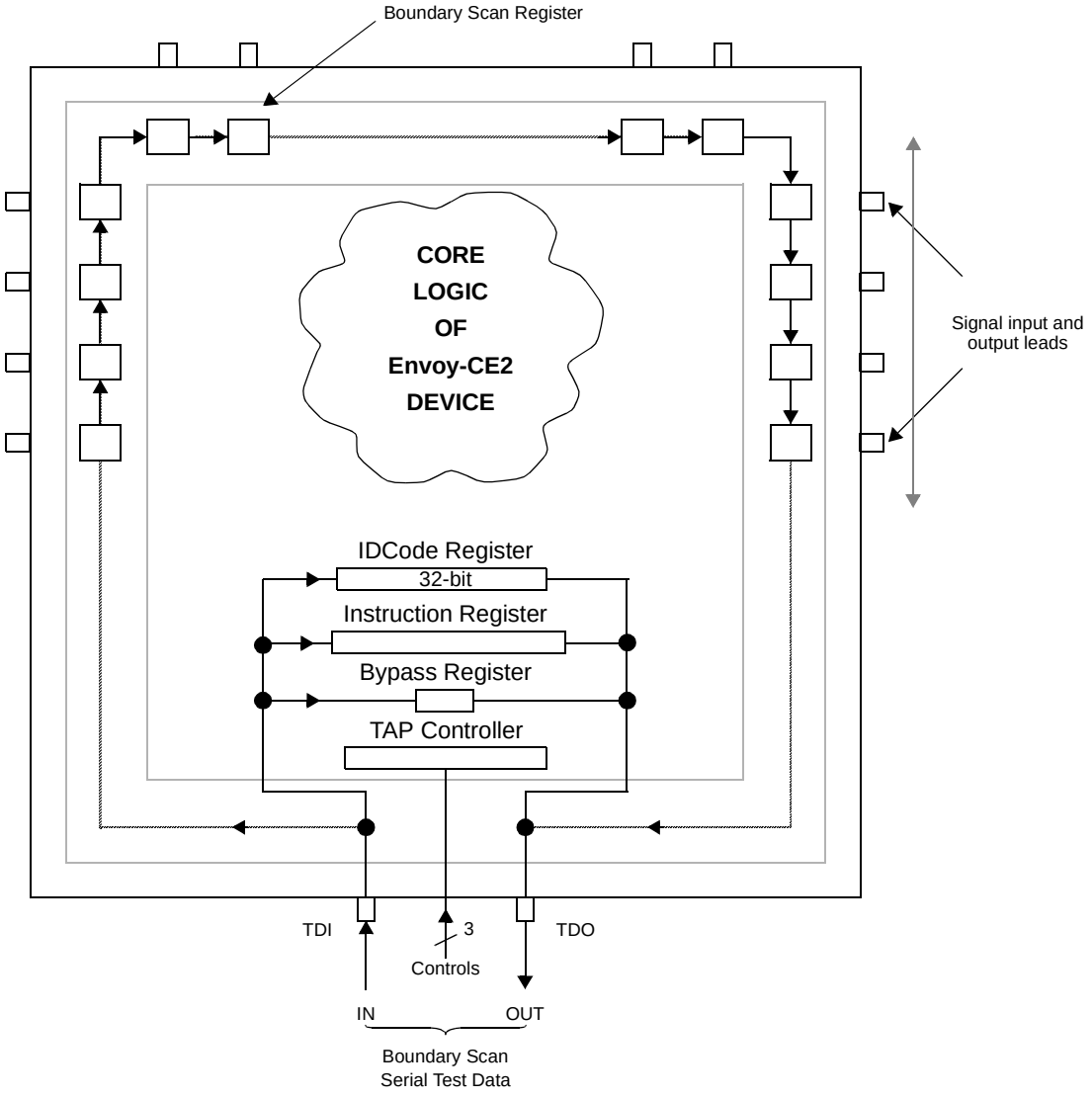


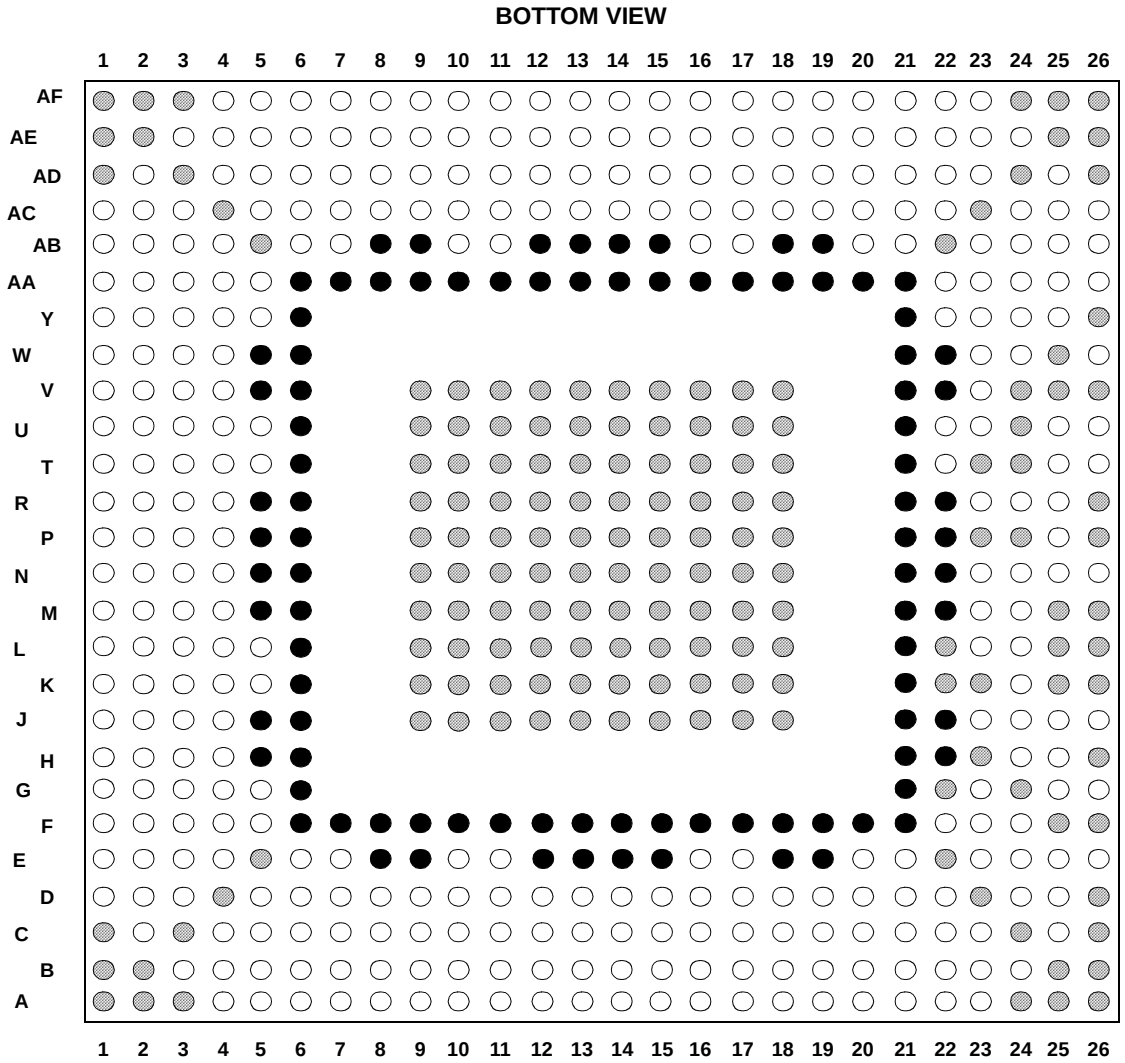
Figure 9. Boundary Scan Schematic

2.1.9.4 Boundary Scan Chain

A Boundary Scan Description Language (BSDL) source file for the Envoy-CE2 is available via the Products page of the TranSwitch Internet World Wide Web site at www.transwitch.com.

3.0 TECHNICAL CHARACTERISTICS

3.1 LEAD DIAGRAM



Notes:
1. This is the bottom view. The leads are solder balls. See Figure 25 for package information.
2. Power supply leads are shown as solid black circles and ground leads are shown as cross-hatched circles.

Figure 10. Envoy-CE2 Lead Diagram

3.2 LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECTS

Symbol	Lead No.	I/O/P *	Name/Function
VDD18	AA8, AA9, AA12, AA15, AA18, AA19, AB8, AB9, AB12, AB15, AB18, AB19, E8, E12, E15, E18, E19, F8, F9, E9, F12, F15, F18, F19, H5, H6, H21, H22, J5, J6, J21, J22, M5, M6, M21, M22, R5, R6, R21, R22, V5, V6, V21, V22, W5, W6, W21, W22	P	**V_{DD18}:** +1.8 volt ±5% CMOS core supply voltage.
VDD33	AA6, AA7, AA10, AA11, AA13, AA14, AA16, AA17, AA20, AA21, AB13, AB14, E13, E14, F6, F7, F10, F11, F13, F14, F16, F17, F20, F21, G21, G6, K6, K21, L6, L21, N5, N6, N21, N22, P5, P6, P21, P22, T6, T21, U6, U21, Y6, Y21	P	**V_{DD33}:** +3.3 volt ±5% CMOS input/output pad supply voltage.

Note: VDD18 and VDD33 Power Up Sequence. Because of the multi-power ESD structure used for CMOS I/O cells, there is a parasitic forward diode path from core power rail (V_{DD18}) to I/O power rail (V_{DD33}). So, if V_{DD18} is powered up earlier than V_{DD33}, there will be current flowing through the parasitic diode that may trigger latch-up. To avoid this problem, users can take either one of the approaches below:

(1) Power Up VDD33 First. Turning on V_{DD33} first, prevents the parasitic diode from turning on. For example, power up V_{DD33} first and then V_{DD18}. Note: TranSwitch does not recommend powering up V_{DD33} seconds earlier than V_{DD18} for reliability reasons. This is because the un-powered V_{DD18} may result in short circuit current (crowbar current) on the CMOS I/O cell's post-driver for unknown state. Bus conflict may also occur when only V_{DD33} is powered on. The maximum interval that V_{DD18} must be powered up after V_{DD33}, depends on the slew rate of power ramp-up in the customer's application.

(2) Place a Schottky Diode Between VDD18 and VDD33. If we can ensure that the parasitic diode does not turn on, we can even power up lower voltage first. This can be done by inserting an external diode between V_{DD18} and V_{DD33} on the board. By connecting the Schottky diode with anode to lower voltage rail (V_{DD18}) and cathode to higher voltage rail (V_{DD33}), we can force the latter to ramp up with the former with the voltage drop (Schottky diode Vt=150mV~200mV) less than the threshold voltage of the parasitic diode (parasitic diode Vt=500mV~600mV). This prevents from turning on the parasitic diode between power rails, avoiding latch up. The external diode will be turned off when V_{DD33} is powered up to its normal voltage.

*Note: I = Input; O = Output; P = Power; T = Tristate

Symbol	Lead No.	I/O/P *	Name/Function
VSS	A1, A2, A3, A24, A25, A26, AB5, AB22, AC4, AC23, AD1, AD3, AD24, AD26, AE1, AE2, AE25, AE26, AF1, AF2, AF3, AF24, AF25, AF26, B1, B2, B25, B26, C1, C3, C24, C26, D4, D23, D26, E5, E22, F25, F26, G22, G24, H23, H26, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K22, K23, K25, K26, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L22, L25, L26, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M25, M26, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P23, P24, P26, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R26, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T23, T24, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U24, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V24, V25, V26, W25, Y26	P	**VSS:** Ground 0 (zero) volts reference.

Symbol	Lead No.	I/O/P *	Name/Function
NC	A5, A20, A22, A23, AA25, AC8, AC17, AC22, AD2, AD4, AD10, AD13, AD23, AD25, AE3, AE8, AE19, AE20, AE24, AF8, AF17, B3, B4, B10, B21, B22, B24, C2, C9, C12, C20, C21, C23, C25, D1, D2, D3, D7, D11, D13, D15, D16, D17, D19, D20, D24, E1, E4, E6, E7, E16, E20, E23, E25, E26, F5, F22, F23, F24, G2, G23, G25, G26, H24, H25, J23, J24, J25, J26, K24, L2, L23, L24, M3, M23, M24, N23, N24, N25, N26, P25, R4, R23, R24, R25, T22, T25, T26, U5, U22, U23, U24, U26, V23, W2, W24, W26, Y1, Y25		**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. Some NC leads may be assigned functions in future upgrades of the device. Backwards compatibility of the upgraded device in existing applications may rely upon these leads having been left floating.

RESET AND TEST LEADS (INCLUDING TEST ACCESS PORT FOR BOUNDARY SCAN)

Symbol	Lead No.	I/O	Type	Name/Function
TDO	D21	O(T)	CMOS 4 mA	**Test Data Output:** Boundary scan output for data and test instructions from internal test registers.
$\overline{\text{TRST}}$	C22	I	LVTTLpu	**Test Mode Reset:** A 1 microsecond (minimum) low on this lead resets the boundary scan; recommended for use after power-up initialization as well. This lead should be held low whenever boundary scan operations are not being performed.
TMS	B23	I	LVTTLpu	**Test Mode Select:** Boundary scan test mode select. This signal must be pulled high. 4.7k Ω pull-up recommended.
TDI	E21	I	LVTTLpu	**Test Data Input:** Boundary scan input for data and test instructions. 4.7k Ω pull-up recommended.
TCK	D22	I	LVTTLpu	**Test Clock:** Boundary scan clock. Input signals are clocked in on its rising edge.

Symbol	Lead No.	I/O	Type	Name/Function
$\overline{\text{RESET}}$	B16	I	LVTLL	**Hardware Reset:** An active low pulse with minimum width of 1 ms which must be applied after power is applied to reset all registers, counters, and FIFOs. The reset is asynchronous going into the reset state, but requires all external clocks to be active and stable during the reset state.
$\overline{\text{TSTMODE}}$	A17	I	LVTTL	**Test Mode:** For TranSwitch testing purposes only. Tie to V_{DD33}. Active low to enable device test.
SCAN	C16	I	LVTTL	**SCAN Test:** For TranSwitch testing purposes only. Tie to V_{SS}. Active high to enable device internal scan test.
TEST1	B17	I	LVTTL	**Test1:** For TranSwitch testing purposes only. Tie to V_{SS}.
$\overline{\text{DEVHIZ}}$	C17	I	LVTTL	**Device High Impedance:** Active low to set all outputs (except TDO) to high impedance state. Tie to V_{DD33}.

INTEL/MOTOROLA HOST INTERFACE

Symbol	Lead No.	I/O/P*	Type	Name/Function
UPCLK	C15	I	LVTTL	**Microprocessor Clock:** This clock should come from the microprocessor being interfaced to this device. For Intel and Motorola modes, it is recommended that this lead be connected to the microprocessor bus clock. In Motorola mode, this clock must be synchronous to the microprocessor bus clock. Maximum frequency of 66 MHz, minimum frequency of 33 MHz.
$\overline{\text{CS}}$	A4	I	LVTTL	**Chip Select:** Chip select lead from Host. Active low assertion.
$\overline{\text{DTACK}}$	A16	O	CMOS 24 mA	**Transfer Acknowledge:** Active low signal indicating normal completion of the bus transfer. This output requires an external pull-up resistor. **Note:** Device asserts this high before tri-stating to improve acknowledge timing.

Symbol	Lead No.	I/O/P*	Type	Name/Function
UPA14 UPA13 UPA12 UPA11 UPA10 UPA9 UPA8 UPA7 UPA6 UPA5 UPA4 UPA3 UPA2 UPA1 UPA0	A15 D14 C14 B14 A14 A13 B13 C13 A12 B12 A11 D12 B11 C11 A10	I	LVTTL	**Microprocessor Address Bus:** 15-bit address bus used by the Host Processor for accessing the Envoy-CE2 for a read/write cycle. UPA14 is the Most Significant Bit (MSB).
UPD15 UPD14 UPD13 UPD12 UPD11 UPD10 UPD9 UPD8 UPD7 UPD6 UPD5 UPD4 UPD3 UPD2 UPD1 UPD0	C10 E11 A9 D10 B9 A8 E10 B8 D9 A7 C8 B7 A6 D8 C7 B6	I/O	LVTTL/ CMOS 16 mA	**Microprocessor Data Bus:** Bi-directional 16-bit data bus used for transferring data between the Envoy-CE2 and the Host Processor. UPD15 is the Most Significant Bit (MSB).
WRDS	B5	I	LVTTL	**Write/Transfer Start:** In Intel Mode, this pin is used for the Write signal and in Motorola mode, this pin is used for the active low Transfer start signal.
RDWR	C6	I	LVTTL	**Read/Write:** In Intel Mode, this pin is used for the Read signal and in Motorola mode, this pin controls type of data transfer (Write = 0/Read = 1).
$\overline{\text{IRQ}}$	B15	O(T)	CMOS 16mA	**Interrupt:** Active low level-based interrupt to Host processor.

COMMON SMII INTERFACES PINS FOR ALL SMII PORTS (Ports 0 to 15) including extended SMII ports

Symbol	Lead No.	I/O/P*	Type	Name/Function
SSYNCIN	D25	I	LVTTL	**Synchronization Input Pulse:** Global input signal that occurs every 10 SMIIREFCLK clock cycles and marks the start of data segments.
SSYNCDIR	E24	I	LVTTL	**Synchronization Pulse Direction:** Determines the source of the synchronization pulse. 0 - The synchronization pulse will be taken from an internally generated source 1 - The synchronization pulse to the 8 SMII ports will be taken from SSYNCIN

SMII INTERFACE PINS FOR Configurable MAC A (Ports 0 to 7).
Extended SMII Ports are Ports 0 and 4

Symbol	Lead No.	I/O/P*	Type	Name/Function
SMIIREFCLKA	F1	I	LVTTL	**SMII Reference Clock for Configurable MAC A:** 125 MHz Clock. Must be active to support the Ethernet statistics registers of CMAC A - even when the CMAC is configured for GMII Mode.
SSYNCOUTA	H4	O	CMOS 12mA	**Synchronization Output Pulse for Configurable MAC A:** Global output signal that occurs every 10 SMIIREFCLKA clock cycles and marks the start of data segments.
TX0A	H3	O	CMOS 12mA	**Transmit Data Port 0:** SMII port 0 data out signal.
RX0A	G1	I	LVTTL	**Receive Data Port 0:** SMII port 0 data in signal.
TX1A	J4	O	CMOS 12mA	**Transmit Data Port 1:** SMII port 1 data out signal.
RX1A	H2	I	LVTTL	**Receive Data Port 1:** SMII port 1 data in signal.
TX2A	K5	O	CMOS 12mA	**Transmit Data Port 2:** SMII port 2 data out signal.
RX2A	J3	I	LVTTL	**Receive Data Port 2:** SMII port 2 data in signal.
TX3A	H1	O	CMOS 12mA	**Transmit Data Port 3:** SMII port 3 data out signal.
RX3A	J2	I	LVTTL	**Receive Data Port 3:** SMII port 3 data in signal.
TX4A	K4	O	CMOS 12mA	**Transmit Data Port 4:** SMII port 4 data out signal.
RX4A	J1	I	LVTTL	**Receive Data Port 4:** SMII port 4 data in signal.

Symbol	Lead No.	I/O/P*	Type	Name/Function
TX5A	L5	O	CMOS 12mA	**Transmit Data Port 5:** SMII port 5 data out signal.
RX5A	K3	I	LVTTL	**Receive Data Port 5:** SMII port 5 data in signal.
TX6A	K2	O	CMOS 12mA	**Transmit Data Port 6:** SMII port 6 data out signal
RX6A	L4	I	LVTTL	**Receive Data Port 6:** SMII port 6 data in signal.
TX7A	K1	O	CMOS 12mA	**Transmit Data Port 7:** SMII port 7 data out signal.
RX7A	L3	I	LVTTL	**Receive Data Port 7:** SMII port 7 data in signal.

SMII INTERFACE PINS FOR Configurable MAC B (Ports 8 to 15).
Extended SMII Ports are Ports 8 and 12

Symbol	Lead No.	I/O/P*	Type	Name/Function
SMIIREFCLKB	P4	I	LVTTL	**SMII Reference Clock for Configurable MAC B:** 125 MHz Clock. Must be active to support the Ethernet statistics registers of CMAC B - even when the CMAC is configured for GMII Mode.
SSYNCOUTB	P3	O	CMOS 12mA	**Synchronization Output Pulse for Configurable MAC B:** Global output signal that occurs every 10 SMIIREFCLKB clock cycles and marks the start of data segments.
TX0B	R1	O	CMOS 12mA	**Transmit Data Port 8:** SMII port 8 data out signal.
RX0B	R2	I	LVTTL	**Receive Data Port 8:** SMII port 8 data in signal.
TX1B	R3	O	CMOS 12mA	**Transmit Data Port 9:** SMII port 9 data out signal.
RX1B	T1	I	LVTTL	**Receive Data Port 9:** SMII port 9 data in signal.
TX2B	T2	O	CMOS 12mA	**Transmit Data Port 10:** SMII port 10 data out signal.
RX2B	T3	I	LVTTL	**Receive Data Port 10:** SMII port 10 data in signal.
TX3B	U1	O	CMOS 12mA	**Transmit Data Port 11:** SMII port 11 data out signal.
RX3B	T4	I	LVTTL	**Receive Data Port 11:** SMII port 11 data in signal.
TX4B	U2	O	CMOS 12mA	**Transmit Data Port 12:** SMII port 12 data out signal.
RX4B	U3	I	LVTTL	**Receive Data Port 12:** SMII port 12 data in signal.

Symbol	Lead No.	I/O/P*	Type	Name/Function
TX5B	T5	O	CMOS 12mA	**Transmit Data Port 13:** SMII port 13 data out signal.
RX5B	V1	I	LVTTL	**Receive Data Port 13:** SMII port 13 data in signal.
TX6B	U4	O	CMOS 12mA	**Transmit Data Port 14:** SMII port 14 data out signal.
RX6B	V2	I	LVTTL	**Receive Data Port 14:** SMII port 14 data in signal.
TX7B	W1	O	CMOS 12mA	**Transmit Data Port 15:** SMII port 15 data out signal.
RX7B	V3	I	LVTTL	**Receive Data Port 15:** SMII port 15 data in signal.

GMII/MII INTERFACE PINS FOR GMII Port 0 (Configurable MAC A)
(SMIIREFCLKA must be active)

Symbol	Lead No.	I/O/P*	Type	Name/Function
SMIIREFCLKA	F1	I	LVTTL	**SMII Reference Clock for Configurable MAC A:** 125 MHz Clock. Must be active to support the Ethernet statistics registers of CMAC A - even when the CMAC is configured for GMII Mode.
GATXCLKO	G3	O	CMOS 16mA	**GMII A Transmit Clock Output:** 125 MHz output clock to which Data, Enable, and Error output signals are synchronized.
GATXCLKI	C4	I	LVTTL	**GMII A Transmit Clock:** 125 MHz input clock
GARXCLK	E3	I	LVTTL	**GMII A Receive Clock:** 125 MHz input clock
GATXEN	F4	O	CMOS 8mA	**GMII A Transmit Enable:** This active high output signal is asserted to indicate that valid data is present on the Data outputs.
GATXER	G5	O	CMOS 8mA	**GMII A Transmit Error:** This active high output signal is asserted to indicate that a coding violation exists in the output data stream.
GARXDV	G4	I	LVTTL	**GMII A Receive Data Valid:** This active high input signal is asserted to indicate that valid data is present on the input data leads.
GARXER	F2	I	LVTTL	**GMII A Receive Error:** This active high input signal is asserted to indicate that an error was detected in the incoming data stream.
TX0A	H3	O	CMOS 12mA	**Transmit Data Port 0A:** Bit 0 (LSB) of 8-bit GMII A Transmit Interface in GMII mode or Bit 0 of 4-bit MII A Transmit interface.
RX0A	G1	I	LVTTL	**Receive Data Port 0A:** Bit 0 (LSB) of 8-bit GMII A Receive Interface in GMII mode or Bit 0 of 4-bit MII A Receive interface.

Symbol	Lead No.	I/O/P*	Type	Name/Function
TX1A	J4	O	CMOS 12mA	**Transmit Data Port 1A:** Bit 1 of 8-bit GMII A Transmit Interface in GMII mode or Bit 1 of 4-bit MII A Transmit interface.
RX1A	H2	I	LVTTL	**Receive Data Port 1A:** Bit 1 of 8-bit GMII A Receive Interface in GMII mode or Bit 1 of 4-bit MII A Receive interface.
TX2A	K5	O	CMOS 12mA	**Transmit Data Port 2A:** Bit 2 of 8-bit GMII A Transmit Interface in GMII mode or Bit 2 of 4-bit MII A Transmit interface.
RX2A	J3	I	LVTTL	**Receive Data Port 2A:** Bit 2 of 8-bit GMII A Receive Interface in GMII mode or Bit 2 of 4-bit MII A Receive interface.
TX3A	H1	O	CMOS 12mA	**Transmit Data Port 3A:** Bit 3 of 8-bit GMII A Transmit Interface in GMII mode or Bit 3 of 4-bit MII A Transmit interface.
RX3A	J2	I	LVTTL	**Receive Data Port 3A:** Bit 3 of 8-bit GMII A Receive Interface in GMII mode or Bit 3 of 4-bit MII A Receive interface.
TX4A	K4	O	CMOS 12mA	**Transmit Data Port 4A:** Bit 4 of 8-bit GMII A Transmit Interface in GMII mode.
RX4A	J1	I	LVTTL	**Receive Data Port 4A:** Bit 4 of 8-bit GMII A Receive Interface in GMII mode.
TX5A	L5	O	CMOS 12mA	**Transmit Data Port 5A:** Bit 5 of 8-bit GMII A Transmit Interface in GMII mode.
RX5A	K3	I	LVTTL	**Receive Data Port 5A:** Bit 5 of 8-bit GMII A Receive Interface in GMII mode.
TX6A	K2	O	CMOS 12mA	**Transmit Data Port 6A:** Bit 6 of 8-bit GMII A Transmit Interface in GMII mode.
RX6A	L4	I	LVTTL	**Receive Data Port 6A:** Bit 6 of 8-bit GMII A Receive Interface in GMII mode.
TX7A	K1	O	CMOS 12mA	**Transmit Data Port 7A:** Bit 7 (MSB) of 8-bit GMII A Transmit Interface in GMII mode.
RX7A	L3	I	LVTTL	**Receive Data Port 7A:** Bit 7 (MSB) of 8-bit GMII A Receive Interface in GMII mode.
GACOL	F3	I	LVTTL	**GMII A (MII Mode) Collision:** This active high input signal is the collision lead used in MII mode for the GMII A interface.
GACRS	E2	I	LVTTL	**GMII A (MII Mode) Carrier Sense:** This active high input signal is the carrier sense lead used in MII mode for the GMII A interface.
GAMTXCLK	D5	I	LVTTL	**GMII A (MII Mode) TXCLK:** This is the TXCLK signal used in MII mode for the GMII A interface.

GMII/MII INTERFACE PINS FOR GMII Port 8 (Configurable MAC B)
(SMIIREFCLKB must be active)

Symbol	Lead No.	I/O/P*	Type	Name/Function
SMIIREFCLKB	P4	I	LVTTL	**SMII Reference Clock for Configurable MAC B:** 125 MHz Clock. Must be active to support the Ethernet statistics registers of CMAC B - even when the CMAC is configured for GMII Mode.
GBTXCLKO	P2	O	CMOS 16mA	**GMII B Transmit Clock Output:** 125 MHz output clock to which Data, Enable, and Error output signals are synchronized.
GBTXCLKI	L1	I	LVTTL	**GMII B Transmit Clock:** 125 MHz input clock
GBRXCLK	M2	I	LVTTL	**GMII B Receive Clock:** 125 MHz input clock
GBTXEN	M1	O	CMOS 8mA	**GMII B Transmit Enable:** This active high output signal is asserted to indicate that valid data is present on the Data outputs.
GBTXER	N4	O	CMOS 8mA	**GMII B Transmit Error:** This active high output signal is asserted to indicate that a coding violation exists in the output data stream.
GBRXDV	N1	I	LVTTL	**GMII B Receive Data Valid:** This active high input signal is asserted to indicate that valid data is present on the input data leads.
GBRXER	P1	I	LVTTL	**GMII B Receive Error:** This active high input signal is asserted to indicate that an error was detected in the incoming data stream.
TX0B	R1	O	CMOS 12mA	**Transmit Data Port 0B:** Bit 0 (LSB) of 8-bit GMII B Transmit Interface in GMII mode or Bit 0 of 4-bit MII B Transmit interface.
RX0B	R2	I	LVTTL	**Receive Data Port 0B:** Bit 0 (LSB) of 8-bit GMII B Receive Interface in GMII mode or Bit 0 of 4-bit MII B Receive interface.
TX1B	R3	O	CMOS 12mA	**Transmit Data Port 1B:** Bit 1 of 8-bit GMII B Transmit Interface in GMII mode or Bit 1 of 4-bit MII B Transmit interface.
RX1B	T1	I	LVTTL	**Receive Data Port 1B:** Bit 1 of 8-bit GMII B Receive Interface in GMII mode or Bit 1 of 4-bit MII B Receive interface.
TX2B	T2	O	CMOS 12mA	**Transmit Data Port 2B:** Bit 2 of 8-bit GMII B Transmit Interface in GMII mode or Bit 2 of 4-bit MII B Transmit interface.
RX2B	T3	I	LVTTL	**Receive Data Port 2B:** Bit 2 of 8-bit GMII B Receive Interface in GMII mode or Bit 2 of 4-bit MII B Receive interface.

Symbol	Lead No.	I/O/P*	Type	Name/Function
TX3B	U1	O	CMOS 12mA	**Transmit Data Port 3B:** Bit 3 of 8-bit GMII B Transmit Interface in GMII mode or Bit 3 of 4-bit MII B Transmit interface.
RX3B	T4	I	LVTTL	**Receive Data Port 3B:** Bit 3 of 8-bit GMII B Receive Interface in GMII mode or Bit 3 of 4-bit MII B Receive interface.
TX4B	U2	O	CMOS 12mA	**Transmit Data Port 4B:** Bit 4 of 8-bit GMII B Transmit Interface in GMII mode.
RX4B	U3	I	LVTTL	**Receive Data Port 4B:** Bit 4 of 8-bit GMII B Receive Interface in GMII mode.
TX5B	T5	O	CMOS 12mA	**Transmit Data Port 5B:** Bit 5 of 8-bit GMII B Transmit Interface in GMII mode.
RX5B	V1	I	LVTTL	**Receive Data Port 5B:** Bit 5 of 8-bit GMII B Receive Interface in GMII mode.
TX6B	U4	O	CMOS 12mA	**Transmit Data Port 6B:** Bit 6 of 8-bit GMII B Transmit Interface in GMII mode.
RX6B	V2	I	LVTTL	**Receive Data Port 6B:** Bit 6 of 8-bit GMII B Receive Interface in GMII mode.
TX7B	W1	O	CMOS 12mA	**Transmit Data Port 7B:** Bit 7 (MSB) of 8-bit GMII B Transmit Interface in GMII mode.
RX7B	V3	I	LVTTL	**Receive Data Port 7B:** Bit 7 (MSB) of 8-bit GMII B Receive Interface in GMII mode.
GBCOL	N2	I	LVTTL	**GMII B (MII Mode) Collision:** This active high input signal is the collision lead used in MII mode for the GMII B interface.
GBCRS	N3	I	LVTTL	**GMII B (MII Mode) Carrier Sense:** This active high input signal is the carrier sense lead used in MII mode for the GMII B interface.
GBMTXCLK	M4	I	LVTTL	**GMII B (MII Mode) TXCLK:** This is the TXCLK signal used in MII mode for the GMII B interface.

Note: The GMII is a 3.3 V interface that will only work with a 3.3 V PHY device.

MII MANAGEMENT PINS

Symbol	Lead No.	I/O/P*	Type	Name/Function
MDC	C5	O	CMOS 16mA	**Management Data Interface Clock:** Management data (MDIO signal) is clocked into and out of the device on the rising edge of this clock.
MDIO	D6	I/O	LVTTL/ CMOS 16mA	**Management Data I/O:** I/O data lead for the IEEE 802.3u compliant management and status interface.

SPI-3 INTERFACE - Data Input

Symbol	Lead No.	I/O/P*	Type	Name/Function
ISPICLK	AC13	I	LVTTL	**SPI-3 Input Clock:** Maximum of 125 MHz.
ISPID31 ISPID30 ISPID29 ISPID28 ISPID27 ISPID26 ISPID25 ISPID24 ISPID23 ISPID22 ISPID21 ISPID20 ISPID19 ISPID18 ISPID17 ISPID16 ISPID15 ISPID14 ISPID13 ISPID12 ISPID11 ISPID10 ISPID9 ISPID8 ISPID7 ISPID6 ISPID5 ISPID4 ISPID3 ISPID2 ISPID1 ISPID0	AD7 AE6 AF5 AC7 AD6 AE5 AF4 AB7 AC6 AD5 AE4 AB6 AC5 AC3 AB4 AA5 AC2 AB3 AA4 Y5 AC1 AB2 AA3 Y4 AB1 AA2 Y3 W4 AA1 Y2 W3 V4	I	LVTTL	**SPI-3 Input Data Bus:** 32-bit bus used to receive data from the Link or PHY Layer device. 8-bit SPI-3 Mode: ISPID(7-0); ISPID7 is MSB. 16-bit SPI-3 Mode: ISPID(15-0); ISPID15 is MSB. 32-bit SPI-3 Mode: ISPID(31-0); ISPID31 is MSB.
ISPIPRTY	AF6	I	LVTTL	**SPI-3 Input Bus Parity:** This input signal indicates the parity calculated over the ISPID(31-0) bus, when start of transfer or read (Link layer mode)/write (PHY layer mode) enable signals are asserted.

Symbol	Lead No.	I/O/P*	Type	Name/Function
ISPIMOD1 ISPIMOD0	AD8 AE7	I	LVTTL	**SPI-3 Input Data Word Modulo:** These 2 inputs indicate the number of valid data bytes in ISPID(31-0). The ISPIMOD bus should always be all zero, except during the last double-word transfer of a frame on ISPID(31-0). 00 - ISPID(31-0) Valid 01 - ISPID(31-8) Valid 10 - ISPID(31-16) Valid 11 - ISPID(31-24) Valid
ISPISOP	AF7	I	LVTTL	**SPI-3 Input Start of Frame:** This active high input is used to delineate the frame boundaries on the ISPID(31-0) bus. When ISPISOP is high, the start of the frame is present on ISPID(31-0).
ISPIEOP	AC9	I	LVTTL	**SPI-3 Input End of Frame:** This input signal is used to delineate the frame boundaries on the ISPID(31-0) bus. When high, the end of the frame is present on ISPID(31-0).
ISPIERR	AB10	I	LVTTL	**SPI-3 Input Error Indicator:** This active high input signal is used to indicate that the current frame should be discarded.
ISPITSX	AE9	I	LVTTL	**SPI-3 Input PHY Mode Transmit Start of Transfer:** This active high input signal indicates when the in-bound port address is present on ISPID(31-0).
ISPITENB	AD9	I	LVTTL	**SPI-3 Input PHY Mode Transmit Write Enable:** This active low input signal is used to control the flow of data to the transmit FIFOs.
ISPITADR7 ISPITADR6 ISPITADR5 ISPITADR4 ISPITADR3 ISPITADR2 ISPITADR1 ISPITADR0	AE11 AD11 AF10 AC11 AE10 AB11 AF9 AC10	I	LVTTL	**SPI-3 Input PHY Mode Transmit Address:** 8-bit bus containing the PHY address. ISPITADR7 is MSB.
ISPISTPA	AC12	O	CMOS 12mA	**SPI-3 Input PHY Mode Selected Transmit Packet Available:** Active high output used to indicate that space is available in the Egress FIFO specified on the inbound address on ISPID(31-0). This signal is used only for byte level flow control.
ISPIPTPA	AF11	O	CMOS 12mA	**SPI-3 Input PHY Mode Polled Transmit Packet Available:** Active high output used to indicate that space is available in the polled Egress FIFO. This signal is used only for packet level flow control.

Symbol	Lead No.	I/O/P*	Type	Name/Function
ISPIRENB	AD12	O	CMOS 12mA	**SPI-3 Input Link Mode Receive Read Enable:** Active low signal used as read enable.
ISPIRVAL	AE12	I	LVTTL	**SPI-3 Input Link Mode Receive Data Valid:** Signal indicating valid data on the data bus ISPID(31-0)
ISPIRSX	AF12	I	LVTTL	**SPI-3 Input Link Mode Receive Start of Transfer:** Signal indicating start of data transfer in Link layer mode.

SPI-3 INTERFACE - Data Out

Symbol	Lead No.	I/O/P*	Type	Name/Function
OSPICLK	AE22	I	LVTTL	**SPI-3 Output Clock:** Minimum of 50 MHz and maximum of 125 MHz for SPI-3 emulation.
OSPID31 OSPID30 OSPID29 OSPID28 OSPID27 OSPID26 OSPID25 OSPID24 OSPID23 OSPID22 OSPID21 OSPID20 OSPID19 OSPID18 OSPID17 OSPID16 OSPID15 OSPID14 OSPID13 OSPID12 OSPID11 OSPID10 OSPID9 OSPID8 OSPID7 OSPID6 OSPID5 OSPID4 OSPID3 OSPID2 OSPID1 OSPID0	AD21 AC20 AF22 AE21 AD20 AC19 AF21 AD19 AF20 AC18 AB17 AD18 AF19 AE18 AF18 AB16 AD17 AE17 AC16 AD16 AE16 AC15 AF16 AD15 AE15 AF15 AC14 AD14 AE14 AF14 AF13 AE13	O	CMOS 12mA	**SPI-3 Output Data Bus:** 32-bit bus used to transmit data to the Link Layer device. 8-bit SPI-3 Mode: OSPID(7-0); OSPID7 is MSB. 16-bit SPI-3 Mode: OSPID(15-0); OSPID15 is MSB. 32-bit SPI-3 Mode: OSPID(31-0); OSPID31 is MSB.

Symbol	Lead No.	I/O/P*	Type	Name/Function
OSPIPRTY	Y22	O	CMOS 12mA	**SPI-3 Output Bus Parity:** This output signal indicates the parity calculated over OSPID(31-0) bus.
OSPIMOD1 OSPIMOD0	AB25 AC26	O	CMOS 12mA	**SPI-3 Output Data Word Modulo:** These 2 inputs indicate the number of valid data bytes in OSPID(31-0). The OSPIMOD bus should always be all zero, except during the last double-word transfer of a frame on OSPID(31-0). 00 - OSPID(31-0) Valid 01 - OSPID(31-8) Valid 10 - OSPID(31-16) Valid 11 - OSPID(31-24) Valid
OSPISOP	AA24	O	CMOS 12mA	**SPI-3 Output Start of Frame:** This active high input is used to delineate the frame boundaries on the OSPID(31-0) bus. When OSPISOP is high, the start of the frame is present on OSPID(31-0).
OSPIEOP	Y23	O	CMOS 12mA	**SPI-3 Output End of Frame:** This output signal is used to delineate the frame boundaries on the OSPID(31-0) bus. When OSPIEOP is high, the end of the frame is present on OSPID(31-0).
OSPIERR	AB26	O	CMOS 12mA	**SPI-3 Output Error Indicator:** This active high output signal is used to indicate that the current frame is aborted and should be discarded.
OSPIRSX	AA26	O	CMOS 12mA	**SPI-3 Output PHY Mode Receive Start of Transfer:** This active high output signal indicates when the in-bound port address is present on OSPID(31-0).
$\overline{\text{OSPIRENB}}$	Y24	I	LVTTL	**SPI-3 Output PHY Mode Receive Read Enable:** This active low input signal is used to control the flow of data from the Ingress FIFOs.
OSPIRVAL	W23	O	CMOS 12mA	**SPI-3 Output PHY Mode Receive Data Valid:** Active high output signal that validates the OSPID(31-0), OSPIPRTY, OSPIMOD(1:0), OSPISOP, OSPIEOP, and OSPIERR signals. OSPIRVAL will transition low when the receive FIFO is empty or at the end of a frame.
$\overline{\text{OSPITENB}}$	AA22	O	CMOS 12mA	**SPI-3 Output Link Mode Transmit Write Enable:** Active low write enable signal.
OSPITADR7 OSPITADR6 OSPITADR5 OSPITADR4 OSPITADR3 OSPITADR2 OSPITADR1 OSPITADR0	AB23 AC24 AB21 AE23 AD22 AC21 AB20 AF23	O	CMOS 12mA	**SPI-3 Output Link Mode Transmit Address:** Address in Link mode for addressing Multiple PHY devices. OSPITADR7 is MSB.

Symbol	Lead No.	I/O/P*	Type	Name/Function
OSPITSX	AA23	O	CMOS 12mA	**SPI-3 Output Link Mode Transmit Start of Transfer:** Signal indicating start of data transfer
OSPISTPA	AB24	I	LVTTL	**SPI-3 Output Link Mode Selected Transmit Packet Available:** Signal indicating packet available status from the selected PHY layer device. This signal is used only for byte level transfer mode.
OSPIPTPA	AC25	I	LVTTL	**SPI-3 Output Link Mode Polled Transmit Packet Available:** Signal indicating packet available status from the PHY layer device whose address is indicated on address bus OSPITADR(7-0). This signal is used only for packet level transfer mode.

CONFIGURATION PINS

Symbol	Lead No.	I/O/P*	Type	Name/Function
CFGUPBW	B18	I	LVTTL	**Host Bus Width:** Host I/F bus width select. 0 - 16 bits 1 - 8 bits
CFGOSPIMD	A19	I	LVTTL	**SPI-3 Output Mode Select:** Output SPI-3 mode select. 0 - SPI-3 in Slave mode 1 - SPI-3 in Master mode
CFGISPIMD	C18	I	LVTTL	**SPI-3 Input Mode Select:** Input SPI-3 mode select. 0 - SPI-3 in Slave mode 1 - SPI-3 in Master mode
CFGSPIBW1 CFGSPIBW0	B19 E17	I	LVTTL	**SPI-3 Data Bus Width:** SPI-3 Data Bus Width select. 00 - 32-bit mode 01 - 16-bit mode 10 - 8-bit mode 11 - Reserved
CFGCMACA1 CFGCMACA0	C19 D18	I	LVTTL	**Configuration for CMACA (Configurable MAC A) Ports 0 to 7:** Ethernet interface mode select 00 - OFF 01 - 1 GMII/MII 10 - 2 Extended SMII 11 - 8 SMII

Symbol	Lead No.	I/O/P*	Type	Name/Function
CFGCMACB1 CFGCMACB0	A21 B20	I	LVTTL	**Configuration for CMACB (Configurable MAC B)** **Ports 8 to 15:** Ethernet interface mode select 00 - OFF 01 - 1 GMII/MII 10 - 2 Extended SMII 11 - 8 SMII
CFGUPMD	A18	I	LVTTL	**Configuration Pin for selecting Host processor interface mode:** 0 - Host Interface in Intel Mode 1 - Host Interface in Motorola Mode

4.0 SELECTED PARAMETER VALUES

4.1 ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	$V_{DD1.8}$	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	$V_{DD3.3}$	-0.3	3.9	V	Notes 1, 4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 5
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	Per IPC/JEDEC J-STD-020B
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	Non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-Up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.8V only.
5. Envoy-CE2 is 5V compatible in the sense that the output logic 1 (VOH) and output logic 0 (VOL) levels of the Envoy-CE2 outputs have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 for the 5V environment. Envoy-CE2 can generally be expected to drive 5V TTL compatible components. However, while Envoy-CE2 outputs are able to meet the minimum input logic switching levels (VIH and VIL) of 5V TTL compatible components, the output logic 1 output voltage of some 5V components may exceed the maximum input voltage of Envoy-CE2. Depending on the technology and circuit implementation, the 5V TTL compatible components may drive their outputs anywhere from 3V to their VDD supply level.

   CAUTION: Before connecting a 5V component to the Envoy-CE2, always check to be sure that the Maximum VOH of the 5V device does not exceed the specified Maximum VIN listed in the table above.

4.2 THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient	-	15.6	-	°C/W	Package mounted on 4-layer JEDEC board

4.3 POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{DD3.3}$	3.15	3.3	3.45	V	
$I_{DD3.3}$	95	100	105	mA	Temp = -40° to +85 °C
$P_{DD3.3}$	0.299	0.330	0.362	W	Temp = -40° to +85 °C
$V_{DD1.8}$	1.71	1.8	1.89	V	
$I_{DD1.8}$	950	1000	1050	mA	Temp = -40° to +85 °C
$P_{DD1.8}$	1.624	1.80	1.984	W	Temp = -40° to +85 °C
Total Power	1.923	2.13	2.346	W	

4.4 INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

4.4.1 Input Parameters For LVTTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

4.4.2 Input Parameters For LVTTLpu (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	-90		-25	µA	$V_{IN} = V_{SS}$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$
Input capacitance		5		pF	

4.4.3 Output Parameters For CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -8 mA
V_{OL}			0.4	V	I_{OL} = 8 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
Leakage Tristate	-10		10	µA	

4.4.4 Output Parameters For CMOS 12mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -12 mA
V_{OL}		0.2	0.4	V	I_{OL} = 12 mA
I_{OL}			12.0	mA	
I_{OH}			-12.0	mA	
Leakage Tristate	-10		10	µA	

4.4.5 Output Parameters For CMOS 16mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -16 mA
V_{OL}		0.2	0.4	V	I_{OL} = 16 mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	
Leakage Tristate	-10		10	µA	

4.4.6 Input/Output Parameters For LVTTL/CMOS 8mA

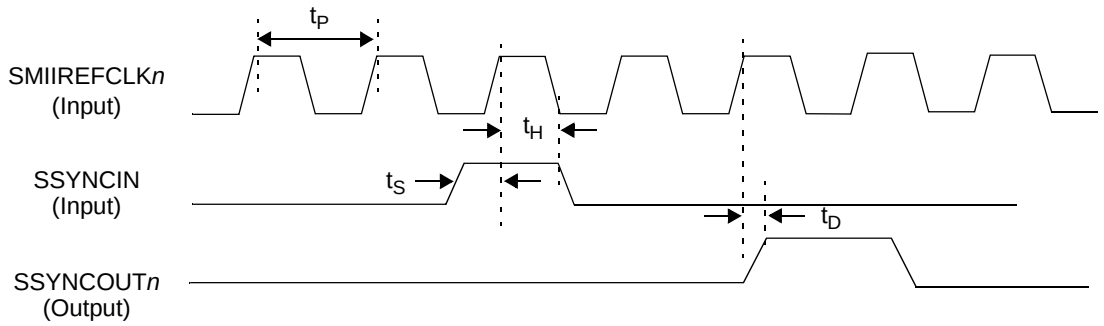
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	V_{DD33} = 3.46
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33}= 3.14; I_{OH} = -8 mA
V_{OL}			0.4	V	V_{DD33}= 3.14; I_{OL} = 8 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

4.4.7 Input/Output Parameters For LVTTL/CMOS 16mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{DD33} = 3.46$
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33}= 3.14$; $I_{OH} = -16$ mA
V_{OL}			0.4	V	$V_{DD33}= 3.14$; $I_{OL} = -16$ mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	

5.0 TIMING CHARACTERISTICS

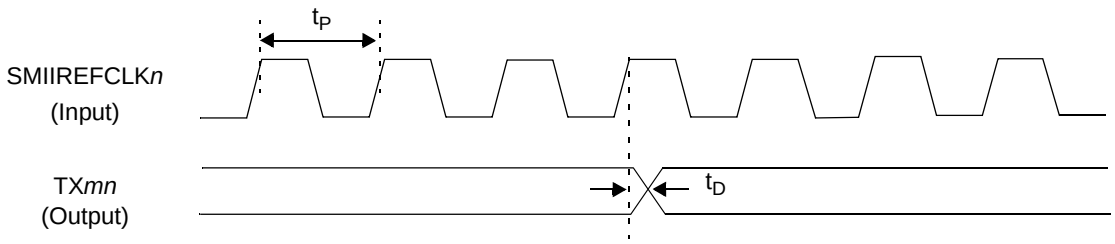
Figure 11. SMII Sync In/Out Timing



n = A, B

Parameter	Symbol	Min	Typ	Max	Unit
SMIIREFCLK*n* period	t_P		8		ns
SMIIREFCLK*n* duty cycle		45		55	%
SSYNCIN setup time to SMIIREFCLK*n* ↑	t_S	1.5			ns
SSYNCIN hold time from SMIIREFCLK*n* ↑	t_H	1			ns
SSYNCOUT*n* delay from SMIIREFCLK*n* ↑	t_D	1.5		5	ns

Figure 12. SMII Transmit Interface Timing

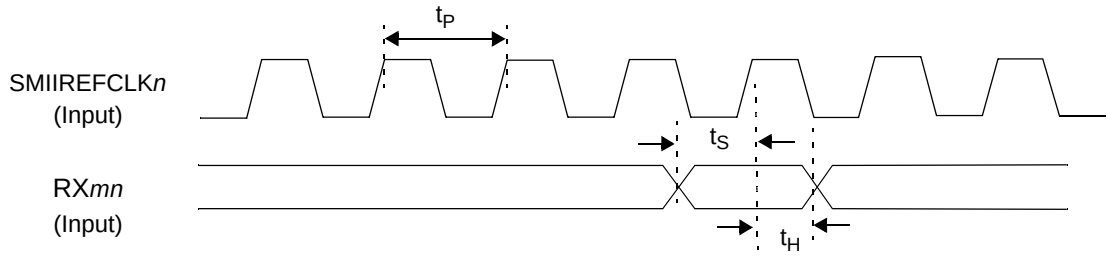


Note: 10 pF Load on All Outputs

m = 0 to 7, *n* = A, B

Parameter	Symbol	Min	Typ	Max	Unit
TX*mn* delay from SMIIREFCLK*n* ↑	t_D	1.5		5	ns

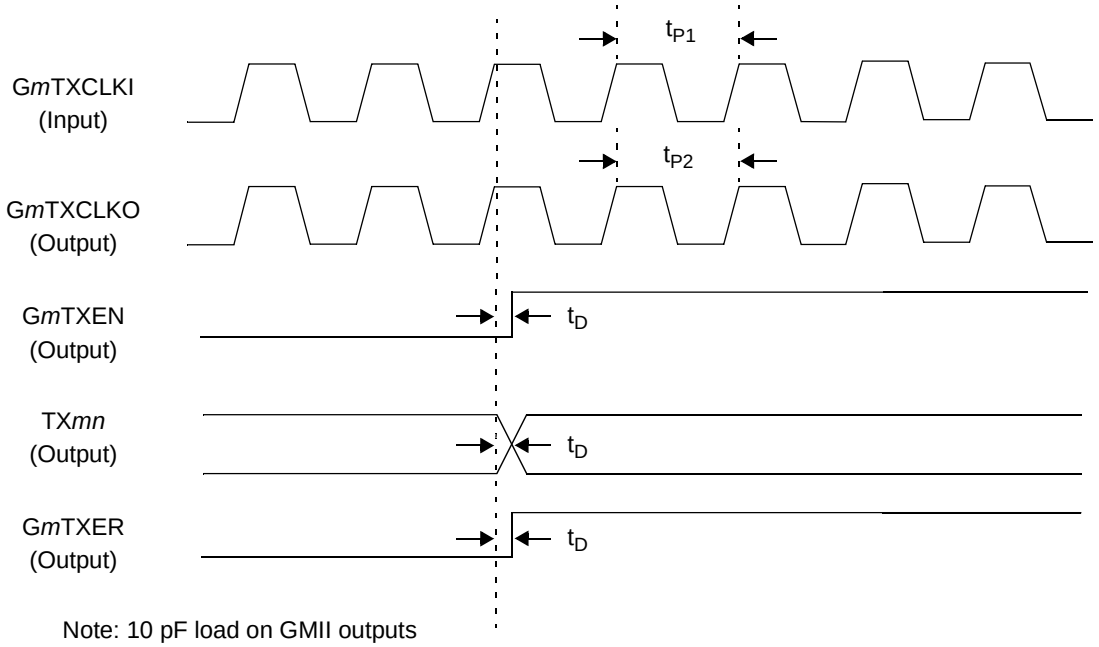
Figure 13. SMII Receive Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
RX*mn* setup to SMIIREFCLK*n* ↑	t_S	1.5			ns
RX*mn* hold from SMIIREFCLK*n* ↑	t_H	1			ns

m = 0 to 7, *n* = A, B

Figure 14. GMII Transmit Interface Timing Using *Gm*TXCLKI

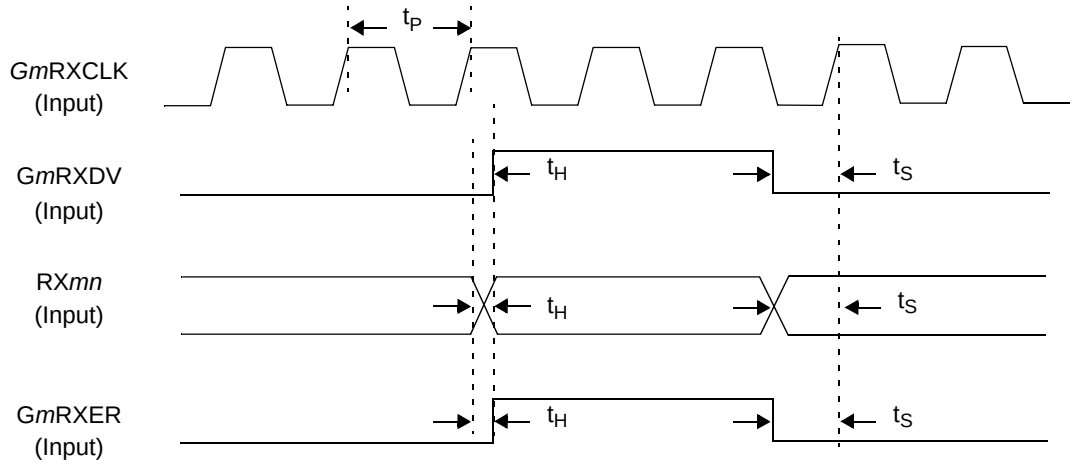


Note: 10 pF load on GMII outputs

Parameter	Symbol	Min	Typ	Max	Unit
G*m*TXCLKI duty cycle		45		55	%
G*m*TXCLKI $_{PERIOD}$	t_{P1}	7.5		8.5	ns
G*m*TXCLKO duty cycle		45		55	%
G*m*TXCLKO period	t_{P2}	7.5		8.5	ns
G*m*TXCLKO↑ (low to high transition time, 10% to 90%)				1	ns
G*m*TXEN, TX*mn*, G*m*TXER delay from G*m*TXCLKO ↑	t_D	0.5		4.5	ns

m = 0 to 7, n = A, B

Figure 15. GMII/MII Receive Interface Timing Using *Gm*RXCLK

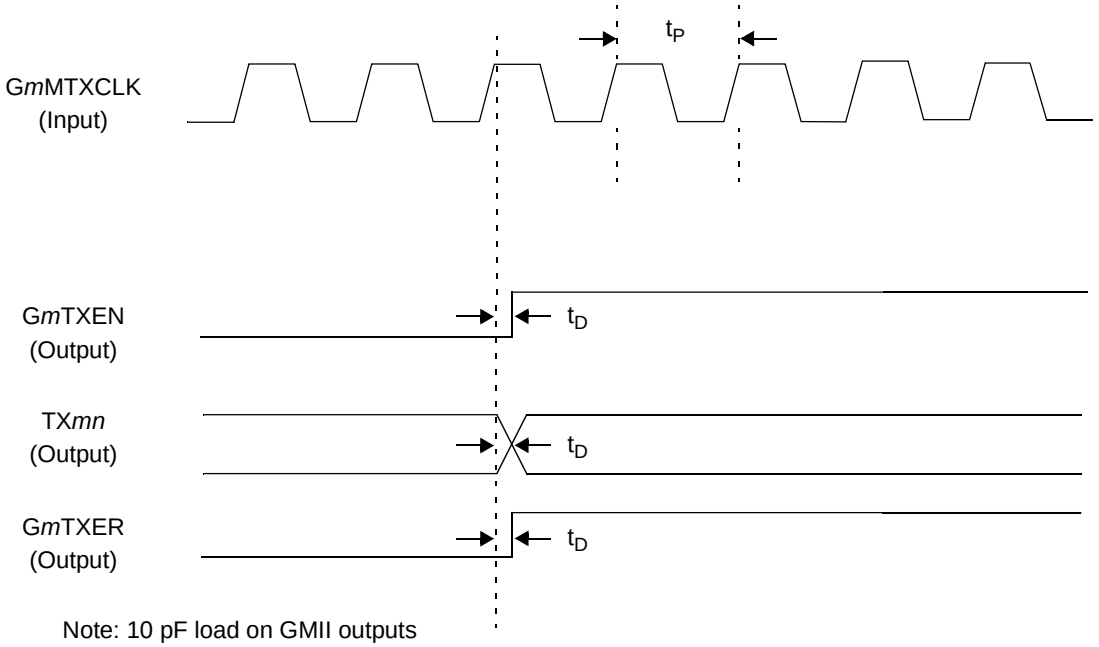


Parameter	Symbol	Min	Typ	Max	Unit
G*m*RXCLK duty cycle		45		55	%
G*m*RXCLK period	t_P	7.5		8.5	ns
G*m*RXDV, RX*mn*, G*m*RXER hold from G*m*RXCLK ↑	t_H	0.5			ns
G*m*RXDV, RX*mn*, G*m*RXER setup to G*m*RXCLK ↑	t_S	2.5			ns

m = 0 to 7, n = A, B

Note: The GMII and MII **Receive** Interface Timing diagrams are specified together in Figure 15, since they are the same. The GMII and MII **Transmit** Interface Timing diagrams are specified separately in Figure 14 and Figure 16, since they are different.

Figure 16. MII Transmit Interface Timing Using *Gm*MTXCLK



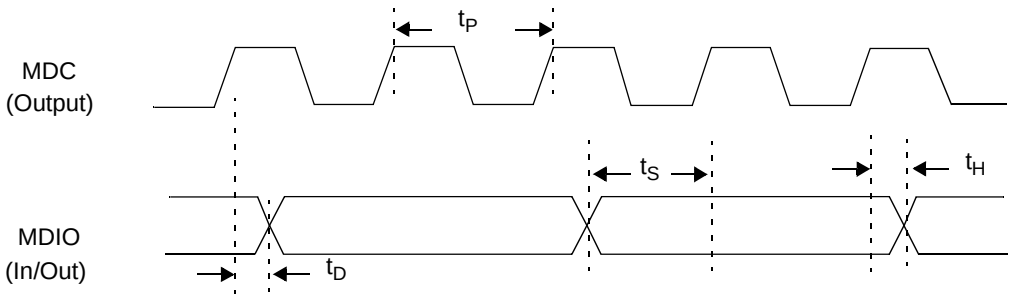
Note: 10 pF load on GMII outputs

Parameter	Symbol	Min	Typ	Max	Unit
G*m*MTXCLK duty cycle		45		55	%
G*m*MTXCLK $_{PERIOD}$	t_P	39	40	41	ns
G*m*MTXCLK ↑ (low to high transition time, 10% to 90%)				1	ns
G*m*TXEN, TX*mn*, G*m*TXER delay from G*m*MTXCLK ↑	t_D	0.5		25	ns

m = 0 to 3, n = A, B

Note: The GMII and MII **Receive** Interface Timing diagrams are specified together in Figure 15, since they are the same. The GMII and MII **Transmit** Interface Timing diagrams are specified separately in Figure 14 and Figure 16, since they are different.

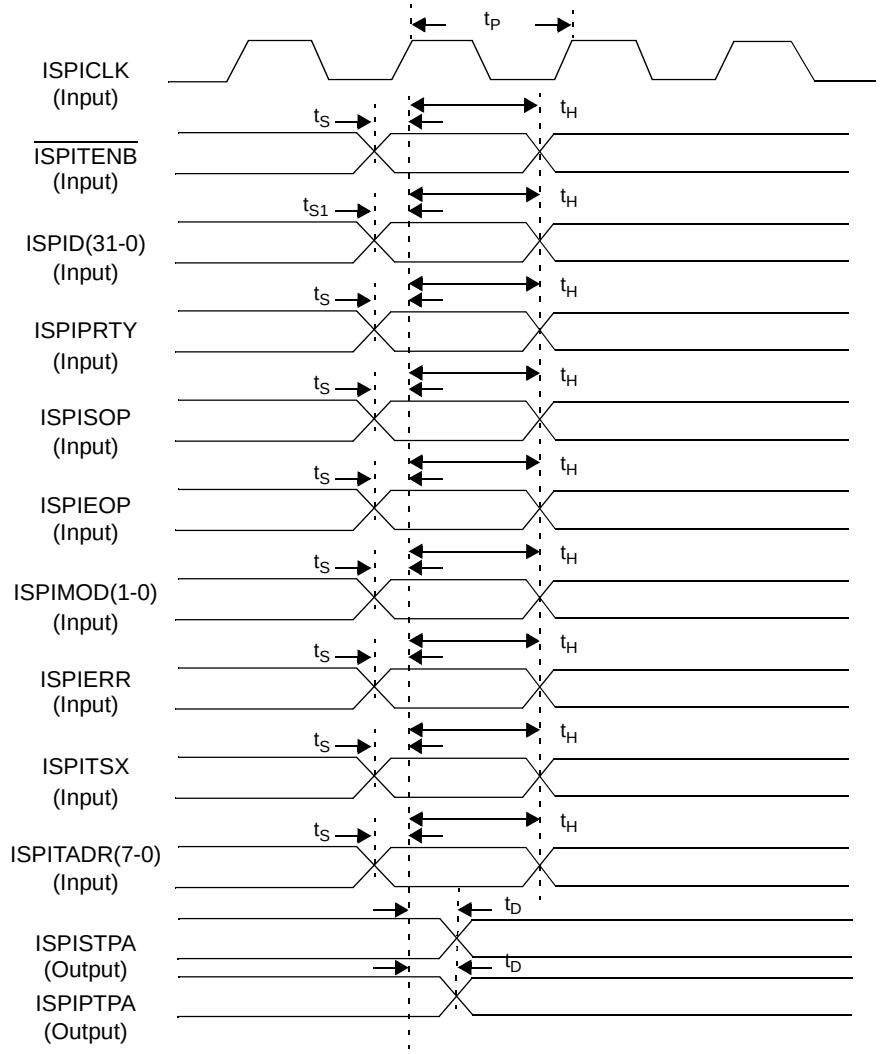
Figure 17. Management MII Interface Timing



Note: 10 pF load on all MII outputs

Parameter	Symbol	Min	Typ	Max	Unit
MDC frequency	$1/t_P$	1.2		15	MHz
MDC duty cycle		45		55	%
MDIO delay from MDC ↑	t_D	10		100	ns
MDIO setup to MDC ↑	t_S	20			ns
MDIO hold from MDC ↑	t_H	0			ns

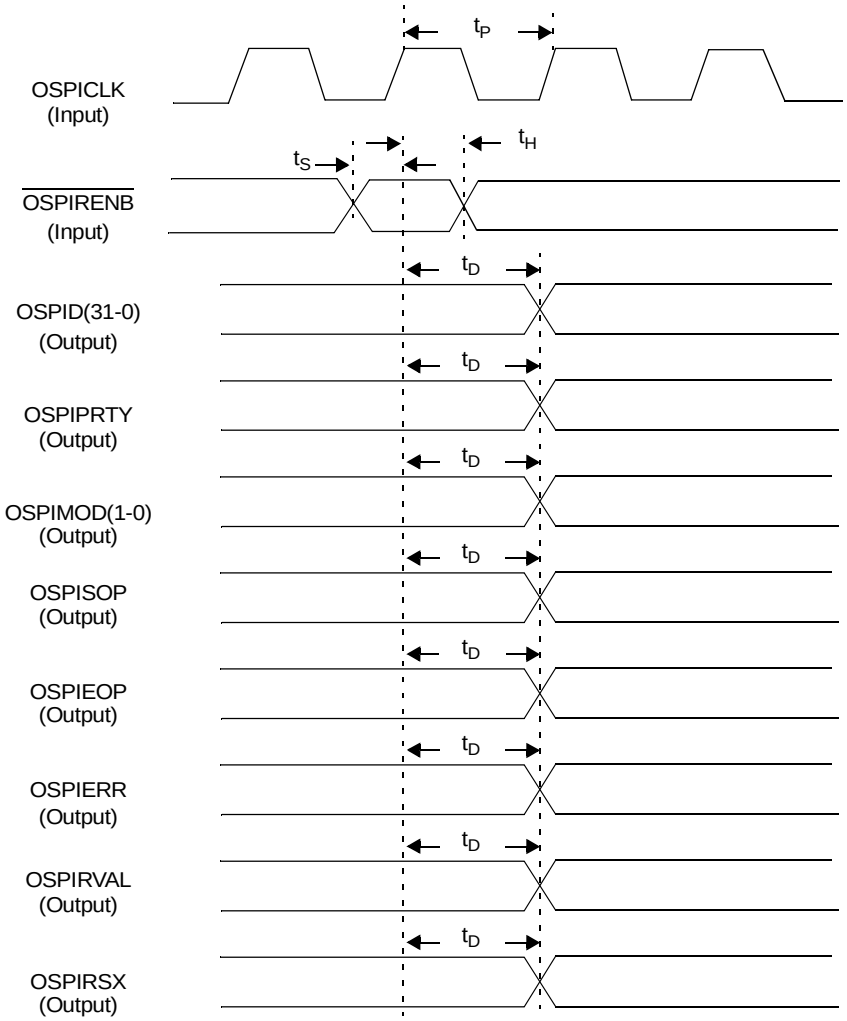
Figure 18. SPI-3 Data Input Interface Timing



Note: 10 pF load on SPI-3 interface outputs.
Please refer to OIF SPI-3 specification for protocol waveform.

Parameter	Symbol	Min	Typ	Max	Unit
ISPICLK frequency	$1/t_P$	25		125	MHz
ISPICLK duty cycle		45		55	%
$\overline{\text{TSPITENB}}$, PRTY, SOP, EOP, MOD(1-0), ERR, TSX, ADR(7-0) setup to ISPICLK ↑	t_S	2.0			ns
ISPID(31-0) setup to ISPICLK ↑	t_{S1}	2.0			ns
$\overline{\text{TSPITENB}}$, ISPID(31-0), PRTY, SOP, EOP, MOD(1-0), ERR, TSX, ADR(7-0) hold from ISPICLK ↑	t_H	0.5			ns
STPA, PTPA(7-0) delay from ISPICLK ↑	t_D	0.8		5	ns

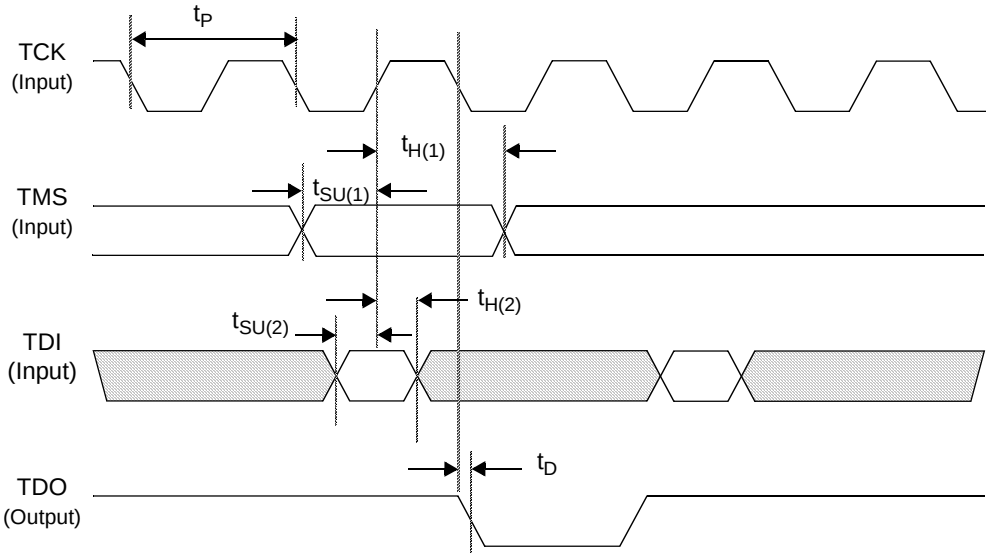
Figure 19. SPI-3 Data Output Interface Timing



Note: 10 pF load on SPI-3 interface outputs.
Please refer to OIF SPI-3 specification for protocol waveform.

Parameter	Symbol	Min	Typ	Max	Unit
OSPICLK frequency	$1/t_P$	25		125	MHz
OSPICLK duty cycle		45		55	%
$\overline{\text{OSPIRENB}}$ setup to OSPICLK ↑	t_S	2.0			ns
$\overline{\text{OSPIRENB}}$ hold from OSPICLK ↑	t_H	0.5			ns
OSPID(31-0), PRTY, MOD(1-0), ERR, SOP, EOP, VAL, RSX delay from OSPICLK ↑	t_D	0.8		5	ns

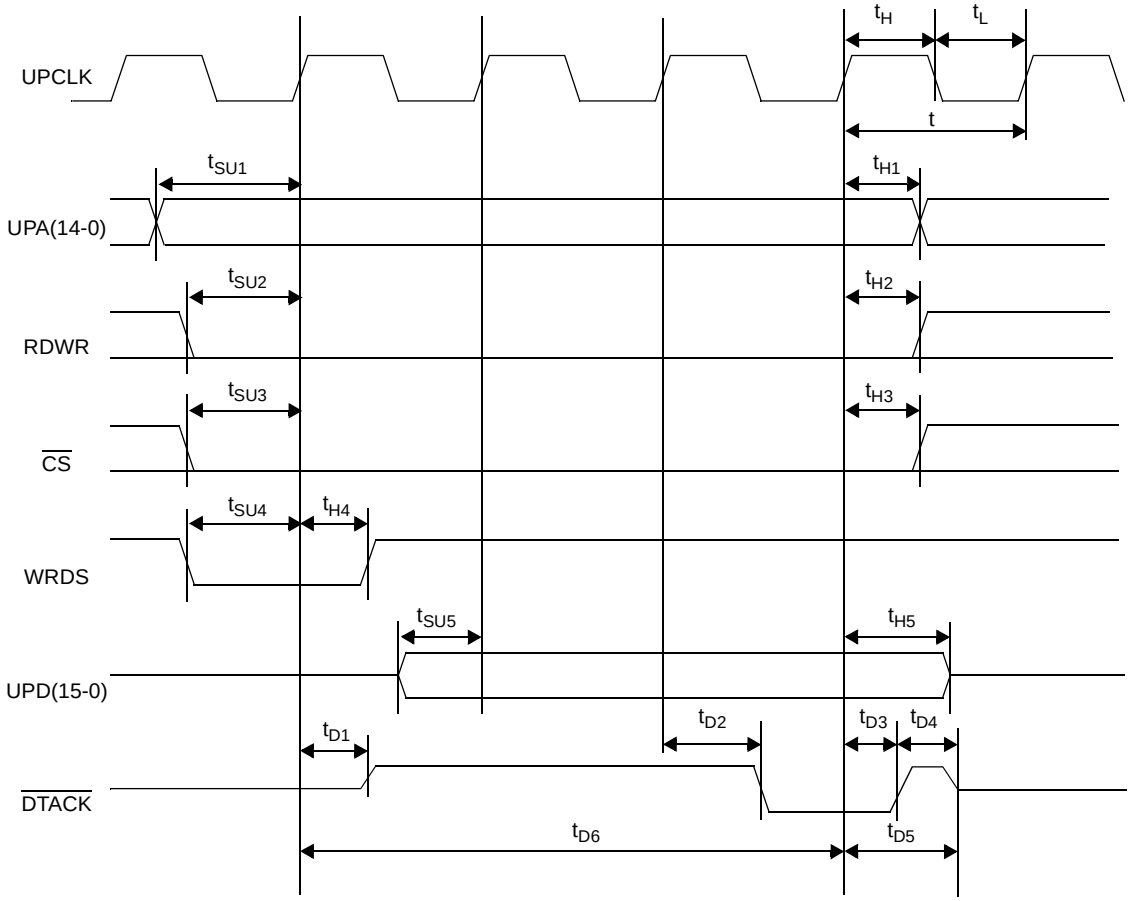
Figure 20. Boundary Scan Timing Diagram



Note: 25 pF Load on All Boundary Scan Interface Outputs

Parameter	Symbol	Min	Typ	Max	Unit
TCK period	t_P	50			ns
TCK clock duty cycle		40		60	%
TMS setup time before TCK ↑	$t_{SU(1)}$	2.0			ns
TMS hold time after TCK ↑	$t_{H(1)}$	3.0			ns
TDI setup time before TCK ↑	$t_{SU(2)}$	1.0			ns
TDI hold time after TCK ↑	$t_{H(2)}$	5.0			ns
TDO delay after TCK ↓	t_D			23.0	ns

Figure 21. Motorola MPC860 Write Cycle Timing

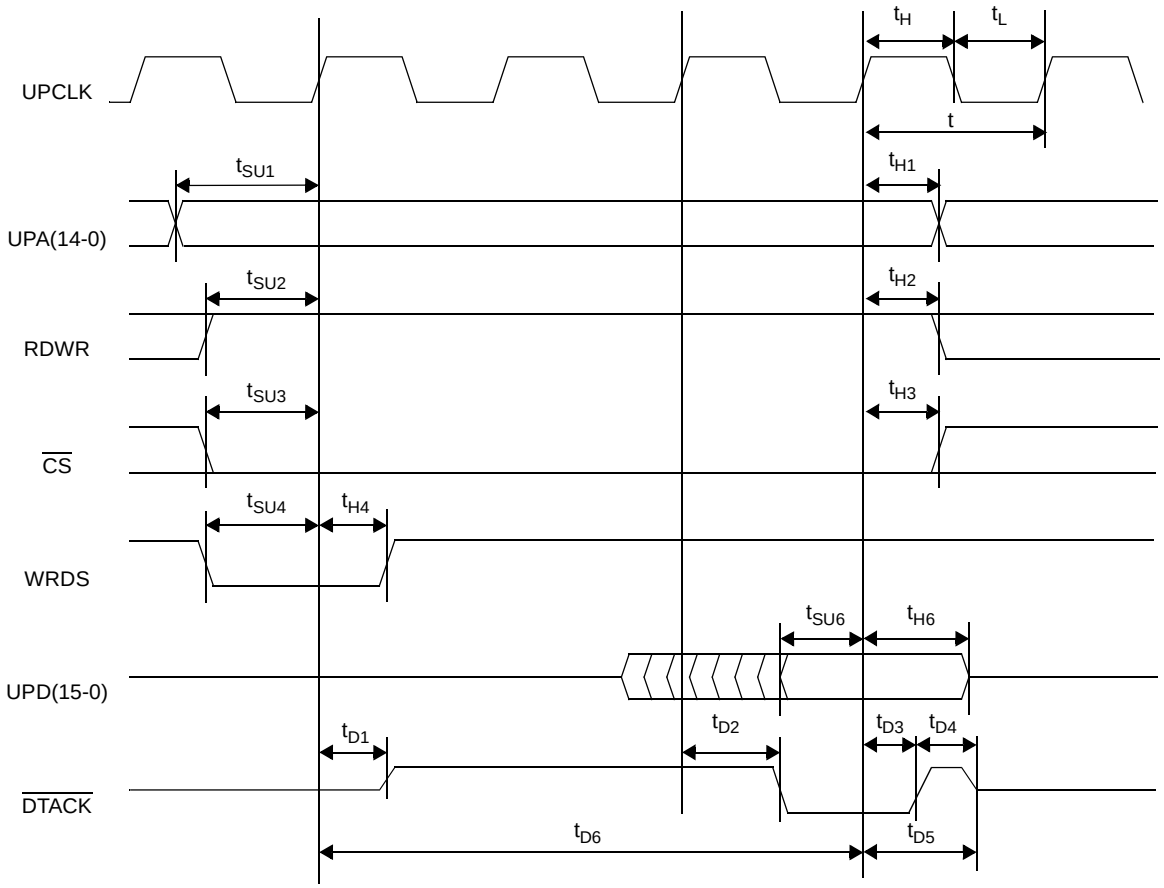


Parameter	Symbol	Min	Typ	Max	Unit
UPCLK clock period	t	15.0		-	ns
UPCLK clock low phase pulse width	t_L	0.4		-	t
UPCLK clock high phase pulse width	t_H	0.4		-	t
Setup time of UPA to rising edge UPCLK	t_{SU1} [a]	4.0		-	ns
Setup time of RDWR to rising edge UPCLK	t_{SU2} [a, b]	4.0		-	ns
Setup time of $\overline{CS}$ to rising edge UPCLK	t_{SU3} [a, c]	3.0		-	ns
Setup time of falling edge WRDS to rising edge UPCLK	t_{SU4}	2.0		-	ns
Setup time of UPD to rising edge UPCLK	t_{SU5} [d]	4.0		-	ns
Hold time of UPA to rising edge UPCLK	t_{H1} [e]	0.0		-	ns

Parameter	Symbol	Min	Typ	Max	Unit
Hold time of RDWR to rising edge UPCLK	t_{H2} [e, f]	0.0		-	ns
Hold time of $\overline{CS}$ to rising edge UPCLK	t_{H3} [e, c]	1.0		-	ns
Hold time of WRDS to rising edge UPCLK	t_{H4}	2.0		-	ns
Hold time of UPD to rising edge UPCLK	t_{H5} [e]	0.0		-	ns
Delay from rising edge UPCLK to $\overline{DTACK}$ driving	t_{D1} [a]	0.0		15.0	ns
Delay from rising edge UPCLK to active edge $\overline{DTACK}$	t_{D2} [g]	3.0		7.0	ns
Delay from rising edge UPCLK to inactive edge $\overline{DTACK}$	t_{D3} [e]	3.0		7.0	ns
Delay from $\overline{DTACK}$ going inactive to $\overline{DTACK}$ going in tristate	t_{D4}	4.0		-	ns
Delay from rising edge UPCLK to $\overline{DTACK}$ going in tristate	t_{D5} [e]	-		15.0	ns
Maximum response latency	t_{D6}	6		22	Cycles

a. Timing is relative to the rising edge of UPCLK during which WRDS is asserted.
b. Only applies if a write access is preceded by a read access. RDWR may stay low between 2 successive write accesses to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.
d. Timing is relative to next rising edge after the one during which WRDS is asserted.
e. Timing is relative to the rising edge of UPCLK during which $\overline{DTACK}$ is asserted.
f. Only applies if a write access is followed by a read access. RDWR may stay low between 2 successive write accesses to the same peripheral.
g. Timing is relative to the rising edge before the one during which $\overline{DTACK}$ is asserted.

Figure 22. Motorola MPC860 Read Cycle Timing

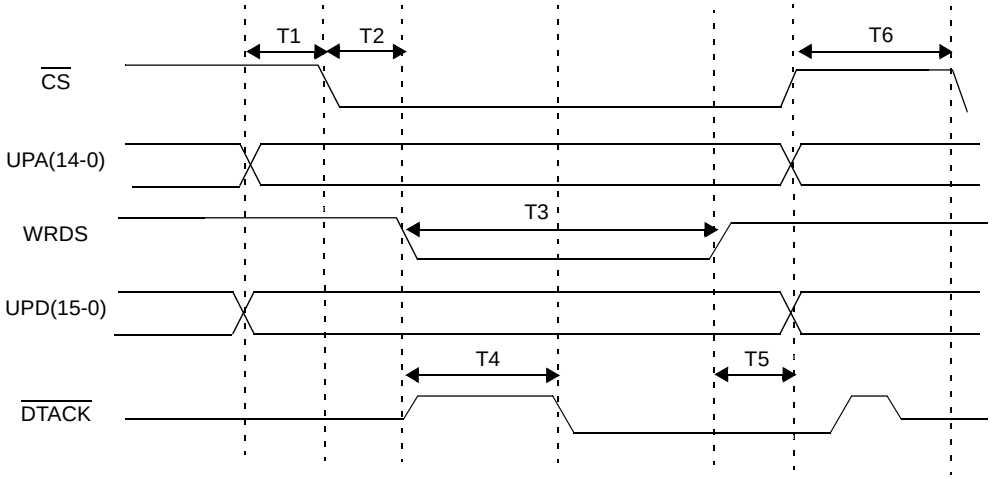


Parameter	Symbol	Min	Typ	Max	Unit
UPCLK clock period	t	15.0		-	ns
UPCLK clock low phase pulse width	t_L	0.4		-	t
UPCLK clock high phase pulse width	t_H	0.4		-	t
Setup time of UPA to rising edge UPCLK	t_{SU1} [a]	4.0		-	ns
Setup time of RDWR to rising edge UPCLK	t_{SU2} [a, b]	4.0		-	ns
Setup time of $\overline{CS}$ to rising edge UPCLK	t_{SU3} [a, c]	3.0		-	ns
Setup time of falling edge WRDS to rising edge UPCLK	t_{SU4}	2.0		-	ns
Hold time of UPA to rising edge UPCLK	t_{H1} [d]	0.0		-	ns
Hold time of RDWR to rising edge UPCLK	t_{H2} [d, e]	0.0		-	ns

Parameter	Symbol	Min	Typ	Max	Unit
Hold time of $\overline{CS}$ to rising edge UPCLK	t_{H3} [c, d]	1.0		-	ns
Hold time of WRDS to rising edge UPCLK	t_{H4}	2.0		-	ns
Delay from rising edge UPCLK to $\overline{DTACK}$ driving	t_{D1} [a]	0.0		20.0	ns
Delay from rising edge UPCLK to active edge $\overline{DTACK}$	t_{D2} [f]	3.0		7.0	ns
Delay from rising edge UPCLK to inactive edge $\overline{DTACK}$	t_{D3} [d]	3.0		7.0	ns
Delay from $\overline{DTACK}$ going inactive to $\overline{DTACK}$ going in tristate	t_{D4}	4.0		-	ns
Delay from rising edge UPCLK to $\overline{DTACK}$ going in tristate	t_{D5} [d]	-		15.0	ns
Maximum response latency	t_{D6}	6		22	Cycles
Setup time of UPD to rising edge UPCLK	t_{SU6} [d]	15.0		-	ns
Hold time of UPD going in tristate to rising edge UPCLK	t_{H6} [d]	3.0		12.0	ns

a. Timing is relative to the rising edge of UPCLK during which WRDS is asserted.
b. Only applies if a read access is preceded by a write access. RDWR may stay high between 2 successive read accesses to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.
d. Timing is relative to the rising edge of UPCLK during which $\overline{DTACK}$ is asserted.
e. Only applies if a read access is followed by a write access. RDWR may stay high between 2 successive read accesses to the same peripheral.
f. Timing is relative to the rising edge before the one during which $\overline{DTACK}$ is asserted.

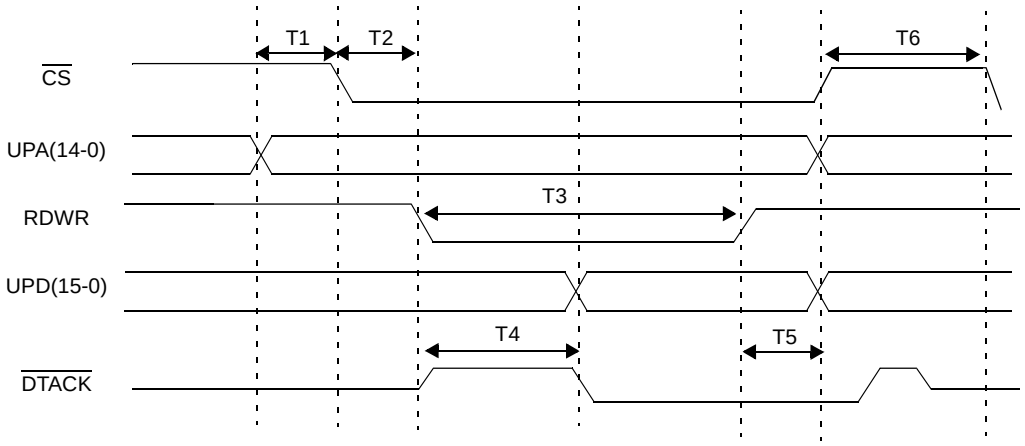
Figure 23. Asynchronous Microprocessor Interface: Intel Write Cycle Timing



Parameter	Symbol	Min in UPCLK Cycles	Max in UPCLK Cycles
Address setup to $\overline{CS}$ driven low	T1	0	
$\overline{CS}$ prior to WRDS (Write strobe) low	T2	0	1
Assertion time for WRDS (Write Strobe)	T3	6	
Write completion to $\overline{DTACK}$ going low	T4	0	22
UPD, UPA, $\overline{CS}$ hold time to $\overline{DTACK}$ going low	T5	0	
$\overline{CS}$ inactive hold time after write completion (for back to back writes or reads)	T6	2	

Note: The microprocessor clock must be present for correct operation.

Figure 24. Asynchronous Microprocessor Interface: Intel Read Cycle Timing



Parameter	Symbol	Min in UPCLK Cycles	Max in UPCLK Cycles
Address setup to $\overline{CS}$ driven low	T1	0	
$\overline{CS}$ prior to RDWR (Read strobe) low	T2	0	
Assertion time for RDWR (Read Strobe)	T3	6	
Read completion to $\overline{DTACK}$ going low	T4	0	22
UPD, UPA, $\overline{CS}$ hold time to $\overline{DTACK}$ going low	T5	0	
$\overline{CS}$ inactive hold time after read completion (for back to back reads or writes)	T6	2	

Note: The microprocessor clock must be present for correct operation.

6.0 OPERATION

6.1 SMII/GMII TO SPI-3 FLOW FUNCTIONAL OPERATION

6.1.1 Receive MAC Data Flow

Ethernet frames arriving at the SMII/GMII interface are qualified by an IEEE 802.3 compliant Media Access Controller (MAC) function. Each SMII/GMII interface or each channel is processed by the MAC. The MAC operates in Full-Duplex or Half-Duplex mode and processes both standard and VLAN tagged Ethernet frames. The MAC supports Control frames in addition to PAUSE control frames per the IEEE 802.3 standard (Generation and Termination). The SMII/GMII interface presents receive frames to the MAC receive block and the MAC removes the PREAMBLE and the SFD (Start of Frame Delimiter) and writes the frames into the appropriate Ingress FIFO.

6.1.2 Receive MAC Checks

Following are the checks performed by the MAC if enabled, for each port on the incoming Ethernet frame.

6.1.2.1 FCS Check:

The Frame Check Sequence (FCS) is checked for its correctness. The FCS of the received frame is checked against the FCS calculated by the MAC over the Data, address, and length/ type fields. Frames failing the FCS check are optionally discarded based on a programmable bit in the configuration register. This configuration bit is the FCS check failed discard bit.

When the IFIFO is configured for Store and Forward mode, the frame is discarded and will not show up on the SPI port. When the IFIFO is configured for Streaming mode, a bad FCS is appended to the frame.

6.1.2.2 Frame Length Check:

The length field of the received Ethernet frame is checked for correctness. The length of the Data field in the Ethernet frame is checked against the frame length field. The Frame length check enable bit is programmable (Register 0x4004 Bit 4). Frames failing the frame length check will be optionally discarded or errored if the frame length check discard configuration bit is set (Register 0x4084 Bit 25).

When the IFIFO is configured for Store and Forward mode, the frame is discarded and will not show up on the SPI port. When the IFIFO is configured for Streaming mode, a bad FCS is appended to the frame.

6.1.2.3 Maximum Frame Size Check:

The maximum size of the accepted Ethernet frame is programmable. The default value is 1536 (decimal) bytes. Frames exceeding the programmed maximum frame size are

truncated. Truncated frames are optionally discarded or errored if the Discard Truncated Frame configuration bit is set (Register 0x4084 Bit 24). The maximum frame size check is disabled by setting the Huge Frame Enable configuration bit (Register 0x4004 Bit 5).

When the IFIFO is configured for Store and Forward mode, the frame is discarded and will not show up on the SPI port. When the IFIFO is configured for Streaming mode, a bad FCS is appended to the frame.

6.1.2.4 Interframe Gap Check:

The Interframe Gap (IFG) is programmable. A received Ethernet frame violating the programmed Interframe gap value is dropped or errored. The default value of the Minimum IFG is 80 (decimal) bits.

When the IFIFO is configured for Store and Forward mode, the frame is discarded and will not show up on the SPI port. When the IFIFO is configured for Streaming mode, a bad FCS is appended to the frame.

6.1.2.5 Destination Address Check:

The Destination address of the received Ethernet frame is compared to the programmed Source address of the device. If the destination address of the frame does not match the programmed source address, the frame will be optionally filtered out based on the Destination Address match discard configuration bit (Register 0x4084 Bit 29).

When the IFIFO is configured for Store and Forward mode, the frame is discarded and will not show up on the SPI port. When the IFIFO is configured for Streaming mode, a bad FCS is appended to the frame.

Note: When an incoming frame (from the Ethernet side) fails all the checks above (except for FCS) and the corresponding configuration bits to discard the frame are NOT SET, the frame will be output on the SPI-3 Receive Interface. The only requirement on the incoming frame for the above to occur, is that the incoming frame has a valid preamble, SFD, and FCS.

6.1.3 Receive MAC Statistics

The Receive MAC provides statistics and performance monitoring, to facilitate remote network monitoring (RMON) per Groups 1, 2, 3, and 9, in addition to supplementary statistics.

6.1.3.1 Counters:

The MAC records the following statistics using counters that are programmable as either clear on read saturating counters or rollover counters (Register 0x0030 Bit 0).

- Total number of bytes received. This counter can be programmed to exclude byte counts from errored frames (40 bit)
- Total number of frames received. This includes errored frames (32 bit)
- Count of Multicast frames received (32 bit)
- Count of Broadcast frames received (32 bit)
- Count of PAUSE Control frames received (32 bit)
- Count of Control frames received with unknown opcode (32 bit)
- Count of frames received with a valid FCS and length less than 64 bytes (32 bit)
- Count of frames received with a valid FCS and total byte count is between 1519 and

maximum frame length (32 bit)

- Count of frames received with an invalid FCS and length less than 64 bytes (32 bit)
- Count of frames received with an invalid FCS and total byte count is between 64 and 1518 bytes (32 bit)
- Count of frames received with an invalid FCS and total byte count is between 1519 and maximum frame length (32 bit)
- Count of frames dropped by the receive MAC due to Ingress FIFO full (32 bit)
- Count of frames dropped by the receive MAC due to Unicast and Source address mismatch (32 bit)
- Count of VLAN tagged frames received (32 bit)
- Six sets of counts for frame sizes that fall in a certain range. The ranges are 64 bytes, 65 to 127 bytes, 128 to 255 bytes, 256 to 511 bytes, 512 to 1023 bytes, and 1024 to 1518 bytes.
- Count of frames received with the RX_ER asserted by the PHY during transmission (32 bit)
- Count of frames received with length error (32 bit)

6.1.4 Ingress FIFO Operations

6.1.4.1 Ingress FIFO Write:

Frames once qualified by the Receive MAC are written into the Ingress FIFO of the appropriate channel. The Ingress FIFO for each channel is 7.75 KBytes deep in SMII mode, 62 KBytes deep in GMII mode, and 31 KBytes deep in extended SMII mode. The ingress FIFO is an integral part of Envoy-CE2 IEEE 802.3 compliant Flow control mechanism, which is used to backpressure the Ethernet interface. When the Ingress FIFO starts becoming full, the flow control is activated (if enabled) and the device transmitting the Ethernet traffic is backpressured. A complete description of the procedure is outlined in section “Ethernet Full Duplex” on page 71. If the Ethernet device transmitting frames, ignores the backpressure indication and attempts to overflow the Ingress FIFO, the Envoy-CE2 will truncate the frame being received during the overflow condition. Frames received when the Ingress FIFO is in an overflow condition are discarded and the number of discarded frames are counted. In Half Duplex mode, the backpressure mechanism used is the “Raise Carrier” method, which is described in section Ethernet “Half-Duplex Flow Control” on page 71.

6.1.4.2 Ingress FIFO Read:

Frames are read out from the Ingress FIFO by the SPI-3 interface. Since the SPI-3 interface aggregates the traffic from the channels, a channel selection is required. The selection of the Ingress FIFO (or channel selection) for frame reads, is done by the SPI-3 interface. For SPI-3, the selection is done by the scheduler in the Envoy-CE2 SPI-3 interface block. The scheduler uses a round robin selection scheme.

6.1.4.3 Ingress FIFO Frame Availability for Transfer (Store and Forward/Streaming):

Frame data stored in the Ingress FIFO will be made available for transfer on the SPI-3 interface, depending on two selectable modes of operation:

- **Store and Forward Mode:** When a complete frame has been written into the Ingress

FIFO, the frame is available for transfer. The SPI-3 interface may be configured for burst (chunk) or packet transfer mode, when the FIFO is configured for store and forward.

- **Streaming Mode:** When a selectable fixed number of bytes have been written into the Ingress FIFO, a chunk is available for transfer. The selection for streaming range from 1 to 255, in units of 8 byte words and is equal to the SPI-3 burst (chunk) size, defined for the SPI-3 output. Hence, in streaming mode, the SPI-3 interface needs to be in burst (chunk) transfer mode. When streaming is enabled and an end of frame is written into the Ingress FIFO, before the selected number of (streaming) bytes have been received, the frame data will be available for transfer across the SPI-3 interface based on the end of frame condition. When streaming is enabled, frame errors at the SMII/GMII interface are indicated on the SPI-3 interface during the transfer of the frame.

6.1.5 SPI-3 Output Operations

6.1.5.1 Data Flow Operations:

Frames from the Ingress FIFO are read out by the Output SPI-3 interface. The interface is programmable in either PHY or Link layer mode. The OIF System Packet Interface Level 3 (SPI-3) specification describes the interface in detail. When the SPI-3 output interface is configured in PHY layer mode, the Link layer device performs flow control by controlling the Read Enable. When the SPI-3 output interface is configured in Link layer mode, the PHY layer device provides backpressure information via the Transmit Packet Available pins and the device provides flow control using the Transmit Enable pins. The channel selection in both PHY and Link layer modes is done by the Envoy-CE2. Once a channel has data available for transfer based on store and forward or streaming mode, the scheduler in the SPI-3 interface block selects the channel for frame transfer. The Envoy-CE2 provides the burst mode option to restrict a channel from transmitting more than a fixed number of bytes once selected. Once a burst of data bytes has been transmitted by the selected channel, a new channel is selected for frame transfer. This prevents a channel from using up all the bandwidth on the SPI-3 interface, by giving the other channels access to the SPI-3 interface. The allowable burst sizes are 1 to 255 in units of 8 byte words. Alternatively, in packet transfer mode, a complete frame is transferred across the SPI-3 interface.

6.1.5.2 SPI-3 Output Interface Frame Format:

Data at the SPI-3 output interface is an Ethernet frame (VLAN frames also), excluding the preamble and start of frame delimiter. The FCS may be programmed to be excluded.

Note: The following figures show the inclusion of the FCS.

Standard Ethernet Frame at SMII/GMII interface

Preamble (7 bytes)	Start of Frame Delimiter (1 byte)	Destination Address (6 bytes)	Source Address (6 bytes)	Length/Type (2 bytes)	Data (46 to 1500 bytes)	Frame Check Sequence (4 bytes)

Frame format at SPI-3 Output Interface

Destination Address (6 bytes)	Source Address (6 bytes)	Length/Type (2 bytes)	Data (46 to 1500 bytes)	Frame Check Sequence (4 bytes)

VLAN Tag Frame format at SPI-3 Output Interface

Destination Address (6 bytes)	Source Address (6 bytes)	VLAN Tag (4 bytes)	Length/Type (2 bytes)	Data (46 to 1500 bytes)	Frame Check Sequence (4 bytes)

Frame with Extension Field at SPI-3 Output Interface

Destination Address (6 bytes)	Source Address (6 bytes)	Length/Type (2 bytes)	Data (46 to 1500 bytes)	Frame Check Sequence (4 bytes)	Extension

6.2 SPI-3 TO SMII/GMII FLOW FUNCTIONAL OPERATION

6.2.1 SPI-3 Input Operation

6.2.1.1 Input SPI-3 Data Flow:

At the SPI-3 input interface, frames are transferred from the Link or PHY layer device to the Envoy-CE2. An Envoy-CE2 channel is selected for data transfer, by the Link or PHY layer device. In PHY layer mode, the Link layer device monitors the “Buffer Space Available” signals, STPA/PTPA and selects an Envoy-CE2 channel for data transfer, based on the Transmit packet available signals (STPA and PTPA). In Link layer mode, the PHY layer device transfers frame based on Envoy-CE2’s read enable signal. Once a data transfer begins, the Link/PHY layer device qualifies the frame data being transferred into the channel’s Egress FIFO, with the read enable/data valid signal. The “Buffer Space Available” signals reflect the full status of the channel’s Egress FIFO and get de-asserted when the associated Egress FIFO becomes near full (near full level is programmable). When the Egress FIFO is configured for Store and Forward mode, frames received with the SPI-3 error pin asserted, will be either discarded or errored and a count of the discarded and errored frames is kept.

When the egress FIFO is configured for Store and Forward mode, frames received with the SPI-3 error pin asserted are discarded and will not show up on the Ethernet port. When the egress FIFO is configured for Streaming mode, frames received with the SPI-3 error pin asserted will show up on the Ethernet port with an additional four bytes of bad CRC appended to it.

6.2.1.2 Oversubscription Mode

The SPI-3 Input interface is designed to support an Oversubscription mode. In this mode, the far end SPI-3 Slave or Master device can ignore the backpressure exerted by the Envoy-CE2 SPI-3 Master or Slave. Since the backpressure is being ignored, it is possible that the per-PHY Egress FIFOs can be filled to overflow. When a PHY’s Egress FIFO is filled, data from the Input SPI-3 data bus will still be clocked into the Envoy-CE2, but it will not be written into the PHY’s Egress FIFO. This allows the SPI-3 bus to still run and service the PHYs whose buffers are not full.

Regardless of the Egress FIFO configuration for Store and Forward mode or Streaming mode, all complete packets received on the SPI-3 port for a full PHY will be discarded and

counted. The only difference between Store and Forward mode and Streaming mode when Oversubscription is being used is in the treatment of the packet that overflows the Egress FIFO. In Store and Forward mode, the overflowing packet will be discarded and counted. In Streaming mode, the overflowing packet will be flagged as errored into the Egress FIFO and it will be errored on the way out of the Transmit MAC.

In PHY Layer mode, Oversubscription is always enabled. STPA/PTPA status is always presented accurately on the external SPI-3 port.

In Link Layer mode, Oversubscription can be enabled or disabled through the Oversubscription Enable bit (Register 0x002C Bit 4). If the Oversubscription enable bit is set to '1', the SPI-3 Master will never raise its ISPIRENB output. Setting this bit shuts off all Rx backpressure reporting from the Envoy-CE2. If the Oversubscription enable bit is set to '0', the SPI-3 Master uses the ISPIRENB output pin to exert standard SPI-3 backpressure.

6.2.1.3 Input SPI-3 Interface Frame Format:

The Data format accepted by Envoy-CE2, at the SPI-3 Input interface, is an Ethernet frame (VLAN frames also), excluding the preamble and the Start of frame delimiter. If the Transmit MAC is configured to generate the Frame Check Sequence (FCS), then the FCS is optional for the frame received by the Envoy-CE2 at the SPI-3 interface. If the Transmit MAC is not configured to generate the FCS, then the FCS needs to be included in the frame.

Standard Ethernet Frame at SMII/GMII Transmit interface

Preamble (7 bytes)	Start of Frame Delimiter (1 byte)	Destination Address (6 bytes)	Source Address (6 bytes)	Length/ Type (2 bytes)	Data (46 to 1500 bytes)	Frame Check Sequence (4 bytes)

Frame format at the SPI-3 Input Interface with Frame Check Sequence

Destination Address (6 bytes)	Source Address (6 bytes)	Length/Type (2 bytes)	Data (46 to 1500 bytes)	Frame Check Sequence (4 bytes)

Frame format at the SPI-3 Input Interface without Frame Check Sequence

Destination Address (6 bytes)	Source Address (6 bytes)	Length/Type (2 bytes)	Data (46 to 1500 bytes)

VLAN Tagged and Extended frames may have the FCS included depending whether Envoy-CE2 is configured to generate FCS or not.

6.2.2 Egress FIFO Operations

6.2.2.1 Egress FIFO Write:

Each Egress FIFO is 3.2 KBytes deep in SMII mode, 32 KBytes deep in GMII mode, and 12.4 KBytes deep in extended SMII mode. The Link or PHY layer device (depending on the mode the Envoy-CE2 is in) is responsible for selecting the channel into which the frame data is written. The Egress FIFO backpressures the SPI-3 input interface when the FIFO becomes near full. The near full indication level is programmable as number of bytes from the FIFO full. If the Link or PHY layer device attempts to overflow the Egress FIFO when it is configured in Store and Forward mode, the complete frames being received are discarded and a count of the discarded frames are provided per channel. If the Link or PHY layer device attempts to overflow the Egress FIFO when it is configured in Streaming mode, the current frame being received is truncated and will be sent out the targeted Ethernet port as an errored frames. All subsequently arriving frames are discarded until some room is freed up in the Egress FIFO and a count of the discarded frames are provided per channel.

Note: The discard frame count is used to count frames discarded due to an Egress FIFO overflow condition and the SPI-3 Error pin assertion condition.

6.2.2.2 Egress FIFO Frame Availability for Transfer (Store and Forward/Streaming):

Frame data stored in the Egress FIFO will be made available for transfer on the Ethernet Transmit interface, depending on two selectable modes of operation:

- **Store and Forward Mode:** When a complete frame has been written into the Egress FIFO, the frame is available for transfer to the Ethernet transmit interface (SMII/GMII).
- **Streaming Mode:** When a selectable fixed number of bytes have been written into the Egress FIFO, a frame is available for transfer. The selections for streaming are 64, 128, 256, 512, 768, or 1544 bytes. When streaming is enabled and an end of frame is written into the Egress FIFO, before the selected number of (streaming) bytes have been received, the frame data will be available for transfer across the Ethernet transmit interface (SMII/GMII) based on the end of frame condition. When streaming is enabled, frame errors at the SPI-3 interface are indicated on the SMII/GMII interface during the transfer of the frame.

6.2.2.3 Egress FIFO Read:

Frame data from the Egress FIFO is read out by the Transmit MAC block. Each channel has an SMII/GMII Transmit block and interfaces to the appropriate Egress FIFO. When a complete frame or a programmed number of bytes have been written into the Egress FIFO, then it is available for transmission on the Ethernet Network via the SMII/GMII Transmit interface.

The Egress FIFO forms an integral part in the implementation of the IEEE 802.3 compliant Ethernet flow control mechanism in the Envoy-CE2, using PAUSE Control frames. When a PAUSE Control frame destined for the Envoy-CE2 reaches the SMII/GMII receive interface, the action taken by the Full-Duplex flow control block is to stop Egress FIFO reads. This may result in the Egress FIFO becoming full. As mentioned above, the SPI-3 interface is backpressured when the Egress FIFO becomes full. A complete explanation of the Full-Duplex Ethernet flow control mechanism is outlined in section "Ethernet Full Duplex" on page 71.

6.2.3 Transmit MAC Data Flow

The MAC can be configured to operate in either Full-Duplex mode or Half Duplex mode (Fast Ethernet only). The MAC transmits both standard Ethernet frames and VLAN tagged Ethernet frames. The MAC supports Control frames in addition to PAUSE control frames per the IEEE 802.3 standard (Generation and Termination). The Egress FIFO indicates availability of a Frame to the Transmit MAC when a complete frame is stored in the Egress FIFO. The Transmit MAC reads the Egress FIFO and transmits the frame over the SMII/GMII transmit interface.

6.2.4 Transmit MAC Configurable Options and Checks

Following are the configurable options and checks for the MAC for the outgoing Ethernet frame.

6.2.4.1 Frame Check Sequence (FCS) Generation Option:

The MAC provides the option to append the correct FCS when Ethernet frames presented to the Envoy-CE2 at the SPI-3 Input interface, do not contain a valid FCS. Please note that this option also works in conjunction with the pad option.

6.2.4.2 Pad Short Ethernet Frames Option:

The MAC can be configured to pad short frames to 64 bytes and append the correct FCS. If this option is set, the FCS generation option is ignored. The pad option is for Ethernet frames presented at the SPI-3 Input interface with lengths less than 64 bytes.

6.2.4.3 Frame Length Check:

The length field of the received Ethernet frame is checked against the actual data length for correctness. The Frame length check enable bit is programmable (Register 0x4004 Bit 4).

6.2.4.4 Maximum Frame Size Check:

The maximum size of the accepted Ethernet frame is programmable. The default value is 1536 (decimal) bytes. Frames exceeding the programmed maximum frame size are truncated. Truncated frames are tagged with RX_ER. The maximum frame size check is disabled by setting the Huge Frame Enable configuration bit (Register 0x4004 Bit 5).

6.2.4.5 Back to Back Interframe Gap Option:

The Interframe Gap (IFG) between two back to back transmitted Ethernet frames is programmable. The default value of the Minimum IFG is 96 bits (decimal).

6.2.4.6 Source Address Replace Option:

The MAC provides the option to replace the source address (SA field) of the Ethernet frame received at the SPI-3 Input interface with the programmed source address (Register 0x4084 Bit 21). The Envoy-CE2 has programmable per port source address registers.

6.2.4.7 PAUSE Frame Filter Option:

The MAC provides the option to filter PAUSE frames received at the SPI-3 Input Interface. The option is provided to filter PAUSE frames with the specified Multicast address (01-80-C2-00-00-01) or to filter all PAUSE frames from the SPI-3 interface destined for the Ethernet Transmit interface (Register 0x4084 Bit 28). These frames will be errored by forcing the MAC to append an incorrect CRC.

6.2.4.8 Preamble Length Option:

The Preamble length of the transmitted Ethernet frame is programmable by the MAC. The default value is 7 bytes (Register 0x4004 Bits 12-15).

6.2.5 Transmit MAC Statistics

The Transmit MAC provides statistics and performance monitoring, to facilitate remote network monitoring (RMON) per Groups 1, 2, 3, and 9, in addition to supplementary statistics.

6.2.5.1 Counters:

The MAC records the following statistics using counters that are programmable as either clear on read saturating counters or rollover counters (Register 0x0030 Bit 0).

- Total number of bytes transmitted. This counter can be programed to exclude byte counts from errored frames (40 bit)
- Total number of frames transmitted. This includes all frames, broadcast and multicast (32 bit)
- Count of Multicast frames transmitted (32 bit)
- Count of Broadcast frames transmitted (32 bit)
- Count of PAUSE Control frames transmitted (32 bit)
- Count of VLAN tagged frames transmitted (32 bit)
- Count of frames transmitted with a valid FCS and total byte count is between 1519 and maximum frame length (32 bit)
- Count of frames transmitted with a valid FCS and length less than 64 bytes (32 bit)
- Count of deferred frames transmitted (32 bit)
- Count of excessive deferred frames transmitted (32 bit)
- Count of single collision frames (32 bit)
- Count of multiple collision frames (32 bit)
- Count of late collision frames (32 bit)
- Count of excessive collision frames (32 bit)
- Count of frames transmitted with an invalid FCS and length less than 64 bytes (32 bit)
- Count of frames transmitted with an invalid FCS and total byte count is between 1519 and maximum frame length (32 bit)
- Count of frames transmitted with an invalid FCS and total byte count is between 64 and 1518 bytes (32 bit)
- Count of dropped frames due to lack of system resources (32 bit)
- Count of aborted frames under command of the Egress FIFO logic (32 bit)
- Six sets of counts for frame sizes that fall in a certain range. The ranges are 64 bytes, 65 to 127 bytes, 128 to 255 bytes, 256 to 511 bytes, 512 to 1023 bytes, and 1024 to 1518 bytes.
- Count of PAUSE frames originated via SPI-3 interface that are discarded (32 bit)

6.3 PORT AGGREGATION

In Port Aggregation mode, the Envoy-CE2 aggregates all the Ethernet ports' receive data onto a single SPI-3 port. Port Aggregation mode may be programmed in SPI-3 Multi-PHY mode or SPI-3 Single-PHY mode. In Multi-PHY mode, all the Ethernet ports aggregate traffic onto SPI-3 port 0. A round robin mechanism schedules traffic from multiple Ingress FIFOs (per Port Ingress FIFOs) onto a single SPI-3 Port. Port Aggregation in Single-PHY mode is similar to the above except that there is no concept of a SPI-3 port and hence no SPI-3 port address. The Envoy-CE2 emulates a single PHY/Link layer device in Single-PHY operation.

A programmable port number is appended to the packet or chunk (depending on whether the device is in burst mode or not). The programmable port number may be used by the downstream device to identify the source of the packet from the Envoy-CE2 Ethernet interface.

In the SPI-3 receive to Ethernet Transmit direction, a prepended port number is required to de-multiplex the incoming packet stream on SPI-3 port 0 onto multiple Ethernet ports. The port number is assigned from 0 to 15 and a byte of packet data is used to convey this information. The appended port number will be removed before transmission onto the appropriate Ethernet interface.

6.3.1 Normal vs. Aggregate Mode

OPERATIONAL MODE	Default	Per Ethernet Port SPI-3 Tx Backpressure	Packet/ Chunk Tagging	PAUSE Frame support per Ethernet Port	SPI-3 Chunking	Number of SPI-3 Ports supported
NORMAL	Yes	Yes	No	Yes	Yes	Multiple
AGGREGATE	No	No	Yes	Yes	Yes	Single*

* **Note:** The single port is either in Multi-PHY or Single-PHY mode.

6.4 ETHERNET HALF DUPLEX

6.4.1 Overview

In Half-Duplex mode, two or more Ethernet devices are connected to a common transmission medium and when one Ethernet device transmits, the others listen. In the case where two Ethernet devices transmit at once, a "Collision" is said to have occurred. A "Jam Sequence" is transmitted by the transmitting Ethernet device indicating the occurrence of a collision. The contention is resolved by each of the Ethernet devices responsible for the collision, backing off, and attempting to re-transmit after a time period. This method is called Carrier Sense Multiple Access/Collision Detection (CSMA/CD). The Envoy-CE2 Configurable Media Access Controller implements the IEEE 802.3 compliant CSMA/CD algorithm. For a complete definition of this algorithm, please refer to the IEEE 802.3 specification.

Note: Carrier Sense and Collision detection status is indicated by the Ethernet PHY device to the Envoy-CE2 via the SMII and MII interface only. Please refer to the Serial Media Independent Interface (SMII) specification for further details.

Following is an outline based on the Envoy-CE2 Configurable MAC.

6.4.2 Carrier Sense

Following the transmission of an Ethernet frame from the Envoy-CE2, the MAC times the Inter Packet Gap (IPG) count as programmed in the Back-to-Back IPG configuration register for the specific port. The MAC monitors the Carrier Sense status for the duration of IPG time before transmitting a new frame for the port. Envoy-CE2 provides an optional IPG mechanism where the IPG time is divided into a two-thirds/one-third ratio. During the first two-thirds of the IPG, the IPG timer is reset and Carrier Sense status is monitored or sensed. During the final one-third of the IPG, the Carrier sense status is ignored and the port begins transmission once the IPG timer has expired. This optional mechanism enhances system robustness. The configuration bits defining the two-thirds/one-third values are IPG1 and IPG2.

6.4.3 Collision Detection

In the event the Envoy-CE2 MAC detects a collision for a port when the device is transmitting an Ethernet frame, the MAC outputs the 32-bit jam sequence for the port. The jam sequence is made up of several bits of the CRC, inverted to guarantee an invalid CRC upon reception of the frame. The port then backs off transmission of the frame (retry) based on the “Truncated Binary Exponential Backoff” (BEB) algorithm. Following this backoff time, the frame is retried. When enabled, the “No Backoff” configuration bit (Register 0x400C Bit 17) retransmits the frame without a backoff, following a collision. This option needs to be enabled with caution.

6.4.4 Alternate BEB Truncation

The backoff time following a collision is a controlled randomization process called “truncated binary exponential backoff”. It is defined as an integer multiple of the slot times. The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer r in the range: $0 \leq r \leq 2^k$ where k = min(n,10). So, after the first collision, the port will backoff either 0 or 1 slot times. After the fifth collision, the port will backoff between 0 and 32 slot times. After the tenth collision, the maximum number of slot times to backoff is 1024. By setting the Alternate BEB Enable bit (Register 0x400C Bit 19), the truncation point can be changed from min(n,10) to min(n,m) where m is set in the Alternate BEB Truncation register (Register 0x400C Bits 20-23).

6.4.5 Excessive Collisions

Upon collision, the port attempts re-transmission of the frame. Per the IEEE 802.3 specification, a frame has excessive collisions if 15 re-transmission attempts have occurred. The number of retransmission attempts for excessive collisions is configurable. In the event a frame has been excessively deferred, the frame is discarded and will not be transmitted. It is possible to configure the Envoy-CE2 not to discard an excessively deferred frame.

6.4.6 Half-Duplex Flow Control

There is no IEEE 802.3 compliant backpressure mechanism for Half Duplex. The common industry implementation is the “Raise Carrier” method. The Envoy-CE2 MAC uses the configurable “Raise Carrier” method for flow control in Half-Duplex mode. In the event the Envoy-CE2 port needs to backpressure the transmission medium, it raises carrier by transmitting the preamble. Other devices on the transmission medium defer to the carrier. If a collision occurs due to the raised carrier, the congestion is resolved using the standardized collision-detect, backoff method. The Host can not initiate flow control in half-duplex mode.

6.5 ETHERNET FULL DUPLEX

6.5.1 Overview

The Envoy-CE2 implements the IEEE 802.3 compliant full-duplex flow control mechanism. This mechanism is used to prevent frame loss, resulting from frame discard due to a buffer becoming full. It is intended for a Full-Duplex link between two devices; for example, a link between a switch and an end device (e.g., host). The mechanism involves the generation and operation of specific Ethernet Control frames called “PAUSE Control frames”. A PAUSE control frame has certain values for the Destination Address field, Type field, Opcode field, MAC control parameter field and must have a valid FCS. Following are the required PAUSE control frame field values.

The Destination address must either be the multicast address (01-80-C2-00-00-01) or the unicast address of the device the frame is being sent to. The Type field should have a reserved value of 0x8808 (MAC Control frame type) and the Control Opcode should be equal to 0x0001. A MAC control parameter called pause_time, specifies the time period, in 512-bit times, for which the device receiving the PAUSE control frame is paused.

The Flow control operation in the Envoy-CE2 is divided into two operations:

1) The action taken when a PAUSE control frame is received from a remote device

2) The action taken when Envoy-CE2 generates a PAUSE control frame and transmits it to a remote device.

The remote device is connected to the Envoy-CE2 via a full duplex link. Envoy-CE2 PAUSE frame processing needs to be enabled for the PAUSE frame flow control mechanism to take effect. An option is provided in the device to filter out the received PAUSE control frame.

6.5.2 PAUSE Control Frame Reception

Remote devices receiving Ethernet frames from Envoy-CE2 can backpressure Envoy-CE2, by sending a PAUSE control frame to Envoy-CE2. The backpressure may be needed if the buffer of the remote device on the link is becoming full. Upon reception of the PAUSE control frame, Envoy-CE2 will stop transmitting frames to the remote device. If Envoy-CE2 is in the middle of transmission of a frame, when it receives a PAUSE control frame, it will complete transmission of the frame and then pause transmission of any further Data frames. When Envoy-CE2 is in the pause state, it allows transmission of PAUSE control frames from the Envoy-CE2. The period for which Envoy-CE2 stays in a PAUSE state is defined by the pause_time parameter in the PAUSE control frame. The pause_time parameter is used as the initial value of an internal count down timer. This timer is started as soon as the pause_time parameter is loaded into the count down timer. Envoy-CE2 will stay in this

PAUSE state until the internal timer counts down to zero, in which case Envoy-CE2 will resume transmission of data frames to the remote device. If a PAUSE control frame with a new non zero pause_time parameter is received, the new pause_time is loaded into the internal down counter and the Envoy-CE2 stays in the PAUSE state for the time specified by the new pause_time. When a PAUSE frame with a timer parameter value of zero is received, the Envoy-CE2 will resume sending data frames to the remote device.

6.5.3 PAUSE Control Frame Generation

There are two modes for PAUSE Control Frame generation: Automatic PAUSE frame generation and Host initiated PAUSE frame generation.

6.5.3.1 Automatic PAUSE Frame Generation

In this mode, when the remote device sends Data frames to the Envoy-CE2 and the Ingress FIFO fills to a programmable High Watermark, Envoy-CE2's flow control mechanism is triggered and automatically generates a PAUSE control frame, which is sent after the current transfer is over. Envoy-CE2 transmits the frame to the remote device and backpressures the remote device. The pause_time value for the generated PAUSE control is programmable. Once the PAUSE control frame is transmitted, Envoy-CE2 will re-transmit another PAUSE control frame, every pause_retransmit_time, if a programmable Low Watermark is not reached in the Ingress FIFO. The effect of the re-transmitted PAUSE control frame on the remote device is that, it (remote device) is held in the PAUSE state and does not transmit data frames to Envoy-CE2. The value of pause_retransmit_time is programmable and is kept by the pause retransmit counter (down counter). In the event the Low Watermark is reached before the pause retransmit counter counts down to zero, Envoy-CE2 will transmit a PAUSE control frame with a pause_time value of zero to the remote device held in the pause state. The PAUSE control frame with pause_time value of zero will initiate resumption of transmission of data frames from the remote device to the Envoy-CE2.

6.5.3.2 Host Initiated PAUSE Frame Generation

The Host device can query Envoy-CE2 for the status of each Ingress FIFO (per channel). The values for the indication of near full status and near empty status, are programmable. They are the Ingress FIFO Control High and Low Watermarks associated with the Ingress FIFOs. The Envoy-CE2 provides the host with the ability to generate a PAUSE control frame from the Envoy-CE2. This is done by the Host enabling the PAUSE generate configuration bit. The Host can generate a PAUSE control frame with a non-zero value for pause_time, to the remote device across the link with Envoy-CE2, when the Ingress FIFOs reach the High Watermark and also generate a PAUSE control frame with a null value for pause_time, when the Ingress FIFO reaches the Low Watermark. This allows the Host to regulate the flow control mechanism.

7.0 MEMORY MAPS AND BIT DESCRIPTIONS

Envoy-CE2 Register Memory Map

Base Address (Hex)	Description	Size in bytes
0x0000	Host I/F Status and Configuration	8K
0x2000	Egress FIFO Status and Configuration Ingress FIFO Status and Configuration Output SPI-3 Status and Configuration Input SPI-3 Status and Configuration	8K
0x4000	Ethernet Status and Configuration for Port 0	256
0x4100	Ethernet Status and Configuration for Port 1	256
. . . Ethernet Status and Configuration for Port 2 ... Port 14 . . .		
0x4F00	Ethernet Port Status and Configuration for Port 15	256
0x6000	Ethernet Statistics for Port 0	256
0x6100	Ethernet Statistics for Port 1	256
. . . Ethernet Statistics for Port 2 .... Port 14 . . .		
0x6F00	Ethernet Statistics for Port 15	256

Note: Please refer to the above table for register addresses for Ethernet Status and Configuration for Port 1 to Port 15 and for register addresses for Ethernet Statistics for Port 1 to Port 15. The SMIIREFCLK for each of the two CMACs must be active for these registers to operate correctly - even when the CMAC is configured in GMII mode.

Mode Description

Mode	Description
RO	Read Only Register
RW	Read/Write Register
RC	Clear On Read Register/Counter that saturated. Note: RMON counters are clear on read saturating counters or rollover counters. This option is programmable.

Host Interface Configuration and Status Register Map

Address	31							24	23						16	15							8	7							0
0x0000	DeviceID																														
0x0004	Reserved																														
0x0008	ScratchReg																														
0x000C	Reserved																														
0x0010	Reserved															ResetControl															
0x0014	Reserved																							ResetControl							
0x0018	Reserved															IrqMask															
0x001C	Reserved																							IrqMask							
0x0020	Reserved															IrqStatus															
0x0024	Reserved																							IrqStatus							
0x0028	CfgPins																														
0x002C	Reserved																								*	Reserved					
0x0030	Reserved																													GlobalControl	
0x0034	Reserved															StatIrqStatus															
0x0038	Reserved															StatIrqMask															
0X003C	Reserved																														
0x0040	MII MGMT Configuration																														
0x0044	MII MGMT Command																														
0x0048	MII MGMT Address																														
0x004C	MII MGMT Control																														
0x0050	MII MGMT Status																														
0x0054	MII MGMT Indicators																														

* This is an Oversubscription enable bit.

Host Interface Status and Configuration Register Definitions

Addr (hex)	Mode	Bit range	Default value after reset	Description
0000	RO	0	1	Reserved
		11-1	06B	**TXC Manufacturing ID:** This field contains the manufacturer identification number for TranSwitch Corp., which is 0x06B.
		27-12	1AE0	**ENVOY ID**: This field contains the Envoy-CE2 part number, TXC-06880.
		31-28	1	**Device Version Level.** This field is 1.
0004	RO	31-0	0	Reserved
0008	RW	31-0	12345678	**Scratchpad Memory.** 32-bits of memory storage available to the host processor.
000C	RO	31-0	0	Reserved
0010	RW	0	0	**Reset Ethernet Port 0:** Writing a 1 to this bit will reset the Ethernet Port 0. The host may access this register when the Ethernet Port 0 is in reset state. A read will always return a 0.
		1	0	**Reset Ethernet Port 1:** Writing a 1 to this bit will reset the Ethernet Port 1. The host may access this register when the Ethernet Port 1 is in reset state. A read will always return a 0.
	RW	15	0	**Reset Ethernet Port 15:** Writing a 1 to this bit will reset the Ethernet Port 15. The host may access this register when the Ethernet Port 15 is in reset state. A read will always return a 0.
	RO	31-16	0	Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
0014	RW	0	0	**Reset Ingress FIFO:** Writing a 1 to this bit will reset the Ingress FIFO for all ports. The host may access this register when the Ingress FIFO is in reset state. Note: This Reset will reset the block specific configuration registers.
		1	0	**Reset SPI-3 Output:** Writing a 1 to this bit will reset the SPI-3 output interface. The host may access this register when the SPI-3 output is in reset state. Note: This Reset will reset the block specific configuration registers.
		2	0	**Reset Egress FIFO:** Writing a 1 to this bit will reset the Egress FIFO for all ports. The host may access this register when the Egress FIFO is in reset state. Note: This Reset will reset the block specific configuration registers.
		3	0	**Reset SPI-3 Input:** Writing a 1 to this bit will reset the SPI-3 input interface. The host may access this register when the SPI-3 input is in reset state. Note: This Reset will reset the block specific configuration registers.
		4	0	**Reset MII Management Port:** Writing a 1 to this bit will reset the MII management port. The host may access this register when the MII management port is in reset state. Note: This Reset will reset the block specific configuration registers.
		5	0	**Reset Ethernet Statistics Module:** Writing a 1 to this bit will reset the Ethernet statistics module. The host may access this register when the Ethernet statistics module is in reset state. Note: This Reset will reset the block specific configuration registers.
	RO	31-6	0	Reserved
0018	RW	0	1	**Interrupt Mask for Ethernet Port 0:** Writing a 1 to this bit will mask the interrupt from Ethernet Port 0. Writing a 0 to this bit will enable interrupts from Ethernet Port 0.
		1	1	**Interrupt Mask for Ethernet Port 1:** Writing a 1 to this bit will mask the interrupt from Ethernet Port 1. Writing a 0 to this bit will enable interrupts from Ethernet Port 1.
	RW	15	1	**Interrupt Mask for Ethernet Port 15:** Writing a 1 to this bit will mask the interrupt from Ethernet Port 15. Writing a 0 to this bit will enable interrupts from Ethernet Port 15.
	RO	31-16		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
001C	RW	0	1	**Interrupt Mask for Ingress FIFO:** Writing a 1 to this bit will mask the interrupt from the Ingress FIFO. Writing a 0 to this bit will enable interrupts from the Ingress FIFO.
		1	1	**Interrupt Mask for SPI-3 Output Interface:** Writing a 1 to this bit will mask the interrupt from the SPI-3 output interface. Writing a 0 to this bit will enable interrupts from the SPI-3 output interface.
		2	1	**Interrupt Mask for Egress FIFO:** Writing a 1 to this bit will mask the interrupt from the Egress FIFO. Writing a 0 to this bit will enable interrupts from the Egress FIFO.
		3	1	**Interrupt Mask for SPI-3 Input Interface:** Writing a 1 to this bit will mask the interrupt from the SPI-3 input interface. Writing a 0 to this bit will enable interrupts from the SPI-3 input interface.
		4	1	**Interrupt Mask for Ethernet Statistics Module:** Writing a 1 to this bit will mask the interrupt from the Ethernet Statistics module. Writing a 0 to this bit will enable interrupts from the Ethernet Statistics module.
		5	1	**Interrupt Mask for MII Management Module:** Writing a 1 to this bit will mask the interrupt from the MII management module. Writing a 0 to this bit will enable interrupts from the MII management module.
	RO	31-6	0	Reserved
0020	RO	0	0	**Interrupt Status for Ethernet Port 0:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		1	0	**Interrupt Status for Ethernet Port 1:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
	RO	15	0	**Interrupt Status for Ethernet Port 15:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		31-16		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
0024	RO	0	0	**Interrupt Status for Ingress FIFO:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		1	0	**Interrupt Status for SPI-3 Output Interface:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		2	0	**Interrupt Status for Egress FIFO:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		3	0	**Interrupt Status for SPI-3 Input Interface:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		4	0	**Interrupt Status for Ethernet Statistics Module:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		5	0	**Interrupt Status for MII Management Module:** A 1 indicates the occurrence of an interrupt in this module. Clearing of the interrupts must be done at the source. Refer to the section for each module.
		31-6	0	Reserved
0028	RO	1-0		**CMAC A Pin Configuration:** Reflection of the Configuration Pin for configuring MAC A (Pin - CFGCMACA[1:0]) 00 - OFF 01 - 1 GMII/MII 10 - 2 Extended SMII 11 - 8 SMII
		3-2		**CMAC B Pin Configuration:** Reflection of the Configuration Pin for configuring MAC B (Pin - CFGCMACB[1:0]) 00 - OFF 01 - 1 GMII/MII 10 - 2 Extended SMII 11 - 8 SMII
		15-4	0	Reserved
		16		**SPI-3 INPUT MODE Pin Configuration:** Reflection of the Configuration Pin for configuring the SPI-3 Input Mode (CFGISPIMD) 0 - SPI-3 in PHY (Slave) mode 1 - SPI-3 in Link (Master) mode

Addr (hex)	Mode	Bit range	Default value after reset	Description
0028 (cont.)	RO	17		**SPI-3 OUTPUT MODE Pin Configuration:** Reflection of the Configuration Pin for configuring the SPI-3 Output Mode (CFGOSPIMD) 0 - SPI-3 in Slave mode 1 - SPI-3 in Master mode
		19-18		**SPI-3 Bus Width Pin Configuration:** Reflection of the Configuration Pin for configuring the SPI-3 Bus width (CFGOSPIBW[1:0]) 00 - 32-bit mode 01 - 16-bit mode 10 - 8-bit mode 11 - Reserved
		25-20	0	Reserved
		26		**Host Interface Bus Width Pin Configuration:** Reflection of the Configuration Pin for configuring the Host Interface Bus Width (CFGUPBW) 0 - 16 bits 1 - 8 bits
		27		**Host Interface Selection Pin Configuration:** Reflection of the Configuration Pin for configuring the Host Interface type, Intel or Motorola (CFGUPMD) 0 - Host Interface in Intel Mode 1 - Host Interface in Motorola Mode
		28		**SMII SYNC Direction Selection Pin:** Reflection of the Configuration Pin for configuring the SMII Sync Signal direction (SSYNCDIR) 0 - The synchronization pulse will be taken from an internally generated source 1 - The synchronization pulse to the 8 SMII ports will be taken from SSYNCIN
		31-29	0	Reserved
002C	RO	3-0	0	Reserved
	RW	4	0	**Oversubscription Enable:** Valid in SPI-3 Link (master) mode only. 0 - The ISPIRENB output pin is used to apply SPI-3 standard backpressure 1 - Allows an external SPI-3 PHY (slave) device to push data into the SPI-3 input without ever being backpressured
	RW	31-5	0	Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
0030	RW	0	1	**RMON Statistics Counter Auto Clear On Read:** 0 - Statistics counter is not cleared on read and counter rolls over to 0 when it reaches maximum value 1 - Statistics counter is automatically cleared after it is read and counter will saturate at maximum value
		1	0	**Received Byte Counter Config:** 0 - The receive byte counter includes bytes from errored packets 1 - The receive byte counter only counts bytes from good packets
	RO	31-2	0	Reserved
0034	RO	0	0	**Interrupt Status for Ethernet Port 0 Ethernet Statistics:** A 1 indicates the occurrence of an interrupt from the Ethernet Statistics block for Ethernet Port 0.
		15-1	0	**Interrupt Status for Ethernet Ports 1 to 15 Ethernet Statistics**
		31-16	0	Reserved
0038	RW	0	0	**Interrupt Mask for Ethernet Port 0 Ethernet Statistics:** A 1 masks the interrupt from the Ethernet Statistics block for Ethernet Port 0.
		15-1	0	**Interrupt Mask for Ethernet Ports 1 to 15 Ethernet Statistics**
		31-16	0	Reserved
003C	RO	31-0	0	Reserved

<table>
<tr><th>Addr (hex)</th><th>Mode</th><th>Bit range</th><th>Default value after reset</th><th>Description</th></tr>
<tr><td rowspan="6">0040</td><td>RW</td><td colspan="3">MII MGMT: CONFIGURATION REGISTER</td></tr>
<tr><td>RW</td><td>2-0</td><td>0</td><td>MGMT Clock Select: This field determines the clock frequency of the MGMT Clock (MDC). Consult Table below - MGMT Clock Select Encoding on how to program this field.
MGMT Clock Select Encoding
<table>
<tr><th>MGMT Clock Select Bits</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>UPCLK divided by 4</td><td>0</td><td>0</td><td>X</td></tr>
<tr><td>UPCLK divided by 6</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>UPCLK divided by 8</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>UPCLK divided by 10</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>UPCLK divided by 14</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>UPCLK divided by 20</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>UPCLK divided by 28</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>RO</td><td>3</td><td></td><td>Reserved</td></tr>
<tr><td>RW</td><td>4</td><td>0</td><td>Preamble Suppression:
0 - MII MGMT will perform MGMT read/write cycles with the 32 clocks of preamble
1 - MII MGMT will suppress preamble generation and reduce the MGMT cycle from 64 clocks to 32 clocks per IEEE 802.3/22.2.4.4.2</td></tr>
<tr><td></td><td>5</td><td>0</td><td>PHY/Register Scan Enable: When Scan Mode Enable is enabled, this bit determines whether or not to increment the PHY or register address for the next read cycle.
1 - Increment address</td></tr>
<tr><td></td><td>6</td><td>0</td><td>Scan Register Increment Select: - When Scan Mode Enable is enabled, this bit determines whether to increment the Register address or the PHY address.
0 - Increment PHY address, allows read scan of the same register in all PHYs
1 - Increment register address, allows read scan of all registers in a specific PHY</td></tr>
<tr><td></td><td>RO</td><td>31-7</td><td></td><td>Reserved</td></tr>
</table>

Addr (hex)	Mode	Bit range	Default value after reset	Description
0044	RW			**MII MGMT: COMMAND REGISTER**
		0	0	**READ Operation Enable:** Low to High transition initiates a Read cycle. The read data is returned in the MII MGMT Read Data register. In scan mode, after each read of the Read Data register, another Read cycle is performed.
		1	0	**SCAN Mode Enable:** When 1 and Read operation is enabled, causes the MII Management to perform Read cycles automatically.
	RO	31-2	0	Reserved
0048	RW			**MII MGMT: ADDRESS REGISTER**
		4-0	0	**Register Address:** This field represents the 5-bit Register Address field of MGMT cycles. Up to 32 registers can be accessed. If scanning across multiple registers in a PHY is enabled, then load the address of the last PHY to be scanned here.
	RO	7-5		Reserved
	RW	12-8	0	**PHY Address:** This field represents the 5-bit PHY Address field of MGMT cycles. Up to 32 PHYs can be addressed. If scanning across multiple PHYs (Scan PHY Mode), then load the address of the last PHY to be scanned here.
	RO	31-13		Reserved
004C	RW			**MII MGMT: Data Write**
		15-0	0	**MII MGMT Write:** When written, an MII MGMT write cycle is performed using the 16-bit data and the pre-configured PHY and Register addresses from the MII MGMT Address Register (0x0048).
	RO	31-16		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
0050	RO			**MII MGMT: Data Read**
		15-0	0	**MII MGMT Read Data:** Following an MII MGMT Read Cycle, the 16-bit data can be read from this location.
		20-16	0	**MII MGMT Read Register Address:** Following an MII MGMT Read Cycle, the 5-bit register address of the register that was accessed can be read from this location. This eases reading registers in scan mode.
		23-21		Reserved
		28-24	0	**MII MGMT Read PHY Address:** Following an MII MGMT Read Cycle, the 5-bit PHY number of the register that was accessed can be read from this location. This eases reading registers in scan mode.
		30-29		Reserved
		31	0	**Read Busy:** 1 - Indicates MII MGMT block is currently performing an MII MGMT Read cycle
0054	RO			**MII MGMT: INDICATORS**
		0	0	**Busy:** 1 - Indicates MII MGMT block is currently performing an MII MGMT Read or Write cycle
		31-1		Reserved

Egress/Ingress FIFO and SPI-3 Input/Output, Status, and Control Register Map

Address	31	24	23	16	15	8	7	0
2000	Reserved		SPI-3 Input Mode		Reserved			
2004	Reserved				SPI-3 Input PHY Enable			
2008	Reserved						SPI-3 Input STPA Low Threshold	
200C	Reserved						SPI-3 Input STPA High Threshold	
2010	Reserved						SPI-3 Input PTPA Low Threshold	
2014	Reserved						SPI-3 Input PTPA High Threshold	
2018	Reserved							
201C	Reserved							
2040	Reserved						SPI Input Error Status	
2050	Reserved						SPI-3 Input Interrupt Mask	
2060	SPI-3 Input Parity Error Counter							
2064	SPI-3 Input Start of Packet Error Counter							
2068	Reserved							
2080	SPI-3 Input Packet Error Counter Port 0							
2084	SPI-3 Input Packet Error Counter Port 1							
	.....							
20BC	SPI-3 Input Packet Error Counter Port 15							
2200	Reserved					SPI-3 Output Config		
2204	Reserved				SPI-3 Output PHY Enable			
2208	Reserved						SPI-3 Output STPA Threshold	
220C	Reserved						SPI-3 Output Burst Size	
2210	Reserved							STPAEN
2214	Reserved							PTPAEN
2280	SPI-3 Output Aggregation Mode Tag Port 0							
2284	SPI-3 Output Aggregation Mode Tag Port 1							
	.....							
22BC	SPI-3 Output Aggregation Mode Tag Port 15							
2400	Egress FIFO Packet Drop Counter Port 0							
2404	Egress FIFO Packet Drop Counter Port 1							
	....							
243C	Egress FIFO Packet Drop Counter Port 15							
2500	Reserved				Per Port Egress FIFO Full Status			

Address	31	24	23	16	15	8	7	0
2504	Reserved				Per Port Egress FIFO Disabled Error Status			
2508	Reserved				Per Port Egress FIFO Start of Packet Error Status			
2540	Reserved							EFIFOMD
2544	Reserved				Per Port Egress FIFO Full Interrupt Mask			
2548	Reserved				Per Port Egress FIFO Disabled Port Error Interrupt Mask			
254C	Reserved				Per Port Egress FIFO Packet Discard Error Interrupt Mask			
2550	Reserved				Per Port Egress FIFO PHY/Port Enable			
2580	Reserved							STRTH0
2584	Reserved							STRTH1
25BC	Reserved							STRTH15
2600	Ingress FIFO Packet Drop Counter Port 0							
2604	Ingress FIFO Packet Drop Counter Port 1							
263C	Ingress FIFO Packet Drop Counter Port 15							
2700	Reserved				Per Port Ingress FIFO Full Status			
2704	Reserved				Per Port Ingress FIFO Near Full Status			
2780	Reserved							IFIFOMD
2784	Reserved							LPBK
2788	Reserved							NOLPBK
278C	Reserved				PAUSE Frame High Threshold CMAC A			
2790	Reserved				PAUSE Frame Low Threshold CMAC A			
2794	Reserved				PAUSE Frame High Threshold CMAC B			
2798	Reserved				PAUSE Frame Low Threshold CMAC B			
27AC	Reserved				PAUSE Frame Regeneration Timer CMAC A			
27B0	Reserved				PAUSE Frame Regeneration Timer CMAC B			
27BC	Reserved				Per Port Ingress FIFO Full Interrupt Mask			
27C0	Reserved				Per Port Ingress FIFO Near Full Interrupt Mask			
27C4	Reserved				Per Port Ingress PHY/Port Enable			

Egress/Ingress FIFO and SPI-3 Input/Output, Status, and Control Register Map

Addr (hex)	Mode	Bit range	Default value after reset	Description
2000	RO			**SPI-3 Input Configuration**
		15-0		Reserved
	RW	16	0	**SPI-3 Input Single-PHY Enable:** The SPI-3 Single-PHY mode enable bit. 0 - Multi-PHY 1 - Single-PHY
		17	0	**SPI-3 Input Aggregation Mode Enable:** The Aggregation Mode Enable bit for SPI-3 Input. 0 - Normal mode 1 - Aggregate mode
		19-18	00	**Aggregate Mode TAG Position:** The Ethernet Aggregate Mode Tag Position. This indicates the byte position in the Aggregate Tag word (4 bytes long), which indicates the PHY number of the packet.
		20	1	**SPI-3 Input Parity Mode:** SPI-3 Input interface parity mode. 0 - Even parity 1 - Odd parity
		21	1	**SPI-3 Input Parity Enable:** SPI-3 Input interface parity checking enable bit. 0 - Parity checking not enabled 1 - Parity checking enabled
	RO	31-22		Reserved
2004	RW	15-0	00000000	**SPI-3 Input PHY/Port Enable Per Port:** SPI-3 Input PHY/Port Enable bits for the 16 SPI-3 Input ports (one per port). Bit 0 = Port 0, Bit 1 = Port 1..... Bit 15 = Port 15.
	RO	31-16	0000	Reserved
2008	RW	7-0	00000000	**SPI-3 Input STPA Low Threshold:** Input SPI-3 near full low threshold for assertion of STPA. Once STPA is de-asserted because the Egress FIFO reached the SPI-3 high threshold (SISHT), STPA will be asserted when the Egress FIFO reaches the STPA low threshold. This allows for a hysteresis in the STPA signal. For a bus width of 8 bits, the value is based on bytes. For a bus width of 16 bits, 2 bytes and a bus width of 32 bits, 4 bytes. Minimum value is 2.
	RO	31-8		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
200C	RW	7-0	00000000	**SPI-3 Input STPA High Threshold:** Input SPI-3 near full high threshold for de-assertion of STPA. The high threshold is the fullness level and when reached by the Egress FIFO will de-assert STPA. The value is specified in terms of the SPI-3 bus width. For a bus width of 8 bits, the value is based on bytes. For a bus width of 16 bits, 2 bytes and a bus width of 32 bits, 4 bytes. Minimum value is 2.
	RO	31-8		Reserved
2010	RW	7-0	00000000	**SPI-3 Input PTPA Low Threshold:** Input SPI-3 near full low threshold for assertion of PTPA. Once the PTPA is de-asserted because the Egress FIFO reached the SPI-3 high threshold (SIPHT), PTPA will be asserted when the Egress FIFO reaches the PTPA low threshold. This allows for a hysteresis in the PTPA signal. The threshold is in words (8 bytes). Programmable values are 1 to 255 which corresponds to threshold values of 8 to 2040, in 8 byte increments.
	RO	31-8		Reserved
2014	RW	7-0	00000000	**SPI-3 Input PTPA High Threshold:** Input SPI-3 near full high threshold for de-assertion of PTPA. The high threshold is the fullness level in words (8 bytes), when reached by the Egress FIFO will de-assert PTPA. Programmable values are 1 to 255 which corresponds to threshold values of 8 to 2040, in 8 byte increments. The PTPA High Threshold should be set to at least 3 times the chunk size being used in the attached device (associated with ISPI flow).
	RO	31-8		Reserved
2018	RW	0	1	**Reserved** **Must be set to 0 for normal operation.**
	RO	31-1	0	Reserved
201C	RO	31-0	0	Reserved
2040	RC	0	0	**SPI-3 Input Overflow Discard Status:** Status bit indicating overflow due to the Link layer device ignoring the Packet available signals (STPA). Occurs when the SPI-3 Input interface is in PHY mode and **SPI-3 Input STPA Enable = 1**. Clear on Read.
		1	0	**SPI-3 Input Parity Error Status:** Status bit indicating occurrence of Parity error across the SPI-3 Input Interface bus. Clear on Read.
		2	0	**SPI-3 Input Packet Error Status:** Status bit indicating occurrence of Packet error across the SPI-3 Input Interface indicated by the Error signal. Clear on Read.
		3	0	**SPI-3 Input Start of Packet Error Status:** Status bit indicating occurrence of Start of Packet error across the SPI-3 Input Interface. Clear on Read.
	RO	31-4		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
2050	RW	0	1	**SPI-3 Input Overflow Discard Interrupt Mask:** Interrupt Mask for SPI-3 Input Overflow Discard Status based interrupt. 0 = Disables Mask, 1 = Enables Mask.
		1	1	**SPI-3 Input Parity Error Interrupt Mask:** Interrupt Mask for SPI-3 Input Parity Error Status based interrupt. 0 = Disables Mask, 1 = Enables Mask.
		2	1	**SPI-3 Input Packet Error Interrupt Mask:** Interrupt Mask for SPI-3 Input Packet Error Status based interrupt. 0 = Disables Mask, 1 = Enables Mask.
		3	1	**SPI-3 Input Start of Packet Error Interrupt Mask:** Interrupt Mask for SPI-3 Input Start of Packet Error Status based interrupt. 0 = Disables Mask, 1 = Enables Mask.
	RO	31-4		Reserved
2060	RC	31-0	00000000	**SPI-3 Input Parity Error Counter:** Counter indicating the number of Parity Errors across the SPI-3 Input interface. Clear on Read.
2064	RC	31-0	00000000	**SPI-3 Input Start of Packet Error Counter:** Counter indicating the number of Start of Packet Errors across the SPI-3 Input interface. Clear on Read.
2068	RO	31-0	00000000	Reserved
2080	RC	31-0	00000000	**SPI-3 Input Packet Error Counter Port 0:** Counter indicating the number of SPI-3 Ingress Packet Errors indicated over the SPI-3 Error pin for Port 0. Clear on Read.
2084	RC	31-0	00000000	**SPI-3 Input Packet Error Counter Port 1:** Counter indicating the number of SPI-3 Ingress Packet Errors indicated over the SPI-3 Error pin for Port 1. Clear on Read.
. **SPI-3 Input Packet Error Counter for Port 2 to Port 14** .				
20BC	RC	31-0	00000000	**SPI-3 Input Packet Error Counter Port 15:** Counter indicating the number of SPI-3 Ingress Packet Errors indicated over the SPI-3 Error pin for Port 15. Clear on Read.

Addr (hex)	Mode	Bit range	Default value after reset	Description
2200	RW	2-0	0	**SPI-3 Base Address:** The 3 bit base address used to create the 8 bit SPI-3 port address for both SPI-3 Input and SPI-3 output. The base address is a 3 bit programmable value and is assigned to the most significant 3 bits of the 8 bit SPI-3 address. Individual SPI-3 port address are calculated by adding the (base address x 32) to the logical Ethernet port number.
	RO	3	0	Reserved
	RW	4	1	**SPI-3 Output Pause Cycle Time:** The minimum Pause time between transfers in SPI-3 clock cycles. Only used in PHY mode. 0 - 0 cycles 1 - 2 cycles
		5	0	**SPI-3 Output Single-PHY Enable:** The SPI-3 Single-PHY mode enable bit. 0 - Multi-PHY 1 - Single-PHY
		6	0	**SPI-3 Output Aggregation Mode Enable:** The Aggregation Mode Enable bit for SPI-3 Output. 0 - Normal mode 1 - Aggregate mode
		7	1	**SPI-3 Output Parity Mode:** SPI-3 Output interface parity mode. 0 - Even parity 1 - Odd parity
		8	1	**SPI-3 Output Parity Enable:** SPI-3 Output interface parity generation enable bit. 0 - Parity generation not enabled 1 - Parity generation enabled
		9	0	**SPI-3 Output Mode:** Bit to enable SPI-3 output mode. 0 - Burst (Chunk) Mode. In Burst mode, a configured number of bytes (**SPI-3 Output Burst Size**) is sent across the SPI-3 interface before a re-selection. 1 - Packet Mode. In Packet mode, a complete packet is sent across the SPI-3 interface by a port before a port re-selection.
	RO	31-10		Reserved
2204	RW	31-0	00000000	**SPI-3 Output PHY/Port Enable Per Port:** SPI-3 Output PHY/Port Enable bits for the 16 SPI-3 Output ports (one per port).
2208	RW	7-0	00000000	**SPI-3 Output STPA Near Full Threshold:** Output SPI-3 near full threshold for de-assertion of STPA.
	RO	31-8		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
220C	RW	7-0	00000000	**SPI-3 Output Burst Size:** Output SPI-3 Burst Size when the SPI-3 output is in Burst Mode (**SPI-3 Output Mode = 0**). The unit is in 8 byte words. Programmable values are 1 to 255 which corresponds to threshold values of 8 to 2040, in 8 byte increments.
	RO	31-8		Reserved
2210	RW	0	1	**SPI-3 Output STPA Enable:** Bit to enable usage of STPA when the SPI-3 Output interface is in Link (Master) mode.
	RO	31-1		Reserved
2214	RW	0	1	**SPI-3 Output PTPA Enable:** Bit to enable usage of PTPA when the SPI-3 Output interface is in Link (Master) mode.
	RO	31-1		Reserved
2280	RW	31-0	00000000	**SPI-3 Output Aggregation Mode Tag Port 0:** The Aggregation Tag for Port 0 that is prepended to each packet/chunk, when in Aggregation mode (**SPI-3 Output Aggregation Mode Enable = 1)**.
2284	RW	31-0	00000000	**SPI-3 Output Aggregation Mode Tag Port 1:** The Aggregation Tag for Port 1 that is prepended to each packet/chunk, when in Aggregation mode (**SPI-3 Output Aggregation Mode Enable = 1)**.
. **SPI-3 Output Aggregation Mode Tags for Port 2 to Port 14** .				
22BC	RW	31-0	00000000	**SPI-3 Output Aggregation Mode Tag Port 15:** The Aggregation Tag for Port 15 that is prepended to each packet/chunk, when in Aggregation mode (**SPI-3 Output Aggregation Mode Enable = 1)**.
2400	RC	31-0	00000000	**Egress FIFO Packet Drop Counter Port 0:** The Egress FIFO Packet Drop Counter counts dropped packets for either of the following conditions: (a) Start of Packet and End of Packet in the same word (b) Assertion of the SPI-3 Error pin after a start of packet has been received. (c) An overflow occurred in the Egress FIFO. Packets are dropped in store and forward mode only (**Egress FIFO Mode = 0**). Clear on Read.
2404	RC	31-0	00000000	**Egress FIFO Packet Drop Counter Port 1:** The Egress FIFO Packet Drop Counter counts dropped packets for either of the following conditions: (a) Start of Packet and End of Packet in the same word (b) Assertion of the SPI-3 Error pin after a start of packet has been received. (c) An overflow occurred in the Egress FIFO. Packets are dropped in store and forward mode only (**Egress FIFO Mode = 0**). Clear on Read.

Addr (hex)	Mode	Bit range	Default value after reset	Description
. **Egress FIFO Packet Drop Counter for Port 2 to Port 14** .				
243C	RC	31-0	00000000	**Egress FIFO Packet Drop Counter Port 15:** The Egress FIFO Packet Drop Counter counts dropped packets for either of the following conditions: (a) Start of Packet and End of Packet in the same word (b) Assertion of the SPI-3 Error pin after a start of packet has been received. (c) An overflow occurred in the Egress FIFO. Packets are dropped in store and forward mode only (**Egress FIFO Mode = 0**). Clear on Read.
2500	RC	15-0	0000	**Egress FIFO Full Status Per Port:** Indication of Egress FIFO for all 16 ports. When 1, indicates the FIFO Full state. Clear on Read.
	RO	31-16	0000	Reserved
2504	RC	15-0	0000	**Egress FIFO Disabled Error Status Per Port:** Indication of Egress FIFO Error when a disabled port (done through configuration register **Egress FIFO PHY/Port Enable**) receives packet data from the SPI-3 interface. The packet data is discarded. When 1, indicates the occurrence of the error. Clear on Read.
	RO	31-16	0000	Reserved
2508	RC	15-0	0000	**Egress FIFO Start of Packet Error Status Per Port:** Indication of Egress FIFO Start of Packet Error. The error status is indicated on the reception of packet data without the reception of a Start of Packet, after an End of Packet. When 1, indicates the occurrence of the error. Clear on Read.
	RO	31-16	0000	Reserved
2540	RW	0	0	**Egress FIFO Mode:** This bit sets the FIFO mode for all Egress FIFOs. 0 - Store and Forward Mode 1 - Streaming Mode
	RO	31-1	0	Reserved
2544	RW	15-0	FFFF	**Egress FIFO Full Interrupt Mask Per Port:** FIFO full interrupt mask for the 16 Egress FIFOs (one per port). A 0 disables the mask and an interrupt will be generated when the appropriate FIFO becomes full. The interrupt is cleared by reading the status register **Egress FIFO Full Status Per Port**. If this bit is 1, no interrupt will be generated.
	RO	31-16	FFFF	Reserved
2548	RW	15-0	FFFF	**Egress FIFO Disabled Error Interrupt Mask Per Port:** Disabled Egress FIFO Error interrupt mask for the 16 Egress FIFOs (one per port). A 0 disables the mask and an interrupt will be generated when the appropriate FIFO/Port is disabled and receives data for a write. The interrupt is cleared by reading the status register **Egress FIFO Disabled Error Status**. If this bit is 1, no interrupt will be generated.
	RO	31-16	FFFF	Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
254C	RW	15-0	FFFF	**Egress FIFO Start of Packet Error Interrupt Mask Per Port:** Egress FIFO Start of Packet Error interrupt mask for the 16 Egress FIFOs (one per port). A 0 disables the mask. An interrupt will be generated when the appropriate FIFO/Port receives consecutive End of Packets. The interrupt is cleared by reading the status register **Egress FIFO Start of Packet Error Status.** If this bit is 1, no interrupt will be generated.
	RO	31-16	FFFF	Reserved
2550	RW	15-0	FFFF	**Egress FIFO PHY/Port Enable Per Port:** Egress FIFO/Port Enable bits for the 16 Egress FIFOs (one per port).
	RO	31-16	FFFF	Reserved
2580	RW	2-0	0	**Egress FIFO Streaming Threshold Port 0:** Egress FIFO Streaming threshold in bytes for Port 0. The values are: 000 - 64 Bytes 001 - 128 Bytes 010 - 256 Bytes 011 - 512 Bytes 100 - 768 Bytes 101 - 1544 Bytes 110 & 111 - Reserved When the Port is in Streaming mode and the Egress FIFO reaches the programmed threshold, an indication is sent to the associated Configurable MAC block to transfer the Port's Packet Data across the Ethernet interface.
	RO	31-3		Reserved
2584	RW	2-0	0	**Egress FIFO Streaming Threshold Port 1:** Egress FIFO Streaming threshold in bytes for Port 1. The values are: 000 - 64 Bytes 001 - 128 Bytes 010 - 256 Bytes 011 - 512 Bytes 100 - 768 Bytes 101 - 1544 Bytes 110 & 111 - Reserved When the Port is in Streaming mode and the Egress FIFO reaches the programmed threshold, an indication is sent to the associated Configurable MAC block to transfer the Port's Packet Data across the Ethernet interface.
	RO	31-3		Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
				Egress FIFO Streaming Threshold for Port 2 to Port 14
25BC	RW	2-0	0	**Egress FIFO Streaming Threshold Port 15:** Egress FIFO Streaming threshold in bytes for Port 15. The values are: 000 - 64 Bytes 001 - 128 Bytes 010 - 256 Bytes 011 - 512 Bytes 100 - 768 Bytes 101 - 1544 Bytes 110 & 111 - Reserved When the Port is in Streaming mode and the Egress FIFO reaches the programmed threshold, an indication is sent to the associated Configurable MAC block to transfer the Port's Packet Data across the Ethernet interface.
	RO	31-3		Reserved
2600	RC	31-0	00000000	**Ingress FIFO Packet Drop Counter Port 0:** The Ingress FIFO Packet Drop Counter counts dropped packets due to the MAC detecting an error. Packets are dropped in store and forward mode only (**Ingress FIFO Mode = 0**). Clear on Read.
2604	RC	31-0	00000000	**Ingress FIFO Packet Drop Counter Port 1:** The Ingress FIFO Packet Drop Counter counts dropped packets due to the MAC detecting an error. Packets are dropped in store and forward mode only (**Ingress FIFO Mode = 0**). Clear on Read.
				Ingress FIFO Packet Drop Counter for Port 2 to Port 14
263C	RC	31-0	00000000	**Ingress FIFO Packet Drop Counter Port 15:** The Ingress FIFO Packet Drop Counter counts dropped packets due to the MAC detecting an error. Packets are dropped in store and forward mode only (**Ingress FIFO Mode = 0**). Clear on Read.
2700	RC	15-0	0000	**Ingress FIFO Full Interrupt Status Per Port:** FIFO full Status for the 16 Ingress FIFOs (one per port).
	RO	31-16	FFFF	Reserved
2704	RC	15-0	0000	**Ingress FIFO Near Full Interrupt Status:** FIFO Near full Status for the 16 Ingress FIFOs (one per port). A Port will go into a near full condition when its Ingress FIFO level goes beyond the Pause Frame High Threshold value associated with that port.
	RO	31-16	FFFF	Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
2780	RW	0	0	**Ingress FIFO Mode:** This bit sets the FIFO mode for all Ingress FIFOs. 0 - Store and Forward Mode 1 - Streaming Mode
	RO	31-1	0	Reserved
2784	RW	0	0	**Ingress FIFO LoopBack Enable:** This bit sets the FIFO mode in loopback mode. Packets from the Ingress FIFO will be loop backed onto the Egress FIFO. *Note: The output SPI-3 must be in slave mode*. This loopback can support a maximum of 800 Mbit/s.
	RO	31-1	0	Reserved
2788	RW	0	0	**Ingress FIFO LoopBack Block SPI-3:** If this bit is set to 1 with the Ingress FIFO LoopBack enabled (**Ingress FIFO LoopBack Enable = 1**), packet data looped back will not appear at the SPI-3 output interface. When set to 0 and Ingress FIFO Loopback enabled, packet data will loopback to the Egress FIFO and appear at the SPI-3 output interface. *Note: For this mode to work, the Output SPI-3 Enable pin needs to be asserted*.
	RO	31-1	0	Reserved
278C	RW	12-0	1FFF	**Flow Control High Threshold CMAC A:** This register sets the high threshold in multiples of 8 bytes, for Ports 0 to 7 (serviced by Configurable MAC A), for generation of PAUSE frames or asserting raise carrier. In the event one of the Ethernet port's ingress FIFO (serviced by Configurable MAC A) reaches this threshold, a Pause frame will be sent or raise carrier will be asserted from that port. *Note: Automatic pause frame generation needs to be enabled*.
	RO	31-13	0	Reserved
2790	RW	12-0	1FFF	**Flow Control Low Threshold CMAC A:** This register sets the low threshold in multiples of 8 bytes, for Ports 0 to 7 (serviced by Configurable MAC A), to stop generation of PAUSE frames or de-asserting raise carrier. In the event one of the Ethernet port's ingress FIFO (serviced by Configurable MAC A) reaches this threshold, when in the pause frame generation state, further generation of Pause frames will halt or raise carrier will be de-asserted from that port. *Note: Automatic pause frame generation needs to be enabled*. *Pause frame generation state is reached once the Pause high threshold is crossed*.
	RO	31-13	0	Reserved

Addr (hex)	Mode	Bit range	Default value after reset	Description
2794	RW	12-0	1FFF	**Flow Control High Threshold CMAC B:** This register sets the high threshold in multiples of 8 bytes, for Ports 8 to 15 (serviced by Configurable MAC B), for generation of PAUSE frames or asserting raise carrier. In the event one of the Ethernet port's ingress FIFO (serviced by Configurable MAC B) reaches this threshold, a Pause frame will be sent or raise carrier will be asserted from that port. *Note: Automatic pause frame generation needs to be enabled*.
	RO	31-13	0	Reserved
2798	RW	12-0	1FFF	**Flow Control Low Threshold CMAC B:** This register sets the low threshold in multiples of 8 bytes, for Ports 8 to 15 (serviced by Configurable MAC B), to stop generation of PAUSE frames or de-asserting raise carrier. In the event one of the Ethernet port's ingress FIFO (serviced by Configurable MAC B) reaches this threshold, when in the pause frame generation state, further generation of Pause frames will halt or raise carrier will be de-asserted from that port. *Note: Automatic pause frame generation needs to be enabled*. *Pause frame generation state is reached once the Pause high threshold is crossed*.
	RO	31-13	0	Reserved
27AC	RW	15-0	FFFF	**Pause Frame Regeneration Timer CMAC A:** This register sets the Pause frame regeneration time in Pause Quanta (1 Pause Quanta = 512 bit times) for ports 0 to 7, (serviced by Configurable MAC A). The Pause Frame Regeneration time sets the time between consecutive Pause frames from an ethernet port, while the port is in the Pause Generation state. *Note: Pause frame generation state is reached once the Pause high threshold is crossed and the Pause low threshold is not reached.*
	RO	31-16	0	Reserved
27B0	RW	15-0	FFFF	**Pause Frame Regeneration Timer CMAC B:** This register sets the Pause frame regeneration time in Pause Quanta (1 Pause Quanta = 512 bit times) for ports 8 to 15, (serviced by Configurable MAC B). The Pause Frame Regeneration time sets the time between consecutive Pause frames from an ethernet port, while the port is in the Pause Generation state. *Note: Pause frame generation state is reached once the Pause high threshold is crossed and the Pause low threshold is not reached.*
	RO	31-16	0	Reserved
27BC	RW	31-0	FFFFFFFF	**Ingress FIFO Full Interrupt Mask Per Port:** FIFO full interrupt mask for the 16 Ingress FIFOs (one per port). When 0, disables the mask and an interrupt will be generated when the appropriate FIFO becomes full. The interrupt is cleared by reading the status register **Ingress FIFO Full Status**. If this bit is 1, no interrupt will be generated.

Addr (hex)	Mode	Bit range	Default value after reset	Description
27C0	RW	31-0	FFFFFFFF	**Ingress FIFO Near Full Interrupt Mask Per Port:** FIFO Near full interrupt mask for the 16 Ingress FIFOs (one per port). When 0, disables the mask and an interrupt will be generated when the appropriate FIFO becomes Near full. The interrupt is cleared by reading the status register **Ingress FIFO Near Full Status**. If this bit is 1, no interrupt will be generated. A Port will go into a near full condition when its Ingress FIFO level goes beyond the Pause Frame High Threshold value associated with the port.
27C4	RW	31-0	FFFFFFFF	**Ingress FIFO PHY/Port Enable Per Port:** Ingress FIFO/Port Enable bits for the 16 Ingress FIFOs (one per port).

Port Ethernet Status and Configuration Register Map

Address Offset	31							24	23						16	15							8	7							0
0x00	MAC Configuration #1																														
0x04	MAC Configuration #2																														
0x08	IPG / IFG																														
0x0C	Reserved								Half-Duplex																						
0x10	Reserved															Maximum Frame Length															
0x14	Reserved																														
0x18	Reserved																														
0x1C	Reserved																													Test Register	
0x20	Reserved																														
0x24	Reserved																														
0x28	Reserved																														
0x2C	Reserved																														
0x30	Reserved																														
0x34	Reserved																														
0x38	SMII Control								Reserved																						
0x3C	Reserved																								SMII Status					Reserved	
0x40	Source Address 1-4																														
0x44	Source Address 5-6																Reserved														
....	Reserved																														
0x80	CFEP																CFPT														
0x84	LocCtrl1																LocCtrl2														
0x88	Reserved								IrqMask								Reserved								IrqStatus					Reserved	
0x8C	Reserved																													GMII/ SMII	

The following table is the Ethernet Configuration and Status Register description for Port 0 (as identified by the register address). The Ethernet Configuration and Status Register description for Ports 1 to 15 are identical to Port 0. Port 1 registers start at 0x4100, Port 2 registers start at 0x4200, and so on. Port 15 registers start at 0x4F00 per the "Envoy-CE2 Register Memory Map" on page 73.

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
				Port 0 MAC Configuration and Status Registers.
4000	RW			**Port 0 Configuration Register #1**
		0	0	**Transmit Enable:** 0 - Transmission of frames is prevented 1 - The port is allowed to transmit frames to the system
	RO	1		**Synchronized Transmit Enable:** 1 - Transmit Enable is synchronized to the transmit stream
	RW	2	0	**Receive Enable:** 0 - Reception of frames is prevented 1 - The port is allowed to receive frames from the PHY
	RO	3		**Synchronized Receive Enable:** 1 - Receive Enable is synchronized to the receive stream.
	RW	4	0	**Transmit Pause Frame Generation Enable:** 0 - Prevents the transmit port MAC Control from sending Flow Control frames 1 - Allows the transmit port MAC Control to send PAUSE Control frames when requested by the system
		5	0	**Receive Pause Frame Processing Enable:** Setting this bit will cause the Receive port MAC Control to detect and act on PAUSE Control frames. Clearing this bit causes the Receive port MAC Control to ignore PAUSE Flow Control frames.
	RO	7-6	0	Reserved
	RW	8	0	**Loopback Mode:** 0 - Results in normal operation 1 - The port will "Loopback" all data received from the Egress FIFO controller to the Ingress FIFO controller, i.e. Data from the SPI-3 is looped back at the Ethernet interface
	RO	15-9		Reserved
	RW	16	0	**Reset Tx Function:** 1 - The Transmit Function block is placed in reset. This block performs the frame transmission protocol.

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4000 (cont.)	RW	17	0	**Reset Rx Function:** 1 - The Receive Function block is placed in reset. This block performs the receive frame protocol.
		18	0	**Reset Tx MAC Control:** 1 - The Transmit port MAC Control block is placed in reset. This block multiplexes data and Control frame transfers. It also responds to XOFF PAUSE Control frames.
		19	0	**Reset Rx MAC Control:** 1 - The Receive port MAC Control block is placed in reset. This block detects Control frames and contains the pause timers.
	RO	29-20	0	Reserved
	RW	30	0	**Simulation Reset:** 1 - This bit will reset those registers, such as the random back-off timer, which are not controlled by normal resets (for simulation only).
		31	1	**Soft Reset:** Setting this bit will put all modules within the MAC in reset, except the Host Interface. The Host Interface is reset via Lead Hardware reset (RESET). Soft Reset should be performed in the absence of traffic.
4004	RW			**Port 0 Configuration Register #2**
		0	0	**Full-duplex:** 0 - The port will operate in Half-Duplex mode 1 - The port will operate in Full-Duplex mode
		1	0	**CRC Enable:** 0 - Frames presented to the port MAC must have a valid length and contain a valid CRC 1 - The port will append a CRC on all frames If the configuration bit PAD/CRC Enable is set, CRC Enable is ignored. **Note:** Used for frames transmitted from the Ethernet (Egress) ports only
		2	0	**PAD / CRC Enable:** 0 - Frames presented to the port's MAC must have a valid length and contain a CRC 1 - The port will pad all short frames and append a CRC to every frame whether or not padding was required **Note:** Used for frames transmitted from the Ethernet (Egress) ports only
	RO	3		Reserved
	RW	4	0	**Length Field Checking:** 0 - No length field checking is performed 1 - The port will check if the frame length field matches the actual data field length

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4004 (cont.)	RW	5	0	**Huge Frame Enable:** 0 - The port will limit the length of frames to the Maximum Frame Length value 1 - Allows frames longer than the Maximum Frame Length to be transmitted and received
	RO	7-6		Reserved
	RW	9-8	0	**Interface Mode:** This field determines the type of interface the port is connected to. These 2-bits **must** be set to "01" for SMII, "10" for GMII and "01" for MII interface. **Note**: This is in addition to the Port Configuration Pins (**CFGCMACA[1:0]** and **CFGCMACB[1:0]**). Ports 0 and 8 are the only ports that can be configured as GMII or MII ports.
	RO	11-10		Reserved
	RW	15-12	0x7	**Preamble Length:** This field determines the length of the preamble field of the frame, in bytes.
	RO	31-16		Reserved
4008	RW			**IPG/IFG SETTINGS**
		6-0	0x60	**Back-to-Back Inter-Packet-Gap:** This is a programmable field representing the IPG between Back-to-Back Frames. This is the IPG parameter used exclusively in Full-Duplex and Half-Duplex modes when two transmit frames are sent back-to-back. Set this field to the number of bits of IPG desired. The default value is 0x60 (96d).
	RO	7		Reserved

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4008 (cont.)	RW	15-8	0x50	**Minimum IFG Enforcement:** This is a programmable field representing the minimum number of bits of IFG to enforce between frames. A frame whose IFG is less than that programmed is dropped or errored. The default value of 0x50 (80d) represents half of the nominal minimum IFG which is 160-bits. IFG = IPG + Preamble + SFD If the IFIFO is configured for Store and Forward mode, the frame will be dropped and will not appear on the SPI port. If the IFIFO is configured for Streaming mode, the frame will appear on the SPI port with 4 additional bad CRC bytes prepended to it. When a port is configured in SMII mode, the allowed range of this register is a minimum of 0x4 (four) up to a maximum of 0xFF. In addition, the lower 2 bits should be masked out since the granularity of this interface is nibble based. (e.g., programming a value of 0x83 (or 0x81, 0x82) is functionally equivalent to 0x80. A packet with an IFG of 0x80 will pass through the device even though its value is less than 0x83 due to the nibble granularity in SMII mode). When a port is configured in GMII mode, the allowed range of this register is a minimum of 0x8 (eight) up to a maximum of 0xFF. In addition, the lower 3 bits should be masked out since the granularity of this interface is byte based. (e.g., programming a value of 0x87 (or 0x81, 0x82...0x86) is functionally equivalent to 0x80. A packet with an IFG of 0x80 will pass through the device even though its value is less than 0x87 due to the byte granularity in GMII mode).
		22-16	0x60	**Non-Back-to-Back Inter-Packet-Gap Part 2 (IPG2):** This is a programmable field representing the Non-Back-to-Back Inter-Packet-Gap in bits. Default value is 0x60 (96d). **Note:** For an IPG length of 96 and a 2/3 ratio, the values 0x20 and 0x7C are required in the IPG1 and IPG2 locations, respectively.
	RO	23		Reserved
	RW	30-24	0x40	**Non-Back-to-Back Inter-Packet-Gap Part 1 (IPG1):** This is a programmable field representing the optional Carrier Sense window referenced in IEEE 802.3/4.2.3.2.1 'Carrier Deference'. If carrier is detected during the timing of IPG1, the MAC defers to carrier. However, if carrier becomes active after IPG1, the MAC continues timing IPG2 and transmits, knowingly causing a collision, thus ensuring fair access to the medium. Its range of values is 0x0 to IPG2. Default value is 0x40 (64d) which follows the two-thirds/one-third guideline. **Note:** For an IPG length of 96 and a 2/3 ratio, the values 0x20 and 0x7C are required in the IPG1 and IPG2 locations, respectively.
	RO	31		Reserved

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
400C	RW			**HALF-DUPLEX REGISTER**
		9-0	0x37	**Collision Window:** This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD are included. Its default value of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.
	RO	11-10		Reserved
	RW	15-12	0xF	**Retransmission Maximum:** This is a programmable field specifying the number of retransmission attempts following a collision before aborting the frame due to excessive collisions. The Standard specifies the attempt limit to be 0xF (15d).
		16	1	**Excessive Defer:** 0 - Causes the Tx MAC to allow transmission of a packet that has been excessively deferred 1 - Configures the Tx MAC to abort transmission of a packet that has been excessively deferred
		17	0	**No Backoff:** 0 - Causes the Tx MAC to follow the binary exponential backoff rule 1 - Configures the Tx MAC to immediately re-transmit following a collision
		18	0	**Backpressure No Backoff:** 0 - Causes the Tx MAC to follow the binary exponential backoff rule 1 - Configures the Tx MAC to immediately re-transmit, following a collision, during backpressure
	RW	19	0	**Alternate Binary Exponential Backoff Enable:** 0 - Causes the Tx MAC to follow the standard binary exponential backoff rule 1 - Configures the Tx MAC to use the Alternate Binary Exponential Backoff Truncation setting instead of the IEEE 802.3 standard tenth collision. The Standard specifies that any collision after the tenth uses “210 - 1” as the maximum backoff time
		23-20	0xA	**Alternate Binary Exponential Backoff Truncation:** This field is used when Alternate Binary Exponential Backoff Enable is set. The value programmed is substituted for the Ethernet standard value of ten.
	RO	31-24		Reserved

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4010	RW			**MAXIMUM FRAME LENGTH REGISTER**
		15-0	0x0600	**Maximum Frame Length:** This field resets to 0x0600 (1536d), which represents the maximum frame size in both the transmit and receive directions.
	RO	31-16		Reserved
4014 to 4018	RO	31-0	0	Reserved
401C	RW			**TEST REGISTER**
		0	0	**Shortcut Slot Time:** This bit allows the slot time counter to expire regardless of the current count. This bit is for testing purposes only.
		1	0	**Test Pause:** For testing purposes only. 1 - Allows the MAC to be paused via the host interface
		2	0	**Registered Transmit Flow Enable:** Register Transmit Half-Duplex Flow Enable, active high assertion.
		3	0	**Maximum Backoff:** 1 - The MAC is configured to backoff for the maximum possible length of time. This test bit is used to predict backoff times in Half-Duplex mode.
	RO	31-4		Reserved
4020 to 4034	RO	31-0	0	Reserved
4038	RO			**SMII CONTROL REGISTER**
		23-0	0	Reserved
	RW	24	1	**SMII PHY Mode:** 0 - Allows MAC-to-MAC connections 1 - Allows MAC-to-PHY connections where Envoy-CE2 connects to a PHY
	RO	30-25	0	Reserved
	RW	31	0	**Reset SMII Port:** This resets the port if it is configured as an SMII port.

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
403C	RO			**SMII STATUS REGISTER**
		3-0	0	Reserved
		4	0	**Speed:** 0 - The Serial MII PHY is operating at 10 Mbit/s mode 1 - The Serial MII PHY is operating at 100 Mbit/s mode
		5	0	**Full Duplex:** 0 - The Serial MII PHY is operating in Half-Duplex mode 1 - The Serial MII PHY is operating in Full-Duplex mode
		6	0	**Link OK:** 0 - The Serial MII PHY has not detected a valid link 1 - The Serial MII PHY has detected a valid link
		7	0	**Jabber:** 1 - The Serial MII PHY has detected a Jabber condition 0 - The Serial MII PHY has not detected a Jabber condition. This bit latches high.
		8	0	**Clash:** 0 - The Serial MII module is either in PHY mode or in MAC-to-MAC mode. 1 - The Serial MII module is in MAC-to-MAC mode with the partner in 10 Mbit/s and/or Half-Duplex mode indicative of a configuration error.
	RC	9	0	**Excess Defer:** This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high.
	RO	31-10	0	Reserved
4040	RW			**SOURCE ADDRESS REGISTER, PART 1**
		7-0	0	**SOURCE ADDRESS, 4th Octet**: This field holds the fourth octet of the source address. The fourth octet is stored in 7:0 and defaults to '0x00'.
		15-8	0	**SOURCE ADDRESS, 3rd Octet:** This field holds the third octet of the source address. The third octet is stored in 15:8 and defaults to '0x00'.
		23-16	0	**SOURCE ADDRESS, 2nd Octet:** This field holds the second octet of the source address. The second octet is stored in 23:16 and defaults to '0x00'.
		31-24	0	**SOURCE ADDRESS, 1st Octet:** This field holds the first octet of the source address. The first octet is stored in 31:24 and defaults to '0x00'.

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4044	RO	**SOURCE ADDRESS REGISTER, PART 2**		
		15-0		Reserved
	RW	23-16	0	**SOURCE ADDRESS, 6th octet:** This field holds the sixth octet of the source address. The sixth octet is stored in 23:16 and defaults to '0x00'. This Byte is the first Address byte transmitted.
		31-24	0	**SOURCE ADDRESS, 5th octet:** This field holds the fifth octet of the source address. The fifth octet is stored in 31:24 and defaults to '0x00'.
4048 to 407C	RO	31-0		Reserved
4080	RW	15-0	0	**CFPT:** Control Frame parameter to set the Pause Time parameter. 16-bit field containing the Pause Time value.
		31-16	0	**CFEP:** Control Frame Extended Parameter. This extended parameter may contain additional information such as VLAN and/or priority information per IEEE 802.1p.

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4084	RW	0	0	**Rx Prepend Packet:** Prepend receive packets with 2 dummy bytes (0X00000000) prior to sending to the SPI-3 output interface.
		1	0	**Tx Prepend Strip:** Strip out Prepend bytes received from the SPI-3 input interface.
		2	0	**Tx Pause Frame Filter:** When set, will enable filtering of Egress Pause Frames from the SPI interface. Pause frames whose EtherType = 8808h and OpCode = 0001h will be errored by forcing the MAC to append an incorrect CRC. **Note**: The RMON statistics counters will count the number of filtered pause frames. The statistics counters will also count each filtered pause frame as a Tx Fragment.
	RO	15-3		Reserved
	RW	16	0	**Host Initiated Flow Control Enable:** Once enabled, a Pause Control Frame is transmitted, when the Pause Regeneration Timer reaches '0'. The timer will reactivate after it reaches '0'. When exiting this mode, a null Pause Frame is sent. 0 - Disable 1 - Enable **Note:** Raise carrier flow mechanism can not be host initiated.
		17	0	**Automatic Flow Control Enable:** In this mode, when the ingress FIFO associated with this port reaches flow control high threshold, the flow control mechanism is activated. For full duplex, Pause Control Frames are used and for half duplex mode, raise carrier method is used. 0 - Disable 1 - Enable **Note:** Set **Flow Control Mode (Bit 30)** to Raise Carrier or PAUSE frame depending whether the Port is in half duplex or full duplex.
		18	0	**STEN:** Statistics Enable. 0 - Disables internal statistics counters update 1 - Enables internal statistics counters to update
	RO	20-19	0	Reserved
	RW	21	0	**Tx Source Address Substitute Enable:** Transmitter Source Address Substitution Enable. 1 - Substitute the outgoing source address field in the Ethernet header with the programmed source address in the MAC (Addresses 0x4040 and 0x4044).

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4084 (cont.)	RW	22	0	**Rx CRC Remove:** Configures the removal of the CRC (FCS) bytes from the Ethernet frame received at the Rx interface destined for the SPI-3 output interface. 1 - Remove CRC
		23	0	**GTx Clock Select:** The Rx clock is used when connecting the Envoy-CE2 to another MAC in a MAC-to-MAC configuration. 0 - Tx clock 1 - Rx clock For normal operation, this bit should set to 0.
		24	0	**Discard Rx Truncated frames:** 0 - Do not discard the frame if it is truncated 1 - Discard the frame if it is truncated If the IFIFO is configured for Store and Forward mode, the frame will be dropped and will not appear on the SPI port. If the IFIFO is configured for Streaming mode, the frame will appear on the SPI port with 4 additional bad CRC bytes prepended to it.
		25	0	**DISC Rx Length Field Mismatch:** Discard unmatched length field. 0 - Do not discard the frame if the frame length field does not match the actual data length field 1 - Discard the frame if the frame length field does not match the actual data length field If the IFIFO is configured for Store and Forward mode, the frame will be dropped and will not appear on the SPI port. If the IFIFO is configured for Streaming mode, the frame will appear on the SPI port with 4 additional bad CRC bytes prepended to it.
		26	0	**DISC Rx CRC Field Mismatch:** Discard frames with CRC error. 0 - Do not discard the frame if it has a CRC error 1 - Discard the frame if it has a CRC error If the IFIFO is configured for Store and Forward mode, the frame will be dropped and will not appear on the SPI port. If the IFIFO is configured for Streaming mode, the frame will appear on the SPI port with 4 additional bad CRC bytes prepended to it.
		27	0	**DISC Rx ERR:** Discard received frame with Rx error. 0 - Do not discard the frame if it has an Rx error 1 - Discard the frame if it has an Rx error If the IFIFO is configured for Store and Forward mode, the frame will be dropped and will not appear on the SPI port. If the IFIFO is configured for Streaming mode, the frame will appear on the SPI port with 4 additional bad CRC bytes prepended to it.

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
		28	0	**Rx PAUSE Frame Filter:** Active high signal to filter out PAUSE frames if the Destination Address (DA) field matches the Source Address (SA) field in addresses 0x4040 and 0x4044 or if the DA is a Multicast address.
		29	0	**Rx SA Filter ENB:** Receive Source Address Filter enable. 0 - No filtering is performed 1 - Frames will be filtered out if the Destination Address (DA) field does not match the programmed Source Address (SA) field in addresses 0x4040 and 0x4044
		30	0	**Flow Control Mode:** Configures the flow control mode. 0 - Raise Carrier Mode 1 - Pause Frames
		31	0	**Half-Duplex Flow Control Duration:** Configures the Half Duplex flow control duration. 0 - Raise Carrier stopped after 128K byte times 1 - Continuous Raise Carrier flow control till congestion is relieved

Port 0 Ethernet Status and Configuration Register Description

Addr (hex)	Mode	Bit Range	Default value after reset	Description
4088	RO	2-0		Reserved
		3	0	**PAUSE Frame Received:** Status indication that an error free, unicast, or multicast PAUSE frame has been received.
		4	0	**Rx Frame Discarded:** Status indication of a frame discard due to lack of FIFO memory resource (overflow). **Note:** A counter for this register is described in the statistics section.
		5	0	**Tx Frame Discarded:** Status indication that an Under-run occurred in the Ethernet transmit direction. **Note:** In Streaming mode, when the port's Egress FIFO goes empty during frame transmission, an under-run occurs.
		6	0	**Tx Abort Frame:** Status indication that a frame has been transmitted with the error pin asserted.
		7	0	**Tx Tag Error Status:** Transmit Byte Buffer detected tag error in data from the Egress FIFO. For example, two start of packet tags without an end of packet tag between them would be an error. Tag errors are counted in the Tx Abort Counter.
		15-8	0	Reserved
		18-16	1	Reserved
	RW	19	1	**PAUSE Frame Received Interrupt Mask:** Interrupt Mask for **PAUSE Frame Received** Status based interrupt. 0 = Mask Disabled, 1 = Mask Enabled.
		20	1	**Rx Frame Discarded Interrupt Mask:** Interrupt Mask for **Rx Frame Discarded** Status based interrupt. 0 = Mask Disabled, 1 = Mask Enabled.
		21	1	**Tx Frame Discarded Interrupt Mask:** Interrupt Mask for **Tx Frame Discarded** Status based interrupt. 0 = Mask Disabled, 1 = Mask Enabled.
		22	1	**Tx Abort Frame Interrupt Mask:** Interrupt Mask for **Tx Abort Frame** Status based interrupt. 0 = Mask Disabled, 1 = Mask Enabled.
		23	1	**Tx Tag Error Mask:** Interrupt Mask for **Tx Tag Error** Status based interrupt. 0 = Mask Disabled, 1 = Mask Enabled.
	RO	31-24	0	Reserved
408C	RO	0	0	Reserved
		1	Depends on CMAC Configuration pins	**GMII/SMII Mode Status:** 0 - SMII Mode 1 - GMII Mode Only Ports 0 and 8 can be configured for GMII operation via external configuration pins. The other ports will always be in SMII mode.
		31-2	0	Reserved

The following table is the Ethernet Statistics Register description for Port 0 (as identified by the register address). The Ethernet Statistics Register description for the other ports are identical to that of Port 0. Port 1 registers start at 0x6100, Port 2 registers start at 0x6200 and so on. Port 15 registers start at 0x6F00 per the "Envoy-CE2 Register Memory Map" on page 73. Upon reset, the following counters are clear on read saturating counters. To change to rollover counters, set **RMON STATISTIC COUNTER AUTO CLEAR ON READ** to 0.

Ethernet Statistics Register Description for Port 0

Addr (hex)	Mode	Bit Range	Default value after reset	Description
6000	RC	31-0	0	**Rx Bytes Lo (Octets)**: The total number of octets of data (including those in bad packets) received on the network (excluding framing bits but including FCS octets). Note: The upper 8 bits of this 40-bit counter are accessed via Rx Byte Hi (Register 0x60C0). **Note:** If Received Byte Counter Config bit = 0 (Register 0x0030 Bit 1), then Rx Byte Counter will only count bytes from good packets.
6004	RC	31-0	0	**Rx Packets:** The total number of packets (including bad packets, broadcast packets, and multicast packets) received.
6008	RC	31-0	0	**Rx Undersize Packets:** The total number of packets received that were less than 64 octets in length (excluding framing bits, but including FCS octets), had a good FCS, and were otherwise well formed. **Note:** Packets less than 64 octets but with a bad FCS are counted in the Rx Fragment Packets counter.
600C	RC	31-0	0	**Rx 64 Octets Packets:** The total number of packets (including bad packets) received that were 64 octets in length (excluding framing bits but including FCS octets).
6010	RC	31-0	0	**Rx 65 to 127 Octet Packets:** The total number of packets (including bad packets) received that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets).
6014	RC	31-0	0	**Rx 128 to 255 Octet Packets:** The total number of packets (including bad packets) received that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets).
6018	RC	31-0	0	**Rx 256 to 511 Octet Packets:** The total number of packets (including bad packets) received that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets).
601C	RC	31-0	0	**Rx 512 to 1023 Octet Packets:** The total number of packets (including bad packets) received that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets).

Addr (hex)	Mode	Bit Range	Default value after reset	Description
6020	RC	31-0	0	**Rx 1024 to 1518 Octet Packets:** The total number of packets (including bad packets) received that were between 1024 and 1518 octets (1522 for VLAN tagged packets) in length inclusive (excluding framing bits but including FCS octets).
6024	RC	31-0	0	**Rx Frame Length Errored Packets:** The total number of good packets received in which the IEEE 802.3 length field did not match the number of data bytes actually received (46-1500 bytes). The counter is not incremented if the length field is not a valid IEEE 802.3 length, e.g., an EtherType value.
6028	RC	31-0	0	**Rx Oversize Packets:** The total number of packets received that were longer than 1518 octets (1522 for VLAN tagged packets), had a good FCS, and were otherwise well formed. **Note:** Packets longer than MAX octets are truncated by the MAC and will therefore have an incorrect FCS; These packets will be counted in the Rx Jabber Packets counter. MAX octets value is the “Maximum Frame Length” value programmed in the MAC.
602C	RC	31-0	0	**Rx Broadcast Packets:** The total number of good packets received that were directed to the broadcast address. **Note:** This does not include multicast packets.
6030	RC	31-0	0	**Rx Multicast Packets:** The total number of good packets received that were directed to a multicast address. **Note:** This does not include packets directed to the broadcast address or packets with the Control Frame multicast address.
6034	RC	31-0	0	**Rx Pause Control Frame Packets:** The total number of good packets received that are Pause Control Frames.
6038	RC	31-0	0	**Rx Unknown Opcode Control Frame Packets:** The total number of good packets received that are Control Frame packets but whose opcode is other than the Pause opcode.
603C	RC	31-0	0	**Rx VLAN Tagged Packets:** The total number of good packets received that are VLAN tagged (Type/Len Field = 0x8100).
6040	RC	31-0	0	**Rx Fragment Packets:** The total number of packets received that were less than 64 octets in length (excluding framing bits but including FCS octets) and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).

Addr (hex)	Mode	Bit Range	Default value after reset	Description
6044	RC	31-0	0	**Rx FCS Errored Packets:** The total number of packets received that had a length (excluding framing bits, but including FCS octets) between 64 and 1518 octets (1522 for VLAN tagged packets), inclusive, but had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).
6048	RC	31-0	0	**Rx Jabber Packets:** The total number of packets received that were longer than 1518 octets (1522 for VLAN tagged packets) (excluding framing bits, but including FCS octets), and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).
604C	RC	31-0	0	**Rx Code Error Counter:** The total number of packets received that the PHY asserted RX_ER during reception.
6050	RC	31-0	0	**Rx Ingress FIFO Full Drop Counter:** The total number of good or bad packets received which were dropped due to Ingress FIFO full condition, i.e., lack of system resources.
6054	RC	31-0	0	**Rx Unicast SA Mismatch Drop Counter:** The total number of good packets received which were dropped because they had a unicast address which did not match the source address and which are not Pause or Control Frames. **Note:** This counter will not be incremented if the packet is also dropped due to FIFO Full condition.
6058	RC	31-0	0	**Tx Bytes Lo (Octets):** The total number of octets of data transmitted on the network (excluding framing bits/SFD or jam octets but including FCS octets). This count does NOT include collided octets from collided transmission attempts. Note: The upper 8 bits of this 40-bit counter are accessed via Tx Bytes Hi (Register 0x60C4).
605C	RC	31-0	0	**Tx Packets:** The total number of packets transmitted successfully.
6060	RC	31-0	0	**Tx Undersize Packets:** The total number of packets transmitted successfully that were less than 64 octets in length (excluding framing bits, but including FCS octets), had a good FCS, and were otherwise well formed. **Note:** Packets less than 64 octets but with a bad FCS are counted in the Tx Fragment Packets counter.
6064	RC	31-0	0	**Tx 64 Octet Packets:** The total number of packets (including bad packets) transmitted successfully that were 64 octets in length (excluding framing bits but including FCS octets).

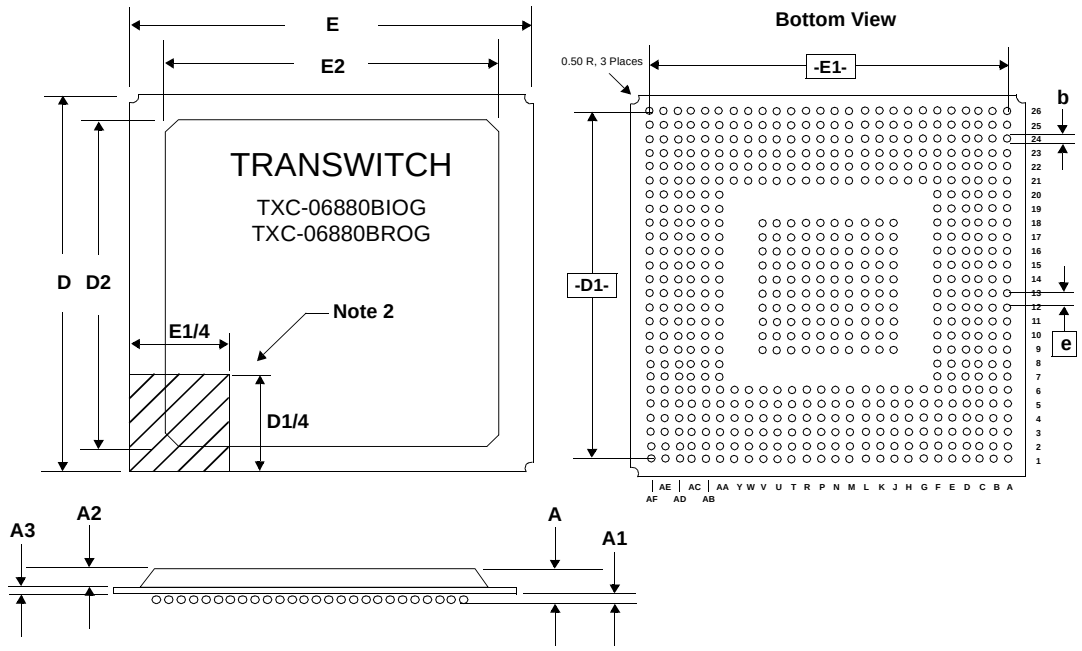
Addr (hex)	Mode	Bit Range	Default value after reset	Description
6068	RC	31-0	0	**Tx 65 to 127 Octet Packets:** The total number of packets (including bad packets) transmitted successfully that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets).
606C	RC	31-0	0	**Tx 128 to 255 Octet Packets:** The total number of packets (including bad packets) transmitted successfully that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets).
6070	RC	31-0	0	**Tx 256 to 511 Octet Packets:** The total number of packets (including bad packets) transmitted successfully that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets).
6074	RC	31-0	0	**Tx 512 to 1023 Octet Packets:** The total number of packets (including bad packets) transmitted successfully that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets).
6078	RC	31-0	0	**Tx 1024 to 1518 Octet Packets:** The total number of packets (including bad packets) transmitted successfully that were between 1024 and 1518 octets (1522 for VLAN tagged packets) in length inclusive (excluding framing bits but including FCS octets).
607C	RC	31-0	0	**Tx Pause Frames Discarded:** Count of transmit Pause Frames originated via the SPI-3 interface which are discarded (incorrect CRC appended).
6080	RC	31-0	0	**Tx Oversize Packets:** The total number of packets transmitted successfully that were longer than 1518 (1522 for VLAN tagged packets) octets (excluding framing bits, but including FCS octets), had a good FCS, and were otherwise well formed. **Note:** Packets longer than MAX octets are truncated by the MAC and will have an incorrect FCS appended; These packets will be counted in the Tx Jabber Packets counter. MAX octets value is the “Maximum Frame Length” value programmed in the MAC.
6084	RC	31-0	0	**Tx Broadcast Packets:** The total number of good packets transmitted that were directed to the broadcast address. **Note:** This does not include multicast packets.
6088	RC	31-0	0	**Tx Multicast Packets:** The total number of good packets transmitted that were directed to a multicast address. **Note:** This does not include packets directed to the broadcast address or packets with the Control Frame multicast address.

Addr (hex)	Mode	Bit Range	Default value after reset	Description
608C	RC	31-0	0	**Tx PAUSE Frame Packets:** The total number of good packets transmitted that are Pause Control Frames. Only Pause Control Frames which originated within the MAC are counted. Those that originated via the SPI-3 interface are not counted.
6090	RC	31-0	0	**Tx VLAN Tagged Packets:** The total number of good packets transmitted that are VLAN tagged (Type/Len Field = 0x8100)
6094	RC	31-0	0	**Tx Deferral:** A count of successfully transmitted packets for which the first transmission attempt was deferred because the medium was busy. The count does not include packets involved in collisions.
6098	RC	31-0	0	**Tx Excess Deferral:** A count of packets not transmitted because they were deferred for an excessive period of time (3036 byte times).
609C	RC	31-0	0	**Tx Single Collision:** A count of successfully transmitted packets for which transmission is inhibited by exactly one collision.
60A0	RC	31-0	0	**Tx Multiple Collision:** A count of successfully transmitted packets for which transmission is inhibited by more than one collision.
60A4	RC	31-0	0	**Tx Late Collision:** A count of packets transmitted which experience a late collision. A “late collision” is a collision detected more than 512 bit-times into the transmission of a packet. **Note:** Packet transmission can be continued or aborted by configuring the Excessive Defer bit in the MAC’s Half-Duplex control register (Register 0x400C Bit 16).
60A8	RC	31-0	0	**Tx Excessive Collision:** A count of packets not transmitted due to excessive collisions.
60AC	RC	31-0	0	**Tx Fragment Packets:** The total number of packets transmitted that were less than 64 octets in length (excluding framing bits but including FCS octets) and had a bad Frame Check Sequence (FCS).
60B0	RC	31-0	0	**Tx FCS Errored Packets:** The total number of packets transmitted that had a length (excluding framing bits, but including FCS octets) of between 64 and 1518 octets (1522 for VLAN tagged packets), inclusive, but had a bad Frame Check Sequence (FCS).
60B4	RC	31-0	0	**Tx Jabber Packets:** The total number of packets transmitted that were longer than 1518 (1522 for VLAN tagged packets) octets (excluding framing bits, but including FCS octets), and had a bad Frame Check Sequence (FCS). This count will include packets truncated by the MAC because they were longer than MAX octets. MAX octets value is the “Maximum Frame Length” value programmed in the MAC.

Addr (hex)	Mode	Bit Range	Default value after reset	Description
60B8	RC	31-0	0	**Tx Drop Frame:** The total number of transmitted packets which were aborted due to an under-run of the Egress FIFO, i.e., lack of system resources. When this is detected, the MAC transmitter will jam the packet and insert an incorrect FCS.
60BC	RC	31-0	0	**Tx Abort:** The total number of transmitted packets which were aborted under command of the Egress FIFO logic (packet TAG = ERROR). When this is detected, the MAC transmitter will jam the packet and insert an incorrect FCS. This counter is also incremented if an unexpected tag is encountered after transmission of a packet has started, i.e., another SOP is detected before we get the EOP for the current packet.
60C0	RC	7-0	0	**Rx Bytes Hi (MSByte of the Rx Byte):** 8 MSBs of the 40-bit Rx Byte Counter. When doing a 32-bit read of this counter, the counter values are in Bits 0-7.
	RO	31-8	0	Reserved
60C4	RC	7-0	0	**Tx Bytes Hi (MSByte of the Tx Byte):** 8 MSBs of the 40-bit Tx Byte Counter. When doing a 32-bit read of this counter, the counter values are in Bits 0-7.
	RO	31-8	0	Reserved

PACKAGE INFORMATION

The Envoy-CE2 device is packaged in a 27 mm × 27 mm, 580-Lead Plastic Ball Grid Array (PBGA) package with a 1.0 mm pitch, as illustrated in Figure 25.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 26 x 26, JEDEC code MO-151.

Dimension (Note 1)	Nominal	
A (Nom)	2.23	
A1	0.4	0.6
A2	1.12	1.22
A3 (Nom)	0.56	
b (Ref.)	0.63	
D	27.0	
D1 (Nom)	25.0	
D2	23.95	24.35
E	27.0	
E1 (Nom)	25.0	
E2	23.95	24.35
e (Ref.)	1.0	

Figure 25. Envoy-CE2 Package Diagram

ORDERING INFORMATION

Part Number: TXC-06880BIOG	580-lead plastic ball grid array (PBGA) package, Non-Green (Non-ROHS and non-lead free) compliant
TXC-06880BROG	580-lead plastic ball grid array (PBGA) package, Green (ROHS and lead free) compliant

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PHAST®-12P Device (STM-4/OC-12 SDH/SONET Overhead Terminator with CDB/PPP UTOPIA/POS-PHY Interface). The PHAST-12P is a highly integrated SDH/SONET overhead terminator device designed for ATM cell and PPP packet payload mappings. A single PHAST-12P can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line.

Envoy-8FE Device (Octal Fast Ethernet Controller). The Envoy-8FE Device is a Serial Media Independent Interface (SMII) to POS-PHY Level 2/3 interface converter transporting Ethernet packets. Envoy-8FE has 8 SMII ports. Packet data from the 8 ports are aggregated onto the POS-PHY interface.

Envoy-2GE Device (Dual Gigabit Ethernet Controller). The Envoy-2GE Device is a Gigabit Media Independent Interface (GMII) to POS-PHY Level 2/3 interface converter transporting Ethernet packets. Envoy-2GE has 2 GMII ports. Packet data from the 2 ports are aggregated onto the POS-PHY interface.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations..

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office
Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office
Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
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Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

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Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland
Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834
Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
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Philadelphia, PA 19111-5094
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Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
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Portland, OR 97221
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Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
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TTC (Japan):

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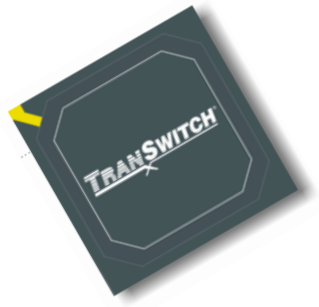

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