Intel® LXT384 Octal T1/E1/J1 Short-Haul PCM Transceiver with Jitter Attenuation (JA)

Datasheet

Product Features

- Octal T1/E1/J1 Pulse-Code Modulation (PCM) Transceiver with Jitter Attenuation for use in both 1.544 Mbps (T1) and 2.048 Mbps (E1) applications
- 16 fully-independent receiver/transmitters
- Support for E1 standards:
  - —Exceeds ETSI ETS 300 166
  - —Meets ETS 300 233
- Low-power single-rail 3.3-V CMOS power supply, with 5-V tolerant I/Os
- Jitter attenuation
  - —Crystal-less
  - —Digital clock recovery PLL
  - —Referenced to a low frequency 1.544 MHz or 2.048-MHz clock. Normal operation requires only MCLK. Does not require a reference clock frequency higher than the line frequency.
  - —Can be switched between receive and transmit path
  - —Meets ETSI CTR12/13, ITU G.736, G.742, G.823, and AT&T Pub 62411
  - —Optimized for Synchronous Optical NETwork (SONET) and Synchronous Digital Hierarchy (SDH) applications, meets ITU G.783 mapping jitter standard
  - —Constant throughput delay
- Differential receiver architecture
  - —High margin for noise interference
  - —Operates at >12 dB of cable attenuation
- Intel® Hitless Protection Switching
  - —Eliminates mechanical relays for redundancy 1+1 protection applications
  - —Increases quality of service
- Transmitters
  - —Power-down mode with fast output tristate capability
  - —Transmit waveform shaping meets ITU G.703 and T1.102 specifications
  - —Exceeds ETSI ETS 300 166 transmit return-loss specifications
  - —Low-impedance transmit drivers, independent of transmit pattern and supply-voltage variations
  - —Low-current transmit output option that can reduce power dissipation by up to 15%. By changing the LXT384 Transceiver output transformer ratio from 1:2 to 1:1.7, the savings occur whether TVCC is at 5 V or 3.3 V. 130 mW per channel (typical). See Table 63 “Intel® LXT384 Transceiver Power Consumption” on page 104 and Table 64 “Load3 Power Consumption” on page 105.
- HDB3, B8ZS, or AMI line encoder/decoder
- LOS per ITU G.775, T1.231, and ETS 300 233
- Diagnostics:
  - —Can be configured for G.722-compliant, non-intrusive performance (protected) monitoring points
  - —Industry-standard P1149.1 JTAG Boundary Scan test port
- Intel®/ Motorola* 8-bit parallel processor interface or 4 wire serial control interface
- Hardware and Software control modes
- Operating temperature -40 °C to 85 °C
- 160-ball BGA or 144-pin LQFP packages

Applications

- SONET/SDH tributary interfaces
- Digital cross connects
- Public/private switching trunk line interfaces
- Microwave transmission systems
- M13, E1-E3 MUX

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Revision History

Intel® LXT384 Transceiver - Revision 005 Revision Date: November 2005	
Page Number	**Description**
1	Revised package information
11	Changed text in Chapter 1.0, “Audience and Purpose”
135	Added RoHS package information, starting at Section 16.1, “Top Label Markings”

Intel® LXT384 Transceiver - Revision 004 Revision Date: September 2005	
Page Number	**Description**
24	Table 7 “Microprocessor-Standard Bus and Interface Signals”. Change to table text.
84	Table 45 “Pulse Shaping Data Register, PSDAT (11h) for Intel® LXT384 Transceiver”. Change to footnotes.

Intel® LXT384 Transceiver - Revision 003 Revision Date: July 2004	
Page Number	**Description**
-	Major editing/rewriting/reorganizing, based on results of extensive testing of this device, and on customer feedback about how the device is actually used.

Intel® LXT384 Transceiver - Revision 002 Revision Date: October 2003	
Page Number	**Description**
9	Revised Figure 3.
21	Table 1, Sheet 11 of 12, revised description of Pin 115.
31	Figure 6, added callout to graphic, for clarity.

Intel® LXT384 Transceiver - Revision 001 Revision Date: February 2003	
Page Number	**Description**
-	Initial release.

1.0 Introduction to this Document

1.1 Audience and Purpose

The audience for this document is design engineers.

The purpose of this document is to provide design information about the Intel® LXT384 Octal Short-Haul Pulse-Code Modulation Transceiver with Jitter Attenuation (called hereafter the LXT384 Transceiver).

The rest of this document is organized as follows:

- Chapter 2.0, “Product Summary”
- Chapter 3.0, “Pin Assignments and Package”
- Chapter 4.0, “Multi-Function Pins”
- Chapter 5.0, “Signal Descriptions”
- Chapter 6.0, “Functional Description”
- Chapter 7.0, “Operating Mode Summary”
- Chapter 8.0, “Registers”
- Chapter 9.0, “JTAG Boundary Scan”
- Chapter 10.0, “Electrical Characteristics”
- Chapter 11.0, “Timing Characteristics”
- Chapter 12.0, “Line-Interface-Unit Circuit Specifications”
- Chapter 13.0, “Mask Specifications”
- Chapter 14.0, “Jitter Performance”
- Chapter 15.0, “Recommendations and Specifications”
- Chapter 16.0, “Mechanical Specifications”
- Chapter 17.0, “Product Ordering Information”
- Chapter 18.0, “Package Information”
- Chapter 19.0, “Abbreviations and Acronyms”

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1.2 Conventions and Terminology

Balls and pins. This document discusses two packages, both a low-profile octal-flat package (an LQFP, which uses pins for signals) and a pin ball-grid array (a PBGA, which uses balls for signals). In this document the term ‘pin’ refers to either a ball or a pin.

Mark. An analog AMI (Alternate Mark Inversion) line-interface signal, containing a digital logic 1. The mark is either a negative or a positive pulse.

Recovered Clock. A clock that is not generated, but is instead derived from received data on a transceiver. The RTIP/RRING received signal is used to generate RCLK on the transceiver.

X = Don’t care.

1.3 Related Documents

Table 1 lists related documents for both the Intel® LXT385 Transceiver and the Intel® LXT384 Transceiver.

- Use the Intel® LXT384 Transceiver for either E1 or T1 applications.
- The Intel® LXT385 Transceiver supports the E1 standard only.

Table 1. Related Documents

1+1 Protection without Relays Using Intel® LXT380/1/4/6/8 Hitless Protection Switching - Application Note	249464
Intel® LXD384 - Evaluation Board for Octal T1/E1 Applications - Developer Manual	249214
Intel® LXT380/1/4/6/8 Redundancy Applications - Application Note	249134
Intel® LXT380/4 Octal T1/E1 LIUs - Interfacing with the Transwitch Octal Framers - Application Note	249136
Intel® LXT384 Octal LIU and Intel® LXT385 Octal PCM Transceiver. - Solutions for Slow Power-Up Rise Time - Application Note	253721
Intel® LXT384/6/8 Frequently Asked Questions	249183
Intel® LXT384/6/8 Twisted Pair Interface - Without Component Changes - Application Note	249138
Intel® LXT384/6/8 Universal 75/100/120 Ohm Interface	251364
T1/E1/J1, N+1 Redundancy with Analog Switches and Intel® LXT3x Line Interface Units - Preliminary Application Note	278832
Transformer Specification for Intel® Transceiver Applications - Application Note	249133

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2.0 Product Summary

The Intel® LXT384 Octal T1/E1/J1 Short-Haul Pulse-Code Modulation Transceiver with Jitter Attenuation (called hereafter the LXT384 transceiver) is designed for use in 1.544 MBps (T1) or 2.048-Mbps (E1) applications. It incorporates eight independent receivers and eight independent transmitters in either a single 144-pin LQFP or a 160-ball PBGA package.

Transmitters. The LXT384 transceiver transmits shaped waveforms that meet ITU G.703 specifications. The transmit drivers provide low impedance, independent of supply-voltage variation and transmit patterns. The output of the transmitters is stable over a variety of loads. The transmit return loss for the LXT384 transceiver exceeds typical specifications such as ETSI ETS 300 166. All transmitters have a power-down mode with the capability for a fast transition to an output high-impedance tristate.

Power Savings. The Intel® transmit output design allows you to use the transmitter output of the LXT384 Transceiver in a broad range of applications, while maintaining circuit stability. As a result, the LXT384 Transceiver can offer a low-current transmit output option that can reduce power dissipation by up to 15%. By changing the LXT384 Transceiver output transformer ratio from 1:2 to 1:1.7, the savings occur whether TVCC is at 5V or 3.3V.

Receivers. The LXT384 Transceiver has a differential receiver architecture that provides a high noise-interference margin so that the receivers can operate well beyond 12 dB of cable attenuation.

Jitter Attenuation. The LXT384 Transceiver incorporates a crystal-less jitter attenuator that can be switched to work inside either the receive or the transmit path, or it can be disabled entirely. The jitter-attenuation performance, optimized for synchronous digital hierarchy (SDH) applications, meets typical international specifications such as ETSI CTR12/13.

Performance Monitoring. You can configure the LXT384 Transceiver for non-intrusive performance monitoring (also known as ‘protected monitoring’) that is compliant with ITU G.772.

Intel® Hitless Protection Switching. The LXT384 Transceiver can operate in an Intel® Hitless Protection Switching mode, which uses one transceiver to back up another, in case the primary transceiver fails. This method is often referred to as 1+1 redundancy protection. Typical redundancy methods used external relays. Intel® Hitless Protection Switching is a solid-state solution, which reduces bit errors that can occur when using external relays for redundancy protection. This mode uses two LXT384 Transceivers in parallel, with one LXT384 Transceiver powered on, while the other LXT384 Transceiver is in standby mode. As a result, one LXT384 Transceiver backs up another LXT384 Transceiver. See the *1+1 Protection without Relays Using Intel® LXT380/1/4/6/8 Hitless Protection Switching - Application Note*.

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Figure 1 is a high-level block diagram of the LXT384 Transceiver.

Figure 1. Intel® LXT384 Transceiver High-Level Block Diagram

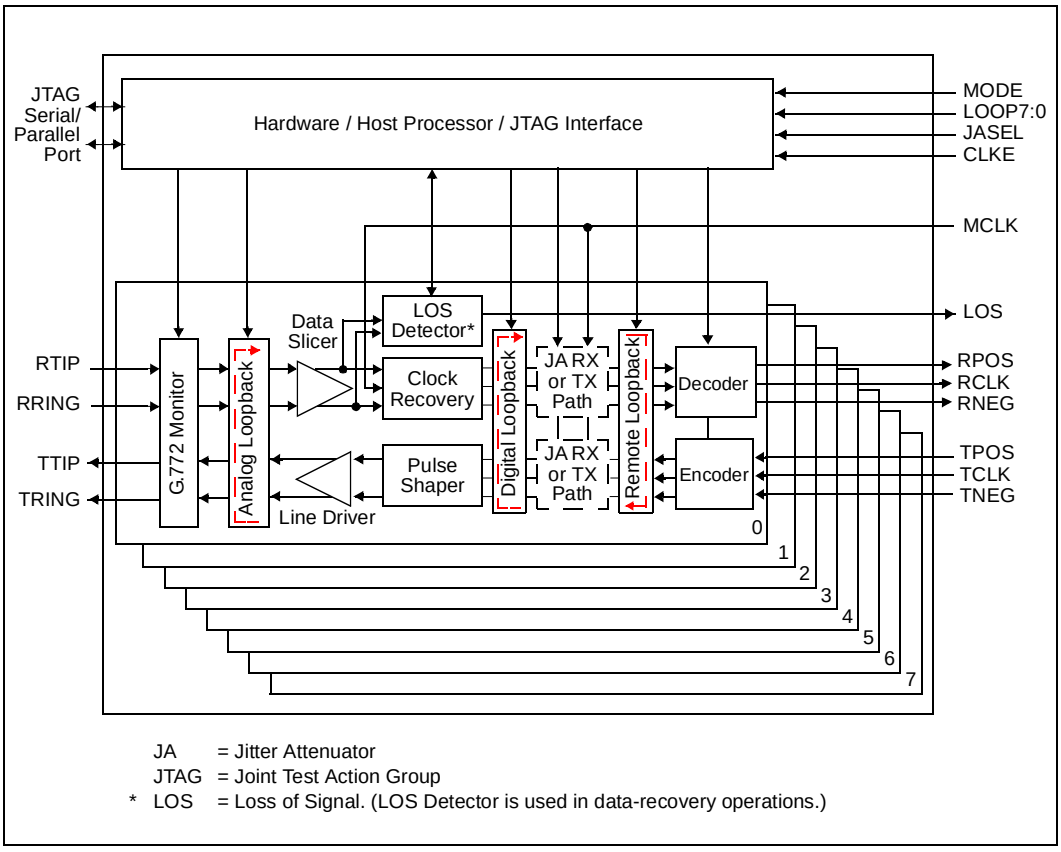

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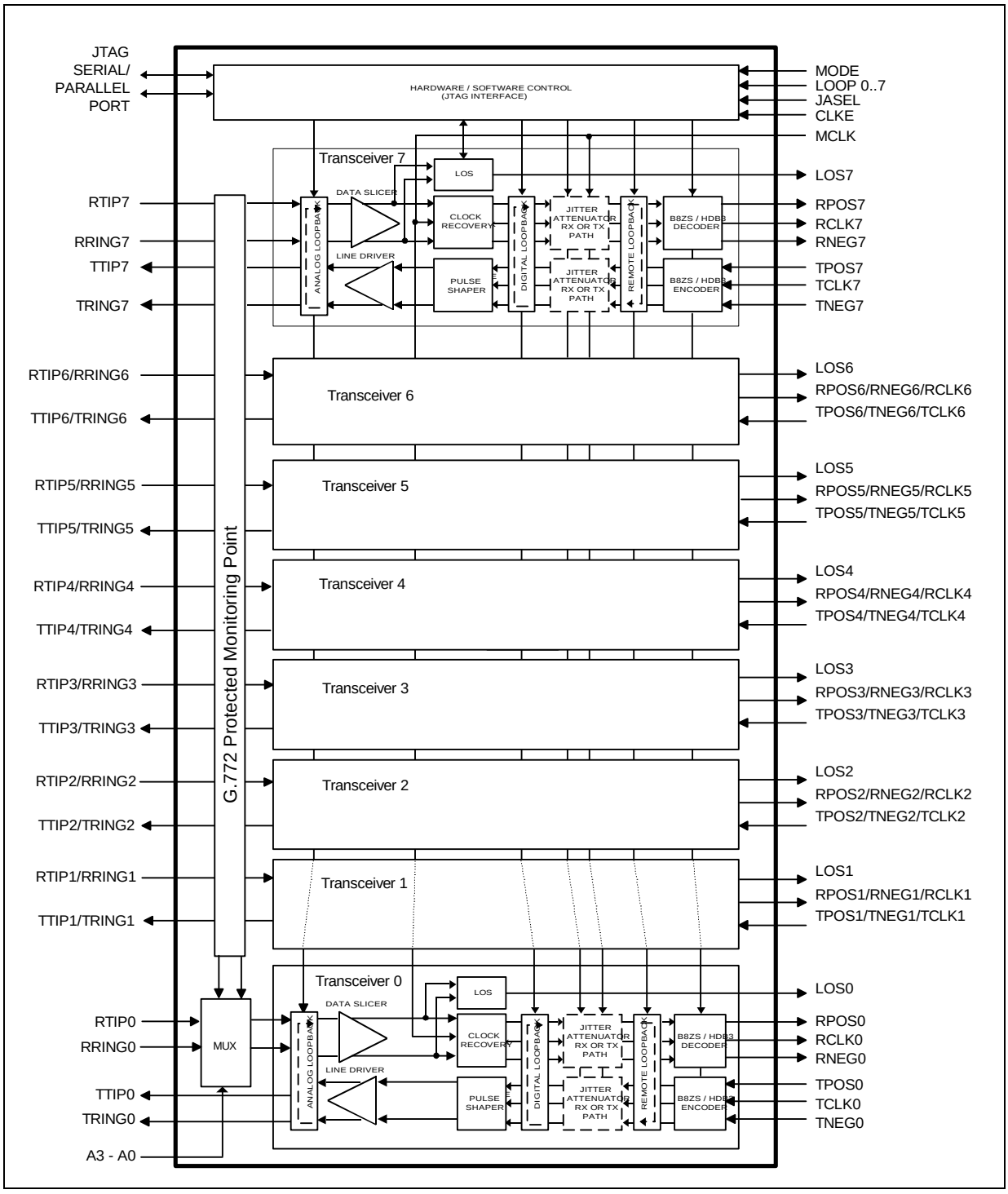
Figure 2 is a detailed block diagram of the LXT384 Transceiver.

Figure 2. Intel® LXT384 Transceiver Detailed Block Diagram



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3.0 Pin Assignments and Package

Table 2 lists the top-side markings for the LXT384 Transceiver, which has two packages:

- A 144-pin Low-Profile Octal-Flat Package, or ‘LQFP’ (Figure 3)
- A 160-ball Plastic Ball Grid Array package, or ‘PBGA’ (Figure 4)

Table 2. Intel® LXT384 Transceiver Package Top-Side Markings

Marking	Definition
Part Number	Number of the unique identifier for this product family
Lot Number	A lot (that is, ‘batch’) number
FPO Number	Identifies the Finish Process Order number
Revision Number	Number of the particular silicon revision, also known as a ‘stepping’. (For information on specific silicon steppings, see specification update documents for the LXT384 Transceiver.)

- For signal descriptions, see Chapter 5.0, “Signal Descriptions”.
- For mechanical specifications, see Chapter 16.0, “Mechanical Specifications”.

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Figure 3 shows a top view of the LXT384 Transceiver Low-profile Octal Flat Pack (LQFP) package, with pin assignments. For package information, see Chapter 18.0, "Package Information".

Figure 3. Intel® LXT384 Transceiver 144-Pin Assignments

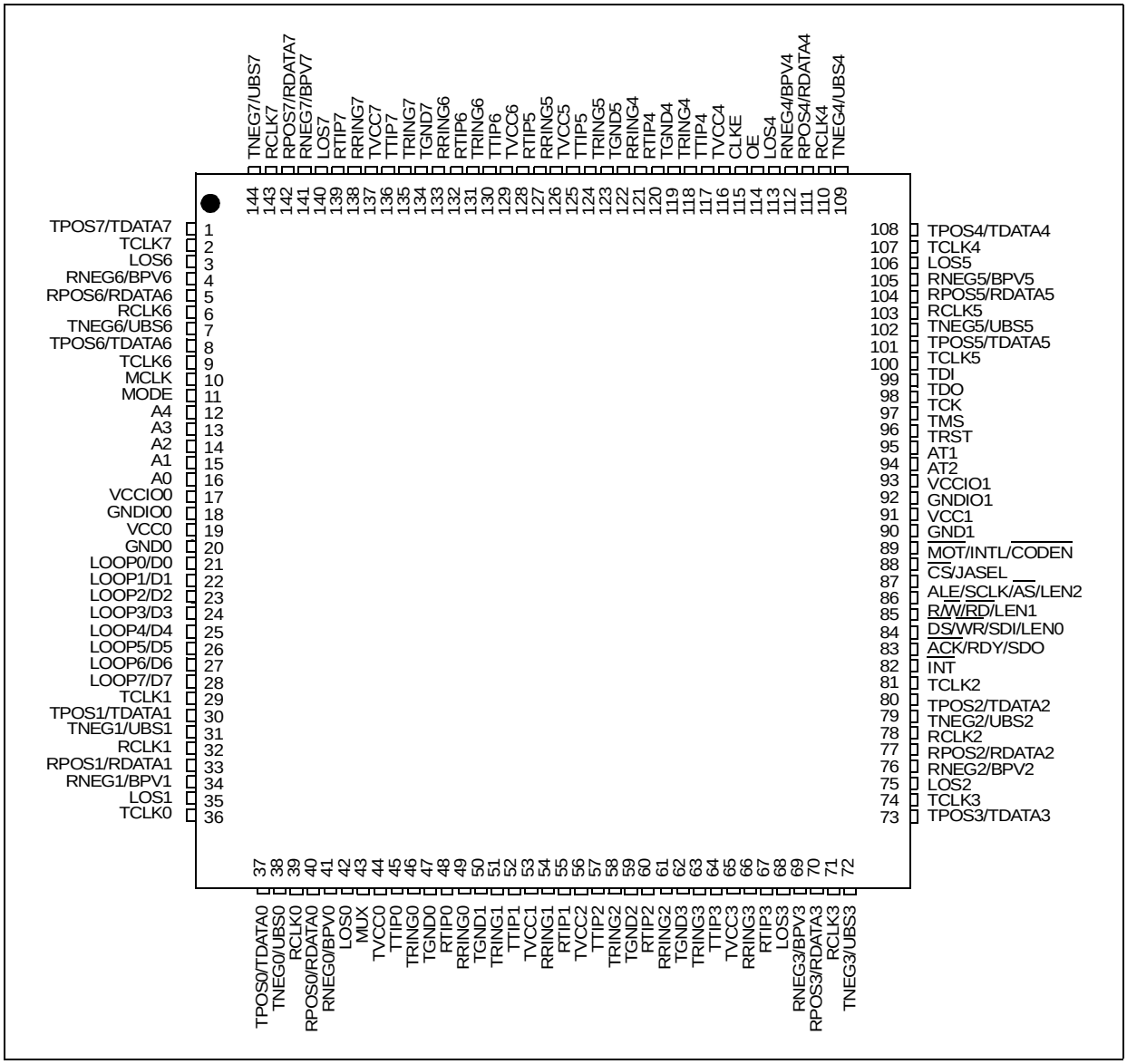

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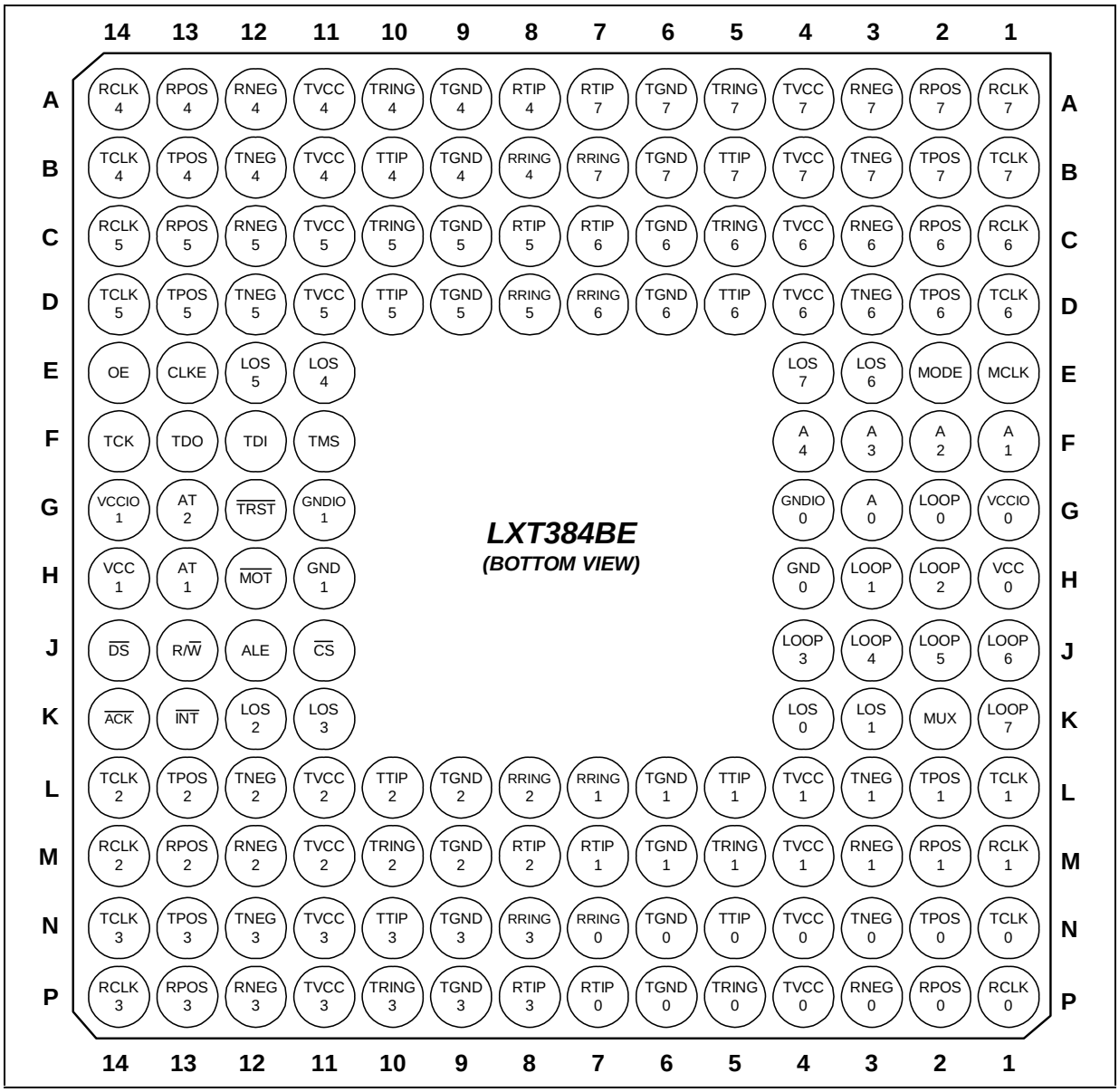
Figure 4 shows a bottom view of the LXT384 Transceiver PBGA package and the pin assignments.

Figure 4. Intel® LXT384 Transceiver Plastic Ball Grid Array (PBGA) Pin Assignments



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4.0 Multi-Function Pins

The LXT384 Transceiver has several pins that have more than one name and more than one function, depending on the mode selected. This chapter lists the multi-function pins. Descriptions of signal functions are in Chapter 5.0, “Signal Descriptions”.

4.1 Operating Mode Multi-Function Pins

Table 3 lists the MODE and $\overline{\text{MOT}}$/INTL pin setting combinations that control the selection of operating modes for the LXT384 Transceiver.

Table 3. Operating Mode Selections

Pin Settings		Operating Mode Selected
MODE	$\overline{\text{MOT}}$/INTL	
Low	Connect either low or high.	Hardware mode
High	Low	Host Processor mode - Motorola processor parallel interface
High	High	Host Processor mode - Intel® processor parallel interface
VCC/2	Connect either low or high.	Host Processor mode - Serial interface

Table 4 lists LXT384 Transceiver pins that have different names and functions depending on the specific operating mode selected. When the operating mode selected is the:

- Hardware mode, Column 1 names and functions apply.
- Host Processor mode with a parallel interface and the $\overline{\text{MOT}}$/INTL pin is:
  - — Low, Column 2 names and functions apply to a Motorola processor with a parallel interface.
  - — High, Column 3 names and functions apply to an Intel® processor with a parallel interface.
- Host Processor mode with a serial interface, Column 4 names and functions apply to either a Motorola processor or an Intel® processor used with a serial interface.

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Table 4. Operating Mode-Specific Signal Names

QFP Pin	PBGA Ball	1. Hardware Mode		Host Processor Mode					
				2. Parallel Interface - Motorola Processor		3. Parallel Interface - Intel® Processor		4. Serial Interface - Motorola or Intel® Processor	
		Signal Name	Signal Function	Signal Name	Signal Function	Signal Name	Signal Function	Signal Name	Signal Function
12	F4	A4	Must connect to ground	A4	Address select	A4	Address select	A4	No connect
13 14 15 16	F3 F2 F1 G3	A3 A2 A1 A0	Use for performance monitoring	A3 A2 A1 A0	Address select	A3 A2 A1 A0	Address select	A3 A2 A1 A0	No connect
88	H12	$\overline{\text{CODEN}}$	HDB3 / AMI select	MOT (see Table 3 on page 19)	Motorola processor select	INTL (see Table 3 on page 19)	Intel® processor select	$\overline{\text{CODEN}}$/ INTL / MOT	No connect
87	J11	JASEL	JA path select	$\overline{\text{CS}}$	Chip select	$\overline{\text{CS}}$	Chip select	$\overline{\text{CS}}$	Chip select
28 27 26 25 24 23 22 21	K1 J1 J2 J3 J4 H2 H3 G2	LOOP7 LOOP6 LOOP5 LOOP4 LOOP3 LOOP2 LOOP1 LOOP0	Loopback mode select	D7 D6 D5 D4 D3 D2 D1 D0	Parallel data bus	D7 D6 D5 D4 D3 D2 D1 D0	Parallel data bus	D7 D6 D5 D4 D3 D2 D1 D0	Must connect to ground
85	J13	R/$\overline{\text{W}}$ / $\overline{\text{RD}}$	Must connect to ground	R/$\overline{\text{W}}$	Read/write	$\overline{\text{RD}}$	Read enable	R/$\overline{\text{W}}$ / $\overline{\text{RD}}$	No connect
86	J12	SCLK / $\overline{\text{AS}}$ / ALE /	Must connect to ground	$\overline{\text{AS}}$	Address strobe	ALE	Address latch enable	SCLK	Shift clock
84	J14	SDI / $\overline{\text{DS}}$ / $\overline{\text{WR}}$	Must connect to ground	$\overline{\text{DS}}$	Data strobe	$\overline{\text{WR}}$	Write enable	SDI	Serial data input
83	K14	SDO / $\overline{\text{ACK}}$ / RDY /	No connect	$\overline{\text{ACK}}$	Data transfer acknowledge	RDY	Ready	SDO	Serial data output

4.2 Framer/Mapper I/O Pins

Depending on the state of a UBS7:0 pin, both the corresponding receiver and transmitter pins are automatically set for either bipolar I/O or unipolar I/O. When a UBS pin is connected:

- Low, bipolar I/O is selected.
- High for more than 16 consecutive MCLK clock cycles, unipolar I/O is selected.

Note: For a description of operating in bipolar or unipolar mode, see Section 5.3.1, "Bipolar vs. Unipolar Operation - Receive Side" on page 27 and Section 5.3.2, "Bipolar vs. Unipolar Operation - Transmit Side" on page 28.

Table 5 lists LXT384 Transceiver receiver pins that have different names and functions depending on the I/O mode selected.

Table 5. Receiver Bipolar/Unipolar I/O Signal Functions

Pins	Balls	Bipolar I/O Signal Functions		Unipolar I/O Signal Functions	
141 4 105 112 69 76 34 41	A3 C3 C12 A12 P12 M12 M3 P3	RNEG7 RNEG6 RNEG5 RNEG4 RNEG3 RNEG2 RNEG1 RNEG0	Receive negative data output	BPV7 BPV6 BPV5 BPV4 BPV3 BPV2 BPV1 BPV0	Detect bipolar violations output
142 5 104 111 70 77 33 40	A2 C2 C13 A13 P13 M13 M2 P2	RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	Receive positive data output	RDATA7 RDATA6 RDATA5 RDATA4 RDATA3 RDATA2 RDATA1 RDATA0	Receive data output
143 6 103 110 71 78 32 39	A1 C1 C14 A14 P14 M14 M1 P1	RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	Receive clock output	RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	Receive clock output

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Table 6 lists LXT384 Transceiver transmitter pins that have different names and functions depending on the I/O mode selected.

Table 6. Transmitter Bipolar/Unipolar I/O Signal Functions

Pins	Balls	Bipolar I/O Signal Functions		Unipolar I/O Signal Functions	
144 7 102 109 72 79 31 38	B3 D3 D12 B12 N12 L12 L3 N3	TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	Transmit negative data input	UBS7 UBS6 UBS5 UBS4 UBS3 UBS2 UBS1 UBS0	Unipolar/Bipolar Select input. In the transmit mode, when TNEG/UBS is high for 16 or more consecutive MCLK clock cycles, unipolar I/O mode is selected.
1 8 101 108 73 80 30 37	B2 D2 D13 B13 N13 L13 L2 N2	TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	Transmit positive data input	TDATA7 TDATA6 TDATA5 TDATA4 TDATA3 TDATA2 TDATA1 TDATA0	Transmit data input
2 9 100 107 74 81 29 36	B1 D1 D14 B14 N14 L14 L1 N1	TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	Transmit clock input	TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	Transmit clock input

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5.0 Signal Descriptions

This chapter lists and describes LXT384 Transceiver signals by function. All digital I/O signals are 5-V tolerant. (For package information, see Chapter 3.0, “Pin Assignments and Package” and Chapter 16.0, “Mechanical Specifications”.)

5.1 Signal Groupings

Signal groupings discussed in this chapter include the following:

- Section 5.2, “Microprocessor-Standard Bus and Interface Signals”
- Section 5.3, “Framer/Mapper Signals”
- Section 5.4, “Line Interface Unit Signals”
- Section 5.5, “Clocks and Clock-Related Signals”
- Section 5.6, “Configuration and Mode-Select Signals”
- Section 5.7, “Signal Loss and Line-Code-Violation Signals”
- Section 5.8, “Power and Grounds”
- Section 5.9, “Test Signals”

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5.2 Microprocessor-Standard Bus and Interface Signals

Table 7 lists and describes the microprocessor-standard bus and interface signals for the LXT384 Transceiver.

For multi-function pins, the pin name in **blue bold** print indicates the signal being discussed.

Note: For information on selecting parallel or serial interfaces, see the signal description for MODE in Section 5.6, "Configuration and Mode-Select Signals", Table 12.

Table 7. Microprocessor-Standard Bus and Interface Signals (Sheet 1 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description

A4
A3
A2
A1
A0
	12
	13
	14
	15
	16
		F4
		F3
		F2
		F1
		G3
			DI	**Address Select Input 4:0.**
				When the LXT384 Transceiver is in the:
				• Host Processor mode using a parallel interface that is in the:
				  • Non-multiplexed mode, A4:0 function as address pins.
				  • Multiplexed mode, A4:0 must be connected to multiplexed Address/Data Bus (AD).
				• Hardware mode, must be connected to ground. See Section 5.7, "Signal Loss and Line-Code-Violation Signals" for other pin functions.

ACK / RDY / SDO	83	K14	DO	**Data Transfer Acknowledge (Active Low) Output.** When the LXT384 Transceiver is in the Host Processor mode using a Motorola processor, ACK acts as a data transfer acknowledge. A low signal on ACK during a data bus operation that is a: • Read operation indicates valid data. • Write operation is an acknowledge signal that indicates a data transfer into an addressed register is accepted. **NOTE:** Wait states occur only if a write cycle immediately follows a previous read or write cycle (for example, read-modify-write). For other pin functions, see RDY and SDO.
ALE / AS / SCLK/LEN2	86	J12	DI	**Address Latch Enable Input.** When the LXT384 Transceiver is in the: • Host Processor mode using an Intel® processor in a parallel interface, ALE acts as an address latch enable. In this case, the address on the multiplexed address/data bus pins D7:0 (also called AD7:0) is clocked into the LXT384 Transceiver with the falling edge of ALE. • Hardware mode, ALE must be connected to ground. For other pin functions, see AS and SCLK.
ALE / **AS** / SCLK/LEN2	86	J12	DI	**Address Strobe (Active Low) Input.** When the LXT384 Transceiver is in the: • Host Processor mode using a Motorola processor in a parallel interface, AS acts as an active-low address strobe. • Hardware mode, AS must be connected to ground. For other pin functions, see ALE and SCLK.
1. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output. OD: Open Drain				

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Table 7. Microprocessor-Standard Bus and Interface Signals (Sheet 2 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
CS / JASEL	87	J11	DI	**Chip Select (Active Low) Input.** When the LXT384 Transceiver is in the: • Host Processor mode, CS is used to select a specific LXT384 Transceiver device so the host processor can communicate with the registers of that LXT384 Transceiver. • Hardware mode, CS functions as JA Select (JASEL). (See JASEL in Section 5.6, "Configuration and Mode-Select Signals".)

D7 / LOOP7
D6 / LOOP6
D5 / LOOP5
D4 / LOOP4
D3 / LOOP3
D2 / LOOP2
D1 / LOOP1
D0 / LOOP0
	28
	27
	26
	25
	24
	23
	22
	21
		K1
		J1
		J2
		J3
		J4
		H2
		H3
		G2
			DI/O	**(Parallel) Data Bus Input/Output 7:0.**
				When the LXT384 Transceiver is in the:
				• Host Processor mode with a parallel interface that is:
				  • Non-multiplexed, D7:0 function as a bi-directional 8-bit data port.
				  • Multiplexed, D7:0 carry both bi-directional 8-bit data and the 8 least-significant address lines.
				• Host processor mode with a serial interface, D7:0 must be grounded.
				• Hardware mode, the D7:0 pins function as LOOP7:0. (See LOOP7:0 in Section 5.4, "Line Interface Unit Signals".)

DS / SDI / WR/ LEN0	84	J14	DI	**Data Strobe (Active Low) Input.** When the LXT384 Transceiver is in the: • Host Processor mode using a Motorola processor, DS acts as a data strobe. • Hardware mode, DS must be connected to ground. For other pin functions, see SDI and WR.
INT	82	K13	OD, DO	**Interrupt (Active Low, Open Drain).** INT is an active low, maskable, open drain output. If either an AIS or LOS interrupt enable bit is enabled, INT goes low to flag the host processor that the status of LXT384 Transceiver registers changed state. The host processor INT input must be set for level triggering. (For information on the LOS interrupt enable, see Table 34. For information on the AIS interrupt enable, see Table 48. For interrupt details, see Section 7.5, "Interrupt Handling"). INT requires an external 10kΩ pull-up resistor.
RD / R/W/ LEN1	85	J13	DI	**Read Enable (Active Low) Input.** When the LXT384 Transceiver is in the: • Host Processor mode using an Intel® processor, RD functions as a read enable. • Hardware mode, RD must be connected to ground. For other pin functions, see R/W.

1. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output. OD: Open Drain

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Table 7. Microprocessor-Standard Bus and Interface Signals (Sheet 3 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
ACK / **RDY** / SDO	83	K14	DO	**Ready Output.** When the LXT384 Transceiver is in the Host Processor mode using an Intel® processor and the signal on RDY is: • Low, RDY indicates a data transfer operation is in progress. • High, RDY indicates a register-access operation is completed. **NOTE:** RDY goes into a high-impedance tristate after completion of a bus cycle. For other pin functions, see $\overline{\text{ACK}}$ and SDO.
$\overline{\text{RD}}$ / **R/$\overline{\text{W}}$**/ LEN1	85	J13	DI	**Read/Write Input (Write Is Active Low).** When the LXT384 Transceiver is in the: • Host Processor mode using a Motorola processor, R/$\overline{\text{W}}$ functions as a read/write signal. • Hardware mode, R/$\overline{\text{W}}$ must be connected to ground. For other pin functions, see $\overline{\text{RD}}$.
$\overline{\text{ALE}}$ / AS / **SCLK**/LEN2	86	J12	DI	**Shift Clock Input.** When SCLK is in the: • Host Processor mode using a serial interface, SCLK acts as a serial shift clock. • Hardware mode, SCLK must be connected to ground. For other pin functions, see $\overline{\text{AS}}$ and ALE.
$\overline{\text{DS}}$ / **SDI** / $\overline{\text{WR}}$/ LEN0	84	J14	DI	**Serial Data Input.** When the LXT384 Transceiver is in the: • Host Processor mode using a serial interface, SDI is used as serial data input. • Hardware mode, SDI must be connected to ground. For other pin functions, see $\overline{\text{DS}}$ and $\overline{\text{WR}}$.
ACK / RDY / **SDO**	83	K14	DO	**Serial Data Output.** When the LXT384 Transceiver is in the Host Processor mode using a serial interface and the signal on CLKE is: • Low, SDO is valid on the falling edge of SCLK. • High, SDO is valid on the rising edge of SCLK. **NOTE:** SDO goes into a high-impedance tristate during a serial port write access. For other pin functions, see $\overline{\text{ACK}}$ and RDY.
$\overline{\text{DS}}$ / SDI / **$\overline{\text{WR}}$**/ LEN0	84	J14	DI	**Write Enable Input.** When the LXT384 Transceiver is in: • Host Processor mode using an Intel® processor, $\overline{\text{WR}}$ acts as a write enable. • Hardware mode, $\overline{\text{WR}}$ must be connected to ground. For other pin functions, see $\overline{\text{DS}}$ and SDI.
1. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output. OD: Open Drain				

5.3 Framer/Mapper Signals

Framer/mapper signals are used to interface the LXT384 Transceiver to a framer/mapper.

5.3.1 Bipolar vs. Unipolar Operation - Receive Side

Table 5 on page 21 lists receive-side framer/mapper signals, which can connect to a framer/mapper using either bipolar or unipolar interface connections. Table 8 lists details.

Depending on the state of a UBS7:0 pin, both the corresponding receiver and transmitter pins are automatically set for either bipolar I/O or unipolar I/O. When a UBS pin is connected:

- Low, bipolar I/O is selected.
- High for more than 16 consecutive MCLK clock cycles, unipolar I/O is selected.

Receive side - Bipolar I/O. When TNEG/UBS is connected low, then bipolar I/O is selected and RNEG/RPOS functions are selected. In this case, the signal flow occurs as follows:

1. The receiver routes receive analog signals from RTIP/RRING to a data recovery circuit.
2. The data recovery circuit converts the incoming line AMI signals, which consist of positive and negative pulses, into a sequence of logic zeroes and ones. It then outputs the resulting information onto RNEG and RPOS.
3. The recovered clock from RTIP/RRING is output at RCLK.
4. The RNEG and RPOS data lines and the RCLK clock line connect the LXT384 Transceiver to a framer/mapper. A logic ‘1’ on:
   - — RNEG indicates that a negative pulse is detected on the line, and corresponds to the receipt of a negative pulse on RRING/RTIP.
   - — RPOS indicates that a positive pulse is detected on the line, and corresponds to the receipt of a positive pulse on RRING/RTIP.
   - — The receiver outputs the recovered clock at RCLK. RCLK synchronizes the data transfer into the framer/mapper.
5. RNEG/RPOS validation relative to RCLK is selectable with CLKE pin polarity. See the CLKE pin description in Table 11, “Clocks and Clock-Related Signals” on page 37.

Note: In bipolar I/O mode, the framer/mapper is responsible for detecting any line-code violations that appear on the line. The framer/mapper also decodes HDB3.

Receive side - Unipolar I/O. When TNEG/UBS is connected high for more than 16 consecutive MCLK cycles, then unipolar I/O is selected and RDATA/BPV functions are active. RDATA does not distinguish between a positive or a negative pulse on the line. In this case, the signal flow occurs as follows:

1. RDATA and RCLK connect the LXT384 Transceiver to a framer/mapper, while BPV acts as a bipolar violation detector. The LXT384 Transceiver internally decodes HDB3/AMI.
2. The receiver outputs the recovered clock at RCLK. RCLK synchronizes the data transfer into the framer/mapper.
3. RDATA does not include information about the polarity of the marks at RTIP/RRING.
4. RDATA validation relative to RCLK is selectable with CLKE pin polarity. See the CLKE pin description in Table 11, “Clocks and Clock-Related Signals” on page 37.

5.3.2 Bipolar vs. Unipolar Operation - Transmit Side

Table 6 on page 22 lists transmit-side framer/mapper signals, which connect to a framer/mapper using either bipolar or unipolar interface connections. Table 8 lists details.

- TDATA - works in combination with BPV outputs, in unipolar mode.
- TNEG - works in combination with TPOS, in bipolar mode.

Depending on the state of a UBS7:0 pin, both the corresponding receiver and transmitter pins are automatically set for either bipolar I/O or unipolar I/O.

When a TNEG/UBS pin is connected low:

- TNEG/TPOS/TCLK lines are active, and bipolar I/O is selected.
  - A logic 1 on TNEG corresponds to the transmission of a negative pulse on TRING/TTIP.
  - A logic 1 on TPOS corresponds to the transmission of a positive pulse on TRING/TTIP.

When a TNEG/UBS pin is connected high for more than 16 consecutive MCLK clock cycles:

- TDATA/TCLK lines are active, and unipolar I/O is selected.
- Polarity cannot be controlled on the TTIP/TRING outputs.
- TCLK supplies the input synchronization for data transfer.

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5.3.3 Framer/Mapper Signals - Details

- Table 8 lists and describes the LXT384 Transceiver framer/mapper receive signals.
- Table 9 on page 31 lists and describes the LXT384 Transceiver framer/mapper transmit signals.

For multi-function pins, the pin name in **blue bold** print indicates the signal being discussed.

Table 8. Framer/Mapper Receive Signals (Sheet 1 of 2)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
BPV7 / RNEG7 **BPV6** / RNEG6 **BPV5** / RNEG5 **BPV4** / RNEG4 **BPV3** / RNEG3 **BPV2** / RNEG2 **BPV1** / RNEG1 **BPV0** / RNEG0	141 4 105 112 69 76 34 41	A3 C3 C12 A12 P12 M12 M3 P3	DO	**Bipolar Violation Detect Output 7:0.** When unipolar I/O is selected for the LXT384 Transceiver, BPV acts as an output line code violation detector. If the LXT384 Transceiver: • Does not detect an in-service line code violation, BPV remains low. • Detects an in-service line code violation, it asserts BPV high. For details on Line Code Violations, see Section 5.7, "Signal Loss and Line-Code-Violation Signals". For other pin functions, see RNEG.
RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	143 6 103 110 71 78 32 39	A1 C1 C14 A14 P14 M14 M1 P1	DO	**Receive Clock Output 7:0.** Normally, this pin provides the recovered clock from the signal received at RTIP and RRING. Under LOS conditions, MCLK replaces RCLK at the RCLK output. For details, see Section 6.3.3, "Receiver Loss-Of-Signal Detector". When MCLK is Low: • The LXT384 Transceiver enters the data recovery mode. • RCLK will be in high impedance state. When MCLK is High: • The clock recovery circuit is disabled. • The RCLK output is then the EX-OR of RPOS and RNEG. This produces a pseudo-recovered clock. For details about the relationship between MCLK and RCLK, see Section 5.5, "Clocks and Clock-Related Signals", especially Table 11 on page 37.
RDATA7 / RPOS7 **RDATA6** / RPOS6 **RDATA5** / RPOS5 **RDATA4** / RPOS4 **RDATA3** / RPOS3 **RDATA2** / RPOS2 **RDATA1** / RPOS1 **RDATA0** / RPOS0	142 5 104 111 70 77 33 40	A2 C2 C13 A13 P13 M13 M2 P2	DO	**Receive Data Output 7:0.** When unipolar I/O is selected for the LXT384 Transceiver, RDATA acts as the receive data output. See Section 5.3.1, "Bipolar vs. Unipolar Operation - Receive Side" on page 27. For other pin functions, see RPOS.

1. AI: Analog Input. AO: Analog Output. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output.

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Table 8. Framer/Mapper Receive Signals (Sheet 2 of 2)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description

BPV7 / **RNEG7**
BPV6 / **RNEG6**
BPV5 / **RNEG5**
BPV4 / **RNEG4**
BPV3 / **RNEG3**
BPV2 / **RNEG2**
BPV1 / **RNEG1**
BPV0 / **RNEG0**
	141
	4
	105
	112
	69
	76
	34
	41
		A3
		C3
		C12
		A12
		P12
		M12
		M3
		P3
			DO	**Receive Negative Data Output 7:0.**
				This signal description applies to both RNEG and RPOS in bipolar I/O mode. When the LXT384 Transceiver is in the:
				• Host processor mode, during an LOS condition, AIS can be inserted into the receive path. See the description of the GCR register RAISEN bit, in Section 6.3.6, "Receive Alarm Indication Signal (RAIS) Enable" on page 50.
				• Hardware mode, RNEG and RPOS remain active during an LOS condition.
				When MCLK is provided with a clocking signal:
				• The LXT384 Transceiver enters clock-recovery mode. RNEG[7:0] act as active-high bipolar Non Return to Zero (NRZ) receive signal outputs.
				  • A High signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING.
				  • A High signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING.
				• These signals are valid on the falling or rising edges of RCLK, depending on the CLKE input. See the CLKE pin description in Table 11, "Clocks and Clock-Related Signals" on page 37.
				When MCLK is high:
				• The LXT384 Transceiver enters data recovery mode. RNEG[7:0] act as RZ data receiver outputs.
				• These signals are valid on the falling or rising edges of RCLK, depending on the CLKE input. See the CLKE pin description in Table 11, "Clocks and Clock-Related Signals" on page 37.
				When MCLK is low:
				• RNEG and RPOS can be placed in a high-impedance tristate with the MCLK pin. (For details, see MCLK in Section 5.5, "Clocks and Clock-Related Signals".)
				NOTE: For pin functions involving unipolar mode, see the BPV pin description.

RDATA7 / **RPOS7** RDATA6 / **RPOS6** RDATA5 / **RPOS5** RDATA4 / **RPOS4** RDATA3 / **RPOS3** RDATA2 / **RPOS2** RDATA1 / **RPOS1** RDATA0 / **RPOS0**	142 5 104 111 70 77 33 40	A2 C2 C13 A13 P13 M13 M2 P2	DO	**Receive Positive Data Output 7:0.** For the RPOS description, see RNEG. **NOTE:** For pin functions involving unipolar mode, see the RDATA pin description.
1. AI: Analog Input. AO: Analog Output. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output.				

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Table 9. Framer/Mapper Transmit Signals (Sheet 1 of 3)

<table>
<tr><th>Signal Name</th><th>QFP Pin</th><th>PBGA Ball</th><th>Signal Type</th><th>Signal Description</th></tr>
<tr><td>TCLK7
TCLK6
TCLK5
TCLK4
TCLK3
TCLK2
TCLK1
TCLK0</td><td>2
9
100
107
74
81
29
36</td><td>B1
D1
D14
B14
N14
L14
L1
N1</td><td>DI</td><td>Transmit Clock Input 7:0.
When the LXT384 Transceiver is in Hardware mode and TCLK is:
Operating with a normal clock signal, TPOS and TNEG are sampled on the falling edge of TCLK.
Low and remains in a low state, the transmitter output drivers enter a low-power high-impedance tristate.
High (for more than 16 consecutive MCLK clock cycles), and MCLK is:
operating normally as a clock, the LXT384 Transceiver enters the TAOS mode. (For details, see Section 6.8, “Transmit All Ones Operations”.
not operating as a clock, but is either low or high, the pulse-shaper circuit shown in Figure 1 is disabled. For information on how to prevent damage to the LXT384 Transceiver when pulse shaping is disabled, see Section 6.4.2, “Transmitter Pulse Shaping”.)
<table>
<tr><th>TCLK</th><th>MCLK</th><th>Result</th></tr>
<tr><td>Normal Clock</td><td>Don’t care</td><td>TNEG and TPOS sampled on falling edge of TCLK</td></tr>
<tr><td>Low</td><td>Don’t care</td><td>Transmitter driver outputs enter high-impedance tristate</td></tr>
<tr><td>High for 16 consecutive MCLK cycles</td><td>Either high or low</td><td>Disables transmit pulse shaping</td></tr>
<tr><td>High for 16 consecutive MCLK cycles</td><td>Normal Clock</td><td>TAOS</td></tr>
</table>
NOTE: When the LXT384 Transceiver is in the Host Processor mode, TAOS mode can be selected using registers in Chapter 8.0, “Registers”.
When pulse shaping is disabled, it is possible to overheat and damage the LXT384 Transceiver by leaving transmit inputs high continuously. For example a programmable ASIC might leave all outputs high over an extended period, until it is programmed. To prevent this, clock one of these signals: TPOS, TNEG, TCLK, or MCLK. Another solution is to set one of these signals low: TPOS, TNEG, TCLK, or OE.
Note: The TAOS generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.</td></tr>
</table>

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Table 9. Framer/Mapper Transmit Signals (Sheet 2 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
TNEG7 / UBS7 **TNEG6** / UBS6 **TNEG5** / UBS5 **TNEG4** / UBS4 **TNEG3** / UBS3 **TNEG2** / UBS2 **TNEG1** / UBS1 **TNEG0** / UBS0	144 7 102 109 72 79 31 38	B3 D3 D12 B12 N12 L12 L3 N3	DI	**Transmit Negative Data Input 7:0.** TNEG and TPOS have the following characteristics: • Operate in bipolar I/O mode. • Active-high NRZ inputs. • Remain active during an LOS condition. TNEG/TPOS pin settings result in the selections shown in the following table. **TPOS** / **TNEG** / **Selection**: 0/0 Space; 0/1 Negative Mark; 1/0 Positive Mark; 1/1 Space (Not legal) • TPOS indicates the transmission of a positive pulse. • TNEG indicates the transmission of a negative pulse. For other pin functions, see UBS.

TNEG7 / **UBS7**
TNEG6 / **UBS6**
TNEG5 / **UBS5**
TNEG4 / **UBS4**
TNEG3 / **UBS3**
TNEG2 / **UBS2**
TNEG1 / **UBS1**
TNEG0 / **UBS0**
	144
	7
	102
	109
	72
	79
	31
	38
		B3
		D3
		D12
		B12
		N12
		L12
		L3
		N3
			DI	**Unipolar/Bipolar Select Input 7:0.**
				The mode-controlled UBS pins define the interface between the framer/mapper and the transceiver.
				When the UBS is connected:
				• Low selects bipolar I/O.
				• High selects unipolar I/O after 16 consecutive TCLK clock cycles. With unipolar I/O, the encoding/decoding type can be either B8ZS/HDB3 or AMI. When the mode is the:
				  • Host Processor mode, the encoding/decoding type is determined by the CODEN bit in the GCR register. (For CODEN bit details, see Chapter 8.0, “Registers”.)
				  • Hardware mode, the encoding/decoding type is determined by the CODEN pin discussed in Section 5.6, “Configuration and Mode-Select Signals”.
				In unipolar I/O mode, TDATA is the data input.
				For other pin functions, see TNEG.

TDATA7 / TPOS7 **TDATA6** / TPOS6 **TDATA5** / TPOS5 **TDATA4** / TPOS4 **TDATA3** / TPOS3 **TDATA2** / TPOS2 **TDATA1** / TPOS1 **TDATA0** / TPOS0	1 8 101 108 73 80 30 37	B2 D2 D13 B13 N13 L13 L2 N2	DI	**Transmit Data Input 7:0.** When unipolar I/O is selected for the LXT384 Transceiver, TDATA is the only data input pin. After passing through the transceiver, TDATA generates the TTIP/TRING outputs. For other pin functions, see TPOS. • TPOS=Transmit Positive data input • TDATA=Transmit Data input

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Table 9. Framer/Mapper Transmit Signals (Sheet 3 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
TDATA7 / **TPOS7** TDATA6 / **TPOS6** TDATA5 / **TPOS5** TDATA4 / **TPOS4** TDATA3 / **TPOS3** TDATA2 / **TPOS2** TDATA1 / **TPOS1** TDATA0 / **TPOS0**	1 8 101 108 73 80 30 37	B2 D2 D13 B13 N13 L13 L2 N2	DI	**Transmit Positive Data Input 7:0.** For the TPOS description, see TNEG. For other pin functions, see TDATA. • TPOS=Transmit Positive Data Input • TDATA=Transmit data Input

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5.4 Line Interface Unit Signals

For multi-function pins, the pin name in **blue bold** print indicates the signal being discussed.

Table 10. Line Interface Unit Signals (Sheet 1 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description

D7 / **LOOP7**
D6 / **LOOP6**
D5 / **LOOP5**
D4 / **LOOP4**
D3 / **LOOP3**
D2 / **LOOP2**
D1 / **LOOP1**
D0 / **LOOP0**
	28
	27
	26
	25
	24
	23
	22
	21
		K1
		J1
		J2
		J3
		J4
		H2
		H3
		G2
			DI/O	**Loopback Mode Input/Output.**
				When the LXT384 Transceiver is in the Hardware mode and a LOOPx pin is:
				• Low, the LXT384 Transceiver enters Remote loopback.
				  • This mode ignores data on TPOS and TNEG, although a TCLK input is still required. An option is to connect RCLK to TCLK externally, outside the transceiver.
				  • Data received on RTIP and RRING is looped around and retransmitted on TTIP and TRING.
				  • In data recovery mode, the pulse template cannot be guaranteed while in a remote loopback. (For details, see Section 6.7.3, “Remote Loopback”.)
				• High, the LXT384 Transceiver enters Analog loopback.
				  • This mode ignores data received on RTIP and RRING.
				  • Data transmitted on TTIP and TRING is internally looped around and routed back to the receive inputs. (For details, see Section 6.7.1, “Analog Loopback”.)
				• Left unconnected, LOOPx stays in a high-impedance tristate.
				  • Loopback is no longer selected.
				  • If the LXT384 Transceiver is used in Hardware mode, to minimize cross-talk, the layout design must not route signals with fast transitions near the LOOP7:0 pins. Also maintain a solid ground plane under these pins.
				When the LXT384 Transceiver is in the Host Processor mode with a:
				• Parallel interface, see the signal descriptions for D7:0 in Section 5.2, “Microprocessor-Standard Bus and Interface Signals”.
				• Serial interface, LOOP7:0 must be grounded.
				For other pin functions, see D7:0 in Section 5.2, “Microprocessor-Standard Bus and Interface Signals”.

1. AI: Analog Input. AO: Analog Output. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output.				

Table 10. Line Interface Unit Signals (Sheet 2 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description

OE	114	E14	DI	**Output Driver Enable Input.**
				Either the (hardware) OE pin or the OER register can be used to place the transmitter TRING and TTIP outputs immediately into a high-impedance mode. This supports redundancy applications without external mechanical relays.
				When the LXT384 Transceiver is in the:
				• Hardware mode and OE is connected:
				  • Low, OE is used to disable all transmit output drivers at one time, and to place TRING and TTIP outputs into high-impedance. All other internal circuitry stays active.
				  • High, OE is used to enable transmitter output drivers.
				• Host Processor mode, instead of the OE pin, you can write a 1 to the $\overline{OE}$ bit of the OER register to place individual TRING and TTIP outputs into high-impedance. (See Table 46 in Chapter 8.0, “Registers”.)
				NOTE: In Host Processor mode, the OE pin when set low overrides the OER register setting.

RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	138 133 126 121 66 61 54 49	B7 D7 D8 B8 N8 L8 L7 N7	AI	**Receive Ring Input 7:0.** RRING (and RTIP) are differential line receiver inputs (see Section 6.3.2, “Receiver Inputs” on page 48). The differential signal received at both RRING and RTIP provides either RDATA, or RPOS/RNEG, depending on mode of operation (unipolar or bipolar). **NOTE:** In clock-recovery mode, the differential signal received at both RRING and RTIP also provides the recovery clock, RCLK. For more information on clock recovery, see Section 6.3.1, “Receiver Clocking”.
RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	139 132 127 120 67 60 55 48	A7 C7 C8 A8 P8 M8 M7 P7	AI	**Receive Tip Input 7:0.** For the RTIP description, see RRING (above).
TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	135 130 123 118 63 58 51 46	A5 C5 C10 A10 P10 M10 M5 P5	AO	**Transmit Ring Output 7:0.** TRING (and TTIP) outputs are used to generate a differential output on the line side of the transmitter transformer. When the LXT384 Transceiver is in: • Hardware mode, and either OE or TCLK is low, TTIP (and TRING) are placed in a high-impedance tristate. • Host Processor mode, TRING and TTIP can be placed in a high-impedance tristate on a port-by-port basis by writing a 1 to the $\overline{OE}$ bit in the Output Enable Register (OER). OE or TCLK low also places TTIP/TRING into high-impedance. (For more information, see Table 46 in Chapter 8.0, “Registers”.)
1. AI: Analog Input. AO: Analog Output. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output.				

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Table 10. Line Interface Unit Signals (Sheet 3 of 3)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
TTIP7	136	B5	AO	**Transmit Tip Output 7:0.**
TTIP6	129	D5		For the TTIP description, see TRING (above).
TTIP5	124	D10		
TTIP4	117	B10		
TTIP3	64	N10		
TTIP2	58	L10		
TTIP1	52	L5		
TTIP0	45	N5		
1. AI: Analog Input. AO: Analog Output. DI: Digital Input. DI/O: Digital Bidirectional Port. DO: Digital Output.				

5.5 Clocks and Clock-Related Signals

Table 11 lists and describes LXT384 Transceiver clocks and clock-related signals.

Note: Within this table, 'RCLK' references RCLK7:0 and 'TCLK' references TCLK7:0. Each RCLK and TCLK signal is used with corresponding signals.

- Example: RCLK6 is the receive clock used by RPOS6 and RNEG6.
- Example: TCLK5 is the transmit clock used by TPOS5 and TNEG5.

Table 11. Clocks and Clock-Related Signals (Sheet 1 of 2)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description

CLKE	115	E13	DI	**Clock Edge Select Input.**
				CLKE is used in clock and data recovery. When the recovery mode is for:
				• Clock recovery (see Section 6.3.1, "Receiver Clocking"), setting the CLKE pin:
				  • Low causes (1) both RDATA or RPOS and RNEG to be valid on the rising edge of RCLK and (2) SDO to be valid on the falling edge of SCLK. (See Figure 20 in Section 19, "Intel® LXT384 Transceiver - Transmit Timing".)
				  • High causes (1) both RDATA or RPOS and RNEG to be valid on the falling edge of RCLK and (2) SDO to be valid on the rising edge of SCLK. (See Figure 20 in Section 19, "Intel® LXT384 Transceiver - Transmit Timing".)
				• Data recovery (see Section 6.3.4, "Receiver Data Recovery Mode"), the output polarity on both RDATA or RPOS and RNEG is:
				  • Active-low when CLKE is low.
				  • Active-high when CLKE is high

CLKE	RCLK for Valid RNEG/RPOS	SCLK for Valid SDO
Low	RCLK 	SCLK 
High	RCLK 	SCLK 

1. DI: Digital Input

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Table 11. Clocks and Clock-Related Signals (Sheet 2 of 2)

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
MCLK	10	E1	DI	**Master Clock Input.** MCLK is an independent, free-running reference clock that must be used at 1.544 MHz for T1 operation or 2.048 MHz for E1 operation, to generate the following internal reference signals: • Reference clock during a blue-alarm transmit-all-ones condition. • Generation of RCLK signal during a loss-of-signal condition. • Timing reference for the integrated clock-recovery unit, and the integrated digital jitter attenuator. • Wait-state generation logic for host processors that use parallel interfaces. If MCLK is: • Low continuously, the complete receive path is powered down and output pins RCLK, RPOS, and RNEG are switched to a high-impedance tristate. • High continuously, the phase-locked loop clock-recovery circuit is disabled and the LXT384 Transceiver operates as only a simple data receiver (without clock recovery). **NOTE:** • MCLK is not required if the LXT384 Transceiver is used as an analog front end without clock recovery and jitter attenuation. • The TAOS generator uses MCLK as a timing reference. To ensure the output frequency is within specification limits, MCLK must have the applicable stability. • If MCLK is not provided, the LXT384 Transceiver cannot be used for data recovery with Motorola processors because wait states cannot be added. (Wait-state generation through $\overline{ACK}$ is not available.) ***Caution:*** Whenever MCLK is not provided, the LXT384 Transceiver is forced into a static state, possibly causing the TTIP/TRING outputs to overheat. To prevent overheating, see Section 6.5, “Line-Interface Protection”.
RCLK				**Receive Clock Output 7:0.** For information on RCLK, see Section 5.3, “Framer/Mapper Signals”.
SCLK				**Shift Clock Input.** For information on SCLK, see Section 5.2, “Microprocessor-Standard Bus and Interface Signals”.
TCLK				**Transmit Clock Input 7:0.** For information on TCLK, see Section 5.3, “Framer/Mapper Signals”.

1. DI: Digital Input

5.6 Configuration and Mode-Select Signals

Table 12 lists and describes the LXT384 Transceiver configuration and mode-select signals. For multi-function pins, the pin name in **blue bold** print indicates the signal being discussed.

Table 12. Configuration and Mode-Select Signals (Sheet 1 of 2)

Signal Name	QFP Pin	PBGA Ball	I/O[1]	Signal Description
CODEN / INTL / $\overline{\text{MOT}}$	88	H12	DI	**Codec Enable Select Input.** When the LXT384 Transceiver is in the Hardware mode, CODEN determines the line encoder/decoder selection when in unipolar mode. When CODEN is: • Low, it enables an HDB3 encoder/decoder for E1 or a B8ZS encoder/decoder for T1. • High, it enables an AMI encoder/decoder (transparent mode). **NOTE:** In the host processor mode, the encoding/decoding type is determined by the CODEN bit. (For CODEN bit details, see Chapter 8.0, "Registers".) For other pin functions, see INTL/$\overline{\text{MOT}}$.
CODEN / **INTL / MOT**	88	H12	DI	**Host Processor Select Input.** When the LXT384 Transceiver is in the host processor mode and this signal is: • high, the host processor interface is configured for Intel® microcontrollers. • low, the host processor interface is configured for Motorola microcontrollers. For other pin functions, see CODEN.
$\overline{\text{CS}}$ / JASEL	87	J11	DI	**Chip Select Input.** In Host Mode, this active Low input is used to access the serial/parallel interface. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low. For information on the $\overline{\text{CS}}$ signal, see Section 5.2, "Microprocessor-Standard Bus and Interface Signals".
$\overline{\text{CS}}$ / **JASEL**	87	J11	DI	**Jitter Attenuator Select Input.** When the LXT384 Transceiver is in the Hardware mode, JASEL determines the jitter attenuator (JA) position, as listed in the following table. JASEL / JA Position: Low = Transmit path; High = Receive path; High impedance = JA is disabled For other pin functions, see $\overline{\text{CS}}$ in Section 5.2, "Microprocessor-Standard Bus and Interface Signals".

1. DI: Digital Input

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Table 12. Configuration and Mode-Select Signals (Sheet 2 of 2)

Signal Name	QFP Pin	PBGA Ball	I/O[1]	Signal Description
MODE	11	E2	DI	**Mode Select Input.** MODE is used to select the type of operating mode the LXT384 Transceiver uses, as shown in the following table. MODE: Low — Hardware mode MODE: High — Host Processor mode - Parallel interface MODE: VCC/2 — Host Processor mode - Serial interface ***Note:*** VCC/2 can be obtained by connecting to a resistive divider consisting of two 10 kΩ resistors across VCC and Ground. • In Hardware Mode (low), the parallel processor interface is disabled and hard-wired pins are used to control configuration and report status. • In Parallel Host Mode (high), the parallel port interface pins are used to control configuration and report status. • In Serial Host mode (VCC/2), the serial interface pins: SDI, SDO, SCLK, and $\overline{CS}$ are used. For details on modes in the table, see the following: • Section 7.2, "Hardware Mode" • Section 7.4.1, "Host Processor Mode - Parallel Interface" • Section 7.4.2, "Host Processor Mode - Serial Interface"
MUX	43	K2	DI	**Multiplexed/Non-Multiplexed Select Input.** When the LXT384 Transceiver is in parallel interface host processor mode, and MUX is: • Low, operation is in non-multiplexed mode. • High, operation is in multiplexed mode. In hardware mode, tie this unused input low. For timing diagrams, see Section 11.2, "Host Processor Mode - Parallel Interface Timing".
TNEG7 / **UBS7** TNEG6 / **UBS6** TNEG5 / **UBS5** TNEG4 / **UBS4** TNEG3 / **UBS3** TNEG2 / **UBS2** TNEG1 / **UBS1** TNEG0 / **UBS0**	144 7 102 109 72 79 31 38	B3 D3 D12 B12 N12 L12 L3 N3	DI	**Unipolar/Bipolar Select Input 7:0.** For information on the UBS signals, see Section 5.3, "Framer/ Mapper Signals".

1. DI: Digital Input

5.7 Signal Loss and Line-Code-Violation Signals

Table 13 lists and the signal loss and line-code violation signals for the LXT384 Transceiver.

Table 13. Signal Loss and Line-Code-Violation Signals

Signal Name	QFP Pin	PBGA Ball	I/O[1]	Signal Description

A4
A3
A2
A1
A0
	12
	13
	14
	15
	16
		F4
		F3
		F2
		F1
		G3
			DI	**Performance Monitoring Input.**
				When the LXT384 Transceiver is in the:
				• Hardware mode, the A3:0 pins make the performance-monitoring selections shown in Table 14. A4 must be connected to ground.
				• Host Processor mode:
				  • These pins no longer control the monitoring function. Instead, in non-multiplexed host mode, these pins function as non-multiplexed address pins (see Section 5.2, “Microprocessor-Standard Bus and Interface Signals”).
				  • For information on how to control performance monitoring, see Table 39, “Performance-Monitoring Register, MON - 0Bh” on page 81.

BPV7:0				**Bipolar Violation Detect Output 7:0.** For information on the BPV signals, see Section 5.3, “Framer/Mapper Signals”.
CLKE				**Clock Edge Select Input.** For information on how CLKE is used for clock and data recovery, see Section 5.5, “Clocks and Clock-Related Signals”.
LOS7 LOS6 LOS5 LOS4 LOS3 LOS2 LOS1 LOS0	140 3 106 113 68 75 35 42	E4 E3 E12 E11 K11 K12 K3 K4	DO	**Loss of Signal Output.** LOS is: • Low when a loss-of-signal condition is cleared (incoming signal with normal levels, being processed through the transceiver). • High (indicating a loss of signal), when there is no incoming signal (sequence of marks for a specified time interval). **NOTE:** When a loss-of-signal condition is cleared, LOS returns to low when an incoming signal has a sufficient number of transitions in a specified time interval. (For details, see Section 6.3.3, “Receiver Loss-Of-Signal Detector”.)
RCLK7:0				**Receive Clock Output 7:0.** For information on how RCLK is used for clock and data recovery, see Section 5.3, “Framer/Mapper Signals”.

1. DI: Digital Input. DO: Digital Output.

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Table 14 lists performance-monitoring selections that can be made when the LXT384 Transceiver is in the Hardware mode.

Table 14. Performance-Monitoring Selections with A3:0 Pins

<table>
<tr><th>Signal Name</th><th>QFP Pin</th><th>PBGA Ball</th><th>Signal Description</th></tr>
<tr><td>A3
A2
A1
A0</td><td>13
14
15
16</td><td>F3
F2
F1
G3</td><td>
Performance Monitoring Input.
When A0 through A2 are low, the LXT384 Transceiver is configured as an octal line transceiver without monitoring.
When the LXT384 Transceiver is in Hardware mode, A3 is used in combination with A2:0 for non-intrusive performance monitoring.

When A2:0 are all ‘0’, there is no performance monitoring of receivers, and the LXT384 Transceiver is configured as an octal line transceiver without monitoring capability.
When A2:0 are not all ‘0’ and:

When A3 = ‘0’, performance monitoring of receivers occurs as shown in the following table.

<table>
<tr><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>No performance monitoring</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Performance monitoring of Receiver 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Performance monitoring of Receiver 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Performance monitoring of Receiver 3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Performance monitoring of Receiver 4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Performance monitoring of Receiver 5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Performance monitoring of Receiver 6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Performance monitoring of Receiver 7</td></tr>
</table>

When A3 = ‘1’, performance monitoring of transmitters occurs as shown in the following table. (Transmitter monitoring is not supported when the respective channel is set to analog loopback mode.)

<table>
<tr><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>Selection</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>No performance monitoring</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Performance monitoring of Transmitter 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Performance monitoring of Transmitter 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Performance monitoring of Transmitter 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Performance monitoring of Transmitter 4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Performance monitoring of Transmitter 5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Performance monitoring of Transmitter 6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Performance monitoring of Transmitter 7</td></tr>
</table>
In non-multiplexed host processor mode, these pins function as processor address pins.
</td></tr>
</table>

5.8 Power and Grounds

Table 15 lists and describes the LXT384 Transceiver power and grounds.

For low-noise operation, the LXT384 Transceiver is designed so that each transmitter has its own power and its own ground. These pins are not necessarily internally connected. For example, for channel 0 transmit, TGND0 is the corresponding ground pin and TVCC0 is the corresponding power pin.

Table 15. Power and Grounds

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
GND1 GND0	89 20	H11 H4	G S	**Ground (Core) 1:0.** GND0 and GND1 pins are ground for the digital core.
GNDIO1 GNDIO0	91 18	G11 G4	G S	**Ground (I/O) 1:0.** GNDIO0and GNDIO1 pins are grounds for the digital I/O interface.
TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	134 131 122 119 62 59 50 47	A6, B6 C6, D6 C9, D9 A9, B9 N9, P9 L9, M9 L6, M6 N6, P6	G	**Transmit Driver Ground 7:0.** TGND[7:0] pins are grounds for the output drivers. Must be tied to PC board ground at all times.
TVCC7 TVCC6 TVCC5 TVCC4 TVCC3 TVCC2 TVCC1 TVCC0	137 128 125 116 65 56 53 44	A4, B4 C4, D4 C11, D11 A11, B11 N11, P11 L11, M11 L4, M4 N4, P4	P	**Transmit Driver Power Supply 7:0.** TVCC[7:0] pins are the power supply pins for the corresponding output drivers. All TVCC pins can be connected to either a 3.3-V or a 5-V power supply. Never leave these pins disconnected. For details, see Section Section 6.4.4, “Transmitter Output Driver Power and Grounds”.
VCC1 VCC0	90 19	H14 H1	P S	**Power (Core) 1:0.** For details, see Chapter 10.0, “Electrical Characteristics”.
VCCIO1 VCCIO0	92 17	G14 G1	P S	**Power (I/O) 1:0.** For details, see Chapter 10.0, “Electrical Characteristics”.

1. G: Ground. P: Power.

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5.9 Test Signals

Table 17 lists and describes the LXT384 Transceiver test signals, which are used to test all digital input, output, and input/output pins.

The JTAG test signals are compatible with the IEEE 1149.1 boundary-scan test.

Table 16. JTAG Analog Interface Test Signals

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
AT2 AT1	93 94	G13 H13	AO AI	**JTAG Analog Test Port 2:1.** • AT2 is the JTAG analog output test port. • AT1 is the JTAG analog input test port. Both test ports are used for test purposes. See Section 9.4.2, “Analog Port Scan Register (ASR)” on page 94 and Figure 17, “Analog Test Port Application” on page 93.
1. AI: Analog Input. AO: Analog Output.				

Table 17. JTAG Digital Interface Test Signals

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
TCK	97	F14	DI	**JTAG Test Clock Input.** TCK is the clock input for JTAG. When TCK is not used, connect it to ground.
TDI	99	F12	DI	**JTAG Test Data Input.** TDI, the test data input for JTAG, is used for loading serial instructions and data into internal test logic. TDI is sampled on the rising edge of TCK. TDI is connected high internally and can be left disconnected.
TDO	98	F13	DO	**JTAG Test Data Output.** TDO, the test data output for JTAG, is used for reading all serial configuration and test data from the internal LXT384 Transceiver test logic. It is updated on the falling edge of TCK.
TMS	96	F11	DI	**JTAG Test Mode Select Input.** TMS, used to control the test-logic state machine, is sampled on the rising edge of TCK. TMS is connected high internally and can be left disconnected.
$\overline{\text{TRST}}$	95	G12	DI	**JTAG Controller Reset Input.** $\overline{\text{TRST}}$ is used to reset the JTAG controller. $\overline{\text{TRST}}$ is connected high internally and can be left disconnected.
1. DI: Digital Input. DO: Digital Output. 2. See Section 9.4.5, “Instruction Register (IR)” on page 95. Figure 15, “JTAG Architecture” on page 86. and Figure 18, “JTAG Timing” on page 95.				

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5.10 Intel® LXT384 Transceiver Line Length Equalizers

In Host Mode, the contents of the Pulse Shaping Data Register (PSDAT) determines the shape of pulse output at TTIP/TRING. Refer to Table 44 and Table 45.

Table 18. Intel® LXT384 Transceiver Line Length Equalizers

Signal Name	QFP Pin	PBGA Ball	Signal Type	Signal Description
LEN0 LEN1 LEN2	84 85 86	J14 J13 J12	DI	**Line Length Equalizer Input 2:0.** In Hardware Mode for the LXT384 Transceiver, these pins determine the shape and amplitude of the transmit pulse.

Table 19. Intel® LXT384 Transceiver Line Length Equalizer Inputs

LEN2	LEN1	LEN0	Line Length[1]	Cable Loss[2]	Operation Mode
0	1	1	0 - 133 ft. ABAM	0.6 dB	T1
1	0	0	133 - 266 ft. ABAM	1.2 dB	
1	0	1	266 - 399 ft. ABAM	1.8 dB	
1	1	0	399 - 533 ft. ABAM	2.4 dB	
1	1	1	533 - 655 ft. ABAM	3.0 dB	
0	0	0	E1 G.703, 75Ω coaxial cable and 120 Ω twisted pair cable.		E1

1. Line length from LXT384 Transceiver to DSX-1 cross-connect point.
2. Maximum cable loss at 772KHz.

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6.0 Functional Description

This functional description chapter follows the flow of signals through an LXT384 Transceiver. This chapter discusses the following topics:

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6.1 Functional Overview

The LXT384 Transceiver is a fully integrated octal line interface unit designed for T1 1.544 Mbps and 2.048 Mbps (E1) short-haul applications. (For a block diagram, see Figure 1.)

The LXT384 Transceiver can be controlled either by a 'Hardware mode' that uses hard-wired pins or by a 'Host Processor mode', which uses either a serial or parallel host processor interface that is controlled in software. (For more information on selecting an operating mode, see Table 3 in Section 4.1, "Operating Mode Multi-Function Pins".)

Each transceiver front end interfaces with four lines: one pair of two lines for transmit, and one pair of two lines for receive. These two pairs make up a digital data loop for full-duplex transmission.

The TCLK pin provides the transmitter timing reference, and the MCLK pin provides the receiver reference clock. The LXT384 Transceiver is designed to operate without any reference clock when it is used as an analog front end (that is, for data recovery in the receiver path and as a line driver in the transmit path). MCLK is mandatory if on-chip clock recovery is required.

Note: MCLK should be true to the recovered clock of the incoming data. It should be only plesiochronous to MCLK.

All eight clock-recovery circuits share the same reference clock defined by the MCLK input signal. (For details on MCLK, see Table 11 in Section 5.5, "Clocks and Clock-Related Signals".)

6.2 Initialization and Reset

Initialization for the LXT384 Transceiver occurs as follows:

1. During power-up, the LXT384 Transceiver is in an unknown state until the power supply reaches approximately 60% of VCC. Also during power-up, an initial reset sets all registers to their default values and resets the status and state machines for the LOS detector circuit.

   (Between 50 and 70% of VCC, the LXT384 Transceiver is in a critical zone. For more information about this critical zone, see the application note on slow power-up rise time, referenced in Section 1.3, "Related Documents".)

2. A write to the reset register (RES, Table 38) initiates a reset cycle that results in setting all LXT384 Transceiver registers to their default values. When the reset cycle occurs:

   a. In the Intel® processor non-multiplexed mode, the reset cycle is 2 microseconds long.

   b. In all other modes, the reset cycle is 1 microsecond long.

Note: For more information related to reset, see Section 7.4.1, "Host Processor Mode - Parallel Interface".

6.3 Receiver

The LXT384 Transceiver has eight identical receivers.

6.3.1 Receiver Clocking

In the receive mode, clocking for the LXT384 Transceiver receiver depends on the following. When the LXT384 Transceiver is in:

- Clock-recovery mode, the RCLK pin provides the recovered clock from the signal received at RRING and RTIP.
- Clock-recovery mode with LOS conditions, at the RCLK output there is a transition from RCLK (derived from recovered data) to MCLK. For more information on clock-recovery mode, see Section 6.3.3, “Receiver Loss-Of-Signal Detector” and Section 6.3.1, “Receiver Clocking”.
- Data-recovery mode and MCLK is:
  - — Low, the RCLK pin is in a high-impedance tristate.
  - — High, the RNEG and RPOS pins are internally connected to an EX-OR output to RCLK for external clock-recovery applications.

For more information on data-recovery mode, see Section 6.3.4, “Receiver Data Recovery Mode”.

6.3.2 Receiver Inputs

A receiver processes input signals as follows:

1. Through the line interface step-down transformer, typically from either a twisted-pair or a coaxial cable. (For transformer specifications, see Figure 6 and Chapter 12.0, “Line-Interface-Unit Circuit Specifications”.) After the transformer, the signal is terminated and is sent to the receiver section of the LXT384 Transceiver.
2. The receiver inputs, RTIP (receives positive pulses) and RRING (receives negative pulses), are processed through the internal differential amplifier. The differential amplifier then sends the signal to the peak detector.

   Recovered data is output at RPOS and RNEG in bipolar mode, or at RDATA in unipolar mode. The recovered clock is output at RCLK. Use the CLKE pin to select the RPOS/RNEG validation relative to the polarity of the edge of RCLK.
3. The peak detector samples a received signal and determines its maximum peak value.

   The receiver can:

   — accurately recover signals in excess of 12 dB of attenuation

   — receive signal levels well below 500 mV.

   Regardless of received signal level, the peak detectors are held above a minimum level of 0.150 V (typical), to provide immunity from impulsive noise.
4. The peak detector sends a percentage of the maximum peak value to the data slicers. This percentage acts as a threshold level to ensure an optimum signal-to-noise ratio. The threshold level is typically 50% for E1 applications (see Table 63, “Intel® LXT384 Transceiver E1 Receive Transmission Characteristics” on page 103) or 70% for T-1 applications (see Table 64, “Intel® LXT384 Transceiver T1 Receive Transmission Characteristics” on page 104).

5. The data slicer processes the received signal, after which the signal simultaneously goes to both the clock and data-recovery sections.
   — The data and timing recovery circuits provide an input jitter tolerance better than required by ITU G.823, as shown in Test Specifications, Figure 33, “Intel® LXT384 Transceiver Jitter Tolerance Performance” on page 128.
   — Depending on the options selected, recovered clock and data signals may be routed through the jitter attenuator, through the HDB3/AMI decoder, and may be output to the framer as either bipolar or unipolar data.

6.3.3 Receiver Loss-Of-Signal Detector

The LXT384 Transceiver loss-of-signal (LOS) detector circuit is designed to detect loss of signals in both analog and digital domains. This circuit is independent of the data slicer.

- In hardware mode, it complies with the latest ITU G.775 (for E1) and ANSI T1.231 (for T1) recommendations.
- Under software control, the detector can be configured to comply to the ETSI ETS 300 233 specification (LACS Register).

The receiver monitor loads a digital counter at the RCLK frequency. The counter is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Depending on the operation mode, a certain number of consecutive zeros sets the LOS signal. The recovered clock is replaced by MCLK at the RCLK output with a minimum amount of phase errors. MCLK is required for receive operation. When the LOS condition is cleared, the LOS flag is reset and another transition replaces MCLK with the recovered clock at RCLK. RPOS/RNEG will reflect the data content at the receiver input during the entire LOS detection period for that channel.

6.3.3.1 G.755 and ETSI 300 233 - Loss of Signal Detection

- In G.775 mode a loss of signal is detected if the signal is below 200mV (typical) for 32 consecutive pulse intervals. The LOS flag is reset when the received signal reaches 12.5% ones density (4 marks in a sliding 32-bit period) with no more than 15 consecutive zeros and the signal level exceeds 250mV (typical). Following the next MCLK transition, MCLK is replaced with a recovered clock at the RCLK output.
- In ETSI 300 233 mode, a loss of signal is detected if the signal is below 200mV for 2048 consecutive intervals (1 ms). The LOS condition is cleared and the output pin returns to Low when the incoming signal has transitions when the signal level is equal or greater than 250mV for more than 32 consecutive pulse intervals. This mode is activated by setting the LACS register bit to one.

6.3.3.2 ANSI T1.231 - Loss of Signal Detection

The T1.231 LOS detection criteria is employed. LOS is detected if the signal is below 200 mV for 175 contiguous pulse positions. The LOS condition is terminated upon detecting an average pulse density of 12.5% over a period of 175 contiguous pulse positions starting with the receipt of a pulse. The incoming signal is considered to have transitions when the signal level is equal or greater than 250 mV.

6.3.4 Receiver Data Recovery Mode

In data-recovery mode, the combined analog/digital LOS detector circuit uses only its LOS analog part, which complies with the ITU-G.775 recommendation. The LOS digital timing is derived from an internal self-timed circuit. RPOS/RNEG stay active during the loss of signal.

The LXT384 Transceiver monitors the incoming signal amplitude. Typically, any signal below 200mV for more than 30µs asserts the corresponding LOS pin. The LOS condition clears when the signal amplitude rises above 250mV. To declare an LOS condition in accordance to ITU G.775, the LXT384 Transceiver requires periods that are more than 10 bits and less than 255 bits.

6.3.5 Receiver Alarm Indication Signal (AIS) Detection

The receiver performs an Alarm Indication Signal (AIS) detection independently of any loopback mode. This feature is available only in the Host Processor mode and only in the clock-recovery mode.

Because there is no clock in the data-recovery mode, AIS detection does not work in that mode. AIS requires MCLK to be active, because the AIS function depends on a clock to count the number of ones in an interval.

6.3.5.1 E1 Mode

After power-on reset, the LACS register (Table 41) can be set to select either the ITU G.775 detection mode or the ETSI 3000 233 detection mode, both of which can be used for AIS. For both ITU G.775 and ETSI ETS 300 233, the AIS condition is:

- Declared when in a 512-bit period, the receiver detects less than 3 zeroes in the data stream.
- Cleared when in a 512-bit period, the receiver detects 3 or more zeroes in the data stream.

6.3.5.2 T1 Mode

ANSI T1.231 detection is employed. The AIS condition is:

- Declared when less than 9 zeros are detected in any string of 8192 bits. This corresponds to a 99.9% ones density over a period of 5.3 ms.
- Cleared when the received signal contains 9 or more zeros in any string of 8192 bits.

6.3.6 Receive Alarm Indication Signal (RAIS) Enable

When an LOS condition is detected, enabling or disabling the Receive Alarm Indication Signal Enable (RAISEN) bit (bit 6) in the Global Control Register (GCR) affects the setting of the AIS Status Monitor register.

- For details on the RAISEN bit, see Table 43, “Global Control Register, GCR - 0Fh” on page 83.
- For details on the AIS Status Monitor register, see Table 47, “AIS Status Monitor Register, AIS - 13h” on page 85.

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When an LOS condition is detected and the RAISEN bit setting is:

- '0', AIS insertion into the receive path is disabled. In this case, there is no effect on the AIS Status Monitor register.
- '1', AIS insertion into the receive path is enabled. In this case, when the signals to the RTIP and RRING inputs to a receiver are:
  - All zeroes, the receiver generates all ones on the RPOS and RNEG outputs, and the AIS Status Monitor register sets to '1'.
  - All ones, the receiver generates all ones on the RPOS and RNEG outputs, and the AIS Status Monitor register clears to '0'.

To prevent inadvertent interrupts during programming, before setting or resetting RAISEN, mask the AIS interrupt enable bit for the corresponding receiver. (See Table 48, "AIS Interrupt Enable Register, AISIE - 14h" on page 85)

6.3.7 Receiver In-Service Line-Code-Violation Monitoring

Receiver in-service line-code-violation monitoring occurs only with unipolar I/O (that is, when TNEG/UBS is connected high for more than 16 consecutive MCLK cycles). In this case, when the LXT384 Transceiver is receiving a line input signal and an in-service line-code violation occurs, how this violation is reported depends on the type of decoder selected.

If the LOS Detector circuit (see Section 6.3.3, "Receiver Loss-Of-Signal Detector") detects an in-service line-code violation and the LXT384 Transceiver decoder type is:

- AMI, all bipolar violations (two consecutive pulses with the same polarity) are reported at the BPV output.
- HDB3, the following occurs:
  - First, the LXT384 Transceiver asserts the BPV pin high for one RCLK period for every bipolar violation that is not part of the zero-code substitution rules.
  - Next, the RDATA pin acts as the receive data output. (For details on the BPV and RDATA pin functions, see Section 5.3, "Framer/Mapper Signals".)
- B8ZS, the following occurs:
  - The LXT384 Transceiver reports bipolar violations on BPV for one RCLK period, for every B8ZS violation that is not part of the zero code substitution rules.
  - Bipolar 8-zero substitution is an encoding method used on T1 circuits that inserts two successive ones of the same voltage—referred to as a bipolar violation—into a signal whenever eight consecutive zeros are transmitted. The device receiving the signal interprets the bipolar violation as a timing mark, which keeps the transmitting and receiving devices synchronized. Ordinarily, when successive ones are transmitted, one has a positive voltage and the other has a negative voltage.

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6.4 Transmitter

The LXT384 Transceiver has eight identical transmitters.

6.4.1 Transmitter Clocking

The eight low-power transmitters of the LXT384 Transceiver are identical. Transmit data is clocked serially into the device at TPOS/TNEG in bipolar mode, or at TDATA in unipolar mode. For each channel, the transmit clock (TCLK) supplies the transmitter input synchronization.

When TNEG/UBS is connected:

- High for more than 16 consecutive MCLK clock cycles, unipolar I/O and HDB3/B8ZS/AMI encoding/decoding is used. In this case, transmit data are clocked serially into the LXT384 Transceiver at TPOS/TDATA, and the LXT384 Transceiver routes the transmit clock and data signals to its internal encoder.
- To an output that supports bipolar mode, the line does not exhibit more than 1 bit consecutively high for any period of time and the LXT384 Transceiver automatically defaults to bipolar operation. Transmit data are clocked serially into the LXT384 Transceiver at TPOS/TNEG.

The transmitter samples TPOS/TNEG or TDATA inputs on the falling edge of TCLK. Refer to the Section 5.5, “Clocks and Clock-Related Signals” on page 37 for MCLK and TCLK timing characteristics.

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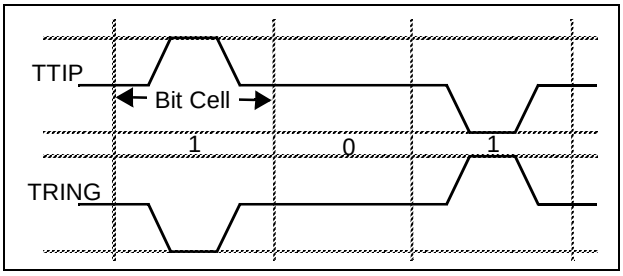
If TCLK:

- Is not supplied, the transmitter output remains powered down and the TTIP/TRING outputs are held in a high-impedance tristate. Fast output tristatability is also available through the OE pin (all ports) or the port's $\overline{OEx}$ bit in the Output Enable Register (OER).
- Is supplied, the input signals that the transmitter samples depends on the TNEG/UBS setting. When TNEG/UBS is connected:
  - — Low (bipolar I/O), the transmitter samples TPOS/TNEG input signals on the falling edge of TCLK.
  - — High for more than 16 consecutive TCLK cycles (unipolar I/O), the transmitter samples TDATA inputs on the falling edge of TCLK.

Zero suppression is available only in Unipolar Mode. The zero-suppression type is HDB3 (E1 environment) or B8ZS (T1 environment). The scheme selected depends on whether the device is set for T1 or E1 operation (determined by LEN2-0 pulse shaping settings). The LXT384 Transceiver also supports AMI line coding/decoding as shown in Figure 5.

- In Hardware mode, use the $\overline{CODEN}$ pin to select AMI coding/decoding.
- In host mode, bit 4 in the GCR (Global Control Register) selects AMI coding/decoding.

Figure 5. 50% AMI Encoding



Each output driver is supplied by its own TVCC and TGND power-supply pins. The transmit pulse shaper is bypassed if no MCLK is supplied. When in this condition, if TCLK is pulled High, then TPOS and TNEG control the pulse width and polarity on TTIP and TRING. With MCLK supplied and TCLK pulled High, the driver enters TAOS (Transmit All Ones pattern).

Note: The TAOS generator uses MCLK as a timing reference. To ensure that the output frequency is within specification limits, MCLK must have the applicable stability. TAOS is inhibited during Remote Loopback.

6.4.2 Transmitter Pulse Shaping

Pulse shaping is a means of converting an input logic '1' into a valid output mark so that the output pulse can be changed (or 'shaped') to adhere to the ITU-T G.703 pulse template (shown in Figure 31 in Chapter 13.0, "Mask Specifications").

The transmit pulse shaper is bypassed if no MCLK is supplied. In this case, if TCLK is pulled high then TPOS and TNEG control the pulse width and polarity on TTIP and TRING. With MCLK supplied and TCLK pulled High, the driver enters TAOS (Transmit All Ones pattern).

Note: The TAOS generator uses MCLK as a timing reference. To ensure that the output frequency is within specification limits, MCLK must have the applicable stability. TAOS is inhibited during Remote Loopback.

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In the Hardware mode, if TCLK is connected high 16 consecutive MCLK clock cycles and MCLK is:

- Not supplied (or 'low'), the transmit pulse-shaper circuit shown in Figure 1 is bypassed (that is, disabled). In this case, TPOS and TNEG control the pulse width and polarity on TTIP and TRING.
- Supplied, the driver enters into a special mode known as Transmit All Ones, or 'TAOS'. For more information on the TAOS mode, see Section 6.8, "Transmit All Ones Operations" and Chapter 8.0, "Registers".

Caution: When the pulse-shaping circuit is disabled, it is possible to overheat and damage the LXT384 Transceiver by leaving transmit inputs connected high continuously. For example, if a programmable ASIC is used in a system that uses the LXT384 Transceiver, the ASIC outputs might be left high until the ASIC is fully programmed. To prevent damage to the LXT384 Transceiver, use either one of the following practices:

- Apply a clock to one of these signals: TPOS, TNEG, TCLK, or MCLK.
- Set one of these signals low: TPOS, TNEG, TCLK, or OE.

6.4.2.1 LXT384 Transceiver Hardware Mode

In hardware mode, pins LEN0-2 of the LXT384 Transceiver determine the pulse shaping as described in Table 20. The LEN settings also determine whether the operating mode is T1 or E1.

Note: In hardware mode, all eight ports will share the same pulse shaping setting. Independent pulse shaping for each channel is available in host mode.

6.4.2.2 LXT384 Transceiver Host Mode

In Host Mode, the contents of the Pulse Shaping Data Register (PSDAT) on the LXT384 Transceiver determines the shape of pulse output at TTIP/TRING. Refer to Table 44 and Table 45.

Table 20. Line Length Equalizer Inputs

LEN2	LEN1	LEN0	Line Length[1]	Cable Loss[2]	Operation Mode
0	1	1	0 - 133 ft. ABAM	0.6 dB	T1
1	0	0	133 - 266 ft. ABAM	1.2 dB	
1	0	1	266 - 399 ft. ABAM	1.8 dB	
1	1	0	399 - 533 ft. ABAM	2.4 dB	
1	1	1	533 - 655 ft. ABAM	3.0 dB	
0	0	0	E1 G.703, 75Ω coaxial cable and 120 Ω twisted pair cable.		E1

1. Line length from LXT384 Transceiver to DSX-1 cross-connect point.
2. Maximum cable loss at 772KHz.

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6.4.2.3 Output Driver Power Supply

The output driver power supply (TVCC pins) can be either 3.3V or 5V nominal.

- When TVCC=5V, theLXT384 Transceiver drives both E1 (75Ω/120Ω) and T1 (100Ω) lines through a 1:2 transformer and 11Ω/9.1Ω series resistors.
- When TVCC=3.3V, the LXT384 Transceiver drives E1 (75Ω/120Ω) lines through a 1:2 transformer and 11Ω series resistor. Use a configuration with a 1:2 transformer and without series resistors to drive T1 100Ω lines.

The Channel 4 (TVCC4) power supply pin sets 3.3V or 5.0V transmit operation. See Table 21.

Removing the series resistors for T1 applications with TVCC=3.3V, improves the power consumption of the device.

However, series resistors in the transmit configuration improve the transmit return loss performance. Good transmit return loss performance minimizes reflections in harsh cable environments. In addition, series resistors provide protection against surges coupled to the device. The resistors should be used in systems requiring protection switching without external relays. Refer to Figure 6 for the recommended external line circuitry.

6.4.2.4 Power Sequencing

For the LXT384 Transceiver, sequence TVCC first, then VCC second or at the same time as TVCC, to prevent excessive current draw.

6.4.3 Transmitter Outputs

A transmitter transmits output signals as follows:

1. Through a step-up transformer, a transmitter transmits an output signal, typically to either a twisted-pair or a coaxial cable. (For transformer specifications, see Figure 6 and Chapter 12.0, “Line-Interface-Unit Circuit Specifications”.)
2. One polarity of the output signal (the positive pulse) is transmitted at TTIP, and the other polarity (the negative pulse) is transmitted at TRING.

Note: If TCLK is not supplied, the transmitter is in a powered-down state and the TTIP and TRING outputs are held in a low-power high-impedance tristate.

6.4.4 Transmitter Output Driver Power and Grounds

Each output driver is supplied by its own separate TVCC and TGND pins. The TVCC pins can be either 3.3 V or 5 V nominal. The LXT384 Transceiver drives either a 75Ω coaxial cable or a 120Ω twisted-pair cable.

For output drive short-circuit protection, see Section 6.5, “Line-Interface Protection”.

6.4.4.1 Transmit Output Standard Power Options

The LXT384 Transceiver standard option uses a 1:2 transformer with two R_T = 11Ω resistors. This power option has more margin for return loss, compared to the low-power option discussed in the following section.

6.4.4.2 Transmitter Output Low-Power Options

The LXT384 Transceiver has a low-power option that meets all other specifications, with a built-in safety margin. This option allows a different turns ratio so that power can be saved on the LXT384 Transceiver power dissipation. To achieve this low-power option, select the turns ratio to 1:1.7 and change the R_T resistor to 10Ω. (See Figure 6 and Table 21.)

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6.5 Line-Interface Protection

Figure 6 shows circuitry for line-interface protection. (While not mandatory for normal operation, Intel® strongly recommends these line-interface protection elements.) For the appropriate values and tolerances of devices used with line-interface protection circuitry, see Table 73 in Chapter 12.0, "Line-Interface-Unit Circuit Specifications".

- **Receive side.** Two 1kΩ resistors protect the receiver against current surges that can couple into the LXT384 Transceiver. Due to the high receiver impedance (typically 70 kΩ), these resistors do not affect the receiver sensitivity.
- **Transmit side.** Resistors R_T and Schottky diodes D1-4 protect the output drivers from line surges. To protect the LXT384 Transceiver output driver from surge currents in excess of 100 mA, a transient voltage suppressor TVS1 (such as Teccor P0080S) is required.

For some power-up operations, on rare occasions there is no activity for several seconds on all of the following transmit-side pins: TPOS, TNEG, TCLK, and MCLK. If this lack of activity occurs for a period of several seconds, then it can cause transmitter outputs to remain in their last-known logic state. If the transmitter outputs are in static mode. As a result, then the transformer output appears as a short circuit to this static DC voltage.

In the worst case of inactivity, one of the transmitter outputs is high while other transmitter outputs are low. In this case, outputs TTIP and TRING would draw excessive current through the transformer primary windings and the LXT384 Transceiver can overheat. To manage this type of power-up operation, do only one of the following:

- Set OE low until normal operations return.
- Set TCLK low until normal operations return.
- Set TNEG low until normal operations return.
- Set TPOS low until normal operations return.
- Provide MCLK with a frequency from 10 kHz to 10 MHz until normal operations return.
- Provide TCLK with a frequency from 100 kHz to 10 MHz until normal operations return.
- Toggle TNEG with a clock from 100 kHz to 10 MHz until normal operations return.
- Toggle TPOS with a clock from 100 kHz to 10 MHz until normal operations return.
- As shown in Figure 6, add a single 0.47 uF capacitor in series with one of the R_T output resistors.

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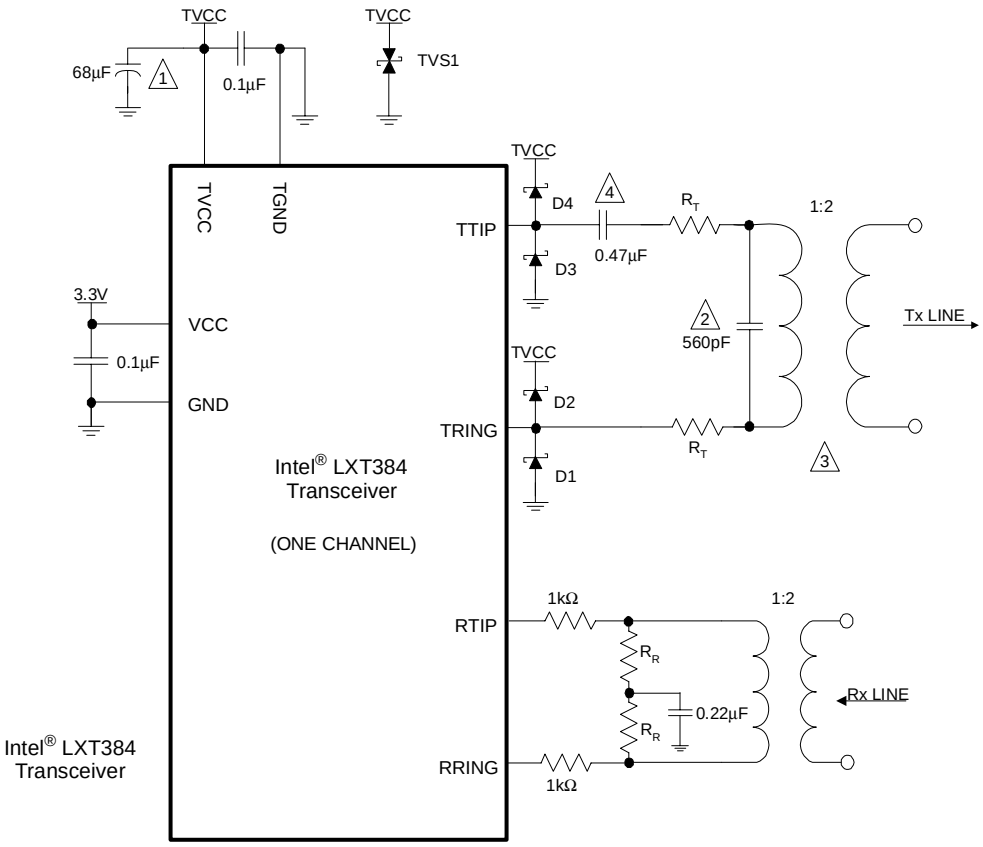
Figure 6. Intel® LXT384 Transceiver External Transmit/Receive Line Circuitry



1. Common decoupling capacitor for all TVCC and TGND pins.
2. Typical value. Adjust for actual board parasitics to obtain optimum return loss.
3. Refer to Transformer Specifications Table for transformer specifications.
4. DC blocking capacitor needed when pulse shaping is disabled. See pin description for TCLK7, pin 2 of QFP package in Table 1.

Component	75Ω Coax	120Ω Twisted Pair	100Ω Twisted Pair TVCC = 5V	100Ω Twisted Pair TVCC = 3.3V
R_T	11Ω ± 1%	11Ω ± 1%	9.1Ω ± 1%	0Ω
R_R	9.31Ω ± 1%	15.0Ω ± 1%	12.4Ω ± 1%	12.4Ω ± 1%
D1 - D4	International Rectifier.....11DQ04 or 10BQ060 Motorola.....MBR0540T1			
TVS1	SGS-Thomson.....SMLVT 3V3 3.3V Transient Voltage Suppressor (TVCC=3.3V) Semtech.....SMCJ5.0AC 5.0V Transient Voltage Suppressor (TVCC=5.0V)			

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Table 21 lists the component values to use with the Figure 6 circuit, depending on the type of power used and the type of cable with which the component is used.

Table 21. Component Values to Use with Transformer Circuit

Component	Component Value to Use with 75 Ω Coaxial Cable	Component Value to Use with 120 Ω Twisted-Pair Cable
R_T Low-Power Value	10 Ω ± 1%	10 Ω ± 1%
R_T Standard-Power Value	11 Ω ± 1%	11 Ω ± 1%
R_R (Receive Resistor)	9.31 Ω ± 1%	15 Ω ± 1%

Table 22 lists the transmitter transformer turns ratios that can selected.

Table 22. Transmitter Transformer Turns Ratio Selection

Characteristic Impedance	Transmitter Transformer Turns Ratio	Component Value to Use with 120 Ω Twisted-Pair Cable
Standard 75/120Ω characteristic impedance	1:2	Rt = 11 Ω ± 1%
Low-power 75/120Ω characteristic impedance	1:1.7	Rt = 10 Ω ± 1%

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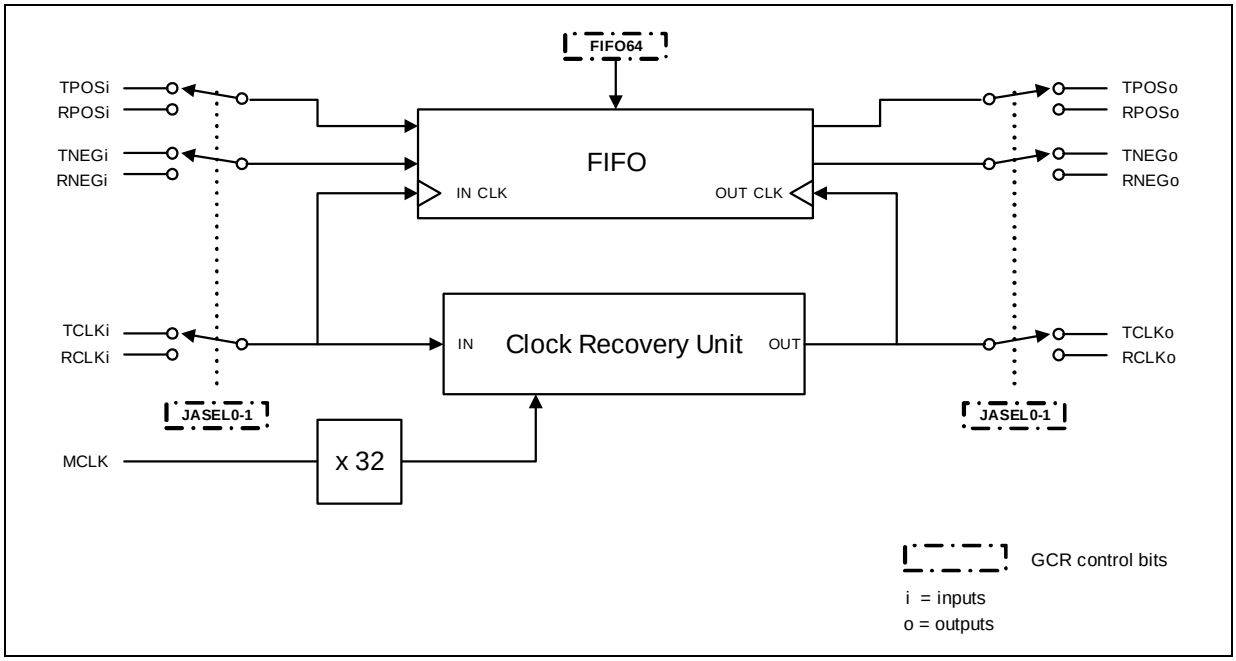
6.6 Jitter Attenuation

Figure 7 shows the internal LXT384 Transceiver jitter attenuation (JA) unit, which requires neither an external crystal nor a reference clock that has a frequency higher than the line frequency.

Data signals are clocked into the FIFO with the associated clock signal (TCLKi or RCLKi) and are clocked out of the FIFO with the JA clock after removing jitter (TCLKo when TCLKi is used, or RCLKo when RCLKi is used). When the FIFO is within two bits of overflowing or underflowing, the FIFO adjusts the output clock by 1/8 of a bit period. For the associated path, the JA produces a constant throughput delay of either 16 bits (when a 32 x 2-bit register is used) or 32 bits (when a 64 x 2-bit register is used).

Figure 7. Jitter Attenuator



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When the LXT384 Transceiver is in the:

- Host Processor mode:
  - The Global Control Register (GCR, Table 43) JASEL bits determine whether the JA is positioned in the receive or transmit path.
  - Depending on the GCR register FIFO64 bit setting, the depth of the FIFO used in the JA is either a 32 x 2-bit FIFO or a 64 x 2-bit FIFO. (For FIFO64 bit details, see Table 43 in Chapter 8.0, “Registers”.)
  - The low-limit jitter attenuator corner frequency depends on the FIFO depth and the JACF bit setting in the GCR register. (For JACF bit details, see Table 43 in Chapter 8.0, “Registers”.)
- Hardware mode:
  - The JASEL pin determines whether JA is positioned in the receive or transmit path.
  - The FIFO length is fixed to 64 bits.
  - The low-limit jitter attenuator corner frequency is fixed to 3.5 Hz for E1 mode, or 6 Hz for T1 mode. (For more information on the JA corner frequency, see Table 76 in Chapter 14.0, “Jitter Performance”.)

For information on jitter attenuation as it applies specifically to the receiver, see Section 6.6, “Jitter Attenuation”.

Standard E1 jitter-attenuation recommendations and specifications that the LXT384 Transceiver JA meets are the following. (For more recommendations and specifications, see Chapter 15.0, “Recommendations and Specifications”.)

- European Telecommunications Standards Institute (ETSI) publication, ETSI CTR12/13
- International Telecommunication Union (ITU) publications:
  - ITU-T G.736
  - ITU-T G.742, when used with the SXT6234 E2-E1 mux/demux.
  - ITU-T G.783, combined jitter when used with the SXT6251 21E1 mapper.
- BAPT220

The LXT 384 Transceiver also supports the following T1 jitter attenuation specifications:

- AT&T Pub 62411
- GR-25-CORE, Category I, R5-203
- TR-TSY-000009

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6.7 Loopbacks

For diagnostics, the LXT384 Transceiver has the following loopback modes:

- Section 6.7.1, “Analog Loopback”
- Section 6.7.2, “Digital Loopback”
- Section 6.7.3, “Remote Loopback”

To select a loopback mode when the mode is in:

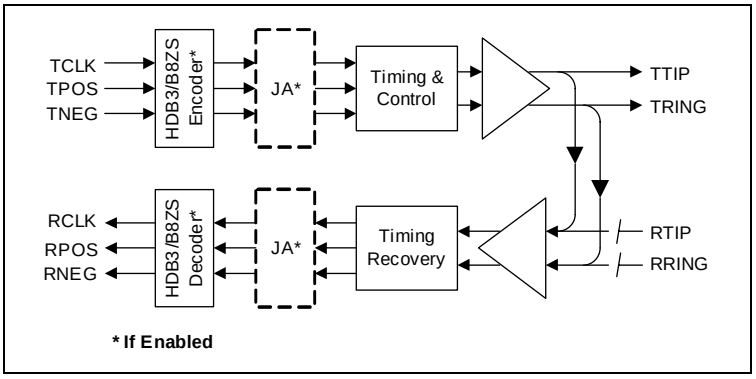
- Hardware mode, the LOOP pins can be used to select either an analog or remote loopback. (See Section 5.4, “Line Interface Unit Signals”.)
- Host Processor mode, the ALOOP, DLOOP, and RLOOP registers can be used to select an analog, digital, or remote loopback. (See Chapter 8.0, “Registers”.)

6.7.1 Analog Loopback

As Figure 8 shows, when analog loopback is selected, the transmitter TTIP and TRING outputs are connected internally to the receiver inputs RTIP and RRING. For the corresponding receiver, clock and data signals are output at RCLK, RPOS, and RNEG. (For the LOOP pin settings that select analog loopback, see Section 5.4, “Line Interface Unit Signals”.)

When the LXT384 Transceiver is in an analog loopback, it ignores signals on RTIP and RRING.

Figure 8. Intel® LXT384 Transceiver Analog Loopback



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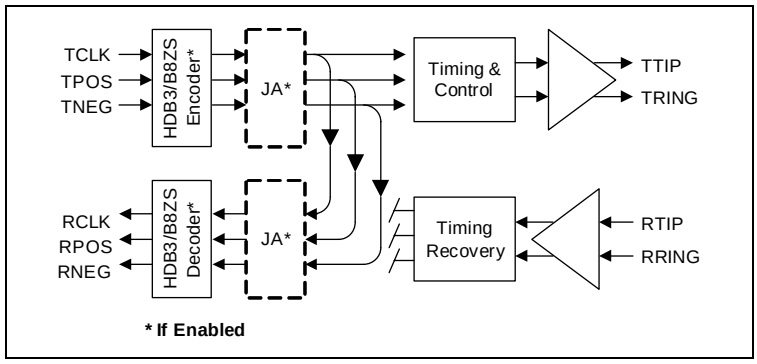
6.7.2 Digital Loopback

The digital loopback function is available in the Host Processor mode only.

As Figure 9 shows, when digital loopback is selected, the transmit clock TCLK and transmit data inputs TPOS and TNEG are looped back and are output on the RCLK, RPOS, and RNEG pins. The data on TPOS and TNEG is also output on the TTIP and TRING pins. (To select digital loopback, see Table 40 in Chapter 8.0, “Registers”.)

When the LXT384 Transceiver is in a digital loopback, it ignores input signals on RTIP and RRING.

Figure 9. Intel® LXT384 Transceiver Digital Loopback



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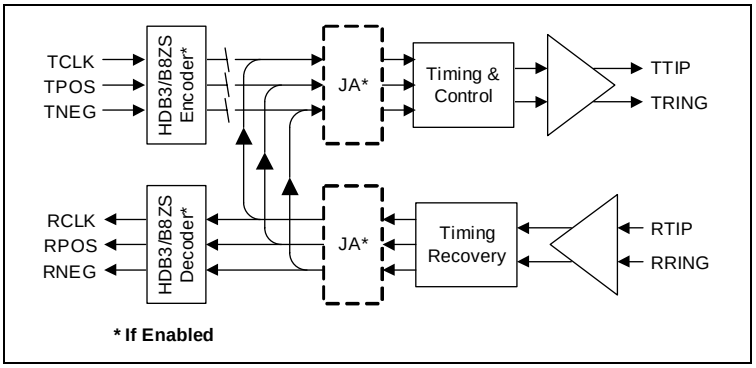
6.7.3 Remote Loopback

As Figure 10 shows, when a remote loopback is selected, the RCLK, RPOS, and RNEG outputs route to the transmit circuits, and data are output on the TTIP and TRING pins. (For the LOOP pin settings that select remote loopback, see Section 5.4, “Line Interface Unit Signals”.)

When the LXT384 Transceiver is in a remote loopback:

- It ignores input signals on the TCLK, TPOS, and TNEG.
- The pulse template cannot be guaranteed in data-recovery mode.

Figure 10. Intel® LXT384 Transceiver Remote Loopback



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6.8 Transmit All Ones Operations

For Transmit All Ones (TAOS) operations, the LXT384 Transceiver has the following TAOS modes:

- Section 6.8.1, “TAOS Generation”
- Section 6.8.2, “TAOS Generation with Analog Loopback”
- Section 6.8.3, “TAOS Generation with Digital Loopback”

Note: The TAOS mode is inhibited during Remote loopback.

6.8.1 TAOS Generation

When the LXT384 Transceiver is set for a:

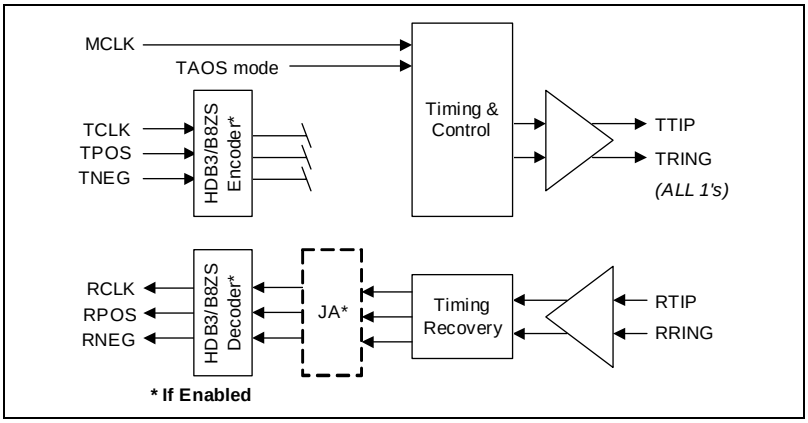
- Hardware mode, the TAOS mode is set by connecting the TCLK pin high for more than 16 MCLK cycles.
- Host Processor mode, the TAOS mode is set by asserting the corresponding bit in the TAOS register. In case of LOS, Automatic TAOS Select (ATS) insertion can be set with the ATS register (Table 42).

Note:

- The TAOS generator uses the clock signal on the MCLK pin as a timing reference. As a result, when the LXT384 Transceiver is set for data-recovery mode with a Motorola processor, TAOS does not work because wait states cannot be added. To ensure the output frequency is within specification limits, MCLK must have the applicable stability.
- When TAOS is active, DLOOP does not function.

Figure 11 shows how the LXT384 Transceiver generates the Transmit All Ones mode.

Figure 11. TAOS Data Path for Intel® LXT384 Transceiver



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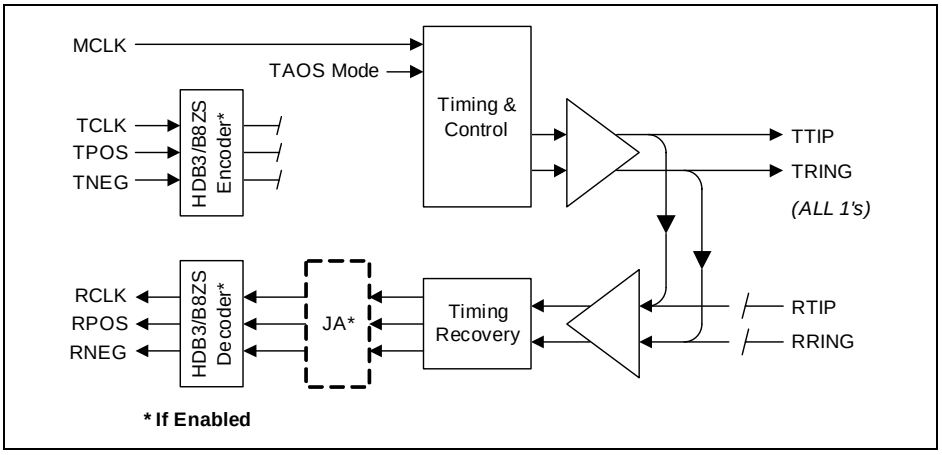
6.8.2 TAOS Generation with Analog Loopback

Figure 12 shows how the TAOS mode affects the receive path after analog loopback.

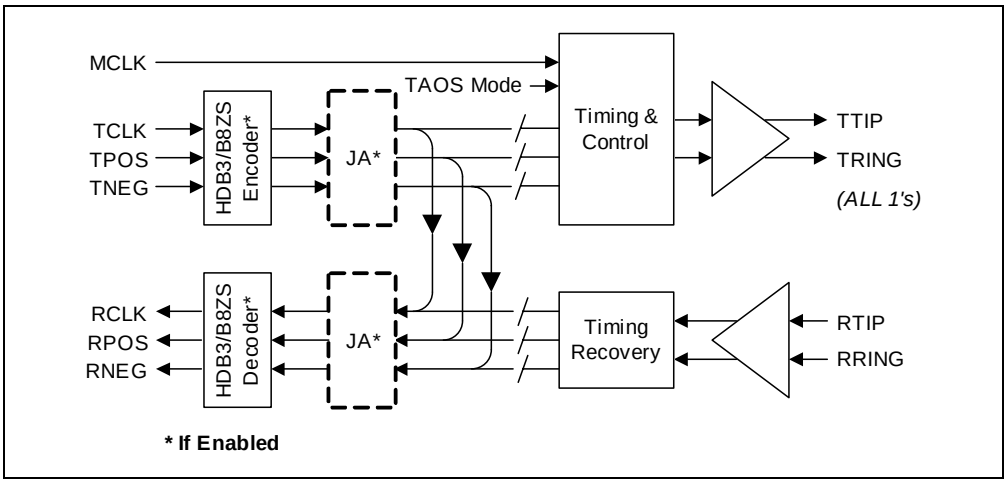
Figure 12. TAOS with Analog Loopback for Intel® LXT384 Transceiver



6.8.3 TAOS Generation with Digital Loopback

Figure 13 shows how the TAOS mode affects the receive path after digital loopback.

Figure 13. TAOS with Digital Loopback for Intel® LXT384 Transceiver



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6.9 Performance Monitoring

The LXT384 Transceiver can be set for either one of the following configurations:

- All eight channels 0 through 7 operating as regular transceivers
- Channels 1 through 7 operating as regular transceivers and the channel 0 transceiver configured for non-intrusive performance monitoring of one of the other channels, per ITU-T G.722

The LXT384 Transceiver can be configured to monitor the performance of either (1) one of the line-side receivers 1 through 7 or (2) one of the line-side transmitters 1 through 7. The configuration can be performed using either the Hardware mode (see Table 14 in Section 5.7, "Signal Loss and Line-Code-Violation Signals") or the Host Processor mode (see Table 39 in Chapter 8.0, "Registers").

Performance Monitoring through Clock and Data Recovery. Performance monitoring of either (1) analog inputs to channels 1 through 7 or (2) analog outputs from any one of channels 1 through 7 can be accomplished through clock and data recovery as follows.

1. As shown in Figure 1 in Chapter 2.0, "Product Summary", the analog input from the channel selected for monitoring is processed by the channel 0 transceiver clock and data recovery.
2. The line signal from the channel selected can then be observed digitally at RCLK0/RPOS0/RNEG0. Channel 0 displays the appropriate LOS state for the line signal of the channel selected, both in transmit and receive directions.

Performance Monitoring through Remote Loopback. Performance monitoring of either (1) analog line inputs RTIP/RRING to any one of channels 1 through 7 or (2) analog line outputs TTIP/TRING from any one of channels 1 through 7 can be accomplished through remote loopback as follows:

1. Configure the LXT384 Transceiver as shown in Figure 10 in Section 6.7.3, "Remote Loopback". (TCLK must be active for remote loopback to operate.)
2. The monitored channel and channel 0 output the same data. By connecting the channel 0 output data (TTIP0/TRING0) to standard test equipment, the line signal from the channel selected can be monitored.

Note: A benefit of performance-monitoring is that the monitored signal can be sent to channel 0, where it can be used as a timing reference clock.

6.10 Intel® Hitless Protection Switching

The LXT384 Transceiver has a feature that allows it to be used in an Intel® Hitless Protection-Switching application. Intel® Hitless Protection-Switching is an alternative redundancy (backup) method that uses very fast silicon switching instead of slow mechanical relays. This method is best implemented using 1+1 circuitry.

The LXT384 Transceiver can provide Intel® Hitless Protection-Switching for the following reasons:

- The transmit outputs from the LXT384 Transceiver can be placed immediately into a high-impedance tristate, which allows two outputs to be connected directly while one output is turned off.
- The jitter attenuator produces a constant throughput delay for smooth switching of data.

For more information about Intel® Hitless Protection-Switching, see the document *1+1 Protection without Relays Using Intel® LXT380/1/4/6/8 Hitless Protection Switching - Application Note* listed in Section 1.3, “Related Documents”.

7.0 Operating Mode Summary

This section discusses the following operating modes:

- Section 7.1, “Interfacing with 5V Logic”
- Section 7.2, “Hardware Mode”
- Section 7.3, “Hardware Mode Settings”
- Section 7.4, “Host Processor Modes”
- Section 7.5, “Interrupt Handling”

7.1 Interfacing with 5V Logic

The LXT384 Transceiver can interface directly with 5V TTL family devices. The internal input pads can tolerate 5V outputs from TTL and CMOS family devices.

7.2 Hardware Mode

The Hardware mode is selected when the MODE pin is connected low, which disables the Host Processor interface. In the Hardware mode, the Host Processor interface pins have different functions, in that they can be hard-wired to control the LXT384 Transceiver for various operation modes and to report on the status of operations.

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7.3 Hardware Mode Settings

Table 23 lists LXT384 Transceiver hardware mode settings for receive, transmit, and loopback operations.

Table 23. Intel® LXT384 Transceiver Operation Mode Summary

MCLK	TCLK	LOOP[1]	Receive Mode	Transmit Mode	Loopback
Clocked	Clocked	Open	Data/Clock recovery	Pulse Shaping ON	No Loopback
Clocked	Clocked	L	Data/Clock recovery	Pulse Shaping ON	Remote Loopback
Clocked	Clocked	H	Data/Clock recovery	Pulse Shaping ON	Analog Loopback
Clocked	L	Open	Data/Clock recovery	Power down	No Loopback
Clocked	L	L	Data/Clock Recovery	Power down	No effect on op.
Clocked	L	H	Data/Clock Recovery	Power down	No Analog Loopback
Clocked	H	Open	Data/Clock Recovery	Transmit All Ones	No Loopback
Clocked	H	L	Data/Clock Recovery	Pulse Shaping ON	Remote Loopback
Clocked	H	H	Data/Clock Recovery	Transmit All Ones	No effect on op.
L	Clocked	Open	Power Down	Pulse Shaping ON	No Loopback
L	Clocked	L	Power Down	Pulse Shaping ON	No Remote Loopback
L	Clocked	H	Power Down	Pulse Shaping ON	No effect on op.
L	H	Open	Power Down	Pulse Shaping OFF	No Loopback
L	H	L	Power Down	Pulse Shaping OFF	No Remote Loop
L	H	H	Power Down	Pulse Shaping OFF	No effect on op.
L	L	X	Power Down	Power down	No Loopback
H	Clocked	Open	Data Recovery	Pulse Shaping ON	No Loopback
H	Clocked	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	Clocked	H	Data Recovery	Pulse Shaping ON	Analog Loopback
H	L	Open	Data Recovery	Power down	No Loopback
H	L	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	H	Open	Data Recovery	Pulse Shaping OFF	No Loopback
H	H	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	H	H	Data Recovery	Pulse Shaping OFF	Analog Loopback

1. Hardware mode only.

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7.4 Host Processor Modes

When the MODE pin is connected high, the following Host Processor modes are available.

- Section 7.4.1, “Host Processor Mode - Parallel Interface”
- Section 7.4.2, “Host Processor Mode - Serial Interface”

7.4.1 Host Processor Mode - Parallel Interface

The parallel interface (listed in Table 3 in Section 4.1, “Operating Mode Multi-Function Pins”) is used to control configuration of the LXT384 Transceiver and to report the status of various operations. The LXT384 Transceiver has a flexible, generic 8-bit parallel host processor interface designed to support both non-multiplexed and multiplexed address/data bus systems for both Motorola bus and Intel® bus topologies. Table 24 lists the four parallel interface modes that can be selected with the pins MODE, $\overline{\text{MOT}}$/INTL, and MUX.

Table 24. Host Processor Mode - Parallel Interface Selections

MODE	$\overline{\text{MOT}}$/ INTL	MUX	Interface Selected
High	Low	Low	Host Processor mode, Motorola processor parallel interface, non-multiplexed
High	Low	High	Host Processor mode, Motorola processor parallel interface, multiplexed
High	High	Low	Host Processor mode, Intel® processor parallel interface, non-multiplexed
High	High	High	Host Processor mode, Intel® processor parallel interface, multiplexed

The Host Processor mode parallel interface includes an address bus (A4:0) and a data bus (D7:0) for non-multiplexed operation and an 8-bit address/data bus for multiplexed operation. The LXT384 Transceiver has a 5-bit address bus and provides 22 user-accessible 8-bit registers for configuration, alarm monitoring, and control of the LXT384 Transceiver.

Control signals that the LXT384 Transceiver and host processors have in common include $\overline{\text{ACK}}$/ RDY, ALE, $\overline{\text{CS}}$, $\overline{\text{DS}}$, $\overline{\text{INT}}$, $\overline{\text{RD}}$, R/$\overline{\text{W}}$, and $\overline{\text{WR}}$. An internal wait-state generator controls the $\overline{\text{ACK}}$/ RDY handshake output signal, which is compatible with both Motorola and Intel® processors. When the processor interface selected is for a:

- Motorola processor and $\overline{\text{ACK}}$ is low, then during a:
  - — Read cycle, $\overline{\text{ACK}}$ indicates that valid information is on the data bus.
  - — Write cycle, $\overline{\text{ACK}}$ indicates the LXT384 Transceiver has accepted the write data from the Motorola processor.
- Intel® processor and RDY is:
  - — Low, the LXT384 Transceiver indicates to the Intel® processor a bus cycle is in progress.

Note: When an Intel® processor is used with a non-multiplexed interface, there is one exception to how write-cycle timing operates that involves the use of Register 0Ah, the reset register. At the start of the write cycle, the RDY line remains high instead of signaling the completion of the write cycle with a transition to a low state. The overall duration of the reset cycle from when the signal on $\overline{\text{CS}}$ is low to the completion of the reset cycle is a total of 3 microseconds. As a result, upon writing to Register 0Ah, allow a minimum of 2 microseconds of constant throughput delay before attempting the next read/write operation. (For more information on the reset cycle, see Table 38 in Section 8.3, “Register Descriptions”.)

7.4.1.1 Host Processor Mode - Parallel Interface, Motorola* Processor

The Motorola processor interface is selected by asserting the LXT384 Transceiver $\overline{\text{MOT}}$/INTL pin low. The R/$\overline{\text{W}}$ signal indicates if a data transfer is to be a read or write. The $\overline{\text{DS}}$ signal is the timing reference for all data transfers and typically has a duty cycle of 50%. When the Motorola processor attempts to:

- Read data from the LXT384 Transceiver, it asserts R/$\overline{\text{W}}$ high on the falling edge on $\overline{\text{DS}}$, and the LXT384 Transceiver drives the data bus.
- Write data to the LXT384 Transceiver, it asserts R/$\overline{\text{W}}$ low on the rising edge on $\overline{\text{DS}}$, and the Motorola processor drives the data bus.

When a Motorola processor is used, $\overline{\text{CS}}$ and $\overline{\text{DS}}$ can be connected. Both read and write cycles require the $\overline{\text{CS}}$ signal to be low and the Motorola processor to actively drive the address pins. The LXT384 Transceiver supports a:

- Non-multiplexed Motorola processor parallel interface when MUX is asserted low. In non-multiplexed mode, the falling edge of $\overline{\text{DS}}$ is used to latch the address information on the address bus, and $\overline{\text{AS}}$ must be connected high.
- Multiplexed Motorola processor parallel interface when MUX is asserted high. The address on the multiplexed address data bus is latched into the LXT384 Transceiver on the falling edge of $\overline{\text{AS}}$.

7.4.1.2 Host Processor Mode - Parallel Interface, Intel® Processor

The Intel® processor interface is selected by asserting the LXT384 Transceiver $\overline{\text{MOT}}$/INTL pin high. Both the read and write cycles require $\overline{\text{CS}}$ to be low. When the Intel® processor attempts to:

- Read data from the LXT384 Transceiver, it asserts $\overline{\text{RD}}$ low while $\overline{\text{WR}}$ is held high.
- Write data to the LXT384 Transceiver, it asserts $\overline{\text{WR}}$ low while $\overline{\text{RD}}$ is held high.

The LXT384 Transceiver supports a:

- Non-multiplexed Intel® processor parallel interface when MUX is asserted low. In non-multiplexed mode, ALE must be connected high and the address and data lines are separate.
- Multiplexed Intel®processor parallel interface when MUX is asserted high. In the multiplexed mode, the falling edge of ALE latches the address.

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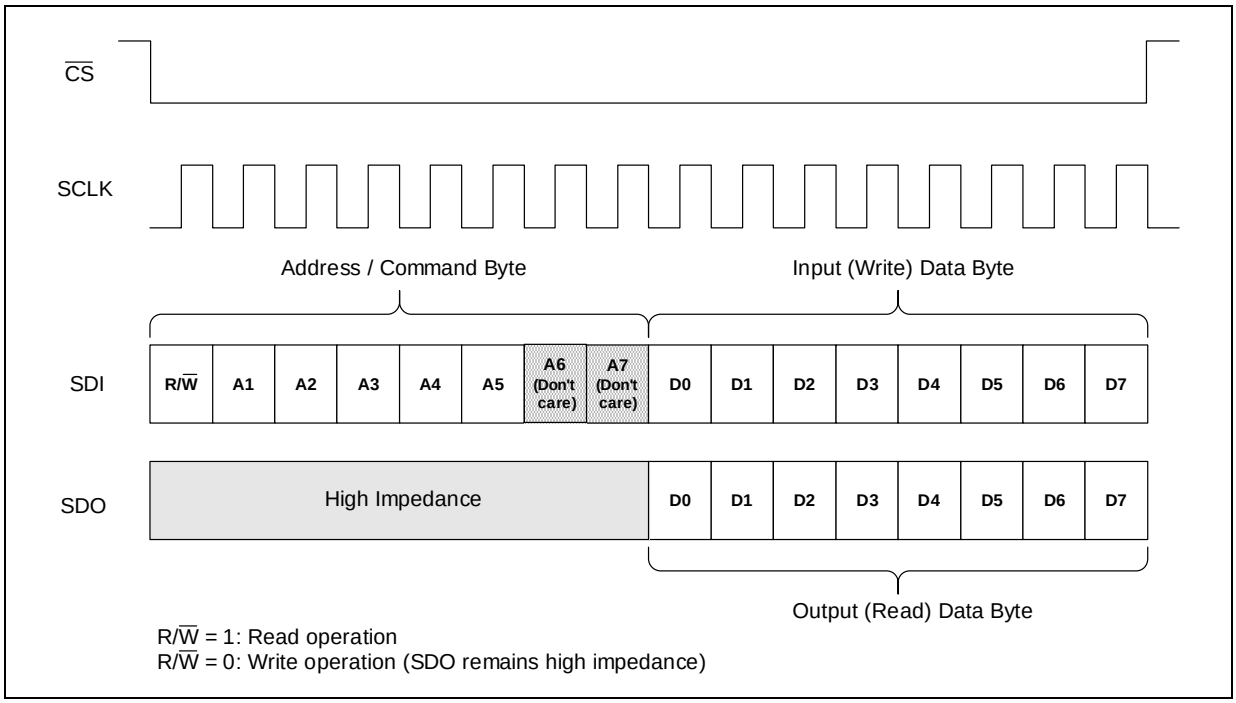
7.4.2 Host Processor Mode - Serial Interface

A Host Processor mode with a serial interface consisting of the $\overline{CS}$, SCLK, SDI, and SDO pins is selected by connecting the MODE pin to a voltage that is equal to 1/2 VCC (which can be accomplished by connecting one 10k Ω resistor to VCC and a second 10k Ω resistor to ground).

Figure 14 shows timing for the host processor interface when it is in serial mode. Registers are accessible through a 16-bit word consisting of the following:

- An 8-bit Address/Command byte.
  - The signal on the R/$\overline{W}$ pin determines whether a read or a write operation occurs.
  - The signals on pins A1-A5 go to an address decoder that decodes an address. (The address decoder ignores signals on the A6 and A7 pins.)
- A subsequent 8-bit Data byte. (Depending on the R/$\overline{W}$ state, the D0-D7 values are valid on either SDI or SDO, but never are the D0-D7 values valid on both SDI and SDO.)
  - When R/$\overline{W}$ = 0, D0-D7 on SDO are don't cares. The D0-D7 values on SDI are active, with valid data being written to the LXT384 Transceiver.
  - When R/$\overline{W}$ = 1, the D0-D7 values on SDO are active, with valid data that the LXT384 Transceiver writes to the host processor. The D0-D7 values on SDI are don't cares.

Figure 14. Host Processor Mode - Serial Interface Read Timing



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7.5 Interrupt Handling

7.5.1 Interrupt Sources

Interrupt sources include the following:

1. Status change in the LOS (Loss of Signal) Status register (04h, Table 32). The LXT384 Transceiver continuously monitors the receiver signal and updates the specific LOS status bit to indicate either the presence or absence of an LOS condition.
2. Status change in the AIS (Alarm Indication Signal) Status register (13h, Table 47). The LOS (Loss of Signal) Status register (04h, Table 32). The LOS (Loss of Signal) Status register (04h, Table 32). The LXT384 Transceiver monitors the incoming data stream and updates the specific AIS status bit to indicate either the presence or absence of a AIS condition.

7.5.2 Interrupt Enable

The LXT384 Transceiver provides a latched interrupt output ($\overline{INT}$). An interrupt occurs any time there is a transition on any enabled bit in the corresponding status register.

Register 06h (Table 34) is the LOS Interrupt Enable register, and register 14h (Table 48) is the AIS Interrupt Enable register. Writing a logic ‘1’ into the corresponding mask register enables a bit in the corresponding interrupt status register to generate an interrupt. The power-on default value is all zeroes. The setting of the interrupt enable bit does not affect the operation of the status registers.

Register 08h (Table 36) is the LOS Interrupt Status register, and register 15h (Table 49) is the RAIS Interrupt Status register. When there is a transition on any enabled bit in a status register, the associated bit of the interrupt status register is set and an interrupt is generated (if one is not already pending). When an interrupt occurs, the $\overline{INT}$ pin is asserted low. The output circuitry of the $\overline{INT}$ pin consists of an active pull-down device (an open drain). An external pull-up resistor of approximately 10kΩ is required to support wired-OR operation with other LXT384 Transceivers.

7.5.3 Interrupt Clear

When an interrupt occurs, the interrupt service routine (ISR) operates as follows:

1. The ISR must read the interrupt status registers (08h and 15h) to identify the interrupt source.
2. The ISR must then read the corresponding status monitor register to obtain the current status of the LXT384 Transceiver.

Note:

- Reading an interrupt-status register clears the ‘sticky’ status bit set by the interrupt. (A ‘sticky’ status bit is a bit that, once set, remains set until it is explicitly cleared.) Automatically clearing an interrupt-status register prepares the register for the next interrupt.
- The status-monitor registers are the LOS Status register (04h, Table 32)and the AIS Status register (13h, Table 47). Reading a status-monitor register clears its corresponding interrupts on the rising edge of the read or data strobe. When all pending interrupts are cleared, the signal on $\overline{INT}$ goes high.

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8.0 Registers

This chapter discusses the LXT384 Transceiver registers.

8.1 Register Summary

Table 25 lists LXT384 Transceiver registers by the hex address of each.

Table 25. Intel® LXT384 Transceiver Register Summary

Address (Hex)	Mnemonic	Cross-Reference
00	ID	Table 28, “ID Register, ID - 00h”
01	ALOOP	Table 29, “Analog Loopback Register, ALOOP - 01h”
02	RLOOP	Table 30, “Remote Loopback Register, RLOOP - 02h”
03	TAOS	Table 31, “TAOS Enable Register, TAOS - 03h”
04	LOS	Table 32, “LOS Status Monitor Register, LOS - 04h”
05	-	Reserved
06	LIE	Table 34, “LOS Interrupt Enable Register, LIE - 06h”
07	-	Reserved
08	LIS	Table 36, “LOS Interrupt Status Register, LIS - 08h”
09	-	Reserved
0A	RES	Table 38, “Reset Register, RES - 0Ah”
0B	MON	Table 39, “Performance-Monitoring Register, MON - 0Bh”
0C	DL	Table 40, “Digital Loopback Register, DL - 0Ch”
0D	LACS	Table 41, “LOS/AIS Criteria Selection Register, LACS - 0Dh”
0E	ATS	Table 42, “Automatic TAOS Select Register, ATS - 0Eh”
0F	GCR	Table 43, “Global Control Register, GCR - 0Fh”
10	-	Reserved
11	-	Reserved
12	OER	Table 46, “Output Enable Register, OER - 12h”
13	AIS	Table 47, “AIS Status Monitor Register, AIS - 13h”
14	AISIE	Table 48, “AIS Interrupt Enable Register, AISIE - 14h”
15	AISIS	Table 49, “AIS Interrupt Status Register, AISIS - 15h”

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Table 26 groups the LXT384 Transceiver registers by function and lists the bit names.

Table 26. Register Bit Names

Register			Bit Names							
Name	**Mne-monic**	**RW**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID, Reset, and Control Registers										
ID	ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset	RES	R/W	RES7	RES6	RES5	RES4	RES3	RES2	RES1	RES0
Global Control	GCR	R/W	Re-served	RAISEN	CDIS	CODEN	FIFO64	JACF	JASEL1	JASEL0
Loopback Registers										
Analog Loopback	ALOOP	R/W	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
Digital Loopback	DL	R/W	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
Remote Loopback	RLOOP	R/W	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
Enable and Select Registers										
AIS Interrupt Enable	AISIE	R/W	AISIE7	AISIE6	AISIE5	AISIE4	AISIE3	AISIE2	AISIE1	AISIE0
LOS Interrupt Enable	LIE	R/W	LIE7	LIE6	LIE5	LIE4	LIE3	LIE2	LIE1	LIE0
Output Enable	OER	R/W	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0
TAOS Enable	TAOS	R/W	TAOS7	TAOS6	TAOS5	TAOS4	TAOS3	TAOS2	TAOS1	TAOS0
Automatic TAOS Select	ATS	R/W	ATS7	ATS6	ATS5	ATS4	ATS3	ATS2	ATS1	ATS0
LOS/AIS Criteria Select	LACS	R/W	LACS7	LACS6	LACS5	LACS4	LACS3	LACS2	LACS1	LACS0
Status and Monitoring Registers										
AIS Interrupt Status	AISIS	R	AISIS7	AISIS6	AISIS5	AISIS4	AISIS3	AISIS2	AISIS1	AISIS0
AIS Status	AIS	R	AIS7	AIS6	AIS5	AIS4	AIS3	AIS2	AIS1	AIS0
LOS Interrupt Status	LIS	R	LIS7	LIS6	LIS5	LIS4	LIS3	LIS2	LIS1	LIS0
LOS Status Monitor	LOS	R	LOS7	LOS6	LOS5	LOS4	LOS3	LOS2	LOS1	LOS0
Performance Monitoring	MON	R/W	Re-served	Re-served	Re-served	Re-served	A3	A2	A1	A0

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8.2 Register Addresses

Table 27 lists the register names and register addresses on:

- Pins A7:1 (used for the LXT384 Transceiver Host Processor mode with a serial interface)
- Pins A7:0 (used for the LXT384 Transceiver Host Processor mode with a parallel interface)

Table 27. Register Addresses for Serial and Parallel Interfaces

Register Name	Host Processor Mode Registers Addresses		Mode
	Serial Interface (Address from Pins A7:1)	Parallel Interface (Address from Pins A7:0)	
ID	xx00000	xxx00000	R
Analog Loopback	xx00001	xxx00001	R/W
Remote Loopback	xx00010	xxx00010	R/W
TAOS Enable	xx00011	xxx00011	R/W
LOS Status Monitor	xx00100	xxx00100	R
LOS Interrupt Enable	xx00110	xxx00110	R/W
LOS Interrupt Status	xx01000	xxx01000	R
Reset	xx01010	xxx01010	R/W
Performance Monitoring	xx01011	xxx01011	R/W
Digital Loopback	xx01100	xxx01100	R/W
LOS/AIS Criteria Selection	xx01101	xxx01101	R/W
Automatic TAOS Select	xx01110	xxx01110	R/W
Global Control	xx01111	xxx01111	R/W
Output Enable	xx10010	xxx10010	R/W
AIS Status Monitor	xx10011	xxx10011	R
AIS Interrupt Enable	xx10100	xxx10100	R/W
AIS Interrupt Status	xx10101	xxx10101	R

8.3 Register Descriptions

Table 28. ID Register, ID - 00h

Bit	Name	Description	R/W
7:0	ID7:0	**Identification.** The identification register contains a unique revision code that is factory programmed for each revision of the LXT384 Transceiver. • Revision code for the LXT384 Transceiver stepping A4 is 00h. • Revision code for the LXT384 Transceiver stepping A5 is 15h.	R

Table 29. Analog Loopback Register, ALOOP - 01h

Bit	Name	Description	R/W
7:0	AL7:0	**Analog Loopback.** Setting one of the AL bits to '1' enables analog loopback for its corresponding transceiver.	R/W

Table 30. Remote Loopback Register, RLOOP - 02h

Bit	Name	Description	R/W
7:0	RL7:0	**Remote Loopback.** Setting one of the RL bits to '1' enables remote loopback for its corresponding transceiver.	R/W

Table 31. TAOS Enable Register, TAOS - 03h

Bit	Name	Description	R/W

7:0	TAOS7:0	**Transmit All Ones (Enable).**
		• On power-up, the TAOS7:0 bits are cleared to '0'.
		• Setting one of the TAOS bits to '1' causes a continuous stream of marks (that is, ones) to be sent out to the TTIP pin and TRING pin of the corresponding transmitter.
		• There are two possible timing references for these bits, depending on the availability of MCLK. If MCLK:
		  • Is not available, then the channel TCLK is used as the timing reference for the output.
		  • Is available, MCLK is used as the timing reference for the output.
		NOTE: TAOS is not available in data-recovery mode or the line-driver mode (that is, when both MCLK = High and TCLK = High).
			R/W

Table 32. LOS Status Monitor Register, LOS - 04h

Bit	Name	Description	R/W
7:0	LOS7:0	**Loss Of Signal Status Monitor.** • On power-up, the LOS7:0 bits are cleared to '0'. • All LOS interrupts are cleared by a single read operation. • Each time the LOS detector detects a valid loss-of-signal condition on a receiver, its corresponding LOS bit is set to '1'.	R

Table 33. DFM Status Monitor Register, DFM (05h) for Intel® LXT384 Transceiver

Bit	Name	Function[1]
7-0	DFM7-DFM0	Respective bit(s) are set to "1" every time the short circuit monitor detects a valid secondary output driver short circuit condition in transceivers 7-0. Note: DFM is available only in configurations with no transmit series resistors (T1 mode with TVCC=3.3V).
1. On power-up all the register bits are set to "0". All DFM interrupts are cleared by a single read operation.		

Table 34. LOS Interrupt Enable Register, LIE - 06h

Bit	Name	Description	R/W
7:0	LIE7:0	**Loss Of Signal Interrupt Enable.** • On power-up, the LIE7:0 bits are cleared to '0' and all LOS interrupts are disabled. • Writing a '1' to an LIE bit enables an LOS interrupt for its corresponding receiver.	R/W

Table 35. DFM Interrupt Enable Register, DIE (07h) for Intel® LXT384 Transceiver

Bit	Name	Function[1]
7-0	DIE7-DIE0	Transceiver 7-0 DFM interrupts are enabled by writing a "1" to the respective bit.
1. On power-up all the register bits are set to "0" and all interrupts are disabled.		

Table 36. LOS Interrupt Status Register, LIS - 08h

Bit	Name	Description	R/W
7:0	LIS7:0	**Loss Of Signal Interrupt Status.** • On power-up, the LIS7:0 bits are cleared to '0'. • After an LOS interrupt is cleared, then each time there is a change in the LOS status of a receiver, the corresponding LIS bit is set to '1'.	R

Table 37. DFM Interrupt Status Register, DIS (09h) for Intel® LXT384 Transceiver

Bit	Name	Function[1]
7-0	DIS7-DIS0	These bits are set to "1" every time a DFM status change has occurred since the last cleared interrupt in transceivers 7-0 respectively.
1. On power up all register bits are set to "0".		

Table 38. Reset Register, RES - 0Ah

Bit	Name	Description	R/W
7:0	RES7:0	**Reset.** The RES7:0 bits are used to set all LXT384 Transceiver registers to their default values. • Except when using an Intel® processor in a non-multiplexed mode, writing to this field initiates a 1-microsecond software reset cycle. • When using Intel® processor in a non-multiplexed mode, to use this field extend the software reset cycle time to 2 microseconds. (For more information on the software reset cycle when using an Intel® processor in a non-multiplexed mode, see Section 7.4.1, “Host Processor Mode - Parallel Interface”.) For details on non-multiplexed and multiplexed modes, see Section 7.4, “Host Processor Modes”.	R/W

Table 39 lists and describes the A3:0 bits that can be used to monitor the performance of one of either Receivers 1 through 7 or one of Transmitters 1 through 7, depending on the setting on the A3 bit. (For more information on performance monitoring, see Section 6.9, "Performance Monitoring".)

Table 39. Performance-Monitoring Register, MON - 0Bh

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>R/W</th></tr>
<tr><td>7:4</td><td>A7:4</td><td>Reserved.</td><td>-</td></tr>
<tr><td>3:0</td><td>A3:0</td><td>
A3:0 (Performance Monitoring Select).
When bits A3:0 are all '0', there is no performance monitoring of receivers, and the LXT384 Transceiver is configured as an octal line transceiver without monitoring capability.
• When A3 is cleared to '0', the following table is used to select how to monitor the performance of receivers.
<table>
<tr><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>No performance monitoring</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Performance monitoring of Receiver 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Performance monitoring of Receiver 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Performance monitoring of Receiver 3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Performance monitoring of Receiver 4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Performance monitoring of Receiver 5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Performance monitoring of Receiver 6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Performance monitoring of Receiver 7</td></tr>
</table>
• When A3 is set to '1', the following table is used to select how to monitor the performance of transmitters. (Transmitter monitoring is not supported when the respective channel is set to analog loopback mode.)
<table>
<tr><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>Selection</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>No performance monitoring</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Performance monitoring of Transmitter 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Performance monitoring of Transmitter 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Performance monitoring of Transmitter 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Performance monitoring of Transmitter 4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Performance monitoring of Transmitter 5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Performance monitoring of Transmitter 6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Performance monitoring of Transmitter 7</td></tr>
</table>
</td><td>R/W</td></tr>
</table>

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Table 40. Digital Loopback Register, DL - 0Ch

Bit	Name	Description	R/W
7:0	DL7:0	**Digital Loopback.** • On power-up, the DL7:0 bits are cleared to '0', and all digital loopback channels are disabled. • Setting a DL bit to '1' enables digital loopback for its corresponding transceiver. During digital loopback, LOS and TAOS stay active and independent of TCLK, while data received on TPOS, TNEG, and CKLK loop back to RPOS, RNEG, and RCLK.	R/W

Table 41. LOS/AIS Criteria Selection Register, LACS - 0Dh

Bit	Name	Description	R/W

7:0	LACS7:0	**Loss of Signal / Alarm Indication Signal Selection Criteria.**
		• At power-up, all LACS7:0 bits are cleared to '0'.
		• After power-up, programming an LACS bit to:
		  • '0' selects the ITU G.775 mode [for LOS, AIS, and remote detect indication (RDI)] for its corresponding receiver.
		  • '1' selects the ETSI 300 233 LOS and AIS detection mode for the corresponding receiver.
		• In T1 mode, this register is "Don't Care." The LXT384 Transceiver uses T1.231 compliant LOS/AIS detection.
			R/W

Table 42. Automatic TAOS Select Register, ATS - 0Eh

Bit	Name	Description	R/W
7:0	ATS7:0	**Automatic Transmit-All-Ones Select.** • On power-on, all ATS7:0 bits are cleared to '0'. • When this field is set to '1', then when there is an LOS condition, TAOS can be generated automatically. **NOTE:** This register does not work during either data-recovery mode or line-driver mode (that is, when both MCLK = High and TCLK = High).	R/W

Table 43. Global Control Register, GCR - 0Fh

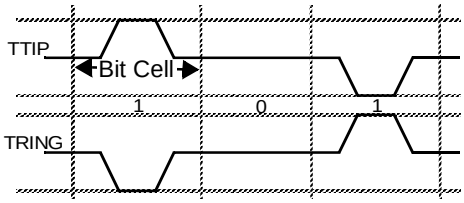
Bit	Name	Description	R/W
7	-	Reserved.	R/W
6	RAISEN	**Receive Alarm Indication Signal Enable.** This bit controls automatic AIS insertion in the receive path when LOS occurs. • 0 = Receive path AIS insertion is disabled on LOS. • 1 = Receive path AIS insertion is enabled on LOS, and the effective output appears on RPOS/RNEG. **NOTE:** This feature is not available in data-recovery mode (that is, when MCLK is high). When changing the value of the RAISEN bit, disable AIS interrupts to prevent inadvertent interrupts.	R/W
5	CDIS	**Circuit Disable.** This bit enables/disables the short-circuit protection feature for the transmitters. • 0 = Enable • 1 = Disable	R/W
4	CODEN	**Code Enable.** This bit selects one of two available zero-suppression codes. Zero suppression operations are available only with unipolar I/O. • 0 = High-Density Bipolar three (HDB3) for E1 or B8ZS for T1 • 1 = Alternate Mark Inversion, or 'AMI'. The following figure shows AMI coding that is 1:1 (or '50%'), indicating that for every one bit sit to a '1', there is a corresponding '0' logic state. 	R/W
3	FIFO64	**First-In First-Out 64-Bit Select.** This bit determines the jitter attenuator FIFO depth as follows: • 0 = Jitter attenuator FIFO is 32 bits deep. • 1 = Jitter attenuator FIFO is 64 bits deep.	R/W
2	JACF	**Jitter Attenuator Corner Frequency.** This bit determines the jitter attenuator low-limit 3-dB corner frequency. For more information, see Chapter 14.0, "Jitter Performance".	R/W
1:0	JASEL1:0	**Jitter Attenuator Select.** These bits determine the jitter attenuator position as follows: JASEL1 / JASEL0 / Jitter Attenuator Position x / 0 / Jitter attenuator is disabled. 0 / 1 / Jitter attenuator position is the transmit path. 1 / 1 / Jitter attenuator position is the receive path.	R/W
1. On power-on reset, the register is set to '0'.			

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Table 44. Pulse Shaping Indirect Address Register, PSIAD (10h)

Bit[1]	Name	Function
0-2	LENAD 0-2	The three bit value written to these bits determine the channel to be addressed. Data can be read from (written to) the Pulse Shaping Data Register (PSDAT). LENAD 0-2 / Channel / LENAD 0-2 / Channel 0h / 0 / 4h / 4 1h / 1 / 5h / 5 2h / 2 / 6h / 6 3h / 3 / 7h / 7
3 - 7	-	Reserved.
1. On power-on reset the register is set to “0”.		

Table 45. Pulse Shaping Data Register, PSDAT (11h) for Intel® LXT384 Transceiver

Bit	Name	Function					
0-2	LEN 0-2[1]	LEN0-2 determine the operation mode of the LXT384 Transceiver: T1 or E1. In addition, for T1 operation, LEN2-0 set the pulse shaping to meet the T1.102 pulse template at the DSX-1 cross-connect point for various cable lengths:					
		LEN2	LEN1	LEN0	Line Length	Cable Loss[2]	Operation Mode
		0	1	1	0 - 133 ft. ABAM	0.6 dB	T1
		1	0	0	133 - 266 ft. ABAM	1.2 dB	
		1	0	1	266 - 399 ft. ABAM	1.8 dB	
		1	1	0	399 - 533 ft. ABAM	2.4 dB	
		1	1	1	533 - 655 ft. ABAM	3.0 dB	
		0	0	0	E1 G.703, 75Ω coaxial cable and 120Ω twisted pair cable.		E1
3 - 7	-	Reserved.					
1. On power-on reset the register is set to “0”. 2. Maximum cable loss at 772 KHz. 3. When reading LEN, bit values appear inverted.							

Table 46. Output Enable Register, OER - 12h

Bit	Name	Description	R/W
7:0	$\overline{OE}$7:0	**Output Enable.** • On power-up, all $\overline{OE}$7:0 bits are cleared to ‘0’. • When an $\overline{OE}$ bit is set to ‘1’, the output driver of its corresponding transmitter goes into a high-impedance tristate.	R/W

Table 47. AIS Status Monitor Register, AIS - 13h

Bit	Name	Description	R/W
7:0	AIS7:0	**Alarm Indication Signal Status Monitor.** • On power-up, all AIS7:0 bits are cleared to '0'. • All AIS interrupts are cleared by a single read operation. • Each time a channel receiver detects an AIS condition, its corresponding AIS bit is set to '1'.	R

Table 48. AIS Interrupt Enable Register, AISIE - 14h

Bit	Name	Description	R/W
7:0	AISIE7:0	**Alarm Indication Signal Interrupt Enable.** • On power-up, all AISIE7:0 bits are cleared to '0'. • When an AISIE bit is set to '1', it enables an AIS interrupt for its corresponding receiver.	R/W

Table 49. AIS Interrupt Status Register, AISIS - 15h

Bit	Name	Description	R/W
7:0	AISIS7:0	**Alarm Indication Signal Interrupt Status.** • On power-up, all AISIS7:0 bits are cleared to '0'. • Each time there is a change in the AIS status of a receiver, its corresponding AISIS bit is set to '1'. • After the host processor reads this register, all AISIS bits clear to '0'.	R

9.0 JTAG Boundary Scan

9.1 Overview

The LXT384 Transceiver supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

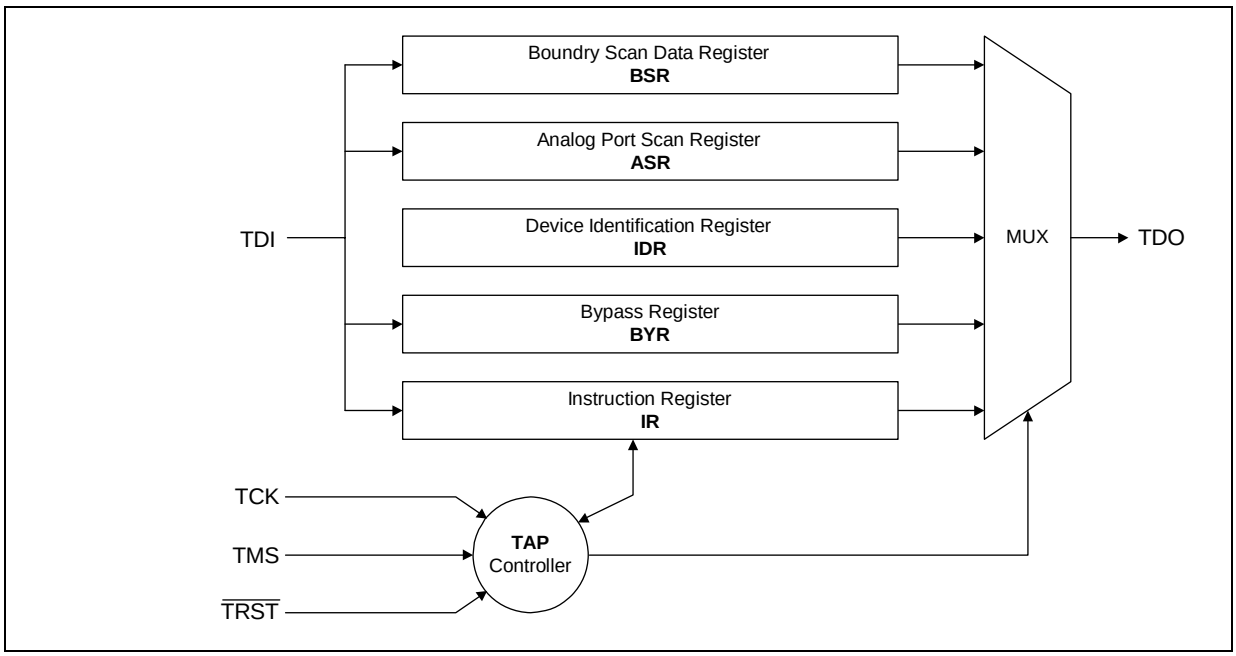
In addition to the traditional IEE1149.1 digital boundary scan capabilities, the LXT384 Transceiver also includes analog test port capabilities. This feature provides access to the TIP and RING signals in each channel (transmit and receive). This way, the signal path integrity across the primary winding of each coupling transformer can be tested.

9.2 Architecture

The basic JTAG architecture of the LXT384 Transceiver is illustrated in Figure 15.

The LXT384 Transceiver JTAG architecture includes a TAP Test Access Port Controller, data registers and an instruction register. The following paragraphs describe these blocks in detail.

Figure 15. JTAG Architecture



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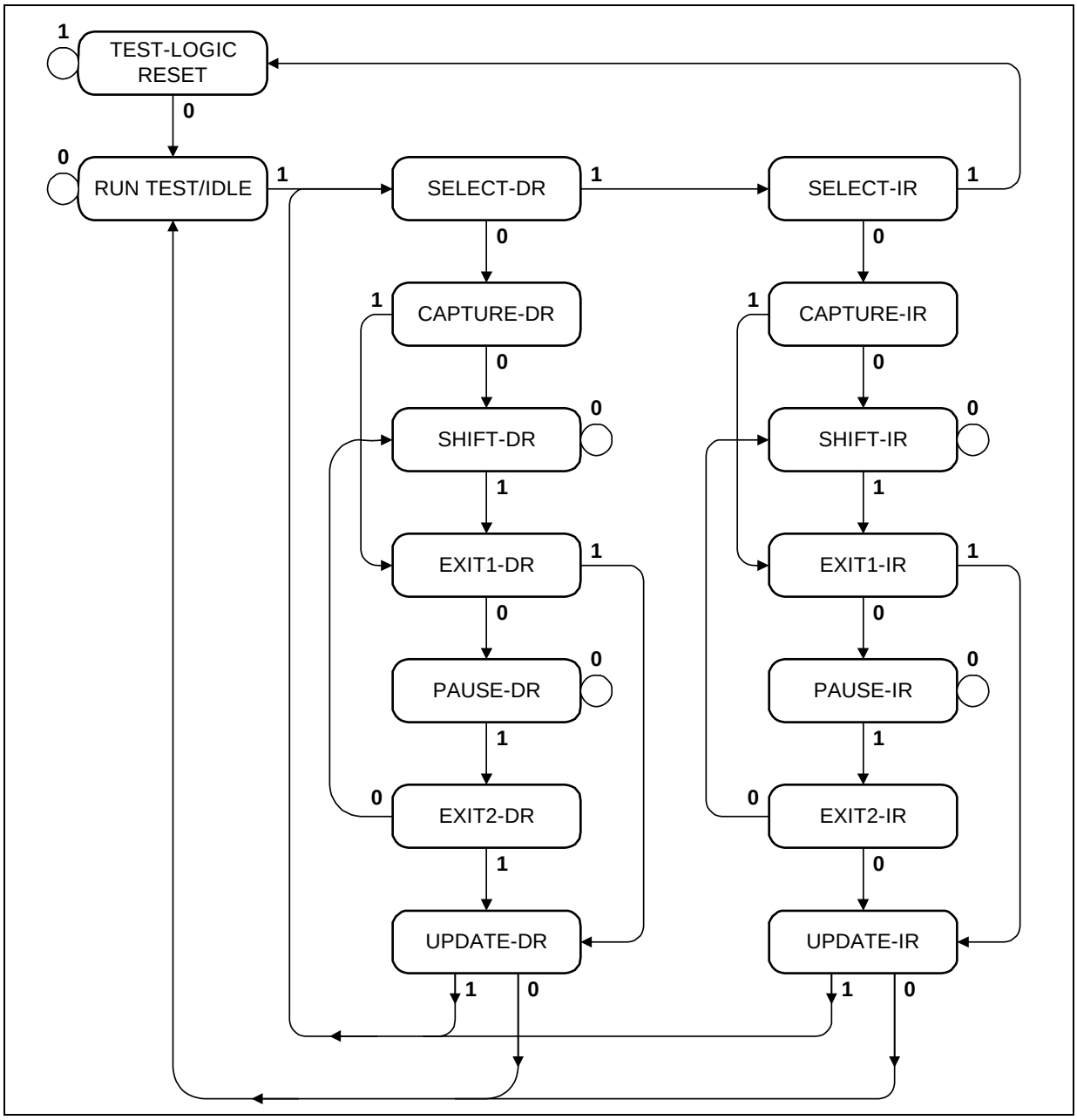
9.3 TAP Controller

The TAP controller is a 16-state synchronous state machine controlled by the TMS input and clocked by TCK (see Figure 16).The TAP controls whether the LXT384 Transceiver is in reset mode, receiving an instruction, receiving data, transmitting data or in an idle state. Table 50 describes in detail each of the states represented in Figure 16.

Table 50. TAP State Description

State	Description
Test Logic Reset	In this state the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run -Test / Idle	The TAP controller stays in this state as long as TMS is Low. Used to perform tests.
Capture - DR	The Boundary Scan Data Register (BSR) is loaded with input pin data.
Shift - DR	Shifts the selected test data registers by one stage toward its serial output.
Update - DR	Data is latched into the parallel output of the BSR when selected.
Capture - IR	Used to load the instruction register with a fixed instruction.
Shift - IR	Shifts the instruction register by one stage.
Update - IR	Loads a new instruction into the instruction register.
Pause - IR Pause - DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1 - IR Exit1 - DR Exit2 - IR Exit2 - DR	Temporary states that can be used to terminate the scanning process.

Figure 16. JTAG State Diagram



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9.4 JTAG Register Description

The following paragraphs describe each of the registers represented in Figure 15.

9.4.1 Boundary Scan Register (BSR)

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the board. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or tristate pins require more than one position in the register. Table 51 shows the BSR scan cells and their functions. Data into the BSR is shifted in LSB first.

The Analog Test Port can be used to verify continuity across the coupling transformer's primary winding as shown in Figure 17. By applying a stimulus to the AT1 input, a known voltage will appear at AT2 for a given load. This, in effect, tests the continuity of a receive or transmit interface.

Table 51. Boundary Scan Register (BSR) (Sheet 1 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
0	LOOP0	I/O	PADD0	
1	LOOP0	I/O	PDO0	
2	LOOP1	I/O	PADD1	
3	LOOP1	I/O	PDO1	
4	LOOP2	I/O	PADD2	
5	LOOP2	I/O	PDO2	
6	LOOP3	I/O	PADD3	
7	LOOP3	I/O	PDO3	
8	LOOP4	I/O	PADD4	
9	LOOP4	I/O	PDO4	
10	LOOP5	I/O	PADD5	
11	LOOP5	I/O	PDO5	
12	LOOP6	I/O	PADD6	
13	LOOP6	I/O	PDO6	
14	LOOP7	I/O	PADD7	
15	N/A	-	PDOENB	PDOENB controls the LOOP0 through LOOP7 pins. Setting PDOENB to "0" configures the pins as outputs. The output value to the pin is set in PDO[0...7]. Setting PDOENB to "1" tristates all the pins. The input value to the pins can be read in PADD[0...7].
16	LOOP7	I/O	PDO7	
17	TCLK1	I	TCLK1	
18	TPOS1	I	TPOS1	
19	TNEG1	I	TNEG1	
20	RCLK1	O	RCLK1	
21	RPOS1	O	RPOS1	

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Table 51. Boundary Scan Register (BSR) (Sheet 2 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
22	N/A	-	HIZ1	HIZ1 controls the RPOS1, RNEG1 and RCLK1 pins. Setting HIZ1 to “0” enables output on the pins. Setting HIZ1 to “1” tristates the pins.
23	RNEG1	O	RNEG1	
24	LOS1	O	LOS1	
25	TCLK0	I	TCLK0	
26	TPOS0	I	TPOS0	
27	TNEG0	I	TNEG0	
28	RCLK0	O	RCLK0	
29	RPOS0	O	RPOS0	
30	N/A	-	HIZ0	HIZ0 controls the RPOS0, RNEG0 and RCLK0 pins. Setting HIZ0 to “0” enables output on the pins. Setting HIZ0 to “1” tristates the pins.
31	RNEG0	O	RNEG0	
32	LOS0	O	LOS0	
33	MUX	I	MUX	
34	LOS3	O	LOS3	
35	RNEG3	O	RNEG3	
36	N/A	-	HIZ3	HIZ3 controls the RPOS3, RNEG3 and RCLK3 pins. Setting HIZ3 to “0” enables output on the pins. Setting HIZ3 to “1” tristates the pins.
37	RPOS3	O	RPOS3	
38	RCLK3	O	RCLK3	
39	TNEG3	I	TNEG3	
40	TPOS3	I	TPOS3	
41	TCLK3	I	TCLK3	
42	LOS2	O	LOS2	
43	RNEG2	O	RNEG2	
44	N/A	-	HIZ2	HIZ2 controls the RPOS2, RNEG2 and RCLK2 pins. Setting HIZ2 to “0” enables output on the pins. Setting HIZ2 to “1” tristates the pins.
45	RPOS2	O	RPOS2	
46	RCLK2	O	RCLK2	
47	TNEG2	I	TNEG2	
48	TPOS2	I	TPOS2	
49	TCLK2	I	TCLK2	
50	$\overline{\text{INT}}$	O	INT	
51	N/A	-	SDOACKENB	SDOACKENB controls the $\overline{\text{ACK}}$ pin. Setting SDOACKEN to “0” enables output on $\overline{\text{ACK}}$ pin. Setting SDOACKEN to “1” tristates the pin.
52	$\overline{\text{ACK}}$	O	ACK	

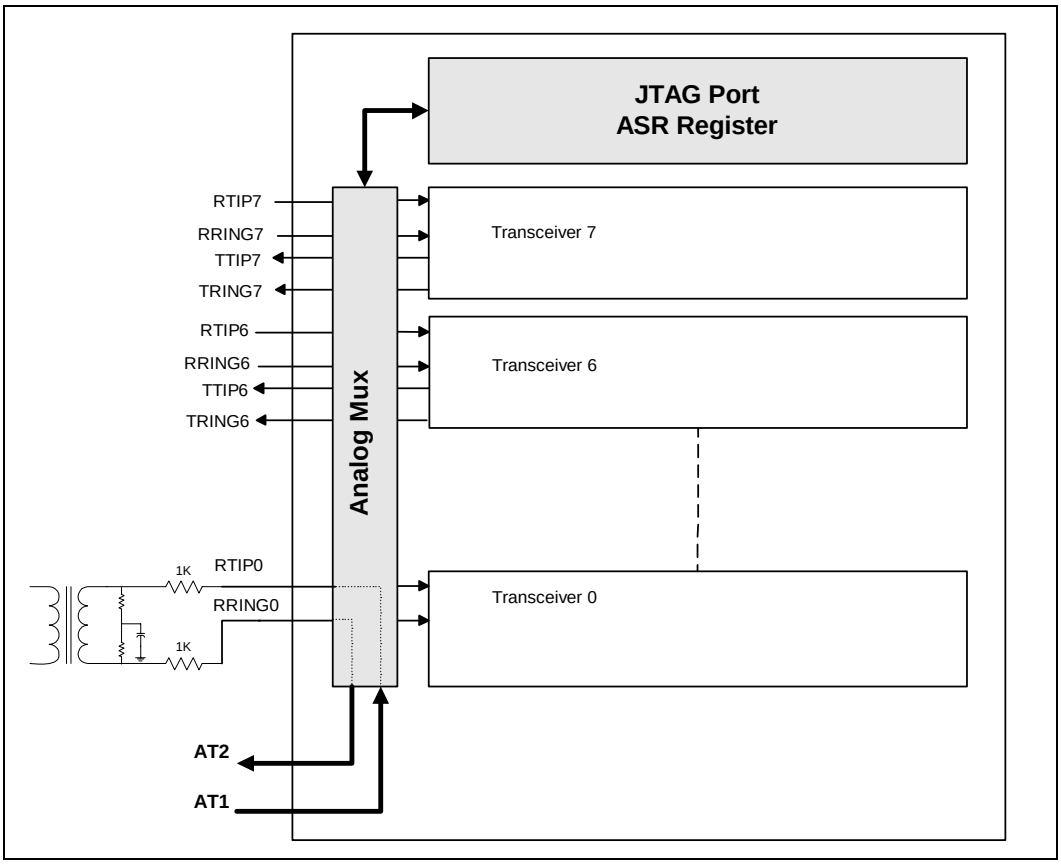
Table 51. Boundary Scan Register (BSR) (Sheet 3 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
53	$\overline{DS}$	I	WRB	
54	R/$\overline{W}$	I	RDB	
55	ALE	I	ALE	
56	$\overline{CS}$	I	CSB	
57	$\overline{MOT}$/INTL	I	MOTO	
58	TCLK5	I	TCLK5	
59	TPOS5	I	TPOS5	
60	TNEG5	I	TNEG5	
61	RCLK5	O	RCLK5	
62	RPOS5	O	RPOS5	
63	N/A	-	HIZ5	HIZ5 controls the RPOS5, RNEG5 and RCLK5 pins. Setting HIZ5 to “0” enables output on the pins. Setting HIZ5 to “1” tristates the pins.
64	RNEG5	O	RNEG5	
65	LOS5	O	LOS5	
66	TCLK4	I	TCLK4	
67	TPOS4	I	TPOS4	
68	TNEG4	I	TNEG4	
69	RCLK4	O	RCLK4	
70	RPOS4	O	RPOS4	
71	N/A	-	HIZ4	HIZ4 controls the RPOS4, RNEG4 and RCLK4 pins. Setting HIZ4 to “0” enables output on the pins. Setting HIZ4 to “1” tristates the pins.
72	RNEG4	O	RNEG4	
73	LOS4	O	LOS4	
74	OE	I	OE	
75	CLKE	I	CLKE	
76	LOS7	O	LOS7	
77	RNEG7	O	RNEG7	
78	N/A	-	HIZ7	HIZ7 controls the RPOS7, RNEG7 and RCLK7 pins. Setting HIZ7 to “0” enables output on the pins. Setting HIZ7 to “1” tristates the pins.
79	RPOS7	O	RPOS7	
80	RCLK7	O	RCLK7	
81	TNEG7	I	TNEG7	
82	TPOS7	I	TPOS7	
83	TCLK7	I	TCLK7	
84	LOS6	O	LOS6	
85	RNEG6	O	RNEG6	

Table 51. Boundary Scan Register (BSR) (Sheet 4 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
86	N/A	-	HIZ6	HIZ6 controls the RPOS6, RNEG6 and RCLK6 pins. Setting HIZ6 to “0” enables output on the pins. Setting HIZ6 to “1” tristates the pins.
87	RPOS6	O	RPOS6	
88	RCLK6	O	RCLK6	
89	TNEG6	I	TNEG6	
90	TPOS6	I	TPOS6	
91	TCLK6	I	TCLK6	
92	MCLK	I	MCLK	
93	MODE	I	MODE	
94	A4	I	A4	
95	A3	I	A3	
96	A2	I	A2	
97	A1	I	A1	
98	A0	I	A0	

Figure 17. Analog Test Port Application



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9.4.2 Analog Port Scan Register (ASR)

The ASR is a 5 bit shift register used to control the analog test port at pins AT1, AT2. When the INTEST_ANALOG instruction is selected, TDI connects to the ASR input and TDO connects to the ASR output. After 5 TCK rising edges, a 5 bit control code is loaded into the ASR. Data into the ASR is shifted in LSB first.

Table 52 shows the 16 possible control codes and the corresponding operation on the analog port.

Table 52. Analog Port Scan Register (ASR)

ASR Control Code	AT1 Forces Voltage To:	AT2 Senses Voltage From:
11111	TTIP0	TRING0
11110	TTIP1	TRING1
11101	TTIP2	TRING2
11100	TTIP3	TRING3
11011	TTIP4	TRING4
11010	TTIP5	TRING5
11001	TTIP6	TRING6
11000	TTIP7	TRING7
10111	RTIP0	RRING0
10110	RTIP1	RRING1
10101	RTIP2	RRING2
10100	RTIP3	RRING3
10011	RTIP4	RRING4
10010	RTIP5	RRING5
10001	RTIP6	RRING6
10000	RTIP7	RRING7

9.4.3 Device Identification Register (IDR)

The IDR register provides access to the manufacturer number, part number and the LXT384 Transceiver revision. The register is arranged per IEEE 1149.1 and is represented in Table 53. Data into the IDR is shifted in LSB first.

Table 53. Device Identification Register (IDR)

Bit #	Comments
31 - 28	Revision number
27 - 12	Part number
11 - 1	Manufacturer number
0	Set to “1”

9.4.4 Bypass Register (BYR)

The Bypass Register is a 1 bit register that allows direct connection between the TDI input and the TDO output.

9.4.5 Instruction Register (IR)

The IR is a 3 bit shift register that loads the instruction to be performed. The instructions are shifted LSB first. Table 54 shows the valid instruction codes and the corresponding instruction description.

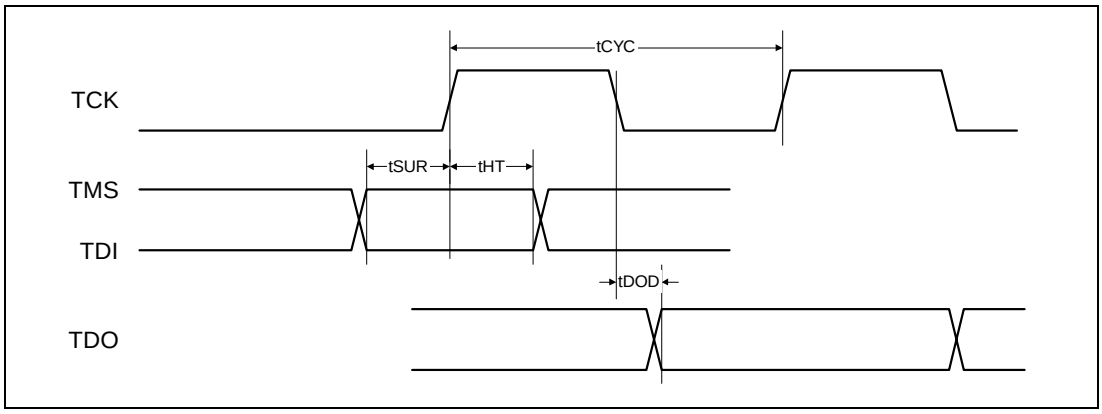
Table 54. Instruction Register (IR)

Instruction	Code #	Comments
EXTEST	000	Connects the BSR to TDI and TDO. Input pins values are loaded into the BSR. Output pins values are loaded from the BSR.
INTEST_ANALOG	010	Connects the ASR to TDI and TDO. Allows voltage forcing/sensing through AT1 and AT2. Refer to Table 52.
SAMPLE / PRELOAD	100	Connects the BSR to TDI and TDO. The normal path between the LXT384 Transceiver logic and the I/O pins is maintained. The BSR is loaded with the signals in the I/O pins.
IDCODE	110	Connects the IDR to the TDO pin.
BYPASS	111	Serial data from the TDI input is passed to the TDO output through the 1 bit Bypass Register.

Table 55. JTAG Timing Characteristics

Parameter	Sym	Min.	Typ	Max	Unit	Test Conditions
Cycle time	Tcyc	200	-	-	ns	
J-TMS/J-TDI to J-TCK rising edge time	Tsut	50	-	-	ns	
J-CLK rising to J-TMS/L-TDI hold time	Tht	50	-	-	ns	
J-TCLK falling to J-TDO valid	Tdod	-	-	50	ns	

Figure 18. JTAG Timing



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10.0 Electrical Characteristics

The tables in this chapter specify the electrical characteristics of the LXT384 Transceiver. The specifications are guaranteed by test except, where noted, by design. The minimum and maximum values listed are guaranteed over the specified recommended operating conditions.

Table 56 lists the absolute maximum ratings for the LXT384 Transceiver.

Table 56. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Voltages and Power				
DC supply core voltage for VCC1:0 and VCCIO1:0 (referenced to ground)	V_{CC} and V_{CCIO}	-0.5	4.0	V
DC supply I/O voltage for TVCC7:0 (referenced to ground)	TV_{CC}	-0.5	7.0	V
Input voltage on any digital pin	V_{IN}	GND - 0.5	5.5	V
Input voltage on RTIP, RRING[1]	V_{IN}	GND - 0.5	VCC0 + 0.5 VCC1 + 0.5	V
ESD voltage on any pin [2]	V_{IN}	2000		V
Maximum power dissipation in package	P_{Max}		1.6	W
Currents				
Transient latch-up current on any pin	I_{IN}		100	mA
Input current on any digital pin [3]	I_{IN}	-10	10	mA
DC input current on TTIP, TRING [3]	I_{IN}		±100	mA
DC input current on RTIP, RRING [3]	I_{IN}		±100	mA
Temperatures				
Storage temperature	T_{STG}	-65	+150	°C
Case temperature, LQFP	T_{CASE}		120	°C
Case temperature, PBGA	T_{CASE}		120	°C

Caution: Exceeding these values can cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods can affect the device reliability.

1. Referenced to ground.
2. ESD sensitivity classification: Human body model
3. Constant input current.

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Table 57 lists recommended values for LXT384 Transceiver operating conditions.

Table 57. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Ambient operating temperature	T_A	-40	25	+85	°C
Average digital power supply current [1, 2]	I_{VCC}		90	120	mA
Output load at TTIP and TRING	R_L	25			Ω
DC Supply Voltages					
DC supply core voltage for VCC1:0 and VCCIO1:0 (referenced to ground)	V_{CC}	3.14	3.30	3.47	V
DC supply voltage rise time [3]	V_{CC}	0		25	ms
DC supply voltage for TVCC7:0 = 5-V nominal	TV_{CC}	4.75	5.0	5.25	V
DC supply voltage for TVCC7:0 = 3.3-V nominal	TV_{CC}	3.14	3.30	3.47	V

1. Current consumption over full range of the operating temperature and power supply voltage for the LXT384 Transceiver. Includes all channels.
2. Digital inputs are within 10% of the supply rails, and digital outputs are driving a 50-pF load.
3. If the DC supply voltage rise time exceeds 25 ms, see the LXT384 Transceiver application note on slow power-up rise time referenced in Chapter 1.0, “Introduction to this Document”.

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Table 58 lists power consumption values for the LXT384 Transceiver.

Table 58. Intel® LXT384 Transceiver Power Consumption

Mode	TVCC	Load	LEN			Typ	Max[1]
E1	3.3V	75 Ω	000	-	-	760	-
				-	-	1270	1420
		120 Ω	000	-	-	640	-
				-	-	1110	1280
T1[2]	3.3V	100 Ω	101-111	-	-	1020	-
				-	-	1820	2100
E1	5.0V	75 Ω	000	-	-	1000	-
				-	-	1730	1940
		120 Ω	000	-	-	820	-
				-	-	1500	1730
T1[2]	5.0V	100 Ω	101-111	-	-	1400	-
				-	-	2670	2960

The LXT384 transceiver dissipates power in two ways:

- Power dissipation of the transceiver itself.
- Load power dissipation on external resistors and capacitors.

The maximum load power (current draw) for the LXT384 transceiver is the sum of these two power dissipation factors.

Table 59 lists load power consumption values. Load includes the power being dissipated in the two RT resistors, the termination resistor, cables, and the transformer.

Table 59. Load[3] Power Consumption

		Transmit 1:2 Transformer		Transmit 1:1.7 Transformer			
Parameter		Typical	Maximum[1,2]	Typical	Maximum[1,2]	Unit	Test Condition
TVCC	Load						
3.3V	75Ω	760				mW	50% marks (1:1)
		1270	1420			mW	100% ones (marks)
	120Ω	640				mW	50% marks (1:1)
		1110	1280			mW	100% ones (marks)
5.0V (1:2 transformer)	75Ω	1000				mW	50% marks (1:1)
		1730	1940			mW	100% ones (marks)
	120Ω	820				mW	50% marks (1:1)
		1500	1730			mW	100% ones (marks)
5.0V (Low power - 1:1.17 transformer)	75Ω	850				mW	50% marks (1:1)
		1450	1650			mW	100% ones (marks)
	120Ω	700				mW	50% marks (1:1)
		1260	1450			mW	100% ones (marks)

1. Current consumption over full range of the operating temperature and power supply voltage for the LXT384 Transceiver. Includes all channels.
2. Power consumption includes power absorbed by the line load external to the LXT384 Transceiver drivers.
3. Load includes the power being dissipated in the two RT resistors, the termination resistor, cables, and transformer

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Table 60 lists the DC characteristics for the LXT384 Transceiver.

Table 60. DC Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Test Condition
Low-level input voltage	V_{IL}			0.8	V	
High-level input voltage	V_{IH}	2.0			V	
Low-level output voltage[1]	V_{OL}	0.0		0.4	V	I_{OUT} = 1.6 mA
High-level output voltage[1]	V_{OH}	2.4		VCCIO	V	I_{OUT} = 400 µA
TTIP, TRING - output current	I_{HZ}			+/- 1	µA	
HIgh-impedance tristate leakage current	Ihz	-10		+10	µA	
Input leakage current	Iil	-10		+10	µA	
Tristate output current	Ihz	–	–	1	µA	TTIP, TRING
Line short circuit current	–	–	–	50	mA RMS	2 x 11 Ω series resistors and 1:2 transformer
Input leakage	TMS TDI $\overline{TRST}$	–	–	50	µA	
Special Input Conditions for JASEL, LOOP7:0, and MODE						
High-level input voltage	V_{INH}	(2/3 VCC) + 0.2[2]			V	
Low-level input current	I_{INL}			50	µA	
High-level input current	I_{INH}			50	µA	

1. Output drivers output CMOS logic levels into CMOS loads.
2. VCC supply refers to VCC0 or VCC1 only.

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Table 61 (E1) and Table 62 (T1) list the AC characteristics for the LXT384 Transceiver transmitter.

Table 61. Intel® LXT384 Transceiver E1 Transmit Transmission Characteristics

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Output pulse amplitude	75Ω 120Ω	–	2.14 2.7	2.37 3.0	2.60 3.3	V V	Tested at the line side
Peak voltage of a space	75Ω 120Ω	–	-0.237 -0.3		0.237 0.3	V V	
Transmit amplitude variation with supply		–	-1		+1	%	
Difference between pulse sequences		–			200	mV	For 17 consecutive pulses
Pulse width ratio of the positive and negative pulses		–	0.95		1.05		At the nominal half amplitude
Transmit transformer turns ratio for 75/120Ω characteristic impedance		–		1:2			Rt = 11 Ω ± 1%
Transmit return loss 75 Ω coaxial cable[1]	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	17 17 17	–	dB dB dB	Using components in the LXD384 evaluation board.
Transmit return loss 120 Ω twisted pair cable[1]	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	20 20 20	–	dB dB dB	Using components in the LXD384 evaluation board
Transmit intrinsic jitter: 20Hz to 100kHz		–	–	0.030	0.050	U.I.	Tx path TCLK is jitter free
Transmit path delay	Bipolar mode			2		U.I.	JA Disabled
	Unipolar mode			7		U.I.	

1. Guaranteed by design and other correlation methods.

Table 62. Intel® LXT384 Transceiver T1 Transmit Transmission Characteristics (Sheet 1 of 2)

Parameter	Sym	Min.	Typ	Max	Unit	Test Condition
Output pulse amplitude	–	2.4	3.0	3.6	V	Measured at the DSX
Peak voltage of a space	–	-0.15	–	+0.15	V	
Driver output impedance[1]	–	–	1	–	Ω	@ 772 KHz
Transmit amplitude variation with power supply	–	-1	–	+1	%	
Ratio of positive to negative pulse amplitude	–	0.95	–	1.05	–	T1.102, isolated pulse
Difference between pulse sequences	–	–	–	200	mV	For 17 consecutive pulses, GR-499-CORE
Pulse width variation at half amplitude	–	–	–	20	ns	
Jitter added by Transmitter[1] 10Hz - 8KHz 8KHz - 40KHz 10Hz - 40KHz Wide Band	–	–	–	0.020 0.025 0.025 0.050	UI_{pk-pk}	AT&T Pub 62411 TCLK is jitter free

1. Guaranteed by design and other correlation methods.
2. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

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Table 62. Intel® LXT384 Transceiver T1 Transmit Transmission Characteristics (Sheet 2 of 2)

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Output power levels[2]	@ 772 KHz @ 1544 KHz	–	12.6 -29	–	17.9	dBm dBm	T1.102 - 1993 Referenced to power at 772 KHz
Transmit Return Loss [1]	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	21 21 21	–	dB dB dB	With transmit series resistors (TVCC=5V). Using components in the LXD384 evaluation board.
Transmit path delay	Bipolar mode			2		U.I.	JA Disabled
	Unipolar mode			7		U.I.	

1. Guaranteed by design and other correlation methods.
2. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 63 (E1) and Table 64(T1) list the AC characteristics for the LXT384 Transceiver receiver.

Table 63. Intel® LXT384 Transceiver E1 Receive Transmission Characteristics

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	–	Vp	
Signal to noise interference margin		S/I	-15	–	–	dB	Per G.703, O.151 @ 6 dB cable Attenuation
Data decision threshold		SRE	43	50	57	%	Relative to peak input voltage
Data slicer threshold		–	–	150	–	mV	
Loss of signal threshold		–	–	200	–	mV	
LOS hysteresis		–	–	50	–	mV	
Consecutive zeros before loss of signal		–	–	32 2048	–	–	G.775 recommendation ETSI 300 233 specification
LOS reset		–	12.5%	–	–	–	1's density
Low limit input jitter tolerance [1]	1Hz to 20Hz 20Hz to 2.4kHz 18kHz to 100kHz	–	36 1.5 0.2	–	–	U.I. U.I. U.I.	G735 recommendation Note 1 Cable Attenuation is 6 dB
Differential receiver input impedance		–	–	70	–	k Ω	@1.024 MHz
Input termination resistor tolerance		–	–	–	±1	%	
Common mode input impedance to ground		–	–	20	–	k Ω	
Input return loss[1]	51 kHz - 102 kHz 102 - 2048 kHz 2048kHz - 3072 kHz	–	20 20 20		–	dB dB dB	Measured against nominal impedance using components in the LXD384 evaluation board.
LOS delay time		–	–	30	–	µs	Data recovery mode
LOS reset		–	10	–	255	marks	Data recovery mode
Receive intrinsic jitter, RCLK output		–	–	0.040	0.0625	U.I.	Wide band jitter
Receive path delay	Bipolar mode			1		U.I.	JA Disabled
	Unipolar mode			6		U.I.	

1. Guaranteed by design and other correlation methods.

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Table 64. Intel® LXT384 Transceiver T1 Receive Transmission Characteristics

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@ 772 KHz
Receiver dynamic range		DR	0.5	–	–	Vp	
Signal to noise interference margin		S/I	-16.5	–	–	dB	@ 655 ft. of 22 ABAM cable
Data decision threshold		SRE	63	70	77	%	Relative to peak input voltage
Data slicer threshold		–	–	150	–	mV	
Loss of signal threshold		–	–	200	–	mV	
LOS hysteresis		–	–	50	–	mV	
Consecutive zeros before loss of signal		–	100	175	250	–	T1.231 - 1993
LOS reset		–	12.5%	–	–	–	1's density
Low limit input jitter tolerance [1]	0.1Hz to 1Hz 4.9Hz to 300Hz 10KHz to 100KHz	-	138 28 0.4	-	-	U.I. U.I. U.I.	AT&T Pub. 62411
Differential receiver input impedance		-	-	70	-	k Ω	@772 kHz
Input termination resistor tolerance		-	-		±1	%	
Common mode input impedance to ground		-	-	20	-	k Ω	
Input return loss[1]	51 KHz - 102 KHz 102 - 2048 KHz 2048 KHz - 3072 KHz	-	20 20 20	-	-	dB dB dB	Measured against nominal impedance. Using components in the LXD384 evaluation board.
LOS delay time		-	-	30	-	µs	Data recovery mode
LOS reset		-	10	-	255	-	Data recovery mode
Receive intrinsic jitter, RCLK output[1]		-	-	0.035	0.0625	U.I.	Wide band jitter
Receive path delay	Bipolar mode			1		U.I.	JA Disabled
	Unipolar mode			6		U.I.	

1. Guaranteed by design and other correlation methods.

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11.0 Timing Characteristics

This chapter discusses the following timing characteristics:

- Section 11.1, “Intel® LXT384 Transceiver Timing”
- Section 11.2, “Host Processor Mode - Parallel Interface Timing”
  - Section 11.2.1, “Intel® Processor - Parallel Interface Timing”
  - Section 11.2.2, “Motorola* Processor - Parallel Interface Timing”
- Section 11.3, “Host Processor Mode - Serial Interface Timing”

11.1 Intel® LXT384 Transceiver Timing

Table 65 lists transmit timing characteristics for the LXT384 Transceiver.

Table 65. Intel® LXT384 Transceiver Transmit Timing Characteristics

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Master clock frequency	E1	MCLK	–	2.048	–	MHz	
	T1	MCLK	–	1.544	–	MHz	
Master clock tolerance		–	-100	–	100	ppm	
Master clock duty cycle		–	40	–	60	%	
Output pulse width	E1	Tw	219	244	269	ns	
	T1	Tw	291	324	356	ns	
Transmit clock frequency	E1	Tclke1	-	2.048	-	MHz	
	T1	Tclkt1	-	1.544	-	MHz	
Transmit clock tolerance		Tclkt	-50	–	+50	ppm	
Transmit clock burst rate		Tclkb	-	–	20	MHz	Gapped transmit clock
Transmit clock duty cycle		Tdc	10	–	90	%	NRZ mode
E1 TPOS/TNEG pulse width (RZ mode)		Tmpwe1	236	–	252	ns	RZ mode (TCLK = H for >16 clock cycles)
TPOS/TNEG to TCLK setup time		Tsut	20	-	-	ns	
TCLK to TPOS/TNEG hold time		Tht	20	-	-	ns	
Delay time OE Low to driver High Z		Toez	-	-	1	µs	
Delay time TCLK Low to driver High Z		Ttz	50	60	75	µs	

Figure 19 is a transmit timing diagram for the LXT384 Transceiver.

Figure 19. Intel® LXT384 Transceiver - Transmit Timing

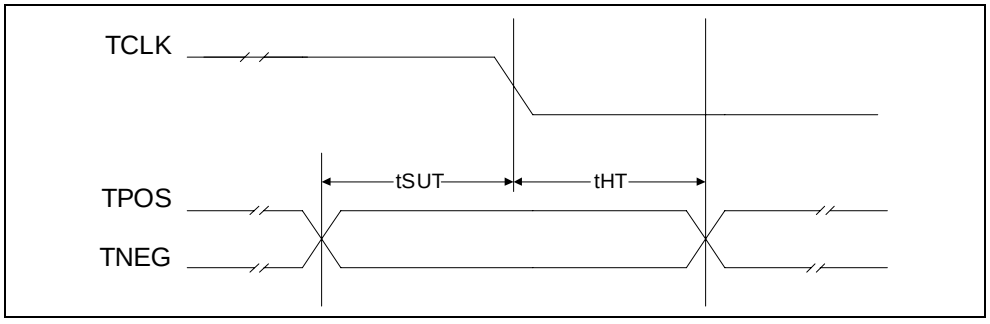

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Table 66 lists receive timing characteristics for the LXT384 Transceiver.

Table 66. Intel® LXT384 Transceiver Receive Timing Characteristics

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Clock recovery capture range	E1	–	–	±80	–	ppm	Relative to nominal frequency MCLK = ±100 ppm
	T1	–	–	±180	–	ppm	
Receive clock duty cycle [1]		Rckd	40	50	60	%	
Receive clock pulse width [1]	E1	Tpw	447	488	529	ns	
	T1	Tpw	583	648	713	ns	
Receive clock pulse width Low time	E1	Tpwl	203	244	285	ns	
	T1	Tpwl	259	324	389	ns	
Receive clock pulse width High time	E1	Tpwh	203	244	285	ns	
	T1	Tpwh	259	324	389	ns	
Rise/fall time [4]		Tr	20	–	–	ns	@ CL=15 pF
RPOS/RNEG pulse width (MCLK=H) [2]	E1	Tpwdl	200	244	300	ns	
	T1	Tpwdl	250	324	400	ns	
RPOS/RNEG to RCLK rising setup time	E1	Tsur	200	244	–	ns	
	T1		200	324	–	ns	
RCLK Rising to RPOS/RNEG hold time	E1	Thr	200	244	–	ns	
	T1		200	324	–	ns	
Delay time between RPOS/RNEG and RCLK		–	–	–	5	ns	MCLK = H [3]

1. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823).
2. Clock recovery is disabled in this mode.
3. If MCLK = H the receive PLLs are replaced by a simple EXOR circuit.
4. For all digital outputs.

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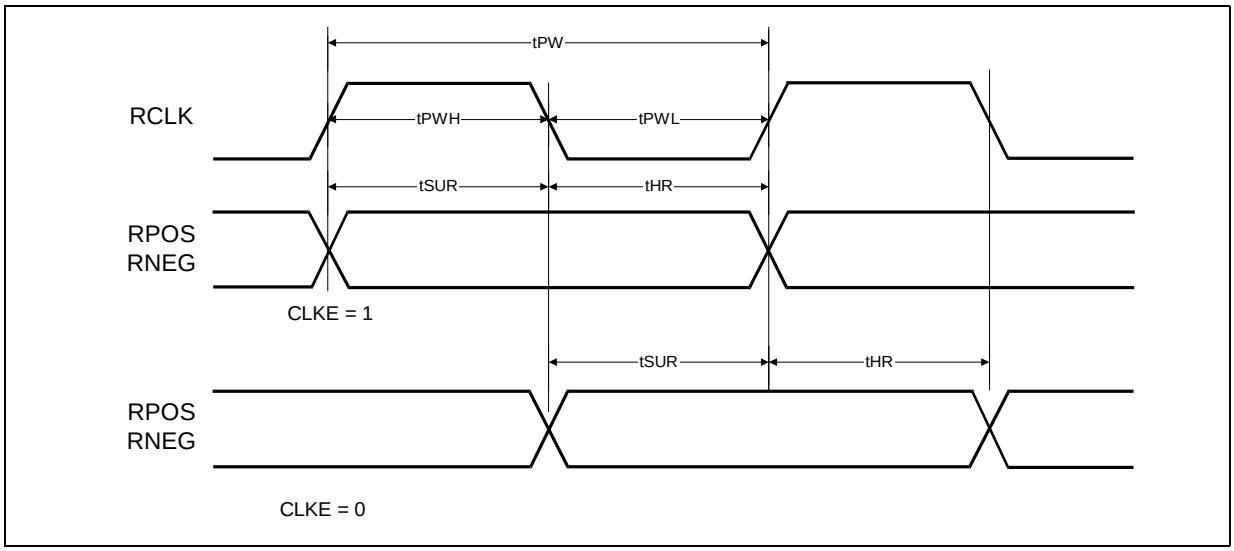
Figure 20 is a receive timing diagram for the LXT384 Transceiver.

Figure 20. Intel® LXT384 Transceiver - Receive Timing



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11.2 Host Processor Mode - Parallel Interface Timing

This sections gives timing characteristics and timing diagrams for both Intel® processors and Motorola processors.

11.2.1 Intel® Processor - Parallel Interface Timing

Table 67 lists read timing characteristics for the Intel® processor.

Table 67. Intel® Processor - Read Timing Characteristics

Parameter	Sym.	Min.[1]	Max.[1]	Unit	Test Conditions
Address setup time to latch	t_{SALR}	10	–	ns	C_{Load} = 100 pF on D7:0. All other outputs are loaded with 50 pF.
Valid address latch pulse width	t_{VL}	30	–	ns	
Latch active to active read setup time	t_{SLR}	10	–	ns	
Chip select setup time to active read	t_{SCSR}	0	–	ns	
Chip select hold time from inactive read	t_{HSCR}	0	–	ns	
Address hold time from inactive ALE	t_{HALR}	5		ns	
Active read to data valid delay time	t_{PRD}	10	50	ns	
Address setup time to $\overline{RD}$ inactive	t_{HAR}	1	–	ns	
Address hold time from $\overline{RD}$ inactive	t_{SAR}	5	–	ns	
Inactive read to data high-impedance tristate delay time	t_{ZRD}	3	35	ns	
Valid read signal pulse width	t_{VRD}	60	–	ns	
Inactive read to inactive $\overline{INT}$ delay time	t_{INT}	–	10	ns	
Active chip select to RDY delay time	t_{DRDY}	0	12	ns	
Active ready low time	t_{VRDY}	–	40	ns	
Inactive ready to high-impedance tristate delay time	t_{RDYZ}	–	3	ns	

1. Minimum and maximum values are at 25 C° and are for design aid only, not guaranteed, and not subject to production testing.

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Figure 21 is a timing diagram for the Intel® processor in the Host Processor mode, with a non-multiplexed interface, and a read cycle takes place.

Figure 21. Intel® Processor Non-Multiplexed Interface - Read Timing

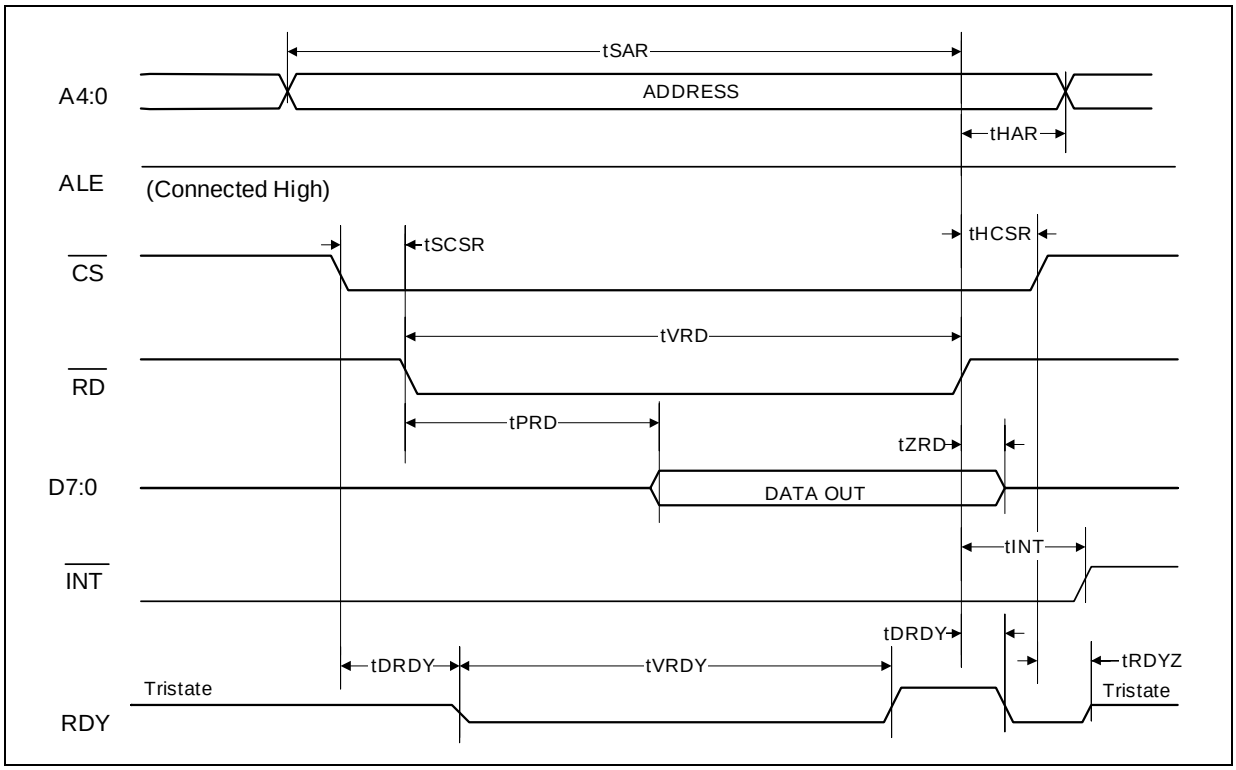

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Figure 22 is a timing diagram for the Intel® processor in the Host Processor mode, with a multiplexed interface, and a read cycle takes place.

Figure 22. Intel® Processor Multiplexed Interface - Read Timing

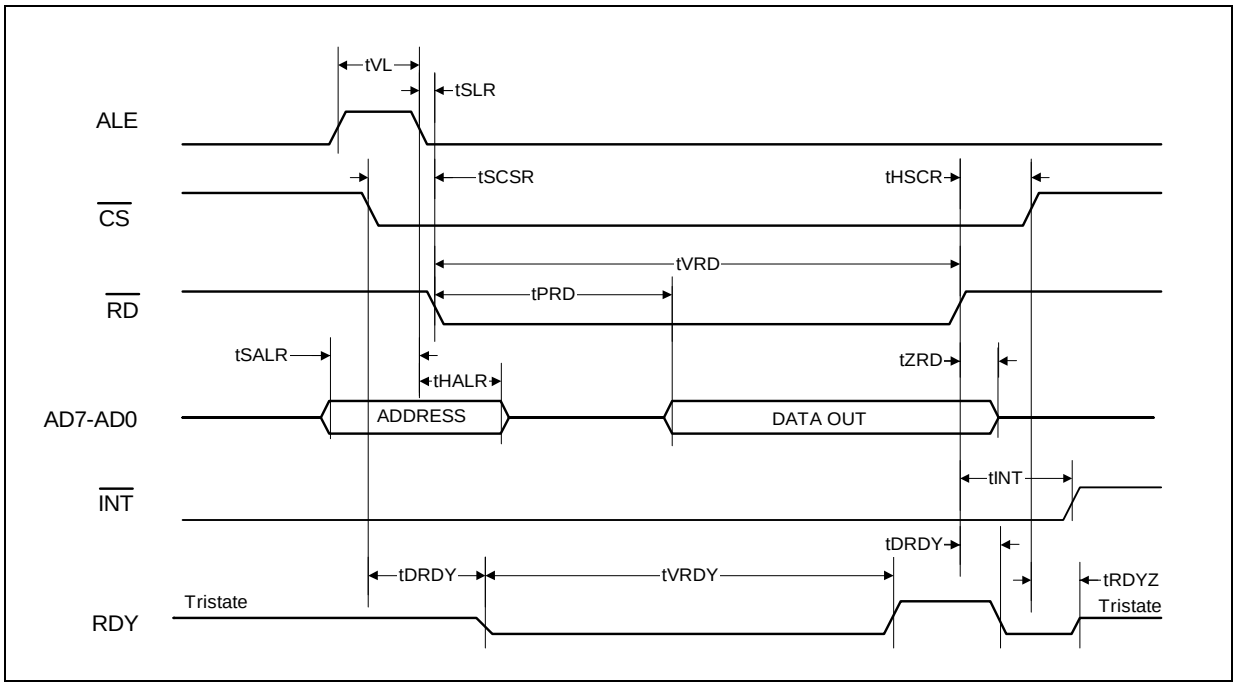

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Table 68 lists write timing characteristics for the Intel® processor.

Table 68. Intel® Processor - Write Timing Characteristics

Parameter	Sym.	Min.[1]	Max.[1]	Unit	Test Conditions
Address setup time to latch	t_{SALW}	10	–	ns	C_{Load} = 100 pF on D7:0. All other outputs are loaded with 50 pF.
Valid address latch pulse width	t_{VL}	30	–	ns	
Latch active to active write setup time	t_{SLW}	10	–	ns	
Chip select setup time to active write	t_{SCSW}	0	–	ns	
Chip select hold time from inactive write	t_{HCSW}	0	–	ns	
Address hold time from inactive ALE	t_{HALW}	5		ns	
Data valid to write active setup time	t_{SDW}	40	–	ns	
Data hold time to active write	t_{HDW}	30	–	ns	
Address setup time to $\overline{WR}$ inactive	t_{HAW}	2	–	ns	
Address hold time from $\overline{WR}$ inactive	t_{SAW}	6	–	ns	
Valid write signal pulse width	t_{VWR}	60	–	ns	
Inactive write to inactive $\overline{INT}$ delay time	t_{INT}	–	10	ns	
Chip select to RDY delay time[2]	t_{DRDY}	0	12	ns	
Low time for active RDY	t_{VRDY}	–	40	ns	
Delay time between inactive RDY to high-impedance tristate[2]	t_{RDYZ}	–	3	ns	

1. Minimum and maximum values are at 25 C° and are for design aid only, not guaranteed, and not subject to production testing.
2. Timing parameters do not apply for Reset Register 0Ah. For details, see Section 7.4.1, “Host Processor Mode - Parallel Interface”.

Figure 23 is a timing diagram for the Intel® processor in the Host Processor mode, with a non-multiplexed interface, and a write cycle takes place.

Figure 23. Intel® Processor Non-Multiplexed Interface - Write Timing

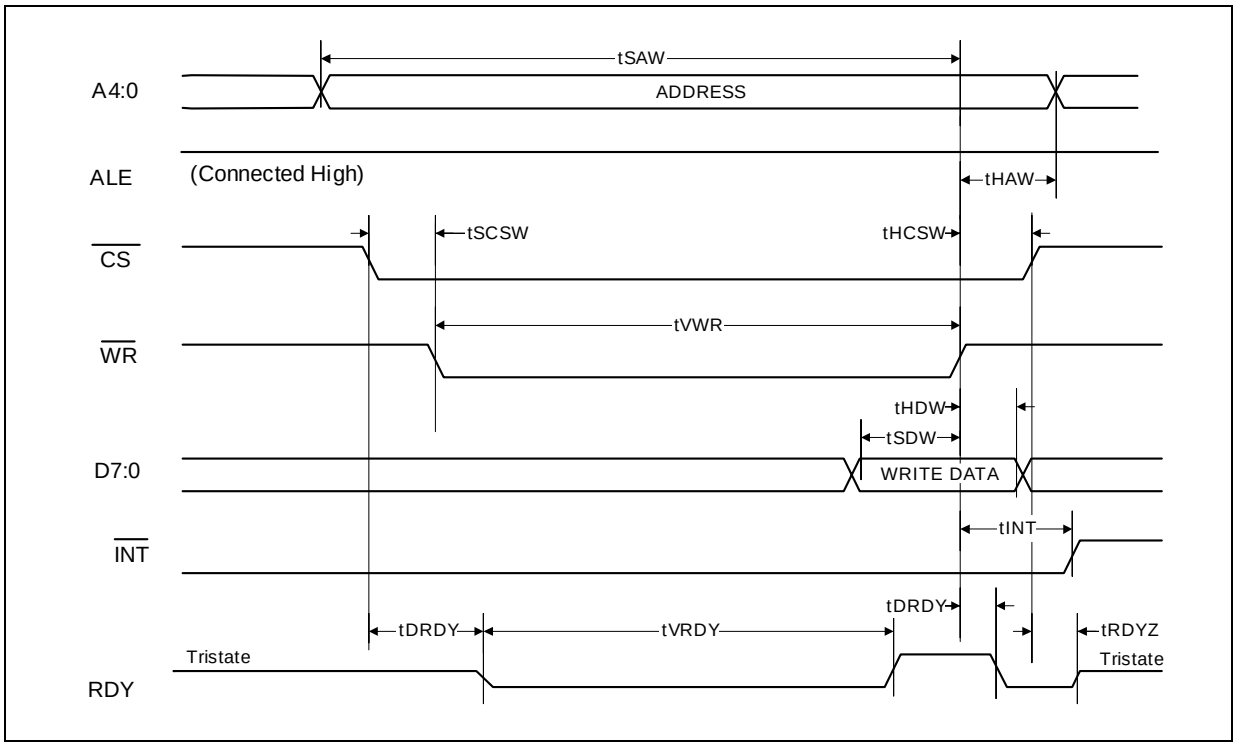

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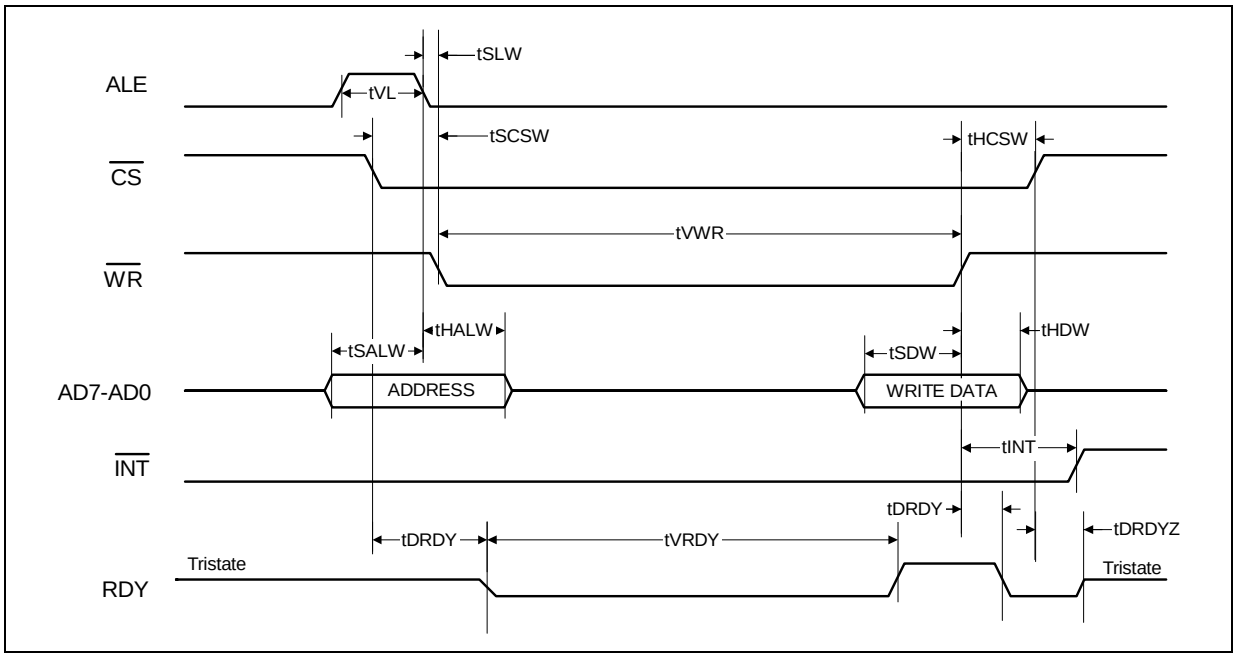
Figure 24 is a timing diagram for the Intel® processor in the Host Processor mode, with a multiplexed interface, and a write cycle takes place.

Figure 24. Intel® Processor Multiplexed Interface - Write Timing



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11.2.2 Motorola* Processor - Parallel Interface Timing

Table 69 lists read timing characteristics for the Motorola processor.

Table 69. Motorola Processor - Read Timing Characteristics

Parameter	Sym.	Min.[1]	Max.[1]	Unit	Test Conditions
Address setup time to address or data strobe	t_{SAR}	10	–	ns	C_L = 100pF on D7:0. All other outputs are loaded with 50 pF.
Address hold time from address or data strobe	t_{HAR}	5	–	ns	
Valid address strobe pulse width	t_{VAS}	95	–	ns	
R/$\overline{W}$ setup time to active data strobe	t_{SRW}	10	–	ns	
R/$\overline{W}$ hold time from inactive data strobe	t_{HRW}	0	–	ns	
Chip select setup time to active data strobe	t_{SCS}	0	–	ns	
Chip select hold time from inactive data strobe	t_{HCS}	0	–	ns	
Address strobe active to data strobe active delay	t_{ASDS}	20	–	ns	
Delay time from active data strobe to valid data	t_{PDS}	3	30	ns	
Delay time from inactive data strobe to data high impedance	t_{DZ}	3	30	ns	
Valid data strobe pulse width	t_{VDS}	60	–	ns	
Inactive data strobe to inactive $\overline{INT}$ delay time	t_{INT}	–	10	ns	
Data strobe inactive to address strobe inactive delay	t_{DSAS}	15	–	ns	
$\overline{DS}$ asserted to $\overline{ACK}$ asserted delay	t_{DACKP}	–	40	ns	
$\overline{DS}$ deasserted to $\overline{ACK}$ deasserted delay	t_{DACK}	–	10	ns	
Active $\overline{ACK}$ to valid data delay	t_{PACK}	–	0	ns	

1. Minimum and maximum values are at 25 C° and are for design aid only, not guaranteed, and not subject to production testing.

Figure 25 is a timing diagram for the Motorola processor in the Host Processor mode, with a non-multiplexed interface, and a read cycle takes place.

Figure 25. Motorola Processor Non-Multiplexed Interface - Read Timing

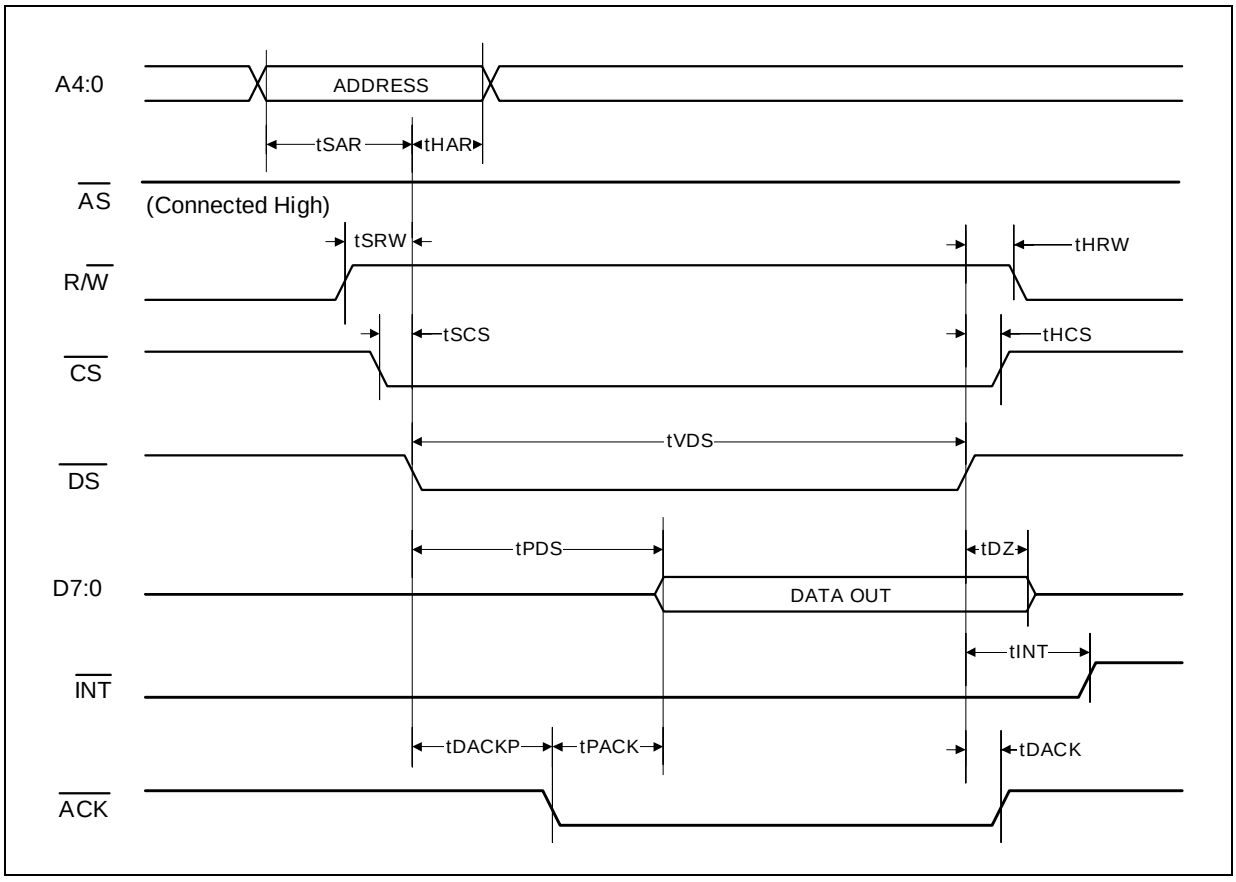

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Figure 26 is a timing diagram for the Motorola processor in the Host Processor mode with a multiplexed interface, and a read cycle takes place.

Figure 26. Motorola Processor Multiplexed Interface - Read Timing

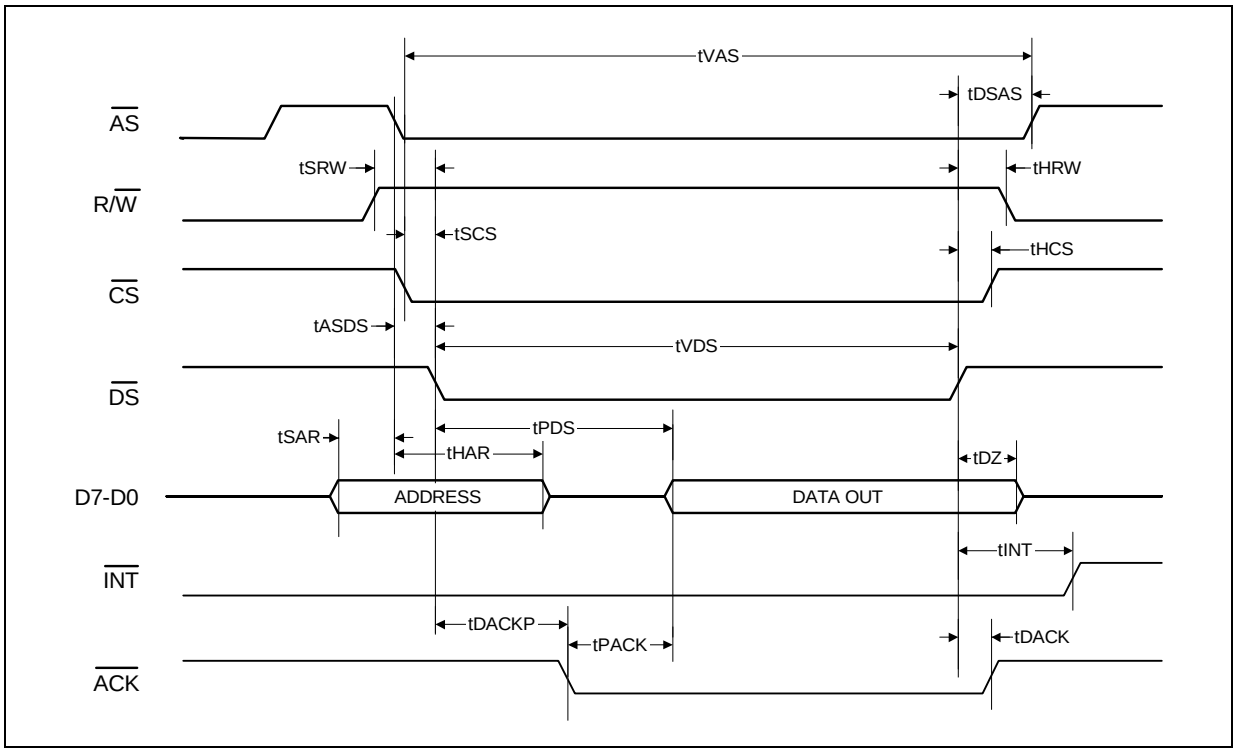

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Table 70 lists write timing characteristics for the Motorola processor.

Table 70. Motorola Processor - Write Timing Characteristics

Parameter	Sym.	Min.[1]	Max.[1]	Unit	Test Conditions
Address setup time to address strobe	t_{SAS}	10	-	ns	C_L= 100 pF on D7:0. All other outputs are loaded with 50 pF.
Address hold time to address strobe	t_{HAS}	5	-	ns	
Valid address strobe pulse width	t_{VAS}	95	-	ns	
R/$\overline{W}$ setup time to active data strobe	t_{SRW}	10	-	ns	
R/$\overline{W}$ hold time from inactive data strobe	t_{HRW}	0	-	ns	
Chip select setup time to active data strobe	t_{SCS}	0	-	ns	
Chip select hold time from inactive data strobe	t_{HCS}	0	-	ns	
Address strobe active to data strobe active delay	t_{ASDS}	20	-	ns	
Data setup time to $\overline{DS}$ deassertion	t_{SDW}	40	-	ns	
Data hold time from $\overline{DS}$ deassertion	t_{HDW}	30	-	ns	
Valid data strobe pulse width	t_{VDS}	60	-	ns	
Inactive data strobe to inactive $\overline{INT}$ delay time	t_{INT}	-	10	ns	
Data strobe inactive to address strobe inactive delay	t_{DSAS}	15	-	ns	
Active data strobe to $\overline{ACK}$ output enable time	t_{DACK}	0	12	ns	
$\overline{DS}$ asserted to $\overline{ACK}$ asserted delay	t_{DACKP}	-	40	ns	

1. Minimum and maximum figures are at 25 C° and are for design aid only, not guaranteed, and not subject to production testing.

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Figure 27 is a timing diagram for the Motorola processor in the Host Processor mode, with a non-multiplexed interface, and a write cycle takes place.

Figure 27. Motorola Processor Non-Multiplexed Interface - Write Timing

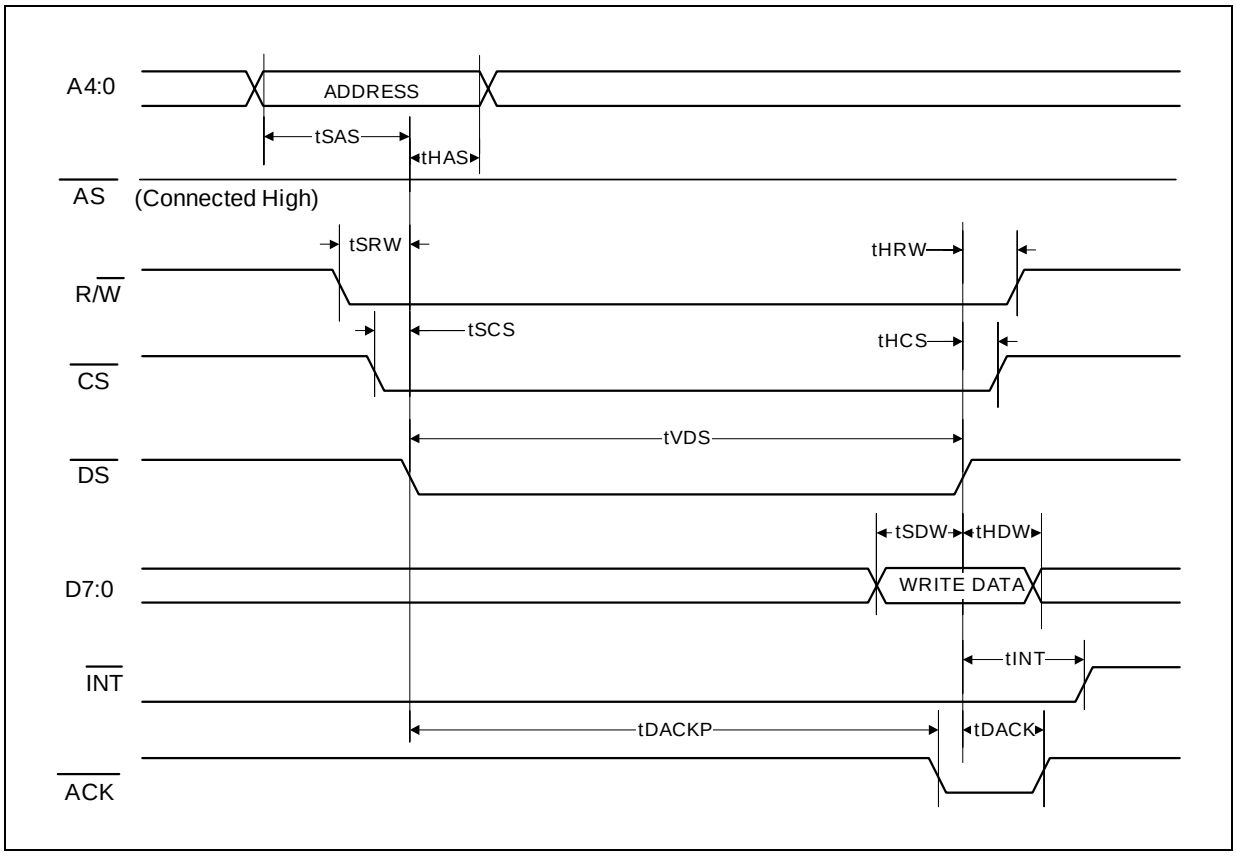

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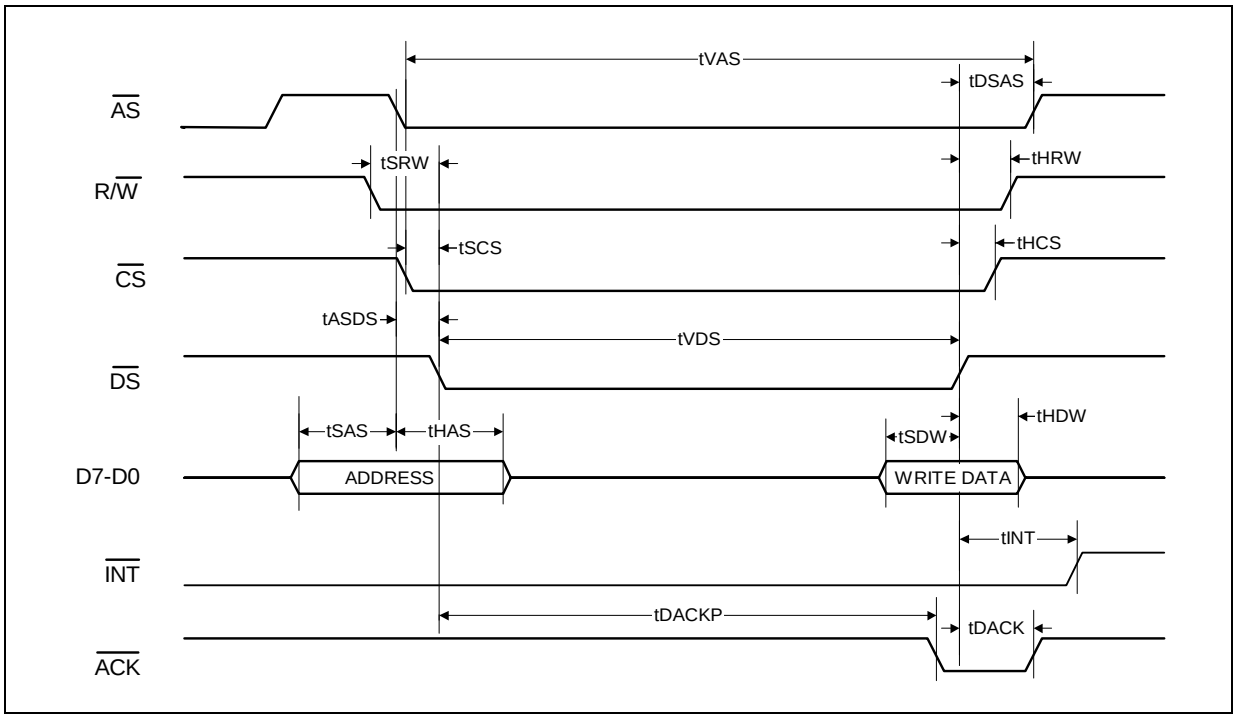
Figure 28 is a timing diagram for the Motorola processor in the Host Processor mode, with a multiplexed interface, and a write cycle takes place.

Figure 28. Motorola Processor Multiplexed Interface - Write Timing



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11.3 Host Processor Mode - Serial Interface Timing

Table 71 lists serial I/O timing for a Motorola or Intel® processor in the Host Processor mode with a serial interface.

Table 71. Serial I/O Timing Characteristics

Parameter	Sym.	Min.	Typ.[1]	Max.	Unit	Test Condition
Rise/fall time any pin	Trf			100	ns	C_{Load} = 1.6 mA, 50 pF
SDI to SCLK setup time	Tdc	5			ns	
SCLK to SDI hold time	Tcdh	5			ns	
SCLK low time	Tcl	25			ns	
SCLK high time	Tch	25			ns	
SCLK rise and fall time	Tr, Tf			50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	Tcc	10			ns	
Last SCLK edge to $\overline{CS}$ rising edge	Tcch	10			ns	
$\overline{CS}$ inactive time	Tcwh	50			ns	
SCLK to SDO valid delay time	Tcdv			5	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high impedance	Tcdz		10		ns	

1. Typical figures are at 25 C° and are for design aid only, not guaranteed, and not subject to production testing.

Figure 29 is a timing diagram for serial input to the Host Processor interface.

Figure 29. Serial Input Timing

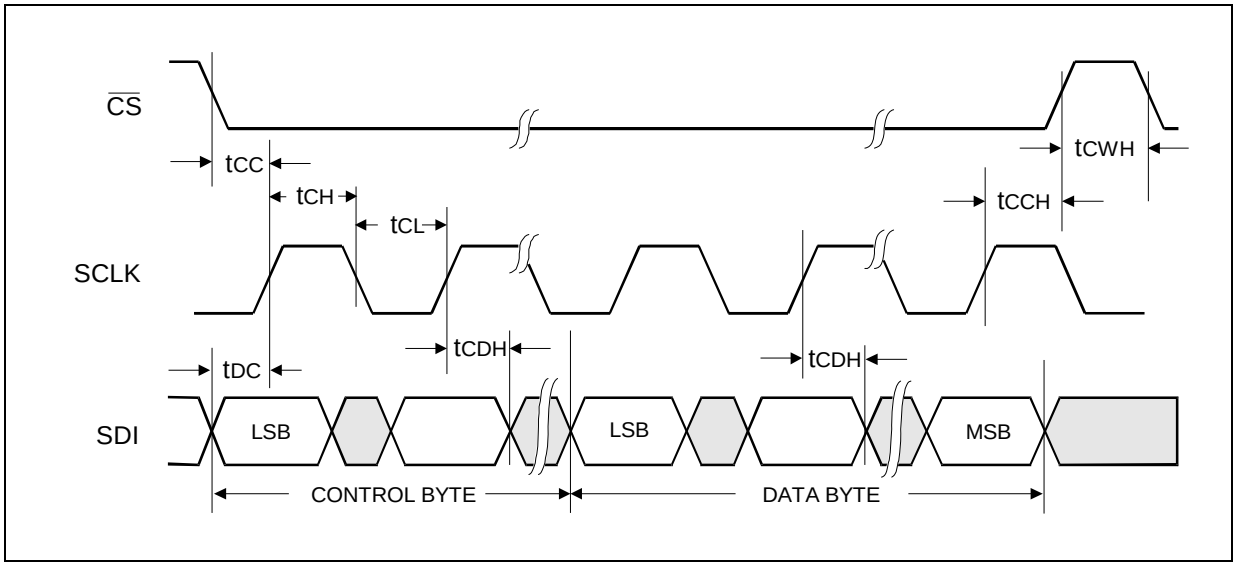

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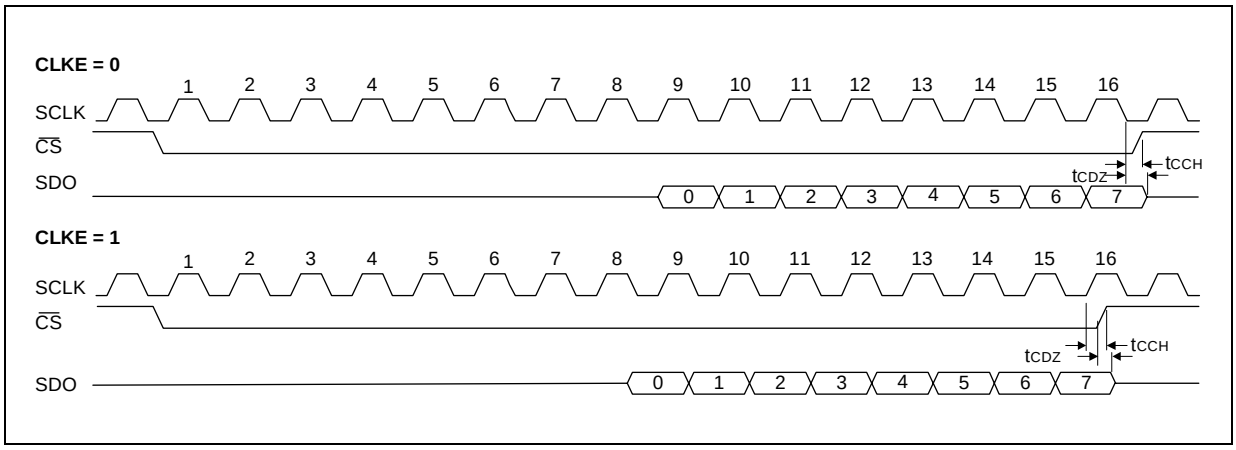
Figure 30 is a timing diagram for serial output from the Host Processor interface.

Figure 30. Serial Output Timing



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12.0 Line-Interface-Unit Circuit Specifications

Table 72 lists specifications for the LIU circuits with which the LXT384 Transceiver is designed to operate. (For a diagram of an LIU circuit to be used with the LXT384 Transceiver, see Figure 6 in Section 6.5, "Line-Interface Protection").

Table 72. Line-Interface-Unit Circuit Specifications

Parameter	Minimum	Typical	Maximum	Units
Termination Resistor Tolerance				
RRING/RTIP termination resistor R_R - Receiver Resistor				
75Ω Coaxial Cable	9.3Ω ± 1%			Ω
120Ω Twisted Pair Cable	15.0Ω ± 1%			Ω
TRING/TTIP termination resistor R_T - Transmitter Resistor				
75Ω Coaxial Cable		8.7Ω ± 1%	9.1Ω ± 1%	Ω
120Ω Twisted Pair Cable		10.5Ω ± 1%	11.0Ω ± 1%	Ω

Table 73 lists specifications for transformers with which the LXT384 Transceiver is designed to operate in an LIU circuit.

Table 73. Intel® LXT384 Transceiver Transformer Specifications

Tx/Rx	Turns Ratio[2]	Primary Inductance mH (min.)	Leakage Inductance µH (max.)	Interwinding Capacitance pF (max.)	DCR Ω (max.)	Dielectric Breakdown Voltage V[1] (min.)
TX	1:2	1.2	0.60	60	0.70 pri 1.20 sec	1500 Vrms
RX	1:2	1.2	0.60	60	1.10 pri 1.10 sec	1500 Vrms

1. This parameter is application dependent.
2. LIU side: Line side. Transformer turns ratio accuracy is ± 2%.

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13.0 Mask Specifications

This chapter discusses the specifications for the mask into which the LXT384 Transceiver transmitter output pulses must fit. The mask specification has two parts.

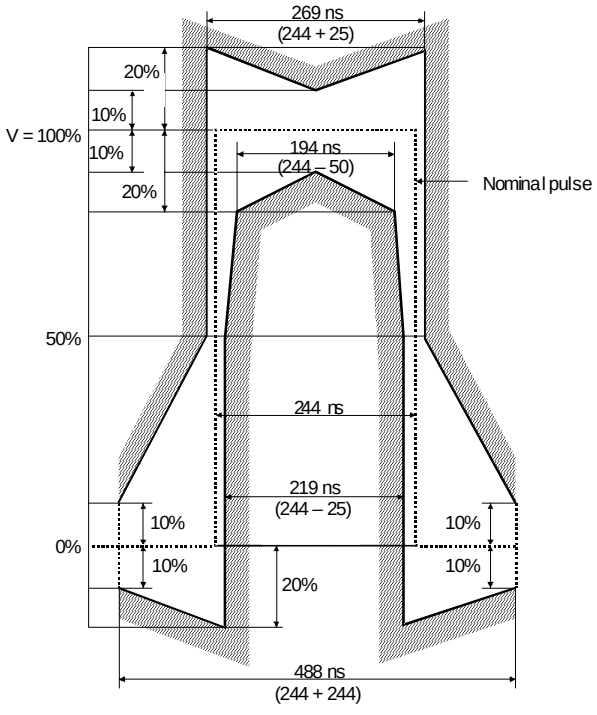
- Part 1 (Table 74) lists specifications on how the pulse relates to load resistance.
- Part 2 (Figure 31) shows the border limits (the mask template) into which the pulse must fit.

Note: For information on pulse shaping, see Section 6.4.2, "Transmitter Pulse Shaping".

Table 74. ITU G.703 2.048 Mbit/s Pulse Mask Specifications

Parameter	Twisted-Pair Cable	Coaxial Cable	Unit
Test load impedance	120	75	Ω
Nominal peak voltage for a mark	3.00	2.37	V
Nominal peak voltage for a space	0 ± 0.300	0 ± 0.237	V
Nominal pulse width	244	244	ns
Ratio (in terms of percentage) of the positive mark amplitude to the negative mark amplitude, with both marks referenced to a space	95 to 105	95 to 105	Ratio in %

Figure 31. E1, ITU G.703 Mask Template



Note: V corresponds to the nominal peak value.

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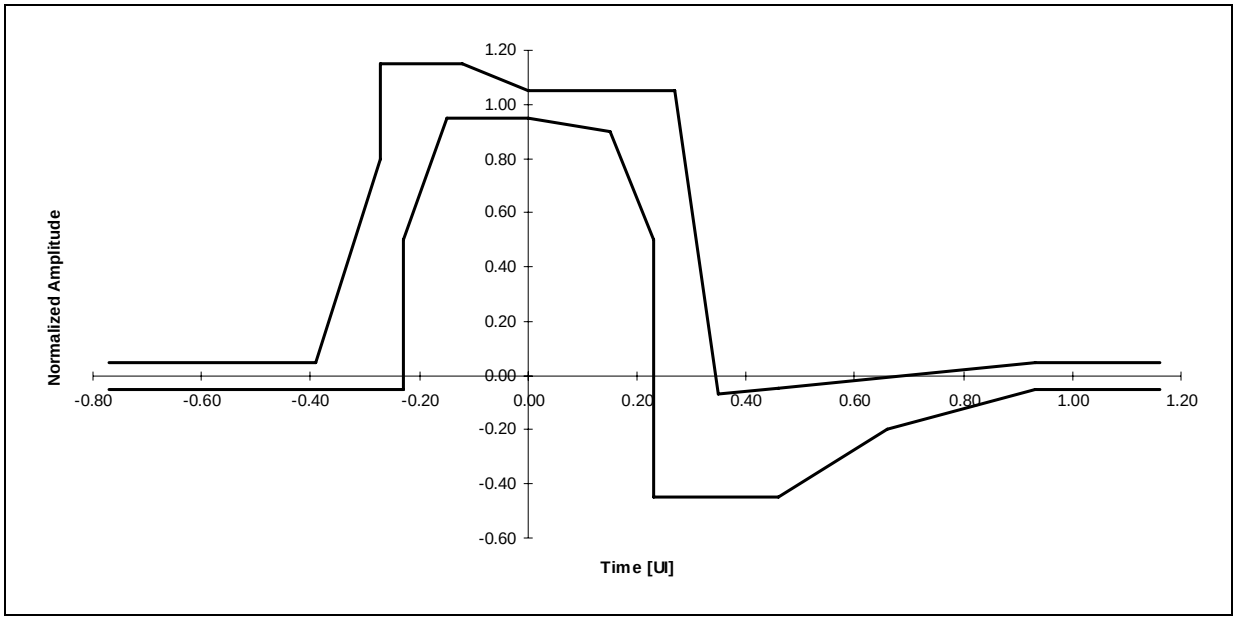
Table 75. T1.102 1.544 Mbit/s Pulse Mask Specifications for Intel® LXT384 Transceiver

Parameter	Cable	Unit
	TWP	
Test load impedance	100	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ±0.15	V
Nominal pulse width	324	ns
Ratio of positive and negative pulse amplitudes	95-105	%

Figure 32. T1, T1.102 Mask Templates for LXT384



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14.0 Jitter Performance

This chapter includes tables and figures on jitter performance. For more information on jitter, see:

- Section 6.6, “Jitter Attenuation”
- Table 43 in Chapter 8.0, “Registers”

Table 76 lists jitter attenuator characteristics for the LXT384 Transceiver.

Table 76. Intel® LXT384 Transceiver Jitter Attenuator Characteristics

Parameter			Min.	Typ	Max	Unit	Test Condition
E1 jitter attenuator 3dB corner frequency, host mode[1]	JACF=0	32bit FIFO	-	2.5	-	Hz	Sinusoidal jitter modulation
		64bit FIFO	-	3.5	-	Hz	
	JACF=1	32bit FIFO	-	2.5	-	Hz	
		64bit FIFO	-	3.5	-	Hz	
T1 jitter attenuator 3dB corner frequency, host mode[1]	JACF=0	32bit FIFO	-	3	-	Hz	
		64bit FIFO	-	3	-	Hz	
	JACF=1	32bit FIFO	-	6	-	Hz	
		64bit FIFO	-	6	-	Hz	
Jitter attenuator 3dB corner frequency, hardware mode[1]		E1	-	3.5	-	Hz	
		T1	-	6	-	Hz	
Data latency delay		32bit FIFO	-	16	-	UI	Delay through the Jitter attenuator only. Add receive and transmit path delay for total throughput delay.
		64bit FIFO	-	32	-	UI	
Input jitter tolerance before FIFO overflow or underflow		32bit FIFO	-	24	-	UI	
		64bit FIFO	-	56	-	UI	
E1 jitter attenuation	@ 3 Hz @ 40 Hz @ 400 Hz @ 100 KHz		-0.5 -0.5 +19.5 +19.5	–	–	dB	ITU-T G.736, See Figure 34 on page 129
T1 jitter attenuation	@ 1 Hz @ 20 Hz @ 1 KHz @ 1.4 KHz @ 70 KHz		0 0 33.3 40 40	–	–	dB	AT&T Pub. 62411, See Figure 34 on page 129
Output Jitter in remote loopback[1]				0.060	0.11	UI	ETSI CTR12/13 Output jitter

1. Guaranteed by design and other correlation methods.

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Table 77. Intel® LXT384 Transceiver Analog Test Port Characteristics

Parameter	Sym	Min.	Typ	Max	Unit	Test Condition
3 dB bandwidth	At13db	-	5	-	MHz	
Input voltage range	At1iv	0	-	VCC0 VCC1	V	
Output voltage range	At2ov	0	-	VCC0 VCC1	V	

Figure 33 shows the typical LXT384 Transceiver jitter tolerance.

Figure 33. Intel® LXT384 Transceiver Jitter Tolerance Performance

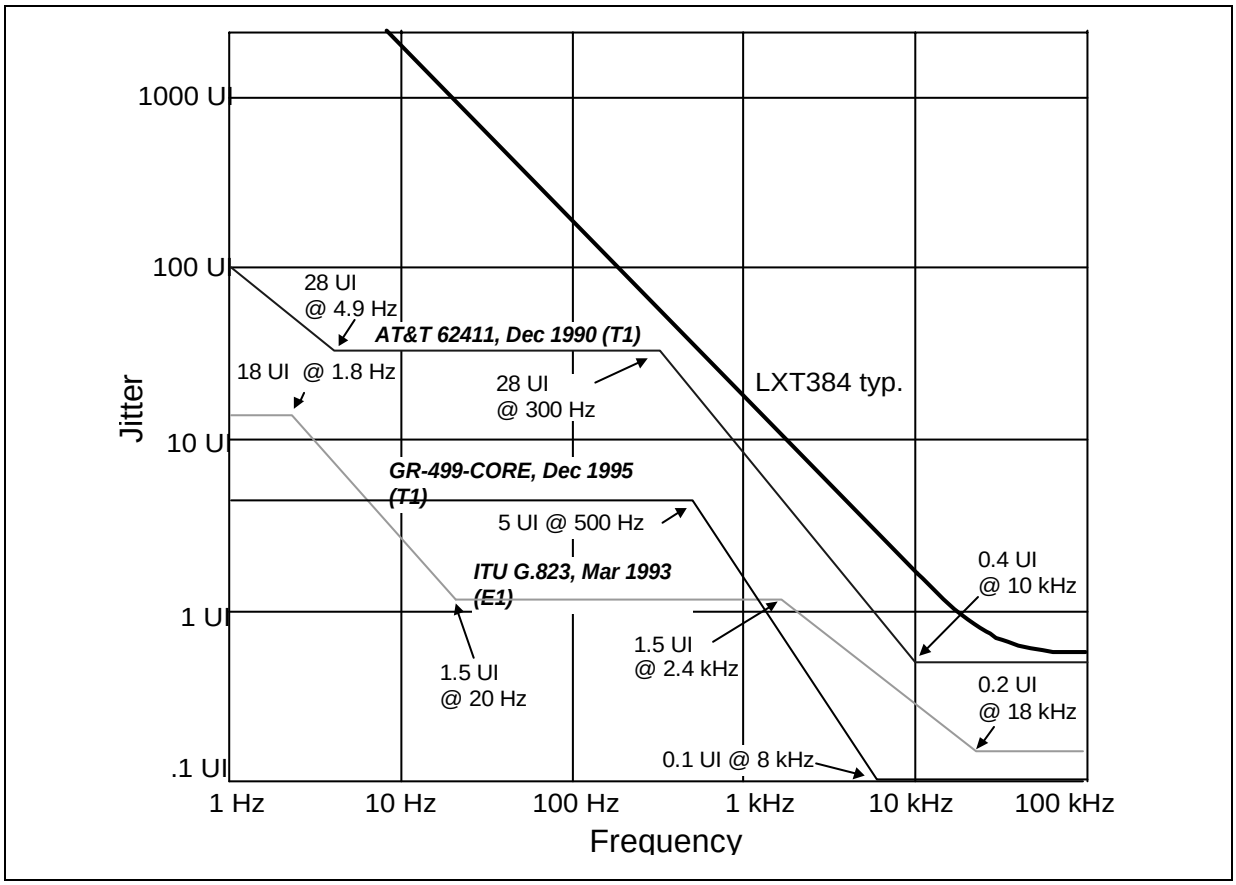

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Figure 34 shows the typical jitter transfer performance for the LXT384 Transceiver.

Figure 34. Intel® LXT384 Transceiver Jitter Transfer Performance

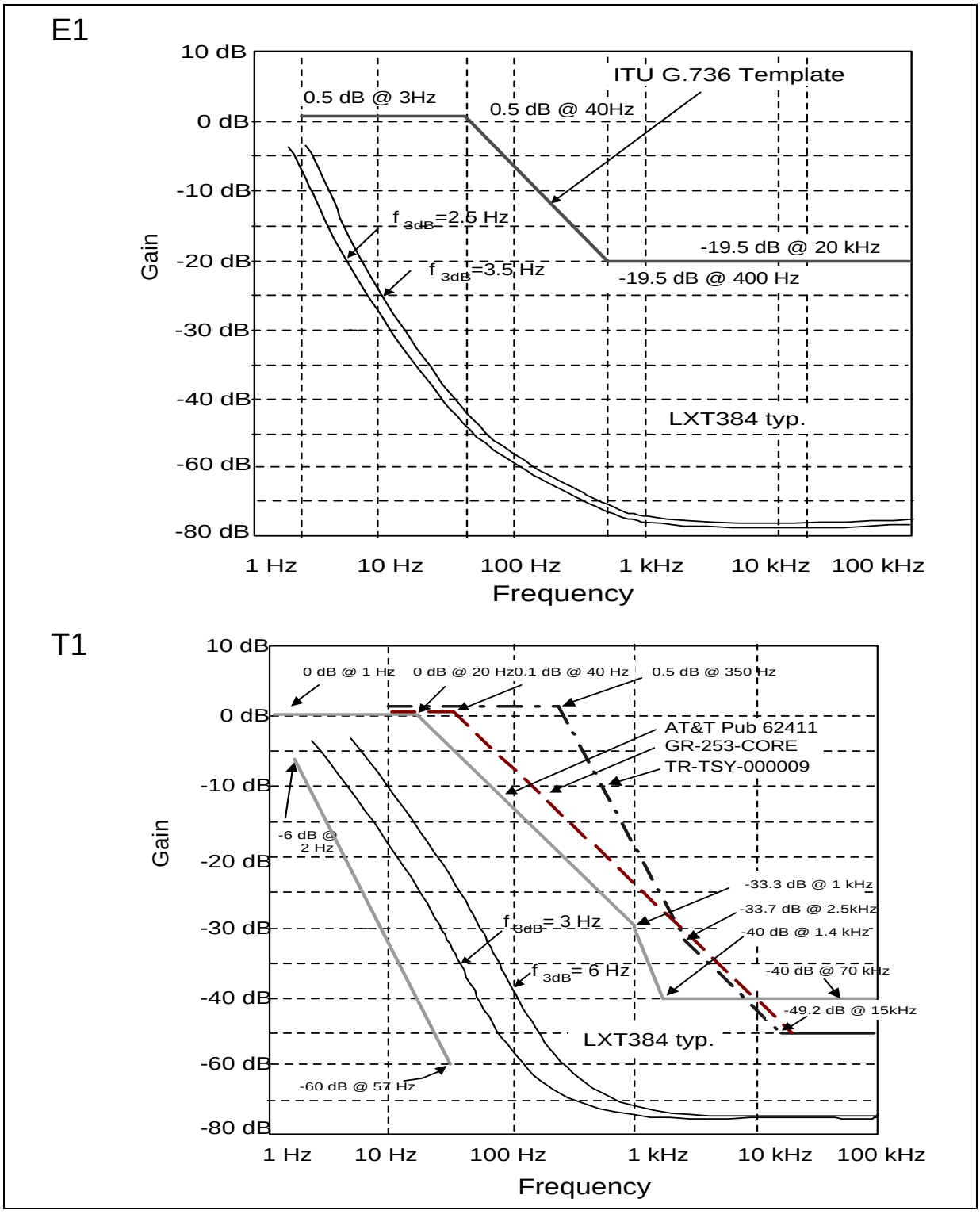

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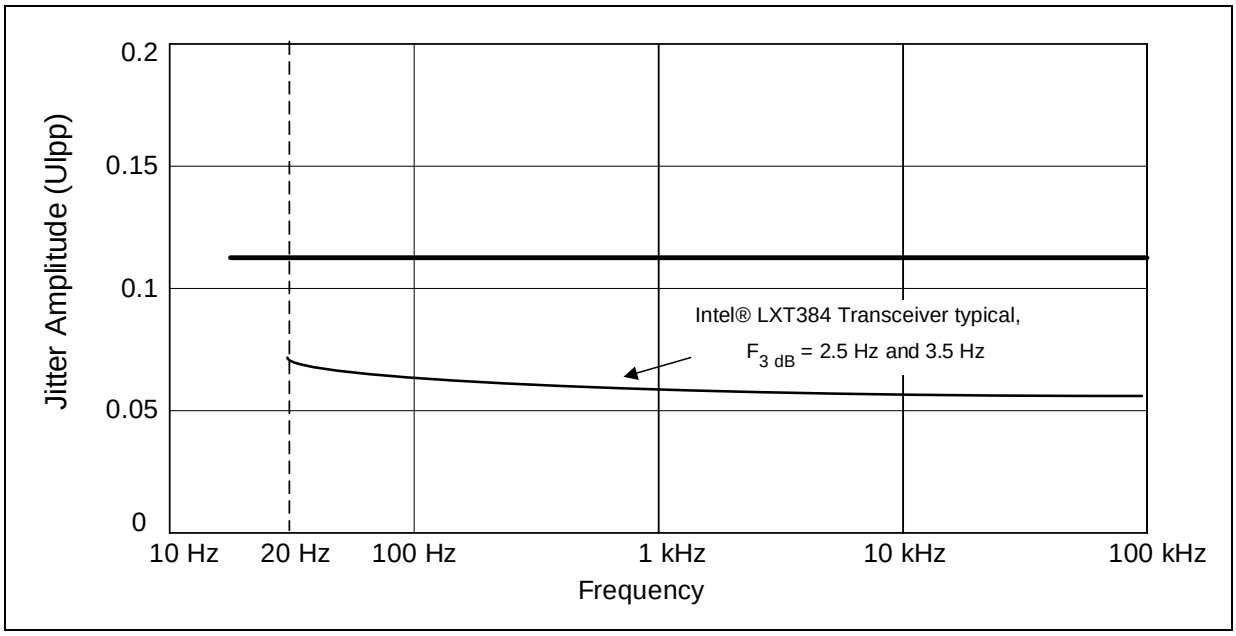
Figure 35 shows the typical jitter performance of the LXT384 Transceiver when it is used in ETSI CTR12/13 applications that place the LXT384 Transceiver in a system with other devices.

As Figure 35 shows, the LXT384 Transceiver output jitter is below the specified jitter requirement (indicated in the figure by the dark line).

Figure 35. Intel® LXT384 Transceiver Output Jitter for ETSI CTR12/13 Applications



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15.0 Recommendations and Specifications

- AT&T* - Technical Reference 62411 “Private Line Services - Description and Interface Specification”, December 1990.
- ANSI T1.102 - 199X Digital Hierarchy Electrical Interface
- ANSI T1.231 - 1993 Digital Hierarchy Layer 1 In-Service Digital Transmission Performance Monitoring
- European Telecommunications Standards Institute (ETSI) publications:
  - ETSI CTR12/13 -
    - TCTR 012 Reference DTR/NA-004001. Network Aspects (NA). ONP study on possible new interfaces at the network side of the NT1
    - TCTR 013 Reference: DTR/NA-001001. Network Aspects (NA). Network support of cordless terminal mobility
  - ETSI ETS 300 166 - Transmission and Multiplexing - Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s
  - ETS 300386-1 Electromagnetic Compatibility Requirement
- IEEE 1149.1, Standard Test Access Port and Boundary-Scan Architecture
- International Telecommunication Union (ITU) publications:
  - G.703 Physical/electrical characteristics of hierarchical digital interfaces
  - G.704 Functional characteristics of interfaces associated with network nodes
  - G.735 Characteristics of Primary PCM multiplex equipment operating at 2048 kbit/s and offering digital access at 384 kbit/s and/or synchronous digital access at 64 kbit/s
  - G.736 Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s
  - G.772 Protected monitoring points provided on digital transmission systems
  - G.775 Loss Of Signal (LOS), Alarm Indication Signal (AIS) and Remote Defect Indication (RDI) and clearance criteria for PDH signals
  - G.783 Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks
  - G.823 The control of jitter and wander within digital networks which are based on 2048 kbit/s hierarchy
  - O.151 Error performance measuring equipment operating at the primary rate and above (This publication specifies instruments to measure error performance in digital systems.)

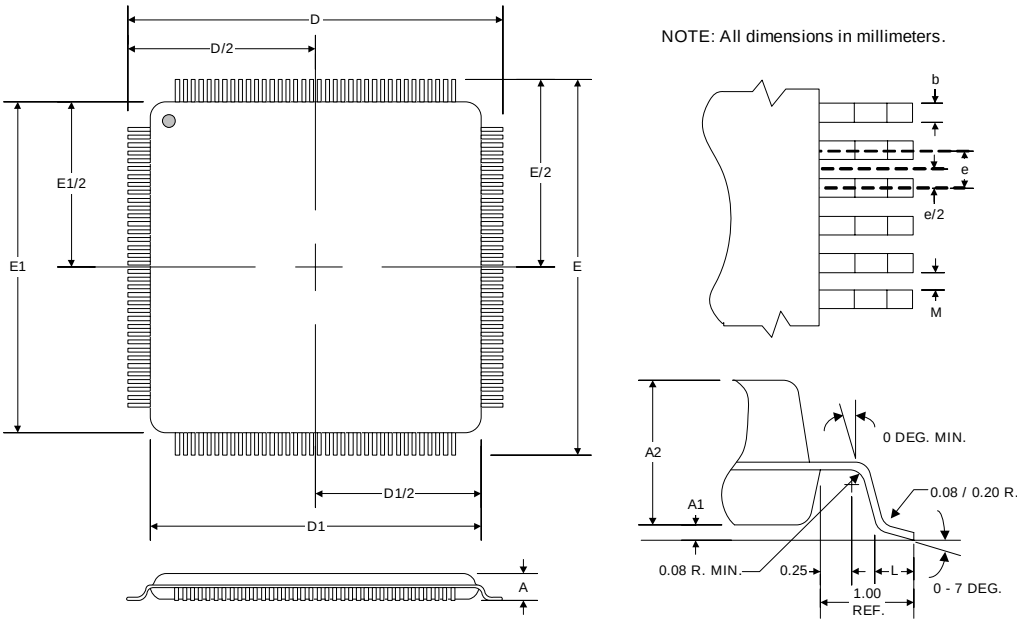
- Office of Telecommunications (United Kingdom) publication: OFTEL OTR-001 Short Circuit Current Requirements
- Telcordia* publications. (Telcordia was formerly known as Bellcore.)
  - GR-253-CORE SONET Transport Systems Common Generic Criteria
  - GR-499-CORE Transport Systems Generic Requirements
  - TR-TSY-000009 Asynchronous Digital Multiplexes Requirements and Objectives

16.0 Mechanical Specifications

Figure 36. Dimensions for 144-Pin Low Octal Flat Package (LQFP)

144-Pin LQFP

- Part Number LXT384LE
- Extended Temperature Range (-40° C to 85° C)



Dimension[1]	Millimeters		
	Minimum	Nominal	Maximum
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D	22.00 Basic Spacing between Centers (BSC)		
D1	20.00 BSC		
E	22.00 BSC		
E1	20.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
M	0.14	-	-

1. See Joint Electronic Devices Engineering Council (JEDEC) publications for additional specifications.

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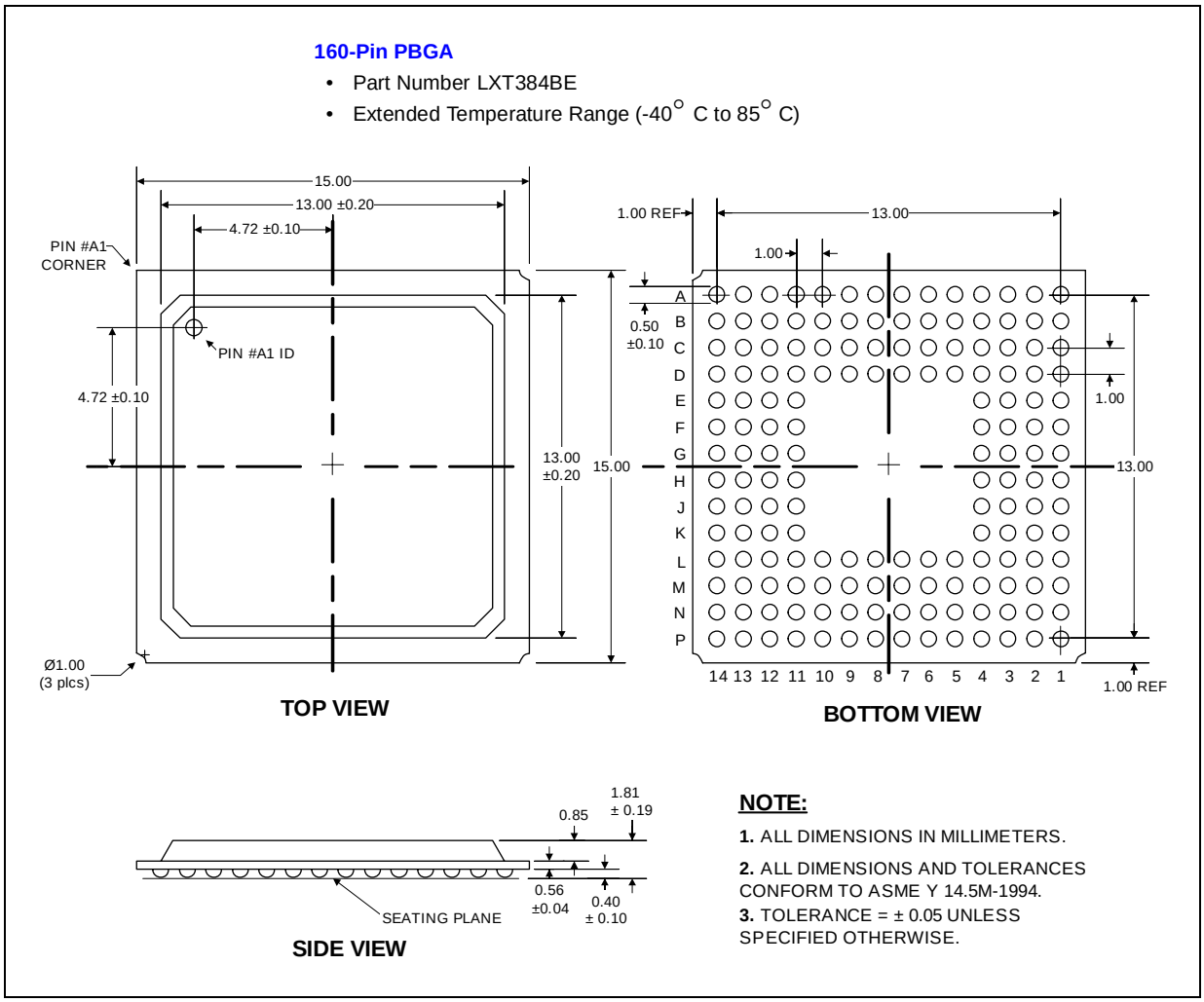
Figure 37. Dimensions for 160-Ball Plastic Ball Grid Array (BGA)



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16.1 Top Label Markings

Figure 38 shows a sample LQFP non-RoHS package for the LXT384 Transceiver.

Note: In contrast to Pb-Free (RoHS-compliant) LQFP packages, the non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.

Figure 38. Sample LQFP Non-RoHS Package - Intel® LXT384 Transceiver

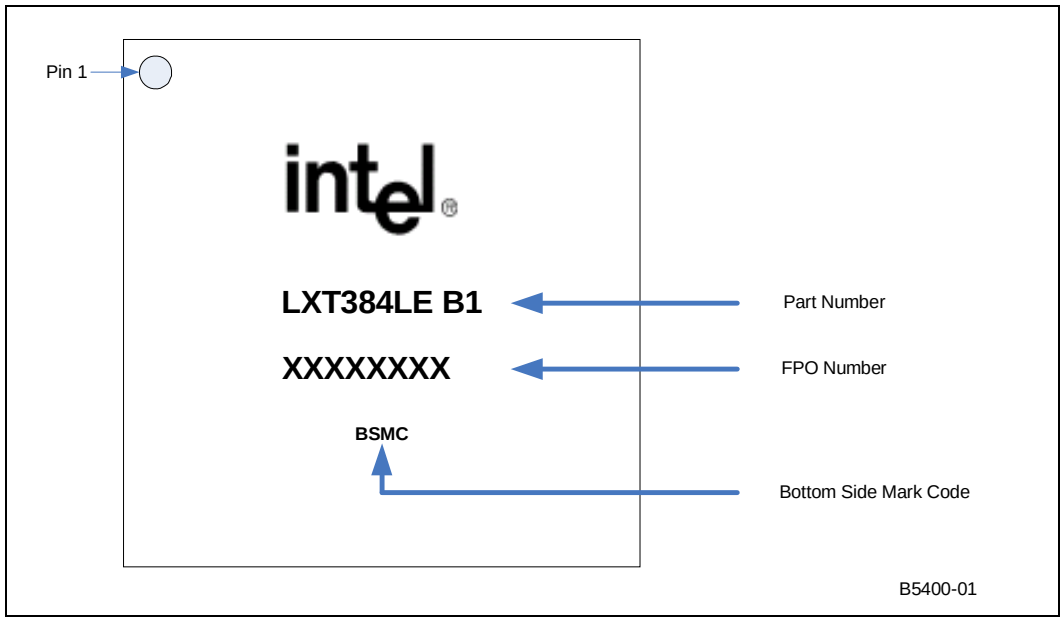

Figure 39 shows a sample LQFP RoHS package for the LXT384 Transceiver.

Figure 39. Sample LQFP RoHS Package - Intel® LXT384 Transceiver

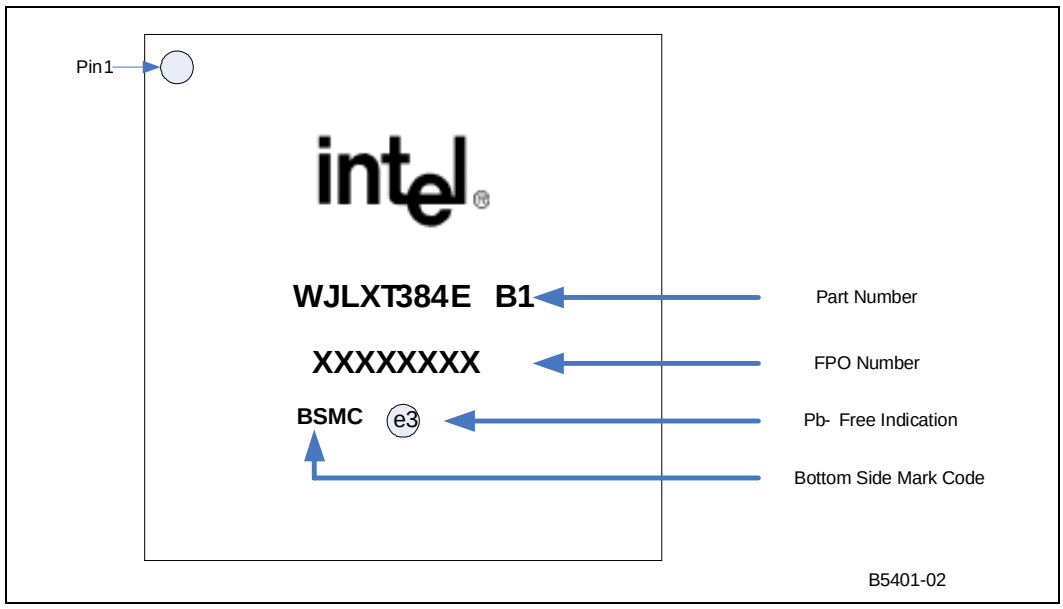

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Figure 40 shows a sample plastic BGA non-RoHS package for the LXT384 Transceiver.

Note: In contrast to Pb-Free (RoHS-compliant) plastic BGA packages, non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.

Figure 40. Sample Plastic BGA Non-RoHS Package - Intel® LXT384 Transceiver

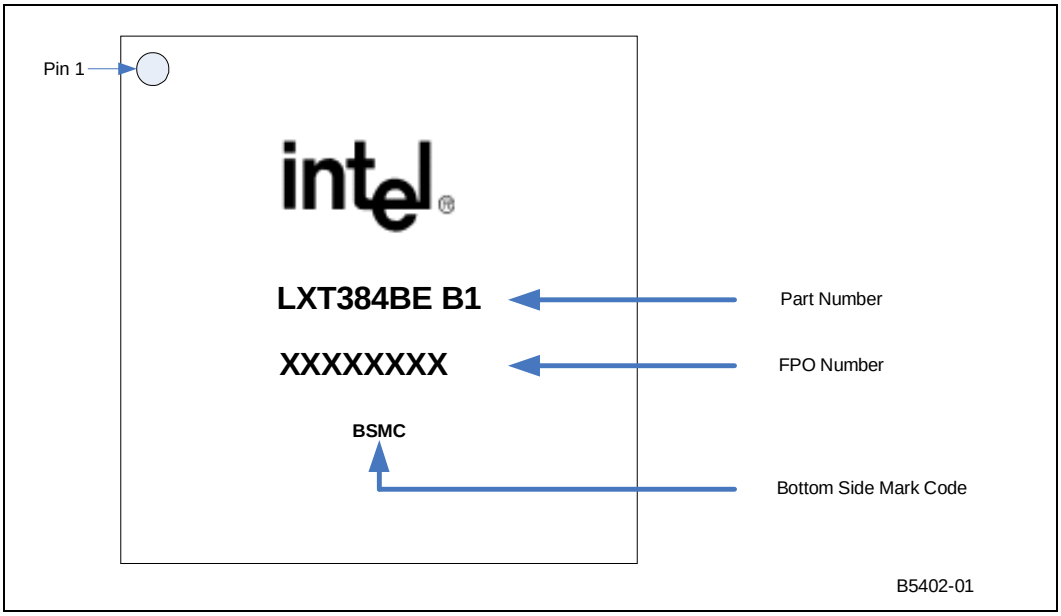
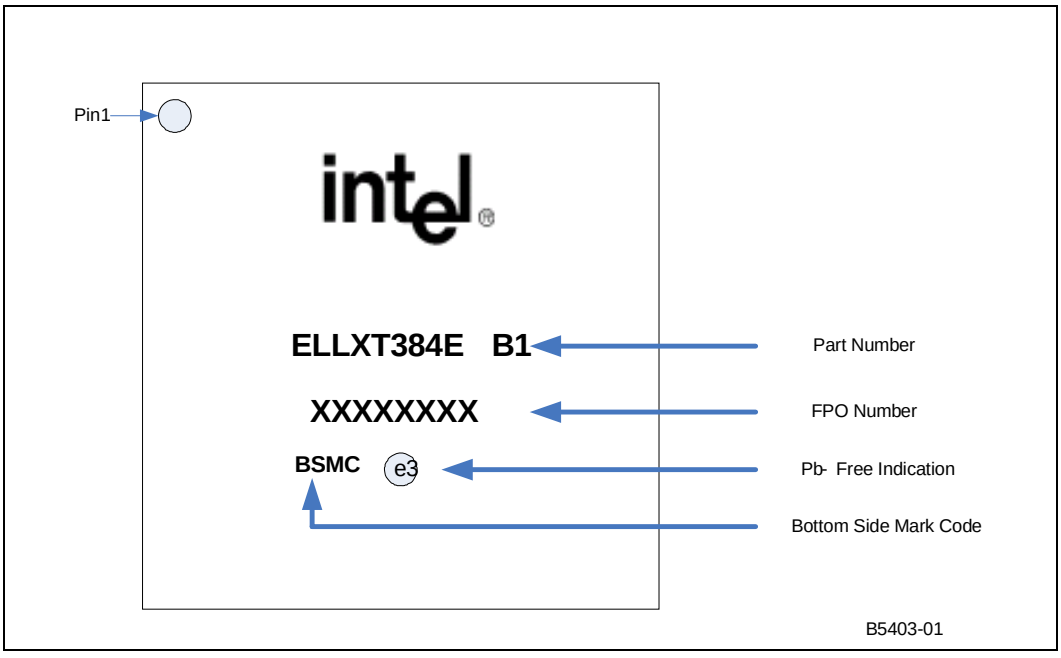


Figure 41 shows a sample plastic BGA RoHS package for the LXT384 Transceiver.

Figure 41. Sample Plastic BGA RoHS Package - Intel® LXT384 Transceiver



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17.0 Product Ordering Information

Table 78 lists product ordering information for the LXT384 Transceiver.

Table 78. Product Ordering Information

Product Number	Revision	Package Type	Pin Count	RoHS Compliant	Figure
DJLXT384LE.B1	B1	LQFP	144	No	Figure 38, “Sample LQFP Non-RoHS Package - Intel® LXT384 Transceiver”
WJLXT384LE.B1	B1	LQFP	144	Yes	Figure 39, “Sample LQFP RoHS Package - Intel® LXT384 Transceiver”
FLLXT384BE.B1	B1	BGA	160	No	Figure 40, “Sample Plastic BGA Non-RoHS Package - Intel® LXT384 Transceiver”
ELLXT384BE.B1	B1	BGA	160	Yes	Figure 41, “Sample Plastic BGA RoHS Package - Intel® LXT384 Transceiver”

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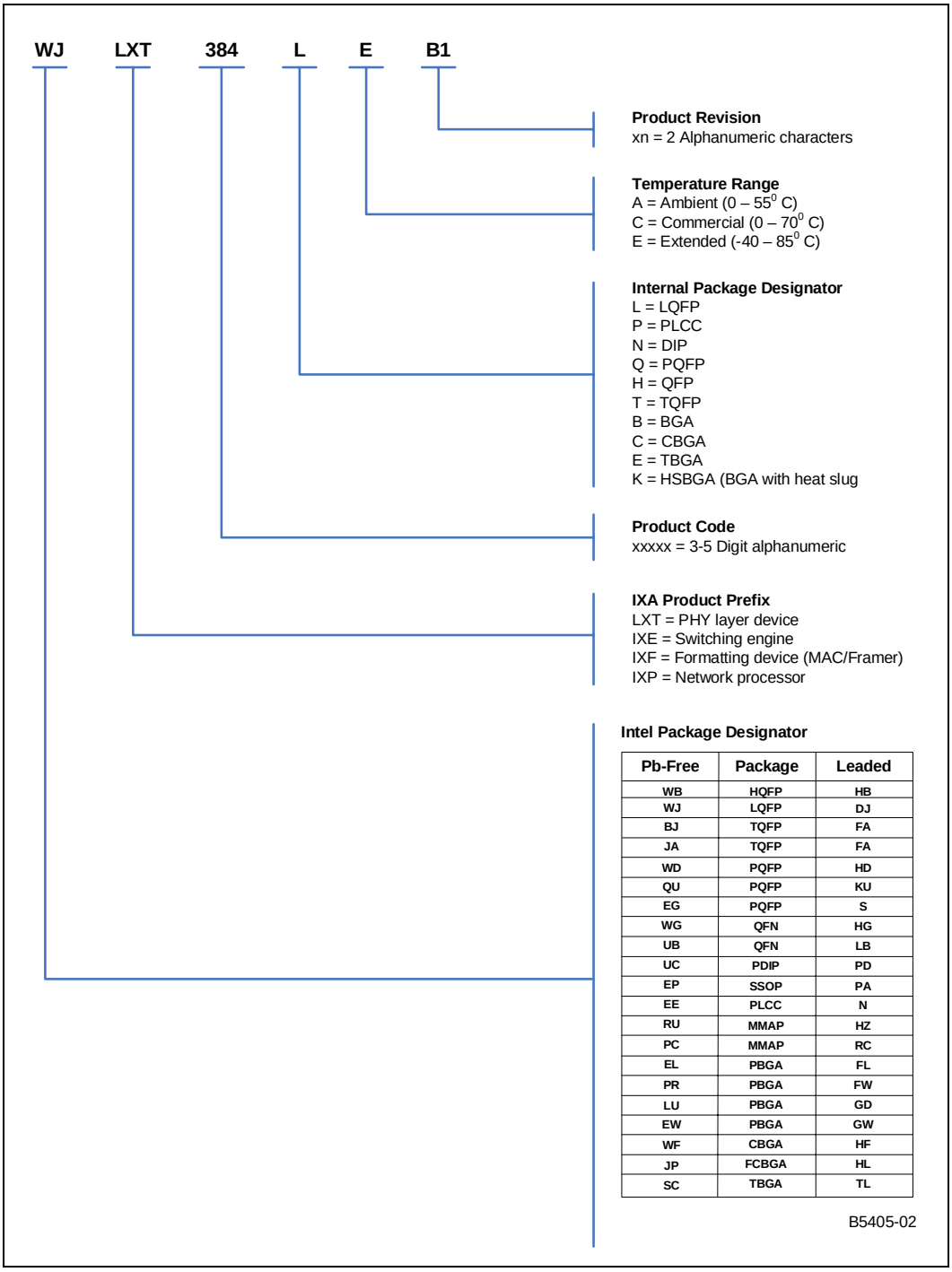
18.0 Package Information

Figure 42 shows an order matrix with sample information on how to order a LXT384 product.

Figure 42. Order Matrix



Pb-Free	Package	Leaded
WB	HQFP	HB
WJ	LQFP	DJ
BJ	TQFP	FA
JA	TQFP	FA
WD	PQFP	HD
QU	PQFP	KU
EG	PQFP	S
WG	QFN	HG
UB	QFN	LB
UC	PDIP	PD
EP	SSOP	PA
EE	PLCC	N
RU	MMAP	HZ
PC	MMAP	RC
EL	PBGA	FL
PR	PBGA	FW
LU	PBGA	GD
EW	PBGA	GW
WF	CBGA	HF
JP	FCBGA	HL
SC	TBGA	TL

19.0 Abbreviations and Acronyms

Table 79 lists abbreviations and acronyms and their meanings.

Table 79. Abbreviations, Acronyms, and Meanings

Abbreviation or Acronym	Meaning of Abbreviation or Acronym
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
B8ZS	Bipolar 8-Zero Substitution
BPV	BiPolar Violation
ESD	Electro-Static Discharge
FCS	Frame Check Sequence
FIFO	First In, First Out
HDB3	High Density Bipolar Three
I/O	In/Out
ITU	International Telecommunication Union
JA	Jitter Attenuator
JA	Jitter Attenuator
JEDEC	Joint Electronic Devices Engineering Council
JTAG	Joint Test Action Group
LIU	Line Interface Unit
LOS	Loss Of Signal
LQFP	Low Octal Flat Package
Max.	Maximum
Mbps	Megabits per second
Min.	Minimum
NEG	Negative
NRZ	Non-Return to Zero
PBGA	Plastic Ball Grid Array
PLL	Phase-Locked Loop
POS	Positive
REBE	Remote End Block Error
RZ	Return to Zero
Sym.	Symbol
TAOS	Transmit All Ones
Typ.	Typical
UI	Unit Interval
UIpp	Unit Interval peak-to-peak

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