Advance Data Sheet
May 2001

TDCS4810G SONET/SDH 10 Gbits/s APS Port and TSI

Features

- 10 Gbit bidirectional data path with common frame synchronization and clocking.
- Versatile IC which supports an aggregate bandwidth of 30 Gbits/s.
- Supports flexible 48-channel STS-12 data links.
- Supports full nonblocking fabric with switching granularity of STS-1/STM-1.
- Support for line/path switching.
- Supports any valid mix of STS-1 and concatenated payloads from STS-3c to STS-192c.
- Provides a standard 5-pin P1149.1 JTAG port with memory BIST scan and boundary scan.
- Low-power 1.5 V operation with 3.3 V inputs and outputs.
- Configurable on-chip TSI block for switching of STS-1s.
- On-chip connection memory for flexible configuration of working connections and protect connections for each STS-1.
- 792 LBGA package.
- –40 °C to +85 °C industrial temperature range.

Interface

- Robust receiver interface capable of handling STS-12 streams having combined static- and dynamic-frame offsets of up to 64 bytes without creating traffic disruption.
- Frames to and performs integrity check on each STS-12 interface.
- Each STS-12 input interface consists of an LVDS data input with integral clock and data recovery (CDR).
- Each STS-12 output interface consists of an LVDS output.
- Ability to insert an AIS-L or pass-through when an LOF condition occurs.
- Interfaces have A1/A2 framing, link trace, parity, and a communications link.

Cross Connect

- Supports up to 576 STS-1 time slots.
- 48 input channels and 48 output channels.
- Each input time slot can be connected to any/all output time slots.
- Each output time slot can be connected to any input time slot or be assigned AIS-P or UNEQ-P.
- Fully programmable and nonblocking cross connect.
- Supports drop-and-continue and full broadcast capabilities.
- Ability to insert path AIS and UNEQ indications on any STS-1 under software control.

Protection Switching

- Supports 1+1, 1:1, 1:N, UPSR, and BLSR protection mechanisms with four connection memory.
- Separate line and path protection mechanisms.
- Supports equipment protection switching.
- On-chip working/protected memory paths for easy switch configurations.

Microprocessor Interface

- Microprocessor interface supports both synchronous and asynchronous operations.
- 16-bit wide data bus interface and 13-bit wide address bus.

Table of Contents

Contents **Page**

List of Figures

Contents **Page**

List of Tables

Contents **Page**

List of Tables (continued)

Contents **Page**

Applications

- SONET/SDH terminal equipment.
- SONET/SDH digital cross connect equipment.
- SONET/SDH add-drop multiplex equipment.
- SONET/SDH test equipment.
- TDCS4810G will interface seamlessly to a number of Agere Systems Inc. existing/next-generation high-speed framers.

Description

The TDCS4810G has four sections: receive interface channels, a cross connect fabric core, transmit channels, and a microprocessor interface. The block diagram of the TDCS4810G is shown in Figure 1.

All data stream channels must be synchronous in frequency, but can be asynchronous in phase.

The TDCS4810G does not perform pointer processing functions. These are performed by the line and tributary cards, which align the payload at known positions relative to a common frame signal.

The TDCS4810G is able to support SONET and SDH cross connects.

The A1, A2, B1, H1, H2, H3, K1, and K2 bytes are used for their original SONET/SDH purposes.

Note: Throughout this document, the term channel always refers to an STS-12 data stream that is carried on a single LVDS link.

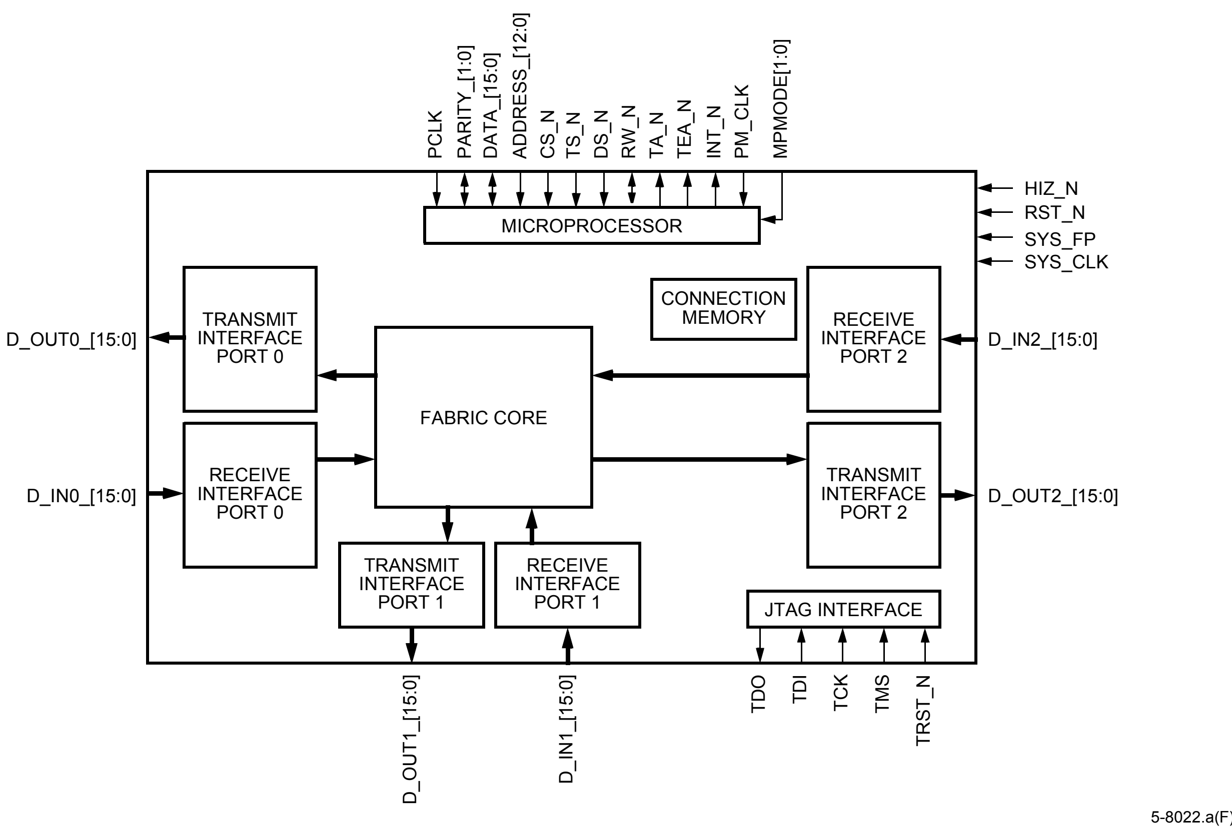


Figure 1. TDCS4810G Block Diagram

Description (continued)

Receive Interface

The receiver is composed of 48 STS-12 channels that are either treated as independent channels, or treated as three groups of 16 channels each, forming three STS-192 streams. Incoming data for each channel is received through an LVDS serial port operating at 622 Mbits/s. The incoming serial stream frequency must be the same as the outgoing LVDS serial stream of the transmitter. Each STS-192 interface (16 channels) has its own PLL using the same reference clock.

The receiver is able to handle STS-12 streams having combined static and dynamic frame offsets of up to 64 bytes without creating any traffic disruption.

The receiver performs three major functions, which are described in greater detail in upcoming sections: the clock and data recovery (CDR), the framer, and the FIFO aligner.

Fabric Core

The cross connect has 48 input channels and 48 output channels. Each channel has the bandwidth capacity to carry an STS-12 worth of data. The channels can also be thought of as three bidirectional STS-192 data streams.

The fabric core consists of a time-slot interchanger (TSI), a connection memory (shown externally in Figure 1), E1/F1/E2 extraction, and AIS/UNEQ insertion.

Time-Slot Interchanger (TSI)

The TSI is used to reorder the STS-1 data. In doing this, the TSI ensures that any output STS-1 channel can be connected to any input STS-1 regardless of any other switch configuration. Incoming data is written into one of two buffers in a regular order while output data is read from another buffer in an order dependent on the address provided to the TSI, from the connection memory, for each channel. Once one buffer has been completely written to, the read and write buffers switch. This switch is controlled by a synchronization input.

Connection Memory

The connection memory is used to configure the TSI to switch the incoming STS-1s to the desired output buffer. There is a working memory to configure the working connections for each STS-1, and there is a protected memory to configure the protection connection for each STS-1. Each of the working and protected memories are duplicated (A and B) to allow for easy software configuration.

E1/F1/E2 Extraction

The E1 and F1 bytes of each STS-1 carry information indicating the path status of that STS-1. Both bytes contain the same information. This information can be used by software to initiate a switch from working to protected configurations. The E1 and F1 bytes are extracted from STS-1s at the output of the TSI and stored.

The bytes are monitored for a change, and if a change is detected, a latched alarm is raised.

The E2 byte of the STS-1 of each STS-12 (channel) carries proprietary information indicating the line status of that STS-12. This information can be used by software to initiate a switch from working to protected configurations. The E2 byte is extracted from the STS-1 of each STS-12 at the input to the TSI and stored.

AIS/UNEQ Insertion

Path AIS(AIS-P) and UNEQ indications can be inserted on individual STS-1s within a stream under software control to squelch individual STS-1s during and after network topology reconfigurations. This process ensures that downstream path processors will detect a normal pointer and will thus be able to extract the path overhead in order to detect an UNEQ defect.

Transmit Interface

The transmitter is composed of 48 STS-12 channels that are always treated as independent channels. Incoming data for each channel is received from the cross connect. Each of the outgoing LVDS serial streams of the transmitter transmits at a rate of 622 Mbits/s, and the data is synchronized to the system clock.

Microprocessor Interface

The microprocessor interface supports both synchronous and asynchronous operations. The microprocessor interface has a 16-bit wide data bus and a 13-bit wide address bus.

Channels can be independently enabled or disabled under software control with powerdown mode. In the event that redundant cross connects are desired, 3-state buffers are available to support redundancy.

Supervisory features built into the TDCS4810G provide diagnostic capabilities and fault coverage. There is an interrupt output for the microprocessor interface. Interrupt sources are maskable.

Pin Information

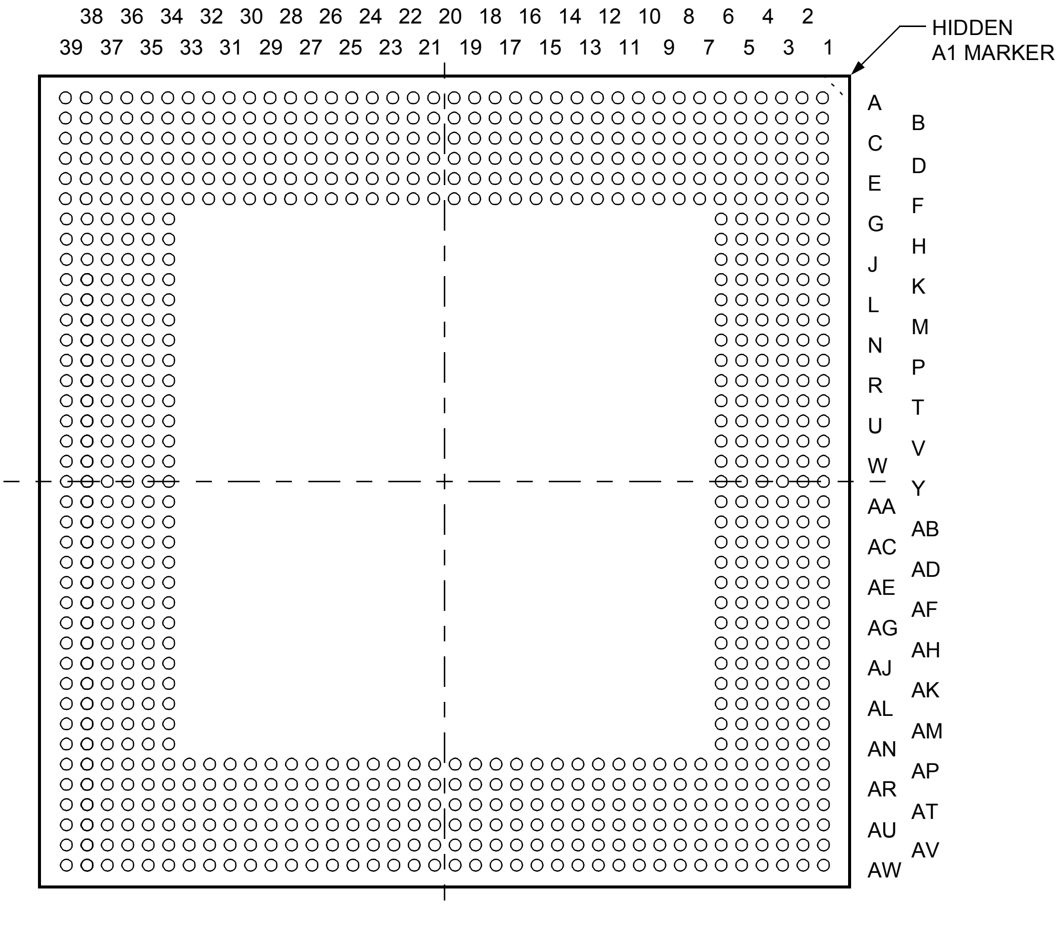


Figure 2. Pin Diagram of 792 LBGA (Bottom View)

Pin Information (continued)

Table 1. Pin Assignments for 792-Pin LBGA by Pin Number Order

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VDD	B1	VDD	C1	D_OUT0_12_N	D1	D_OUT0_15_N
A2	VDD	B2	VDD	C2	D_OUT0_12	D2	D_OUT0_15
A3	D_OUT0_11	B3	D_OUT0_11_N	C3	VSS	D3	VSS
A4	D_OUT0_08	B4	D_OUT0_08_N	C4	VSS	D4	VSS
A5	REF14_0	B5	REF10_0	C5	D_OUT0_10	D5	D_OUT0_10_N
A6	D_OUT0_05	B6	D_OUT0_05_N	C6	D_OUT0_07	D6	D_OUT0_07_N
A7	D_OUT0_04	B7	D_OUT0_04_N	C7	VDD	D7	VSS
A8	D_OUT0_02	B8	D_OUT0_02_N	C8	UNUSED	D8	UNUSED
A9	D_OUT0_00	B9	D_OUT0_00_N	C9	VSS	D9	VDD2
A10	D_IN0_00	B10	D_IN0_00_N	C10	UNUSED	D10	UNUSED
A11	D_IN0_01	B11	D_IN0_01_N	C11	VDD	D11	VSS
A12	D_IN0_03	B12	D_IN0_03_N	C12	CTAP0_0	D12	REXT0
A13	D_IN0_05	B13	D_IN0_05_N	C13	VSS	D13	VDD2
A14	D_IN0_07	B14	D_IN0_07_N	C14	CTAP0_1	D14	UNUSED
A15	D_IN0_09	B15	D_IN0_09_N	C15	VDD	D15	VSS
A16	D_IN0_10	B16	D_IN0_10_N	C16	CTAP0_2	D16	UNUSED
A17	D_IN0_12	B17	D_IN0_12_N	C17	VSS	D17	VDD2
A18	D_IN0_14	B18	D_IN0_14_N	C18	CTAP0_3	D18	UNUSED
A19	UNUSED	B19	VDD	C19	VSS	D19	D_IN0_15
A20	VDD	B20	VDD	C20	VSS	D20	VSS
A21	UNUSED	B21	VDD	C21	VSS	D21	D_IN1_15
A22	D_IN1_14	B22	D_IN1_14_N	C22	CTAP1_3	D22	UNUSED
A23	D_IN1_12	B23	D_IN1_12_N	C23	VSS	D23	VDD2
A24	D_IN1_10	B24	D_IN1_10_N	C24	CTAP1_2	D24	UNUSED
A25	D_IN1_09	B25	D_IN1_09_N	C25	VDD	D25	VSS
A26	D_IN1_07	B26	D_IN1_07_N	C26	CTAP1_1	D26	UNUSED
A27	D_IN1_05	B27	D_IN1_05_N	C27	VSS	D27	VDD2
A28	D_IN1_03	B28	D_IN1_03_N	C28	CTAP1_0	D28	REXT1
A29	D_IN1_01	B29	D_IN1_01_N	C29	VDD	D29	VSS
A30	D_IN1_00	B30	D_IN1_00_N	C30	UNUSED	D30	UNUSED
A31	D_OUT1_00	B31	D_OUT1_00_N	C31	VSS	D31	VDD2
A32	D_OUT1_02	B32	D_OUT1_02_N	C32	UNUSED	D32	UNUSED
A33	D_OUT1_04	B33	D_OUT1_04_N	C33	VDD	D33	VSS
A34	D_OUT1_05	B34	D_OUT1_05_N	C34	D_OUT1_07	D34	D_OUT1_07_N
A35	RESHI_1	B35	RESLO_1	C35	D_OUT1_10	D35	D_OUT1_10_N
A36	D_OUT1_08	B36	D_OUT1_08_N	C36	VSS	D36	VSS
A37	D_OUT1_11	B37	D_OUT1_11_N	C37	VSS	D37	VSS
A38	VDD	B38	VDD	C38	D_OUT1_12	D38	D_OUT1_15
A39	VDD	B39	VDD	C39	D_OUT1_12_N	D39	D_OUT1_15_N

Notes:
Do not connect pins designated as NC (no connect pins).
Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 1. Pin Assignments for 792-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
E1	NC	F1	NC	G1	NC	K4	NC
E2	NC	F2	NC	G2	NC	K5	NC
E3	D_OUT0_13_N	F3	NC	G3	VDD	K6	NC
E4	D_OUT0_13	F4	NC	G4	VSS	K34	NC
E5	VDD2	F5	VDD2	G5	D_OUT0_14_N	K35	NC
E6	VDD2	F6	VDD2	G6	D_OUT0_14	K36	NC
E7	D_OUT0_09	F7	D_OUT0_09_N	G34	D_OUT1_14	K37	NC
E8	D_OUT0_06	F8	D_OUT0_06_N	G35	D_OUT1_14_N	K38	NC
E9	RESLO_0	F9	RESHI_0	G36	VSS	K39	NC
E10	D_OUT0_03	F10	D_OUT0_03_N	G37	VDD	L1	NC
E11	D_OUT0_01	F11	D_OUT0_01_N	G38	NC	L2	NC
E12	VDDA	F12	VSSA	G39	NC	L3	VDD
E13	D_IN0_02	F13	D_IN0_02_N	H1	UNUSED	L4	VSS
E14	D_IN0_04	F14	D_IN0_04_N	H2	UNUSED	L5	NC
E15	D_IN0_06	F15	D_IN0_06_N	H3	NC	L6	NC
E16	D_IN0_08	F16	D_IN0_08_N	H4	NC	L34	NC
E17	D_IN0_11	F17	D_IN0_11_N	H5	NC	L35	NC
E18	D_IN0_13	F18	D_IN0_13_N	H6	NC	L36	VSS
E19	D_IN0_15_N	F19	VDD2	H34	NC	L37	VDD
E20	VDD2	F20	VDD2	H35	NC	L38	NC
E21	D_IN1_15_N	F21	VDD2	H36	NC	L39	NC
E22	D_IN1_13	F22	D_IN1_13_N	H37	NC	M1	UNUSED
E23	D_IN1_11	F23	D_IN1_11_N	H38	NC	M2	UNUSED
E24	D_IN1_08	F24	D_IN1_08_N	H39	NC	M3	NC
E25	D_IN1_06	F25	D_IN1_06_N	J1	NC	M4	NC
E26	D_IN1_04	F26	D_IN1_04_N	J2	NC	M5	NC
E27	D_IN1_02	F27	D_IN1_02_N	J3	VSS	M6	NC
E28	VDDA	F28	VSSA	J4	VDD2	M34	NC
E29	D_OUT1_01	F29	D_OUT1_01_N	J5	NC	M35	NC
E30	D_OUT1_03	F30	D_OUT1_03_N	J6	NC	M36	NC
E31	REF10_1	F31	REF14_1	J34	NC	M37	NC
E32	D_OUT1_06	F32	D_OUT1_06_N	J35	NC	M38	UNUSED
E33	D_OUT1_09	F33	D_OUT1_09_N	J36	VDD2	M39	UNUSED
E34	VDD2	F34	VDD2	J37	VSS	N1	UNUSED
E35	VDD2	F35	VDD2	J38	NC	N2	UNUSED
E36	D_OUT1_13	F36	NC	J39	NC	N3	VSS
E37	D_OUT1_13_N	F37	NC	K1	NC	N4	VDD2
E38	NC	F38	NC	K2	NC	N5	UNUSED
E39	NC	F39	NC	K3	NC	N6	UNUSED

Notes:
Do not connect pins designated as NC (no connect pins).
Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 1. Pin Assignments for 792-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
N34	UNUSED	T37	ADDRESS_8	Y1	VDD	AC4	VDD2
N35	UNUSED	T38	ADDRESS_7	Y2	VDD	AC5	NC
N36	VDD2	T39	ADDRESS_6	Y3	VSS	AC6	NC
N37	VSS	U1	NC	Y4	VSS	AC34	DATA_9
N38	UNUSED	U2	NC	Y5	VDD2	AC35	DATA_8
N39	NC	U3	VSS	Y6	VDD2	AC36	VDD2
P1	NC	U4	VDD2	Y34	VDD2	AC37	VSS
P2	UNUSED	U5	NC	Y35	VDD2	AC38	DATA_7
P3	NC	U6	NC	Y36	VSS	AC39	DATA_6
P4	UNUSED	U34	ADDRESS_5	Y37	VSS	AD1	UNUSED
P5	UNUSED	U35	ADDRESS_4	Y38	VDD	AD2	UNUSED
P6	UNUSED	U36	VDD2	Y39	VDD	AD3	UNUSED
P34	DXP	U37	VSS	AA1	UNUSED	AD4	NC
P35	DXN	U38	ADDRESS_3	AA2	VDD	AD5	UNUSED
P36	NC	U39	ADDRESS_2	AA3	VSS	AD6	CTAP_CLK_FP
P37	NC	V1	TRST_N	AA4	UNUSED	AD34	PARITY_1
P38	NC	V2	TDO	AA5	RST_N	AD35	PARITY_0
P39	NC	V3	TSTMD_N	AA6	VDD2	AD36	DATA_13
R1	NC	V4	SCANEN_N	AA34	VDD2	AD37	DATA_12
R2	NC	V5	NC	AA35	SYNC_N	AD38	DATA_11
R3	VDD	V6	NC	AA36	INT_N	AD39	DATA_10
R4	VSS	V34	ADDRESS_1	AA37	VSS	AE1	NC
R5	NC	V35	ADDRESS_0	AA38	VDD	AE2	NC
R6	NC	V36	MPMODE_1	AA39	UNUSED	AE3	VDD
R34	UNUSED	V37	MPMODE_0	AB1	HIZ_N	AE4	VSS
R35	NC	V38	CS_N	AB2	NC	AE5	SYS_CLK_N
R36	VSS	V39	TS_N	AB3	NC	AE6	SYS_CLK
R37	VDD	W1	TCK	AB4	NC	AE34	UNUSED
R38	ADDRESS_11	W2	VDD	AB5	NC	AE35	UNUSED
R39	ADDRESS_10	W3	VSS	AB6	NC	AE36	VSS
T1	NC	W4	TDI	AB34	DATA_5	AE37	VDD
T2	NC	W5	TMS	AB35	DATA_4	AE38	DATA_15
T3	NC	W6	VDD2	AB36	DATA_3	AE39	DATA_14
T4	NC	W34	VDD2	AB37	DATA_2	AF1	SYS_FP_N
T5	NC	W35	DS_N	AB38	DATA_1	AF2	SYS_FP
T6	NC	W36	RW_N	AB39	DATA_0	AF3	NC
T34	UNUSED	W37	VSS	AC1	NC	AF4	UNUSED
T35	ADDRESS_12	W38	VDD	AC2	NC	AF5	NC
T36	ADDRESS_9	W39	PCLK	AC3	VSS	AF6	NC

Notes:
Do not connect pins designated as NC (no connect pins).

Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 1. Pin Assignments for 792-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
AF34	UNUSED	AJ37	VDD	AN1	NC	AP28	VSSA
AF35	UNUSED	AJ38	NC	AN2	NC	AP29	D_OUT2_01_N
AF36	UNUSED	AJ39	NC	AN3	VDD	AP30	D_OUT2_03_N
AF37	UNUSED	AK1	NC	AN4	VSS	AP31	RESHI_2
AF38	TEA_N	AK2	NC	AN5	NC	AP32	D_OUT2_06_N
AF39	TA_N	AK3	NC	AN6	NC	AP33	D_OUT2_09_N
AG1	UNUSED	AK4	NC	AN34	D_OUT2_14	AP34	VDD2
AG2	UNUSED	AK5	NC	AN35	D_OUT2_14_N	AP35	VDD2
AG3	VSS	AK6	NC	AN36	VSS	AP36	NC
AG4	VDD2	AK34	NC	AN37	VDD	AP37	NC
AG5	NC	AK35	NC	AN38	NC	AP38	NC
AG6	NC	AK36	NC	AN39	NC	AP39	NC
AG34	UNUSED	AK37	NC	AP1	NC	AR1	NC
AG35	UNUSED	AK38	NC	AP2	NC	AR2	NC
AG36	VDD2	AK39	NC	AP3	NC	AR3	NC
AG37	VSS	AL1	NC	AP4	NC	AR4	NC
AG38	UNUSED	AL2	NC	AP5	VDD2	AR5	VDD2
AG39	UNUSED	AL3	VSS	AP6	VDD2	AR6	VDD2
AH1	NC	AL4	VDD2	AP7	NC	AR7	NC
AH2	NC	AL5	NC	AP8	NC	AR8	NC
AH3	NC	AL6	NC	AP9	NC	AR9	NC
AH4	NC	AL34	NC	AP10	NC	AR10	NC
AH5	NC	AL35	NC	AP11	NC	AR11	NC
AH6	NC	AL36	VDD2	AP12	VSSA	AR12	VDDA
AH34	NC	AL37	VSS	AP13	NC	AR13	NC
AH35	NC	AL38	NC	AP14	NC	AR14	NC
AH36	NC	AL39	NC	AP15	NC	AR15	NC
AH37	NC	AM1	NC	AP16	NC	AR16	NC
AH38	UNUSED	AM2	NC	AP17	NC	AR17	NC
AH39	UNUSED	AM3	NC	AP18	NC	AR18	NC
AJ1	NC	AM4	NC	AP19	VDD2	AR19	NC
AJ2	NC	AM5	NC	AP20	VDD2	AR20	VDD2
AJ3	VDD	AM6	NC	AP21	VDD2	AR21	D_IN2_15_N
AJ4	VSS	AM34	NC	AP22	D_IN2_13_N	AR22	D_IN2_13
AJ5	NC	AM35	NC	AP23	D_IN2_11_N	AR23	D_IN2_11
AJ6	NC	AM36	NC	AP24	D_IN2_08_N	AR24	D_IN2_08
AJ34	NC	AM37	NC	AP25	D_IN2_06_N	AR25	D_IN2_06
AJ35	NC	AM38	UNUSED	AP26	D_IN2_04_N	AR26	D_IN2_04
AJ36	VSS	AM39	UNUSED	AP27	D_IN2_02_N	AR27	D_IN2_02

Notes:
Do not connect pins designated as NC (no connect pins).

Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 1. Pin Assignments for 792-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
AR28	VDDA	AT31	VDD2	AU34	D_OUT2_07	AV37	D_OUT2_11_N
AR29	D_OUT2_01	AT32	UNUSED	AU35	D_OUT2_10	AV38	VDD
AR30	D_OUT2_03	AT33	VSS	AU36	VSS	AV39	VDD
AR31	RESLO_2	AT34	D_OUT2_07_N	AU37	VSS	AW1	VDD
AR32	D_OUT2_06	AT35	D_OUT2_10_N	AU38	D_OUT2_12	AW2	VDD
AR33	D_OUT2_09	AT36	VSS	AU39	D_OUT2_12_N	AW3	NC
AR34	VDD2	AT37	VSS	AV1	VDD	AW4	NC
AR35	VDD2	AT38	D_OUT2_15	AV2	VDD	AW5	NC
AR36	D_OUT2_13	AT39	D_OUT2_15_N	AV3	NC	AW6	NC
AR37	D_OUT2_13_N	AU1	NC	AV4	NC	AW7	NC
AR38	NC	AU2	NC	AV5	NC	AW8	NC
AR39	NC	AU3	VSS	AV6	NC	AW9	NC
AT1	NC	AU4	VSS	AV7	NC	AW10	NC
AT2	NC	AU5	NC	AV8	NC	AW11	NC
AT3	VSS	AU6	NC	AV9	NC	AW12	NC
AT4	VSS	AU7	VDD	AV10	NC	AW13	NC
AT5	NC	AU8	UNUSED	AV11	NC	AW14	NC
AT6	NC	AU9	VSS	AV12	NC	AW15	NC
AT7	VSS	AU10	UNUSED	AV13	NC	AW16	NC
AT8	UNUSED	AU11	VDD	AV14	NC	AW17	NC
AT9	VDD2	AU12	NC	AV15	NC	AW18	NC
AT10	UNUSED	AU13	VSS	AV16	NC	AW19	UNUSED
AT11	VSS	AU14	NC	AV17	NC	AW20	VDD
AT12	NC	AU15	VDD	AV18	NC	AW21	UNUSED
AT13	VDD2	AU16	NC	AV19	VDD	AW22	D_IN2_14
AT14	UNUSED	AU17	VSS	AV20	VDD	AW23	D_IN2_12
AT15	VSS	AU18	NC	AV21	VDD	AW24	D_IN2_10
AT16	UNUSED	AU19	VSS	AV22	D_IN2_14_N	AW25	D_IN2_09
AT17	VDD2	AU20	VSS	AV23	D_IN2_12_N	AW26	D_IN2_07
AT18	UNUSED	AU21	VSS	AV24	D_IN2_10_N	AW27	D_IN2_05
AT19	NC	AU22	CTAP2_3	AV25	D_IN2_09_N	AW28	D_IN2_03
AT20	VSS	AU23	VSS	AV26	D_IN2_07_N	AW29	D_IN2_01
AT21	D_IN2_15	AU24	CTAP2_2	AV27	D_IN2_05_N	AW30	D_IN2_00
AT22	UNUSED	AU25	VDD	AV28	D_IN2_03_N	AW31	D_OUT2_00
AT23	VDD2	AU26	CTAP2_1	AV29	D_IN2_01_N	AW32	D_OUT2_02
AT24	UNUSED	AU27	VSS	AV30	D_IN2_00_N	AW33	D_OUT2_04
AT25	VSS	AU28	CTAP2_0	AV31	D_OUT2_00_N	AW34	D_OUT2_05
AT26	UNUSED	AU29	VDD	AV32	D_OUT2_02_N	AW35	REF14_2
AT27	VDD2	AU30	UNUSED	AV33	D_OUT2_04_N	AW36	D_OUT2_08
AT28	REXT2	AU31	VSS	AV34	D_OUT2_05_N	AW37	D_OUT2_11
AT29	VSS	AU32	UNUSED	AV35	REF10_2	AW38	VDD
AT30	UNUSED	AU33	VDD	AV36	D_OUT2_08_N	AW39	VDD

Notes:
Do not connect pins designated as NC (no connect pins).

Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 2. Pin Assignments for 792-Pin LBGA by Signal Name Order

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
ADDRESS_0	V35	D_IN0_04	E14	D_IN1_07_N	B26	D_IN2_11	AR23
ADDRESS_1	V34	D_IN0_04_N	F14	D_IN1_08	E24	D_IN2_11_N	AP23
ADDRESS_2	U39	D_IN0_05	A13	D_IN1_08_N	F24	D_IN2_12	AW23
ADDRESS_3	U38	D_IN0_05_N	B13	D_IN1_09	A25	D_IN2_12_N	AV23
ADDRESS_4	U35	D_IN0_06	E15	D_IN1_09_N	B25	D_IN2_13	AR22
ADDRESS_5	U34	D_IN0_06_N	F15	D_IN1_10	A24	D_IN2_13_N	AP22
ADDRESS_6	T39	D_IN0_07	A14	D_IN1_10_N	B24	D_IN2_14	AW22
ADDRESS_7	T38	D_IN0_07_N	B14	D_IN1_11	E23	D_IN2_14_N	AV22
ADDRESS_8	T37	D_IN0_08	E16	D_IN1_11_N	F23	D_IN2_15	AT21
ADDRESS_9	T36	D_IN0_08_N	F16	D_IN1_12	A23	D_IN2_15_N	AR21
ADDRESS_10	R39	D_IN0_09	A15	D_IN1_12_N	B23	NC	AW10
ADDRESS_11	R38	D_IN0_09_N	B15	D_IN1_13	E22	NC	AV10
ADDRESS_12	T35	D_IN0_10	A16	D_IN1_13_N	F22	NC	AW11
CS_N	V38	D_IN0_10_N	B16	D_IN1_14	A22	NC	AV11
CTAP_CLK_FP	AD6	D_IN0_11	E17	D_IN1_14_N	B22	NC	AR13
CTAP0_0	C12	D_IN0_11_N	F17	D_IN1_15	D21	NC	AP13
CTAP0_1	C14	D_IN0_12	A17	D_IN1_15_N	E21	NC	AW12
CTAP0_2	C16	D_IN0_12_N	B17	D_IN2_00	AW30	NC	AV12
CTAP0_3	C18	D_IN0_13	E18	D_IN2_00_N	AV30	NC	AR14
CTAP1_0	C28	D_IN0_13_N	F18	D_IN2_01	AW29	NC	AP14
CTAP1_1	C26	D_IN0_14	A18	D_IN2_01_N	AV29	NC	AW13
CTAP1_2	C24	D_IN0_14_N	B18	D_IN2_02	AR27	NC	AV13
CTAP1_3	C22	D_IN0_15	D19	D_IN2_02_N	AP27	NC	AR15
CTAP2_0	AU28	D_IN0_15_N	E19	D_IN2_03	AW28	NC	AP15
CTAP2_1	AU26	D_IN1_00	A30	D_IN2_03_N	AV28	NC	AW14
CTAP2_2	AU24	D_IN1_00_N	B30	D_IN2_04	AR26	NC	AV14
CTAP2_3	AU22	D_IN1_01	A29	D_IN2_04_N	AP26	NC	AR16
NC	AU12	D_IN1_01_N	B29	D_IN2_05	AW27	NC	AP16
NC	AU14	D_IN1_02	E27	D_IN2_05_N	AV27	NC	AW15
NC	AU16	D_IN1_02_N	F27	D_IN2_06	AR25	NC	AV15
NC	AU18	D_IN1_03	A28	D_IN2_06_N	AP25	NC	AW16
D_IN0_00	A10	D_IN1_03_N	B28	D_IN2_07	AW26	NC	AV16
D_IN0_00_N	B10	D_IN1_04	E26	D_IN2_07_N	AV26	NC	AR17
D_IN0_01	A11	D_IN1_04_N	F26	D_IN2_08	AR24	NC	AP17
D_IN0_01_N	B11	D_IN1_05	A27	D_IN2_08_N	AP24	NC	AW17
D_IN0_02	E13	D_IN1_05_N	B27	D_IN2_09	AW25	NC	AV17
D_IN0_02_N	F13	D_IN1_06	E25	D_IN2_09_N	AV25	NC	AR18
D_IN0_03	A12	D_IN1_06_N	F25	D_IN2_10	AW24	NC	AP18
D_IN0_03_N	B12	D_IN1_07	A26	D_IN2_10_N	AV24	NC	AW18

Notes:
Do not connect pins designated as NC (no connect pins).
Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 2. Pin Assignments for 792-Pin LBGA by Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
NC	AV18	D_OUT1_02	A32	D_OUT2_05_N	AV34	NC	AR7
NC	AT19	D_OUT1_02_N	B32	D_OUT2_06	AR32	NC	AP7
NC	AR19	D_OUT1_03	E30	D_OUT2_06_N	AP32	NC	AU5
D_OUT0_00	A9	D_OUT1_03_N	F30	D_OUT2_07	AU34	NC	AT5
D_OUT0_00_N	B9	D_OUT1_04	A33	D_OUT2_07_N	AT34	NC	AW3
D_OUT0_01	E11	D_OUT1_04_N	B33	D_OUT2_08	AW36	NC	AV3
D_OUT0_01_N	F11	D_OUT1_05	A34	D_OUT2_08_N	AV36	NC	AU2
D_OUT0_02	A8	D_OUT1_05_N	B34	D_OUT2_09	AR33	NC	AU1
D_OUT0_02_N	B8	D_OUT1_06	E32	D_OUT2_09_N	AP33	NC	AR4
D_OUT0_03	E10	D_OUT1_06_N	F32	D_OUT2_10	AU35	NC	AR3
D_OUT0_03_N	F10	D_OUT1_07	C34	D_OUT2_10_N	AT35	NC	AN6
D_OUT0_04	A7	D_OUT1_07_N	D34	D_OUT2_11	AW37	NC	AN5
D_OUT0_04_N	B7	D_OUT1_08	A36	D_OUT2_11_N	AV37	NC	AT2
D_OUT0_05	A6	D_OUT1_08_N	B36	D_OUT2_12	AU38	NC	AT1
D_OUT0_05_N	B6	D_OUT1_09	E33	D_OUT2_12_N	AU39	DATA_0	AB39
D_OUT0_06	E8	D_OUT1_09_N	F33	D_OUT2_13	AR36	DATA_1	AB38
D_OUT0_06_N	F8	D_OUT1_10	C35	D_OUT2_13_N	AR37	DATA_2	AB37
D_OUT0_07	C6	D_OUT1_10_N	D35	D_OUT2_14	AN34	DATA_3	AB36
D_OUT0_07_N	D6	D_OUT1_11	A37	D_OUT2_14_N	AN35	DATA_4	AB35
D_OUT0_08	A4	D_OUT1_11_N	B37	D_OUT2_15	AT38	DATA_5	AB34
D_OUT0_08_N	B4	D_OUT1_12	C38	D_OUT2_15_N	AT39	DATA_6	AC39
D_OUT0_09	E7	D_OUT1_12_N	C39	NC	AW9	DATA_7	AC38
D_OUT0_09_N	F7	D_OUT1_13	E36	NC	AV9	DATA_8	AC35
D_OUT0_10	C5	D_OUT1_13_N	E37	NC	AR11	DATA_9	AC34
D_OUT0_10_N	D5	D_OUT1_14	G34	NC	AP11	DATA_10	AD39
D_OUT0_11	A3	D_OUT1_14_N	G35	NC	AW8	DATA_11	AD38
D_OUT0_11_N	B3	D_OUT1_15	D38	NC	AV8	DATA_12	AD37
D_OUT0_12	C2	D_OUT1_15_N	D39	NC	AR10	DATA_13	AD36
D_OUT0_12_N	C1	D_OUT2_00	AW31	NC	AP10	DATA_14	AE39
D_OUT0_13	E4	D_OUT2_00_N	AV31	NC	AW7	DATA_15	AE38
D_OUT0_13_N	E3	D_OUT2_01	AR29	NC	AV7	DS_N	W35
D_OUT0_14	G6	D_OUT2_01_N	AP29	NC	AW6	DXN	P35
D_OUT0_14_N	G5	D_OUT2_02	AW32	NC	AV6	DXP	P34
D_OUT0_15	D2	D_OUT2_02_N	AV32	NC	AR8	HIZ_N	AB1
D_OUT0_15_N	D1	D_OUT2_03	AR30	NC	AP8	INT_N	AA36
D_OUT1_00	A31	D_OUT2_03_N	AP30	NC	AU6	MPMODE_0	V37
D_OUT1_00_N	B31	D_OUT2_04	AW33	NC	AT6	MPMODE_1	V36
D_OUT1_01	E29	D_OUT2_04_N	AV33	NC	AW4	NC	E1
D_OUT1_01_N	F29	D_OUT2_05	AW34	NC	AV4	NC	E2

Notes:
Do not connect pins designated as NC (no connect pins).

Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 2. Pin Assignments for 792-Pin LBGA by Signal Name Order (continued)

Signal Name	Pin
NC	E38
NC	E39
NC	F1
NC	F2
NC	F3
NC	F4
NC	F36
NC	F37
NC	F38
NC	F39
NC	G1
NC	G2
NC	G38
NC	G39
NC	H3
NC	H4
NC	H5
NC	H6
NC	H34
NC	H35
NC	H36
NC	H37
NC	H38
NC	H39
NC	J1
NC	J2
NC	J5
NC	J6
NC	J34
NC	J35
NC	J38
NC	J39
NC	K1
NC	K2
NC	K3
NC	K4
NC	K5
NC	K6
NC	K34
NC	K35
NC	K36
NC	K37
NC	K38
NC	K39
NC	L1
NC	L2
NC	L5
NC	L6
NC	L34
NC	L35
NC	L38
NC	L39
NC	M3
NC	M4
NC	M5
NC	M6
NC	M34
NC	M35
NC	M36
NC	M37
NC	N39
NC	P1
NC	P3
NC	P36
NC	P37
NC	P38
NC	P39
NC	R1
NC	R2
NC	R5
NC	R6
NC	R35
NC	T1
NC	T2
NC	T3
NC	T4
NC	T5
NC	T6
NC	U1
NC	U2
NC	U5
NC	U6
NC	V5
NC	V6
NC	AB2
NC	AB3
NC	AB4
NC	AB5
NC	AB6
NC	AC1
NC	AC2
NC	AC5
NC	AC6
NC	AD4
NC	AE1
NC	AE2
NC	AF3
NC	AF5
NC	AF6
NC	AG5
NC	AG6
NC	AH1
NC	AH2
NC	AH3
NC	AH4
NC	AH5
NC	AH6
NC	AH34
NC	AH35
NC	AH36
NC	AH37
NC	AJ1
NC	AJ2
NC	AJ5
NC	AJ6
NC	AJ34
NC	AJ35
NC	AJ38
NC	AJ39
NC	AK1
NC	AK2
NC	AK3
NC	AK4
NC	AK5
NC	AK6
NC	AK34
NC	AK35
NC	AK36
NC	AK37
NC	AK38
NC	AK39
NC	AL1
NC	AL2
NC	AL5
NC	AL6
NC	AL34
NC	AL35
NC	AL38
NC	AL39
NC	AM1
NC	AM2
NC	AM3
NC	AM4
NC	AM5
NC	AM6
NC	AM34
NC	AM35
NC	AM36
NC	AM37
NC	AN1
NC	AN2
NC	AN38
NC	AN39
NC	AP1
NC	AP2
NC	AP3

Notes:
Do not connect pins designated as NC (no connect pins).

Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 2. Pin Assignments for 792-Pin LBGA by Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
NC	AP4	SYS_FP_N	AF1	UNUSED	P2	UNUSED	AT32
NC	AP36	TA_N	AF39	UNUSED	P4	UNUSED	AU8
NC	AP37	TCK	W1	UNUSED	P5	UNUSED	AU10
NC	AP38	TDI	W4	UNUSED	P6	UNUSED	AU30
NC	AP39	TDO	V2	UNUSED	R34	UNUSED	AU32
NC	AR1	TEA_N	AF38	UNUSED	T34	UNUSED	AW19
NC	AR2	TMS	W5	UNUSED	AA1	UNUSED	AW21
NC	AR38	TRST_N	V1	UNUSED	AA4	VDD	A1
NC	AR39	TS_N	V39	UNUSED	AA39	VDD	A2
PARITY_0	AD35	TSTMD_N	V3	UNUSED	AD1	VDD	A20
PARITY_1	AD34	UNUSED	A19	UNUSED	AD2	VDD	A38
PCLK	W39	UNUSED	A21	UNUSED	AD3	VDD	A39
REF10_0	B5	UNUSED	C8	UNUSED	AD5	VDD	B1
REF10_1	E31	UNUSED	C10	UNUSED	AE34	VDD	B2
REF10_2	AV35	UNUSED	C30	UNUSED	AE35	VDD	B19
NC	AR9	UNUSED	C32	UNUSED	AF4	VDD	B20
REF14_0	A5	UNUSED	D8	UNUSED	AF34	VDD	B21
REF14_1	F31	UNUSED	D10	UNUSED	AF35	VDD	B38
REF14_2	AW35	UNUSED	D14	UNUSED	AF36	VDD	B39
NC	AP9	UNUSED	D16	UNUSED	AF37	VDD	C7
RESHI_0	F9	UNUSED	D18	UNUSED	AG1	VDD	C11
RESHI_1	A35	UNUSED	D22	UNUSED	AG2	VDD	C15
RESHI_2	AP31	UNUSED	D24	UNUSED	AG34	VDD	C25
NC	AW5	UNUSED	D26	UNUSED	AG35	VDD	C29
RESLO_0	E9	UNUSED	D30	UNUSED	AG38	VDD	C33
RESLO_1	B35	UNUSED	D32	UNUSED	AG39	VDD	G3
RESLO_2	AR31	UNUSED	H1	UNUSED	AH38	VDD	G37
NC	AV5	UNUSED	H2	UNUSED	AH39	VDD	L3
REXT0	D12	UNUSED	M1	UNUSED	AM38	VDD	L37
REXT1	D28	UNUSED	M2	UNUSED	AM39	VDD	R3
REXT2	AT28	UNUSED	M38	UNUSED	AT8	VDD	R37
NC	AT12	UNUSED	M39	UNUSED	AT10	VDD	W2
RST_N	AA5	UNUSED	N1	UNUSED	AT14	VDD	W38
RW_N	W36	UNUSED	N2	UNUSED	AT16	VDD	Y1
SCANEN_N	V4	UNUSED	N5	UNUSED	AT18	VDD	Y2
SYNC_N	AA35	UNUSED	N6	UNUSED	AT22	VDD	Y38
SYS_CLK	AE6	UNUSED	N34	UNUSED	AT24	VDD	Y39
SYS_CLK_N	AE5	UNUSED	N35	UNUSED	AT26	VDD	AA2
SYS_FP	AF2	UNUSED	N38	UNUSED	AT30	VDD	AA38

Notes:
Do not connect pins designated as NC (no connect pins).
Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 2. Pin Assignments for 792-Pin LBGA by Signal Name Order (continued)

Signal Name	Pin
VDD	AE3
VDD	AE37
VDD	AJ3
VDD	AJ37
VDD	AN3
VDD	AN37
VDD	AU7
VDD	AU11
VDD	AU15
VDD	AU25
VDD	AU29
VDD	AU33
VDD	AV1
VDD	AV2
VDD	AV19
VDD	AV20
VDD	AV21
VDD	AV38
VDD	AV39
VDD	AW1
VDD	AW2
VDD	AW20
VDD	AW38
VDD	AW39
VDD2	D9
VDD2	D13
VDD2	D17
VDD2	D23
VDD2	D27
VDD2	D31
VDD2	E5
VDD2	E6
VDD2	E20
VDD2	E34
VDD2	E35
VDD2	F5
VDD2	F6
VDD2	F19
VDD2	F20
VDD2	F21
VDD2	F34
VDD2	F35
VDD2	J4
VDD2	J36
VDD2	N4
VDD2	N36
VDD2	U4
VDD2	U36
VDD2	W6
VDD2	W34
VDD2	Y5
VDD2	Y6
VDD2	Y34
VDD2	Y35
VDD2	AA6
VDD2	AA34
VDD2	AC4
VDD2	AC36
VDD2	AG4
VDD2	AG36
VDD2	AL4
VDD2	AL36
VDD2	AP5
VDD2	AP6
VDD2	AP19
VDD2	AP20
VDD2	AP21
VDD2	AP34
VDD2	AP35
VDD2	AR5
VDD2	AR6
VDD2	AR20
VDD2	AR34
VDD2	AR35
VDD2	AT9
VDD2	AT13
VDD2	AT17
VDD2	AT23
VDD2	AT27
VDD2	AT31
VDDA	E12
VDDA	E28
VDDA	AR12
VDDA	AR28
VSS	C3
VSS	C4
VSS	C9
VSS	C13
VSS	C17
VSS	C19
VSS	C20
VSS	C21
VSS	C23
VSS	C27
VSS	C31
VSS	C36
VSS	C37
VSS	D3
VSS	D4
VSS	D7
VSS	D11
VSS	D15
VSS	D20
VSS	D25
VSS	D29
VSS	D33
VSS	D36
VSS	D37
VSS	G4
VSS	G36
VSS	J3
VSS	J37
VSS	L4
VSS	L36
VSS	N3
VSS	N37
VSS	R4
VSS	R36
VSS	U3
VSS	U37
VSS	W3
VSS	W37
VSS	Y3
VSS	Y4
VSS	Y36
VSS	Y37
VSS	AA3
VSS	AA37
VSS	AC3
VSS	AC37
VSS	AE4
VSS	AE36
VSS	AG3
VSS	AG37
VSS	AJ4
VSS	AJ36
VSS	AL3
VSS	AL37
VSS	AN4
VSS	AN36
VSS	AT3
VSS	AT4
VSS	AT7
VSS	AT11
VSS	AT15
VSS	AT20
VSS	AT25
VSS	AT29
VSS	AT33
VSS	AT36
VSS	AT37
VSS	AU3
VSS	AU4
VSS	AU9
VSS	AU13
VSS	AU17
VSS	AU19
VSS	AU20
VSS	AU21
VSS	AU23
VSS	AU27
VSS	AU31
VSS	AU36
VSS	AU37
VSSA	F12
VSSA	F28
VSSA	AP12
VSSA	AP28

Notes:
Do not connect pins designated as NC (no connect pins).

Pins designated as UNUSED (unused pins) have no connection between the pin and the die.

Pin Information (continued)

Table 3. Pin Descriptions—Receive Interface

Note: The speed for each channel below is 622.08 Mbits/s.

Pin	Symbol	Type*	Name/Description
A10 B10	D_IN0_00 D_IN0_00_N	I LVDS	**Port 0 Input 0.** LVDS data input pair for port 0, channel 0.
A11 B11	D_IN0_01 D_IN0_01_N	I LVDS	**Port 0 Input 1.** LVDS data input pair for port 0, channel 1.
E13 F13	D_IN0_02 D_IN0_02_N	I LVDS	**Port 0 Input 2.** LVDS data input pair for port 0, channel 2.
A12 B12	D_IN0_03 D_IN0_03_N	I LVDS	**Port 0 Input 3.** LVDS data input pair for port 0, channel 3.
E14 F14	D_IN0_04 D_IN0_04_N	I LVDS	**Port 0 Input 4.** LVDS data input pair for port 0, channel 4.
A13 B13	D_IN0_05 D_IN0_05_N	I LVDS	**Port 0 Input 5.** LVDS data input pair for port 0, channel 5.
E15 F15	D_IN0_06 D_IN0_06_N	I LVDS	**Port 0 Input 6.** LVDS data input pair for port 0, channel 6.
A14 B14	D_IN0_07 D_IN0_07_N	I LVDS	**Port 0 Input 7.** LVDS data input pair for port 0, channel 7.
E16 F16	D_IN0_08 D_IN0_08_N	I LVDS	**Port 0 Input 8.** LVDS data input pair for port 0, channel 8.
A15 B15	D_IN0_09 D_IN0_09_N	I LVDS	**Port 0 Input 9.** LVDS data input pair for port 0, channel 9.
A16 B16	D_IN0_10 D_IN0_10_N	I LVDS	**Port 0 Input 10.** LVDS data input pair for port 0, channel 10.
E17 F17	D_IN0_11 D_IN0_11_N	I LVDS	**Port 0 Input 11.** LVDS data input pair for port 0, channel 11.
A17 B17	D_IN0_12 D_IN0_12_N	I LVDS	**Port 0 Input 12.** LVDS data input pair for port 0, channel 12.
E18 F18	D_IN0_13 D_IN0_13_N	I LVDS	**Port 0 Input 13.** LVDS data input pair for port 0, channel 13.
A18 B18	D_IN0_14 D_IN0_14_N	I LVDS	**Port 0 Input 14.** LVDS data input pair for port 0, channel 14.
D19 E19	D_IN0_15 D_IN0_15_N	I LVDS	**Port 0 Input 15.** LVDS data input pair for port 0, channel 15.
C18 C16 C14 C12	CTAP0_3 CTAP0_2 CTAP0_1 CTAP0_0	—	**Center Taps for Port 0 Inputs.** Provides center-tapped common-mode termination. These inputs should be terminated through individual external 0.01 µF capacitors to ground.

* I = input, LVDS = low-voltage differential signal.

Pin Information (continued)

Table 3. Pin Descriptions—Receive Interface (continued)

Note: The speed for each channel below is 622.08 Mbits/s.

Pin	Symbol	Type*	Name/Description
A30 B30	D_IN1_00 D_IN1_00_N	I LVDS	**Port 1 Input 0.** LVDS data input pair for port 1, channel 0.
A29 B29	D_IN1_01 D_IN1_01_N	I LVDS	**Port 1 Input 1.** LVDS data input pair for port 1, channel 1.
E27 F27	D_IN1_02 D_IN1_02_N	I LVDS	**Port 1 Input 2.** LVDS data input pair for port 1, channel 2.
A28 B28	D_IN1_03 D_IN1_03_N	I LVDS	**Port 1 Input 3.** LVDS data input pair for port 1, channel 3.
E26 F26	D_IN1_04 D_IN1_04_N	I LVDS	**Port 1 Input 4.** LVDS data input pair for port 1, channel 4.
A27 B27	D_IN1_05 D_IN1_05_N	I LVDS	**Port 1 Input 5.** LVDS data input pair for port 1, channel 5.
E25 F25	D_IN1_06 D_IN1_06_N	I LVDS	**Port 1 Input 6.** LVDS data input pair for port 1, channel 6.
A26 B26	D_IN1_07 D_IN1_07_N	I LVDS	**Port 1 Input 7.** LVDS data input pair for port 1, channel 7.
E24 F24	D_IN1_08 D_IN1_08_N	I LVDS	**Port 1 Input 8.** LVDS data input pair for port 1, channel 8.
A25 B25	D_IN1_09 D_IN1_09_N	I LVDS	**Port 1 Input 9.** LVDS data input pair for port 1, channel 9.
A24 B24	D_IN1_10 D_IN1_10_N	I LVDS	**Port 1 Input 10.** LVDS data input pair for port 1, channel 10.
E23 F23	D_IN1_11 D_IN1_11_N	I LVDS	**Port 1 Input 11.** LVDS data input pair for port 1, channel 11.
A23 B23	D_IN1_12 D_IN1_12_N	I LVDS	**Port 1 Input 12.** LVDS data input pair for port 1, channel 12.
E22 F22	D_IN1_13 D_IN1_13_N	I LVDS	**Port 1 Input 13.** LVDS data input pair for port 1, channel 13.
A22 B22	D_IN1_14 D_IN1_14_N	I LVDS	**Port 1 Input 14.** LVDS data input pair for port 1, channel 14.
D21 E21	D_IN1_15 D_IN1_15_N	I LVDS	**Port 1 Input 15.** LVDS data input pair for port 1, channel 15.
C22 C24 C26 C28	CTAP1_3 CTAP1_2 CTAP1_1 CTAP1_0	—	**Center Taps for Port 1 Inputs.** Provides center-tapped common-mode termination. These inputs should be terminated through individual external 0.01 µF capacitors to ground.

* I = input, LVDS = low-voltage differential signal.

Pin Information (continued)

Table 3. Pin Descriptions—Receive Interface (continued)

Note: The speed for each channel below is 622.08 Mbits/s.

Pin	Symbol	Type*	Name/Description
AW30 AV30	D_IN2_00 D_IN2_00_N	I LVDS	**Port 2 Input 0.** LVDS data input pair for port 2, channel 0.
AW29 AV29	D_IN2_01 D_IN2_01_N	I LVDS	**Port 2 Input 1.** LVDS data input pair for port 2, channel 1.
AR27 AP27	D_IN2_02 D_IN2_02_N	I LVDS	**Port 2 Input 2.** LVDS data input pair for port 2, channel 2.
AW28 AV28	D_IN2_03 D_IN2_03_N	I LVDS	**Port 2 Input 3.** LVDS data input pair for port 2, channel 3.
AR26 AP26	D_IN2_04 D_IN2_04_N	I LVDS	**Port 2 Input 4.** LVDS data input pair for port 2, channel 4.
AW27 AV27	D_IN2_05 D_IN2_05_N	I LVDS	**Port 2 Input 5.** LVDS data input pair for port 2, channel 5.
AR25 AP25	D_IN2_06 D_IN2_06_N	I LVDS	**Port 2 Input 6.** LVDS data input pair for port 2, channel 6.
AW26 AV26	D_IN2_07 D_IN2_07_N	I LVDS	**Port 2 Input 7.** LVDS data input pair for port 2, channel 7.
AR24 AP24	D_IN2_08 D_IN2_08_N	I LVDS	**Port 2 Input 8.** LVDS data input pair for port 2, channel 8.
AW25 AV25	D_IN2_09 D_IN2_09_N	I LVDS	**Port 2 Input 9.** LVDS data input pair for port 2, channel 9.
AW24 AV24	D_IN2_10 D_IN2_10_N	I LVDS	**Port 2 Input 10.** LVDS data input pair for port 2, channel 10.
AR23 AP23	D_IN2_11 D_IN2_11_N	I LVDS	**Port 2 Input 11.** LVDS data input pair for port 2, channel 11.
AW23 AV23	D_IN2_12 D_IN2_12_N	I LVDS	**Port 2 Input 12.** LVDS data input pair for port 2, channel 12.
AR22 AP22	D_IN2_13 D_IN2_13_N	I LVDS	**Port 2 Input 13.** LVDS data input pair for port 2, channel 13.
AW22 AV22	D_IN2_14 D_IN2_14_N	I LVDS	**Port 2 Input 14.** LVDS data input pair for port 2, channel 14.
AT21 AR21	D_IN2_15 D_IN2_15_N	I LVDS	**Port 2 Input 15.** LVDS data input pair for port 2, channel 15.
AU22 AU24 AU26 AU28	CTAP2_3 CTAP2_2 CTAP2_1 CTAP2_0	—	**Center Taps for Port 2 Inputs.** Provides center-tapped common-mode termination. These inputs should be terminated through individual external 0.01 µF capacitors to ground.

* I = input, LVDS = low-voltage differential signal.

Pin Information (continued)

Table 4. Pin Descriptions—Transmit Interface

Note: The speed for each channel below is 622.08 Mbits/s.

Pin	Symbol	Type*	Name/Description
A9 B9	D_OUT0_00 D_OUT0_00_N	O LVDS	**Port 0 Output 0.** LVDS output pair for port 0, channel 0.
E11 F11	D_OUT0_01 D_OUT0_01_N	O LVDS	**Port 0 Output 1.** LVDS output pair for port 0, channel 1.
A8 B8	D_OUT0_02 D_OUT0_02_N	O LVDS	**Port 0 Output 2.** LVDS output pair for port 0, channel 2.
E10 F10	D_OUT0_03 D_OUT0_03_N	O LVDS	**Port 0 Output 3.** LVDS output pair for port 0, channel 3.
A7 B7	D_OUT0_04 D_OUT0_04_N	O LVDS	**Port 0 Output 4.** LVDS output pair for port 0, channel 4.
A6 B6	D_OUT0_05 D_OUT0_05_N	O LVDS	**Port 0 Output 5.** LVDS output pair for port 0, channel 5.
E8 F8	D_OUT0_06 D_OUT0_06_N	O LVDS	**Port 0 Output 6.** LVDS output pair for port 0, channel 6.
C6 D6	D_OUT0_07 D_OUT0_07_N	O LVDS	**Port 0 Output 7.** LVDS output pair for port 0, channel 7.
A4 B4	D_OUT0_08 D_OUT0_08_N	O LVDS	**Port 0 Output 8.** LVDS output pair for port 0, channel 8.
E7 F7	D_OUT0_09 D_OUT0_09_N	O LVDS	**Port 0 Output 9.** LVDS output pair for port 0, channel 9.
C5 D5	D_OUT0_10 D_OUT0_10_N	O LVDS	**Port 0 Output 10.** LVDS output pair for port 0, channel 10.
A3 B3	D_OUT0_11 D_OUT0_11_N	O LVDS	**Port 0 Output 11.** LVDS output pair for port 0, channel 11.
C2 C1	D_OUT0_12 D_OUT0_12_N	O LVDS	**Port 0 Output 12.** LVDS output pair for port 0, channel 12.
E4 E3	D_OUT0_13 D_OUT0_13_N	O LVDS	**Port 0 Output 13.** LVDS output pair for port 0, channel 13.
G6 G5	D_OUT0_14 D_OUT0_14_N	O LVDS	**Port 0 Output 14.** LVDS output pair for port 0, channel 14.
D2 D1	D_OUT0_15 D_OUT0_15_N	O LVDS	**Port 0 Output 15.** LVDS output pair for port 0, channel 15.

* O = output, LVDS = low-voltage differential signal.

Pin Information (continued)

Table 4. Pin Descriptions—Transmit Interface (continued)

Note: The speed for each channel below is 622.08 Mbits/s.

Pin	Symbol	Type*	Name/Description
A31 B31	D_OUT1_00 D_OUT1_00_N	O LVDS	**Port 1 Output 0.** LVDS output pair for port 1, channel 0.
E29 F29	D_OUT1_01 D_OUT1_01_N	O LVDS	**Port 1 Output 1.** LVDS output pair for port 1, channel 1.
A32 B32	D_OUT1_02 D_OUT1_02_N	O LVDS	**Port 1 Output 2.** LVDS output pair for port 1, channel 2.
E30 F30	D_OUT1_03 D_OUT1_03_N	O LVDS	**Port 1 Output 3.** LVDS output pair for port 1, channel 3.
A33 B33	D_OUT1_04 D_OUT1_04_N	O LVDS	**Port 1 Output 4.** LVDS output pair for port 1, channel 4.
A34 B34	D_OUT1_05 D_OUT1_05_N	O LVDS	**Port 1 Output 5.** LVDS output pair for port 1, channel 5.
E32 F32	D_OUT1_06 D_OUT1_06_N	O LVDS	**Port 1 Output 6.** LVDS output pair for port 1, channel 6.
C34 D34	D_OUT1_07 D_OUT1_07_N	O LVDS	**Port 1 Output 7.** LVDS output pair for port 1, channel 7.
A36 B36	D_OUT1_08 D_OUT1_08_N	O LVDS	**Port 1 Output 8.** LVDS output pair for port 1, channel 8.
E33 F33	D_OUT1_09 D_OUT1_09_N	O LVDS	**Port 1 Output 9.** LVDS output pair for port 1, channel 9.
C35 D35	D_OUT1_10 D_OUT1_10_N	O LVDS	**Port 1 Output 10.** LVDS output pair for port 1, channel 10.
A37 B37	D_OUT1_11 D_OUT1_11_N	O LVDS	**Port 1 Output 11.** LVDS output pair for port 1, channel 11.
C38 C39	D_OUT1_12 D_OUT1_12_N	O LVDS	**Port 1 Output 12.** LVDS output pair for port 1, channel 12.
E36 E37	D_OUT1_13 D_OUT1_13_N	O LVDS	**Port 1 Output 13.** LVDS output pair for port 1, channel 13.
G34 G35	D_OUT1_14 D_OUT1_14_N	O LVDS	**Port 1 Output 14.** LVDS output pair for port 1, channel 14.
D38 D39	D_OUT1_15 D_OUT1_15_N	O LVDS	**Port 1 Output 15.** LVDS output pair for port 1, channel 15.

* O = output, LVDS = low-voltage differential signal.

Pin Information (continued)

Table 4. Pin Descriptions—Transmit Interface (continued)

Note: The speed for each channel below is 622.08 Mbits/s.

Pin	Symbol	Type*	Name/Description
AW31 AV31	D_OUT2_00 D_OUT2_00_N	O LVDS	**Port 2 Output 0.** LVDS output pair for port 2, channel 0.
AR29 AP29	D_OUT2_01 D_OUT2_01_N	O LVDS	**Port 2 Output 1.** LVDS output pair for port 2, channel 1.
AW32 AV32	D_OUT2_02 D_OUT2_02_N	O LVDS	**Port 2 Output 2.** LVDS output pair for port 2, channel 2.
AR30 AP30	D_OUT2_03 D_OUT2_03_N	O LVDS	**Port 2 Output 3.** LVDS output pair for port 2, channel 3.
AW33 AV33	D_OUT2_04 D_OUT2_04_N	O LVDS	**Port 2 Output 4.** LVDS output pair for port 2, channel 4.
AW34 AV34	D_OUT2_05 D_OUT2_05_N	O LVDS	**Port 2 Output 5.** LVDS output pair for port 2, channel 5.
AR32 AP32	D_OUT2_06 D_OUT2_06_N	O LVDS	**Port 2 Output 6.** LVDS output pair for port 2, channel 6.
AU34 AT34	D_OUT2_07 D_OUT2_07_N	O LVDS	**Port 2 Output 7.** LVDS output pair for port 2, channel 7.
AW36 AV36	D_OUT2_08 D_OUT2_08_N	O LVDS	**Port 2 Output 8.** LVDS output pair for port 2, channel 8.
AR33 AP33	D_OUT2_09 D_OUT2_09_N	O LVDS	**Port 2 Output 9.** LVDS output pair for port 2, channel 9.
AU35 AT35	D_OUT2_10 D_OUT2_10_N	O LVDS	**Port 2 Output 10.** LVDS output pair for port 2, channel 10.
AW37 AV37	D_OUT2_11 D_OUT2_11_N	O LVDS	**Port 2 Output 11.** LVDS output pair for port 2, channel 11.
AU38 AU39	D_OUT2_12 D_OUT2_12_N	O LVDS	**Port 2 Output 12.** LVDS output pair for port 2, channel 12.
AR36 AR37	D_OUT2_13 D_OUT2_13_N	O LVDS	**Port 2 Output 13.** LVDS output pair for port 2, channel 13.
AN34 AN35	D_OUT2_14 D_OUT2_14_N	O LVDS	**Port 2 Output 14.** LVDS output pair for port 2, channel 14.
AT38 AT39	D_OUT2_15 D_OUT2_15_N	O LVDS	**Port 2 Output 15.** LVDS output pair for port 2, channel 15.

* O = output, LVDS = low-voltage differential signal.

Pin Information (continued)

Table 5. Pin Descriptions—LVDS Reference Cell Pins

Pin	Symbol	Type*	Name/Description
B5	REF10_0	I	**1.0 V Reference Voltage for Port 0.**
E31	REF10_1	I	**1.0 V Reference Voltage for Port 1.**
AV35	REF10_2	I	**1.0 V Reference Voltage for Port 2.**
AR9	REF10_3	I	**1.0 V Reference Voltage for Port 3.**
A5	REF14_0	I	**1.4 V Reference Voltage for Port 0.**
F31	REF14_1	I	**1.4 V Reference Voltage for Port 1.**
AW35	REF14_2	I	**1.4 V Reference Voltage for Port 2.**
AP9	REF14_3	I	**1.4 V Reference Voltage for Port 3.**
F9	RESHI_0	—	Connect a 100 Ω ± 1% resistor between these two pins.
E9	RESLO_0	—	
A35	RESHI_1	—	Connect a 100 Ω ± 1% resistor between these two pins.
B35	RESLO_1	—	
AP31	RESHI_2	—	Connect a 100 Ω ± 1% resistor between these two pins.
AR31	RESLO_2	—	
AW5	RESHI_3	—	Connect a 100 Ω ± 1% resistor between these two pins.
AV5	RESLO_3	—	

* I = input.

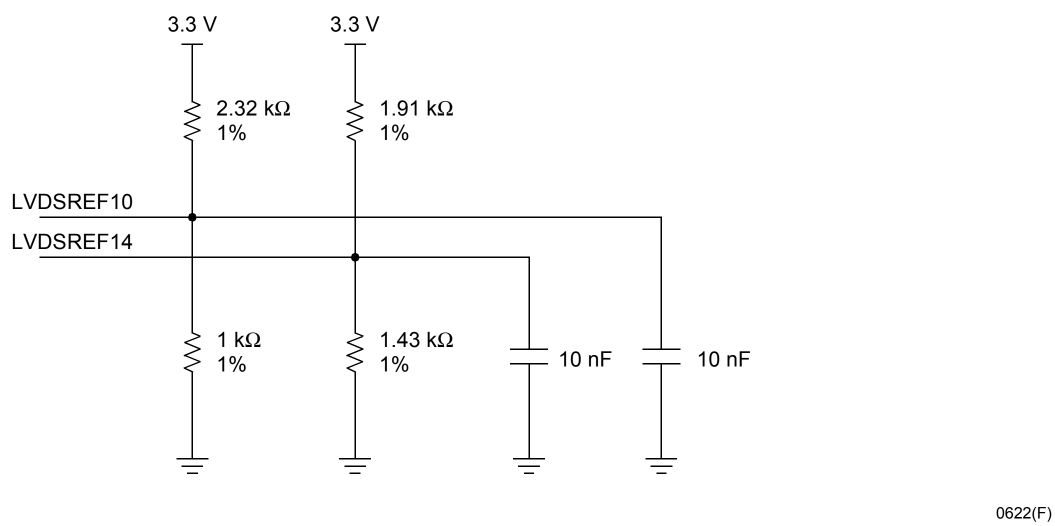


Figure 3. Suggested Schematic for 1.0 V and 1.4 V Reference Voltages

Pin Information (continued)

Table 6. Pin Descriptions—Microprocessor Interface

Pin	Symbol	Type*	Name/Description
V36 V37	MPMODE_1 MPMODE_0	I	**Microprocessor Mode.** These pins must be driven to select a microprocessor mode. 00 = Asynchronous mode—M360 (*Motorola*† MC68360, for example). 01 = DSP synchronous mode (*Motorola* DSP56309, for example). 10 = Synchronous mode—M860 (*Motorola* MPC860, for example). 11 = Synchronous mode, no parity—M860 (MPC860, for example).
W39	PCLK	I	**Microprocessor Clock.** Must be provided in order to read and write to any register. Rising edge.
V38	CS_N	I	**Chip Select (Active-Low).** This signal must be low during register access. Requires an external pull-up resistor of 10 kΩ.
V39	TS_N	I	**Transfer Start or Address Strobe (Active-Low).** Transfer start when MPMODE = 01, 10, or 11 (synchronous). Address strobe when MPMODE = 00 (asynchronous). Requires an external pull-up resistor of 10 kΩ.
W35	DS_N	I	**Data Strobe (Active-Low).** This signal, when used in the asynchronous mode (MPMODE = 00), indicates that the data is valid for MPU writes. Requires an external pull-up resistor of 10 kΩ for M860 and DSP modes.
W36	RW_N	I	**Read/$\overline{\text{Write}}$.** This signal is low to indicate a write operation and is high to indicate a read operation.
AF39	TA_N	O	**Data Transfer Acknowledge (Active-Low).** This signal acknowledges the data transfer cycle. Requires an external pull-up resistor of 10 kΩ.
AF38	TEA_N	O	**Transfer Error Acknowledge (Active-Low).** This signal goes low to indicate an internal error related to the data transfer cycle. Requires an external pull-up resistor of 10 kΩ.
AA36	INT_N	O	**Interrupt (Active-Low).** This signal goes low when the device generates an unmasked interrupt. Requires an external pull-up resistor of 10 kΩ. It is an open-drain output.
T35	ADDRESS_12	I	**Address Bus [12:0].** This bus is used to address registers for the microprocessor.
R38	ADDRESS_11	I	
R39	ADDRESS_10	I	
T36	ADDRESS_9	I	
T37	ADDRESS_8	I	
T38	ADDRESS_7	I	
T39	ADDRESS_6	I	
U34	ADDRESS_5	I	
U35	ADDRESS_4	I	
U38	ADDRESS_3	I	
U39	ADDRESS_2	I	
V34	ADDRESS_1	I	
V35	ADDRESS_0	I	

* I = input, I^U = input with internal pull-up resistor, O^U = output with internal pull-up resistor. Non-LVDS inputs and outputs are 3.3 V CMOS, 5 V compatible, and TTL-compatible.
† *Motorola* is a registered trademark of Motorola, Inc.

Pin Information (continued)

Table 6. Pin Descriptions—Microprocessor Interface (continued)

Pin	Symbol	Type*	Name/Description
AE38	DATA_15	I/O	Data Bus [15:0]. This bus is a bidirectional data bus for writing and reading software registers.
AE39	DATA_14	I/O	
AD36	DATA_13	I/O	
AD37	DATA_12	I/O	
AD38	DATA_11	I/O	
AD39	DATA_10	I/O	
AC34	DATA_9	I/O	
AC35	DATA_8	I/O	
AC38	DATA_7	I/O	
AC39	DATA_6	I/O	
AB34	DATA_5	I/O	
AB35	DATA_4	I/O	
AB36	DATA_3	I/O	
AB37	DATA_2	I/O	
AB38	DATA_1	I/O	
AB39	DATA_0	I/O	
AD34	PARITY_1	I/O	**Data Bus Parity—Upper Byte.** Odd parity for upper byte [15:8].
AD35	PARITY_0	I/O	**Data Bus Parity—Lower Byte.** Odd parity for lower byte [7:0].

* I/O^{u} = bidirectional pin with internal pull-up resistor. Non-LVDS inputs, outputs, and bidirects are 3.3 V CMOS, 5 V compatible, and TTL-compatible.

Table 7. Pin Descriptions—System Control

Pin	Symbol	Type*	Name/Description
AE6 AE5	SYS_CLK SYS_CLK_N	I LVDS	**System Clock.** Must be provided in order to read and write to any register. LVDS input pair for the 155.52 MHz system reference clock.
AF2 AF1	SYS_FP SYS_FP_N	I LVDS	**System Frame Pulse.** LVDS input pair for the 8 kHz system frame pulse. The frame is defined as beginning on the rising edge of the system frame pulse. The frame pulse is synchronous to SYS_CLK.
AD6	CTAP_CLK_FP	—	**Center Tap for Clock and Frame Pulse.** Center tap for SYS_CLK and SYS_FP input buffers. This input should be terminated through an external 0.01 µF capacitor to ground.
AA35	SYNC_N	I/O	**Switch Synchronization (Active-Low).** Requires an external pull-up resistor of 10 kΩ. It is an open-drain output.
AA5	RST_N	I	**Asynchronous Chip Reset (Active-Low).** This input incorporates hysteresis. Setting this input to 0 causes an asynchronous reset of the device. To ensure proper reset, this input should be held low for a minimum of 26 ns (at least two 77.76 MHz clock cycles). Requires an external pull-up resistor of 10 kΩ.
AB1	HIZ_N	I^{u}	**Global Pin 3-State Control (Active-Low).** This input incorporates hysteresis. Setting this input to 0 causes all TDCS4810G outputs to assume a high-impedance state except for the JTAG test data output (TDO) pin.
P34	DXP	—	**Temperature Sensing Diode Anode.**
P35	DXN	—	**Temperature Sensing Diode Cathode.**

* I = input, I^{u}/O = bidirectional pin with internal pull-up resistor. Non-LVDS inputs, outputs, and bidirects are 3.3 V CMOS, 5 V compatible, and TTL-compatible.

Pin Information (continued)

Table 8. Pin Descriptions—PLL References

Pin	Symbol	Type	Name/Description
D12	REXT0	—	**External PLL Bypass Resistor—Port 0.** Should be externally connected through a 10 kΩ ± 1% resistor to PLL analog ground (V_{SSA}).
D28	REXT1	—	**External PLL Bypass Resistor—Port 1.** Should be externally connected through a 10 kΩ ± 1% resistor to PLL analog ground (V_{SSA}).
AT28	REXT2	—	**External PLL Bypass Resistor—Port 2.** Should be externally connected through a 10 kΩ ± 1% resistor to PLL analog ground (V_{SSA}).

Table 9. Pin Descriptions—JTAG Interface

Pin	Symbol	Type*	Name/Description
W1	TCK	I^u	**Test Clock.** This signal provides timing for test operations.
W5	TMS	I^u	**Test Mode Select.** Controls test operations. TMS is sampled on the rising edge of TCK.
W4	TDI	I^u	**Test Data In.** TDI is sampled on the rising edge of TCK.
V2	TDO	O	**Test Data Out.** This output is updated on the falling edge of TCK. The TDO output is 3-stated except when scanning out test data.
V1	TRST_N	I^u	**Test Reset (Active-Low).** This signal provides an asynchronous reset for the TAP. **Note:** This input should be tied low (to V_{SS}) for normal device operation. If TRST_N is high, a TCK must be present to ensure that the correct test mode is clocked in on the TMS input.
V3	TSTMD_N	I^u	**Scan Test Mode (Active-Low).**
V4	SCANEN_N	I^u	**Scan Mode Enable (Active-Low).**

* O = output, I^u = input with internal pull-up resistor. Non-LVDS inputs and outputs are 3.3 V CMOS, 5 V compatible, and TTL-compatible.

Pin Information (continued)

Table 10. Pin Descriptions—Power and Ground

Pin	Symbol	Type*	Name/Description
D9, D13, D17, D23, D27, D31, E5, E6, E20, E34, E35, F5, F6, F19, F20, F21, F34, F35, J4, J36, N4, N36, U4, U36, W6, W34, Y5, Y6, Y34, Y35, AA6, AA34, AC4, AC36, AG4, AG36, AL4, AL36, AP5, AP6, AP19, AP20, AP21, AP34, AP35, AR5, AR6, AR20, AR34, AR35, AT9, AT13, AT17, AT23, AT27, AT31	VDD2	I	**1.5 V Internal Supply Voltage ±5%.** Provides 1.5 V internal to the device.
A1, A2, A20, A38, A39, B1, B2, B19, B20, B21, B38, B39, C7, C11, C15, C25, C29, C33, G3, G37, L3, L37, R3, R37, W2, W38, Y1, Y2, Y38, Y39, AA2, AA38, AE3, AE37, AJ3, AJ37, AN3, AN37, AU7, AU11, AU15, AU25, AU29, AU33, AV1, AV2, AV19, AV20, AV21, AV38, AV39, AW1, AW2, AW20, AW38, AW39	VDD	I	**3.3 V I/O Supply Voltage ±5%.** Provides 3.3 V to the I/O pins.

* I = input.

Pin Information (continued)

Table 10. Pin Descriptions—Power and Ground (continued)

Pin	Symbol	Type*	Name/Description
C3, C4, C9, C13, C17, C19, C20, C21, C23, C27, C31, C36, C37, D3, D4, D7, D11, D15, D20, D25, D29, D33, D36, D37, G4, G36, J3, J37, L4, L36, N3, N37, R4, R36, U3, U37, W3, W37, Y3, Y4, Y36, Y37, AA3, AA37, AC3, AC37, AE4, AE36, AG3, AG37, AJ4, AJ36, AL3, AL37, AN4, AN36, AT3, AT4, AT7, AT11, AT15, AT20, AT25, AT29, AT33, AT36, AT37, AU3, AU4, AU9, AU13, AU17, AU19, AU20, AU21, AU23, AU27, AU31, AU36, AU37	VSS	I	**Digital Ground.**
E12 E28 AR12 AR28	VDDA	I	**1.5 V Analog Positive Supply Voltage for PLL Circuits ±5%.** Power dissipation is 0.28 W (See Absolute Maximum Ratings on page 72).
F12 F28 AP12 AP28	VSSA	I	**Analog Ground for PLL Circuits.**

* I = input.

Pin Information (continued)

Table 11. Pin Descriptions—No Connect

Pin	Symbol	Type*	Name/Description
E1, E2, E38, E39, F1, F2, F3, F4, F36, F37, F38, F39, G1, G2, G38, G39, H3, H4, H5, H6, H34, H35, H36, H37, H38, H39, J1, J2, J5, J6, J34, J35, J38, J39, K1, K2, K3, K4, K5, K6, K34, K35, K36, K37, K38, K39, L1, L2, L5, L6, L34, L35, L38, L39, M3, M4, M5, M6, M34, M35, M36, M37, N39, P1, P3, P36, P37, P38, P39, R1, R2, R5, R6, R35, T1, T2, T3, T4, T5, T6, U1, U2, U5, U6, V5, V6, AB2, AB3, AB4, AB5, AB6, AC1, AC2, AC5, AC6, AD4, AE1, AE2, AF3, AF5, AF6, AG5, AG6, AH1, AH2, AH3, AH4, AH5, AH6, AH34, AH35, AH36, AH37, AJ1, AJ2, AJ5, AJ6, AJ34, AJ35, AJ38, AJ39, AK1, AK2, AK3, AK4, AK5, AK6, AK34, AK35, AK36, AK37, AK38, AK39, AL1, AL2, AL5, AL6, AL34, AL35, AL38, AL39, AM1, AM2, AM3, AM4, AM5, AM6	NC	—	**No Connect.** Do not connect these pins. Includes internal manufacturing test pins.

* Non-LVDS inputs and outputs are 3.3 V CMOS, 5 V compatible, and TTL-compatible.

Pin Information (continued)

Table 11. Pin Descriptions—No Connect (continued)

Pin	Symbol	Type*	Name/Description
AM34, AM35, AM36, AM37, AN1, AN2, AN38, AN39, AP1, AP2, AP3, AP4, AP7, AP8, AP9, AP10, AP11, AP13, AP14, AP15, AP16, AP17, AP18, AP36, AP37, AP38, AP39, AR1, AR2, AR3, AR4, AR7, AR8, AR9, AR10, AR11, AR13, AR14, AR15, AR16, AR17, AR18, AR19, AR38, AR39, AT1, AT2, AT5, AT6, AT12, AT19, AU1, AU2, AU3, AU6, AU12, AU14, AU16, AU18, AV4, AV5, AV6, AV7, AV8, AV9, AV10, AV11, AV12, AV13, AV14, AV15, AV16, AV17, AV18, AW3, AW4, AW5, AW6, AW7, AW8, AW9, AW10, AW11, AW12, AW13, AW14, AW15, AW16, AW17, AW18	NC	—	**No Connect.** Do not connect these pins. Includes internal manufacturing test pins.

* Non-LVDS inputs and outputs are 3.3 V CMOS, 5 V compatible, and TTL-compatible.

Pin Information (continued)

Table 12. Pin Descriptions—Unused Pins

Pin	Symbol	Type*	Name/Description
A19, A21, C8, C10, C30, C32, D8, D10, D14, D16, D18, D22, D24, D26, D30, D32, H1, H2, M1, M2, M38, M39, N1, N2, N5, N6, N34, N35, N38, P2, P4, P5, P6, R34, T34, AA1, AA4, AA39, AD1, AD2, AD3, AD5, AE34, AE35, AF4, AF34, AF35, AF36, AF37, AG1, AG2, AG34, AG35, AG38, AG39, AH38, AH39, AM38, AM39, AT8, AT10, AT14, AT16, AT18, AT22, AT24, AT26, AT30, AT32, AU8, AU10, AU30, AU32, AW19, AW21	UNUSED	—	**Unused Pins.** These pins are unused, and there is no connection between the pin and the die.

* Non-LVDS inputs and outputs are 3.3 V CMOS, 5 V compatible, and TTL-compatible.

Pin Information (continued)

Table 13. Pin Summary

Pin Type	Pin Direction	Count
LVDS	Input	100
	Output	96
	Reference Cell Pins	12
CMOS	Input	28
	Output	4
	Bidirectional	19
NC		238
UNUSED		75
Other (Center taps, external resistors, diodes)		23
Power		116
Ground		84
Total		792

Overview

Byte Ordering

Each channel carries an STS-12 worth of data. The ordering of bytes within the STS-12 is shown in Table 14. In the case of an STS-192, each of the STS-12 channels comprising the STS-192 carries an STS-12 extracted from the STS-192. The byte ordering in this case is shown in Table 15. STS-48 ordering follows the same format, with each constituent STS-12 of the STS-48 entering the chip on separate channels.

Table 14. STS-12 Byte Ordering

Timeslot	0	1	2	3	4	5	6	7	8	9	10	11
Byte	1	4	7	10	2	5	8	11	3	6	9	12

Table 15. STS-192 Byte Ordering

Time (Left to Right for each STS-12 Channel) ⇒												STS-12 Number
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	
1	4	7	10	2	5	8	11	3	6	9	12	0
13	16	19	22	14	17	20	23	15	18	21	24	1
25	28	31	34	26	29	32	35	27	30	33	36	2
37	40	43	46	38	41	44	47	39	42	45	48	3
49	52	55	58	50	53	56	59	51	54	57	60	4
61	64	67	70	62	65	68	71	63	66	69	72	5
73	76	79	82	74	77	80	83	75	78	81	84	6
85	88	91	94	86	89	92	95	87	90	93	96	7
97	100	103	106	98	101	104	107	99	102	105	108	8
109	112	115	118	110	113	116	119	111	114	117	120	9
121	124	127	130	122	125	128	131	123	126	129	132	10
133	136	139	142	134	137	140	143	135	138	141	144	11
145	148	151	154	146	149	152	155	147	150	153	156	12
157	160	163	166	158	161	164	167	159	162	165	168	13
169	172	175	178	170	173	176	179	171	174	177	180	14
181	184	187	190	182	185	188	191	183	186	189	192	15

Receive Interface

Receiver Operations

The receiver is composed of 48 STS-12 channels that are either treated as independent channels, treated as three groups of 16 channels each, forming three STS-192 streams, or treated as 16 groups of three channels each, forming 12 STS-48 streams. Incoming data for each channel is received through an LVDS serial port operating at 622 Mbits/s. The incoming serial stream frequency must be the same as the outgoing LVDS serial stream of the transmitter. Each STS-192 interface (16 channels) uses the system clock (SYS_CLK) as a reference clock.

The receiver is able to handle STS-12 streams having combined static and dynamic frame offsets of up to 64 bytes without creating any traffic disruption.

Overview (continued)

Receive Interface (continued)

The receiver consists of the following major blocks: the clock and data recovery (CDR), the framer, and the FIFO aligner.

The CDR is responsible for recovering clock and data. It interfaces directly with the framer by providing an 8-bit parallel data output and the recovered 77.76 MHz clock. Note that parallel data is not byte-aligned at this point.

The framer is responsible for locking onto the STS-12 frame. It does so by first finding the byte boundary within the received 8-bit data bus and then identifying A1/A2 transitions.

Receiver behavior during an LOF condition is under software control. It is possible to select either insert AIS or pass-through when an LOF condition occurs (per-channel control). It is also possible to force AIS on a per-channel basis.

Note: AIS forces all bytes to ones. Moreover, occurrence of LOF on a specific channel does not have any impact on all other in-frame channels.

The FIFO aligner is responsible for aligning the 48 STS-12 frames to the system frame pulse for proper cross connect operation. The FIFO aligner is 64-bytes deep and thus provides room for aligning channels having frame offsets of up to 64 bytes. The 64-byte window is determined by the system frame pulse and a software-programmable offset register. The FIFO is designed so that some streams can be taken from the outputs of another cross connect without the need to realign the frame position (due to delay through the first cross connect). Thus, the offset register should be programmed so that the FIFO causes as little delay as possible through the cross connect. Since the FIFO aligner for each channel is independent, the state of any FIFO will not affect any other FIFO. (See FIFO Aligner section for more details, page 44.)

Cross Connect

Cross Connect Operations

The cross connect has 48 input channels and 48 output channels. Each channel operates at 77.76 MHz and thus carries an STS-12 worth of bandwidth. The channels can also be thought of as three bidirectional STS-192 data streams.

The cross connect is fully programmable and non-blocking. Each STS-1 of each output channel is independently programmed to connect to any STS-1 from any input channel.

The basic architecture of the cross connect consists of a time-slot interchange (TSI) macro, a connection memory, E1/F1/E2 extraction, APS byte handling, and AIS/UNEQ insertion.

Time-Slot Interchanger (TSI)

A TSI is used to reorder the STS-1 data. Incoming data is written into one of two buffers in a regular order, while output data is read from another buffer in an order dependent on the address provided to the TSI for each channel. When one buffer has been completely written to, the read and write buffers switch. This is controlled by a synchronization input.

Connection Memory

The connection memory is used to configure the TSI to switch the incoming STS-1s to the desired output STS-1s. There is a working memory to configure the working connections for each STS-1, and there is a protected memory to configure the protection connection for each STS-1. Each of the working and protected memories are duplicated (A and B) to allow for easy software configuration. The four memories are working A, working B, protected A, and protected B.

The memory that is used for switching is selectable by software. Configuration A or configuration B memory is selected per-STS-12 (channel). This can be used for line switching or for software preconfiguration. For example, if a new configuration is required, and a particular STS-12 is using configuration A memory (working or protected), the new configuration is programmed into configuration B memory (working and protected), and then the STS-12 is switched to use configuration B.

Working or protected memory is selected per STS-1 or per channel. This is configurable for each channel. Switching on an STS-1 basis can be used for path switching applications while switching on a per-channel basis can be used for line switching applications. For example, if a particular STS-1 is using the working A memory, it can be switched to the configuration in protected A memory without affecting any other STS-1s.

Synchronization

Any software-programmed switch from one connection memory to another will take effect on an A1/A2 boundary. Triggers are ignored and the switch is made at the

Overview (continued)

Cross Connect (continued)

next A1/A2 boundary; the switch is made during the S1 byte time. The trigger for a switch is configurable on a per-channel basis. The possible triggers are the following:

- The SYNC_N pin.
- A chip-level control bit.
- The S1 byte received in the channel has changed to or from the value 0xF0.
- The S1 byte received in a particular channel (selected at the top level) has changed to or from the value 0xF0.

APS Byte Handling

The K1 and K2 bytes of the STS-1 of each channel are monitored for a change. If a change is detected, a latched alarm is raised. The received value is stored and is available in a status register. The LTE is responsible for validating the K bytes and ensuring only the validated value is sent on the STS-1 of the channel. Agere LTE chips support this function.

The APS bytes (K1, K2) along with the data communication bytes (D1—D12) and the line status (E2) can optionally be switched separately, regardless of the content of the connection memory. Each output channel can source these bytes (for all STS-1s in the channel) from any input channel, bypassing the maps programmed into the connection memories. This allows these bytes to take a different path through a system than the data, easing APS operations in a system with multiple cross connects.

Note: When changing the source of these bytes via a register write, the change occurs immediately and is not synchronized to the frame boundary.

The K1 and K2 bytes of the outgoing channels can be overridden with a software-programmable value (programmed on a per-channel basis). The software-programmed values are inserted in the second time slot (STS-1 #4) of the output channel, allowing the validated bytes to pass through from the input to make them available to subsequent equipment. To use the inserted values for APS, the LTE must be able to insert the K1 and K2 from the second time slot into the correct APS byte positions on the output line. Agere LTE chips support this function.

E1/F1/E2 Extraction

The E1 and F1 bytes of each STS-1 carry information indicating the path status of that STS-1. Both bytes contain the same information. This information can be used by software to initiate a switch from working to protected configurations. The E1 and F1 bytes are extracted from STS-1s at the output of the TSI and stored.

The bytes are monitored for a change and, if a change is detected, latched alarms (E1F1ALM, E2ALM) are set (see Register Descriptions, page 66 and page 62 respectively).

The received values can be read through the microprocessor interface. A single read will return both the E1 and F1 value for a particular STS-1.

The E2 byte of the STS-1 of each STS-12 (channel) carries information indicating the line status of that STS-12. This information can be used by software to initiate a switch from working to protected configurations.

AIS/UNEQ Insertion

Path AIS and UNEQ indications can be inserted on any STS-1 under software control. This ensures that downstream path processors will detect a normal pointer and will thus be able to extract the path overhead in order to detect an UNEQ defect. AIS/UNEQ insertion does not affect E1/F1 or E2 values (or any of the TOH).

AIS insertion takes precedence over UNEQ insertion. Changes to the AIS/UNEQ microprocessor registers will not take effect until the next frame boundary.

Overview (continued)

Transmit Interface

The transmitter is composed of 48 STS-12 channels that are always treated as independent channels. Each of the outgoing LVDS serial streams of the transmitter transmits at a rate of 622 Mbits/s, and the data is synchronized to the system clock (SYS_CLK).

SPE and TOH data received through the cross connect is transferred, unaltered, to the serial LVDS output. However, the B1 byte of STS-1 #1 is always replaced with a new calculated value (the 11 bytes following B1 are replaced with all zeros). Also, A1 and A2 bytes of all STS-1s are always regenerated.

TOH bytes on LVDS outputs are as shown in Figure 4.

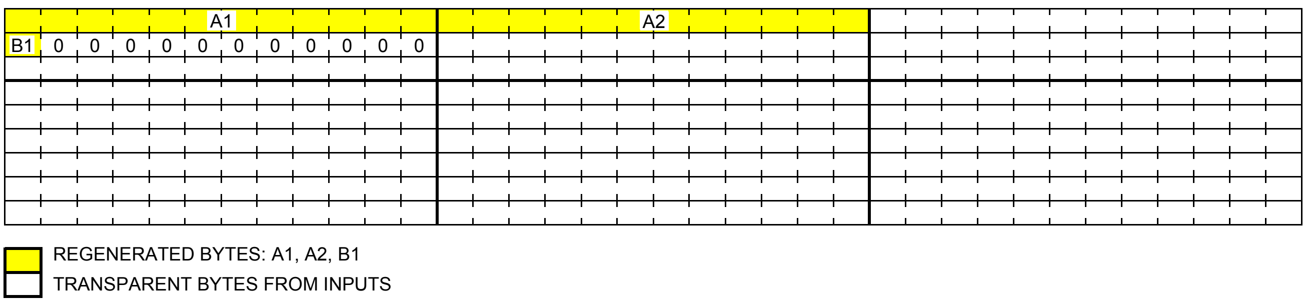
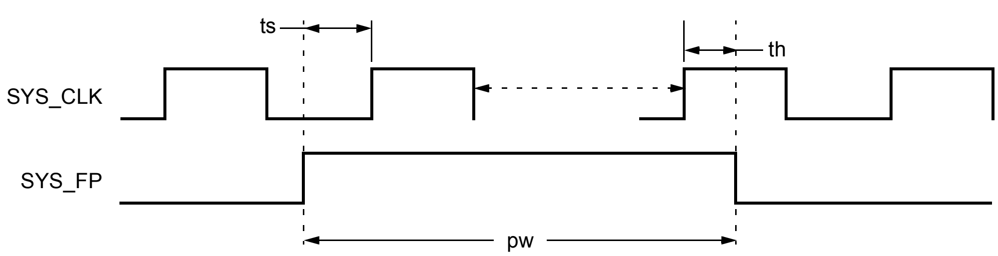


Figure 4. Transmitter TOH on LVDS Output

Frame Pulse

The input frame pulse should be synchronous to the input 155.52 MHz clock. It is then internally synchronized to the 77.76 MHz clock that is generated from the 155.52 MHz system clock. The frame pulse, in combination with the frame pulse offset register, determines the alignment of the frame internal to the device. If the frame pulse occurs, it must occur for at least eight frames (1 ms) since the previous frame pulse, and must occur in multiples of 125 µs (one frame). The minimum time that must elapse after the rising edge of the frame pulse before the SYS_CLK can correctly sample the frame pulse is 2 ns. See Figure 5 below.



Notes:
ts = minimum 2 ns.

th = minimum 1 ns.

pw = minimum 6.43 ns FP_MODE = 1.

pw = minimum 51.44 ns FP_MODE = 0 (default).

pw can be longer than the minimum, and the hold time for the falling edge of the pulse is not critical as long as the minimum width has been exceeded.

Figure 5. SYS_FP Timing Requirements

Overview (continued)

Frame Pulse (continued)

If SYS_CLK rises in under 2 ns after the rising edge of the frame pulse, the SYS_CLK will not sample the frame pulse until its next rising edge.

The frame pulse detection is configured by a device-level control bit (FP_MODE). The frame pulse can be a one (or more) clock wide pulse or it can be an eight (or more) clock wide pulse (in reference to the 155.52 MHz system clock). For normal operation, the device can be set to one or more clocks. If the frame pulse comes from a source that encodes the S1 byte onto the frame pulse signal with manchester encoding, then the frame pulse detection must be set to four or more clocks. This ensures that the manchester-encoded S1 does not interfere with framing.

Microprocessor Interface

Architecture

The TDCS4810G microprocessor interface architecture is configured for glueless interface to two specific microprocessors, the *Motorola* MPC860 and the MC68360, and to the *Motorola* DSP56309 digital signal processor; however, other processors may also be used, as long as the bus cycles comply with those of the MPC860, DSP56309, or the MC68360. Bus transfers using the MC68360 are asynchronous, while the MPC860 and DSP56309 transfers are synchronous to the processor clock. When the MPC860 is used, parity is generated and checked on the data bus.

The microprocessor interface operates at the frequency of the microprocessor clock (PCLK) input. The state of the MPMODE input signal determines whether bus transfers are synchronous or asynchronous with respect to PCLK.

The TDCS4810G has a separate 13-bit wide address bus and a 16-bit wide data bus. The microprocessor interface generates an external processor bus error (from pin TEA_N) if an internal data acknowledgment is not received in a predetermined period of time or on parity errors.

Transfer Error Acknowledge (Pin TEA_N)

The TDCS4810G contains a bus time-out counter. When this counter saturates, a bus error is generated to the external processor through the transfer error acknowledge signal pin TEA_N. This feature must be considered with respect to the external processor's ability to generate its own internal bus time-out. Transfer error acknowledge will be asserted if an internal data acknowledgment is not received within 32 PCLK periods of the start of the access. This interval is used since all valid internal accesses to the device will be completed in significantly less than 32 PCLK periods. (See Table 6, page 26.)

Transfer error acknowledge is also asserted if the calculated parity value does not match the parity generated by the external microprocessor on a data transfer. The generation of transfer error acknowledge on parity errors can be disabled by setting the MPMODE bits to 11.

Interrupt Structure

The interrupt structure of the TDCS4810G is designed to minimize the effort for software/firmware to isolate the interrupt source. The interrupt structure is comprised of different registers depending on the consolidation level. At the lowest level (source level), there are two registers. The first is an alarm register (AR). An alarm register is typically of the write 1 clear (W1C) type. The second is an interrupt mask (IM) register of the read/write (RW) type.

An alarm register latches a raw status alarm. This latched alarm may contribute to an interrupt if its corresponding interrupt mask bit is disabled. Individual latched alarms are consolidated into an interrupt status register (ISR). If any of the latched alarms that are consolidated into a bit of an ISR are set and unmasked, the ISR bit is set. The ISR bit may contribute to an interrupt if its corresponding interrupt mask bit is disabled. ISRs may be consolidated into higher-level ISR in a similar fashion until all alarms are consolidated into the chip-level ISR. The alarm register that causes an interrupt can be determined by traversing the tree of ISRs, starting at the chip-level ISR, until the source alarm is found.

Note: Interrupts are masked when the corresponding bit in the mask register is 1. If the mask register bit is 0, then the interrupt is enabled.

Powerdown Mode

In powerdown mode, clocks are stopped from toggling whenever clock gating is possible. When clock gating is not possible, logic is inhibited from toggling by either using clock enable signals on flip-flops, or by forcing data paths to all ones.

The CDR block should also be powered down.

Overview (continued)

Powerdown Mode (continued)

Channels can be independently enabled or disabled under software control using powerdown mode. The default setting after powerup or a device reset is with all 48 channels in powerdown mode (disabled). The desired channels must be enabled via the microprocessor interface before normal operations can commence.

Supervisory Features

Supervisory features built into the TDCS4810G provide diagnostic capabilities and fault coverage.

- Frame Pulse Integrity: The input frame pulse is monitored to ensure that it does not move and that it repeats at least once every 1 ms (8 frames). If the frame pulse moves or does not repeat for more than 1 ms, latched alarm FPERR is raised (see Register Descriptions, page 59).
- LVDS Link Integrity: There is B1 parity generation on each of the 48 LVDS output channels. Performance monitoring on each of the 48 LVDS input channels is implemented as B1 parity error checking. Upon detection of an error, a counter is incremented (one count per errored bit) and a latched alarm is raised. The counter is 8 bits wide and does not roll over after the maximum value is reached. This feature is provisionable on a per-channel basis.
- Framer Monitoring: There is framer performance monitoring in the receive section of the 48 channels. Framer status (LOF) and A1/A2 frame error count are reported. These features are provisionable on a per-channel basis:
  - — Framer status is implemented as a simple LOF latched alarm. While the framer state machine is in the LOF state, this bit is forced active. It is meant to report any LOF occurrence as well as to report the actual state machine status (if the flag is cleared while the state machine is in LOF, the bit will not be cleared).
  - — A1/A2 frame error counter is incremented (one count per errored STS-12 frame) upon detection of a frame error on any of the used A1/A2 bytes (only consider the last A1 byte and the first A2 byte). The counter is 8 bits wide and does not roll over after the maximum value is reached.
- FIFO Aligner Monitoring: There is monitoring of the FIFO aligner operating point. Upon deviating from the nominal operating point of the FIFO by more than user-programmable threshold values (minimum and maximum threshold values), a latched alarm bit will be set. Threshold values are defined per port (16 channels); alarms are defined per channel.
- Frame Offset Monitoring: There is monitoring of the frame offset between all enabled channels; disabled channels are excluded from the monitoring. Monitoring is performed continuously. Upon exceeding the maximum allowed frame offset between all enabled channels, a latched alarm bit will be set.
- Microprocessor Interface Monitoring: There is monitoring of potential write cycles that may occur when operating in write protect mode. Upon detecting a write access to the TDCS4810G when the device is in write protect mode, latched alarm WLOCKALM will be set (see Register Descriptions, page 59).

The B1 error counter and A1/A2 frame error counter are latched into a read-only register and cleared when the CNTFRZ bit is set (see Register Descriptions, page 61).

The B1 error, LOF error, FIFO operating point, and frame offset alarms are latched internally. The latched values are transferred to a freeze register and then cleared when the ALMFRZ bit is set (see Register Descriptions, page 61).

Test Features

Test features built into the TDCS4810G are a key element in providing testing and debugging capabilities for the many aspects of chip-level, board-level, and system-level functionality.

- A1/A2 Error Insert: A frame error inject feature is provided in the transmitter section, allowing the user to replace framing bytes A1/A2 (only the last A1 byte and first A2 byte) with a selectable A1/A2 byte value for a selectable number of consecutive frames. The number of consecutive frames to alter is specified by a 4-bit field, while the A1/A2 value is specified by a 16-bit field. The error insert feature is on a per-channel basis; A1/A2 values and 4-bit frame count value are on a per-device basis.
- B1 Error Insert: A B1 error insert feature is provided in the transmitter section, allowing the user to insert errors on user-selectable bits in the B1 byte. Errors are created by simply inverting bit values. This feature is on a per-bit basis and can insert a single error per bit. Bits to invert are specified through an 8-bit register, where each bit is associated with one of the 8 B1 bits. This feature is provisionable on a per-channel basis.

Overview (continued)

Test Features (continued)

- Scrambler/Descrambler Disable: A scrambler/descrambler disable feature is provided, allowing the user to disable the scrambler of the transmitter and the descrambler of the receiver. Note that B1 should then be calculated (in the transmitter and the receiver) on the nonscrambled data stream. This feature is provisionable for the entire device.

Software Reset

An asynchronous software reset is provided. The software reset is self-clearing, and it resets the whole device.

Interrupts

There is a common interrupt output for the microprocessor interface. Interrupt sources are maskable and are caused by the following (if not masked):

- Write to Locked Registers: An interrupt when the WLOCKALM flag is set (per device). See Register Descriptions, page 59.
- Frame Pulse Error: An interrupt when the input frame pulse moves or is not asserted for more than 1 ms (per device).
- B1 Parity Error: An interrupt when the B1 parity error flag is set (per STS-12).
- LOF: An interrupt when the LOF flag is set (per STS-12).
- FIFO Threshold Error: An interrupt when the FIFO aligner threshold error flag is set (per STS-12).
- Frame Offset Error: An interrupt when the frame offset error flag is set (per STS-12).
- E1/F1 Change: An interrupt when extracted bytes from the current frame differ from those in the previous frame (per STS-1).
- E2 Change: An interrupt when the extracted byte from the current frame differs from that in the previous frame (per STS-12).

Functional Description

Receiver Block

The receiver block converts the incoming LVDS serial stream into an 8-bit parallel bus. The output bus is synchronized to the system clock and the frame is synchronized to the system frame signal. The system frame signal is high to indicate when data on the bus corresponds to the A1 byte of STS-1 #1. SPE bytes are transferred, unaltered, from LVDS input to parallel output. Figure 6 shows a block diagram of the receiver section.

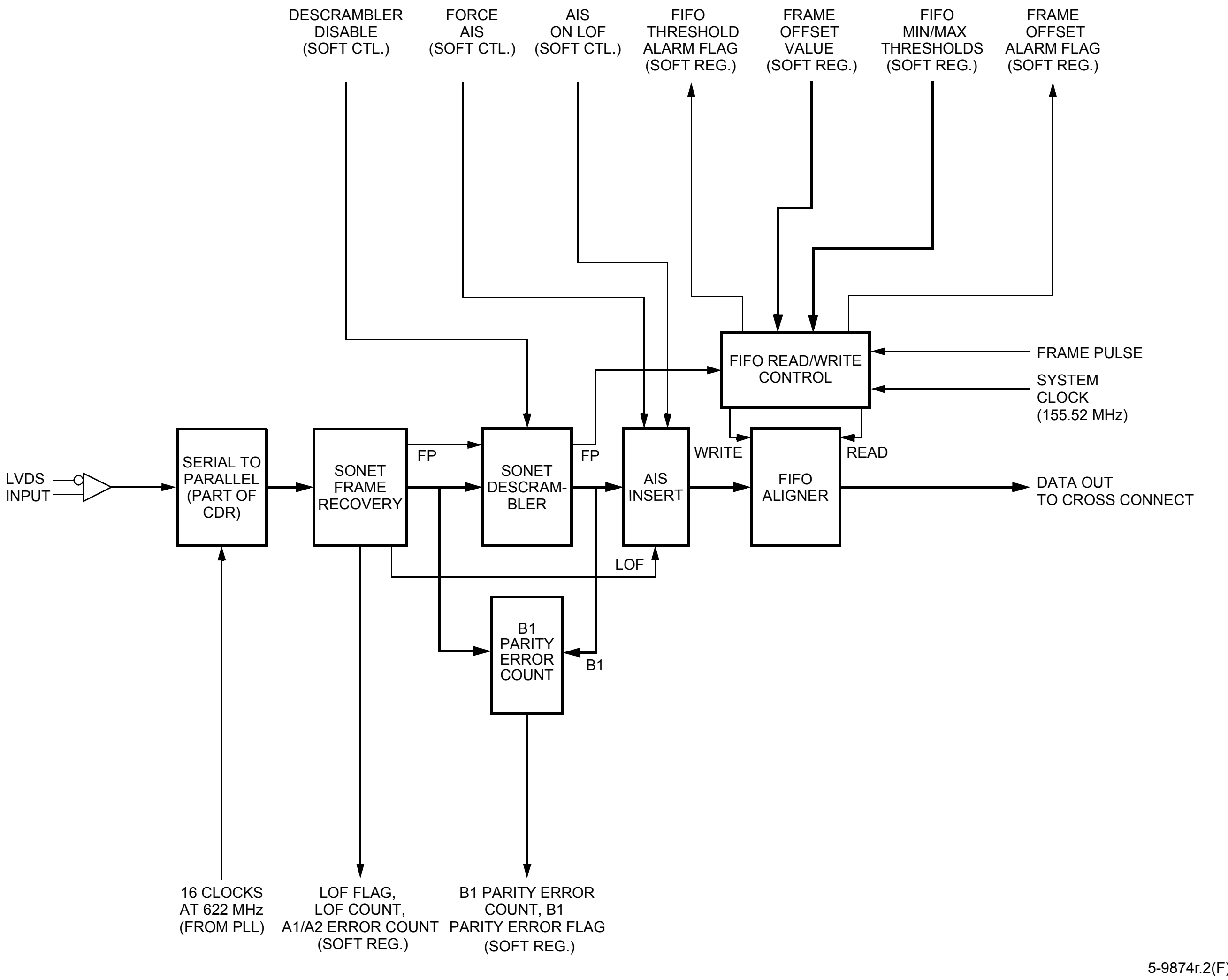


Figure 6. Receiver Block Diagram

Functional Description (continued)

Receiver Block (continued)

LVDS Serial-to-Parallel Converter

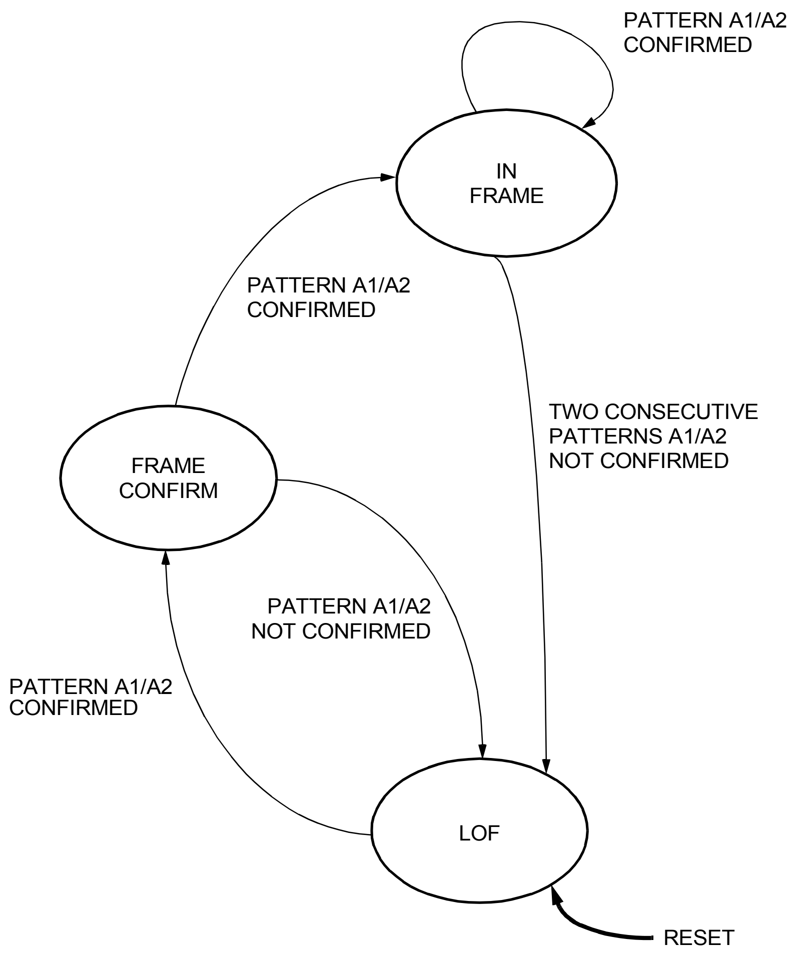
Each CDR incorporates a PLL, which is locked onto the system clock. The PLL multiplies the 77.76 MHz system clock to a 622 MHz clock, which is used to provide LVDS clock recovery modules with 16 phase-shifted clocks (100 ps resolution). Each channel is able to recover the 622 MHz clock associated with its LVDS input and captures the incoming STS-12 data stream.

If an LVDS input is unconnected (floating), the LVDS clock recovery continues to provide a valid clock for downstream logic: internal logic timing is not violated and logic does not lock up. In such a case, loss of framing occurs. The framer also goes back to the in-frame state when LVDS input is back (assuming good data). No reset is needed.

SONET Frame Recovery

The SONET framer detects the position of the SONET frame and generates a frame pulse (FP) signal to mark the position of byte A1 in STS-1 #1.

The framer is not a fully SONET-compliant framer. Instead, it is a simple four-state machine: two consecutive errored frames bring the state machine from in-frame state to LOF (loss of framing) state, while two consecutive frames with aligned A1/A2 transitions bring the state machine from LOF to in-frame state. Figure 7 shows the framer state machine. The framer is completely autonomous.



Notes:
Row, column, and STS counters are only set/reset by state transition from LOF to frame confirm.

The confirmed A1/A2 pattern means that row/col/STS counter values indicate time for the last (12th) A1 byte.

Figure 7. Framer State Machine

Functional Description (continued)

Receiver Block (continued)

This block also incorporates a few monitors: LOF flag, LOF count, and A1/A2 error count. These are cleared by a specific **freeze** command from the CPU interface. The LOF flag is simply a latched alarm bit which indicates that the framer state machine went through LOF state or is in LOF state (the alarm is forced active while in LOF state even if there is a **clear** command from the CPU interface). The LOF counter is incremented each time the framer state machine goes into the LOF state. The A1/A2 error counter is incremented (one count per errored STS12 frame) upon detection of an error on either A1 byte of STS-1#12 or A2 byte of STS-1#1.

The framer propagates an LOF signal to the AIS-L insert block. This is needed in order to support AIS insertion on occurrence of LOF (under software control). Occurrence of LOF on a specific channel does not have any impact on all other in-frame channels.

SONET Descrambler

This block does a framed synchronized descrambling of the framed data using a parallel equivalent of the SONET polynomial of $(1 + x^6 + x^7)$. Note that the framing bytes A1, A2 and the section trace J0/Z0 are not modified by this module.

Furthermore, a debug feature allows disabling the descrambler. Control is common to the scrambler (in transmitter) and descrambler (in receiver) of all 48 channels.

B1 Parity Check

This block calculates parity on the incoming data. The calculated parity is even and calculated for all the bytes in the frame before descrambling. It is compared for errors with the parity byte B1 embedded in the frame after the descrambler block. The B1 byte is defined in the STS-1#1 of the frame. Upon detection of an error, a counter is incremented (one count per errored bit, for a possibility of eight errors per frame) and a latched alarm is raised. The counter is 8 bits wide and does not roll over after the maximum value is reached.

Note that when the scrambler and descrambler are disabled, B1 will be calculated on a nonscrambled data stream.

FIFO Aligner

The FIFO aligner is responsible for aligning each of the 48 STS-12 frames to the system frame pulse for proper cross connect operations. The FIFO aligner is 64-bytes deep and the nominal operating point is determined by the position of the input system frame pulse and the value in a frame offset register. Thus, it provides room for aligning channels having frame offsets of up to 64 bytes (see Figure 8). The FIFO of each channel is filled with the incoming STS-12 stream, using the recovered clock. On the other side, the FIFO is read with the system clock.

The FIFO read/write control block is responsible for managing the FIFO. It handles read and write pointers, and monitors FIFO operating point against software-programmable threshold values. Upon deviating from the nominal operating point of the FIFO by more than the programmed minimum and maximum threshold values, a latched alarm is raised.

An active channel going into LOF does not impact FIFO aligner operations on any of the other channels. A channel being enabled or an active channel coming back from LOF is handled automatically by the FIFO aligner and becomes frame aligned (provided its frame is within the 64-byte window) without causing hits on other active channels.

The FIFO also monitors the frame offset with respect to the 64-byte window. If the frame alignment of the incoming frame is outside the 64-byte window, a latched alarm is raised.

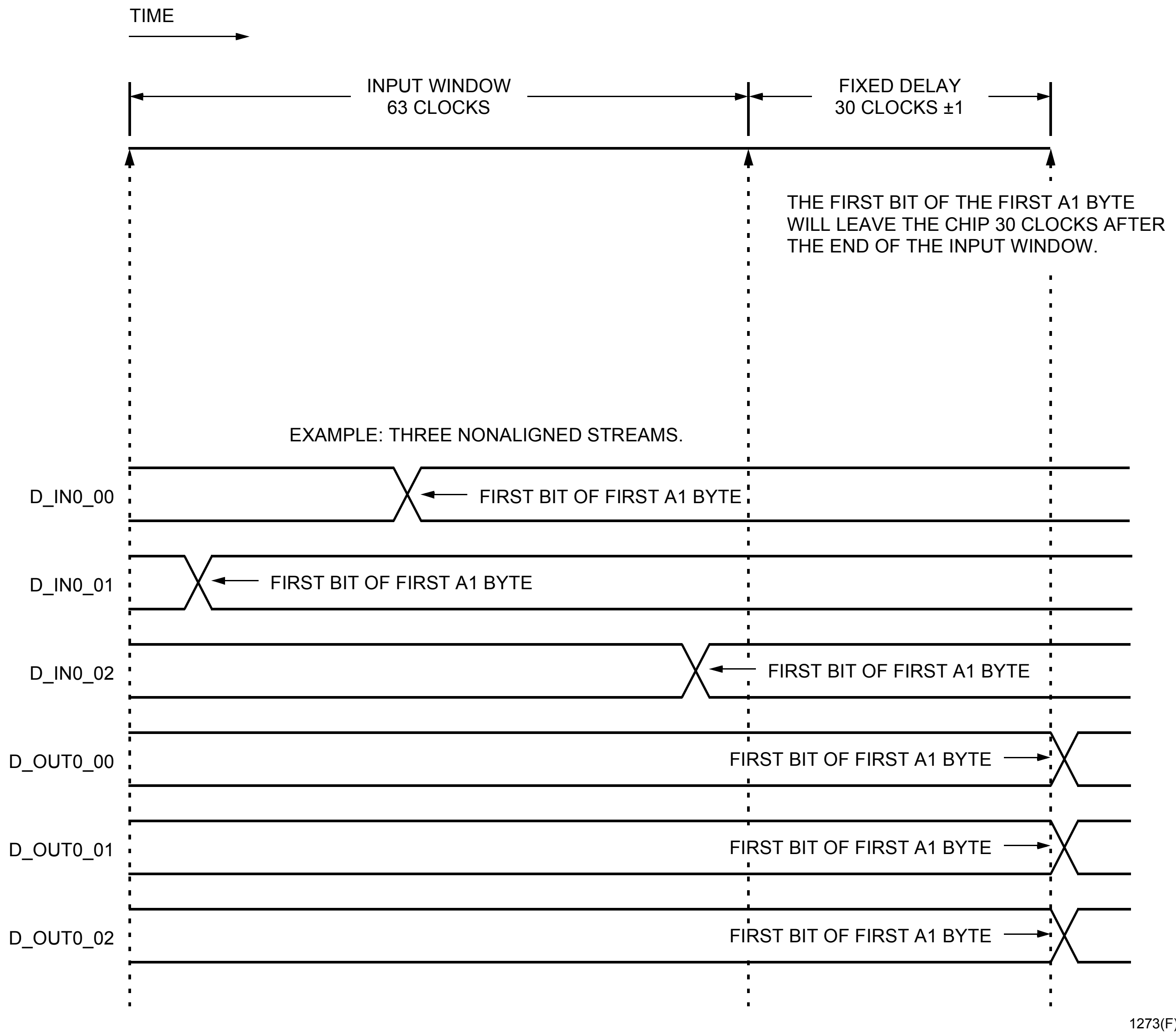
The end of the input window, as shown in Figure 8, is delayed from the incoming SYS_FP by the value of the FRMOFFS register +4. The FRMOFFS register goes from 0 to 9719(dec) (9720 is the number of clock/bytes in an STS-12 frame) (9 rows x 90 columns x 12 time slots). For example, if the user wanted the end of the input window to occur simultaneously with the rising edge of SYS_FP, then the user would need to delay the window by either 0 or 9720 (which is exactly the same thing). So to work out the value to be written into the FRMOFFS register (0X00B), use the following formula:

$$\text{FRMOFFS} = \text{Total\_delay} - 4$$

Once the system in which the TDCS4810G is being used is characterized, the frame offset register should be programmed to position the 64-byte window so that the delay through the chip is minimized (i.e., the FIFO is as close to empty as the system will allow). This will minimize the delay through the cross connect, and thus, a downstream cross connect will be able to absorb the delay through the first cross connect.

Functional Description (continued)

Receiver Block (continued)



Note: A clock is defined as 12.86 ns.

Figure 8. TSHIM Timeline

Functional Description (continued)

Receiver Block (continued)

AIS Insertion

Receiver behavior under the LOF event is under software control; it is possible to select either insert AIS or pass-through when an LOF condition occurs (per-channel control). It is also possible to force AIS (per-channel control). Note that AIS will overwrite all bytes to ones. AIS insertion could be performed at different stages in the receiver. It was placed before the FIFO aligner since the output of the FIFO aligner will be all ones under any circumstances, since the CDR macro will always provide a clock when powered up. When the CDR channel is powered down, the output of the FIFO automatically forces all data to ones.

Cross Connect Block

TSI Memory Organization

The memory is logically organized into two banks. Writes occur to successive locations, rotating through all locations in one bank (having written 12 bytes from each of the 48 write data inputs) before starting on the other bank. Reads from each of the 48 read ports are random access and are always performed on the bank that is not being written to. Since there are 576 STS-1 inputs, each bank contains 576 bytes. The banks are switched at the rate of 6.48 MHz.

Connection Memory

The connection memory is logically organized into four memories: configuration A map C (AC), configuration A map D (AD), configuration B map C (BC), and configuration B map D (BD). Each memory has one entry for each STS-1 output. Functionally, the memory is divided into many small memories. Each STS-12 channel uses two separate memories containing entries for all STS-1s in the channel. One of the memories contains configuration A (both map C and map D), and the other contains configuration B (both map C and map D). Thus, each memory holds 24 entries (12 for map C, 12 for map D). This organization is shown in Figure 9

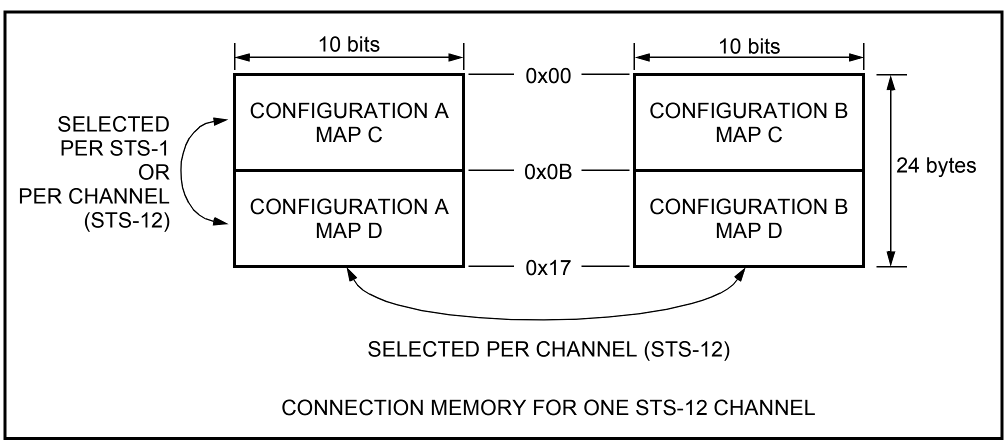


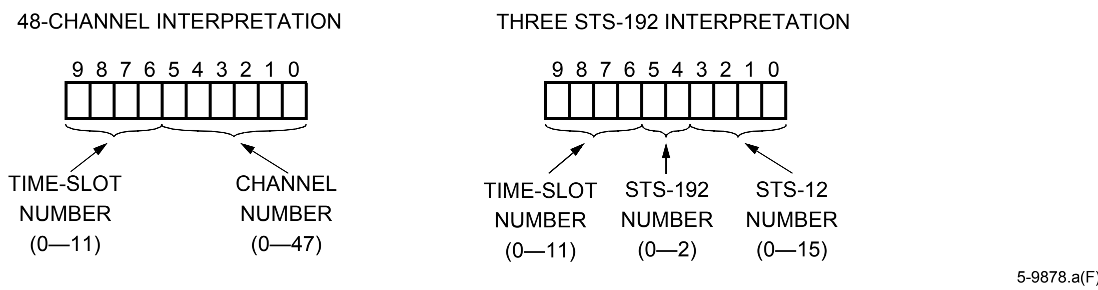
Figure 9. Connection Memory Physical Organization

Functional Description (continued)

Cross Connect Block (continued)

Since only one of the two memories is in use for switching at any time, read operations can be carried out on the other memory. Thus, the preferred method of setting up a configuration is to program the configuration that is not in use, confirm the programming by reading it back, and then switch to that configuration. The configuration that is in use cannot be written to, but a read will return 0x03FF.

Each entry in the connection memory is a 10-bit number that can be broken down into two or three fields, depending on how the channels are interpreted as 48 individual STS-12 channels or as three STS-192 streams. Note that the differences are only in interpretation. There is no actual implementation difference between the two interpretations. The breakdown of the connection memory entry is shown in Figure 10. STS-48 interpretation is similar to the STS-192 interpretation, except there are 4 bits for STS-48 number and 2 bits for STS-12 number.



Note: Time slot and STS-12 number to STS-1 number conversion is shown in Table 14 and Table 15.

Figure 10. Connection Memory Entry

The write address and data to the connection memory are taken from the CPU interface that controls the connection memory. When the memory is being used for switching, the read address is derived from the time-slot count and the working/protect status for each time slot (STS-1). The read data is used to create the address for the TSI macro read port when the memory is being used for switching. Otherwise, the read data is used for microprocessor reads.

Synchronization

Synchronization is divided into two functions: control of the SYNC_N pin and per-channel control of connection memory synchronization. The connection memories will switch to the preprogrammed software configuration during A1A2 when the corresponding SYNC_CM signal is asserted. (The associated register of SYNC_CM is ALM_SW (address 0000, bit 14)). At that point, a latched alarm is raised and the S1 is toggled (to or from 0xF0 and 0x00). This feature can be enabled on a per-channel basis.

The SYNC_N pin can be configured as an open-drain output (master) or input (slave). When configured as an input, individual channels may be programmed to synchronize to the pin. When configured as an output, several options exist to control it:

- A chip-level control bit (the same bit that each channel can synchronize to directly).
- The S1 byte received in a particular channel (the same S1 byte that each channel can synchronize to directly).

The current state of the output S1 (either 0xF0 or 0x00) for each channel is available in a status register. A control register can be used to force a toggle of the S1 byte (regardless of synchronization state) if a particular output state is required.

Functional Description (continued)

Cross Connect Block (continued)

APS Byte Handling

As described in the general description section, incoming K1 and K2 are stored and monitored for a change and the outgoing K1 and K2 can be inserted from a software register with separate control for K1 and K2. These features are per channel.

The K1 and K2 bytes, along with D1 through D12 and E2, can also be switched from any input channel to any output channel separately from the cross connect configuration programmed into the connection memories. There is a single control per output channel to select the input channel to source these bytes from. This feature can be disabled through a software control bit.

Below is a diagram indicating the bytes that can be separately switched and which K bytes are monitored/inserted.

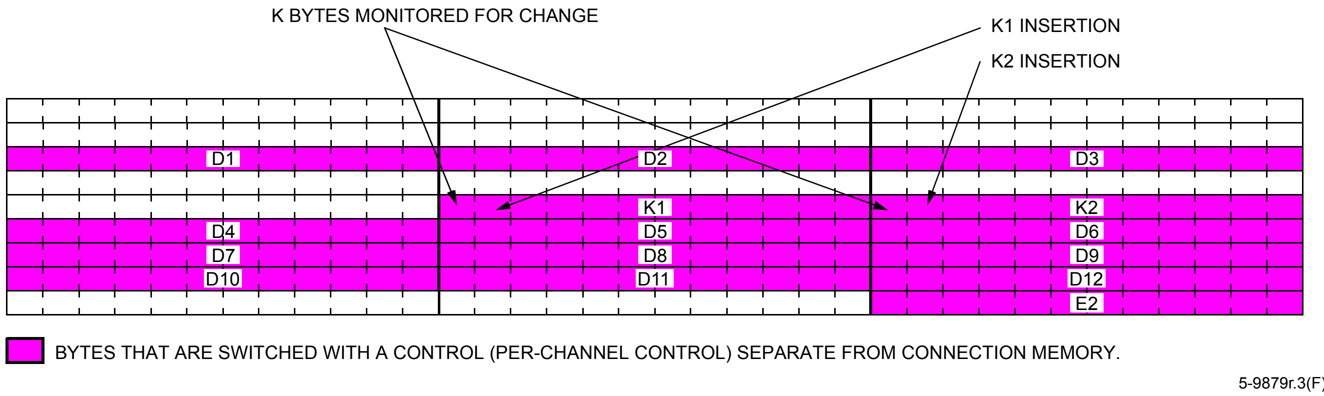


Figure 11. APS Byte Handling

The following diagram illustrates an example of the K-byte switching feature.

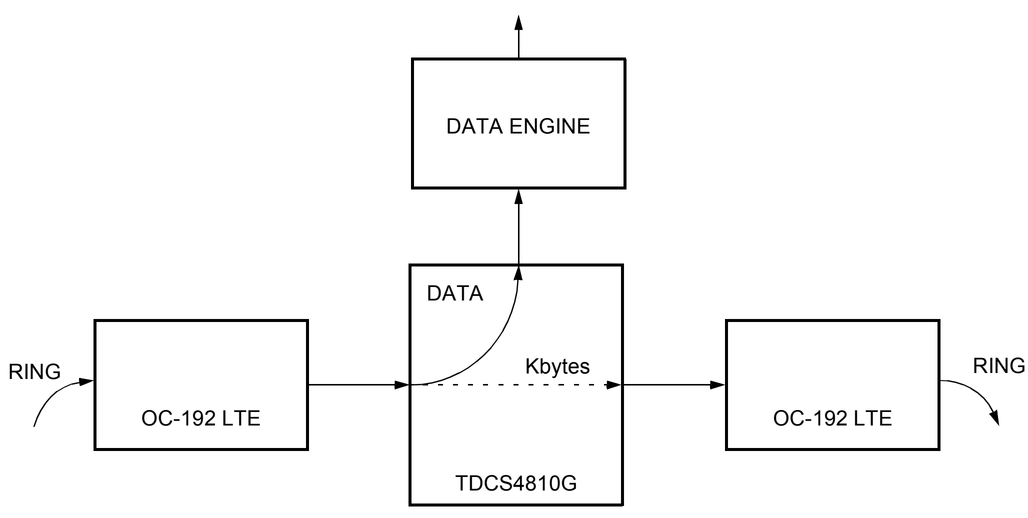


Figure 12. APS Byte Switching Example

Functional Description (continued)

Cross Connect Block (continued)

E1/F1/E2 Extraction

The E1, F1, and E2 bytes carry information that can be used to initiate a switch. The E1 and F1 bytes contain path status information, and the E2 byte contains line status. The E1 and F1 bytes contain identical information. The E1/F1 codes are shown in Table 16. The E2 codes are shown in Table 17. Note that these codes are presented for information purposes only. The circuit will respond to any change in E1 and/or F1, regardless of code.

Table 16. Path Alarm (E1/F1) Information Encoding

E1/F1 Value	Definition
00111111	Loss of Pointer or Path AIS
01111111	Concatenation Mismatch or Software AIS Insertion
00111110	Unequipped Signal Label
TBD	Path Trace Identifier Mismatch
00111101	Signal Fail (SF)
00111100 to 00100001	PDI Code 28 to PDI Code 1
00011111	Signal Degrade (SD)
00011110	Payload Label Mismatch
00000000	No Alarms

Table 17. Line Alarm (E2) Information Encoding

E2 Value	Definition
00000111	Loss of Signal
00000110	Loss of Frame
00000101	Line AIS
TBD	Section Trace Identifier Mismatch
00000100	Signal Fail (SF)
00000011	Signal Degrade (SD)
00000000	No Alarms

Functional Description (continued)

Cross Connect Block (continued)

The E1/F1 bytes for each STS-1 are used, but the E2 byte of only the STS-1 #1 of each channel (STS-12) is used.

The E2 byte for each channel is extracted (EXTRE2) from the input data and is compared to the received value each frame. If a change is detected, a latched alarm is raised (E2ALM). (See Register Descriptions, page 69 and page 62.)

The E1 and F1 bytes are extracted from the output data and stored in memories. The device can be configured under software control so that E1 byte is always taken from working memory and the F1 byte is always taken from protected memory. This is ensured in the connection memory address generator circuit. The E1 and F1 bytes are compared to the previously stored values and if a change is detected, a latched alarm is raised. If this feature is disabled, the E1 and F1 bytes pass through the cross connect normally.

The E1 and F1 bytes are stored in separate memories. The bytes for four channels are stored together in one memory for both E1 and F1. A shadow memory for each channel is used to allow reading of the extracted values. The shadow memory must be set to accumulate data or to read the accumulated data. This is done through a read enable bit in a control register. If a read is made when the memory is accumulating data, the read will return a zero value.

AIS/UNEQ Insertion

Path AIS and UNEQ indications can be inserted on any STS-1 under software control in order to squelch individual STS-1s during and after network topology reconfigurations. Path AIS consists of all ones being inserted into H1, H2, H3, and the entire SPE. UNEQ consists of all zeros in H3 and the entire SPE, with H1/H2 = 0x6000, indicating a normal NDF with an offset of zero. This ensures that downstream path processors will detect a normal pointer and will thus be able to extract the path overhead in order to detect an UNEQ defect. AIS/UNEQ insertion does not affect E1/F1 or E2 values (or any of the TOH).

AIS insertion takes precedence over UNEQ insertion. Changes to the AIS/UNEQ microprocessor registers will not take effect until the next frame boundary.

The registers are arranged such that the AIS controls for an entire channel (12 bits) are in one register and the UNEQ controls (12 bits) are in another register.

Functional Description (continued)

Transmitter Block

The transmitter is composed of 48 STS-12 channels that are treated as independent channels.

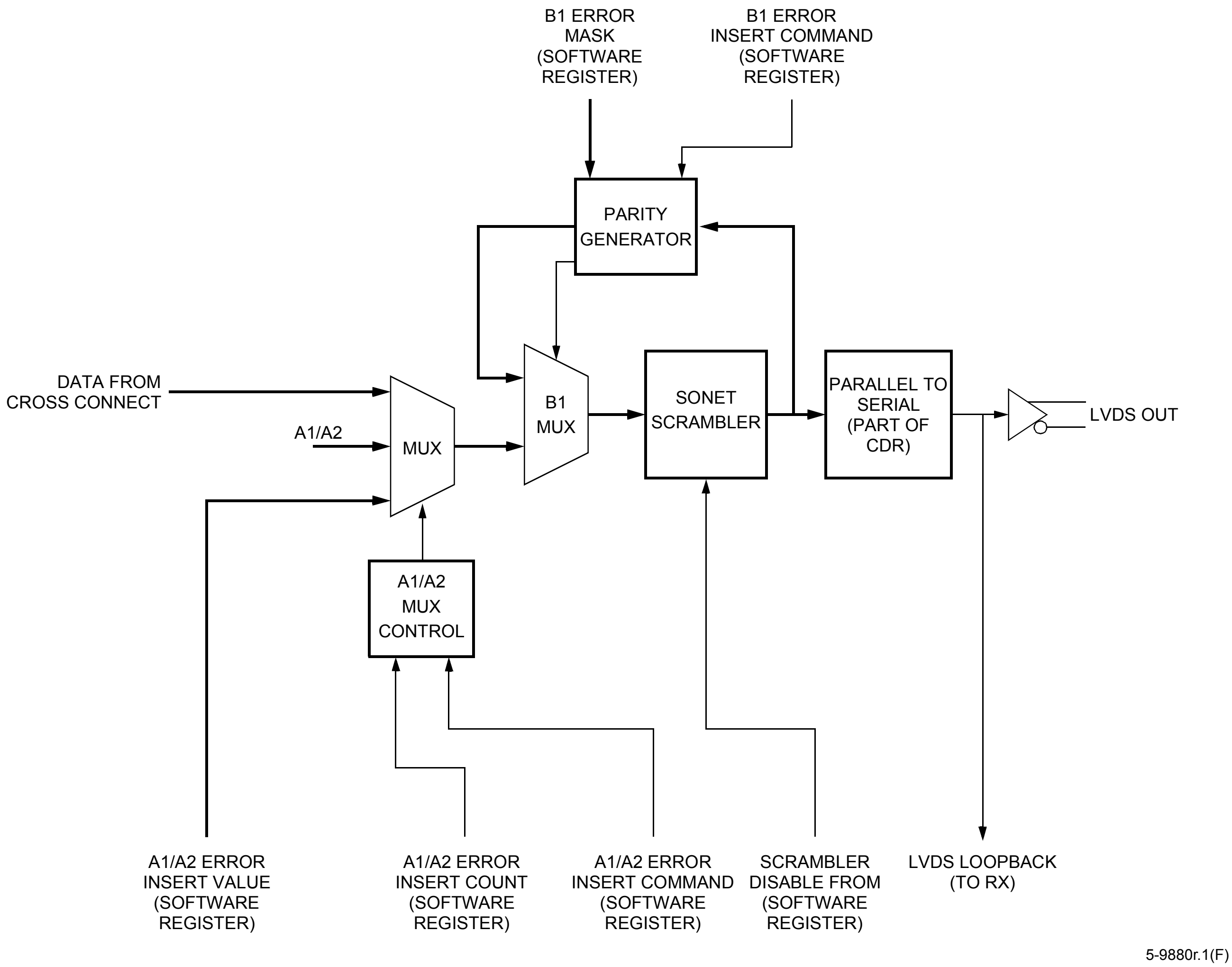


Figure 13. Transmitter Block Diagram

Functional Description (continued)

Transmitter Block (continued)

STS-12 Input Format

Each of the 48 parallel input buses from the cross connect is synchronized to the system clock. The data stream format is a standard SONET STS-12 frame. Framing bytes (A1/A2) of all STS-1s are regenerated. The last A1 and the first A2 can optionally be corrupted via software registers. The B1 parity is always regenerated and the 11 bytes following the B1 are forced to zero.

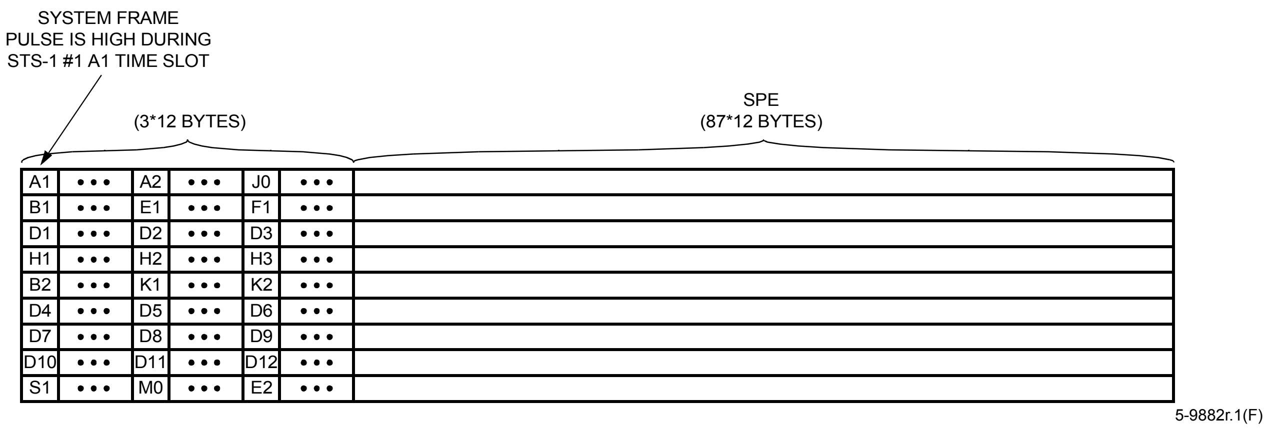


Figure 14. STS-12 Frame Structure

A1/A2 MUX Control

With this block, the A1/A2 bytes are regenerated for all transmitted STS-1s.

A1/A2 errors can be inserted in the frame by the register 000C. A1 of STS-1 #12 and A2 byte of STS-1 #1 are replaced with user-specified byte values (values are shared by the 48 channels) for a user-specified number of consecutive frames (value is shared by the 48 channels).

SONET Scrambler

The SONET scrambler does a framed synchronized scrambling of the input using the SONET polynomial of $(1 + x^6 + x^7)$. Note that the framing bytes A1, A2 and the section trace J0/Z0 are not scrambled.

Furthermore, a debug feature allows disabling the scrambler. Control is common to the scrambler (in transmitter) and descrambler (in receiver) of all 48 channels.

B1 Byte Parity Generator

The B1 byte parity generator generates B1 parity as defined in Bellcore* GR-253 for an OC-12 signal. Parity is even and is calculated over the entire payload after the scrambler. The resulting B1 is inserted in the next frame prior the scrambler block.

The B1 error insert feature allows the user to insert errors on user-selectable bits in the B1 byte. Errors are created by simply inverting bit values. This feature is provisionable on a per-bit basis and will insert a single error (any mix of bits can be inverted). Bits to be inverted are specified through an 8-bit register per channel (each bit is associated with one of the 8 B1 bits). Error insertion is enabled through a single control bit per channel.

When the scrambler is disabled, B1 is calculated on the nonscrambled data stream.

CPU Interface Block

The microprocessor interface is designed to accommodate connection to the *Motorola* MC68360 and MPC860 microprocessors and DSP56309 digital signal processor. Bus transfers using the MC68360 are asynchronous to microprocessor clock, while the MPC860 and DSP56309 transfers are synchronous to the processor clock. The TDCS4810G has a 13-bit wide address and a 16-bit wide data bus.

* Bellcore is now Telcordia Technologies. *Telcordia Technologies* is a trademark of Telcordia Technologies, Inc.

Functional Description (continued)

Back-to-Back Cross Connect

When data is fed into the TDCS4810G, it must not loop back into the TDCS4810G through another TDCS4810G without another device, with pointer mover or pointer processor capability, between them to align the frames. Data streaming out of the TDCS4810G into a series of back-to-back TDCS4810Gs must flow in a straight line. As an illustration of what not to do, see Figure 15.

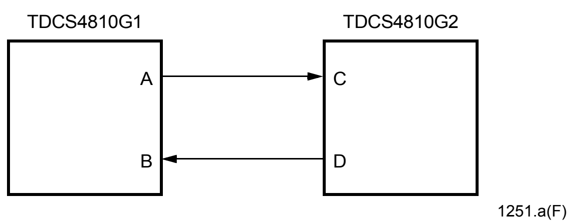


Figure 15. Illegal Back-to-Back Cross Connect Illustration

In Figure 15, there are two data streams, one flowing from A to C, and the other flowing from D to B. Assume that the first bit of the first A1 arrives at C at clock period 0. Because of the nature of the TDCS4810G, the outgoing first bit of the first A1 from D cannot be launched before clock period 0. The reason for this is that the outgoing streams can be made up from any of the incoming streams (i.e., the TSI function), so theoretically, the data on the link from D to B could be the same as on the link from A to C (if TDCS4810G is configured to do that). The consequence is that the first bit of the first A1 leaving on D cannot be launched until after the first bit of the first A1 arrives at C, because they could be the same bit (i.e., all the data from C could be looped back to D inside the TSI). Therefore, the first bit of the first A1 must leave D after the clock period 0. We assume a really low latency through the chip so that the first bit of the first A1 can leave D on clock period 1 (one clock later than it arrived at C). The problem is that the earliest possible time that the first bit of the first A1 from D can arrive at B is clock 1 (assuming zero travel time). So for the same reason that the first bit of the first A1 must leave TDCS4810G on D after it arrives via C, we have the constraint that the first bit of the first A1 must arrive at B before the first bit of the first A1 leaves at A. As in the previous case, this is because the data coming in on B must be able to be sent out on A (if the TSI is so configured). So now the first bit of the first A1 arrives at B at least one clock period before it leaves at A, but it leaves A at clock period 0, so the first bit of the first A1 must arrive at B at clock period –1.

For an alternate way to look at this, see Figure 16.

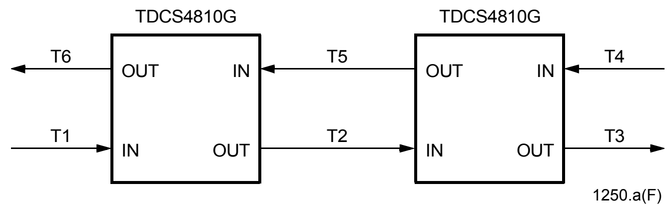


Figure 16. Alternate Illegal Back-to-Back Cross Connect Illustration

From the above figure, the following must be true:

$T1 < T2 < T3$
&
$T4 < T5 < T6.$

Because all data leave a single TDCS4810G at the same time (no delay between them):

$T3 = T5$
&
$T2 = T6.$

Which substituted into the above relationship produces:

$T1 < T2 < T5$
&
$T4 < T5 < T2.$

Note that this equations now state that:

$T2 < T5$
&
$T5 < T2.$

This is mathematically impossible. This is a result of the T5 from Figure 16. Removing T5 would make the entire setup functional. Without the loopback in place, it is possible to have back-to-back TDCS4810G configurations.

Register Descriptions

The address shown for each register is the address of the first occurrence of the register. The number following the T character is the offset to the register for the next time slot in the same channel. The number following the C character is the offset to the first register for the next channel in the port. The number following the P character is the offset to the first register for the next port.

All unused bits read zero and should be written zero with the exception of unused mask bits, which should be written with one to disable (mask out) an alarm.

A summary of the memory map is shown in Table 18, showing the major functional blocks and their associated address range. Areas marked Unused will return a transfer error acknowledge (TEA_N) when accessed. Areas marked Reserved will read 0, and writes will have no effect.

Table 18. Memory Map Summary

Address	Detail
0x0000 0x000D	Device-wide alarms, masks, provisioning, and configuration.
0x000E 0x000F	RESERVED.
0x0010	Write lock register.
0x0011	RESERVED.
0x0012 0x01FF	UNUSED.
0x0200	Port 0.
0x0200 0x0209	Port-wide alarms and masks.
0x020A 0x0229	Channel alarms and masks: channels 0—15.
0x022A 0x0249	Path status alarms and masks: channels 0—15.
0x024A 0x027F	RESERVED.
0x0280 0x0287	Port configuration. FIFOs, AB select, CD selects, etc.
0x0288 0x02FF	RESERVED.
0x0300 0x030C	Provisioning and configuration: channel 0.
0x030D 0x030F	RESERVED.
0x0310— 0x03FF	Provisioning and configuration: channels 1—15 (as for channel 0).

Register Descriptions (continued)

Table 18. Memory Map Summary (continued)

Address	Detail
0x0400— 0x05FF	Port 1: See per-port structure above.
0x0600— 0x07FF	Port 2: See per-port structure above.
0x0800— 0x09FF	RESERVED.
0x0A00— 0x0AFF	RESERVED.
0x0B00 0x0B17	Audit memory port 0.
0x0B18 0x0B1F	RESERVED.
0x0B20 0x0B37	Audit memory port 1.
0x0B38 0x0B3F	RESERVED.
0x0B40 0x0B57	Audit memory port 2.
0x0B58 0x0B5F	RESERVED.
0x0B60 0x0B77	RESERVED.
0x0B78 0x0BFF	RESERVED.

Register Descriptions (continued)

Table 18. Memory Map Summary (continued)

Address	Detail
0x0C00	Extracted path status (E1/F1): channel 0.
0x0C00 0x0C0B	Path status for all paths within channel 0 (12 paths in total).
0x0C0C 0x0C0F	RESERVED.
0x0C10— 0x0EFF	Extracted path status (E1/F1): channels 1 to 47 (See extracted path status for channel 0 above.).
0x0F00 0x0FFF	RESERVED.
0x1000	Connection memory: channel 0.
0x1000 0x100B	AC connection memory (channel 0).
0x100C 0x1017	AD connection memory (channel 0).
0x1018 0x101F	RESERVED.
0x1020 0x102B	BC connection memory (channel 0).
0x102C 0x1037	BD connection memory (channel 0).
0x1038 0x103F	RESERVED.
0x1040— 0xBFFF	Connection memories: channels 1 to 47 (See connection memory for channel 0 above.).

A Note on Alarm Register Reset Defaults

Although all alarms will be cleared on reset, some alarms may be asserted shortly after reset. For example, the LOF alarm is cleared on reset and then immediately asserted by the framer (which resets to the LOF state). Other alarms are also affected, but exactly which alarms are asserted after reset depends on the application.

Register Descriptions (continued)

Device-Level Registers

These registers appear only once in the device.

Table 19. Device Interrupt Status Register (RO)

Address (Hex)	Bit	Name	Description	Reset
0000	14	ALM_SW	Connection memory switch synchronization alarm.	0
	13	ALM_CH	Channel-level alarm.	0
	12	ALM_DEV	Device-level alarm.	0
	11	—	RESERVED.	x
	10	—	RESERVED.	x
	9	—	RESERVED.	x
	8	ALM_LS2	Line status alarm, port 2.	0
	7	ALM_PS2	Path status alarm, port 2.	0
	6	ALM_APS2	APS bytes alarm, port 2.	0
	5	ALM_LS1	Line status alarm, port 1.	0
	4	ALM_PS1	Path status alarm, port 1.	0
	3	ALM_APS1	APS bytes alarm, port 1.	0
	2	ALM_LS0	Line status alarm, port 0.	0
	1	ALM_PS0	Path status alarm, port 0.	0
	0	ALM_APS0	APS bytes alarm, port 0.	0

Register Descriptions (continued)

Device-Level Registers (continued)

Table 20. Device Interrupt Status Mask Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0001	14	ALM_SW_MSK	Connection memory switch synchronization alarm mask.	1
	13	ALM_CH_MSK	Channel-level alarm mask.	1
	12	ALM_DEV_MSK	Device-level alarm mask.	1
	11	—	RESERVED.	x
	10	—	RESERVED.	x
	9	—	RESERVED.	x
	8	ALM_LS2_MSK	Line status alarm mask, port 2.	1
	7	ALM_PS2_MSK	Path status alarm mask, port 2.	1
	6	ALM_APS2_MSK	APS bytes alarm mask, port 2.	1
	5	ALM_LS1_MSK	Line status alarm mask, port 1.	1
	4	ALM_PS1_MSK	Path status alarm mask, port 1.	1
	3	ALM_APS1_MSK	APS bytes alarm mask, port 1.	1
	2	ALM_LS0_MSK	Line status alarm mask, port 0.	1
	1	ALM_PS0_MSK	Path status alarm mask, port 0.	1
	0	ALM_APS0_MSK	APS bytes alarm mask, port 0.	1

Table 21. Channel Alarm Interrupt Status Register (RO)

Address (Hex)	Bit	Name	Description	Reset
0002	6	ALM_CH2	Channel-level alarm, port 2.	0
	5	ALM_CH1	Channel-level alarm, port 1.	0
	4	ALM_CH0	Channel-level alarm, port 0.	0
	3	—	RESERVED.	x
	2	ALM_SW2	Connection memory sync, port 2.	0
	1	ALM_SW1	Connection memory sync, port 1.	0
	0	ALM_SW0	Connection memory sync, port 0.	0

Register Descriptions (continued)

Device-Level Registers (continued)

Table 22. Channel Alarm Interrupt Status Mask Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0003	6	ALM_CH2_MSK	Channel-level alarm mask, port 2.	1
	5	ALM_CH1_MSK	Channel-level alarm, mask port 1.	1
	4	ALM_CH0_MSK	Channel-level alarm mask, port 0.	1
	3	—	RESERVED.	x
	2	ALM_SW2_MSK	Connection memory sync mask, port 2.	1
	1	ALM_SW1_MSK	Connection memory sync mask, port 1.	1
	0	ALM_SW0_MSK	Connection memory sync mask, port 0.	1

Table 23. Device-Level Alarm Register (W1C)

Address (Hex)	Bit	Name	Description	Reset
0004	1	WLOCKALM	Write occurred when registers are locked.	0
	0	FPERR	Frame pulse error (lost or moved).	0

Table 24. Device-Level Alarm Mask Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0005	1	WLOCKALM_MSK	WLOCKALM mask.	1
	0	FPERR_MSK	Frame pulse error mask.	1

Table 25. Device ID Register (RO)

Address (Hex)	Bit	Name	Description	Reset
0006	15—0	CHIP_ID	Chip identification.	0x6440

Register Descriptions (continued)

Device-Level Registers (continued)

Table 26. Device Vintage Register (RO)

Address (Hex)	Bit	Name	Description	Reset
0007	15—0	CHIP_VINTAGE	Chip vintage.	0x0001

Table 27. Scratch Pad Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0008	15—0	SCRATCH_PAD	Scratchpad register. (Does not affect chip operation.)	0x0000

Table 28. Device Provisioning Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0009	12—7	S1SEL	Selects which channel to monitor S1 for chip synchronization.	0
	6	SYNCEN	Enables control of SYNC_N pin (master mode).	0
	5	SW_HW_SYNC	Controls SYNC_N pin from: 0 = SW_SYNC bit. 1 = S1 byte from channel selected by S1SEL bits.	0
	4	FP_MODE	Frame pulse detect mode: 0 = pulse $\geq$ 4 clocks. 1 = pulse $\geq$ 1 clock.	0
	3	SCRDIS	Scrambler/descrambler disable.	0
	2—1	—	RESERVED.	0
	0	SWRST	Software reset.	0

Register Descriptions (continued)

Device-Level Registers (continued)

Table 29. Device Control Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
000A	6	SW_SYNC	Software control of chip synchronization.	0
	5	ALMFRZ	Freeze alarm states.	0
	4	CNTFRZ	Freeze performance counters.	0
	3—0	A1A2INSCNT	A1A2 framing error insert count.	0

Table 30. Frame Offset Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
000B	13—0	FRMOFFS	Frame offset control.	0

Table 31. Framing Error A1A2 Corrupt Value (R/W)

Address (Hex)	Bit	Name	Description	Reset
000C	15—8	A1CRPT	A1 corrupt value.	0
	7—0	A2CRPT	A2 corrupt value.	0

Table 32. Number of Columns (R/W)

Address (Hex)	Bit	Name	Description	Reset
000D	15—7	NUMCOL_LCK	Change value to 9’b1010_0000_1 to change to NUM_COL columns.	0
	6—0	NUM_COL	Number of columns.	0x5A

Table 33. Write Lock Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0010	15—0	LOCKVAL	Lock value. Write 0xA001 to this register to unlock all other registers. Any other value will prevent writes to all other registers and cause an alarm if any register (including this one) is written to.	0

Register Descriptions (continued)

Port (STS-192) Level Registers

These registers appear once for each group of 16 channels. Thus, they are replicated three times in the device.

Table 34. Channel Alarm Interrupt Status (Consolidation) Register

Address (Hex)	Bit	Name	Description	Reset
0200 P+200	15—0	CH_ALM[15—0]	Unmasked channel-level alarm present in channel [15—0].	0

Table 35. Channel Alarm Interrupt Status Mask Register

Address (Hex)	Bit	Name	Description	Reset
0201 P+200	15—0	CH_ALM_MSK[15—0]	Channel alarm consolidation mask.	0xFFFF

Table 36. Path Status Alarm Interrupt Status (Consolidation) Register

Address (Hex)	Bit	Name	Description	Reset
0202 P+200	15—0	PS_ALM[15—0]	Unmasked path status alarm present in channel [15—0].	0

Table 37. Path Status Alarm Interrupt Status Mask Register

Address (Hex)	Bit	Name	Description	Reset
0203 P+200	15—0	PS_ALM_MSK[15—0]	Path status alarm consolidation mask.	0xFFFF

Table 38. Line Status (E2) Change Alarm (W1C)

Address (Hex)	Bit	Name	Description	Reset
0204 P+200	15—0	E2ALM	E2 change alarm for channel [15—0].	0

Register Descriptions (continued)

Port (STS-192) Level Registers (continued)

Table 39. Line Status (E2) Change Mask (R/W)

Address (Hex)	Bit	Name	Description	Reset
0205 P+200	15—0	E2ALM_MSK	E2 change alarm mask for channel [15—0].	0xFFFF

Table 40. APS (K1K2) Change Alarm (W1C)

Address (Hex)	Bit	Name	Description	Reset
0206 P+200	15—0	K1K2ALM	APS (K1K2) change alarm for channel [15—0].	0

Table 41. APS (K1K2) Change Alarm Mask (R/W)

Address (Hex)	Bit	Name	Description	Reset
0207 P+200	15—0	K1K2ALM_MSK	APS (K1K2) change alarm for channel [15—0] mask.	0xFFFF

Table 42. Connection Memory Switch Alarm (W1C)

Address (Hex)	Bit	Name	Description	Reset
0208 P+200	15—0	SW_ALM	Connection memory switch indication for channel [15—0].	0

Table 43. Connection Memory Switch Alarm Mask (R/W)

Address (Hex)	Bit	Name	Description	Reset
0209 P+200	15—0	SW_ALM_MSK	Connection memory switch indication mask for channel [15—0].	0xFFFF

Register Descriptions (continued)

Port (STS-192) Level Registers (continued)

Table 44. FIFO Thresholds (R/W)

Address (Hex)	Bit	Name	Description	Reset
0280 P+200	11—6	FIFOMAX	FIFO maximum depth threshold.	0x003F
	5—0	FIFOMIN	FIFO minimum depth threshold.	0

Note: Thresholds are compared to (N – 1) where N is the number of bytes stored in the FIFO.

Table 45. Configuration A/B Select (R/W)

Address (Hex)	Bit	Name	Description	Reset
0281 P+200	15—0	ABSEL[15—0]	Preselect configuration A or B for channel [15—0]: 0 = A. 1 = B.	0

Table 46. Configuration A/B Readback (RO)

Address (Hex)	Bit	Name	Description	Reset
0282 P+200	15—0	ABRDBK[15—0]	Read back active configuration for channel [15—0]: 0 = A. 1 = B.	0

Table 47. Configuration C/D Line or Path Switching Mode (R/W)

Address (Hex)	Bit	Name	Description	Reset
0283 P+200	15—0	PATHLINE[15—0]	Select path switching (using channel path switch control registers, page 69) or line switching (using configuration C/D select register, Table 48) for channel [15—0]: 0 = path. 1 = line.	0

Table 48. Configuration C/D Select (R/W)

Address (Hex)	Bit	Name	Description	Reset
0284 P+200	15—0	CDSEL[15—0]	Select configuration C or D for channel [15—0]: 0 = C. 1 = D.	0

Table 49. Configuration C/D Readback (RO)

Address (Hex)	Bit	Name	Description	Reset
0285 P+200	15—0	CDRDBK[15—0]	Read back active configuration for channel [15—0]: 0 = C. 1 = D.	0

Register Descriptions (continued)

Port (STS-192) Level Registers (continued)

Table 50. Audit Memory Control (R/W)

Address (Hex)	Bit	Name	Description	Reset
0286 P+200	4	AUDSTART*	Audit control*.	0
	3—0	AUDCH	Channel [15—0] to audit.	0

* When this bit changes from 0 to 1, the active configuration of the channel requested by AUDCH is copied into the audit memory during the next A1/A2 bytes.

Table 51. Audit Memory Status (RO)

Address (Hex)	Bit	Name	Description	Reset
0287 P+200	0	AUDDONE	Audit memory has been filled (cleared when AUDSTART bit is written 0).	0

Table 52. Audit Memory [23:0] (RO)

Address (Hex)	Bit	Name	Description	Reset
0B00 P+20 T+1	9—6	SRCTS	Source time slot [11:0].	x
	5—0	SRCCH	Source channel [47:0].	x

Note: The audit memory stores the full C and D maps (24 entries) of the active configuration (A or B as determined by the appropriate ABSEL bit) of the channel determined by the AUDCH bits.

Table 53. S1 Generation Status (RO)

Address (Hex)	Bit	Name	Description	Reset
0288 P+200	15—0	S1STAT	Current state of S1 generation for channel [15—0]: 0 = 0x00. 1 = 0xF0.	0

Table 54. S1 Generation Force Toggle (R/W)

Address (Hex)	Bit	Name	Description	Reset
0289 P+200	15—0	S1FORCE*	Force toggle of current state of S1 generation (change will be reflected in S1STAT bit) for channel [15—0].	0

* The bit must be changed from a 0 to a 1 to force the change.

Register Descriptions (continued)

Channel-Level Registers

These registers appear once for each channel. Thus, they are replicated 48 times in the device.

Table 55. Channel Alarm Register (W1C)

Address (Hex)	Bit	Name	Description	Reset
020A P+200 C+2	3	FIFOERR	FIFO threshold error.	0
	2	B1ERR	B1 BIP error.	0
	1	LOF	Loss of frame.	0
	0	FRMOFFS	Frame offset error (frame out of range of FIFO).	0

Table 56. Channel Alarm Mask Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
020B P+200 C+2	3	FIFOERR_MSK	FIFO threshold error mask.	1
	2	B1ERR_MSK	B1 BIP error mask.	1
	1	LOF_MSK	Loss of frame mask.	1
	0	FRMOFFS_MSK	Frame offset error mask.	1

Table 57. Path Status (E1/F1) Change Alarm (W1C)

Address (Hex)	Bit	Name	Description	Reset
022A P+200 C+2	11—0	E1F1ALM	Path status (E1, or E1 and F1*) change alarm on time slot [11:0].	0

* Reports both E1 and F1 changes when the E1F1EN bit is set and only E1 changes otherwise.

Register Descriptions (continued)

Channel-Level Registers (continued)

Table 58. Path Status (E1/F1) Change Alarm Mask (R/W)

Address (Hex)	Bit	Name	Description	Reset
022B P+200 C+2	11—0	E1F1ALM_MSK	Path status alarm mask.	0x0FFF

Table 59. Channel Provisioning Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0300 P+200 C+10	9—8	SYNC_SRC	Synchronization source: 00 = sync to local S1 01 = sync to S1 selected by S1SEL bits 10 = sync to SW_SYNC bit 11 = sync to SYNC_N pin	0
	7	SYNC_CTL	Enable synchronization of connection memory switching.	0
	6	INS_S1	Use toggle between 0xF0 and 0x00 on output S1 to indicate when channel is switching.	0
	5	USEKBYTES	APS bytes (K1/K2), D1—D12, and E2 are switched separately using KCH bits.	0
	4	—	RESERVED.	x
	3	—	RESERVED.	x
	2	E1F1EN	Enable monitoring of path status (E1 from working/C and F1 from protect/D).	1
	1	AISONLOF	Insert AIS on LOF condition.	1
	0	PWRDN	Channel powerdown.	1

Register Descriptions (continued)

Channel-Level Registers (continued)

Table 60. Channel Control Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0301 P+200 C+10	12	READE1F1	Enables reading of received E1/F1 values.	0
	11	FAISL	Force AIS-L on input channel.	0
	10	—	RESERVED.	x
	9	FRMERRINS	Insert framing (A1A2) error (based on A1CRPT, A2CRPT, and A1A2INSCNT).	0
	8	B1COREN	Enable corruption of B1 with B1CRTP bits. This is a one shot function—the bit must be reset to 0 and set to 1 again to repeat the B1 error.	0
	7—0	B1CRPT	B1 corrupt value.	0

Table 61. APS Control Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0302 P+200 C+10	7	INSK1	Insert K1 value from register*.	0
	6	INSK2	Insert K2 value from register*.	0
	5—0	KCH	Switch all K1, K2, D1—D12, and E2 bytes from this channel [0:47] instead of passing through TSI (when enabled with USEKBYTES bit in the channel provisioning register).	0

* Values are inserted in the **raw** K-byte location. This is in the second time slot of the channel (STS-1 #4).

Table 62. APS Status Register (RO)

Address (Hex)	Bit	Name	Description	Reset
0303 P+200 C+10	15—8	RCDK1	Received K1 value*.	0
	7—0	RCDK2	Received K2 value*.	0

* Values are those received in the **validated** K-byte location. This is in the first time slot of the channel (STS-1 #1).

Table 63. APS Insert Value Register (R/W)

Address (Hex)	Bit	Name	Description	Reset
0304 P+200 C+10	15—8	K1INSVAL	Value to insert in K1*.	0
	7—0	K2INSVAL	Value to insert in K2*.	0

* Values are inserted in the **raw** K-byte location. This is in the second time slot of the channel (STS-1 #4).

Register Descriptions (continued)

Channel-Level Registers (continued)

Table 64. Channel Path Switch Control (R/W)

Address (Hex)	Bit	Name	Description	Reset
0307 P+200 C+10	11—0	WP[11:0]	Preselect time slot [11:0] to protect configuration: 0 = working/C. 1 = protect/D.	0

Table 65. Channel Path Switch Readback (RO)

Address (Hex)	Bit	Name	Description	Reset
0308 P+200 C+10	11—0	WPRDBK[15:0]	Read back active configuration for time slot [11:0]: 0 = working/C. 1 = protect/D.	0

Table 66. Channel AIS-P Insert (R/W)

Address (Hex)	Bit	Name	Description	Reset
0309 P+200 C+10	11—0	AISINS[11:0]	Insert AIS-P in time slot [11:0].	0

Table 67. Channel UNEQ-P Insert (R/W)

Address (Hex)	Bit	Name	Description	Reset
030A P+200 C+10	11—0	UNEQINS[11:0]	Insert UNEQ-P in time slot [11:0].	0

Table 68. Extracted Line Status (E2) (RO)

Address (Hex)	Bit	Name	Description	Reset
030B P+200 C+10	7—0	EXTRE2	Extracted E2 byte.	0

Table 69. Line Error Counts (RO)

Address (Hex)	Bit	Name	Description	Reset
030C P+200 C+10	15—8	FRMERRCNT	Framing (A1/A2) error count.	0
	7—0	B1ERRCNT	B1 BIP error count.	0

Note:Note that the counts are latched by changing the CNTFRZ bit from 0 to 1. This is like a PM register, but instead of a PM_CLK, the ALMFRZ bit is used.

Register Descriptions (continued)

Channel-Level Registers (continued)

Table 70. Channel Alarm Freeze Register (RO)

Address (Hex)	Bit	Name	Description	Reset
030D P+200 C+10	4	—	RESERVED.	x
	3	FIFOERR_FZ	FIFO threshold error frozen status.	0
	2	B1ERR_FZ	B1 BIP error frozen status.	0
	1	LOF_FZ	Loss of frame frozen status.	0
	0	FRMOFFS_FZ	Frame offset error (frame out of range of FIFO) frozen status.	0

Note:The errors that occur between occurrences of a 0 to 1 change to the ALMFRZ bit are latched when there is a 0 to 1 change to the ALMFRZ bit. This is like a PM register, but instead of a PM_CLK, the ALMFRZ bit is used.

STS-1 Level Registers

These registers appear once for each time slot in each channel. Thus, they are replicated 576 times in the device.

Note that connection memory registers are implemented with internal RAM and the contents are not guaranteed on powerup. Also, the active configuration (A or B) will return 0x3FF if read directly. In order to read the active configuration, the audit memory must be used.

The connection memories are divided into 24 entry blocks. Each channel has two 24 entry blocks of connection memory, named A and B. Each block describes two connection maps for the channel, named C and D (12 entries per map). Thus, there are four maps for each channel, with each map describing the connections for 12 time slots. The four maps are named AC, AD, BC, and BD.

The active configuration is determined by the ABSEL bit for the channel. This selects one of the two blocks (A or B) for the channel. The map that is used within the A or B configuration is determined by either the CDSEL bit for the channel (in which case all 12 time slots use the C or D map) or by the WP bits (in which case each time slot uses the map determined by its corresponding WP bit). The PATHLINE bit for the channel determines whether the CDSEL bit or the WP bits control the map selection for the channel.

When PATHLINE is 0, the WP bits select map C or D on a per-time-slot basis. This can be used for path switching. In this case, map C is referred to as **working** and map D as **protect**.

Table 71. Connection Memory AC (R/W)

Address (Hex)	Bit	Name	Description	Reset
1000 C+40 T+1	9—6	SRCTS	Source time slot [11:0].	x
	5—0	SRCCH	Source channel [47:0].	x

Register Descriptions (continued)

STS-1 Level Registers (continued)

Table 72. Connection Memory AD (R/W)

Address (Hex)	Bit	Name	Description	Reset
100C C+40 T+1	9—6	SRCTS	Source time slot [11:0].	x
	5—0	SRCCH	Source channel [47:0].	x

Table 73. Connection Memory BC (R/W)

Address (Hex)	Bit	Name	Description	Reset
1020 C+40 T+1	9—6	SRCTS	Source time slot [11:0].	x
	5—0	SRCCH	Source channel [47:0].	x

Table 74. Connection Memory BD (R/W)

Address (Hex)	Bit	Name	Description	Reset
102C C+40 T+1	9—6	SRCTS	Source time slot [11:0].	x
	5—0	SRCCH	Source channel [47:0].	x

Table 75. Extracted Path Status (RO)

Address (Hex)	Bit	Name	Description	Reset
0C00 C+10 T+1	15—8	EXTRE1	Extracted E1 byte.	x
	7—0	EXTRF1	Extracted F1 byte.	x

Note: For all the STS-1 level registers above, the hex address is for the output and the value to be programmed is for the input.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 76. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage:				
3.3 V dc Supply	V_{DD}	—	4.2	V
1.5 V dc Supply	V_{DD2}	—	2.0	V
1.5 V Analog Supply	V_{DDA}	—	2.0	V
Storage Temperature	T_{stg}	–65	125	°C
Power Consumption				
3.3 V dc Supply	P_D	—	5.0	W
1.5 V dc Supply	P_{D2}	—	3.22	W
1.5 V Analog Supply	P_{DA}	—	0.28	W

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Agere employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industrywide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

Table 77. ESD Threshold Voltage

Device	Model	Voltage
TDCS4810G	HBM	TBD
	CDM (corner pins)	TBD
	CDM (noncorner pins)	TBD

Operating Conditions

Table 78. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage:					
3.3 V dc Supply	$V_{DDI/O}$	3.135	3.3	3.465	V
1.5 V dc Supply	V_{DDI}	1.425	1.5	1.575	V
1.5 V Analog Supply	V_{DDA}	1.425	1.5	1.575	V
Junction Temperature	T_J	–40	—	125	°C
Ambient Temperature	T_A	–40	—	85	°C

Electrical Characteristics

Power Sequencing

The device power may be applied concurrently to both voltage level inputs. If power sequencing is used for other devices on a board or in a system, it is a preferred that the highest voltage be applied first and removed last.

Low Voltage Differential Signal (LVDS) Buffers

The LVDS buffers are compliant with the *EIA*-644 standard. The only exception to compliance with this standard is associated with the input leakage current. The LVDS input buffers have an input leakage current of 300 µA maximum.

The LVDS buffers are also compliant to the *IEEE** 1596.3 standard. The only exception to compliance with this standard is the input termination resistance. The LVDS input buffers have an input termination resistance of 100 Ω ± 20%.

The LVDS outputs are hot-swap compatible, and can be connected to other vendor's LVDS I/O buffers. The maximum input current for the Agere LVDS input buffers is 9 mA. Prolonged exposure to higher current levels will have an impact on long term reliability.

CML or open collector transmitters cannot be directly connected to the TDCS4810G LVDS inputs. This is not possible, since up to four LVDS inputs share one center tap line with one center tap pin. The 10 µm center tap line is relatively long in the TDCS4810G, therefore resistances and capacitances cannot be ignored.

Unused LVDS inputs may be left unconnected. There are internal pull-up resistors (nominal 14 kΩ) which pull open inputs to greater than 2.75 Vdc (the common mode range is 0 Vdc to 2.4 Vdc). A sense circuit becomes active for input voltages above 2.75 Vdc and clamps the buffer output to a defined state. Open inputs will not oscillate for this reason.

For board layout, LVDS traces should be run on controlled impedance layers, and should be specified as 50 Ω line-to-ground. The LVDS buffers support point-to-point connections. They are not intended for bussed implementations.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Electrical Characteristics (continued)

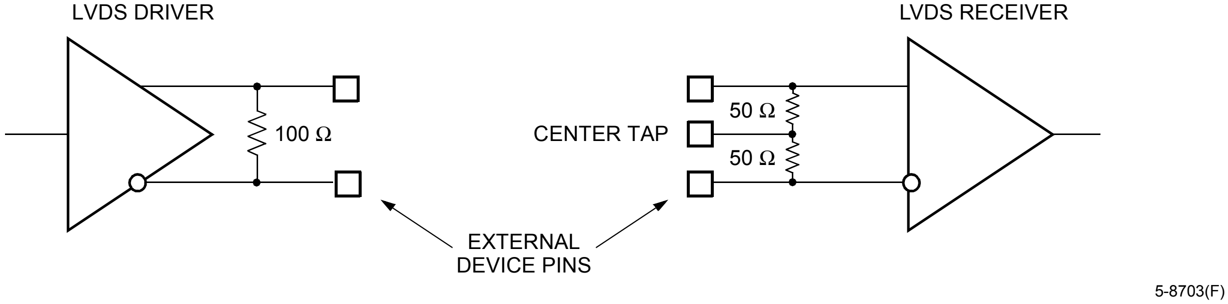


Figure 17. LVDS Driver and Receiver and Associated Internal Components

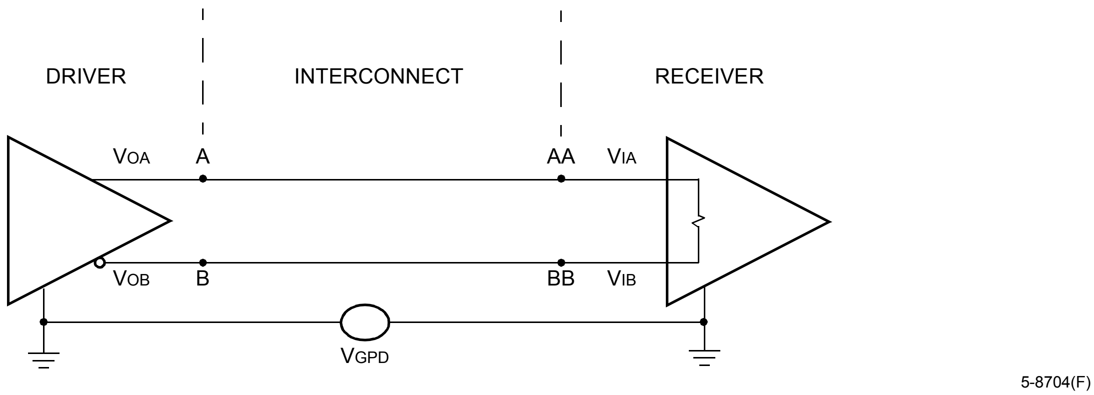


Figure 18. LVDS Driver and Receiver

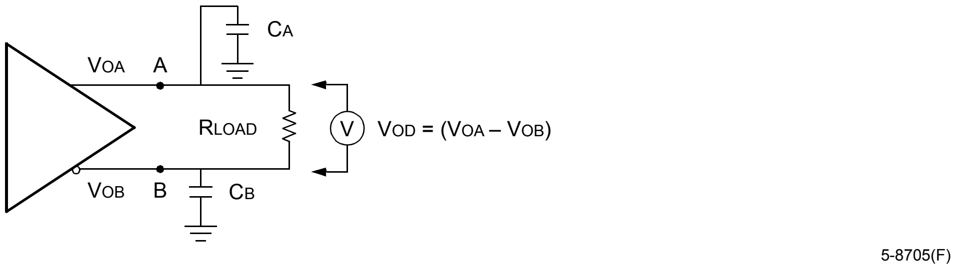


Figure 19. LVDS Driver

Electrical Characteristics (continued)

LVDS Receiver Buffer Capabilities

A disabled or unpowered LVDS receiver can withstand a driving LVDS transmitter over the full range of driver operating range, for an unlimited period of time, without being damaged. Table 79 illustrates LVDS driver dc data, Table 80 the ac data, and Table 82, “LVDS Receiver Data,” on page 76 the LVDS receiver data.

Note: V_{DD} = 3.1 V—3.5 V, 0 °C—125 °C, slow-fast process.

Table 79. LVDS Driver dc Data

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Driver Output Voltage High, V_{OA} or V_{OB}	V_{OH}	R_{LOAD} = 100 Ω ± 1%.	—	—	1.475*	V
Driver Output Voltage Low, V_{OA} or V_{OB}	V_{OL}	R_{LOAD} = 100 Ω ± 1%.	0.925[1]	—	—	V
Driver Output Differential Voltage $V_{OD} = (V_{OA} - V_{OB})$ (with external reference resistor)	$\lvert V_{OD} \rvert$	R_{LOAD} = 100 Ω ± 1%.	0.25	—	0.45[1]	V
Driver Output Offset Voltage $V_{OS} = (V_{OA} + V_{OB})/2$	V_{OS}	R_{LOAD} = 100 Ω ± 1%, refer to Figure 19. on page 74.	1.125[1]	—	1.275[1]	V
Output Impedance, Single-Ended	R_O	V_{CM} = 1.0 V and 1.4 V.	40	50	60	Ω
R_O Mismatch Between A & B	ΔR_O	V_{CM} = 1.0 V and 1.4 V.	—	—	10	%
Change in $\lvert \Delta V_{OD} \rvert$ Between 0 and 1	$\lvert \Delta V_{OD} \rvert$	R_{LOAD} = 100 Ω ± 1%.	—	—	25	mV
Change in $\lvert \Delta V_{OS} \rvert$ Between 0 and 1	$\lvert \Delta V_{OS} \rvert$	R_{LOAD} = 100 Ω ± 1%.	—	—	25	mV
Output Current	I_{SA}, I_{SB}	Driver shorted to ground.	—	—	24	mA
Output Current	I_{SAB}	Driver shorted together.	—	—	12	mA
Power-Off Output Leakage	$\lvert I_{XA} \rvert$, $\lvert I_{XB} \rvert$	V_{DD} = 0 V V_{PAD}, V_{PADN} = 0 V—3 V.	—	—	30	µA

* External reference, REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%.

Table 80. LVDS Driver ac Data

Parameter	Symbol	Conditions	Min	Max	Unit
V_{OD} Fall Time, 80% to 20%	t_{FALL}	Z_{LOAD} = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PADN} = 3.0 pF.	100	200	ps
V_{OD} Rise Time, 20% to 80%	t_{RISE}	Z_{LOAD} = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PADN} = 3.0 pF.	100	200	ps
Differential Skew $\lvert t_{pHLA} - t_{pLHB} \rvert$ or $\lvert t_{pHLB} - t_{pLHA} \rvert$	t_{SKEW1}	Any differential pair on package at 50% point of the transition.	—	50	ps

Electrical Characteristics (continued)

Table 81. LVDS Driver Reference Data

Parameter	Conditions	Min	Typ	Max	Unit
REF10E, REF10L Voltage Range	—	0.95	1.0	1.05	V
REF14E, REF14L Voltage Range	—	1.35	1.4	1.45	V
Nominal Input Current—REF10 and REF14 Reference Inputs	—	—	10	—	µA

Table 82. LVDS Receiver Data

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Receiver input Voltage Range, V_{IA} or V_{IB} (Common Mode Voltage)	V_I	$\lvert V_{GPD} \rvert$ < 925 mV dc—1MHz.	0	1.2	2.4	V
Receiver Input Differential Threshold (Differential Mode Voltage)	$\lvert V_{IDTH} \rvert$	$\lvert V_{GPD} \rvert$ < 925 mV 400 MHz.	–100	—	100	mV
Receiver Input Differential Hysteresis	V_{HYST}	$V_{IDTHH} – V_{IDTHL}$.	—	—	—*	mV
Receiver Differential Input Impedance	R_{IN}	With built-in termination, center tapped.	80	100	120	Ω

* Buffer will not produce transition when input is open-circuited.

Table 83. LVTTL 3.3 V Logic Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage	I_L	—	—	—	1.0	µA
Input Voltage: Low	$V_{ILLVTTL}$	—	GND	—	1.0	V
Input Voltage: High	$V_{IHLVTTL}$	—	V_{DD} – 1.0	—	V_{DD}	V
Output Voltage: Low	$V_{OLLVTTL}$	–5.0 mA	GND	—	0.5	V
Output Voltage: High	$V_{OHLVTTL}$	5.0 mA	V_{DD} – 1.0	—	V_{DD}	V
Input Capacitance	C_I	—	—	2.2	3.0	pF
Load Capacitance	C_L	—	—	0.4	—	pF

Timing Characteristics

Microprocessor Interface Timing

The I/O timing specifications for the microprocessor interface are given in Table 84. The read and write timing diagrams for all three microprocessor interface modes are shown in Figures 20—24.

Table 84. Microprocessor Interface Timing

Symbol	Mode	Parameter	Min	Max	Unit
tc_M860	Synch M860	PCLK Period	15	—	ns
tcycle_M860		Bus Transfer Cycle Time	8 (tc_M860)	12 (tc_M860)	ns
t1		CS_N, TS_N, RW_N Valid to PCLK	4	—	ns
t2		ADDRESS, DATA Valid to PCLK	18	—	ns
t3	(Write)	CS_N, TS_N, RW_N, ADDRESS, DATA Hold	0	—	ns
t4		PCLK to TA_N/TEA_N 3-State to High	—	4	ns
t5		PCLK to TA_N/TEA_N High to Low	—	5	ns
t6		PCLK to TA_N/TEA_N Low to High	2	—	ns
t7		PCLK to TA_N/TEA_N 3-State	—	4	ns
t8	(Read)	DATA Valid to PCLK with TA_N Low	2 (tc_M860)	3 (tc_M860)	ns
t9		PCLK to DATA 3-State	2	—	ns
tc_M360	Asynch M360	PCLK Period	12.76	—	ns
t10		ADDRESS Valid to CS_N, DS_N, TS_N Fall	0	—	ns
t11		TA_N Fall to CS_N, DS_N, TS_N Rise	0	—	ns
t12		TA_N Fall to DATA, ADDRESS Invalid	0	—	ns
t13	(Write)	RW_N Fall to CS_N, DS_N, TS_N Fall	0	—	ns
t14		DS_N Rise to RW_N Rise	0	—	ns
t15		DATA Valid to DS_N Fall	0	—	ns
t16		CS_N, DS_N, TS_N Fall to TA_N/TEA_N High	4 (tc_M360)	—	ns
t17		CS_N, DS_N, TS_N Fall to TA_N/TEA_N Fall	5 (tc_M360)	35 (tc_M360)*	ns
t18		CS_N, DS_N, TS_N Rise to TA_N/TEA_N Rise	2 (tc_M360)	3 (tc_M360)	ns
t19		CS_N, DS_N, TS_N Rise to TA_N/TEA_N 3-State	4 (tc_M360)	5 (tc_M360)	ns
t20	(Read)	TA_N/TEA_N Valid to DATA Valid	tc_M360	2 (tc_M360)	ns
t21		CS_N,TS_N, DS_N Rise to DATA 3-State	2 (tc_M360)	4 (tc_M360)	ns
tc_DSP	DSP Synch	PCLK Period	10	—	ns
tcycle_DSP		Bus Transfer Cycle Time	5 (tc_DSP)	—	ns
t22		CS_N, ADDRESS Valid to PCLK (Setup)	3.5	—	ns
t23		TS_N, RW_N Valid to PCLK (Setup)	3.0	—	ns
t24	(Write)	CS_N to TA_N Active/High Impedance	—	9.5	ns
t25		PCLK to TA_N (Clock to Out)	—	6.0	ns
t26		PCLK to CS_N, ADDRESS Invalid (Hold)	0	—	ns
t27		PCLK to TS_N, RW_N Invalid (Hold)	0	—	ns
t28		PCLK to DATA Input Invalid (Hold)	0	—	ns
t29		DATA Input Valid to PCLK (Setup)	20.0	—	ns
t30		PCLK to DATA Output Active/High Impedance	—	14.0	ns
t31		PCLK to DATA Output Valid	—	26.0	ns

* This value represents the timing for a transfer error (TA_N = 1, TEA_N = 0). The typical value during normal access would be 9(tc_M360) ns.

Timing Characteristics (continued)

Microprocessor Interface Timing (continued)

Synchronous Mode—M860

The synchronous microprocessor interface (like *Motorola* MPC860) mode is selected when MPMODE = 10 or 11. Parity is selected when MPMODE = 10; no parity is selected when MPMODE = 11. Interface timing for the synchronous mode write cycle is given in Figure 20 and for the read cycle in Figure 21.

In synchronous mode, a transfer error (TA_N = 1, TEA_N = 0) will occur if the internal cycle is not terminated in 32 PCLK cycles from the first rising edge of PCLK where CS_N = 0 and TS_N = 0.

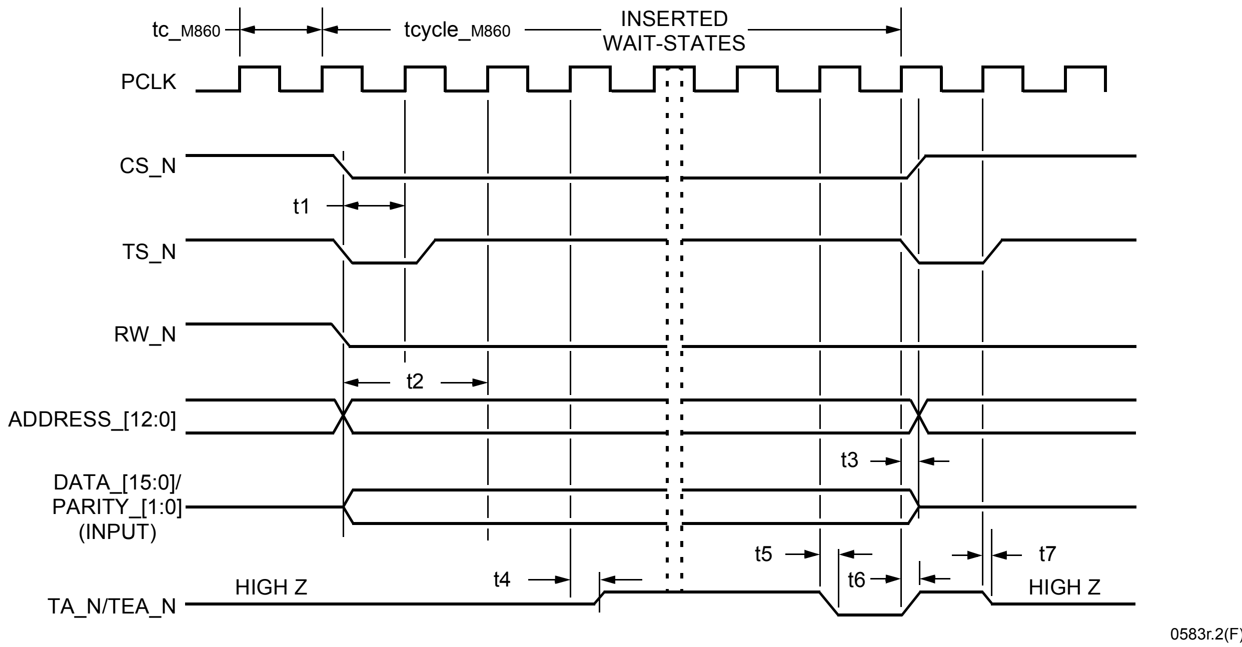


Figure 20. M860 Synchronous Write Cycle (MPMODE = 10 or 11)

Table 85. TA_N/TEA_N Cycle Termination for Synchronous Write Cycle

TA_N	TEA_N	Encoding Description
0	0	Write data parity error.
0	1	Normal cycle termination.
1	0	Access to undefined address region—transfer error.
1	1	No cycle termination—processor-generated time out.

Timing Characteristics (continued)

Microprocessor Interface Timing (continued)

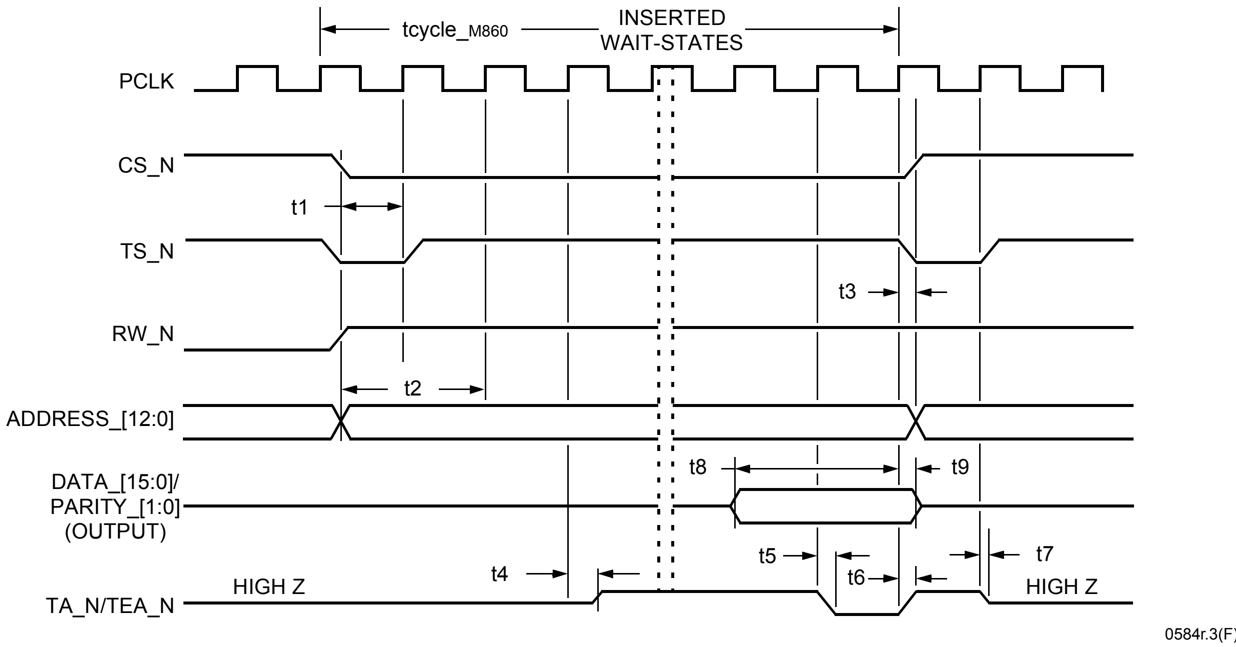


Figure 21. M860 Synchronous Read Cycle (MPMODE = 10 or 11)

Table 86. TA_N/TEA_N Cycle Termination for Synchronous Read Cycle

TA_N	TEA_N	Encoding Description
0	0	Not possible during read cycle.
0	1	Normal cycle termination.
1	0	Access to undefined address region—transfer error.
1	1	No cycle termination—processor-generated time out.

Timing Characteristics (continued)

Microprocessor Interface Timing (continued)

Asynchronous Mode—M360

The asynchronous microprocessor interface (like *Motorola* MC68360) mode is selected when MPMODE = 00. Interface timing for the asynchronous mode write cycle is given in Figure 22 and for the read cycle in Figure 23.

In asynchronous mode, the PCLK can be connected to a 77.76 MHz clock. This can be divided down from the SYS_CLK at 155.52 MHz. The microprocessor should run at no more than half the frequency of PCLK in asynchronous mode. The timing numbers shown assume a PCLK frequency of 77.76 MHz.

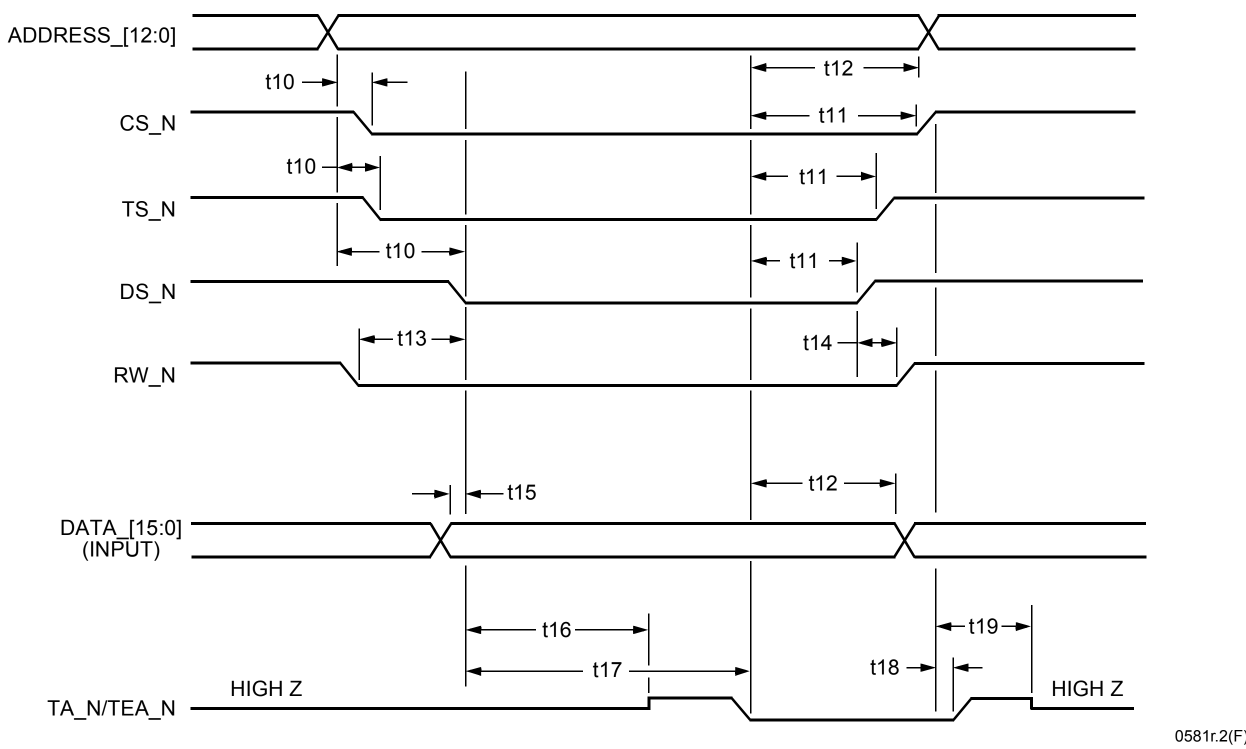


Figure 22. M360 Asynchronous Write Cycle (MPMODE = 00)

Table 87. TA_N/TEA_N Cycle Termination for Asynchronous Write Cycle

TA_N	TEA_N	Encoding Description
0	0	Not possible during asynchronous write cycle.
0	1	Normal cycle termination.
1	0	Access to undefined address region—transfer error.
1	1	No cycle termination—processor-generated time out.

Timing Characteristics (continued)

Microprocessor Interface Timing (continued)

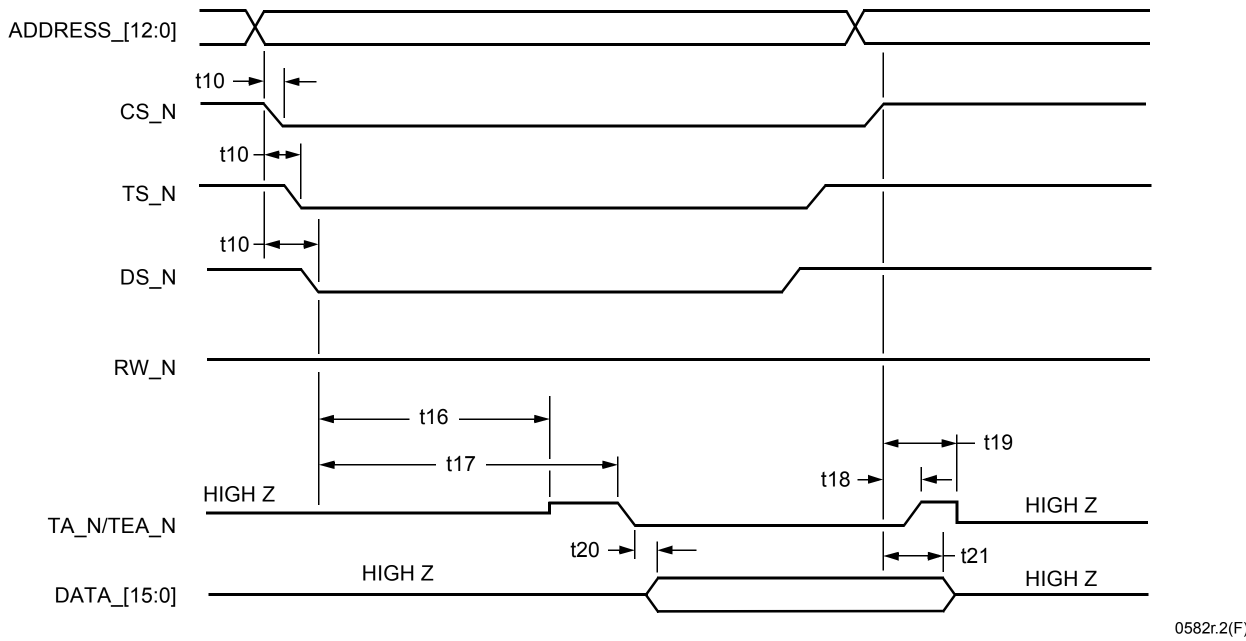


Figure 23. M360 Asynchronous Read Cycle (MPMODE = 00)

Table 88. TA_N/TEA_N Cycle Termination for Asynchronous Read Cycle

TA_N	TEA_N	Encoding Description
0	0	Not possible during read cycle.
0	1	Normal cycle termination.
1	0	Access to undefined address region—transfer error.
1	1	No cycle termination—processor-generated time out.

Timing Characteristics (continued)

Microprocessor Interface Timing (continued)

DSP Synchronous Mode

The synchronous digital signal processor interface (like *Motorola* DSP56309) mode is selected when MPMODE = 01. The DSP mode allows for five-cycle read/write **only** when accessing the connection memory and E1/F1 memory. All other addressing will have a significant number of wait-states depending on what internal block is being accessed.

Note: Although the *Motorola* DSP56309 must be in two or more wait-states mode, there will always be at least four wait-states (i.e., five clock cycles).

$\overline{WR}$ and $\overline{RD}$ in Figure 24 refer to DSP56309 pins which are analogous to pins RW_N and TS_N, respectively, in the TDCS4810G device.

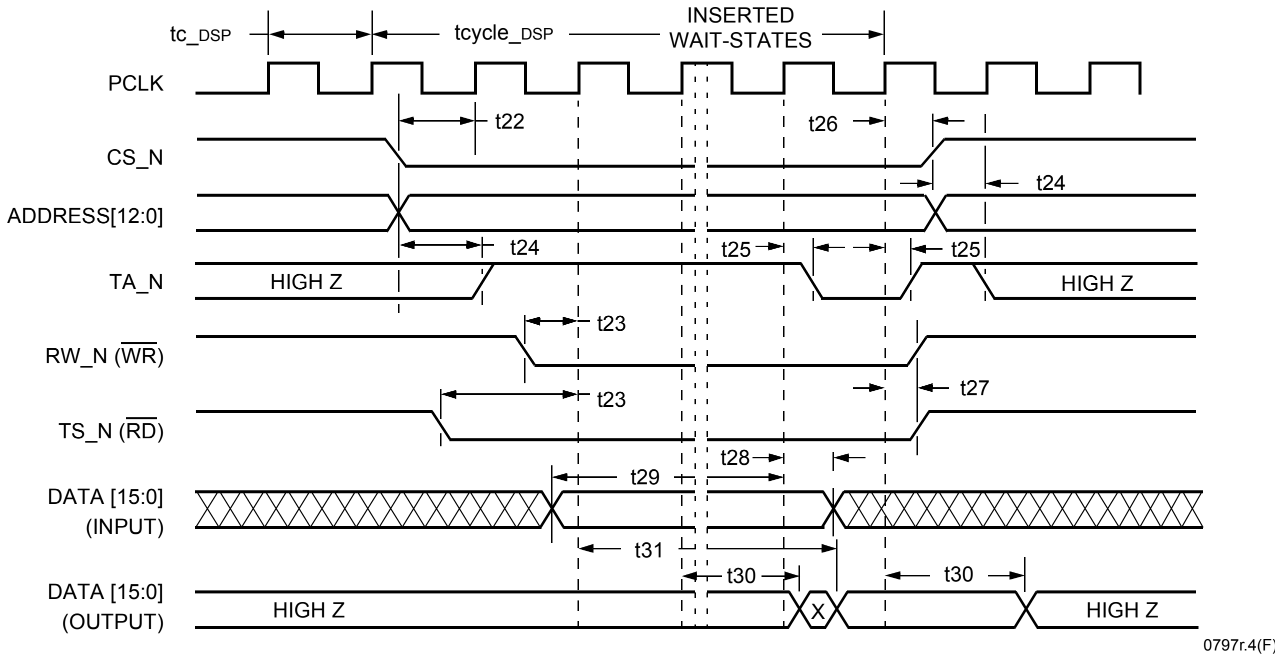


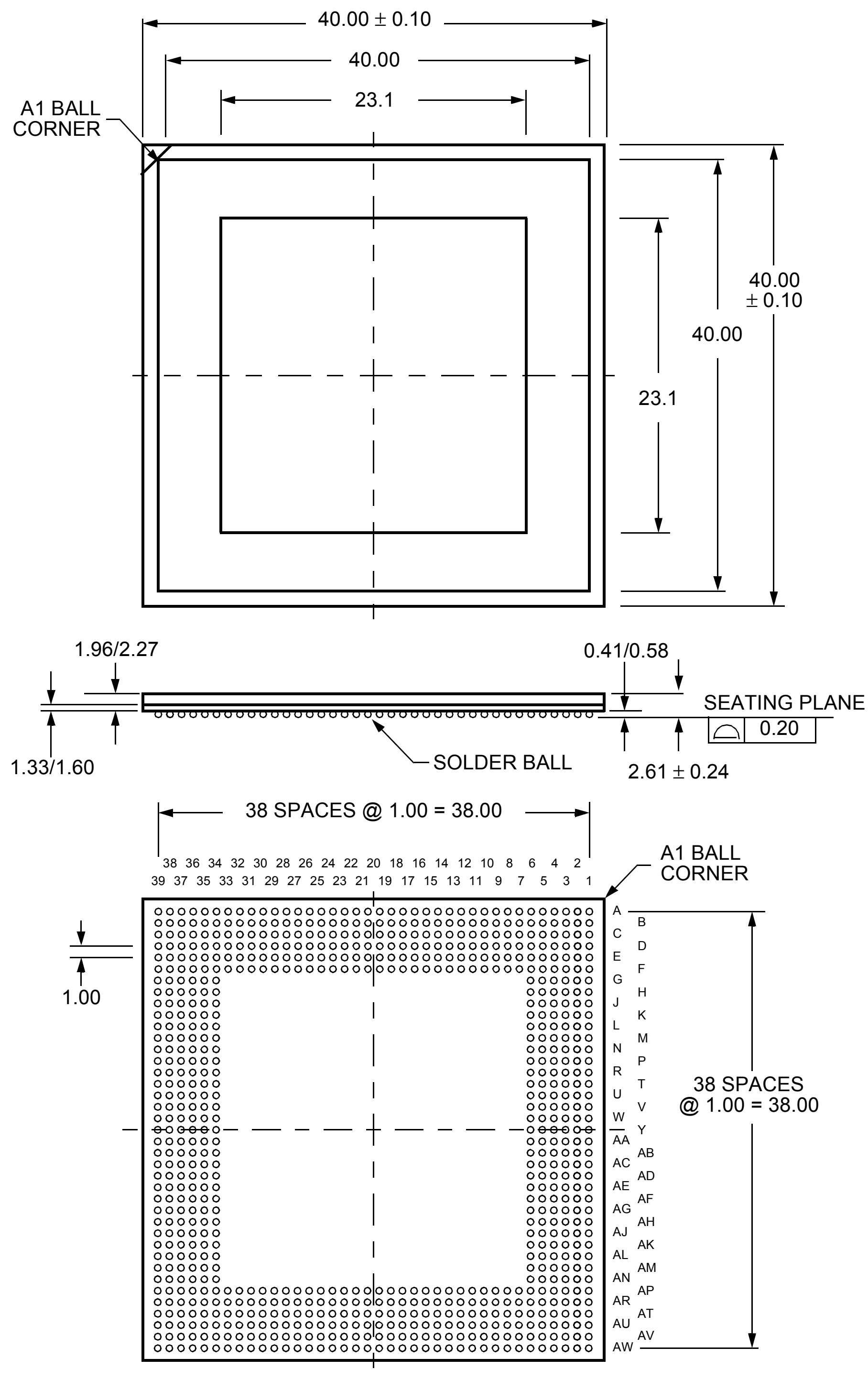
Figure 24. DSP R/W Synchronous Write Cycle (MPMODE = 01)—Two or More Wait-States Mode

Outline Diagram

792-Pin LBGA

Dimensions are in millimeters.

.



Note: A dimension x/y refers to the minimum and maximum values for the given parameter.

Outline Diagram (continued)

792-Pin LBGA (continued)

Table 89. Basic 792-Pin LBGA

Act. Balls	Ball Pitch mm (mils)	Width/Length mm (mils)	Thickness mm (mils) (nom.)	Max Height* mm (mils)	PWR/GND
792	1.00 (39.4)	40.00 (1575)	2.11 (83)	2.85 (112)	192

* Maximum height from the board to the top surface of the package before solder ball collapse.

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
TDCS4810G	792-pin LBGA	–40 °C to +85 °C	109057265

Revision History

May 2001—Rev 2

Pin Information

- Page 25, Table 5, added second footnote (†) and reworked name/description for rows F9—AR31.
- Page 25, Figure 3, added to document.

Register Descriptions

- Page 66, Table 55 and Table 56, removed row for bit 4.

Absolute Maximum Ratings

- Page 72, Table 76, replaced TBD with corresponding values.

Operating Conditions

- Page 72, Table 78, replaced TBD with corresponding values.

Electrical Characteristics

- Page 73 to 76, added section to document.

Outline Diagram

- Page 84, Table 89, removed the following colums: descriptor, layers, array-size, max signals, and number of pads.

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Agere Systems Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Agere Systems (Shanghai) Co., Ltd., 33/F Jin Mao Tower, 88 Century Boulevard Pudong, Shanghai 200121 PRC
Tel. (86) 21 50471212, FAX (86) 21 50472266
JAPAN: Agere Systems Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries:GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 3507670** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

May 2001
DS01-150SONT