M13E Device
DS3/DS1 MUX/DEMUX, Extended Features
TXC-03303

DATA SHEET

FEATURES

- Multiplexes/demultiplexes 28 DS1 signals to/from a DS3 signal.
- M13 or C-bit parity mode operation
- FEBE, C, or P-bit parity error insertion capability
- DS3 idle signal generators
- DS1 idle signal (QRS, AIS or ESF) generators
- DS3 LOS, LOF, P-bit parity, C-bit parity, AIS and idle detectors
- Receive or transmit DS1 LOS detectors
- DS2 LOF detectors
- External interface for receiving 14 C-bits and transmitting either 13 or 14 C-bits based on a control bit setting
- DS3 and DS2 X-bit access
- DS3 transmit and receive selectable AIS generation and detection
- Supports Intel, Motorola, or multiplexed microprocessor interfaces.
- DS2 Tx/Rx X-bit control/status
- Test Access Port for boundary scan
- Single +5V, ±5% power supply
- 208-pin plastic quad flat package

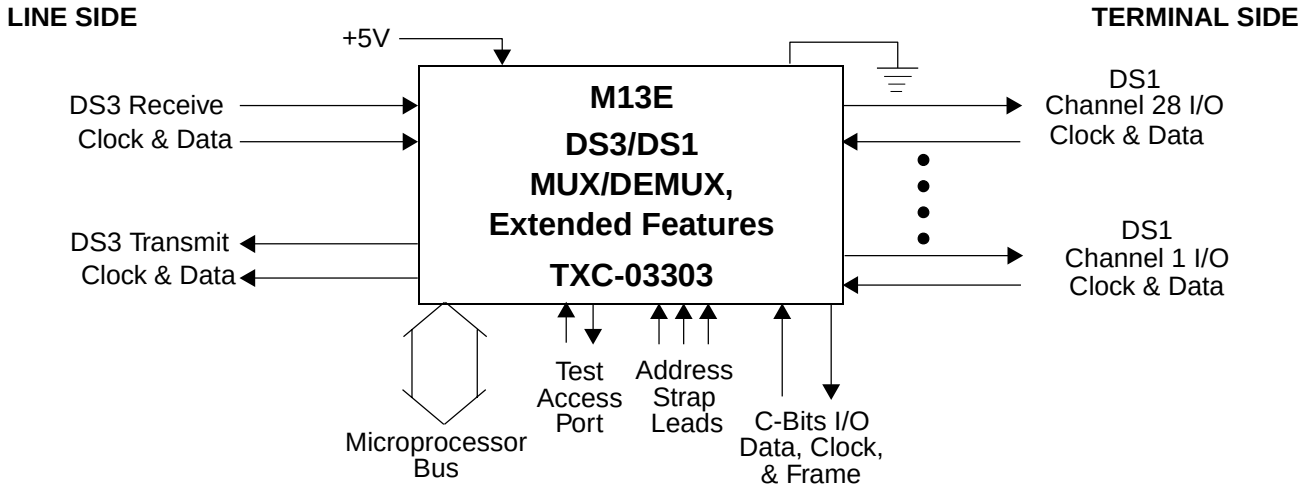
DESCRIPTION

The M13E CMOS VLSI device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some extended features relative to the M13 device. The M13E line side signals typically interface with a TranSwitch ART or ARTE device, DS3LIM-SN Module or other line circuitry; terminal side signals interface with commercially available DS1 line interface devices. A DS1 line interface device containing an internal dejitter buffer is recommended.

The M13E provides an external transmit (13 or 14 bits) and receive (14 bits) interface for the 21 C-bits while operating in the C-bit parity mode. The FEAC channel (C3) can be accessed via the external interface or the M13E memory. The M13E memory map contains 35, 8-bit register locations for software control, performance counters, and alarm reporting. The microprocessor interface provides for connection to an Intel or Motorola-compatible microprocessor, or for use of a multiplexed address/data bus.

APPLICATIONS

- Single-board M13 multiplexer
- Compact add/drop mux
- Fractional T3
- DCS and EDSX
- CSU/DSU



Document Number:
TXC-03303-MB
Ed. 4, August 1998

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* Please note that TranSwitch provides documentation for all of its products. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

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BLOCK DIAGRAM

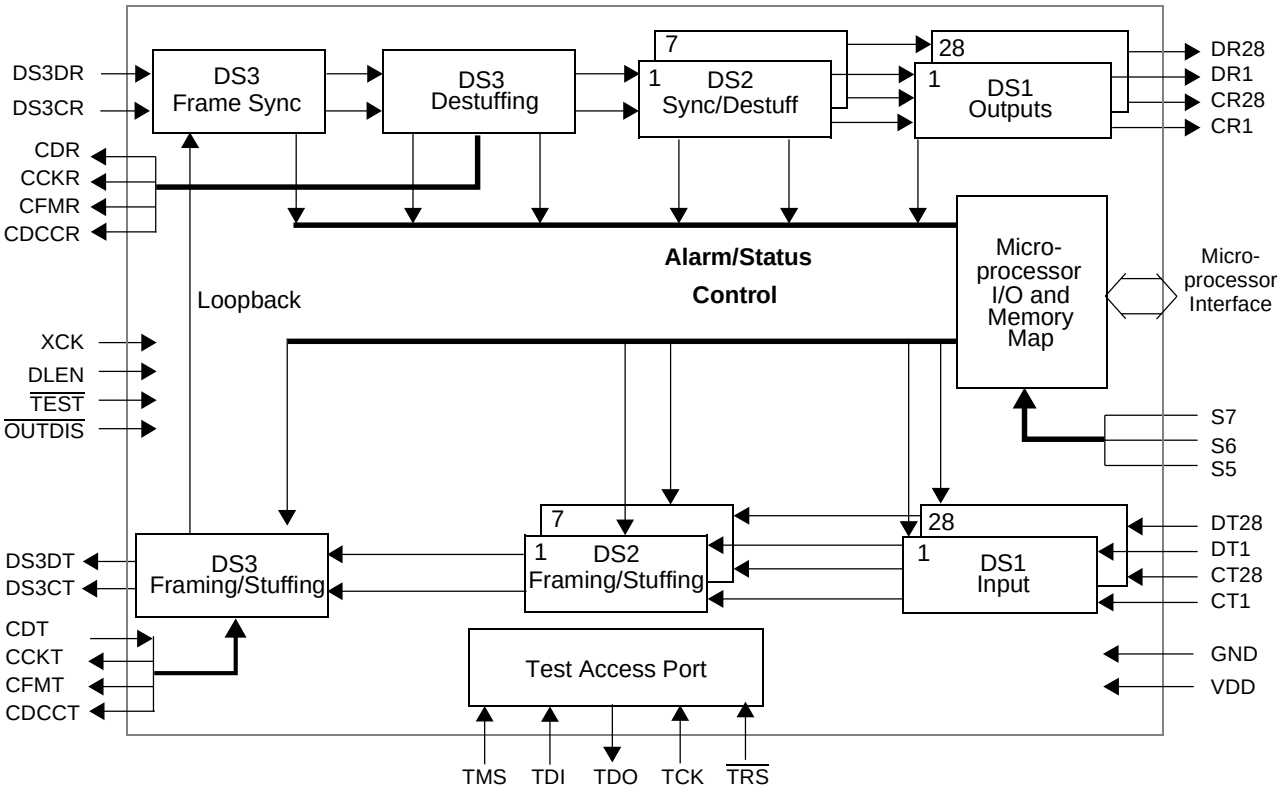


Figure 1. M13E TXC-03303 Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 shows a simplified block diagram of the M13E and its signal leads. In the receive direction, DS3 data (DS3DR) is clocked into the M13E on positive transitions of the DS3 input clock (DS3CR). The data and clock signals may be derived from any line interface device such as TranSwitch's ART, ARTE or DS3LIM-SN, or from other line circuitry.

The DS3 Frame Sync Block searches for and locks to the DS3 frame, as specified in Bellcore's TR-TSY-000499, "Transport System Generic Requirements," and in ANSI's T1.107-1988 and supplement T1.107a-1990. The M13E receiver monitors the DS3 signal for out of frame, loss of signal, a DS3 AIS, DS3 idle signal, P-bit parity, the state of the X-bits, and loss of clock. The DS3 AIS detection mechanism is software selectable, with a choice of six detectors. These range from full compliance to T1.107/107a to unframed all ones AIS detection. Control bits are also provided in memory which allows all, some of, or none of the DS3 alarms to cause the insertion of AIS into the receive DS1 channels.

In the M13 mode, destuffing from DS3 to DS2 is performed based on the states of the C-bits in the DS3 subframes. If two or three of the C-bits in a subframe are ones, the associated stuff bit is interpreted as being a stuff bit and is removed from the data stream and discarded.

In the C-bit parity mode, the C-bits are allocated for network performance. The M13E performs Far End Alarm and Control (FEAC) detection, C-bit parity error detection, and Far End Block Error (FEBE) detection. FEAC loopback requests and alarm/status information is provided in the memory map. In addition, the states of 14 C-bits (C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21) are provided at a serial interface (CDR), along with an output clock signal (CCKR), framing pulse (CFMR), and data link indicator pulse (CDCCR). The data link indicator pulse identifies the location of the data link bits, C13, C14, and C15.

The M13E synchronizes and extracts the 28 DS1 channels from the seven DS2 channels. Each of the DS2 channels is monitored for out of frame. The M13E may generate AIS in each of the DS1 signal tributaries corresponding to the DS2 channel(s) that lost frame, depending on the DS1 AIS alarm insertion control bits. DS2 to DS1 destuffing is based on the states of the three C-bits in each DS2 subframe. If two or three of the C-bits in one of the DS2 subframes are ones, the stuff bit for that subframe is discarded. In the M13 mode, the DS2 C-bits or stuffing bits are used for DS1 remote loopback requests. The M13E provides control bits in the memory map for selecting the remote loopback detection mechanism. The destuffing operation is still active during loopback request and operation. In addition to DS2 synchronization, destuffing, and remote loopback detection, the M13E also extracts the seven DS2 X-bits.

An option is provided that allows the received or transmitted DS1 channels to be monitored for loss of signal. Receive data for each of the DS1 channels (DRn) is clocked out of the M13E on positive transitions of the associated clock signal (CRn). In addition, the M13E provides a stable DS1 clock signal for the data signals received during AIS periods.

In the transmit direction, DS1 transmit data (DTn) is clocked into the M13E on positive transitions of the clock input (CTn) for each of the 28 DS1 channels. A DS1 Input Block, which consists of a FIFO and supporting logic, is provided for each DS1 channel. Under software control, the M13E can invert the transmit data signals, or the clock signals, for all 28 DS1 channels. The data inversion feature provides compatibility with certain T1 line interface devices, while the clock inversion feature allows back-to-back M13 operation.

The DS1 Input Block is also used to insert one of three idle patterns from a common generator into a DS1 bit stream, under software control. The selection of the idle pattern is common to all 28 DS1 channels. The idle patterns are: a QRS, an Extended Super Frame DS1 (ESF) format with all ones in channels 1 through 28, and an AIS format (all ones).

Each DS1 signal is multiplexed into the respective DS2 frame, with the stuff bits inserted based on the fill level of an internal FIFO. When the fill of the FIFO drops below half full, a stuff bit is inserted into the DS1 bit stream in the DS2 signal. The DS2 signal is formed by combining four DS1 signals. In each frame there are 287 data bit positions and one stuff bit per DS1 channel (for a DS1 total of 1152 bits) and 24 overhead bits, for a frame total of 1176 bits. The overhead bits are used for framing, X-bit channel and stuff control.

The DS3 signal is partitioned into M-frames of 4760 bits each. The M-frames are divided into seven M-subframes having 680 bits each. Each M-subframe is further divided into eight blocks of 85 bits each. Each block uses 84 bits for payload and one bit for frame overhead. There are 56 overhead bits in each M-frame: the M-frame alignment uses three bits, the M-subframe alignment (F-bits) uses 28 bits, 21 bits are defined as C-bits, two bits are assigned for parity, and two bits are assigned for the X-bit channel.

The DS3 frame is constructed and timed according to the operating mode, i.e., C-bit parity mode or M13 mode. In the C-bit parity mode, all seven of the DS2 stuff bits are fixed as stuff, resulting in 7 pseudo DS2 frames of 671 bits per DS2 frame in each DS3 frame, for a DS2 rate of 6.3062723 Mbit/s. Since stuffing always occurs, the 21 C-bits are assigned for other functions, as shown in Figure 2. A C-bit interface is provided for transmitting 13 or 14 C-bits (C2, C3-depending on the state of bit 7 of register 19H (C3CLKI), C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, C21). The external transmit C-bit interface consists of a serial data input (CDT), an output clock (CCKT), a data link indicator pulse (CDCCT), and an output framing pulse (CFMT). The data link indicator pulse identifies the location of the three data link bits, C13, C14, and C15. In addition, a control bit is provided in the memory map which enables the M13E to generate an extra clock cycle during the C3 bit time. A receive C-bit interface is provided for extraction of 14 C-bits (C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, C21). The receive C-bit interface consists of a serial data output (CDR), an output clock (CCKR), a data link indicator pulse (CDCCR), and an output framing pulse (CFMR). The data link indicator pulse identifies the location of the three data link C-bits, C13, C14, and C15.

C1	C2*	C3**	C1 = C-bit parity mode C2 = Reserved C3 = Far End Alarm & Control (FEAC)
C4*	C5*	C6*	Not defined, set to one
C7	C8	C9	C-Parity bits
C10	C11	C12	Far End Block Error (FEBE)
C13*	C14*	C15*	Maintenance data link (28 kbit/s)
C16*	C17*	C18*	Not defined, set to one
C19*	C20*	C21*	Not defined, set to one

*These bits are provided at the C-bit interface in the C-bit mode
** Always provided at the receive C-bit interface in the C-bit mode

Figure 2. C-Bit Assignments

Of the eight remaining C-bits, C1 is used as an identification channel; C3 is defined as a Far End Alarm and Control (FEAC) bit and is controlled via the memory map; C7, C8, and C9 are used for C-bit parity; and the remaining three bits, C10, C11, and C12, are used to transmit a FEBE indication. A FEBE is automatically transmitted if a C-bit parity error or framing error is received.

Fixed DS2 to DS3 stuffing is used for M23 multiplexing at a rate of seven stuffs for every 18 DS3 stuff opportunities. This yields a DS2 frequency of +2.6 ppm above the desired frequency of 6.312 Mbit/s. After adding this to the tolerance of the DS3 clock signal, ±20 ppm, the frequency is still within the ±32 ppm allowed for a DS2 signal.

Under software control, the M13E can generate DS3 idle and AIS signals, and loop back the transmitted DS3 signal to the receiver for test purposes. Other functions provided by the M13E include: DS1 loopback capability, and transmit clock failure protection. The microprocessor interface is selectable via two external hardware straps. Interface options are: Multiplexed, Intel compatible, or Motorola compatible.

PIN DIAGRAM

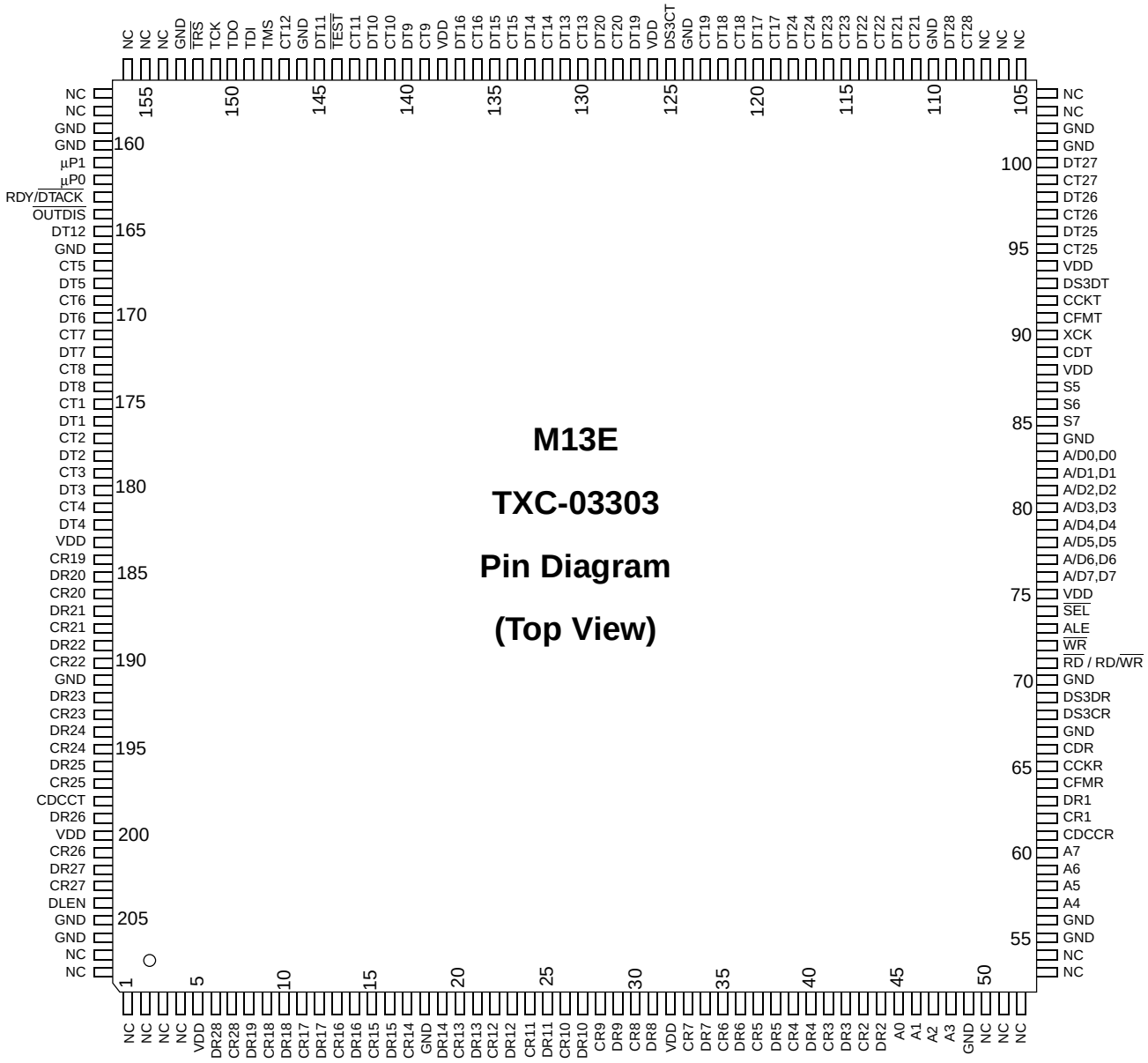


Figure 3. M13E TXC-03303 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY, GROUND, AND NO CONNECT

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	5, 32, 75, 88, 94, 126, 138, 183, 200	P		**VDD:** +5-volt supply voltage, ±5%.
GND	18, 49, 55, 56, 67, 70, 84, 101, 102, 110, 124, 146, 153, 159, 160, 166, 191, 205, 206	P		**Ground:** 0 volts reference
NC	1-4, 50-54, 103-107, 154-158, 207, 208	--		**No Connect:** NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of NC pins may impair performance or cause damage to the device.

*Note: I = Input; O = Output; P = Power

DS1 RECEIVE INTERFACES

Symbol	Pin No.	I/O/P	Type *	Name/Function
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28	62 43 41 39 37 35 33 30 28 26 24 22 20 17 15 13 11 9 184 186 188 190 193 195 197 201 203 7	O	TTL2mA	**Receive Clock Channels 1 - 28:** Receive data is clocked out of the M13E on positive transitions. The clock for the first DS1 channel corresponds to CR1, while the clock for the last DS1 channel corresponds to CR28. The DS1 clock signals are derived from the DS3 clock signal (DS3CR). During periods of DS3/DS2 out of frame or AIS, the M13E provides a DS1 clock signal for clocking out AIS which is derived from the XCK clock (pin 90).

*See Input, Output and I/O Parameters section below for Type definitions.

Symbol	Pin No.	I/O/P	Type *	Name/Function
DR1 DR2 DR3 DR4 DR5 DR6 DR7 DR8 DR9 DR10 DR11 DR12 DR13 DR14 DR15 DR16 DR17 DR18 DR19 DR20 DR21 DR22 DR23 DR24 DR25 DR26 DR27 DR28	63 44 42 40 38 36 34 31 29 27 25 23 21 19 16 14 12 10 8 185 187 189 192 194 196 199 202 6	O	TTL2mA	**Receive Data DS1 Channels 1 - 28:** Demultiplexed DS1 channels. The first DS1 channel corresponds to DR1, while the last DS1 channel corresponds to DR28.

DS1 TRANSMIT INTERFACES

Symbol	Pin No.	I/O/P	Type	Name/Function
CT1 CT2 CT3 CT4 CT5 CT6 CT7 CT8 CT9 CT10 CT11 CT12 CT13 CT14 CT15 CT16 (continued next page)	175 177 179 181 167 169 171 173 139 141 143 147 130 132 134 136	I	TTL	**Transmit DS1 Clocks Channels 1 - 28:** Transmit data is clocked into the M13E on positive transitions. The clock for the first DS1 channel corresponds to CT1, while the clock for the last DS1 channel corresponds to CT28.

Symbol	Pin No.	I/O/P	Type	Name/Function
CT17 CT18 CT19 CT20 CT21 CT22 CT23 CT24 CT25 CT26 CT27 CT28	119 121 123 128 111 113 115 117 95 97 99 108	I	TTL	**Transmit DS1 Clocks** (continued from previous page)
DT1 DT2 DT3 DT4 DT5 DT6 DT7 DT8 DT9 DT10 DT11 DT12 DT13 DT14 DT15 DT16 DT17 DT18 DT19 DT20 DT21 DT22 DT23 DT24 DT25 DT26 DT27 DT28	176 178 180 182 168 170 172 174 140 142 145 165 131 133 135 137 120 122 127 129 112 114 116 118 96 98 100 109	I	TTL	**Transmit Data DS1 Channels 1 - 28:** The first DS1 channel corresponds to DT1, while the last DS1 channel corresponds to DT28.

DS3 INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
DS3CR	68	I	CMOS	**DS3 Receive Clock:** A 44.736 MHz clock that is used to clock DS3 data into the M13E. This clock is used as the time base for demultiplexing the DS3 data. When the loop timing feature is active (a one written into bit 3 (LPTIME) in 02H), or when the DS3 external transmit clock (XCK) fails, this clock becomes the transmit clock.
DS3DR	69	I	CMOS	**DS3 Receive Data:** Receive 44.736 Mbit/s data is clocked into the M13E on positive transitions of the receive clock (DS3CR).
DS3CT	125	O	TTL8mA	**DS3 Transmit Clock:** A 44.736 MHz clock which is derived from the external transmit clock input signal (XCK). It is used to clock DS3 data from the M13E.
DS3DT	93	O	TTL8mA	**DS3 Transmit Data:** Transmit C-bit parity or M13 formatted DS3 data is clocked out of the M13E on positive transitions of the transmit clock (DS3CT).

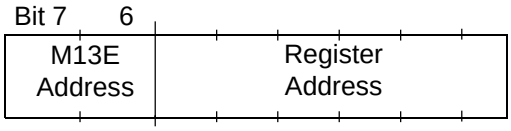
MICROPROCESSOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
A(7-4) A(3-0)	60-57 48-45	I	TTLp	**Address Bus (Intel/Motorola):** These are active high address line inputs that are used by the microprocessor for accessing the M13E registers for a read/write cycle. A7 is the most significant bit. These leads are disabled when the multiplexed interface is selected.
A/D (7-0) D(7-0)	76-83	I/O	TTL8mA	**Address/Data Bus (Multiplexed), Data Bus (Intel/Motorola):** For a multiplexed interface, these bidirectional leads constitute address/data buses for accessing the M13E registers. For either the Intel or Motorola interface, these bidirectional leads are used for transferring data. The most significant bit is A/D7 or D7.
$\overline{\text{SEL}}$	74	I	TTL	**Select:** A low enables data transfers between the microprocessor and the M13E registers during a read/write bus cycle.
$\overline{\text{RD}}$ RD/$\overline{\text{WR}}$	71	I	TTL	**Read (Intel/Multiplexed) or Read/Write (Motorola):** Intel/Multiplexed - An active low signal generated by the microprocessor for reading the M13E register locations. Motorola - An active high signal generated by the microprocessor for reading the M13E register locations. An active low signal is used to write to the M13E register locations.

Symbol	Pin No.	I/O/P	Type	Name/Function
ALE	73	I	TTL	**Address Latch Enable (Multiplexed):** An active high enable signal generated by the microprocessor. The falling transition is used to store an address during a read/write bus cycle.
$\overline{WR}$	72	I	TTL	**Write (Intel/Multiplexed):** Intel/Multiplexed - An active low signal generated by the microprocessor for writing to the M13E register locations. Motorola - not used.
RDY/ $\overline{DTACK}$	163	O	TTL8mA	**Ready (Intel) or Data Transfer Acknowledge (Motorola):** Intel - The M13E is always ready. Connection to an Intel microprocessor is optional. If connected, a pull-up resistor is required. Motorola - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data. A pull-up resistor is required for this pin.
µP0 µP1	162 161	I	TTLp	**Microprocessor Interface Type Select:** The type of microprocessor interface selected by these two bits is given in the table below: µP1 / µP0 / Interface 1 / 1 / Multiplexed[1] 1 / 0 / Multiplexed[2] 0 / 0 / Intel Compatible 0 / 1 / Motorola Compatible The multiplexed interface consists of eight bidirectional address/data leads, select, address latch enable, read, and write. The Intel compatible interface (80X86 family) consists of eight address leads, eight bidirectional data leads, select, read, write, and ready. The Motorola compatible interface (680X0 family) consists of eight address leads, eight bidirectional data leads, select, read/write, and data transfer acknowledge.

Note 1: When µP1 and µP0 are both set to 1 only registers 00H - 1FH are accessible, to maintain backwards compatibility with previous devices. Address straps S5 - S7 are active.

Note 2: When µP1 = 1 and µP0 = 0 all registers are accessible. Only address straps S6 and S7 are active.

Symbol	Pin No.	I/O/P	Type	Name/Function
S(7-5)	85, 86, 87	I	TTLp	**Address Straps:** When the Intel, Motorola, or Multiplexed (µP1 = 1 and µP0 = 0) microprocessor interfaces are selected, the two address straps, S7 and S6, allow the M13E to be partitioned as a segment of memory. The straps define the address offset of the device. The address register is partitioned as shown below. The data register pointed to by the 6 LSBs is only accessed if the 2 MSBs match the address straps. Address register partition for Intel, Motorola, or Multiplexed (µP1 = 1 and µP0 = 0) microprocessor interfaces:  When the multiplexed microprocessor interface is selected, by setting µP1 = 1 and µP0 = 1, the three address straps, S7, S6, and S5, allow the M13E to be partitioned as a segment of memory. The straps define the offset of the device. The address register is partitioned as shown below. The data register pointed to by the five LSBs is only accessed if the three MSBs match the address straps. Address register partition for the multiplexed microprocessor interface when µP1 = 1 and µP0 = 1: 

RECEIVE C-BIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
CCKR	65	O	TTL8mA	**Receive C-Bit Clock:** A gapped clock signal is provided for clocking out the selected receive C-bit data. Data (CDR) is clocked out on positive transitions.
CDR	66	O	TTL8mA	**Receive C-Bit Data:** The following C-bits are provided at this interface: C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21.
CFMR	64	O	TTL8mA	**Receive C-Bit Framing Pulse:** This positive framing pulse occurs prior to the C2 bit.
CDCCR	61	O	TTL8mA	**Receive Data Link Indication:** A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15). The receive C-bit clock (CCKR) may be and-gated with this signal to provide a gapped data link clock signal for loading the three C-bits from the C-bit data (CDR) into external circuitry. This signal is enabled by placing a high on the signal lead labeled DLEN.

TRANSMIT C-BIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
CCKT	92	O	TTL8mA	**Transmit C-Bit Clock:** A gapped clock signal is provided for clocking in selected transmit C-bit data (CDT). Data is clocked into the M13E on positive transitions.
CDT	89	I	TTL	**Transmit C-Bit Data:** The transmit gapped clock (CCKT) is provided for clocking in the following C-bits: C2, C3 (depending on the setting of bit 7 of register 19H, C3CLKI), C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. An unused C-bit should be transmitted as a one.
CFMT	91	O	TTL8mA	**Transmit C-Bit Framing Pulse:** This positive framing pulse occurs prior to the C2 bit.
CDCCT	198	O	TTL8mA	**Transmit Data Link Indication:** A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15). The transmit C-bit clock (CCKT) may be and-gated with this signal to provide a gapped data link clock signal. This signal is enabled by placing a high on the signal lead labeled DLEN.

CONTROL PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{OUTDIS}}$	164	I	TTLp	**Outputs Disable:** A low causes all M13E outputs and bidirectional signal leads to be set to a high impedance state for test purposes except the CDCCR and CDCCT pins. The CDCCR and CDCCT pins can be tri-stated by applying a low to the DLEN pin. This lead is provided with an internal pull-up resistor.
DLEN	204	I	TTLp	**Data Link Enable:** Normally left open. A high enables the transmit and receive data link indication signals, CDCCT and CDCCR. The data link indication signals identify the location of the three data link C-bits (C13, C14, and C15).
$\overline{\text{TEST}}$	144	I	TTLp	**TranSwitch Test Pin:** Leave open.

EXTERNAL CLOCK

Symbol	Pin No.	I/O/P	Type	Name/Function
XCK	90	I	CMOS	**External Transmit Clock:** An external clock having a frequency of 44.736 MHz and a stability of ±20 ppm is required to meet DSX-3 cross-connect requirements. The clock duty cycle should be kept to (50 ±5)%. The transmit clock is also used to operate the M13E microprocessor interface. The M13E monitors this clock for transitions. When a clock failure is detected, the M13E automatically switches to the receive clock (DS3CR) for multiplexer and microprocessor operation. Receive loop timing (a one written to bit 3, LPTIME, in 02H) also causes the receive clock to become the transmit clock.

TEST ACCESS PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
TMS	148	I	TTLp	**Test Mode Select:** The signal present on this lead is used to control boundary scan test operations.
TDI	149	I	TTLp	**Test Data Input:** Serial data input for boundary scan test messages.
TDO	150	O	TTL8mA	**Test Data Output:** Serial data output whose information is clocked out on negative transitions of TCK.
TCK	151	I	TTLp	**Test Clock:** The input clock for boundary scan testing. The TDI and TMS states are clocked in on positive transitions.
$\overline{\text{TRS}}$	152	I	TTLp	**Test Reset:** When an active low signal is applied to this pin, the M13E Test Access Port (TAP) controller resets and the boundary scan is disabled. The controller is also reset by writing F0H followed by 00H to the initialization register 1FH or by holding the TMS signal lead high for at least five rising clock transitions of TCK. During power-up of the M13E, this pin must be held low, to reset the TAP controller. Failure to do so may cause the TAP controller to take control of the M13E output pins. When the boundary scan feature is not used, this pin must be held low.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		$\pm$2000	V	per MIL-STD-833D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		40	42	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			133	mA	
P_{DD}			700	mW	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 V
Input capacitance		5.5		pF	

Note: Input has a 9K (nominal) internal pull-up resistor.

OUTPUT PARAMETERS FOR TTL2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -1.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-1.0	mA	
t_{RISE}	5.0	11.0	20.0	ns	C_{LOAD} = 15 pF
t_{FALL}	2.0	4.0	8.0	ns	C_{LOAD} = 15 pF

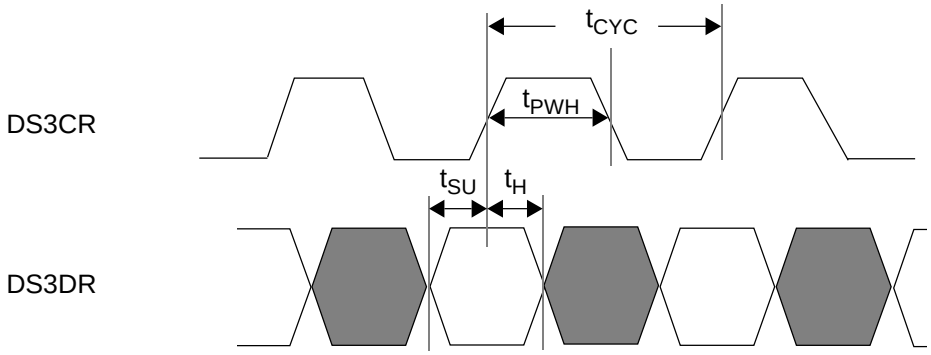
INPUT/OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 $\leq V_{DD} \leq$ 5.25
V_{IL}			0.8	V	4.75 $\leq V_{DD} \leq$ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.4	4.9	7.0	ns	C_{LOAD} = 25 pF
t_{FALL}	1.1	1.8	2.5	ns	C_{LOAD} = 25 pF

TIMING CHARACTERISTICS

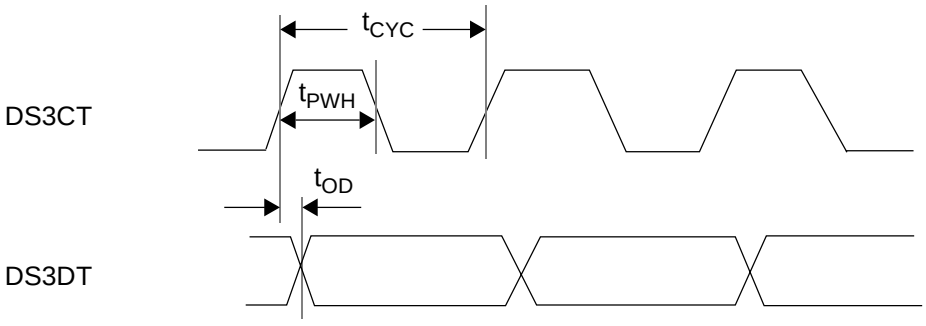
Detailed timing diagrams for the M13E are illustrated in Figures 4 through 16, with values of the timing intervals tabulated below each diagram. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

Figure 4. DS3 Receive Timing



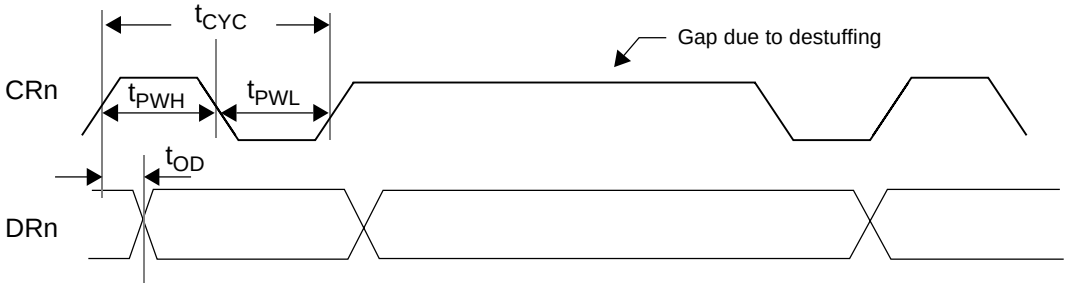
Parameter	Symbol	Min	Typ	Max	Unit
DS3CR clock period	t_{CYC}	20.0	22.35		ns
DS3CR duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
DS3DR set-up for DS3CR↑	t_{SU}	-1.0			ns
DS3DR hold time after DS3CR↑	t_H	6.0			ns

Figure 5. DS3 Transmit Timing



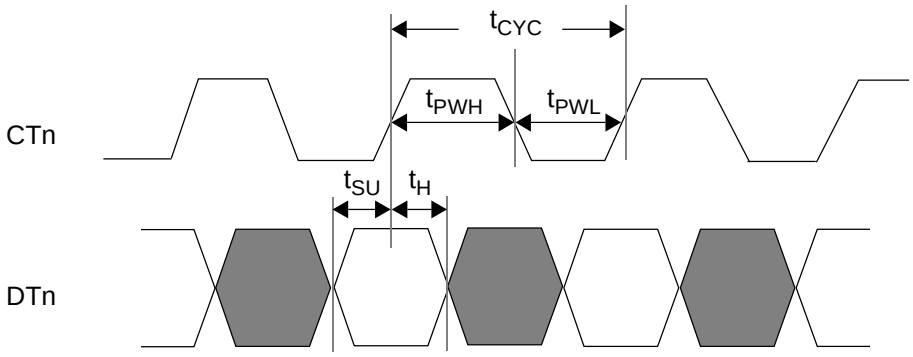
Parameter	Symbol	Min	Typ	Max	Unit
DS3CT clock period	t_{CYC}	20.0	22.35		ns
DS3CT duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
DS3DT output delay after DS3CT↑	t_{OD}	2.5		8.0	ns

Figure 6. DS1 Receive Timing



Parameter	Symbol	Min	Typ	Max	Unit
CR clock period	t_{CYC}	585		1300	ns
CR high time	t_{PWH}	14 DS3CR Cycles		21 DS3CR Cycles	ns
CR low time	t_{PWL}	14 DS3CR Cycles		14 DS3CR Cycles	ns
DR output delay after CR↑	t_{OD}	-12		10	ns

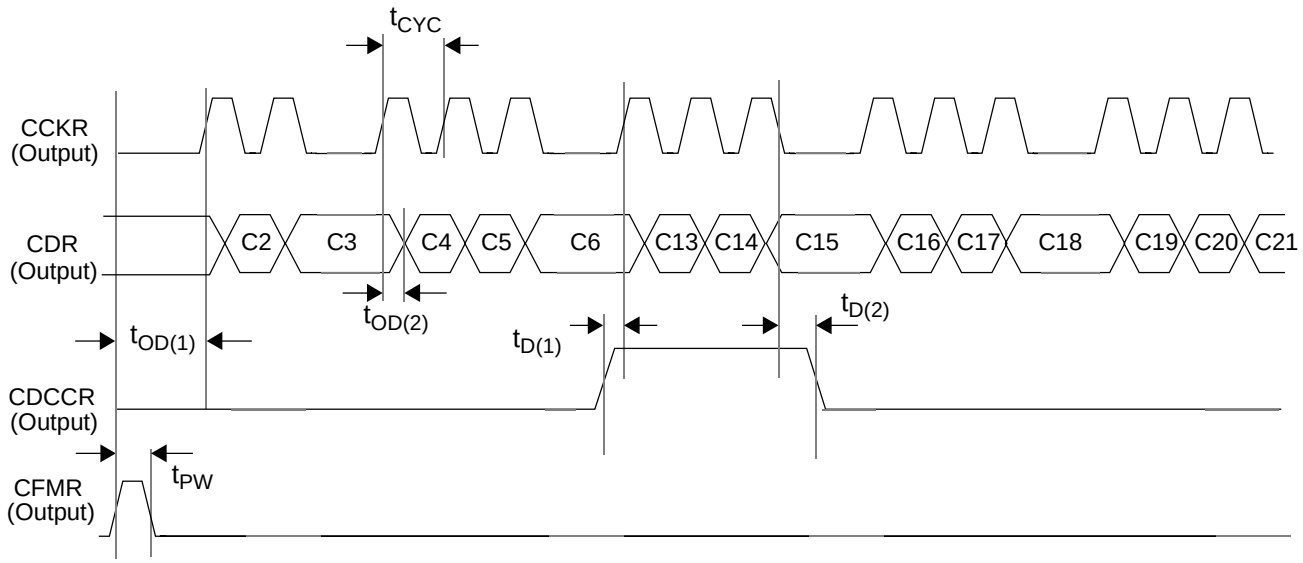
Figure 7. DS1 Transmit Timing



Parameter	Symbol	Min	Typ	Max	Unit
CT clock period	t_{CYC}	583	648	712.8	ns
CT high time	t_{PWH}	174	324	453	ns
CT low time	t_{PWL}	174	324	453	ns
CT duty cycle (t_{PWH}/t_{CYC})	--	30	50	70	%
DT set-up time to CT↑	t_{SU}	4			ns
DT hold time after CT↑	t_H	6			ns

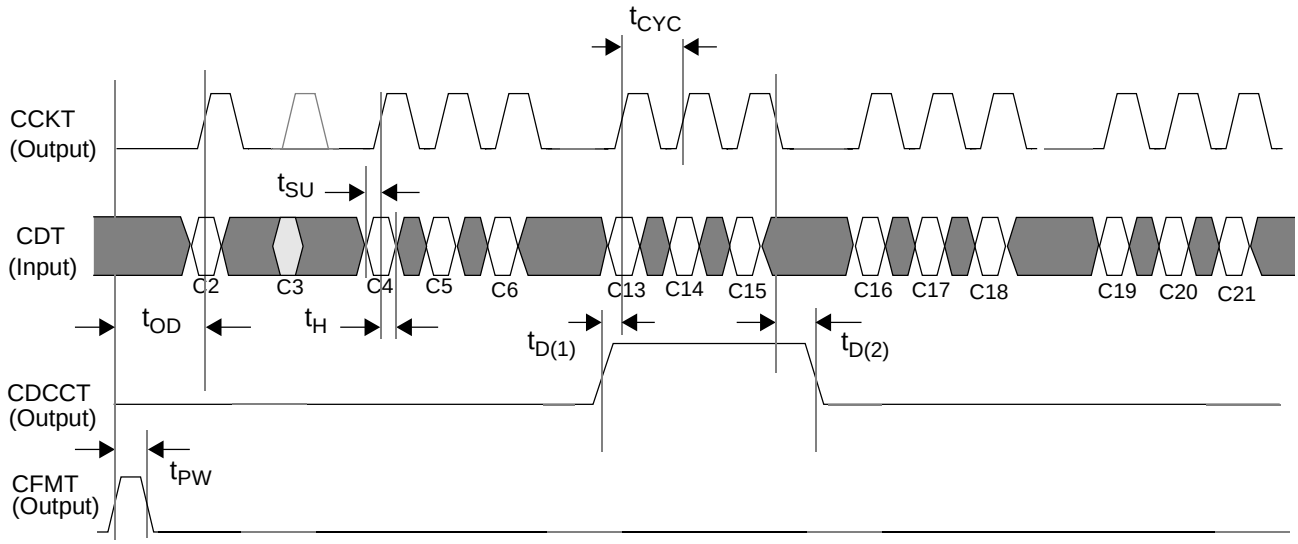
Note: Each DS1 input can be asynchronous with respect to another DS1 channel. The diagram above is shown for INVCK = 0. When INVCK = 1 DTn is clocked into the M13E on the falling edges of their corresponding CTn signals.
The timing parameters in the table above do not change when INVCK = 1 except that t_{SU} and t_H are measured with respect to the falling edges of the CTn signals.

Figure 8. C-Bit Receive Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
CCKR clock period	t_{CYC}		3800		ns
CCKR output delay after CFMR↑	$t_{OD(1)}$		3800		ns
CDR output delay after CCKR↑	$t_{OD(2)}$	0	13	20	ns
CCKR↑ delay after CDCCR↑	$t_{D(1)}$		1900		ns
CDCCR↓ delay after CCKR↓	$t_{D(2)}$		3800		ns
CFMR pulse width (high)	t_{PW}		1900		ns

Figure 9. C-Bit Transmit Interface Timing

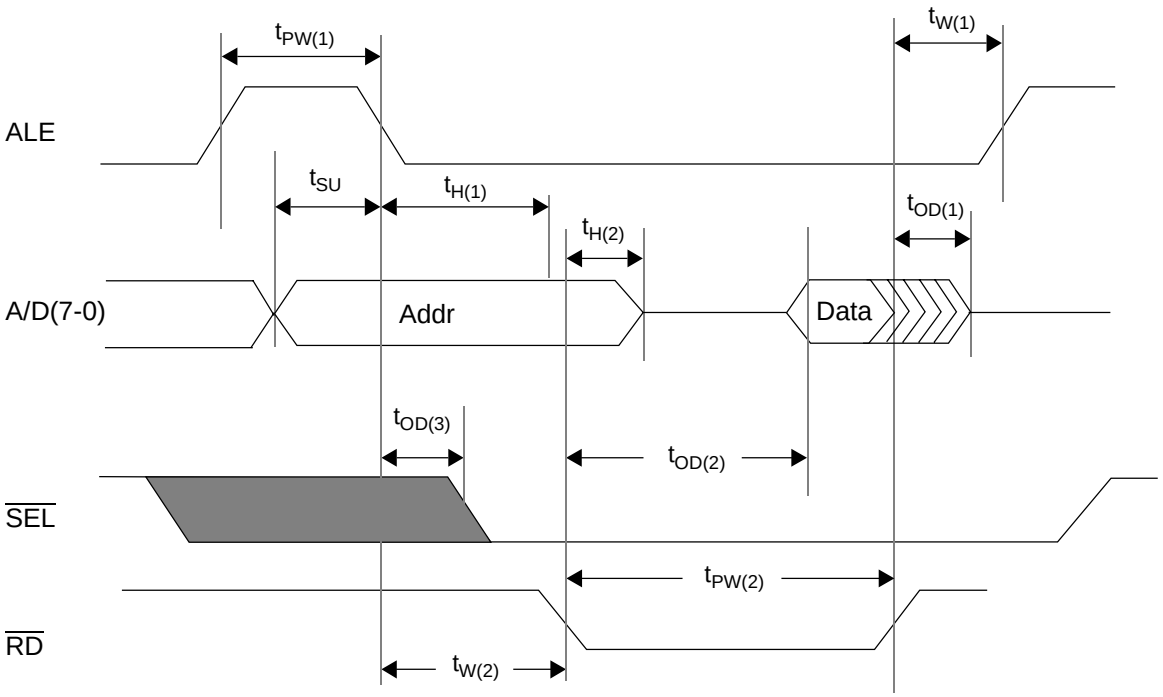


Note 1: A C-bit must be transmitted as a one when not needed.

Note 2: Following normal power-up procedures, bit 7 in register 19H will be set to “0” and the extra clock pulse for the C3 bit in the CCKT clock will be present. If bit 7 is then set to “1,” the extra C3 bit clock pulse will not be present.

Parameter	Symbol	Min	Typ	Max	Unit
CCKT clock period	t_{CYC}		3800		ns
CDT set-up time to CCKT↑	t_{SU}	25			ns
CDT hold time after CCKT↑	t_{H}	40			ns
CCKT output delay after CFMT↑	t_{OD}		3800		ns
CCKT↑ delay after CDCCT↑	$t_{D(1)}$		1900		ns
CDCCT↓ delay after CCKT↓	$t_{D(2)}$		3800		ns
CFMT pulse width	t_{PW}		1900		ns

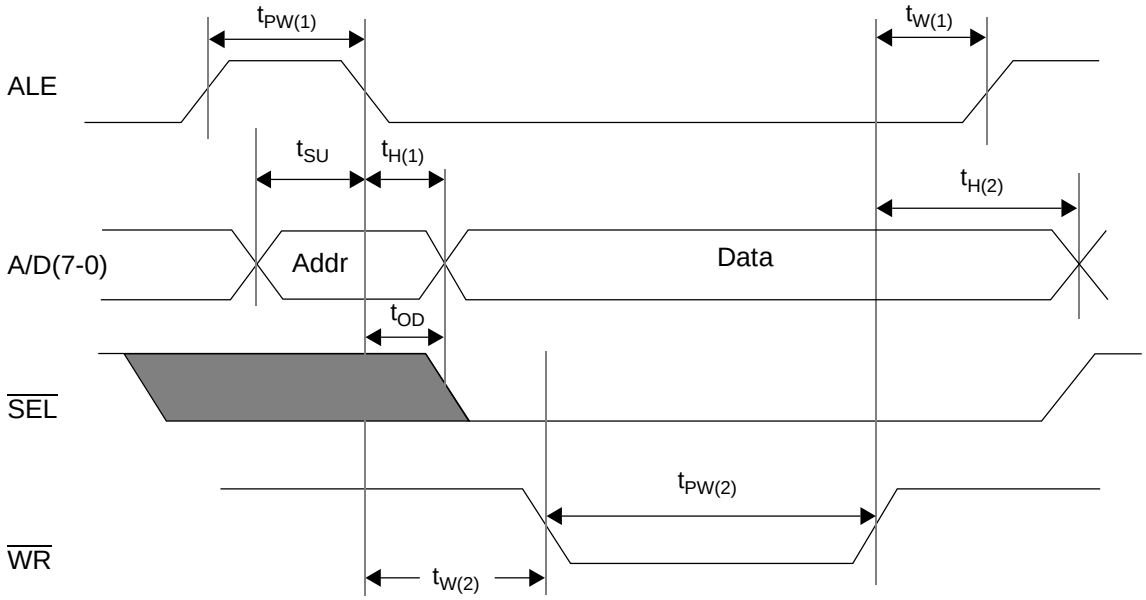
Figure 10. Microprocessor Read Cycle Timing - Multiplexed Interface



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	95			ns
ALE wait after $\overline{RD}$ ↑	$t_{W(1)}$	20			ns
A/D(7-0) address set-up time to ALE ↓	t_{SU}	30			ns
A/D(7-0) address hold time after ALE ↓	$t_{H(1)}$	25			ns
A/D(7-0) address hold time after $\overline{RD}$ ↓	$t_{H(2)}$			20	ns
A/D(7-0) data output delay (to tri-state) after $\overline{RD}$ ↑	$t_{OD(1)}$	10		50	ns
A/D(7-0) data valid delay after $\overline{RD}$ ↓	$t_{OD(2)}$			150	ns
$\overline{SEL}$↓ delay after ALE↓	$t_{OD(3)}$			80	ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	180			ns
$\overline{RD}$ wait after ALE ↓	$t_{W(2)}$	25			ns

Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

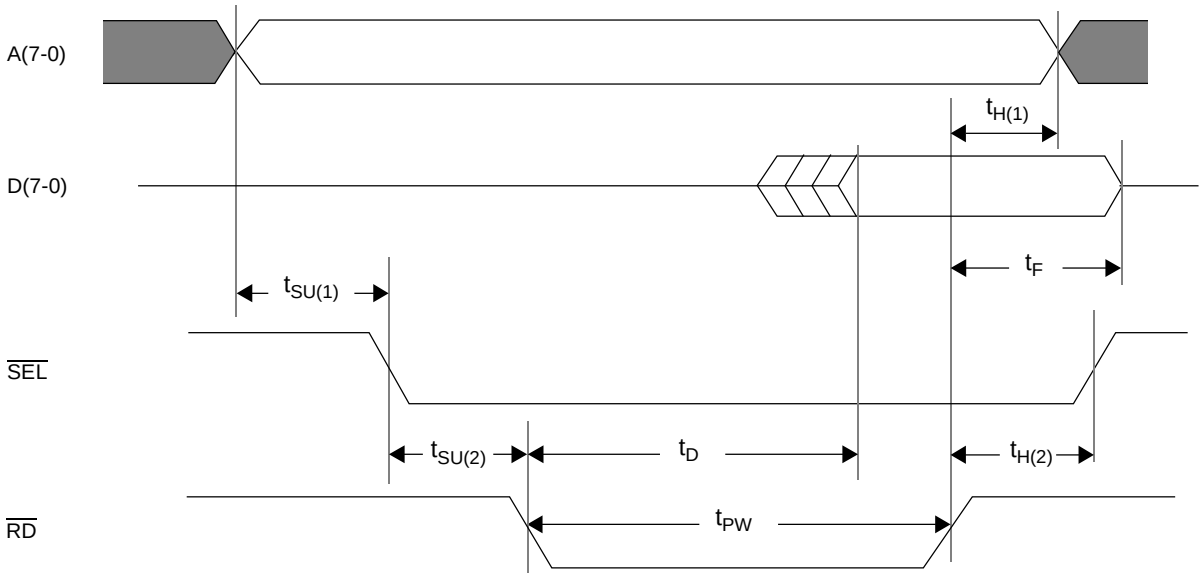
Figure 11. Microprocessor Write Cycle Timing - Multiplexed Interface



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	95			ns
ALE wait after $\overline{WR}$ ↑	$t_{W(1)}$	20			ns
A/D(7-0) address set-up time to ALE ↓	t_{SU}	30			ns
A/D(7-0) address hold time after ALE ↓	$t_{H(1)}$	25			ns
A/D(7-0) data hold time after $\overline{WR}$ ↑	$t_{H(2)}$	20			ns
$\overline{SEL}$ output delay after ALE↓	t_{OD}			80	ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	200			ns
$\overline{WR}$ wait after ALE ↓	$t_{W(2)}$	25			ns

Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

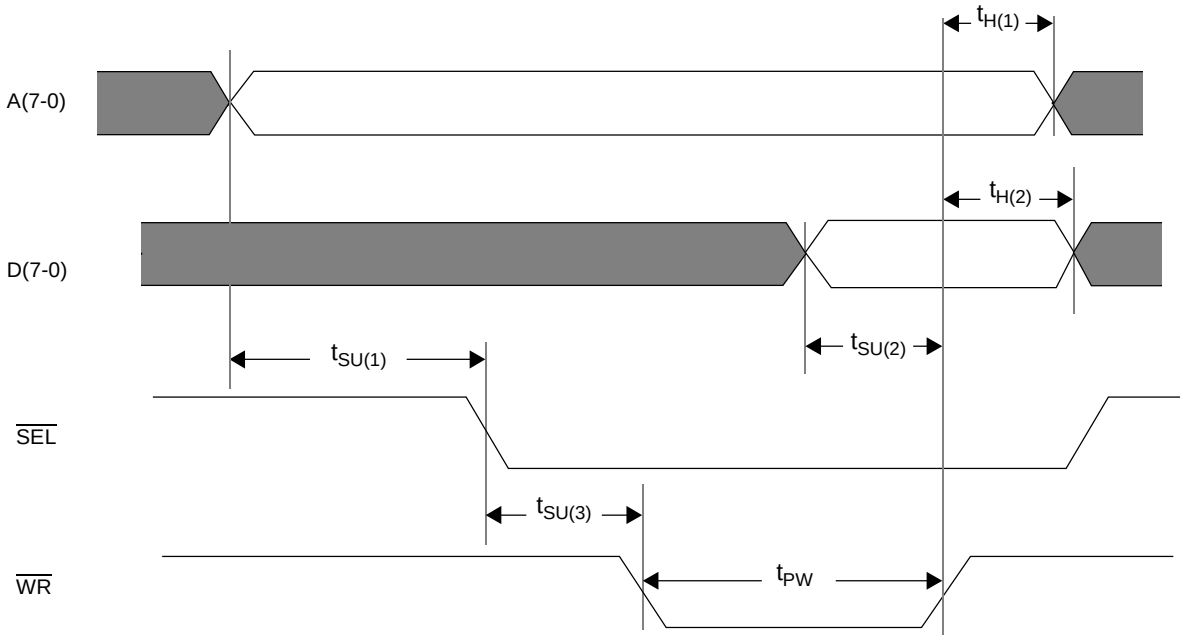
Figure 12. Microprocessor Read Cycle Timing - Intel Interface



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0			ns
A(7-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid delay after $\overline{RD}\downarrow$	t_D			60	ns
D(7-0) data float time after $\overline{RD}\uparrow$	t_F			80	ns
$\overline{RD}$ pulse width	t_{PW}	80			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	10			ns
$\overline{SEL}\uparrow$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	0			ns

Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

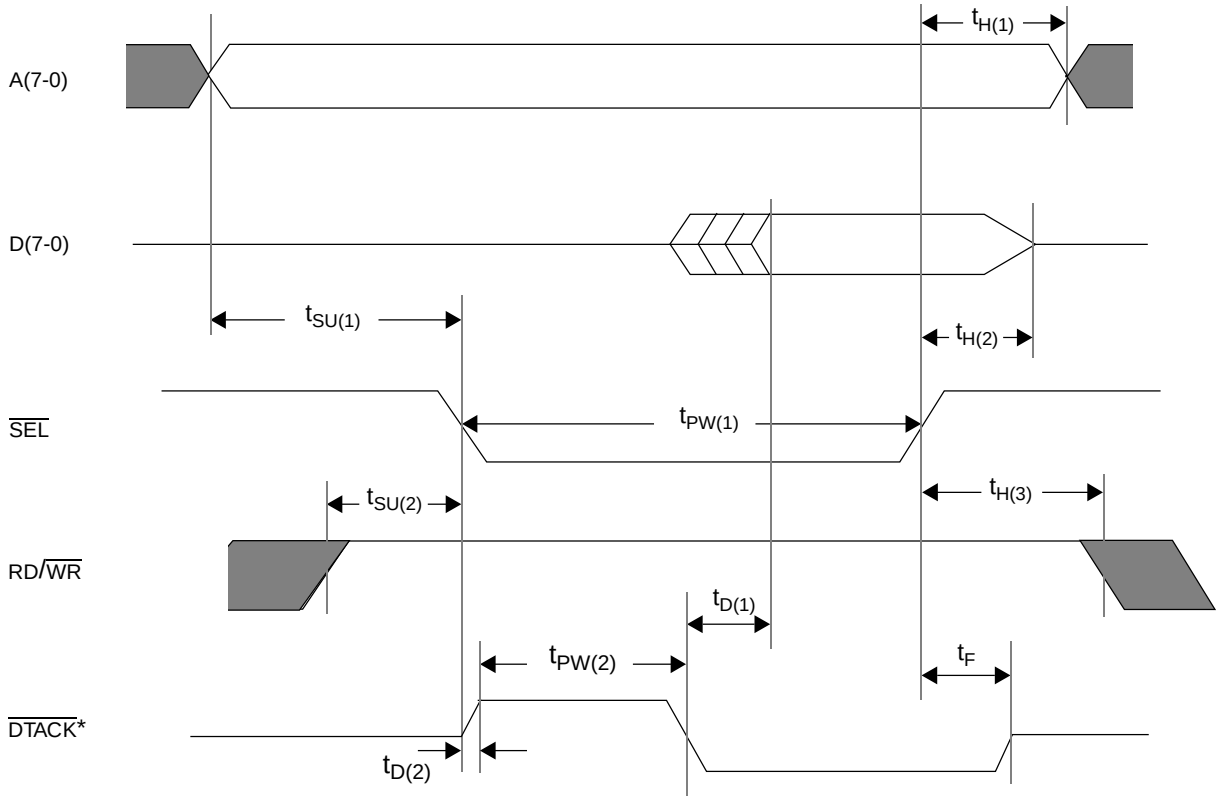
Figure 13. Microprocessor Write Cycle Timing - Intel Interface



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	0			ns
A(7-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid set-up time to $\overline{WR}\uparrow$	$t_{SU(2)}$	20			ns
D(7-0) data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	10			ns
$\overline{WR}$ pulse width	t_{PW}	80			ns

Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

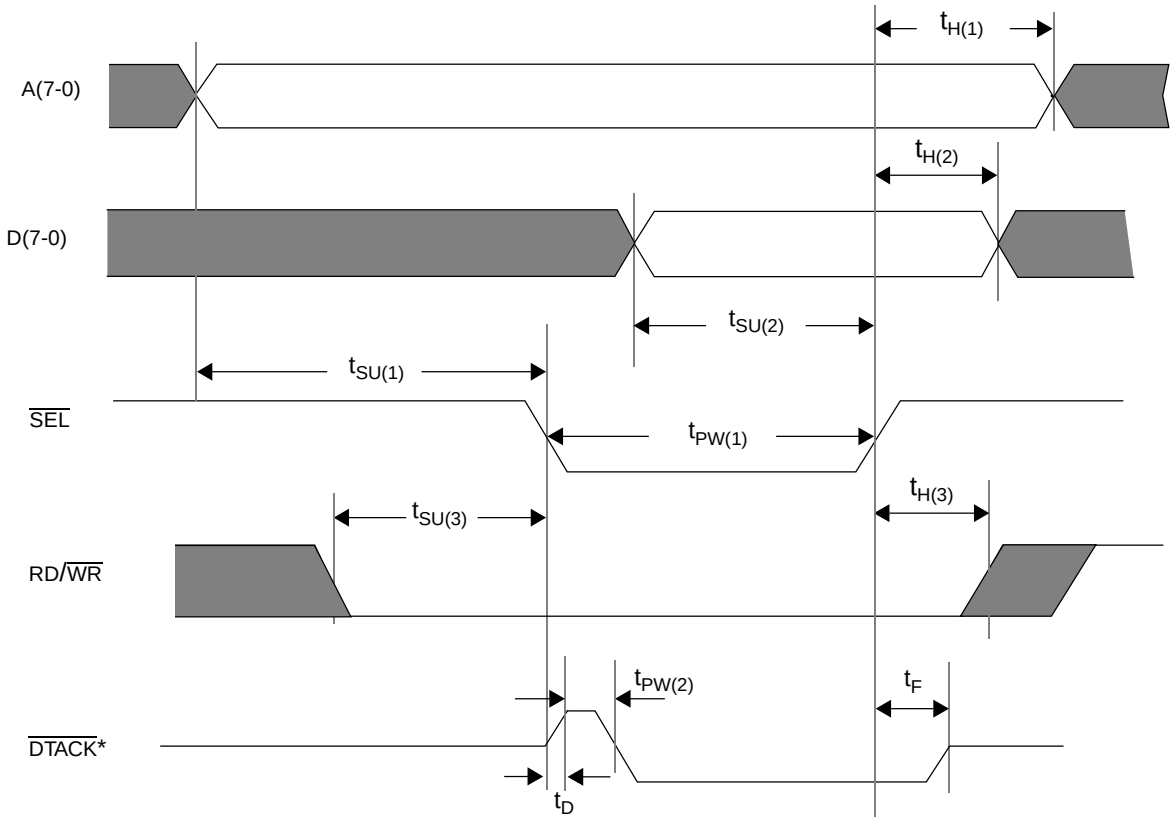
Figure 14. Microprocessor Read Cycle Timing - Motorola Interface



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0			ns
A(7-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$		16	21	ns
D(7-0) data hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$			42	ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	60			ns
RD/$\overline{WR}\uparrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	20			ns
RD/$\overline{WR}\downarrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			60	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0		4	µs
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			20	ns

* The $\overline{DTACK}$ signal lead is tri-stated when $\overline{SEL}$ is high.
Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

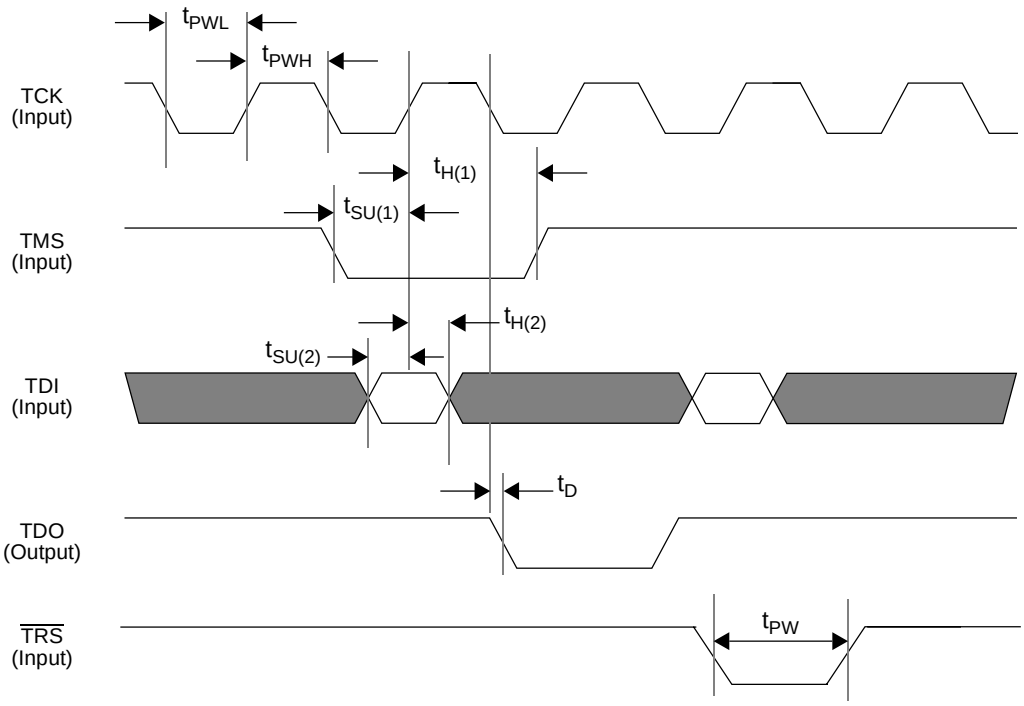
Figure 15. Microprocessor Write Cycle Timing - Motorola Interface



Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0			ns
A(7-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid set-up time to $\overline{SEL}\uparrow$	$t_{SU(2)}$	10			ns
D(7-0) data hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	60			ns
RD/$\overline{WR}\downarrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	20			ns
RD/$\overline{WR}\uparrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	t_D			60	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$			4	µs
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			20	ns

* The $\overline{DTACK}$ signal lead is tri-stated when $\overline{SEL}$ is high.
Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.

Figure 16. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	2.0	-	ns
TDO delay from TCK↓	t_D	-	7.0	ns
$\overline{TRS}$ pulse width	t_{PW}	10	-	ns

OPERATION

MEMORY MAP

The M13E memory map consists of control bits, alarms (non-latched and latched), and counters accessed by a microprocessor read/write cycle. The unused bit positions (shown below shaded) in a register must be masked by software to avoid reading incorrect data. At power up the memory map will remain random until a soft reset is applied via register 1FH. This register location is used to reset and initialize the M13E. After power becomes stable, a F0 Hex followed by a 00 Hex must be written into this location.

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R	R3LOS	R3OOF	R3AIS	R3IDL	R3CKF	T3CKF	XR2	XR1
01	R/W			T3AIS	T3IDL	FEBE	PBITE	CBITE	XT
02	R/W	IDLB	IDLA	TEST1	3LBK	LPTIME	INVCK	1INV	M13MODE
03	R	CBIT1	DS2OOF7	DS2OOF6	DS2OOF5	DS2OOF4	DS2OOF3	DS2OOF2	DS2OOF1
04	R	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
05	R	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0
06	R	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0
07	R/W	EXEC	CON/DIS	LBSEL	D22	D21	D20	D11	D10
08	R	LBALL	LB25	LB21	LB17	LB13	LB9	LB5	LB1
09	R	LBDS3	LB26	LB22	LB18	LB14	LB10	LB6	LB2
0A	R		LB27	LB23	LB19	LB15	LB11	LB7	LB3
0B	R		LB28	LB24	LB20	LB16	LB12	LB8	LB4
0C	R		LOS25	LOS21	LOS17	LOS13	LOS9	LOS5	LOS1
0D	R		LOS26	LOS22	LOS18	LOS14	LOS10	LOS6	LOS2
0E	R		LOS27	LOS23	LOS19	LOS15	LOS11	LOS7	LOS3
0F	R		LOS28	LOS24	LOS20	LOS16	LOS12	LOS8	LOS4
10	R/W		IDL25	IDL21	IDL17	IDL13	IDL9	IDL5	IDL1
11	R/W		IDL26	IDL22	IDL18	IDL14	IDL10	IDL6	IDL2
12	R/W		IDL27	IDL23	IDL19	IDL15	IDL11	IDL7	IDL3
13	R/W		IDL28	IDL24	IDL20	IDL16	IDL12	IDL8	IDL4
14	R		R2X7	R2X6	R2X5	R2X4	R2X3	R2X2	R2X1
15	R/W		T2X7	T2X6	T2X5	T2X4	T2X3	T2X2	T2X1
16	R(L)	R3LOS	R3OOF	R3AIS	R3IDL	R3CKF	T3CKF	$\overline{XR2}$	$\overline{XR1}$
17	R(L)	CERROR	DS2OOF7	DS2OOF6	DS2OOF5	DS2OOF4	DS2OOF3	DS2OOF2	DS2OOF1
18		TEST							
19	R/W	C3CLKI	TEST						
1A		TEST							
1B	R	FME7	FME6	FME5	FME4	FME3	FME2	FME1	FME0
1C	R/W	EXEC	CONT/10	TFEAC6	TFEAC5	TFEAC4	TFEAC3	TFEAC2	TFEAC1
1D	R	FIDL	NEW	RFEAC6	RFEAC5	RFEAC4	RFEAC3	RFEAC2	RFEAC1
1E	R/W	EXEC	CON/DIS		LLB22	LLB21	LLB20	LLB11	LLB10
1F**	R/W	RESET							
20	R/W	1TRIST	1LOSSEL	1TAIS1	1TAIS0	1LBV3	1LBV2	1LBV1	1LBV0
21	R/W				R3AIS2	R3AIS1	R3AIS0	T3AIS1	T3AIS0
22	R	C1BZ7	C1BZ6	C1BZ5	C1BZ4	C1BZ3	C1BZ2	C1BZ1	C1BZ0
23	R	ME7	ME6	ME5	ME4	ME3	ME2	ME1	ME0
24	R(L)	AISX=1	AISC=0	TEST					SEF

*Read/write (R/W); Read only (R); Read only - latched register R(L).
**F0H followed by 00H resets the entire device.

MEMORY MAP DESCRIPTIONS

Address	Bit	Symbol	Description
00	7	R3LOS	**Receive DS3 Loss of Signal:** A receive LOS alarm occurs when the incoming DS3 data (DS3DR) is stuck low for more than 1022 clock cycles (DS3CR). Recovery occurs when two or more ones are detected in the incoming data bit stream. This bit position is unlatched.
	6	R3OOF	**Receive DS3 Out of Frame:** A receive OOF alarm occurs when three out of 16 F-bits are in error utilizing a sliding window of 16 bits, or one or more M-bits are in error in two consecutive frames. Recovery occurs when the F framing pattern of 1001 is detected, and the M framing pattern of 010 is detected for two consecutive frames. Recovery takes approximately 0.95 milliseconds, worst case. This bit position is unlatched. An OOF also inhibits the performance counters (04H, 05H, 06H, 1BH, 22H, and 23H).
	5	R3AIS	**Receive AIS Alarm Indication Signal:** The M13E detects DS3 AIS by six methods. The method of detection that drives the R3AIS alarm is selected by the states written to the three R3AISn bits in register 21H. This bit position is unlatched. When the M13E is configured to detect one of the framed AIS signals (selected via bits 4-2 of register 21H), the R3OOF (bit 6 of this register) should be examined to ensure that the M13E is detecting DS3 frame.
	4	R3IDL	**Receive DS3 Idle Pattern Signal:** A DS3 idle pattern signal has a valid M-frame alignment channel, M-subframe alignment channel, and P-bit channel. The information bits are a 1100 sequence that starts with 11 after each M-frame alignment, M-subframe alignment, X-bit, P-bit, and C-bit channels. The C-bits (C7, C8, and C9) in M-subframe 3 are set to zero. A valid received DS3 idle signal is detected when the M13 detects zeros for C7, C8, and C9 in subframe 3 and the 1100 sequence. The M13E searches for the 1100 pattern sequence on a per DS3 frame basis. The M13E can tolerate up to and including 5 errored 4-bit groups of the 1100 pattern per DS3 frame and still recognize the 1100 pattern as valid. If the M13E detects 6 or more errored 4-bit groups of the 1100 pattern per DS3 frame the M13E will exit the R3IDL state. This bit position is unlatched. A DS3 idle signal as defined in ANSI T1.107a-1990 is being received by the M13E device if this bit and bits 1 and 0 of this register are all set to 1.
	3	R3CKF	**Receive DS3 Clock Failure:** A receive DS3 clock failure alarm occurs when the receive clock (DS3CR) is stuck high or low for 30-100 DS3 clock periods. Recovery occurs on the first clock transition. The demultiplexer does not function when the receive clock is lost. The DS3CR pin is still monitored for this alarm during DS3 line loopback (control bit 3LBK=1), so that it may be necessary to set control bits 1TAIS1 and 1TAIS0 to 11 to prevent AIS insertions into the receive DS1 data stream. This bit position is unlatched.
	2	T3CKF	**Transmit DS3 Clock Failure:** A transmit DS3 clock failure alarm occurs when the transmit input clock (XCK) is stuck high or low for 30-100 DS3 clock periods. A failure causes the receive clock to become the transmit clock. This permits the M13E microprocessor interface and multiplexer to function. Recovery occurs when the first clock transition is detected.
	1	XR2	**Receive DS3 X-bit Number 2:** This bit position indicates the receive state of X2. This bit position is updated each frame.

Address	Bit	Symbol	Description
00 (cont.)	0	XR1	**Receive DS3 X-bit Number 1:** This bit position indicates the receive state of X1. This bit position is updated each frame.
01	5	T3AIS	**Transmit DS3 Alarm Indication Signal:** A one causes the M13E to transmit a DS3 AIS. The type of AIS sent is determined by the states written into bit 1 (T3AIS1) and bit 0 (T3AIS0) in register 21H.
	4	T3IDL	**Transmit DS3 Idle Signal:** To transmit a DS3 idle signal, (i) a one must be written in this bit 4 (T3IDL) register location, and (ii) a one must also be written (if not already written) into bit 0 (XT) of this register 01H, and (iii) bit 0 (T3AIS0) and bit 1 (T3AIS1) of register 21H must also be set to zero.
	3	FEBE	**Transmit Far End Block Error:** A one causes the M13E to transmit a single FEBE error indication (C10, C11, and C12 equal to 0) in the next DS3 frame. To send an additional FEBE indication, the microprocessor must first write a zero followed by a one.
	2	PBITE	**Transmit P-Bit Parity Error:** A one causes the M13E to transmit a single P-bit parity error in the next DS3 frame. The P-bit error is transmitted by inverting the value of the two calculated bits. To send an additional error, the microprocessor must first write a zero followed by a one.
	1	CBITE	**Transmit C-Bit Parity Error:** A one causes the M13E to transmit a single C-bit parity error in the next available DS3 frame when the M13E is operating in the C-bit parity mode. The C-bit error is transmitted by inverting the calculated C-bit parity bits in subframe 3 (C7, C8, and C9). To send an additional error, the microprocessor must first write a zero followed by a one.
	0	XT	**Transmit X-Bits:** The X-bits may be used to transmit a yellow alarm or may be used as a low speed signaling channel. A one or zero causes the M13E to transmit a one or zero for both X1 and X2. Note: Set to 1 when transmitting DS3 idle signal (see T3IDL in this register 01H).

Address	Bit	Symbol	Description
02	7 6	IDLB IDLA	**DS1 Idle Code Selection:** Three DS1 idle codes are provided according to the table given below. A selected idle code is common to all DS1 channels selected. One or more transmitted DS1 channels is selected by writing a one in IDLn register locations 10H, 11H, 12H, or 13H, provided register location 1EH has not selected that DS1 channel for loopback. **IDLB** / **IDLA** / **DS1 Idle Code Selected** 0 / 0 / Quasi-Random Signal (2^{20} - 1 QRS) including zero suppression. 1 / 0 / Framed Extended Super Frame (ESF) signal format which consists of an S-bit pattern of 001011 in every fourth signaling bit position, CRC-6 pattern, and ones in the 64 kbit/s channels 1 through 24. X / 1 / Unframed all ones signal (AIS).
	5	TEST1	**Reserved for TranSwitch Testing Purposes:** A zero must be written into this bit position.
	4	3LBK	**DS3 Line Loopback:** A one disables the DS3 receive input and causes the DS3 transmit output to be looped back as receive data. Transmit data is provided at the output (DS3DT).
	3	LPTIME	**Receive Loop Timing:** A one disables the transmit clock input (XCK), and causes the DS3 receive clock to become the DS3 transmit clock. If the DS3 receive clock fails in this mode, the M13E switches over to the transmit clock. The demultiplexer becomes inoperative, but the multiplexer and microprocessor interface continue to function.
	2	INVCK	**Invert DS1 Transmit Clocks:** A one causes all transmit DS1 data inputs (DTn) to be sampled on the falling edges of their respective DS1 clock inputs (CTn). This is provided for back-to-back M13 operation.
	1	1INV	**Invert DS1 Transmit Data:** A one causes the transmit data inputs for all DS1 channels (DTn) to be inverted.
	0	M13MODE	**M13 Operating Mode:** A one enables the M13E to operate in the M13 mode as specified in Bellcore TR-TSY-000009, and the ANSI T1.107-1988 standard. A zero enables the M13E to operate in the C-bit parity mode as specified in the ANSI T1.107a-1990, supplement to ANSI T1.107-1988.
03	7	CBIT1	**C-bit Number 1 State:** This bit is updated each frame with the state of the received C1 bit. The C1 bit is used to identify the DS3 application according to the table given below: **C1 Value** / **Application** Random / M13 format All 1s / C-bit parity format In addition, any C-bit that is received as zero will index the C-bit Equals Zero Counter (C1BZCNT) in 22H.

Address	Bit	Symbol	Description
03 (cont.)	6-0	DS2OOFn (n=7-1)	**DS2 Out of Frame Alarm Indication:** A one in bits 6-0 corresponds to an out of frame alarm for the corresponding DS2 channel (7-1). A DS2 OOF occurs when two out of four consecutive framing bits are in error. A DS2 OOF for a DS2 channel causes AIS to be inserted into its four DS1 channels when 1TAIS1, 1TAIS0 = 0, 0 or 0, 1. Recovery is based on searching for the 0101 framing pattern. Framing is accomplished by starting at an arbitrary point with the first received bit (0 or 1) and looking 49 bit positions later for the bit of opposite sense. This search is performed for 12 bit positions simultaneously. Once the framing pattern is found, one more frame is used to acquire alignment. Recovery takes approximately 6.8 milliseconds, worst case average.
04	7-0	FBn (n=7-0)	**FEBE Performance Counter/DS3 F&M Bit Error Counter:** This performance counter counts the number of FEBEs received since the last read cycle in the C-bit parity mode. A FEBE indication occurs when C10, C11, or C12 is received equal to zero in a DS3 frame. The counter is protected from overflow by stopping at the maximum count of 255 until read. The counter is protected during the period of a microprocessor read cycle and when the M13E is attempting to write to the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterwards, the counter increments. Only the indication of one error count is held during the microprocessor read and the M13E write cycle. The counter is also inhibited during DS3 loss of signal or out of frame times. This counter is cleared when it is read by the microprocessor. In the M13 mode, this saturating counter counts the number of DS3 F&M bits that have been received in error. This counter is inhibited when a DS3 OOF occurs and clears when read.
05	7-0	CPn (n=7-0)	**C-Bit Parity Performance/Number of Frames Counter:** In the C-bit parity mode, this counter counts the number of C-bit parity errors received since the last read cycle. In the M13 mode, it counts the number of DS3 frames since the last read cycle. The counter is protected during the period of a microprocessor read cycle and when the M13E is attempting to write to the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterwards, the counter increments. Only the indication of one error count is held during the microprocessor read and the M13E write cycle. The counter is inhibited during DS3 loss of signal or out of frame times, and is cleared when it is read by the microprocessor.
06	7-0	PPn (n=7-0)	**P-Bit Parity Performance Counter:** This counter counts the number of P-bit parity errors received since the last read cycle. This performance count is valid in either operating mode. The counter is protected during the period of a microprocessor read cycle and when the M13E is attempting to write to the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterward, the counter increments. Only the indication of one error count is held during the microprocessor read and the M13E write cycle. The counter is also inhibited during DS3 loss of signal or out of frame times. This counter is cleared when it is read by the microprocessor.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>07</td><td>7
6
5
4
3
2
1
0</td><td>EXEC
CON/DIS
LBSEL
D22
D21
D20
D11
D10</td><td>Remote Loopback: The bits in this location are used to send a DS1 remote loopback request in the M13 mode, or a DS3/DS1 remote loopback request in the C-bit parity mode. Bit 7 (EXEC) executes the command. Bit 6 (CON/DIS)* selects the command to connect or disconnect the loopback selected. When in C-bit parity mode bit 5 (LBSEL) selects either C or stuff bit inversions, defined by the 1LBVn bits in register 20H or a double FEAC message (in C-bit parity mode only) when sending a loopback request. The C or stuff bit inversion mechanism in the M13 (or C-bit parity) mode is selected by the states written to the four 1LBVn bits in register 20H. Bits 4 (D22), 3 (D21), and 2 (D20) select the DS2 channels (1-7). Bits 1 (D11) and 0 (D10) select one of four DS1 channels. In the C-Parity mode, the FEAC channel (C3) can be used for sending DS1 and DS3 remote loopback requests. The channel to be looped is written into bits 4-0. The M13E translates this code into the FEAC codeword. To send a loopback request using the FEAC channel, the M13E sends 10 repetitions of the FEAC line activator code sequence (0 000111 0 11111111) followed immediately by 10 repetitions of the loopback codeword (0 xxxxxx 0 11111111). At the end of this sequence (20 codewords or 320 DS3 frames), completion is indicated by bit 7 (EXEC) resetting to zero. To deactivate a loopback using the FEAC channel, the M13E sends 10 repetitions of the deactivate code followed immediately by 10 repetitions of the channel selected. Only one loopback request can be sent at a time. The codes for sending and deactivating a remote loopback request are shown below:
<table>
<tr><th>Bits</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><th>Channel</th><th>EXEC</th><th>CON/DIS</th><th>LBSEL</th><th>D22</th><th>D21</th><th>D20</th><th>D11</th><th>D10</th></tr>
<tr><td>All</td><td>1</td><td>1 or 0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Channel 1</td><td>1</td><td>1 or 0</td><td>X</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Channel 2</td><td>1</td><td>1 or 0</td><td>X</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>- - - - - - - - - - -</td><td>- - - - - - -</td><td>- - - - - - - - -</td><td>- - - - - -</td><td>- - - - -</td><td>- - - - -</td><td>- - - - -</td><td>- - - - - -</td><td>- - - - - -</td></tr>
<tr><td>Channel 28</td><td>1</td><td>1 or 0</td><td>X</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>DS3</td><td>1</td><td>1 or 0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
</table>
For CON/DIS, Connect = 1, Disconnect = 0
For X, 1 = FEAC (C-bit parity mode only), 0 = C or stuff bit inversion</td></tr>
</table>

*Note: 1 CON/DIS is not used when LBSEL = 0. Instead, bit 7 (EXEC) is used when LBSEL = 0 to send (EXEC=1) or stop sending (EXEC=0) a remote loopback request via the C or stuff bit inversions defined by register 20H bits 3-0. If a loopback request for a different channel is sent via register 07H (that uses C or stuff bit inversion), the current loopback request is taken down. i.e., multiple loopback requests can not be transmitted simultaneously.

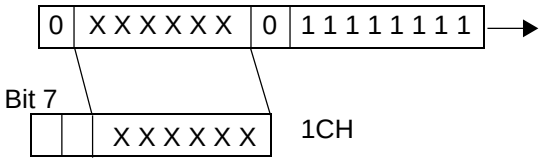
Note: 2 If this register is used to send a remote loopback request using the double word FEAC message then the C3CLKI bit in register 19 Hex must be set to a 1.

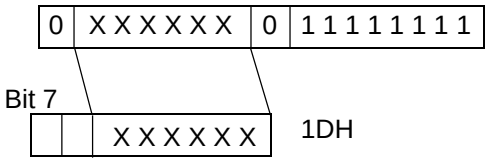
Address	Bit	Symbol	Description
08	7 6 5 4 3 2 1 0	LBALL LB25 LB21 LB17 LB13 LB9 LB5 LB1	**Receive Loopback Requests:** Bit 7, LBALL (all DS1 channels), and bits 6-0 (LBn) indicate the loopback request detected. For the M13 mode, a loopback request is received when any of the conditions (C-bit or stuff) are detected five or more times in succession. The remote loopback selection is determined by the states written to the 1LBVn bits in register location 20H. A remote loopback request is cancelled when the normal state of the bit is received five or more times in succession. In the C-bit parity mode, a remote loopback request is received by detecting the FEAC connect word five times in succession, followed by five consecutive receptions of the DS1 channel number word. A remote loopback request is cleared upon the reception of five consecutive disconnect FEAC messages followed by the reception of the DS1 channel number word. The M13E will also respond to the conditions (C-bit or stuff) set up by the 1LBVn bits in register location 20H while in C-bit parity mode. Note: It is possible to have multiple loopbacks set. Once a loopback request is received or taken down in registers 08H-0BH, the microprocessor must write the appropriate code to register 1EH to correspondingly set up or take down the loopback in the appropriate DS1 channel. When detecting loopback requests via the mechanism indicated by the 1LBVn bits in register 20H, the M13E must have DS2 and DS3 frame synchronization. When detecting loopback requests via the FEAC channel, the M13E must have DS3 frame synchronization and not be receiving DS3 AIS or DS3 Idle signals. LBALL is valid only in C-bit parity mode.
09	7 6 5 4 3 2 1 0	LBDS3 LB26 LB22 LB18 LB14 LB10 LB6 LB2	**Receive Loopback Requests:** Bits 7 (LBDS3) and 6-0 (LBn) indicate loopback requests sent by the distant end for either a DS3 loopback or for the DS1 channels indicated. For complete explanation, see 08H. LBDS3 is valid only in C-bit parity mode.
0A	6 5 4 3 2 1 0	LB27 LB23 LB19 LB15 LB11 LB7 LB3	**Receive Loopback Requests:** Bits 6-0 (LBn) indicate loopback requests sent by the distant end for the DS1 channels indicated. For complete explanation, see 08H.
0B	6 5 4 3 2 1 0	LB28 LB24 LB20 LB16 LB12 LB8 LB4	**Receive Loopback Requests:** Bits 6-0 (LBn) indicate loopback requests sent by the distant end for the DS1 channels indicated. For complete explanation, see 08H.

Address	Bit	Symbol	Description
0C	6 5 4 3 2 1 0	LOS25 LOS21 LOS17 LOS13 LOS9 LOS5 LOS1	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to bit 6 in 20H. A one selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight to sixteen DS2 frames of consecutive zeros.
0D	6 5 4 3 2 1 0	LOS26 LOS22 LOS18 LOS14 LOS10 LOS6 LOS2	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to bit 6 in 20H. A one selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight to sixteen DS2 frames of consecutive zeros.
0E	6 5 4 3 2 1 0	LOS27 LOS23 LOS19 LOS15 LOS11 LOS7 LOS3	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to bit 6 in 20H. A one selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight to sixteen DS2 frames of consecutive zeros.
0F	6 5 4 3 2 1 0	LOS28 LOS24 LOS20 LOS16 LOS12 LOS8 LOS4	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to bit 6 in 20H. A one selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight to sixteen DS2 frames of consecutive zeros.
10	6 5 4 3 2 1 0	IDL25 IDL21 IDL17 IDL13 IDL9 IDL5 IDL1	**Internal DS1 Idle Channel/Loopback:** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a local DS1 loopback. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding DS1 channel in this register location is written with a one, the M13E generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead. The loopback is from the Rx to the Tx direction. When the channel in this register is written with a 0, the DS1 transmit source is from the channel's DTn/CTn pins.

Address	Bit	Symbol	Description
11	6 5 4 3 2 1 0	IDL26 IDL22 IDL18 IDL14 IDL10 IDL6 IDL2	**Internal DS1 Idle Channel/Loopback:** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a local DS1 loopback. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding DS1 channel in this register location is written with a one, the M13E generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead. The loopback is from the Rx to the Tx direction. When the channel in this register is written with a 0, the DS1 transmit source is from the channel's DTn/CTn pins.
12	6 5 4 3 2 1 0	IDL27 IDL23 IDL19 IDL15 IDL11 IDL7 IDL3	**Internal DS1 Idle Channel/Loopback:** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a local DS1 loopback. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding DS1 channel in this register location is written with a one, the M13E generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead. The loopback is from the Rx to the Tx direction. When the channel in this register is written with a 0, the DS1 transmit source is from the channel's DTn/CTn pins.
13	6 5 4 3 2 1 0	IDL28 IDL24 IDL20 IDL16 IDL12 IDL8 IDL4	**Internal DS1 Idle Channel/Loopback:** The bits in this register location are used for generating and transmitting a DS1 idle pattern or a local DS1 loopback. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding DS1 channel in this register location is written with a one, the M13E generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a one is written into the corresponding DS1 channel in this location, the DS1 channel is looped back instead. The loopback is from the Rx to the Tx direction. When the channel in this register is written with a 0, the DS1 transmit source is from the channel's DTn/CTn pins.
14	6-0	R2Xn (n=7-1)	**Receive DS2 X-Bits:** The bits in this location indicate the state of the seven received DS2 channel X-bits.
15	6-0	T2Xn (n=7-1)	**Transmit DS2 X-bits:** The bits in this location are used to transmit the state of the seven DS2 channel X-bits. An X-bit off state is normally a one.
16	7 6 5 4 3 2 1 0	R3LOS R3OOF R3AIS R3IDL R3CKF T3CKF $\overline{XR2}$ $\overline{XR1}$	**Latched Receive Alarms/Status:** The bits in this register location are the same alarm/status bits listed in register location 00H, except the corresponding bit latches on with an alarm. The X-bits are the inverse of the two X-bits received. They latch when they are equal to zero. A microprocessor read cycle clears a set alarm. If an alarm state or status condition remains true (a one), the corresponding bit relatches.

Address	Bit	Symbol	Description
17	7 6-0	CERROR DS2OOFn (n=7-1)	**Latched C-bit Status/DS2 Out Of Frame Bits:** The bits in this register location are the same bits listed in register location 03H, except the corresponding bit latches on with an alarm. For example, CERROR latches to a one on the first time C1 is 0. A microprocessor read cycle clears a set bit. If a DS2 OOF remains true (a one), the corresponding bit relatches.
18	7-0	TEST	**TranSwitch Test Register:** Used for TranSwitch testing. No value is required to be written into this register location.
19	7	C3CLKI	**C-Bit Parity C3 Clock Inhibit:** A zero enables the M13E to generate an extra clock pulse in the CCKT clock signal for clocking the C3 bit in from external logic. A one disables the generation of the C3 clock pulse. This bit must be set to 1 if the FEAC register 1CH is used to transmit FEAC codes or if register 07H is used to send a remote loopback request via a double word FEAC message (LBSEL = 1). If this bit is set to 0, then the FEAC messages are derived from the external C-bit interface.
	6-0	TEST	**TranSwitch Test Bits:** Used for TranSwitch testing. No value is required to be written into these bit locations.
1A	7-0	TEST	**TranSwitch Test Register:** Used for TranSwitch testing. No value is required to be written into this register location.
1B	7-0	FMEn (n=7-0)	**DS3 F-bits and M-bits in Error Counter:** An 8-bit saturating counter that counts the number of DS3 F-bits and DS3 M-bits that are in error since the last read cycle. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared when it is read by the microprocessor.

Address	Bit	Symbol	Description
1C	7 6 5-0	EXEC CONT/10 TFEACn (n=6-1)	**Transmit FEAC Word:** Bit 7 (EXEC) initiates the FEAC transmission and also indicates when the transmission is completed. Bit 6 (CONT/10) controls the duration of the FEAC transmission (1 = continuous, 0 = 10 times). Bits 5-0 (TFEACn) constitute the variable (XXXXXX) field in the FEAC word. A FEAC word is written in the field in the same order of transmission as shown below: **16-Bit FEAC Word**  FEAC Word/Microprocessor Write Relationship The M13E formats and generates the other ones and zeros that comprise the FEAC word. A minimum length (send FEAC word 10 times) message is sent using the following sequence: - Write 1 0 X X X X X X (X=6-bit FEAC word) - M13E sends 16-bit FEAC word 10 times - M13E indicates completion by resetting bit 7 (0 0 X X X X X X) A continuous FEAC word is sent using the following sequence: - Write 1 1 X X X X X X (X=6-bit FEAC word) - M13E sends 16-bit FEAC word continuously - Write Y 0 Y Y Y Y Y Y (Y = Don't Care) - M13E terminates FEAC word transmission - Transmission must be terminated before another FEAC word can be loaded and transmitted. Note: The C3CLKI bit in register 19H must be set to a 1 if this register is used to transmit a FEAC message.

Address	Bit	Symbol	Description
1D	7 6 5-0	FIDL NEW RFEACn (n=6-1)	**Receive Single FEAC Word:** Bit 7 (FIDL) is the FEAC idle channel indication. It clears whenever a zero C3 bit is received framing the six-bit variable word. Bit 7 cannot be reset by a microprocessor read cycle. Bit 6 (NEW) indicates when a new FEAC word has been detected. It clears when the register is read. Bits 5-0 (RFEACn) constitute the variable (XXXXXX) field in the FEAC word. A FEAC word is read in the field in the same order of being received as shown below: **16-Bit FEAC Word**  The following table lists possible FEAC combinations: **FIDL** / **NEW** / **Status** 1 / 0 / FEAC channel idle - No message received since last read cycle 0 / 1 / New message received - FEAC channel busy 1 / 1 / New message received - FEAC channel idle Notes: 1. There is no buffering for the received FEAC message. The latest, validated FEAC message is provided and bit 6 (NEW) is set to one even if the previous message is not read. 2. Line loopback activate and deactivate FEAC codes are not displayed in this register. Also the individual line loopback activate and deactivate codewords are not displayed in this register.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1E</td><td>7
6
4
3
2
1
0</td><td>EXEC
CON/DIS
LLB22
LLB21
LLB20
LLB11
LLB10</td><td>DS1 Local Loopback: This register is used in conjunction with registers 10H-13H. Bit 7 (EXEC) initiates the loopback. This bit is reset upon completion of the command. Bit 6 (CON/DIS) connects or disconnects the specified loopback. Bits 4 through 2 (LLB2n) selects one of seven DS2s. Bits 1 and 0 (LLB1n) selects the DS1 within the DS2 signal. The following table lists the commands for generating local loopback:
<table>
<tr><th>Bits</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><th>Channel</th><th>EXEC</th><th>CON/ DIS</th><th>---</th><th>D22</th><th>D21</th><th>D20</th><th>D11</th><th>D10</th></tr>
<tr><td>All</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Clear All</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Clear All Confirmed</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Channel 1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Channel 2</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>----------</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Channel 28</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Clear Channel 28</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Clear Channel 28 Confirmed</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>1F</td><td>7-0</td><td>RESET</td><td>Initialization Register: This register location is used to reset and initialize the M13E. After power becomes stable, a F0 Hex followed by a 00 Hex must be written into this location.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="4">20</td><td>7</td><td>1TRIST</td><td>Tri-State DS1 Receive Channels: A one causes all 28 receive DS1 data (DRn) and clock (CRn) output leads to be set to a high impedance state.</td></tr>
<tr><td>6</td><td>1LOSSEL</td><td>DS1 Loss of Signal Selection: A zero selects the receive DS1 channels for loss of signal detection. A one selects the transmit DS1 channels for loss of signal detection. The DS1 loss of signals (LOSn) are reported in register locations 0CH through 0FH.</td></tr>
<tr><td>5
4</td><td>1TAIS1
1TAIS0</td><td>DS1 AIS Insertion Selection: These two bits control the insertion of AIS (unframed all ones) into the 28 DS1 channels on certain DS3 alarm conditions that are defined in register location 00H. The following table lists the settings for having various alarm conditions selected to cause AIS:

<table>
<tr><th>1TAIS1</th><th>1TAIS0</th><th>Received DS3 Alarm Conditions</th></tr>
<tr><td>0</td><td>0</td><td>R3OOF, R3AIS, R3LOS, R3CKF</td></tr>
<tr><td>0</td><td>1</td><td>R3OOF, R3AIS, R3CKF</td></tr>
<tr><td>1</td><td>0</td><td>R3LOS</td></tr>
<tr><td>1</td><td>1</td><td>No AIS insertions</td></tr>
</table>
For the settings of 1TAIS1 and 1TAIS0 other than 0,0, the DS1 clock and data outputs of the M13E go to one level for those cases where a received DS3 alarm condition that is not supposed to produce a receive DS1 AIS condition occurs.

The XCK clock (pin 90) is used as the timebase for generating the DS1 AIS clocks.</td></tr>
<tr><td>3
2
1
0</td><td>1LBV3
1LBV2
1LBV1
1LBV0</td><td>Remote Loopback Options: The following table indicates the various ways the M13E can transmit and receive a DS1 remote loopback request in the M13 or C-bit parity operating modes. The specified condition is transmitted for the duration of the loopback request (see register 07H for transmission operation):

<table>
<tr><th>1LBV3</th><th>1LBV2</th><th>1LBV1</th><th>1LBV0</th><th>Loopback Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Third C-bit inverted</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Second C-bit inverted</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>First C-bit inverted</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Undefined - Do not use</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Third C-bit &/+* stuff bit inverted</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Second C-bit &/+* stuff bit inverted</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>First C-bit &/+* stuff bit inverted</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Stuff bit inverted</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Stuff bit = 0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Stuff bit = 1</td></tr>
<tr><td>1</td><td>X</td><td>1</td><td>X</td><td>Undefined - Do not use</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>X</td><td>Undefined - Do not use</td></tr>
</table>
*Note: & = AND in the transmit direction, + = OR in the receive direction.</td></tr>
</table>

Address	Bit	Symbol	Description
21	4 3 2	R3AIS2 R3AIS1 R3AIS0	**Receive DS3 AIS Selection:** A DS3 AIS may be detected in one of six ways. The following table selects the DS3 AIS detection mechanism that is used for providing an R3AIS alarm. Note: The M13E detects all of the AIS selections in parallel.

R3AIS2	R3AIS1	R3AIS0	Receive DS3 AIS Selection
0	0	0	Framed 1010 pattern C-bits = 0 X-bits disregarded
0	0	1	Framed 1010 pattern C-bits = 0 X-bits = 1
0	1	0	Framed 1010 pattern C-bits disregarded X-bits disregarded
0	1	1	Framed 1111 pattern C-bits disregarded X-bits disregarded
1	0	0	Unframed 1010 pattern
1	0	1	Unframed all ones pattern
1	1	X	Undefined - Do not use

The C-Bits = 0 & X bits = 1 conditions are detected as explained for bits 6 & 7 of Address 24H.

R3AIS(2-0) set to 000, 001, & 010 respectively:
The framed 1010 pattern detection consists of looking for the 1010 pattern on a per DS3 subframe basis and monitoring for errors in 4-bit groups of the 1010 pattern. The 1010 pattern is accepted as valid if the M13E receives 4 or less errored 4-bit groups of the 1010 pattern per DS3 subframe and the 1010 pattern starts with a 1 after each DS3 overhead bit.

R3AIS(2-0) set to 011_2:
The framed 1111 pattern detection consists of looking for the 1111 pattern on a per DS3 subframe basis and monitoring for errors in 4-bit groups of the 1111 pattern. The 1111 pattern is accepted as valid if the M13E receives 4 or less errored 4-bit groups of the 1111 pattern per DS3 subframe.

R3AIS(2-0) set to 100_2:
For the unframed 1010 pattern detection the M13E looks for 1010 pattern and declares R3AIS if it receives 2 or less errored 4-bit groups of the 1010 pattern per DS3 subframe. The M13E will exit the R3AIS state if it receives 5 or more errored 4-bit groups of the 1010 pattern per DS3 subframe. If 3 - 4 4-bit groups of the 1010 pattern are errored per DS3 subframe the M13E will exit and reenter the R3AIS state.

R3AIS(2-0) set to 101_2:
The unframed 1111 pattern detection consists of looking for the 1111 pattern and monitoring for errors in 4-bit groups of the 1111 pattern. The 1111 pattern is accepted as valid if the M13E receives 4 or less errored 4-bit groups of the 1111 pattern out of a total of 168 4-bit groups.

Address	Bit	Symbol	Description
21 (cont.)	1 0	T3AIS1 T3AIS0	**Transmit DS3 AIS Selection:** A DS3 AIS may be generated in one of four ways. The following table selects the DS3 AIS generation mechanism: **T3AIS1** / **T3AIS0** / **Transmit DS3 AIS Selection** 0 / 0 / ANSI defined AIS generation Note: A one must be written to bit 0 of register 01H to set the transmitted DS3 X-bits to 1. 0 / 1 / Framed all ones & C-bits set to 1 1 / 0 / Unframed 1010 pattern 1 / 1 / Unframed all ones pattern Note: Set these bits to 0 when transmitting DS3 idle (see T3IDL in register 01H).
22	7-0	C1BZn (n=7-0)	**C1 Bit Zero Counter:** An 8-bit saturating counter that counts the number of C1 bits equal to zero in both the C-bit parity mode and M13 mode. In the M13 mode the contents of this counter should be disregarded. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared when it is read by the microprocessor.
23	7-0	MEn (n=7-0)	**DS3 M-bits in Error Counter:** An 8-bit saturating counter that counts the number of M-bits that are in error since the last read cycle. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared when it is read by the microprocessor.

Address	Bit	Symbol	Description
24	7	AISX=1	**DS3 AIS Detection:** This bit provides a filtered indication of the receive DS3 X-bits equal to one. Two counters are used to implement this filter, a mod 16 counter CXE1 which counts the receive DS3 X-bit pairs=1, and a mod 4 counter CXE0 which counts the receive DS3 X-bit pairs=0. When either counter matures, both counters are reset. The AISX=1 bit becomes latched when the CXE1 counter matures. This bit is used for determining if the X-bits=1 condition is met when R3AIS2=0, R3AIS1=0, and R3AIS0=1 in register 21H (ANSI DS3 defined AIS detection). This is a latched bit, and clears when it is read by the microprocessor. This bit will relatch if the condition that causes this bit to latch is still present.
	6	AISC=0	**DS3 AIS Detection:** This bit provides a filtered indication of the receive DS3 C-bits equal to zero. This bit will be set if the M13E receives 7 contiguous DS3 frames with 30 or less DS3 C-Bits set to 1. This bit is used for determining if the C Bits = 0 condition is met when R3AIS2 = 0 & R3AIS1 = 0 & R3AIS0 = X, where X means don't care. This is a latched bit, and clears when it is read by the microprocessor. This bit will relatch if the condition that causes this bit to latch is still present.
	5	TEST	**Test Bit:** Used for diagnostic purposes.
	4	TEST	**Test Bit:** Used for diagnostic purposes.
	3	TEST	**Test Bit:** Used for diagnostic purposes.
	2	TEST	**Test Bit:** Used for diagnostic purposes.
	1		Not Used.
	0	SEF	**Severely Errored Frame Indication:** A one indicates a severely errored frame has been detected. An SEF is defined as 3 out of 16 F-bits are in error, utilizing a sliding window of 16 bits. This is a latched bit, and clears when it is read by the microprocessor. This bit will relatch if the condition that causes this bit to latch is still present.

INITIALIZATION SEQUENCE

The following table lists the sequence that should be followed for initializing the M13E by writing codes to register 1FH:

Location	Code (Hex)	Comments
1F (R/W)	F0	Resets internal counters and FIFOs.
1F (R/W)	00	Presets internal counters and FIFOs.

SYSTEM CONSIDERATIONS

Careful attention must be paid to power supply decoupling, device layout, and printed circuit board traces. The M13E has separate +5 volt supply (V_{DD}) pins which provide internal circuit isolation. All V_{DD} pins must be tied together to a single +5 volt power supply in order to avoid excessive substrate currents. TranSwitch recommends that good quality, high frequency, low lead inductance 0.1 microfarad ceramic capacitors be used for decoupling and that they be connected in close proximity to the supply input pins on the device. If low frequency noise is present on the +5 volt supply lead, TranSwitch recommends that a 10 microfarad 6.3 volt tantalum capacitor be connected between +5 volts and ground.

A multilayer board that has separate planes for ground and power should be used. Because of the data rate at which the M13E operates, it is important that connections between devices be as short as possible. This is especially true for the DS3 receive and transmit interface connections between the M13E and a line interface device, such as the TranSwitch ART, ARTE or DS3LIM-SN. In addition, the clock and data traces should be the same length.

THROUGHPUT DELAYS

The data transmission paths of the M13E device are subject to throughput delays from input to output, as identified in the following table:

Direction	From	To	Delay (min.)	Delay (typ.)	Delay (max.)	Notes
Receive	DS3DR	DRn	200 ns		800 ns	n = 1-28
Transmit	DTn	DS3DT	400 ns	4100 ns	7800 ns	n = 1-28

TEST ACCESS PORT

Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. The Test Access Port Block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output pins, as illustrated in Figure 17. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a three-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device pins to pass to and from the M13E device's internal logic, as illustrated in Figure 17. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 16.

Boundary Scan Support

The maximum frequency the M13E device will support for boundary scan is 10 MHz. The M13E device performs the following boundary scan test instructions:

- EXTEST (000)
- SAMPLE/PRELOAD (010)
- BYPASS (111)

It should be noted that the Capture - IR State (INSTRUCTION_CAPTURE attribute of BSDL) is "101".

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the M13E device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external M13E input and output leads.

SAMPLE/PRELOAD Test Instruction:

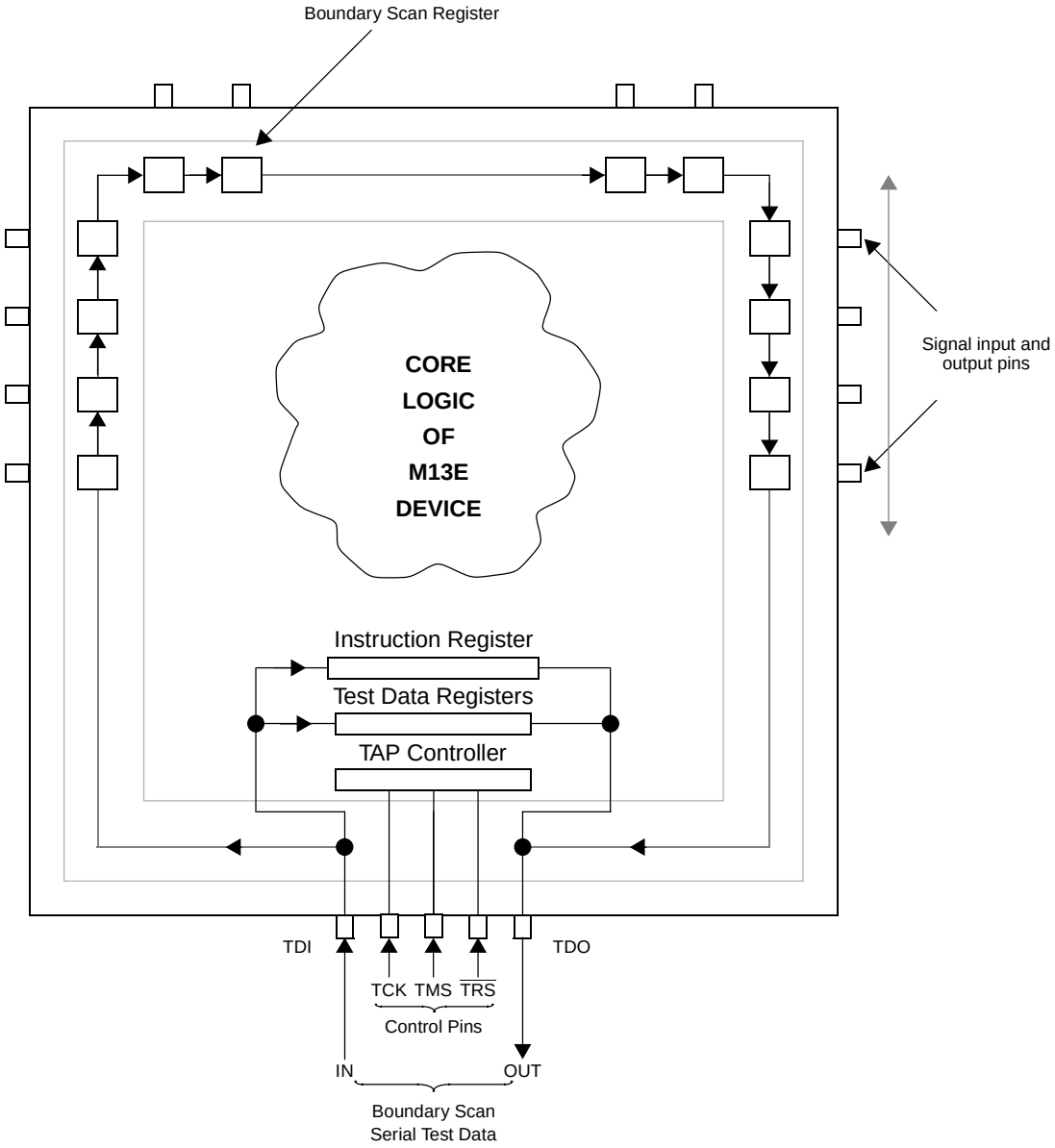
When the SAMPLE/PRELOAD instruction is shifted in, the M13E device remains fully operational. While in this test mode, M13E input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the M13E device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

Boundary Scan Reset

Specific control of the $\overline{TRS}$ pin is required in order to ensure that the boundary scan logic does not interfere with normal device operation. The pin must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the TAP controller. If boundary scan testing is to be performed and the pin is held low, then a pull-down resistor value should be chosen which will allow the tester to drive the pin high.



Note: Pin locations are shown for illustration only, and do not correspond to the physical device pins.

Figure 17. Boundary Scan Schematic

Boundary Scan Chain

There are 163 boundary scan register cells in the boundary scan chain. Scan cell number 0 is defined as the cell nearest the TDO pin and is therefore the first to be shifted out. The last scan cell to be shifted out is number 162. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their function.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
	Input	149	TDI	[SCAN Input]
162	O	6	DR28	Output2
161	O	7	CR28	Output2
160	O	8	DR19	Output2
159	O	9	CR18	Output2
158	O	10	DR18	Output2
157	O	11	CR17	Output2
156	O	12	DR17	Output2
155	O	13	CR16	Output2
154	O	14	DR16	Output2
153	O	15	CR15	Output2
152	O	16	DR15	Output2
151	O	17	CR14	Output2
150	O	19	DR14	Output2
149	O	20	CR13	Output2
148	O	21	DR13	Output2
147	O	22	CR12	Output2
146	O	23	DR12	Output2
145	O	24	CR11	Output2
144	O	25	DR11	Output2
143	O	26	CR10	Output2
142	O	27	DR10	Output2
141	O	28	CR9	Output2
140	O	29	DR9	Output2
139	O	30	CR8	Output2
138	O	31	DR8	Output2
137	O	33	CR7	Output2
136	O	34	DR7	Output2
135	O	35	CR6	Output2

Note: The comments column indicates the functional operation of the corresponding pin.
The signals listed as Output2 can however be tristated.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
134	O	36	DR6	Output2
133	O	37	CR5	Output2
132	O	38	DR5	Output2
131	O	39	CR4	Output2
130	O	40	DR4	Output2
129	O	41	CR3	Output2
128	O	42	DR3	Output2
127	O	43	CR2	Output2
126	O	44	DR2	Output2
125	I	45	A0	Input
124	I	46	A1	Input
123	I	47	A2	Input
122	I	48	A3	Input
121	I	57	A4	Input
120	I	58	A5	Input
119	I	59	A6	Input
118	I	60	A7	Input
117	O	61	CDCCR	Output2
116	--	--	erd	Control. This is not a pin. erd=0 sets A/D(7-0) bus outputs to high impedance state.
115	O	62	CR1	Output2
114	O	63	DR1	Output2
113	O	64	CFMR	Output2
112	O	65	CCKR	Output2
111	O	66	CDR	Output2
110	I	68	DS3CR	Input
109	I	69	DS3DR	Input
108	I	71	$\overline{RD}$	Input
107	I	72	$\overline{WR}$	Input
106	I	73	ALE	Input
105	I	74	$\overline{SEL}$	Input
104	I/O	76	A/D7	Input
103	I/O	76	A/D7	Output3
102	I/O	77	A/D6	Input
101	I/O	77	A/D6	Output3

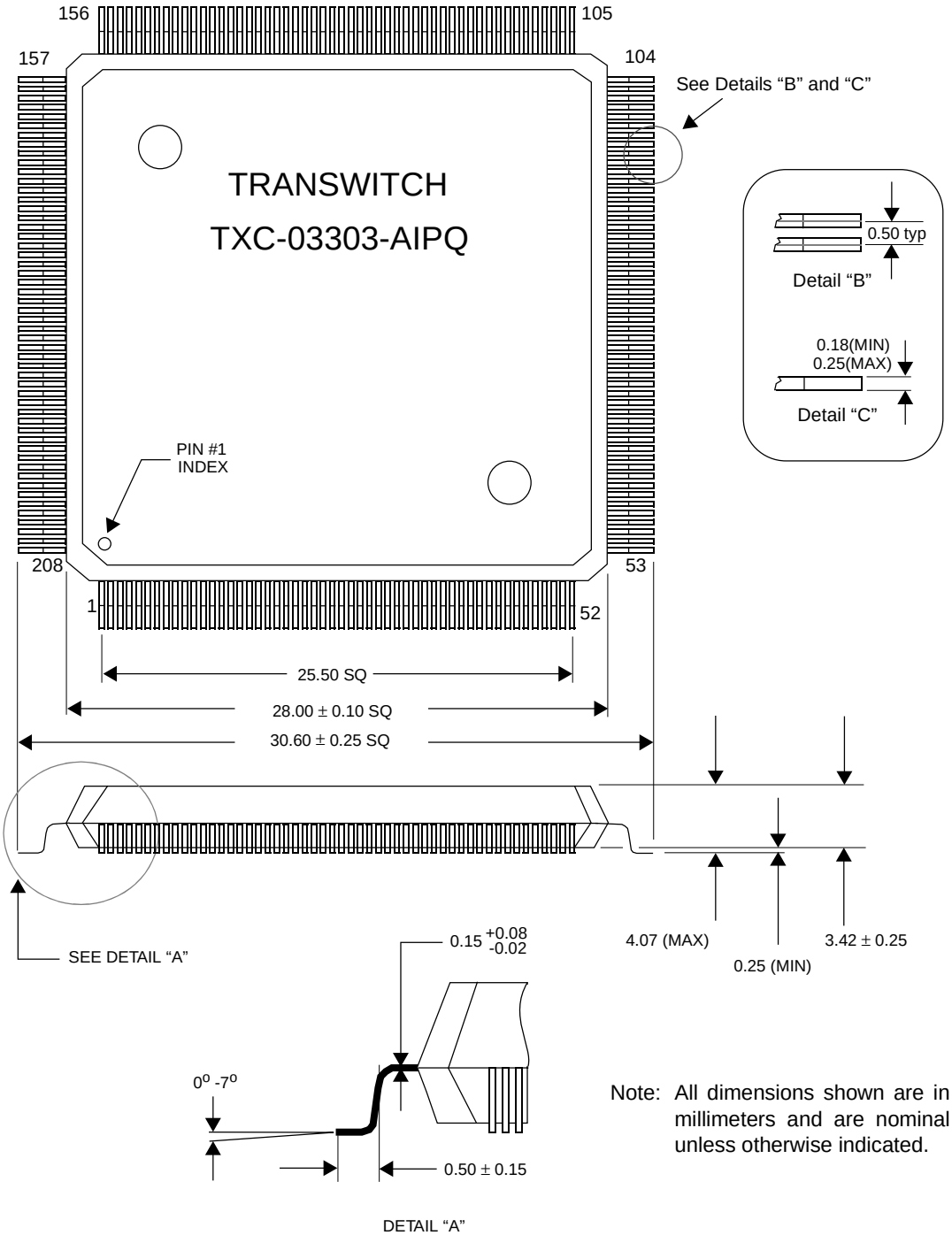
Scan Cell No.	I/O	Pin No.	Symbol	Comments
100	I/O	78	A/D5	Input
99	I/O	78	A/D5	Output3
98	I/O	79	A/D4	Input
97	I/O	79	A/D4	Output3
96	I/O	80	A/D3	Input
95	I/O	80	A/D3	Output3
94	I/O	81	A/D2	Input
93	I/O	81	A/D2	Output3
92	I/O	82	A/D1	Input
91	I/O	82	A/D1	Output3
90	I/O	83	A/D0	Input
89	I/O	83	A/D0	Output3
88	I	85	S7	Input
87	I	86	S6	Input
86	I	87	S5	Input
85	I	89	CDT	Input
84	I	90	XCK	Input
83	O	91	CFMT	Output2
82	O	92	CCKT	Output2
81	O	93	DS3DT	Output2
80	I	95	CT25	Input
79	I	96	DT25	Input
78	I	97	CT26	Input
77	I	98	DT26	Input
76	I	99	CT27	Input
75	I	100	DT27	Input
74	I	108	CT28	Input
73	I	109	DT28	Input
72	I	111	CT21	Input
71	I	112	DT21	Input
70	I	113	CT22	Input
69	I	114	DT22	Input
68	I	115	CT23	Input
67	I	116	DT23	Input
66	I	117	CT24	Input

Scan Cell No.	I/O	Pin No.	Symbol	Comments
65	I	118	DT24	Input
64	I	119	CT17	Input
63	I	120	DT17	Input
62	I	121	CT18	Input
61	I	122	DT18	Input
60	I	123	CT19	Input
59	I	127	DT19	Input
58	I	128	CT20	Input
57	I	129	DT20	Input
56	I	130	CT13	Input
55	I	131	DT13	Input
54	I	132	CT14	Input
53	I	133	DT14	Input
52	I	134	CT15	Input
51	I	135	DT15	Input
50	I	136	CT16	Input
49	I	137	DT16	Input
48	I	139	CT9	Input
47	I	140	DT9	Input
46	I	141	CT10	Input
45	I	142	DT10	Input
44	I	143	CT11	Input
43	I	145	DT11	Input
42	I	147	CT12	Input
41	I	144	$\overline{\text{TEST}}$	Input
40	O	125	DS3CT	Output2
39	I	165	DT12	Input
38	I	167	CT5	Input
37	I	168	DT5	Input
36	I	169	CT6	Input
35	I	170	DT6	Input
34	I	171	CT7	Input
33	I	172	DT7	Input
32	I	173	CT8	Input
31	I	174	DT8	Input

Scan Cell No.	I/O	Pin No.	Symbol	Comments
30	I	175	CT1	Input
29	I	176	DT1	Input
28	I	177	CT2	Input
27	I	178	DT2	Input
26	I	179	CT3	Input
25	I	180	DT3	Input
24	I	181	CT4	Input
23	I	182	DT4	Input
22	O	184	CR19	Output2
21	O	185	DR20	Output2
20	O	186	CR20	Output2
19	O	187	DR21	Output2
18	O	188	CR21	Output2
17	O	189	DR22	Output2
16	O	190	CR22	Output2
15	O	192	DR23	Output2
14	O	193	CR23	Output2
13	O	194	DR24	Output2
12	O	195	CR24	Output2
11	O	196	DR25	Output2
10	O	197	CR25	Output2
9	O	199	DR26	Output2
8	O	201	CR26	Output2
7	O	202	DR27	Output2
6	O	203	CR27	Output2
5	I	161	µP1	Input
4	I	162	µP0	Input
3	I	204	DLEN	Input
2	I	164	$\overline{\text{OUTDIS}}$	Input
1	O	163	RDY/$\overline{\text{DTACK}}$	Output2
0	O	198	CDCCT	Output2
	2-State	150	TDO	[SCAN Output]

PACKAGE INFORMATION

The M13E device is packaged in a 208-pin plastic quad flat package suitable for surface mounting, as illustrated in Figure 18.



Note: All dimensions shown are in millimeters and are nominal unless otherwise indicated.

Figure 18. M13E TXC-03303 208-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number:TXC-03303-AIPQ	208-Pin Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02020 (02021), ART (ARTE) VLSI Device (Advanced DS3/STS-1 Receiver/Transmitter). Performs the receive and transmit line interface functions required for transmission of DS3 (44.736 Mbit/s) or STS-1 (51.840 Mbit/s) signals across a coaxial interface. The ARTE is an extended-feature version of the ART, in a larger package.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). The QT1F-*Plus* is a 4-channel DS1 framer designed for voice and data communications applications. AMI, B8ZS, and NRZ line codes are supported.

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals. Packaged in a 160-pin plastic quad flat package. Does not have as many features as the TXC-03303 M13E (with extended features).

TXC-20153D, DS3/STS-1 Line Interface Module (DS3LIM-SN). Complete and compact analog-to-digital interface that converts B3ZS-encoded DS3 or STS-1 line signals to and from NRZ data and clock signals. Packaged as 2.6 inch x 1.0 inch 50-pin DIP.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated M13E Data Sheet that have significant differences relative to the superseded M13E Data Sheet:

Updated M13E Data Sheet: Edition 4, August 1998

Superseded M13E Data Sheet: Edition 3, June 1996

The page numbers indicated below of this updated data sheet include significant changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1	Clarified External Interface in Features and Description.
2,3	Updated Table of Contents and List of Figures.
5	Removed redundancy of Boundary Scan/Test Access Port leads from Figure 1. Changed last sentence of first paragraph.
6	Changed fourth sentence of last paragraph.
7	Changed last sentence of first paragraph.
14	Change CCKT to CCKR in Name/Function column for CDCCR.
15	Changed Name/Function for Symbol CDT.
16	Changed Name/Function for Symbols TDO and $\overline{TRS}$.
17	Added last six rows, second note and right column to (renamed) Absolute Maximum Ratings and Environmental Limitations table and deleted third and fourth rows. Moved Ambient Operating Temperature row from last table to first table. Renamed last table.
21	Changed Min and Max values for t_{PWH} and t_{PWL} in both tables. Changed Min and Max values for Duty Cycle in last table. Changed Note for Figure 7.
28	Changed Max values in table for $t_{D(1)}$ and $t_{H(2)}$.
30	Added $\overline{TRS}$ to waveform diagrams and last row of table.
31	Added last three sentences to paragraph.
32	Changed fourth sentence of Description for Symbol R3CKF.
34	Changed Description for Symbol INVCK.
36	Changed Description for Remote Loopback and modified Note section at the bottom of the page.
37	Changed first and last paragraphs of Description for Receive Loopback Requests in register 08H. Added last sentence to Description for Receive Loopback Requests in register 09H.

Page Number of Updated Data Sheet	Summary of the Change
38,39	Changed Descriptions for Internal DS1 Idle Channel/Loopback (four places).
40	Changed Description for Symbol C3CLKI.
41	Changed last paragraph of Description for Transmit FEAC Word and added Note.
42	Added Note 2.
43	Added first sentence to Description for DS1 Local Loopback.
44	Changed first paragraph of Description for Remote Loopback Options.
48	Updated second paragraph of System Considerations.
49	Removed last sentence of first paragraph and last paragraph of Bypass Test Instruction section.
50	Added Boundary Scan Reset section.
51-55	Made major changes to Scan Cell table and added note at the bottom of page 51.
57	Updated Related Products list.
58-59	Updated Standard Documentation Sources list.
60	Replaced List of Data Sheet Changes.

- NOTES -

- NOTES -

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