TFRA84J13 Ultraframer DS3/E3/DS2/E2/DS1/E1/DS0

1 Introduction

The last issue of this data sheet was December 17, 2003 - Revision 4. A change history is included in Section 13, Change History, on page 54. Red change bars have been installed on all text, figures, and tables that were added or changed. All changes to the text are highlighted in red. Changes within figures, and the figure title itself, are highlighted in red, if feasible. Formatting or grammatical changes have not been highlighted. Deleted sections, paragraphs, figures, or tables will be specifically mentioned.

The documentation package for the TFRA84J13 Ultraframer DS3/E3/DS2/E2/DS1/E1/DS0 system chip consists of the following documents:

- The Register Description and the System Design Guide. These documens are available on a password-protected website.
- The Ultraframer Product Description and the Ultraframer Hardware Design Guide (this document). These documents are available on the public website shown below (select Mappers/MUXes).

If the reader displays this document using *Acrobat Reader* ®, clicking on any blue text will bring the reader to that reference point. Clicking on the back arrow (Go to previous View) in the toolbar of the *Acrobat Reader* will bring the reader back to the starting point.

To access related documents, including the documents mentioned above, please go to the following public website, or contact your Agere representative (see the last page of this document).

http://www.agere.com/enterprise_metro_access/index.html

This document describes the hardware interfaces to the Agere Systems Inc. TFRA84J13 Ultraframer device. Information relevant to the use of the device in a board design is covered. Pin descriptions, dc electrical characteristics, timing diagrams, ac timing parameters, packaging, and operating conditions are included.

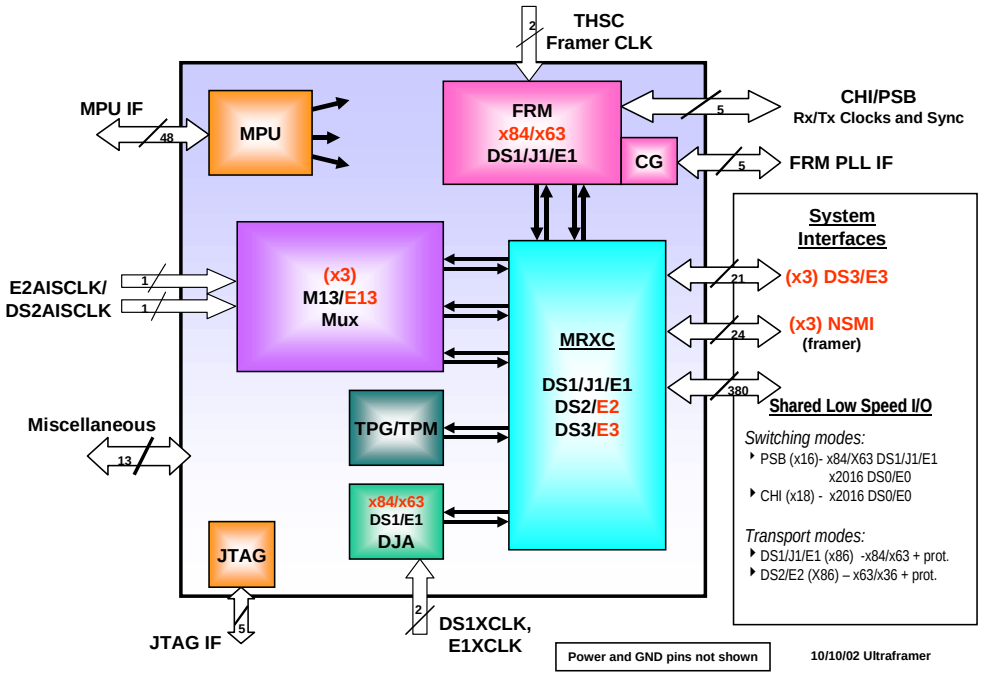

Figure 1-1. Ultraframer Block Diagram and High-Level Interface Definition

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2 Pin Information

2.1 Ball Diagram

The TFRA84J13 Ultraframer is housed in a 909-pin plastic ball grid array. Figure 2-1 shows the ball assignment viewed from the top of the package. The pins are spaced on a 1.0 mm pitch.

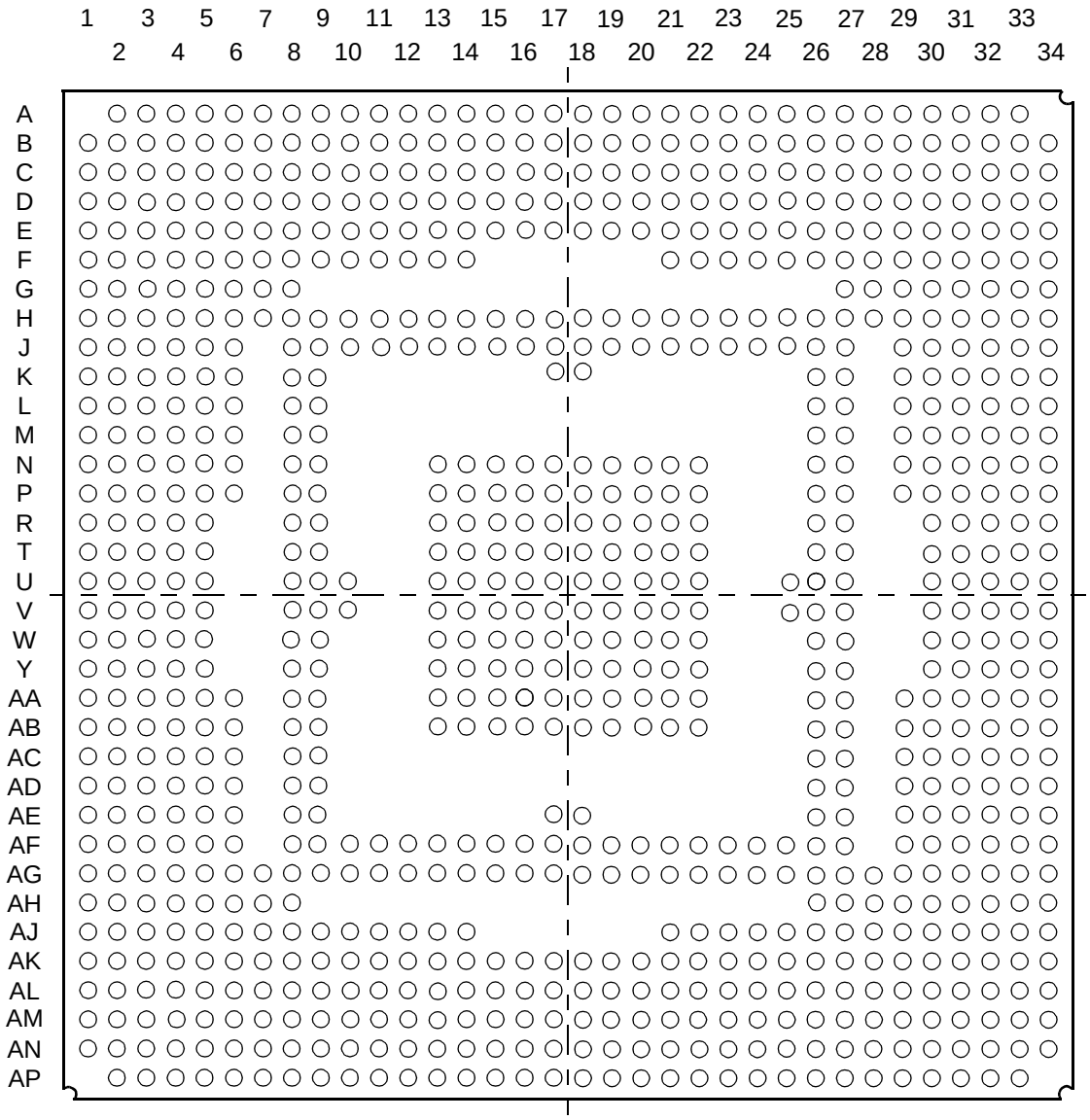


Figure 2-1. Ultraframer Package Diagram (Top View)

2.2 Package Pin Assignments

Table 2-1. Package Pin Assignments

Signal Name	Pin
ADDR[0]	K6
ADDR[1]	H4
ADDR[2]	G3
ADDR[3]	J8
ADDR[4]	J4
ADDR[5]	K5
ADDR[6]	F1
ADDR[7]	G2
ADDR[8]	L6
ADDR[9]	L5
ADDR[10]	H2
ADDR[11]	M6
ADDR[12]	K4
ADDR[13]	L8
ADDR[14]	M5
ADDR[15]	N6
ADDR[16]	J1
ADDR[17]	L3
ADDR[18]	M4
ADDR[19]	P8
ADDR[20]	N5
ADSN	F3
NC	Y1
NC	AM13
CG_PLLCLKOUT	AF26
CLKIN_PLL	AF27
CSN	G7
NC	AF8
NC	AG10
CTAPTH	AG9
NC	AG14
DATA[0]	K1
DATA[1]	L2
DATA[2]	U2
DATA[3]	N4
DATA[4]	R8
DATA[5]	M2
DATA[6]	T5
DATA[7]	M1
DATA[8]	R5
DATA[9]	U5
DATA[10]	P4
DATA[11]	N2
DATA[12]	R4
DATA[13]	T4

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
DATA[14]	U9
DATA[15]	P1
DS1XCLK	AP21
DS2AISCLK	V8
DS3DATAINCLK[1]	AB1
DS3DATAINCLK[2]	V4
DS3DATAINCLK[3]	V3
NC	AE1
NC	AF1
NC	AB4
DS3DATAOUTCLK[1]	AB5
DS3DATAOUTCLK[2]	AB8
DS3DATAOUTCLK[3]	AC5
NC	AD5
NC	AE5
NC	AG4
DS3NEGDATAIN[1]	V1
DS3NEGDATAIN[2]	AC1
DS3NEGDATAIN[3]	Y4
NC	AC2
NC	Y5
NC	AA5
DS3NEGDATAOUT[1]	AC3
DS3NEGDATAOUT[2]	AC4
DS3NEGDATAOUT[3]	AJ1
NC	AL1
NC	AG3
NC	AJ2
DS3POSDATAIN[1]	W3
DS3POSDATAIN[2]	AB2
DS3POSDATAIN[3]	AD1
NC	V5
NC	W8
NC	W5
DS3POSDATAOUT[1]	V2
DS3POSDATAOUT[2]	AA6
DS3POSDATAOUT[3]	AH1
NC	AK1
NC	AG2
NC	AF4
DS3RXCLKOUT[1]	AD2
DS3RXCLKOUT[2]	AD3
DS3RXCLKOUT[3]	AB6
NC	AC8
NC	AD6

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
NC	AE8
DSN	J5
DTN	T3
E1XCLK	AM18
E2AISCLK	AA1
NC	H18
NC	AL14
NC	AP15
NC	AP16
HP_INTN	U8
IC3STATEN	AL20
IDDQ	AL21
LINERXCLK[1]	A18
LINERXCLK[2]	C17
LINERXCLK[3]	E16
LINERXCLK[4]	C16
LINERXCLK[5]	B16
LINERXCLK[6]	A15
LINERXCLK[7]	A14
LINERXCLK[8]	C13
LINERXCLK[9]	B13
LINERXCLK[10]	D12
LINERXCLK[11]	B12
LINERXCLK[12]	D11
LINERXCLK[13]	B11
LINERXCLK[14]	E12
LINERXCLK[15]	D10
LINERXCLK[16]	H12
LINERXCLK[17]	D9
LINERXCLK[18]	C8
LINERXCLK[19]	H11
LINERXCLK[20]	B7
LINERXCLK[21]	E9
LINERXCLK[22]	E10
LINERXCLK[23]	D7
LINERXCLK[24]	E8
LINERXCLK[25]	F9
LINERXCLK[26]	E7
LINERXCLK[27]	D6
LINERXCLK[28]	G8
LINERXCLK[29]	B4
LINERXCLK[30]	F7
LINERXCLK[31]	J9
LINERXCLK[32]	F4
LINERXCLK[33]	C1
LINERXCLK[34]	H9
LINERXCLK[35]	E5

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
LINERXCLK[36]	F6
LINERXCLK[37]	A10
LINERXCLK[38]	A12
LINERXCLK[39]	H14
LINERXCLK[40]	D14
LINERXCLK[41]	A16
LINERXCLK[42]	E17
LINERXCLK[43]	B18
LINERXCLK[44]	D19
LINERXCLK[45]	H20
LINERXCLK[46]	D21
LINERXCLK[47]	B24
LINERXCLK[48]	F22
LINERXCLK[49]	B28
LINERXCLK[50]	A29
LINERXCLK[51]	H24
LINERXCLK[52]	A32
LINERXCLK[53]	D29
LINERXCLK[54]	D30
LINERXCLK[55]	H26
LINERXCLK[56]	E30
LINERXCLK[57]	F29
LINERXCLK[58]	L30
LINERXCLK[59]	M27
LINERXCLK[60]	M30
LINERXCLK[61]	N29
LINERXCLK[62]	M31
LINERXCLK[63]	N30
LINERXCLK[64]	L33
LINERXCLK[65]	N31
LINERXCLK[66]	P29
LINERXCLK[67]	M34
LINERXCLK[68]	N34
LINERXCLK[69]	T27
LINERXCLK[70]	T33
LINERXCLK[71]	U33
LINERXCLK[72]	V30
LINERXCLK[73]	W34
LINERXCLK[74]	W31
LINERXCLK[75]	AA34
LINERXCLK[76]	Y30
LINERXCLK[77]	AC33
LINERXCLK[78]	AH3
LINERXCLK[79]	AH2
LINERXCLK[80]	AE4
LINERXCLK[81]	AD4
LINERXCLK[82]	Y8

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
LINERXCLK[83]	AA4
LINERXCLK[84]	W4
LINERXCLK[85]	U1
LINERXCLK[86]	T2
LINERXDATA[1]	E18
LINERXDATA[2]	D17
LINERXDATA[3]	B17
LINERXDATA[4]	D16
LINERXDATA[5]	H16
LINERXDATA[6]	E15
LINERXDATA[7]	E14
LINERXDATA[8]	D13
LINERXDATA[9]	F14
LINERXDATA[10]	A13
LINERXDATA[11]	E13
LINERXDATA[12]	F13
LINERXDATA[13]	H13
LINERXDATA[14]	A11
LINERXDATA[15]	A9
LINERXDATA[16]	A8
LINERXDATA[17]	B8
LINERXDATA[18]	E11
LINERXDATA[19]	A7
LINERXDATA[20]	D8
LINERXDATA[21]	F11
LINERXDATA[22]	C7
LINERXDATA[23]	A6
LINERXDATA[24]	F10
LINERXDATA[25]	B6
LINERXDATA[26]	C6
LINERXDATA[27]	F8
LINERXDATA[28]	A5
LINERXDATA[29]	A4
LINERXDATA[30]	E6
LINERXDATA[31]	H6
LINERXDATA[32]	G5
LINERXDATA[33]	H8
LINERXDATA[34]	G6
LINERXDATA[35]	F5
LINERXDATA[36]	H10
LINERXDATA[37]	F12
LINERXDATA[38]	C11
LINERXDATA[39]	C12
LINERXDATA[40]	H15
LINERXDATA[41]	D15
LINERXDATA[42]	A17
LINERXDATA[43]	H17

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
LINERXDATA[44]	C18
LINERXDATA[45]	A22
LINERXDATA[46]	E21
LINERXDATA[47]	D22
LINERXDATA[48]	A26
LINERXDATA[49]	H23
LINERXDATA[50]	D25
LINERXDATA[51]	A30
LINERXDATA[52]	F25
LINERXDATA[53]	A33
LINERXDATA[54]	G27
LINERXDATA[55]	E29
LINERXDATA[56]	F28
LINERXDATA[57]	G28
LINERXDATA[58]	L29
LINERXDATA[59]	L31
LINERXDATA[60]	M29
LINERXDATA[61]	N27
LINERXDATA[62]	L32
LINERXDATA[63]	K34
LINERXDATA[64]	P30
LINERXDATA[65]	M32
LINERXDATA[66]	L34
LINERXDATA[67]	M33
LINERXDATA[68]	R27
LINERXDATA[69]	P34
LINERXDATA[70]	T32
LINERXDATA[71]	U30
LINERXDATA[72]	U34
LINERXDATA[73]	V32
LINERXDATA[74]	V31
LINERXDATA[75]	W30
LINERXDATA[76]	AB34
LINERXDATA[77]	AC34
LINERXDATA[78]	AD8
LINERXDATA[79]	AE6
LINERXDATA[80]	AC6
LINERXDATA[81]	AA8
LINERXDATA[82]	AG1
LINERXDATA[83]	AB3
LINERXDATA[84]	V9
LINERXDATa[85]	W2
LINERXDATA[86]	T1
LINETXCLK[1]	K31
LINETXCLK[2]	J34
LINETXCLK[3]	H34
LINETXCLK[4]	J30

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
LINETXCLK[5]	H32
LINETXCLK[6]	H31
LINETXCLK[7]	J29
LINETXCLK[8]	G31
LINETXCLK[9]	G30
LINETXCLK[10]	H27
LINETXCLK[11]	C31
LINETXCLK[12]	J26
LINETXCLK[13]	F27
LINETXCLK[14]	F26
LINETXCLK[15]	D28
LINETXCLK[16]	C29
LINETXCLK[17]	A31
LINETXCLK[18]	E25
LINETXCLK[19]	C28
LINETXCLK[20]	B29
LINETXCLK[21]	C27
LINETXCLK[22]	D24
LINETXCLK[23]	A28
LINETXCLK[24]	A27
LINETXCLK[25]	C24
LINETXCLK[26]	A25
LINETXCLK[27]	C23
LINETXCLK[28]	A24
LINETXCLK[29]	H21
LINETXCLK[30]	A23
LINETXCLK[31]	AA31
LINETXCLK[32]	AA27
LINETXCLK[33]	AD33
LINETXCLK[34]	AB31
LINETXCLK[35]	AB29
LINETXCLK[36]	AD32
LINETXCLK[37]	AC31
LINETXCLK[38]	AB27
LINETXCLK[39]	AG34
LINETXCLK[40]	AD31
LINETXCLK[41]	AD29
LINETXCLK[42]	AD30
LINETXCLK[43]	AG32
LINETXCLK[44]	AE29
LINETXCLK[45]	AE27
LINETXCLK[46]	AJ28
LINETXCLK[47]	AK29
LINETXCLK[48]	AH28
LINETXCLK[49]	AH27
LINETXCLK[50]	AM31
LINETXCLK[51]	AL28

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
LINETXCLK[52]	AL26
LINETXCLK[53]	AM27
LINETXCLK[54]	AG22
LINETXCLK[55]	AL30
LINETXCLK[56]	AG20
LINETXCLK[57]	AG24
LINETXCLK[58]	AG25
LINETXCLK[59]	AK19
LINETXCLK[60]	AL19
LINETXCLK[61]	AF17
LINETXCLK[62]	AJ25
LINETXCLK[63]	AH7
LINETXCLK[64]	AN18
LINETXCLK[65]	AJ12
LINETXCLK[66]	AK12
LINETXCLK[67]	AN16
LINETXCLK[68]	AK14
LINETXCLK[69]	AL4
LINETXCLK[70]	AH6
LINETXCLK[71]	AL3
LINETXCLK[72]	AF9
LINETXCLK[73]	AJ4
LINETXCLK[74]	AH4
LINETXCLK[75]	AG5
LINETXCLK[76]	AF5
LINETXCLK[77]	U3
LINETXCLK[78]	N3
LINETXCLK[79]	P5
LINETXCLK[80]	P6
LINETXCLK[81]	H1
LINETXCLK[82]	G1
LINETXCLK[83]	K8
LINETXCLK[84]	F2
LINETXCLK[85]	D1
LINETXCLK[86]	H7
LINETXDATA[1]	L27
LINETXDATA[2]	K30
LINETXDATA[3]	K29
LINETXDATA[4]	J31
LINETXDATA[5]	H33
LINETXDATA[6]	K27
LINETXDATA[7]	H30
LINETXDATA[8]	H29
LINETXDATA[9]	J27
LINETXDATA[10]	G29
LINETXDATA[11]	H28
LINETXDATA[12]	B32

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
LINETXDATA[13]	E28
LINETXDATA[14]	B31
LINETXDATA[15]	E27
LINETXDATA[16]	H25
LINETXDATA[17]	E26
LINETXDATA[18]	D27
LINETXDATA[19]	D26
LINETXDATA[20]	F24
LINETXDATA[21]	E24
LINETXDATA[22]	F23
LINETXDATA[23]	B27
LINETXDATA[24]	E23
LINETXDATA[25]	D23
LINETXDATA[26]	H22
LINETXDATA[27]	E22
LINETXDATA[28]	F21
LINETXDATA[29]	B23
LINETXDATA[30]	C22
LINETXDATA[31]	AA29
LINETXDATA[32]	AB32
LINETXDATA[33]	AD34
LINETXDATA[34]	AA30
LINETXDATA[35]	AC32
LINETXDATA[36]	AE34
LINETXDATA[37]	AB30
LINETXDATA[38]	AF34
LINETXDATA[39]	AC30
LINETXDATA[40]	AC29
LINETXDATA[41]	AG33
LINETXDATA[42]	AE31
LINETXDATA[43]	AC27
LINETXDATA[44]	AE30
LINETXDATA[45]	AJ33
LINETXDATA[46]	AL31
LINETXDATA[47]	AM33
LINETXDATA[48]	AK30
LINETXDATA[49]	AJ29
LINETXDATA[50]	AM32
LINETXDATA[51]	AN33
LINETXDATA[52]	AK25
LINETXDATA[53]	AK24
LINETXDATA[54]	AK23
LINETXDATA[55]	AP28
LINETXDATA[56]	AP26
LINETXDATA[57]	AP25
LINETXDATA[58]	AN24
LINETXDATA[59]	AM22

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
LINETXDATA[60]	AG18
LINETXDATA[61]	AM19
LINETXDATA[62]	AL18
LINETXDATA[63]	AN19
LINETXDATA[64]	AK11
LINETXDATA[65]	AK16
LINETXDATA[66]	AP17
LINETXDATA[67]	AL15
LINETXDATA[68]	AG8
LINETXDATA[69]	AK5
LINETXDATA[70]	AJ5
LINETXDATA[71]	AK4
LINETXDATA[72]	AH5
LINETXDATA[73]	AG6
LINETXDATA[74]	AL2
LINETXDATA[75]	AF6
LINETXDATA[76]	AJ3
LINETXDATA[77]	N1
LINETXDATA[78]	T8
LINETXDATA[79]	L1
LINETXDATA[80]	M3
LINETXDATA[81]	M8
LINETXDATA[82]	L4
LINETXDATA[83]	H3
LINETXDATA[84]	N8
LINETXDATA[85]	E1
LINETXDATA[86]	H5
NC	B22
NC	A21
NC	D20
NC	H19
NC	E20
NC	A20
NC	AG27
LP_INTN	W1
MODE0_PLL	AJ31
MODE1_PLL	AG30
MODE2_PLL	AK31
MPCLK	G4
MPMODE	D2
CHIRXDATA[17]	N32
CHIRXDATA[14]	N33
CHIRXDATA[18]	P27
CHIRXDATA[16]	P31
CHIRXDATA[15]	R30
CHIRXDATA[13]	R31
CHIRXDATA[10]	R34

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
CHIRXDATA[12]	T30
CHIRXDATA[11]	T31
CHIRXDATA[7]	T34
CHIRXDATA[6]	U27
CHIRXDATA[9]	U31
CHIRXDATA[8]	U32
CHIRXDATA[3]	V27
CHIRXDATA[4]	V33
CHIRXDATA[5]	V34
CHIRXGCLK	W27
CHIRXDATA[1]	W32
CHIRXDATA[2]	W33
CHITXGCLK	Y27
CHIRXGTCLK	Y31
CHIRXGFS	Y34
CHITXGFS	AB33
CHITXDATA[16]	AD27
CHITXDATA[11]	AF29
CHITXDATA[13]	AF30
CHITXDATA[15]	AF31
CHITXDATA[5]	AG28
CHITXDATA[8]	AG29
CHITXDATA[12]	AG31
CHITXDATA[6]	AH29
CHITXDATA[10]	AH32
CHITXDATA[17]	AH33
CHITXDATA[18]	AH34
CHITXDATA[7]	AJ30
CHITXDATA[9]	AJ32
CHITXDATA[14]	AJ34
CHITXDATA[1]	AK26
CHITXDATA[3]	AK27
CHITXDATA[4]	AL29
CHITXDATA[2]	AN32
NSMIRXCLK[1]	AJ22
NSMIRXCLK[2]	AK28
NSMIRXCLK[3]	AG21
NSMIRXDATA[1]	AM24
NSMIRXDATA[2]	AP27
NSMIRXDATA[3]	AN27
NSMIRXSYNC[1]	AL22
NSMIRXSYNC[2]	AL23
NSMIRXSYNC[3]	AP29
NSMITXCLK[1]	AG23
NSMITXCLK[2]	AP31
NSMITXCLK[3]	AN31
NSMITXDATA[1]	AN28

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
NSMITXDATA[2]	AL25
NSMITXDATA[3]	AP33
NSMITXSYNC[1]	AP30
NSMITXSYNC[2]	AP32
NSMITXSYNC[3]	AL27
PAR[0]	R1
PAR[1]	U4
PMRST	AJ24
REF10	AK6
REF14	AJ6
RESHI	AL5
RESLO	AL6
NC	AN1
NC	AM1
NC	AM3
NC	AM2
NC	AP22
NC	AJ14
NC	AN10
NC	AM10
NC	AP12
NC	AP10
NC	AM9
NC	AP11
NC	AM17
NC	AG17
NC	AP19
NC	AM8
NC	AM7
NC	AP6
NC	AN6
RSTN	AK18
NC	AM16
NC	AK15
NC	AN17
RWN	J6
RXDATAEN[1]	AK21
RXDATAEN[2]	AK22
RXDATAEN[3]	AL24
SCAN_EN	AJ23
SCANMODE	AK20
SCK1	AP24
SCK2	AM23
TCK	AN22
TDI	AP23
TDO	AJ21
THSCN	AP4

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
NC	AP2
NC	AN2
THSCP	AN4
NC	AM6
NC	AM5
NC	AL13
NC	AK13
NC	AM11
NC	AN13
NC	AP14
NC	AN11
NC	AN12
NC	AP13
TMS	AN23
NC	AL17
NC	AK17
NC	AP20
NC	AP8
NC	AN8
NC	AN9
NC	AP9
TRST	AG26
NC	AJ13
NC	AG15
NC	AG7
NC	AH8
NC	AL16
NC	AP18
TXDATAEN[1]	AN29
TXDATAEN[2]	AM28
TXDATAEN[3]	AM29
V_{DD15}	J10
V_{DD15}	J13
V_{DD15}	J17
V_{DD15}	J18
V_{DD15}	J22
V_{DD15}	J25
V_{DD15}	K9
V_{DD15}	K17
V_{DD15}	K18
V_{DD15}	K26
V_{DD15}	N9
V_{DD15}	N13
V_{DD15}	N14
V_{DD15}	N15
V_{DD15}	N16
V_{DD15}	N17

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
V_{DD15}	N18
V_{DD15}	N19
V_{DD15}	N20
V_{DD15}	N21
V_{DD15}	N22
V_{DD15}	N26
V_{DD15}	P13
V_{DD15}	P22
V_{DD15}	R13
V_{DD15}	R22
V_{DD15}	T13
V_{DD15}	T22
V_{DD15}	U10
V_{DD15}	U13
V_{DD15}	U22
V_{DD15}	U25
V_{DD15}	U26
V_{DD15}	V10
V_{DD15}	V13
V_{DD15}	V22
V_{DD15}	V25
V_{DD15}	V26
V_{DD15}	W13
V_{DD15}	W22
V_{DD15}	Y13
V_{DD15}	Y22
V_{DD15}	AA9
V_{DD15}	AA13
V_{DD15}	AA22
V_{DD15}	AA26
V_{DD15}	AB9
V_{DD15}	AB13
V_{DD15}	AB14
V_{DD15}	AB15
V_{DD15}	AB16
V_{DD15}	AB17
V_{DD15}	AB18
V_{DD15}	AB19
V_{DD15}	AB20
V_{DD15}	AB21
V_{DD15}	AB22
V_{DD15}	AB26
V_{DD15}	AE9
V_{DD15}	AE17
V_{DD15}	AE18
V_{DD15}	AE26
V_{DD15}	AF10

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
VDD15	AF13
VDD15	AF14
VDD15	AF18
VDD15	AF21
VDD15	AF22
VDD15	AF25
VDD15	AH26
VDD15	AJ26
VDD15	AJ27
VDD15	J14
VDD15	J21
VDD15	P9
VDD15	P26
NC	AG12
NC	AL11
NC	C19
NC	B19
NC	AM12
VDD33	A2
VDD33	A3
VDD33	B1
VDD33	B3
VDD33	B5
VDD33	B9
VDD33	B10
VDD33	B14
VDD33	B15
VDD33	B20
VDD33	B21
VDD33	B25
VDD33	B26
VDD33	B30
VDD33	B33
VDD33	B34
VDD33	C2
VDD33	C4
VDD33	C32
VDD33	C33
VDD33	C34
VDD33	D3
VDD33	D5
VDD33	D32
VDD33	D33
VDD33	D34
VDD33	E2
VDD33	E4
VDD33	E33

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
VDD33	E34
VDD33	J2
VDD33	J11
VDD33	J12
VDD33	J15
VDD33	J16
VDD33	J19
VDD33	J20
VDD33	J23
VDD33	J24
VDD33	J33
VDD33	K2
VDD33	K33
VDD33	L9
VDD33	L26
VDD33	M9
VDD33	M26
VDD33	P2
VDD33	P33
VDD33	R2
VDD33	R9
VDD33	R26
VDD33	R33
VDD33	T9
VDD33	T26
VDD33	W9
VDD33	W26
VDD33	Y2
VDD33	Y9
VDD33	Y26
VDD33	Y33
VDD33	AA2
VDD33	AA33
VDD33	AC9
VDD33	AC26
VDD33	AD9
VDD33	AD26
VDD33	AE2
VDD33	AE33
VDD33	AF2
VDD33	AF11
VDD33	AF12
VDD33	AF15
VDD33	AF16
VDD33	AF19
VDD33	AF20
VDD33	AF23

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
VDD33	AF24
VDD33	AF33
VDD33	AK2
VDD33	AK33
VDD33	AK34
VDD33	AL33
VDD33	AL34
VDD33	AM34
VDD33	AN14
VDD33	AN15
VDD33	AN20
VDD33	AN21
VDD33	AN25
VDD33	AN26
VDD33	AN30
VDD33	AN34
VDD33A_SFPLL	AH30
VSS	B2
VSS	C3
VSS	C5
VSS	C9
VSS	C10
VSS	C14
VSS	C15
VSS	C20
VSS	C21
VSS	C25
VSS	C26
VSS	C30
VSS	D4
VSS	D31
VSS	E3
VSS	E31
VSS	E32
VSS	F30
VSS	F31
VSS	F32
VSS	F33
VSS	F34
VSS	G32
VSS	G33
VSS	G34
VSS	J3
VSS	J32
VSS	K3
VSS	K32
VSS	P3

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
VSS	P14
VSS	P15
VSS	P16
VSS	P17
VSS	P18
VSS	P19
VSS	P20
VSS	P21
VSS	P32
VSS	R3
VSS	R14
VSS	R15
VSS	R16
VSS	R17
VSS	R18
VSS	R19
VSS	R20
VSS	R21
VSS	R32
VSS	T14
VSS	T15
VSS	T16
VSS	T17
VSS	T18
VSS	T19
VSS	T20
VSS	T21
VSS	U14
VSS	U15
VSS	U16
VSS	U17
VSS	U18
VSS	U19
VSS	U20
VSS	U21
VSS	V14
VSS	V15
VSS	V16
VSS	V17
VSS	V18
VSS	V19
VSS	V20
VSS	V21
VSS	W14
VSS	W15
VSS	W16
VSS	W17

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
VSS	W18
VSS	W19
VSS	W20
VSS	W21
VSS	Y3
VSS	Y14
VSS	Y15
VSS	Y16
VSS	Y17
VSS	Y18
VSS	Y19
VSS	Y20
VSS	Y21
VSS	Y32
VSS	AA3
VSS	AA14
VSS	AA15
VSS	AA16
VSS	AA17
VSS	AA18
VSS	AA19
VSS	AA20
VSS	AA21
VSS	AA32
VSS	AE3
VSS	AE32
VSS	AF3
VSS	AF32
VSS	AG16
VSS	AG19
VSS	AJ7
VSS	AJ8
VSS	AJ9

Table 2-1. Package Pin Assignments (continued)

Signal Name	Pin
VSS	AJ10
VSS	AJ11
VSS	AK3
VSS	AK7
VSS	AK8
VSS	AK9
VSS	AK10
VSS	AK32
VSS	AL7
VSS	AL8
VSS	AL9
VSS	AL10
VSS	AL32
VSS	AM4
VSS	AM14
VSS	AM15
VSS	AM20
VSS	AM21
VSS	AM25
VSS	AM26
VSS	AM30
VSS	AN3
VSS	AN5
VSS	AN7
VSS	AP3
VSS	AP5
VSS	AP7
NC	AG11
NC	AG13
NC	D18
NC	A19
VSSA_SFPLL	AH31
NC	AL12
NC	E19

2.3 Pin Assignment Matrix

Table 2-2. Pin Matrix

	1	2	3	4	5	6	7	8	9	10	11	12
A	—	VDD33	VDD33	LINERXDATA[29]	LINERXDATA[28]	LINERXDATA[23]	LINERXDATA[19]	LINERXDATA[16]	LINERXDATA[15]	LINERXCLK [37]	LINERXDATA [14]	LINERXCLK [38]
B	VDD33	VSS	VDD33	LINERXCLK[29]	VDD33	LINERXDATA[25]	LINERXCLK[20]	LINERXDATA[17]	VDD33	VDD33	LINERXCLK[13]	LINERXCLK[11]
C	LINERXCLK[33]	VDD33	VSS	VDD33	VSS	LINERXDATA[26]	LINERXDATA[22]	LINERXCLK[18]	VSS	VSS	LINERXDATA[38]	LINERXDATA[39]
D	LINETXCLK[85]	MPMODE	VDD33	VSS	VDD33	LINERXCLK[27]	LINERXCLK[23]	LINERXDATA[20]	LINERXCLK[17]	LINERXCLK[15]	LINERXCLK[12]	LINERXCLK[10]
E	LINETXDATA[85]	VDD33	VSS	VDD33	LINERXCLK[35]	LINERXDATA[30]	LINERXCLK[26]	LINERXCLK[24]	LINERXCLK[21]	LINERXCLK[22]	LINERXDATA[18]	LINERXCLK[14]
F	ADDR[6]	LINETXCLK[84]	ADSN	LINERXCLK[32]	LINERXDATA[35]	LINERXCLK[36]	LINERXCLK[30]	LINERXDATA[27]	LINERXCLK[25]	LINERXDATA[24]	LINERXDATA[21]	LINERXDATA[37]
G	LINETXCLK[82]	ADDR[7]	ADDR[2]	MPCLK	LINERXDATA[32]	LINERXDATA[34]	CSN	LINERXCLK[28]	—	—	—	—
H	LINETXCLK[81]	ADDR[10]	LINETXDATA[83]	ADDR[1]	LINETXDATA[86]	LINERXDATA[31]	LINETXCLK[86]	LINERXDATA[33]	LINERXCLK[34]	LINERXDATA[36]	LINERXCLK[19]	LINERXCLK[16]
J	ADDR[16]	VDD33	VSS	ADDR[4]	DSN	RWN	—	ADDR[3]	LINERXCLK[31]	VDD15	VDD33	VDD33
K	DATA[0]	VDD33	VSS	ADDR[12]	ADDR[5]	ADDR[0]	—	LINETXCLK[83]	VDD15	—	—	—
L	LINETXDATA[79]	DATA[1]	ADDR[17]	LINETXDATA[82]	ADDR[9]	ADDR[8]	—	ADDR[13]	VDD33	—	—	—
M	DATA[7]	DATA[5]	LINETXDATA[80]	ADDR[18]	ADDR[14]	ADDR[11]	—	LINETXDATA[81]	VDD33	—	—	—
N	LINETXDATA[77]	DATA[11]	LINETXCLK[78]	DATA[3]	ADDR[20]	ADDR[15]	—	LINETXDATA[84]	VDD15	—	—	—
P	DATA[15]	VDD33	VSS	DATA[10]	LINETXCLK[79]	LINETXCLK[80]	—	ADDR[19]	VDD15	—	—	—
R	PAR[0]	VDD33	VSS	DATA[12]	DATA[8]	—	—	DATA[4]	VDD33	—	—	—
T	LINERXDATA[86]	LINERXCLK[86]	DTN	DATA[13]	DATA[6]	—	—	LINETXDATA[78]	VDD33	—	—	—
U	LINERXCLK[85]	DATA[2]	LINETXCLK[77]	PAR[1]	DATA[9]	—	—	HP_INTN	DATA[14]	VDD15	—	—
V	DS3NEGDATAIN[1]	DS3POSDATAOUT[1]	DS3DATAINCLK[3]	DS3DATAINCLK[2]	NC	—	—	DS2AISCLK	LINERXDATA[84]	VDD15	—	—
W	LP_INTN	LINERXDATA[85]	DS3POSDATAIN[1]	LINERXCLK[84]	NC	—	—	NC	VDD33	—	—	—
Y	NC	VDD33	VSS	DS3NEGDATAIN[3]	NC	—	—	LINERXCLK[82]	VDD33	—	—	—
AA	E2AISCLK	VDD33	VSS	LINERXCLK[83]	NC	DS3POSDATAOUT[2]	—	LINERXDATA[81]	VDD15	—	—	—
AB	DS3DATAINCLK[1]	DS3POSDATAIN[2]	LINERXDATA[83]	NC	DS3DATAOUTCLK[1]	DS3RXCLKOUT[3]	—	DS3DATAOUTCLK[2]	VDD15	—	—	—
AC	DS3NEGDATAIN[2]	NC	DS3NEGDATAOUT[1]	DS3NEGDATAOUT[2]	DS3DATAOUTCLK[3]	LINERXDATA[80]	—	NC	VDD33	—	—	—
AD	DS3POSDATAIN[3]	DS3RXCLKOUT[1]	DS3RXCLKOUT[2]	LINERXCLK[81]	NC	NC	—	LINERXDATA[78]	VDD33	—	—	—
AE	NC	VDD33	VSS	LINERXCLK[80]	NC	LINERXDATA[79]	—	NC	VDD15	—	—	—
AF	NC	VDD33	VSS	NC	LINETXCLK[76]	LINETXDATA[75]	—	NC	LINETXCLK[72]	VDD15	VDD33	VDD33
AG	LINERXDATA[82]	NC	NC	NC	LINETXCLK[75]	LINETXDATA[73]	NC	LINETXDATA[68]	CTAPTH	NC	NC	NC
AH	DS3POSDATAOUT[3]	LINERXCLK[79]	LINERXCLK[78]	LINETXCLK[74]	LINETXDATA[72]	LINETXCLK[70]	LINETXCLK[63]	NC	—	—	—	—
AJ	DS3NEGDATAOUT[3]	NC	LINETXDATA[76]	LINETXCLK[73]	LINETXDATA[70]	REF14	VSS	VSS	VSS	VSS	VSS	LINETXCLK[65]
AK	NC	VDD33	VSS	LINETXDATA[71]	LINETXDATA[69]	REF10	VSS	VSS	VSS	VSS	LINETXDATA[64]	LINETXCLK[66]
AL	NC	LINETXDATA[74]	LINETXCLK[71]	LINETXCLK[69]	RESHI	RESLO	VSS	VSS	VSS	VSS	NC	NC
AM	NC	NC	NC	VSS	NC	NC	NC	NC	NC	NC	NC	NC
AN	NC	NC	VSS	THSCP	VSS	NC	VSS	NC	NC	NC	NC	NC
AP	—	NC	VSS	THSCN	VSS	RPSDN	VSS	NC	NC	NC	NC	NC

Table 2-2. Pin Matrix (continued)

	13	14	15	16	17	18	19	20	21	22	23
A	LINERXDATA [10]	LINERXCLK [7]	LINERXCLK [6]	LINERXCLK [41]	LINERXDATA [42]	LINERXCLK [1]	NC	NC	NC	LINERXDATA[45]	LINETXCLK[30]
B	LINERXCLK[9]	VDD33	VDD33	LINERXCLK[5]	LINERXDATA[3]	LINERXCLK[43]	NC	VDD33	VDD33	NC	LINETXDATA[29]
C	LINERXCLK[8]	VSS	VSS	LINERXCLK[4]	LINERXCLK[2]	LINERXDATA[44]	NC	VSS	VSS	LINETXDATA[30]	LINETXCLK[27]
D	LINERXDATA[8]	LINERXCLK[40]	LINERXDATA[41]	LINERXDATA[4]	LINERXDATA[2]	NC	LINERXCLK[44]	NC	LINERXCLK[46]	LINERXDATA[47]	LINETXDATA[25]
E	LINERXDATA[11]	LINERXDATA[7]	LINERXDATA[6]	LINERXCLK[3]	LINERXCLK[42]	LINERXDATA[1]	NC	NC	LINERXDATA[46]	LINETXDATA[27]	LINETXDATA[24]
F	LINERXDATA[12]	LINERXDATA[9]	—	—	—	—	—	—	LINETXDATA[28]	LINERXCLK[48]	LINETXDATA[22]
G	—	—	—	—	—	—	—	—	—	—	—
H	LINERXDATA[13]	LINERXCLK[39]	LINERXDATA[40]	LINERXDATA[5]	LINERXDATA[43]	NC	NC	LINERXCLK[45]	LINETXCLK[29]	LINETXDATA[26]	LINERXDATA[49]
J	VDD15	VDD15	VDD33	VDD33	VDD15	VDD15	VDD33	VDD33	VDD15	VDD15	VDD33
K	—	—	—	—	VDD15	VDD15	—	—	—	—	—
L	—	—	—	—	—	—	—	—	—	—	—
M	—	—	—	—	—	—	—	—	—	—	—
N	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	—
P	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
R	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
T	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
U	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
V	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
W	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
Y	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
AA	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD15	—
AB	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	—
AC	—	—	—	—	—	—	—	—	—	—	—
AD	—	—	—	—	—	—	—	—	—	—	—
AE	—	—	—	—	VDD15	VDD15	—	—	—	—	—
AF	VDD15	VDD15	VDD33	VDD33	LINETXCLK[61]	VDD15	VDD33	VDD33	VDD15	VDD15	VDD33
AG	NC	NC	NC	VSS	NC	LINETXDATA[60]	VSS	LINETXCLK[56]	NSMIRXCLK[3]	LINETXCLK[54]	NSMITXCLK[1]
AH	—	—	—	—	—	—	—	—	—	—	—
AJ	NC	NC	—	—	—	—	—	—	TDO	NSMIRXCLK[1]	SCAN_EN
AK	NC	LINETXCLK[68]	NC	LINETXDATA[65]	NC	RSTN	LINETXCLK[59]	SCANMODE	RXDATAEN[1]	RXDATAEN[2]	LINETXDATA[54]
AL	NC	NC	LINETXDATA[67]	NC	NC	LINETXDATA[62]	LINETXCLK[60]	IC3STATEN	IDDQ	NSMIRXSYNC[1]	NSMIRXSYNC[2]
AM	NC	VSS	VSS	NC	NC	E1XCLK	LINETXDATA[61]	VSS	VSS	LINETXDATA[59]	SCK2
AN	NC	VDD33	VDD33	LINETXCLK[67]	NC	LINETXCLK[64]	LINETXDATA[63]	VDD33	VDD33	TCK	TMS
AP	NC	NC	NC	NC	LINETXDATA[66]	NC	NC	NC	DS1XCLK	NC	TDI

Table 2-2. Pin Matrix (continued)

	24	25	26	27	28	29	30	31	32	33	34
A	LINETXCLK[28]	LINETXCLK[26]	LINERXDATA[48]	LINETXCLK[24]	LINETXCLK[23]	LINERXCLK[50]	LINERXDATA[51]	LINETXCLK[17]	LINERXCLK[52]	LINERXDATA[53]	—
B	LINERXCLK[47]	VDD33	VDD33	LINETXDATA[23]	LINERXCLK[49]	LINETXCLK[20]	VDD33	LINETXDATA[14]	LINETXDATA[12]	VDD33	VDD33
C	LINETXCLK[25]	VSS	VSS	LINETXCLK[21]	LINETXCLK[19]	LINETXCLK[16]	VSS	LINETXCLK[11]	VDD33	VDD33	VDD33
D	LINETXCLK[22]	LINERXDATA[50]	LINETXDATA[19]	LINETXDATA[18]	LINETXCLK[15]	LINERXCLK[53]	LINERXCLK[54]	VSS	VDD33	VDD33	VDD33
E	LINETXDATA[21]	LINETXCLK[18]	LINETXDATA[17]	LINETXDATA[15]	LINETXDATA[13]	LINERXDATA[55]	LINERXCLK[56]	VSS	VSS	VDD33	VDD33
F	LINETXDATA[20]	LINERXDATA[52]	LINETXCLK[14]	LINETXCLK[13]	LINERXDATA[56]	LINERXCLK[57]	VSS	VSS	VSS	VSS	VSS
G	—	—	—	LINERXDATA[54]	LINERXDATA[57]	LINETXDATA[10]	LINETXCLK[9]	LINETXCLK[8]	VSS	VSS	VSS
H	LINERXCLK[51]	LINETXDATA[16]	LINERXCLK[55]	LINETXCLK[10]	LINETXDATA[11]	LINETXDATA[8]	LINETXDATA[7]	LINETXCLK[6]	LINETXCLK[5]	LINETXDATA[5]	LINETXCLK[3]
J	VDD33	VDD15	LINETXCLK[12]	LINETXDATA[9]	—	LINETXCLK[7]	LINETXCLK[4]	LINETXDATA[4]	VSS	VDD33	LINETXCLK[2]
K	—	—	VDD15	LINETXDATA[6]	—	LINETXDATA[3]	LINETXDATA[2]	LINETXCLK[1]	VSS	VDD33	LINERXDATA[63]
L	—	—	VDD33	LINETXDATA[1]	—	LINERXDATA[58]	LINERXCLK[58]	LINERXDATA[59]	LINERXDATA[62]	LINERXCLK[64]	LINERXDATA[66]
M	—	—	VDD33	LINERXCLK[59]	—	LINERXDATA[60]	LINERXCLK[60]	LINERCLK[62]	LINERXDATA[65]	LINERXDATA[67]	LINERXCLK[67]
N	—	—	VDD15	LINERXDATA[61]	—	LINERXCLK[61]	LINERXCLK[63]	LINERXCLK[65]	CHIRXDATA[17]	CHIRXDATA[14]	LINERXCLK[68]
P	—	—	VDD15	CHIRXDATA[18]	—	LINERXCLK[66]	LINERXDATA[64]	CHIRXDATA[16]	VSS	VDD33	LINERXDATA[69]
R	—	—	VDD33	LINERXDATA[68]	—	—	CHIRXDATA[15]	CHIRXDATA[13]	VSS	VDD33	CHIRXDATA[10]
T	—	—	VDD33	LINERXCLK[69]	—	—	CHIRXDATA[12]	CHIRXDATA[11]	LINERXDATA[70]	LINERXCLK[70]	CHIRXDATA[7]
U	—	VDD15	VDD15	CHIRXDATA[6]	—	—	LINERXDATA[71]	CHIRXDATA[9]	CHIRXDATA[8]	LINERXCLK[71]	LINERXDATA[72]
V	—	VDD15	VDD15	CHIRXDATA[3]	—	—	LINERXCLK[72]	LINERXDATA[74]	LINERXDATA[73]	CHIRXDATA[4]	CHIRXDATA[5]
W	—	—	VDD33	CHIRXGCLK	—	—	LINERXDATA[75]	LINERXCLK[74]	CHIRXDATA[1]	CHIRXDATA[2]	LINERXCLK[73]
Y	—	—	VDD33	CHIRXGCLK	—	—	LINERXCLK[76]	CHIRXGTCLK	VSS	VDD33	CHIRXGFS
AA	—	—	VDD15	LINETXCLK[32]	—	LINETXDATA[31]	LINETXDATA[34]	LINETXCLK[31]	VSS	VDD33	LINERXCLK[75]
AB	—	—	VDD15	LINETXCLK[38]	—	LINETXCLK[35]	LINETXDATA[37]	LINETXCLK[34]	LINETXDATA[32]	CHITXGFS	LINERXDATA[76]
AC	—	—	VDD33	LINETXDATA[43]	—	LINETXDATA[40]	LINETXDATA[39]	LINETXCLK[37]	LINETXDATA[35]	LINERXCLK[77]	LINERXDATA[77]
AD	—	—	VDD33	CHITXDATA[16]	—	LINETXCLK[41]	LINETXCLK[42]	LINETXCLK[40]	LINETXCLK[36]	LINETXCLK[33]	LINETXDATA[33]
AE	—	—	VDD15	LINETXCLK[45]	—	LINETXCLK[44]	LINETXDATA[44]	LINETXDATA[42]	VSS	VDD33	LINETXDATA[36]
AF	VDD33	VDD15	CG_PLLCLKOUT	CLKIN_PLL	—	CHITXDATA[11]	CHITXDATA[13]	CHITXDATA[15]	VSS	VDD33	LINETXDATA[38]
AG	LINETXCLK[57]	LINETXCLK[58]	TRST	NC	CHITXDATA[5]	CHITXDATA[8]	MODE1_PLL	CHITXDATA[12]	LINETXCLK[43]	LINETXDATA[41]	LINETXCLK[39]
AH	—	—	VDD15	LINETXCLK[49]	LINETXCLK[48]	CHITXDATA[6]	VDD33A_SFPLL	VSSA_SFPLL	CHITXDATA[10]	CHITXDATA[17]	CHITXDATA[18]
AJ	PMRST	LINETXCLK[62]	VDD15	VDD15	LINETXCLK[46]	LINETXDATA[49]	CHITXDATA[7]	MODE0_PLL	CHITXDATA[9]	LINETXDATA[45]	CHITXDATA[14]
AK	LINETXDATA[53]	LINETXDATA[52]	CHITXDATA[1]	CHITXDATA[3]	NSMIRXCLK[2]	LINETXCLK[47]	LINETXDATA[48]	MODE2_PLL	VSS	VDD33	VDD33
AL	RXDATAEN[3]	NSMITXDATA[2]	LINETXCLK[52]	NSMITXSYNC[3]	LINETXCLK[51]	CHITXDATA[4]	LINETXCLK[55]	LINETXDATA[46]	VSS	VDD33	VDD33
AM	NSMIRXDATA[1]	VSS	VSS	LINETXCLK[53]	TXDATAEN[2]	TXDATAEN[3]	VSS	LINETXCLK[50]	LINETXDATA[50]	LINETXDATA[47]	VDD33
AN	LINETXDATA[58]	VDD33	VDD33	NSMIRXDATA[3]	NSMITXDATA[1]	TXDATAEN[1]	VDD33	NSMITXCLK[3]	CHITXDATA[2]	LINETXDATA[51]	VDD33
AP	SCK1	LINETXDATA[57]	LINETXDATA[56]	NSMIRXDATA[2]	LINETXDATA[55]	NSMIRXSYNC[3]	NSMITXSYNC[1]	NSMITXCLK[2]	NSMITXSYNC[2]	NSMITXDATA[3]	—

2.4 Pin Types

Table 2-3 describes each type of input, output, and I/O pin used in the Ultraframer device.

Table 2-3. Pin Types

Type Label	Description
I	**LVCMOS Input, LVTTL Switching Thresholds.**
I pd	**LVCMOS Input, LVTTL Switching Thresholds with Internal 50 kΩ Pull-Down Resistor.**
I pu	**LVCMOS Input, LVTTL Switching Thresholds with Internal 50 kΩ Pull-Up Resistor.**
O	**LVCMOS Output.**
O od	**Open-Drain Output.**
LIN	**LVDS Inputs.**
I/O	**Bidirectional Pin.** LVCMOS input with LVTTL switching thresholds and LVCMOS output.
I/O pd	B**idirectional Pin.** LVCMOS input with LVTTL switching thresholds with internal 50 kΩ pull-down resistor and LVCMOS output.
—	**Power, Ground, Analog Inputs for External Resistors, Capacitors, Voltage References, etc.**
NC	**No Connect.**

2.5 Pin Definitions

This section describes the function of each of the device pins. Pin functionality is descriptive information. The actual functionality is dependent upon the device configuration via the registers.

Table 2-4. LVDS Framer Reference Clock

Pin	Symbol	Type	Name/Description
AN4	THSCP	LIN	**Framer High-Speed Clock.** The clock on this pin is internally routed to the DS1/E1 framers and is used as an internal master clock. This input clock can be at 155 MHz or 622 MHz. Note there are no advantages in using a 622 MHz clock vs. a 155 MHz clock.
AP4	THSCN		
AG9	CTAPTH	—	**Center Tap TH.** LVDS buffer terminator center tap for THSCP/N. An optional 0.1 µF capacitor, connected between CTAP pin and ground, will improve the common-mode rejection of the LVDS input buffers.
AL5	RESHI	—	**Resistor.** A 100 Ω, 1% resistor is required between the RESHI and RESLO pins as a reference for the LVDS input buffer termination.
AL6	RESLO		
AK6	REF10*	I	**Reference 1.0 V.** External 1 V reference voltage pin (optional).
AJ6	REF14*	I	**Reference 1.4 V.** External 1.4 V reference voltage pin (optional).

* Optional: selected by MPU/top-level register UMPR_LVDS_REF_SEL. External reference voltage can be sourced from a low-impedance resistor (<1 kΩ) divider circuit decoupled with a 0.1 µF capacitor.

Table 2-5. DS3/E3 Out

Pin	Symbol	Type	Name/Description
AH1, AA6, V2	DS3POSDATAOUT[3:1]	O	**DS3/E3 Positive Data Output.** Either contains the positive-rail of the B3ZS/HDB3 encoded output data, or single-rail NRZ data.
AJ1, AC4, AC3	DS3NEGDATAOUT[3:1]	O	**DS3/E3 Negative Data Output.** Negative-rail B3ZS/HDB3 encoded output data. Not used in single-rail mode (held low in this case).
AC5, AB8, AB5	DS3DATAOUTCLK[3:1]	I pd	**DS3/E3 Data Output Clock.** 44.736 MHz or 34.368 MHz clock input and is typically connected to a crystal oscillator or clocking chip. This clock is required for M13 and E13 applications.
AB6, AD3, AD2	DS3RXCLKOUT[3:1]	O	**DS3/E3 Receive Clock Output.** 44.736 MHz DS3/34.368 MHz E3 clock out to external circuit.

Table 2-6. DS3/E3 In

Pin	Symbol	Type	Name/Description
AD1, AB2, W3	DS3POSDATAIN[3:1]	I pd	**DS3/E3 Positive Data Input.** Either contains the positive-rail of the B3ZS/HDB3 encoded input data, or single-rail NRZ data.
Y4, AC1, V1	DS3NEGDATAIN[3:1]	I pd	**DS3/E3 Negative Data Input.** Either contains the negative-rail of the B3ZS/HDB3 encoded input data, or in single-rail mode, this input may be used to count bipolar violations.
V3, V4, AB1	DS3DATAINCLK[3:1]	I pd	**DS3/E3 Data Input Clock.** 44.736 MHz or 34.368 MHz clock for the DS3/E3 positive and negative data inputs.

Table 2-7. NSMI In

Pin	Symbol	Type	Name/Description
AN27, AP27, AM24	NSMIRXDATA[3:1]	I pd	**Network Serial Multiplex Interface (NSMI) Receive* Data.** This is used in the following applications: ■ 51.84 Mbits/s serial data input that is used to bring in multiplexed DS1 or E1 channels to the framer. ■ DS3/E3 rate clear channel receive data to M13/E13.
AG21, AK28, AJ22	NSMIRXCLK[3:1]	I/O pd	**NSMI Receive Clock.** Used in the following applications: ■ Input (51.84 MHz) for the DS1/E1 application. ■ Output (44.736/34.368 MHz) for the DS3/E3 application.
AP29, AL23, AL22	NSMIRXSYNC[3:1]	I/O pd	**NSMI Receive Frame Sync.** Used in the following applications: ■ Input receive NSMI control for the framer. ■ Output receive control frame sync signal for M13/E13.
AL24, AK22, AK21	RXDATAEN[3:1]	O	**NSMI Receive Data Enable.** In FRM NSMI mode, this pin is not used. In M13 NSMI mode, the signal output on this pin goes low during the M1 byte of the first M1 frame of the DS3 frame. In E13 NSMI mode, the signal output on this pin goes low during the overhead bytes and control bits of the E3 frame.

* The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., NSMIRXDATA, on the transmit path, are labeled **receive**. Low-speed outputs, e.g., NSMITXDATA, on the receive path, are labeled **transmit**.

Table 2-8. NSMI Out

Pin	Symbol	Type	Name/Description
AP33, AL25, AN28	NSMITXDATA[3:1]	O	**NSMI Transmit Data.** NSMI output data from the framer or the M13/E13 blocks.
AN31, AP31, AG23	NSMITXCLK[3:1]	O	**NSMI Transmit Clock Output.** Output clock at 51.84 MHz for the DS1/E1 application or a 44.736/34.368 MHz output clock for the DS3/E3 application.
AL27, AP32, AP30	NSMITXSYNC[3:1]	O	**Transmit System Frame Sync Output.** Output transmit control frame sync signal from the framer or M13/E13 blocks.
AM29, AM28, AN29	TXDATAEN[3:1]	O	**Transmit Data Enable for NSMI Mode.** This output is used to request data for a particular link when the FRM NSMI is operating in nonloop timing mode. This output acts as a sync signal when the FRM NSMI operates in loop-timing mode. In M13 NSMI mode, the signal output on this pin goes low during the M1 byte of the first M1 frame of the DS3 frame. In E13 NSMI mode, the signal output on this pin goes low during the overhead bytes and control bits of the E3 frame.

* The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., NSMIRXDATA, on the transmit path, are labeled **receive**. Low-speed outputs, e.g., NSMITXDATA, on the receive path, are labeled **transmit**.

The transmit path is toward the high-speed fiber output, and the receive path is from the high-speed input. Low-speed inputs, e.g., LINERXDATA, on the transmit path, are labeled **receive**. Low-speed outputs, e.g., LINETXDATA, on the receive path, are labeled **transmit**.

Table 2-9. Shared Low-Speed Line In

Pin	Symbol	Type	Name/Description
T1, W2, V9, AB3, AG1, AA8, AC6, AE6, AD8, AC34, AB34, W30, V31, V32, U34, U30, T32, P34, R27, M33, L34, M32, P30, K34, L32, N27, M29, L31, L29, G28, F28, E29, G27, A33, F25, A30, D25, H23, A26, D22, E21, A22, C18, H17, A17, D15, H15, C12, C11, F12, H10, F5, G6, H8, G5, H6, E6, A4, A5, F8, C6, B6, F10, A6, C7, F11, D8, A7, E11, B8, A8, A9, A11, H13, F13, E13, A13, F14, D13, E14, E15, H16, D16, B17, D17, E18	LINERXDATA[86:1]	I pd	**Line Receive Data [86:1].** Inputs to the internal multirate crossconnect. These signals are used for received single-rail DS1/E1 line data input, sourced from an external LIU. In this mode, these signals will be routed via the crossconnect to the M13 multiplexer, E13 multiplexer, or the receive line inputs of the DS1/E1 framers. These signals may also be used as input data for DS2/E2 applications (see the System Design Guide).
T2, U1, W4, AA4, Y8, AD4, AE4, AH2, AH3, AC33, Y30, AA34, W31, W34, V30, U33, T33, T27, N34, M34, P29, N31, L33, N30, M31, N29, M30, M27, L30, F29, E30, H26, D30, D29, A32, H24, A29, B28, F22, B24, D21, H20, D19, B18, E17, A16, D14, H14, A12, A10, F6, E5, H9, C1, F4, J9, F7, B4, G8, D6, E7, F9, E8, D7, E10, E9, B7, H11, C8, D9, H12, D10, E12, B11, D11, B12, D12, B13, C13, A14, A15, B16, C16, E16, C17, A18	LINERXCLK[86:1]	I/O pd	**Line Receive Clock [86:1].** Configurable inputs to the internal multirate crossconnect. These inputs are used for asynchronous clocks associated with the line receive data inputs from external line interface units, or payload termination functions. In certain cases, this input can be used as an output. These pins may be used for DS2/E2 clocks in DS2/E2 applications. More information will be published in the System Design Guide.

The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., LINERXDATA, on the transmit path, are labeled **receive**. Low-speed outputs, e.g., LINETXDATA, on the receive path, are labeled **transmit**.

Table 2-10. Shared Low-Speed Line Out

Pin	Symbol	Type	Name/Description
H5, E1, N8, H3, L4, M8, M3, L1, T8, N1, AJ3, AF6, AL2, AG6, AH5, AK4, AJ5, AK5, AG8, AL15, AP17, AK16, AK11, AN19, AL18, AM19, AG18, AM22, AN24, AP25, AP26, AP28, AK23, AK24, AK25, AN33, AM32, AJ29, AK30, AM33, AL31, AJ33, AE30, AC27, AE31, AG33, AC29, AC30, AF34, AB30, AE34, AC32, AA30, AD34, AB32, AA29, C22, B23, F21, E22, H22, D23, E23, B27, F23, E24, F24, D26, D27, E26, H25, E27, B31, E28, B32, H28, G29, J27, H29, H30, K27, H33, J31, K29, K30, L27	LINETXDATA[86:1]	O	**Line Transmit Data [86:1].** Outputs from the internal multirate crossconnect. These signals are used for transmit of single-rail DS1/E1 line data output, sourced to an external LIU. In this mode, these signals will be routed via the crossconnect from the M13 multiplexer, the E13 multiplexer, or the transmit line outputs of the DS1/E1 framers. Each of these outputs comes from the internal MRXC and can be individually set to high impedance. These pins may be used for output data in DS2/E2 applications (see the System Design Guide).
H7, D1, F2, K8, G1, H1, P6, P5, N3, U3, AF5, AG5, AH4, AJ4, AF9, AL3, AH6, AL4, AK14, AN16, AK12, AJ12, AN18, AH7, AJ25, AF17, AL19, AK19, AG25, AG24, AG20, AL30, AG22, AM27, AL26, AL28, AM31, AH27, AH28, AK29, AJ28, AE27, AE29, AG32, AD30, AD29, AD31, AG34, AB27, AC31, AD32, AB29, AB31, AD33, AA27, AA31, A23, H21, A24, C23, A25, C24, A27, A28, D24, C27, B29, C28, E25, A31, C29, D28, F26, F27, J26, C31, H27, G30, G31, J29, H31, H32, J30, H34, J34, K31	LINETXCLK[86:1]	I/O pd	**Line Transmit Clock [86:1].** Configurable outputs from the internal multirate crossconnect. These outputs are used for asynchronous clocks, associated with the line transmit data outputs to external line interface units or payload termination functions. Each of these outputs comes from the internal MRXC and can be individually set to high impedance. In certain cases, these pins can be used as inputs (input DS2/E2 clocks). More information will be published in the System Design Guide .

The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., CHIRXDATA, on the transmit path are labeled **receive**. Low-speed outputs, e.g., CHITXDATA, on the receive path are labeled **transmit**.

Table 2-11. TDM Concentration Highway (CHI) In

Pin	Symbol	Type	Name/Description
P27, N32, P31, R30, N33, R31, T30, T31, R34, U31, U32, T34, U27, V34, V33, V27, W33, W32	CHIRXDATA[18:1]	I pd	**CHI Receive Data [42:1].** Configurable synchronous TDM inputs to the internal multirate cross connect. Can be used in one of the following modes: CHI mode: Receive TDM input highways. Can be configured to operate at 8.192 Mbits/s or 16.384 Mbits/s. Parallel system bus mode: The parallel system bus is a 16-bit wide 19.44 Mbits/s synchronous TDM highway. Bits [16:9] are used for time-slot data. Bits [8:1] are used for robbed-bit signaling data in a ASM like fashion and are optional. CHIRXGFS is the frame synchronization input for the parallel system bus and CHIRXGCLK is the 19.44 MHz clock input. Asynchronous mode: In this mode, these inputs are used for DS1/E1 received negative-rail data. These pins may be used as input data for DS2/E2 applications. More information will be published in the System Design Guide.

Table 2-12. TDM Concentration Highway (CHI) Out

Pin	Symbol	Type	Name/Description
AH34, AH33, AD27, AF31, AJ34, AF30, AG31, AF29, AH32, AJ32, AG29, AJ30, AH29, AG28, AL29, AK27, AN32, AK26	CHITXDATA[18:1]	I/O pd	**CHI Transmit Data [42:1].** Configurable synchronous TDM outputs from the internal multirate cross connect. Can be used in one of the following modes: CHI mode: Transmit TDM output highways. Can be configured to operate at 8.192 Mbits/s or 16.384 Mbits/s. Parallel system bus mode: The parallel system bus is a 16-bit wide 19.44 Mbits/s synchronous TDM highway. Bits [16:9] are used for time-slot data. Bits [8:1] are used for robbed-bit signaling data in a ASM like fashion and are optional. CHITXGFS is the frame synchronization input for the parallel system bus and CHITXGCLK is the 19.44 MHz clock input. Asynchronous mode: In this mode, these outputs are used for DS1/E1 transmit negative-rail data. Each of these outputs comes from the internal MRXC and can be individually set to high impedance. In rare cases, this output can be used as an input. These pins have various functionalities in DS2/E2 applications. More information will be published in the System Design Guide. When running in CHI compression mode, CHITXDATA[17] becomes a frame sync output from the device, which signifies the beginning of the CHI output frame. This feature is only available in V3.0 devices and later.

Table 2-13. Framer (FRM) Block, CHI/Parallel System Bus (PSB) Clock and Sync

Pin	Symbol	Type	Name/Description
Y31	CHIRXGTCLK	I pd	**Global Transmit Line Clock.** This is the transmit line clock for the DS1 or E1 framer. Normally this input is not used and the transmit clock is generated by an internal phase-lock loop which uses CLKIN_PLL as a reference. Note that if this input is used all the transmit framers must run at the same rate, either 1.544 MHz or 2.048 MHz. This signal could be used for both CHI and parallel system bus.
W27	CHIRXGCLK	I pd	**Receive Global System Clock.** This signal is used for both CHI and parallel system bus. In CHI mode, it is a 8.192 MHz or 16.384 MHz TDM clock. In parallel system bus mode, it is a 19.44 MHz clock.
Y34	CHIRXGFS	I pd	**Receive System Frame Sync.** This signal is used for both CHI and parallel system bus. In CHI mode, it is an 8 kHz pulse that references the location of time slots in the receive CHI inputs. Its polarity, sampling edge, and offset from time slots in the concentration highways may all be programmed. In parallel system bus mode, it is an 8 kHz reference for time slots within the parallel system bus input highways. In this mode, the frame strobe is a positive pulse with active edge provisioned by a register.
AB33	CHITXGFS	I pd	**Transmit System Frame Sync.** This signal is used for both CHI and parallel system bus. In CHI mode, it is an 8 kHz pulse that references the location of time slots in the transmit CHI outputs. Its polarity, sampling edge, and offset from time slots in the concentration highways may all be programmed. In parallel system bus mode, it is an 8 kHz reference for time slots within the parallel system bus output highways. In this mode, the frame strobe is a positive pulse with active edge provisioned by a register. For version 3.0 devices and later, CHITXGFS also serves as a required 8 kHz frame sync when operating in NSMI slip mode.
Y27	CHITXGCLK	I pd	**Transmit Global System Clock.** This signal is used for both CHI and parallel system bus. In CHI mode, it is a 8.192 MHz or 16.384 MHz TDM clock. In parallel system bus mode, it is a 19.44 MHz clock.

Table 2-14. Reference Clocks

Pin	Symbol	Type	Name/Description
V8	DS2AISCLK	I pd	**DS2 AIS Clock.** See separate DS2/E2 application note for use in DS2 mode. If used, this input can be provided by a free-running crystal or clocking chip.
AA1	E2AISCLK	I pd	**E2 AIS Clock.** See separate DS2/E2 application note for use in E2 mode. If used, this input can be provided by a free-running crystal or clocking chip.
AM18	E1XCLK	I pd	**E1 X Clock.** This clock signal is used for three purposes: to generate E1 AIS (all 1s), as a reference to the E1 DJA, and as a clock source for the test pattern generator and test pattern monitor. This input may be provided by a 2.048 MHz, a 32.768 MHz, or a 65.536 MHz ± 50 ppm free-running crystal oscillator or clocking chip. **Note:** For the E1 DJA, an input of 32.768 MHz or 65.536 MHz must be used.
AP21	DS1XCLK	I pd	**DS1 X Clock**. This clock signal is used for three purposes: to generate DS1 AIS (all 1s), as a reference to the DS1 DJA, and as a clock source for the test pattern generator and test pattern monitor. This input may be provided by a 1.544 MHz, a 24.704 MHz, or a 49.408 MHz ± 32 ppm free-running crystal oscillator or clocking chip. **Note:** For the DS1 DJA, an input of 24.704 MHz or 49.408 MHz must be used.

Table 2-15. Clock Generator

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Name/Description</th></tr>
<tr><td>AF27</td><td>CLKIN_PLL</td><td>I pd</td><td>Transmit Line Clock Generator Reference Input. The clock generator is used to derive a transmit line clock of the appropriate frequency (DS1/E1) synchronized to CLKIN_PLL. The derived clock is used in the DS1/E1 transmit framer sections.</td></tr>
<tr><td>AF26</td><td>CG_PLLCLKOUT</td><td>O</td><td>Framer PLL Test Mode Output. Framer PLL clock (1.544 MHz, 2.048 MHz) selected by the device register.</td></tr>
<tr><td>AK31, AG30, AJ31</td><td>MODE[2:0]_PLL</td><td>I pd</td><td>Framer PLL Input Clock Mode Select Bits. The settings of these mode select pins must correspond to the frequency of CLKIN_PLL as shown below.
<table>
<tr><th>MODE[2:0]_PLL</th><th>CLKIN_PLL</th><th>MODE[2:0]_PLL</th><th>CLKIN_PLL</th></tr>
<tr><td>000</td><td>Reserved</td><td>100</td><td>16.384 MHz</td></tr>
<tr><td>001</td><td>51.840 MHz</td><td>101</td><td>8.192 MHz</td></tr>
<tr><td>010</td><td>26.624 MHz</td><td>110</td><td>4.096 MHz</td></tr>
<tr><td>011</td><td>19.440 MHz</td><td>111</td><td>2.048 MHz</td></tr>
</table></td></tr>
</table>

Table 2-16. Microprocessor Interface

Pin	Symbol	Type	Name/Description
G4	MPCLK	I	**Microprocessor Clock.** This clock is required to properly sample address, data, and control signals from the microprocessor in both asynchronous and synchronous modes of operation.
D2	MPMODE	I	**Microprocessor Mode.** If the microprocessor interface is synchronous, MPMODE should be set to 1. If the microprocessor interface is asynchronous, MPMODE should be set to 0.
G7	CSN	I pu	**Chip Select.** Active-low high-order address signal. Chip select must be set low at the beginning of any read or write access and returned high at the end of the cycle.
F3	ADSN	I	**Address Strobe.** Active-low address strobe that indicates the beginning of a read or write access. It is a one MPCLK cycle-wide pulse for synchronous mode. In asynchronous mode, it is active for the entire read/write cycle. Address bus signals, ADDR[20:0], are available to the Ultraframer when ADSN is low. The address bus should remain valid for the duration of ADSN.
J6	RWN	I	**Read/Write.** RWN is set high during a read cycle, or set low during a write cycle.
J5	DSN	I	**Data Strobe.** For a read cycle, the contents of the internal register will be output on DATA [15:0]. For a write cycle, the DATA [15:0] will be clocked into the internal register. To initiate the start of the read/write operation, DSN must be low during the entire read/write cycle. This signal should only be used for asynchronous mode.
N5, P8, M4, L3, J1, N6, M5, L8, K4, M6, H2, L5, L6, G2, F1, K5, J4, J8, G3, H4, K6	ADDR[20:0]	I	**Address [20:0].** ADDR[20] is the MSB and ADDR[0] is the LSB for addressing all the internal registers during microprocessor access cycles. All addresses are 21-bit word addresses; therefore, in a typical application, ADDR[0] of the TFRA84J13 device would be connected to address bit 1 of a byte-addressable system address bus. **Note:** The Ultraframer is little endian, i.e., the least significant byte is stored in the lowest address and the most significant byte is stored in the highest address. Care must be exercised in connection with microprocessors that use big endian byte ordering.
P1, U9, T4, R4, N2, P4, U5, R5, M1, T5, M2, R8, N4, U2, L2, K1	DATA[15:0]	I/O	**Data [15:0].** 16-bit data bus input for write operations and output for read operations. DATA[15] is the MSB, and DATA[0] is the LSB.
U4, R1	PAR[1:0]	I/O	**Data Parity.** Byte-wide parity bits for data. PAR[1] is the parity for DATA[15:8], and PAR[0] is the parity for DATA[7:0]
T3	DTN	O	**Data Transfer Acknowledge.** The delay associated with DTN going low depends on the Ultraframer block being accessed. In asynchronous mode, when ADSN or DSN is deasserted it will drive the DTN signal high. When inactive, CSN will drive DTN to be 3-stated. The microprocessor should wait after DTN is deasserted, before starting the next operation.
U8	HP_INTN	O od	**High-Priority and Low-Priority Interrupt.** Active-low. Each functional block contains its individual low-priority interrupt. High-priority interrupts are generated by E13 blocks. Each interrupt is individually maskable. Requires an external 5 kΩ pull-up resistor.
W1	LP_INTN		

Table 2-17. Boundary Scan (*IEEE*® 1149.1)

Pin	Symbol	Type	Name/Description
AN22	TCK	I	**Test Clock.** This signal provides timing for boundary-scan test operations.
AP23	TDI	I pu	**Test Data In.** Boundary-scan test data input signal, sampled on the rising edge of TCK.
AN23	TMS	I pu	**Test Mode Select.** Controls boundary-scan test operations. TMS is sampled on the rising edge of TCK.
AG26	TRST	I pu	**Test Reset (Active-Low).** This signal provides an asynchronous reset for the boundary-scan TAP controller.
AJ21	TDO	O	**Test Data Out.** Boundary-scan test data output signal is updated on the falling edge of TCK. The TDO output will be high-impedance, except when transmitting test data.

Table 2-18. General-Purpose Interface

Pin	Symbol	Type	Name/Description
AK18	RSTN	I pu	**Global Hardware Reset.** Active-low. Initializes all internal registers to their default state. This is an asynchronous reset on the falling edge, but RSTN should be held low for at least 1 µs. RSTN should be held low until both power supplies (1.5 V and 3.3 V) are stabilized upon power up.
AJ24	PMRST	I/O pd	**Performance Monitor Reset.** Resets error counters. When enabled as an input, it is a 1s square wave that forces an update of PM counters upon the rising edge. When the PMRST is generated internally from the MPU clock, this pin is an output.
AL20	IC3STATEN	I pu	**Output Enable.** When high, output buffers will operate normally. When low, all outputs will be forced to a high-impedance state. IC3STATEN should be held low until both power supplies (1.5 V and 3.3 V) are stabilized upon power up.
AP24	SCK1	I pd	**Scan Clock 1.** Reserved. Do not connect.
AM23	SCK2	I pd	**Scan Clock 2.** Reserved. Do not connect.
AJ23	SCAN_EN	I pd	**Scan Enable.** Reserved. Do not connect.
AK20	SCANMODE	I pd	**Serial Scan Input for Testing.** Reserved. Do not connect.
AL21	IDDQ	I	**IDDQ Input.** This pin must be externally pulled down with a 1 kΩ resistor.

Table 2-19. Analog Power and Ground Signals

Pin	Symbol	Type	Name/Description
AH31	V_{SSA_SFPLL}	—	**SFPLL Ground.** Isolated ground for the internal SFPLL.
AH30	V_{DD33A_SFPLL}	—	**SFPLL Power.** This is a 3.3 V power supply for the internal SFPLL. Good engineering practice needs to be applied. Please refer to the System Design Guide.

Table 2-20. Digital Power and Ground Signals

Pin	Symbol	Type	Name/Description
J10, J13, J14, J17, J18, J21, J22, J25, K9, K17, K18, K26, N9, N13, N14, N15, N16, N17, N18, N19, N20, N21, N22, N26, P9, P13, P22, P26, R13, R22, T13, T22, U10, U13, U22, U25, U26, V10, V13, V22, V25, V26, W13, W22, Y13, Y22, AA9, AA13, AA22, AA26, AB9, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB26, AE9, AE17, AE18, AE26, AF10, AF13, AF14, AF18, AF21, AF22, AF25, AH26, AJ26, AJ27	V_{DD15}	—	Common power signals for 1.5 V V_{DD}.
A2, A3, B1, B3, B5, B9, B10, B14, B15, B20, B21, B25, B26, B30, B33, B34, C2, C4, C32, C33, C34, D3, D5, D32, D33, D34, E2, E4, E33, E34, J2, J11, J12, J15, J16, J19, J20, J23, J24, J33, K2, K33, L9, L26, M9, M26, P2, P33, R2, R9, R26, R33, T9, T26, W9, W26, Y2, Y9, Y26, Y33, AA2, AA33, AC9, AC26, AD9, AD26, AE2, AE33, AF2, AF11, AF12, AF15, AF16, AF19, AF20, AF23, AF24, AF33, AK2, AK33, AK34, AL33, AL34, AM34, AN14, AN15, AN20, AN21, AN25, AN26, AN30, AN34	V_{DD33}	—	Common power signals for 3.3 V V_{DD}.
B2, C3, C5, C9, C10, C14, C15, C20, C21, C25, C26, C30, D4, D31, E3, E31, E32, F30, F31, F32, F33, F34, G32, G33, G34, J3, J32, K3, K32, P3, P14, P15, P16, P17, P18, P19, P20, P21, P32, R3, R14, R15, R16, R17, R18, R19, R20, R21, R32, T14, T15, T16, T17, T18, T19, T20, T21, U14, U15, U16, U17, U18, U19, U20, U21, V14, V15, V16, V17, V18, V19, V20, V21, W14, W15, W16, W17, W18, W19, W20, W21, Y3, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y32, AA3, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA32, AE3, AE32, AF3, AF32, AG16, AG19, AJ7, AJ8, AJ9, AJ10, AJ11, AK3, AK7, AK8, AK9, AK10, AK32, AL7, AL8, AL9, AL10, AL32, AM4, AM14, AM15, AM20, AM21, AM25, AM26, AM30, AN3, AN5, AN7, AP3, AP5, AP7	V_{SS}	—	Common ground signals.

Table 2-21. No Connects

Pin	Symbol	Type	Name/Description
Y1, AM13, AF8, AG10, AG14, AE1, AF1, AB4, AD5, AE5, AG4, AC2, Y5, AA5, AL1, AG3, AJ2, V5, W8, W5, AK1, AG2, AF4, AC8, AD6, AE8, H18, AL14, AP15, AP16, B22, A21, D20, H19, E20, A20, AG27, AN1, AM1, AM3, AM2, AP22, AJ14, AN10, AM10, AP12, AP10, AM9, AP11, AM17, AG17, AP19, AM8, AM7, AP6, AN6, AM16, AK15, AN17, AP2, AN2, AM6, AM5, AL13, AK13, AM11, AN13, AP14, AN11, AN12, AP13, AL17, AK17, AP20, AP8, AN8, AN9, AP9, AJ13, AG15, AG7, AH8, AL16, AP18, AG12, AL11, C19, B19, AM12, AG11, AG13, D18, A19, AL12, E19	No Connect	NC	**No Connects.** These pins are not used in the Ultraframer device.

3 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3-1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (V_{DD33})	–0.5	4.2	V
Supply Voltage (V_{DD15})	–0.3	2.0	V
Input Voltage: LVCMOS LVDS	 –0.3 –0.3	 5.25 V_{DD33} + 0.3	 V V
Power Dissipation	—	—	mW
Storage Temperature Range	–65	125	°C

3.1 Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Table 3-2. ESD Tolerance

Device	Minimum Threshold	
	HBM	CDM
TFRA84J13	2000 V	500 V

3.2 Thermal Parameters (Definitions and Values)

System and circuit board level performance depends not only on device electrical characteristics, but also on device thermal characteristics. The thermal characteristics frequently determine the limits of circuit board or system performance, and they can be a major cost adder or cost avoidance factor. When the die temperature is kept below 125 °C, temperature-activated failure mechanisms are minimized. The thermal parameters that Agere provides for its packages help the chip and system designer choose the best package for their applications, including allowing the system designer to thermally design and integrate their systems.

It should be noted that all the parameters listed below are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA} - Junction to Air Thermal Resistance

Θ_{JA} is a number used to express the thermal performance of a part under JEDEC standard natural convection conditions. Θ_{JA} is calculated using the following formula:

$\Theta_{JA} = (T_J – T_{amb}) / P$; where P = power

Θ_{JMA} - Junction to Moving Air Thermal Resistance

Θ_{JMA} is effectively identical to Θ_{JA} but represents performance of a part mounted on a JEDEC four layer board inside a wind tunnel with forced air convection. Θ_{JMA} is reported at airflows of 200 LFPM and 500 LFPM (linear feet per minute), which roughly correspond to 1 m/s and 2.5 m/s (respectively). Θ_{JMA} is calculated using the following formula:

$\Theta_{JMA} = (T_J - T_{amb}) / P$

Θ_{JC} - Junction to Case Thermal Resistance

Θ_{JC} is the thermal resistance from junction to the top of the case. This number is determined by forcing nearly 100% of the heat generated in the die out the top of the package by lowering the top case temperature. This is done by placing the top of the package in contact with a copper slug kept at room temperature using a liquid refrigeration unit. Θ_{JC} is calculated using the following formula:

$\Theta_{JC} = (T_J - T_C) / P$

Θ_{JB} - Junction to Board Thermal Resistance

Θ_{JB} is the thermal resistance from junction to board. This number is determined by forcing the heat generated in the die out of the package through the leads or balls by lowering the board temperature and insulating the package top. This is done using a special fixture, which keeps the board in contact with a water chilled copper slug around the perimeter of the package while insulating the package top. Θ_{JB} is calculated using the following formula:

$\Theta_{JB} = (T_J - T_B) / P$

Ψ_{JT}

Ψ_{JT} correlates the junction temperature to the case temperature. It is generally used by the customer to infer the junction temperature while the part is operating in their system. It is not considered a true thermal resistance. Ψ_{JT} is calculated using the following formula:

$\Psi_{JT} = (T_J - T_C) / P$

Table 3-3. Thermal Parameter Values

Parameter	Temperature °C/Watt
Θ_{JA}	12.8
Θ_{JMA} (1 m/s)	9.5
Θ_{JMA} (2.5 m/s)	8
Θ_{JC}	2.5
Θ_{JB}	7.6
Ψ_{JT}	1

3.3 Reliability

Product reliability can be calculated as the probability that the product will perform under normal operating conditions for a set period of time. Factors influencing the reliability of a product cover a range of variables, including design and manufacturing. The failure rate of a product is given as the number of units failing per unit time. This failure rate is known as FIT, which is as follows:

1 FIT = 1 failure/1 x 10^9 hours.

Another unit used for failure rate is known as MTBF, which is 1/FIT. Many assumptions are made when calculating the failure rate for a product, such as the average junction temperature and activation energy. The assumptions made for calculating FIT and MTBF are shown in Table 3-4:

Table 3-4. Reliability Data

Junction Temperature	FIT (Per 1 x 10^9 Device Hours)	MTBF	Activation Energy
55 °C	36	2.78 x 10^7 hours	0.7eV

4 Electrical Characteristics

4.1 Recommended Operating Voltages

The following table lists the voltages, along with the tolerances, required for proper operation of the TFRA84J13 device.

Table 4-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3 V Power Supply	V_{DD33}	3.14	3.3	3.47	V
1.5 V Power Supply	V_{DD15}	1.4	1.5	1.6	V
Ground	V_{SS}	—	0.0	—	V
1.0 V—LVDS Reference*	REF10	—	1.0	—	V
1.4 V—LVDS Reference*	REF14	—	1.4	—	V
Ambient Temperature	T_A	–40	—	85	°C

* Internal reference voltage is used if UMPR_LVDS_REF_SEL = 1, or else external voltage is used.

4.2 Recommended Powerup Sequence

The Ultraframer device requires dual power supplies, a 3.3 V supply for the I/O and a 1.5 V supply for the core.

During power up, RSTN should be held low (holding the device in reset) and IC3STATEN should be held low (3-stating all output buffers). After the 3.3 V and 1.5 V supplies are stable, MPCLK (which affects the device reset) should be applied and must be present for at least two clock cycles before RSTN and IC3STATEN are released. It is then recommended that IC3STATEN be released concurrent with, or after, the release of RSTN. There are no constraints as to which supply (3.3 V or 1.5 V) must come up first, nor does it matter how long it takes the second supply to come up after the first supply.

4.3 Power Consumption

The power consumption of the device is application dependent since it is not possible to use all the device features simultaneously. The nominal measured values for power per block are shown in Table 4-2.

Table 4-2. Typical Power Consumption Per Block

Typical power by block refers to all instances being used.

Block	Maximum Instance	Typical, Per Single Instance	Unit
E13	3	0.013	W
M13	3	0.013	W
TPG/TPM	1	TBD	W
FRM	3	0.195	W
DS1DJA	3	0.026	W
MPU	1	0.420*	W
LVDS I/O	2	0.020	W
NSMI I/O	3	0.032	W
DS3 I/O	3	0.050	W
MRXC	1	0.050	W

* Measured with a 50 MHz MPCLK. With a 25 MHz MPCLK, the typical per single instance value of MPU power is approximately 0.2 W.

Testing has shown that, on the average, approximately 0.35 W can be saved by utilizing the **divide by 16** MPU clock power down feature. Please refer to MPU register 0x0019 in the *Ultramapper*™ Register Description document for further information. Additional MPU clock divisor options are available.

4.4 ac and dc Characteristics

4.4.1 LVCMOS Interface Characteristics

Table 4-3. LVCMOS Inputs Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_I	$V_{SS} < V_{IN} < V_{DD33}$	—	—	1.0*	µA
High-input Voltage	V_{IH}	—	2.0	—	—	V
Low-input Voltage	V_{IL}	—	V_{SS}	—	0.8	V
Input Capacitance	C_I	—	—	—	1.5	pF

* Excludes current due to pull-up or pull-down resistors.

Table 4-4. LVCMOS Outputs Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage Low	V_{OL}	I_{OL} = max	V_{SS}	—	0.5	V
Output Voltage High	V_{OH}	I_{OL} = max	V_{DD} – 0.5	—	V_{DD}	V
Output Current Low	I_{OL}	—	—	—	6*	mA
Output Current High	I_{OH}	—	—	—	–6*	mA
Output Capacitance	C_O	—	—	3	—	pF
HIZ Output Leakage Current	I_{OZ}	—	—	—	10	µA

* DTN output current is 10 mA max.

Table 4-5. LVCMOS Bidirectionals Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Leakage Current	I_L	$V_{SS} < V_{IN} < V_{DD33}$	—	—	11	µA
High-input Voltage	V_{IH}	—	2.0	—	V_{DD33} + 0.3	V
Low-input Voltage	V_{IL}	—	V_{SS}	—	0.8	V
Biput Capacitance	C_{IB}	—	—	5.0	—	pF
Output Voltage Low	V_{OL}	I_{OL} = –6 mA*	—	—	0.5	V
Output Voltage High	V_{OH}	I_{OH} = 6 mA*	2.4	—	—	V

* The following bidirectional pins can sink/source 10 mA: NSMIRXCLK[3:1].

4.4.2 LVDS Interface Characteristics

3.3 V ± 5% V_{DD}, –40 °C to +125 °C junction temperature.

Table 4-6. LVDS Interface dc Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Buffer Parameters						
Input Voltage Range High (V_{IA} or V_{IB}) Low (V_{IA} or V_{IB})	V_I V_{IH} V_{IL}	$\lvert V_{GPD}\rvert$ < 925 mV, dc—1 MHz	 — 0	 — —	 2.4 —	 V V
Input Differential Threshold	V_{IDTH}	dc— 450 MHz	–100	—	100	mV
Input Differential Hysteresis	V_{HYST}	(+V_{IDTH}) – (–V_{IDTH})	—	—	*	mV
Receiver Differential Input Impedance	R_{IN}	With build-in termination, center-tapped	80	100	120	Ω

* The buffer will not produce output transitions when input is open-circuited. When the true and complement inputs are floating, the input buffer will not oscillate.

5 Timing

5.1 DS3/E3 Timing

Figure 5-1 shows a simplified representation of the DS3/E3 I/O.

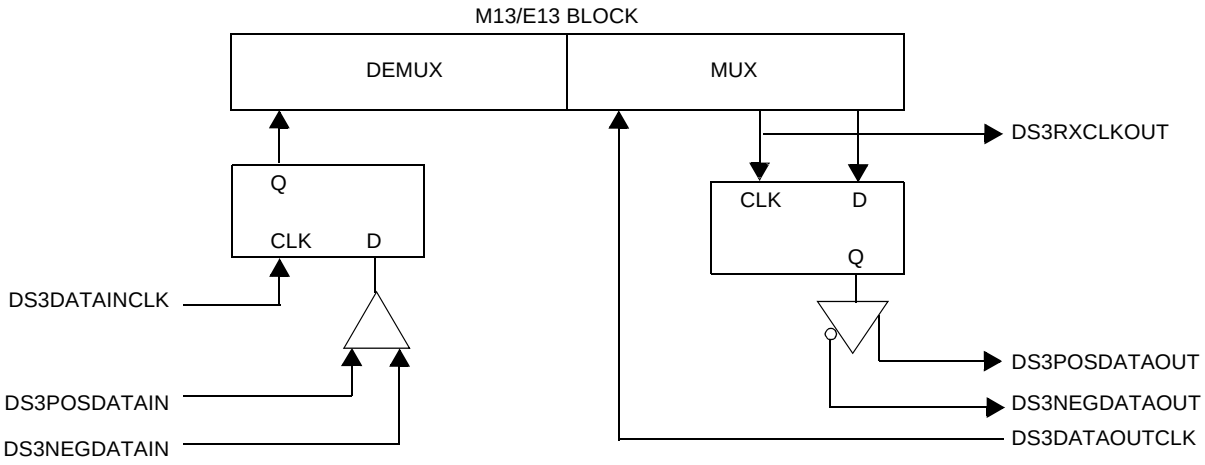


Figure 5-1. DS3/E3 Interface Diagram in M13/E13 Block

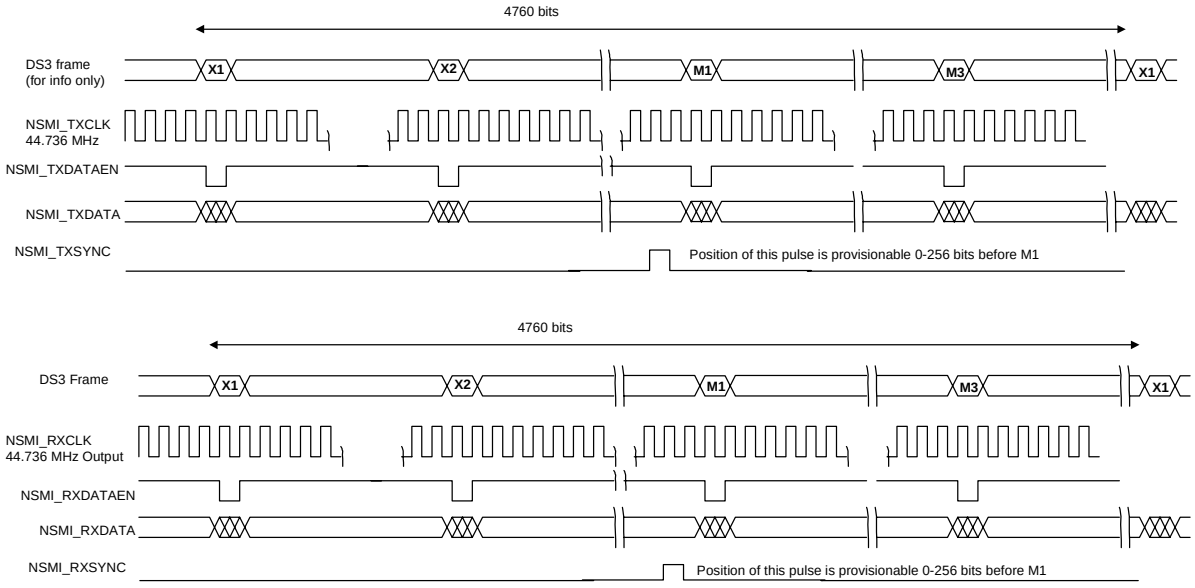
Table 5-1. DS3/E3 Input Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
DS3POSDATAIN[3:1] DS3NEGDATAIN[3:1]	DS3DATAINCLK	R/F	5	5	3	3

Table 5-2. DS3/E3 Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
DS3POSDATAOUT[3:1] DS3NEGDATAOUT[3:1]	DS3RXCLKOUT	R/F	0	3

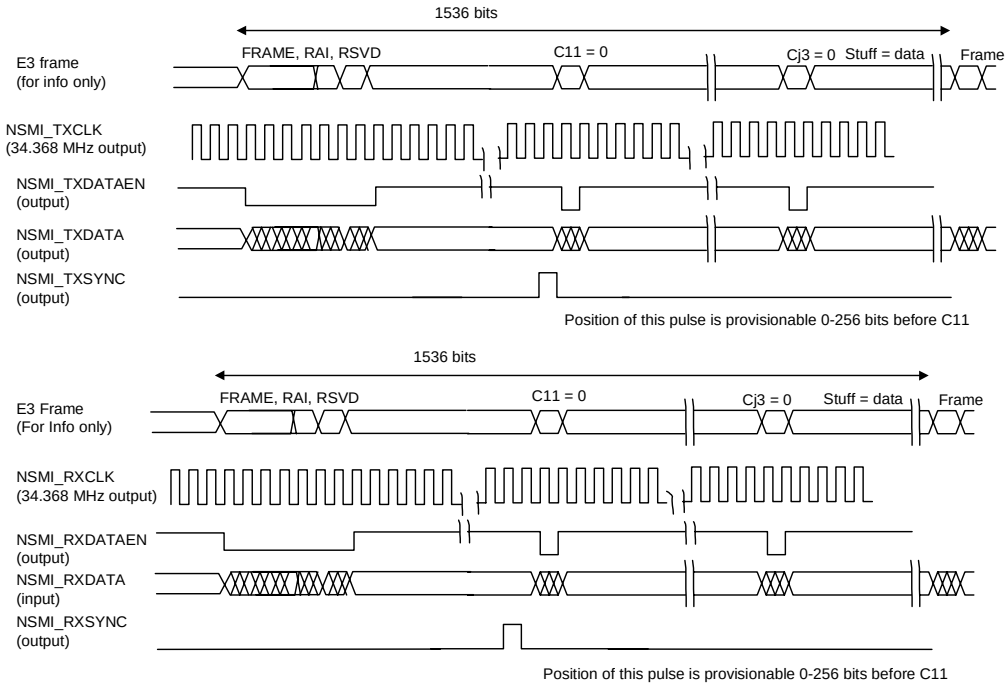
5.2 NSMI Timing



Notes:
Clock from M13 is at 44.736 MHz rate and is not gapped. TXDATAEN is provided to mark the DS3 frame overhead times.

M1 can occur asynchronously and its position is optionally marked by TXSYNC, which is provisioned to be 0 to 255 bits before the M1 bit. TXDATAEN goes low during DS3 frame overhead bits.

Figure 5-2. NSMI Clock and Data Diagram for M13 NSMI Mode (NSMI <---> M13 <---> DS3 External I/O)

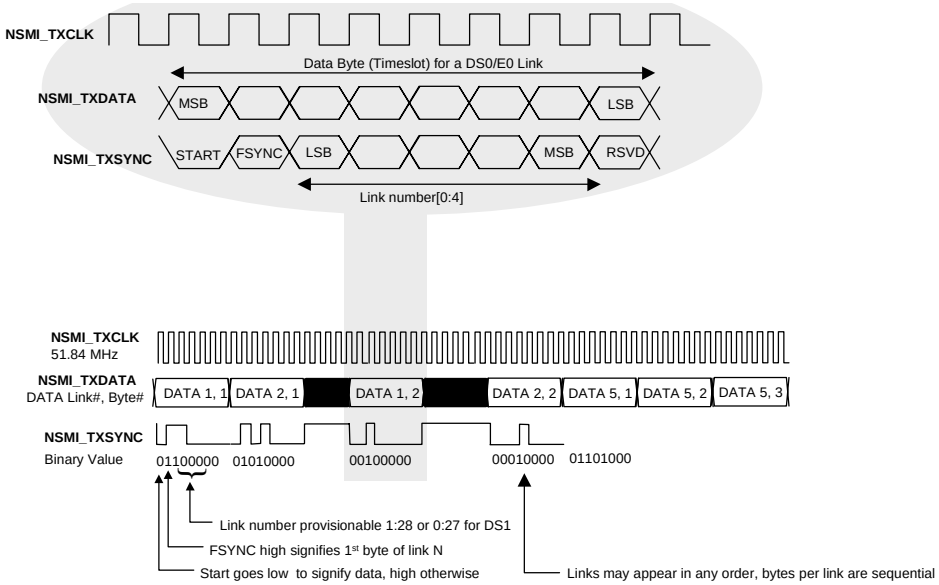


Notes:
Clock from E13 is at 34.368 MHz rate and is not gapped. TXDATAEN is provided to mark the overhead time and control bits time of the E3 frame.

C11's (the first C bit of the first tributary) position is optionally marked by TXSYNC, which is provisioned to be 0 to 255 bits before C11 (bit 385 of the E3 frame).

During periods where the OH is present the TXDATAEN signal goes low. All C bits are zero and the stuff bits are used for data.

Figure 5-3. NSMI Clock and Data Diagram for E13 NSMI Mode 1 (NSMI <---> E13 <---> E3 External I/O)



Note: The 193rd bit of a DS1 frame is not transmitted on the NSMI but is used to locate the FSYNC position. As a consequence of this, signaling bits are not transported in Ultraframer.

Figure 5-4. NSMI Clock and Data Diagram for Framer (FRM) NSMI Mode

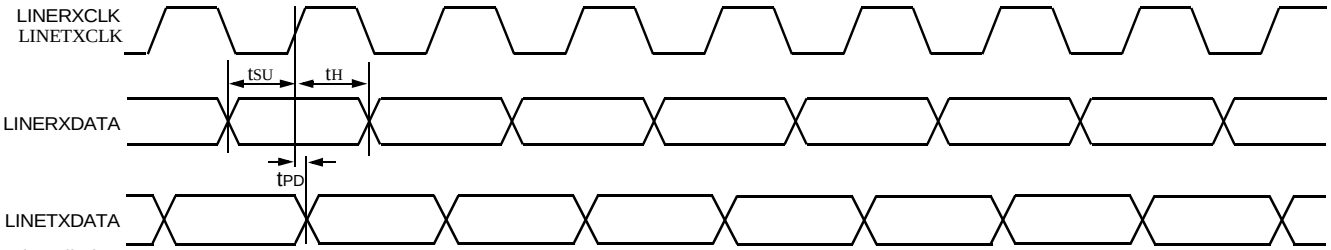
Table 5-3. NSMI Input Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
NSMIRXDATA[3:1]	NSMIRXCLK	R	3.5	3.5	5	0
NSMIRXSYNC[3:1]	NSMIRXCLK	R	3.5	3.5	5	0

Table 5-4. NSMI Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
NSMITXDATA[3:1]	NSMITXCLK	R	0.5	8.75
NSMITXSYNC[3:1]	NSMITXCLK	R	0.5	8.75
RXDATAEN[3:1]	NSMIRXCLK	R	0.5	8.75
TXDATAEN[3:1]	NSMITXCLK	R	0.5	8.75
NSMIRXSYNC[3:1]	NSMIRXCLK	R	0.5	8.75

5.3 Shared Low-Speed Line Timing



Note: Single-rail shown.

Figure 5-5. Shared Low-Speed Line Clock and Data Timing

Table 5-5. Shared Low-Speed Line Timing Input Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
LINERXDATA[86:1]	LINERXCLK[86:1]	R/F	10*	10*	15	10*

* Alternative spec: the maximum rise and fall times may be increased to 20 ns each if the minimum hold time is increased to 12 ns. The minimum setup time will remain at 15 ns.

Table 5-6. Shared Low-Speed Line Timing Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
LINETXDATA[86:1]	LINETXCLK[86:1]	R/F	–10	10

5.4 CHI Timing

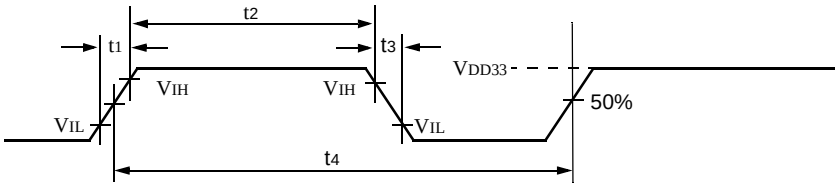
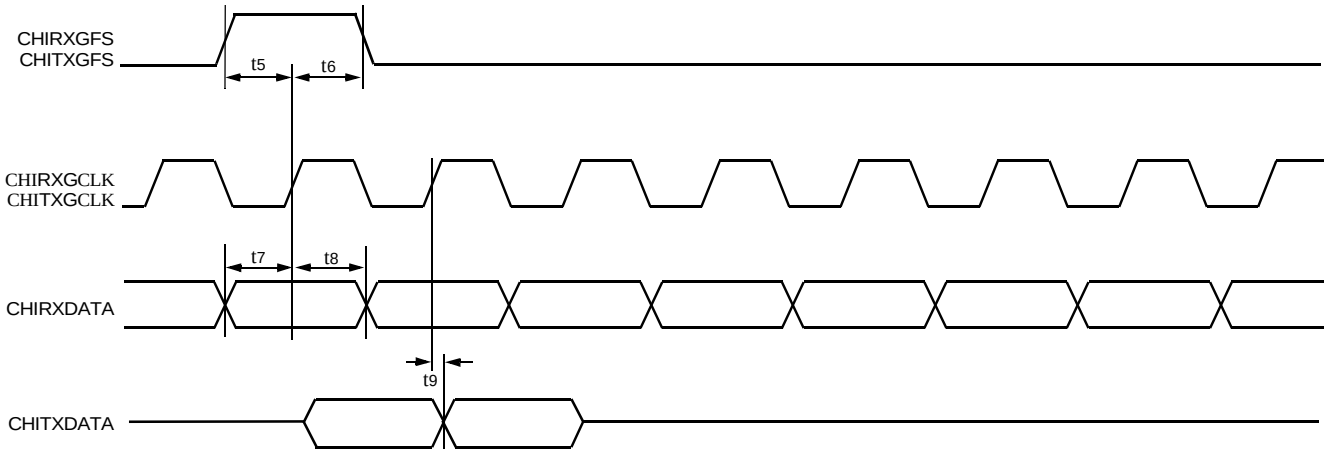


Figure 5-6. CHI Clock Timing

Table 5-7. CHIRXGCLK and CHITXGCLK Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t1	Rise Time	—	2	7	ns
t2	Width (8.192 MHz)*	48.84	—	73.24	ns
t2	Width (16.384 MHz)*	24.42	—	36.62	ns
t3	Fall Time	—	2	7	ns
t4	Period (8.192 MHz)	—	122.07	—	ns
t4	Period (16.384 MHz)	—	61.03	—	ns

* VIH to VIH or VIL to VIL.

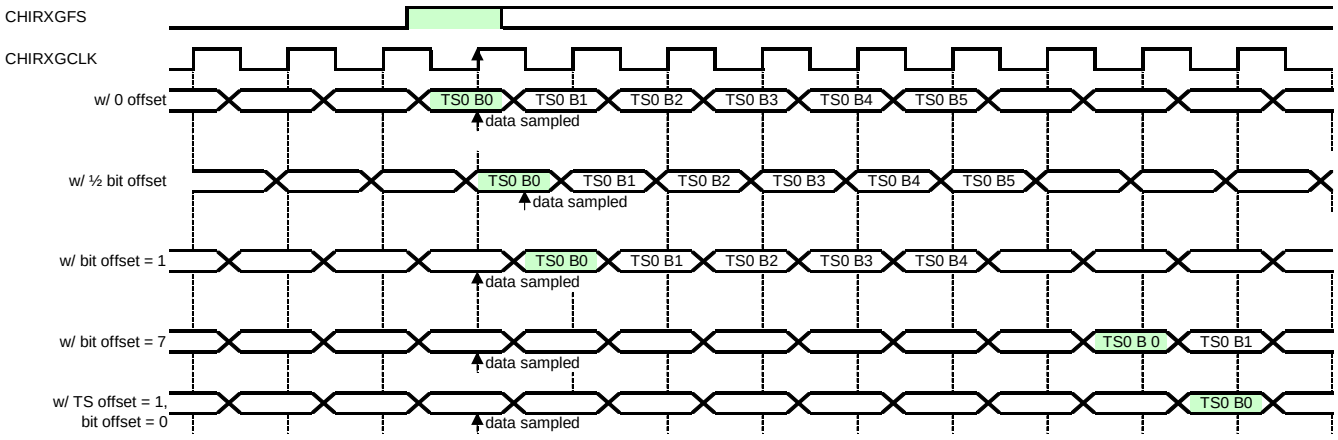


Note: This figure assumes TFRA84J13 is programmed to sample the frame sync signal on rising edge of the bit clock.

Figure 5-7. CHI Bus Timing

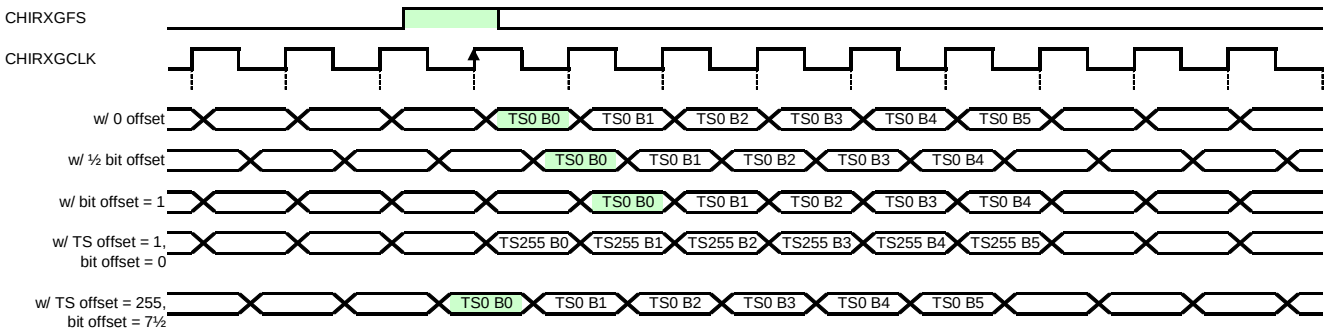
Table 5-8. CHI Interface Timing Specifications

Parameter	Description	Min	Max	Unit
t5	Frame Sync Setup Time to Active CHI Clock Edge	15	—	ns
t6	Frame Sync Hold Time from Active CHI Clock Edge	4	—	ns
t7	CHIRXDATA Setup to Active CHI Clock Edge	15	—	ns
t8	CHIRXDATA Hold Time from Active CHI Clock Edge	4	—	ns
t9	CHITXDATA Propagation Delay from Active CHI Clock Edge	4	30	ns



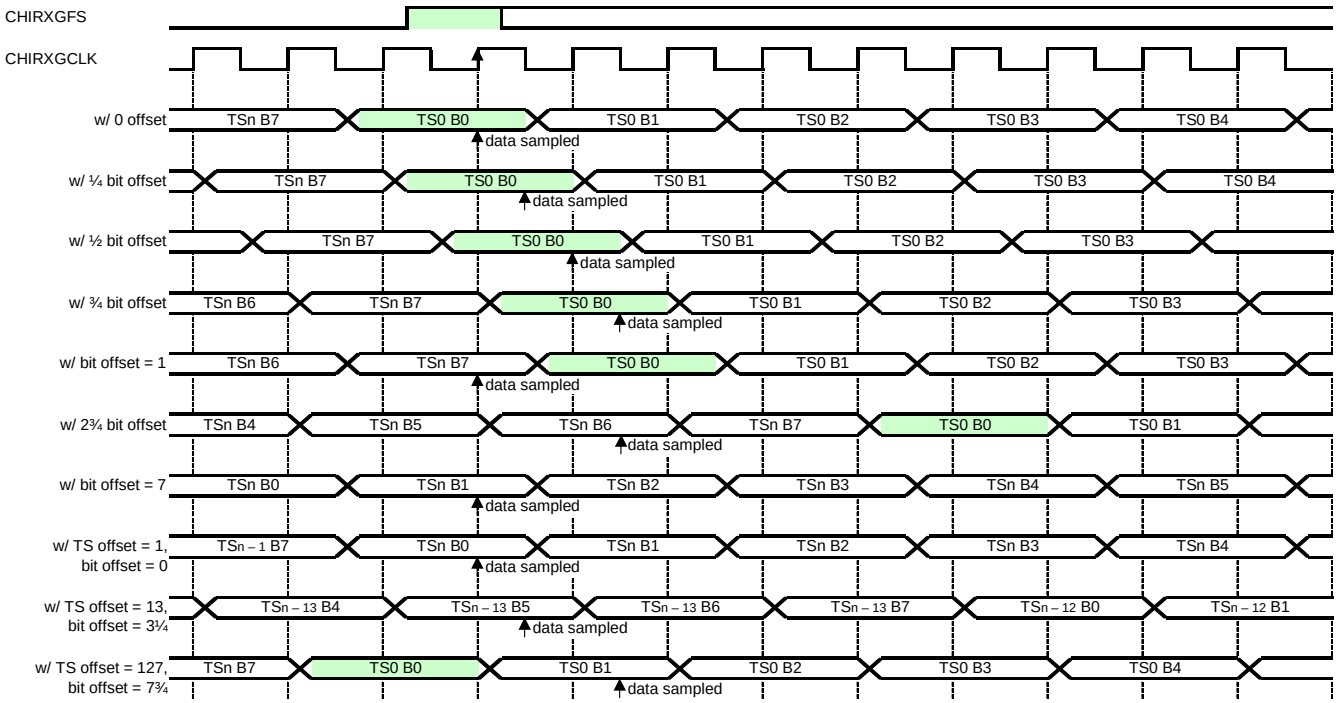
Note: For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

Figure 5-8. Typical Receive CHI Timing (Non-CMS Mode—FRM_CMS = 0)



Note: For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

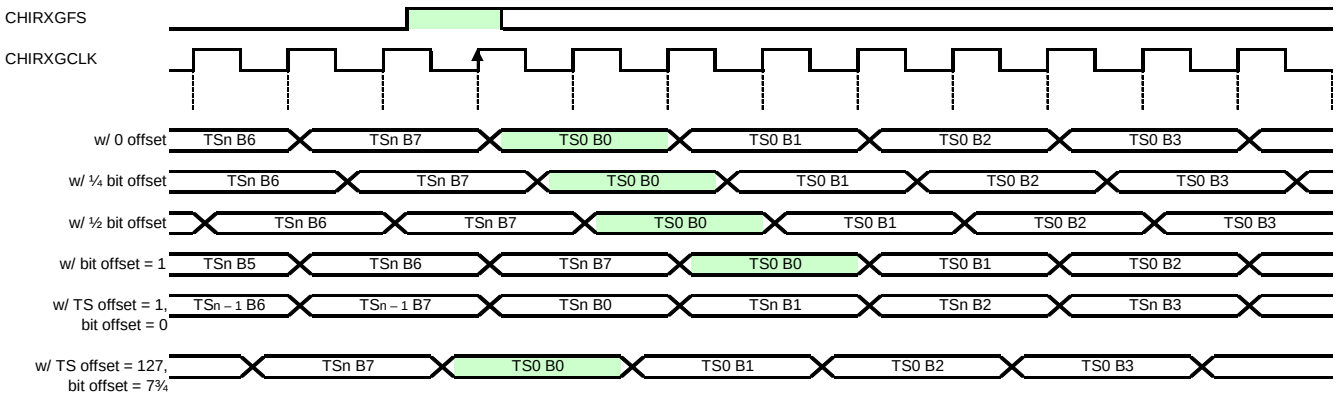
Figure 5-9. Transmit CHI Timing (Non-CMS Mode—FRM_CMS = 0)



Notes:
n = 127 at 16 MHz, n = 63 at 8 MHz.

For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

Figure 5-10. Typical Receive CHI Timing (CMS Mode—FRM_CMS = 1)



Note: For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

Figure 5-11. Transmit CHI Timing (CMS Mode—FRM_CMS = 1)

5.5 Parallel System Bus (PSB) Timing

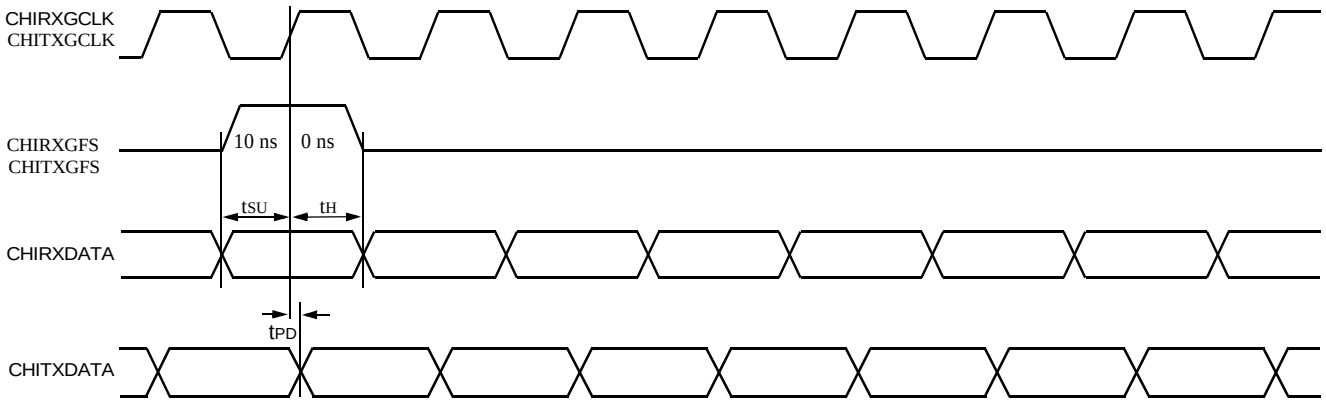


Figure 5-12. PSB Clock and Data Timing

Table 5-9. PSB Input Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
CHIRXDATA[16:1] (PSB mode)	CHIRXGCLK	R/F	10	10	10	0
CHIRXGFS (PSB mode)	CHIRXGCLK	R/F	10	10	10	0
CHITXGFS (PSB mode)	CHITXGCLK	R/F	10	10	10	0

Table 5-10. PSB Output Specifications

Name	Reference	Edge Rising (R) Falling (F)	Propagation Delay	
			Min (ns)	Max (ns)
CHITXDATA[16:1] (PSB mode)	CHITXGCLK	R/F	4	22

6 Reference Clocks

Duty cycles indicated in the following tables should be interpreted as follows: 50% ±10% means 45%—55%; 50% ± 5% means 47.5%—52.5%.

Table 6-1. Framer Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
THSCP/N	6.43	155.52 MHz	20	0.01 UIp-p or 64 psp-p or 0.001 UIrms (12 KHz—1.3 MHz)	0.4	0.4	Nom	50% ± 5%
THSCP/N	1.6	622.08 MHz	20	0.04 UIp-p or 64 psp-p 12 KHz—5 MHz	0.4 nom	0.6 max	—	50% ± 5%

Table 6-2. DS3/E3 Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
DS3DATAOUTCLK[3:1] (DS3)	22.353	44.736 MHz	20	0.05 UIp-p or 1.12 nsp-p (10 kHz—400 kHz)	5	5	Max	50% ± 10%
DS3DATAINCLK[3:1] (DS3)	22.353	44.736 MHz	20	—	3.5	2.5	Max	50% ± 5%
DS3DATAOUTCLK[3:1] (E3)	29.09	34.368 MHz	20	0.03 UIp-p or 0.87 nsp-p (100 kHz—800 kHz)	5	5	Max	50% ± 10%
DS3DATAINCLK[3:1] (E3)	29.09	34.368 MHz	20	—	3.5	2.5	Max	50% ± 5%

Table 6-3. DS1/E1 DJA Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
E1XCLK	15.25	65.536 MHz	50	0.1 UIp-p or 1.5 nsp-p (20 kHz—100 kHz)	3.5	3.5	Max	50% ± 10%
DS1XCLK	20.20	49.408 MHz	32	0.1 UIp-p or 2.0 nsp-p (10 kHz—40 kHz)	3.5	3.5	Max	50% ± 10%
E1XCLK	30.52	32.768 MHz	50	0.1 UIp-p or 3.0 nsp-p (20 kHz—100 kHz)	3.5	3.5	Max	50% ± 10%
DS1XCLK	40.40	24.704 MHz	32	0.1 UIp-p or 4.0 nsp-p (10 kHz—40 kHz)	3.5	3.5	Max	50% ± 10%

Table 6-4. M13/E13 Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
DS2AISCLK	158.42	6.312 MHz	30	—	5	5	Max	50% ± 5%
E2AISCLK	118.37	8.448 MHz	30	—	5	5	Max	50% ± 5%

Table 6-5. Microprocessor Interface Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
MPCLK (min)*	62.5	16 MHz	—	—	4	4	Min	50% ± 10%
MPCLK (max)	15.15	66 MHz	—	—	4	4	Max	50% ± 10%

* The following applies to the synchronous microprocessor mode (MPMODE pin = 1): If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. MPU maximum bus operating frequency = 1/(MPU DTN setup time + tDTNVPD). For example, an 8 ns setup time would limit MPCLK to 50 MHz for reliable DTN detection.

Table 6-6. Framer PLL Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
CLKIN_PLL	19.2	51.84 MHz	20	GR-499 and G.823	—	—	—	50% ± 10%
CHIRXGTCLK (DS1 mode)	647.66	1.544 MHz	32	GR-499	10	10	Max	50% ± 10%
CHIRXGTCLK (E1 mode)	488.28	2.048 MHz	50	G.823	10	10	Max	50% ± 10%

Table 6-7. CHI Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
CHIRXGCLK (CHI mode)	122.07	8.192 MHz	50	—	10	10	Max	50% ± 10%
CHIRXGCLK (CHI mode)	61.035	16.384 MHz	50	—	10	10	Max	50% ± 10%
CHITXGCLK (CHI mode)	122.07	8.192 MHz	50	—	10	10	Max	50% ± 10%
CHITXGCLK (CHI mode)	61.035	16.384 MHz	50	—	10	10	Max	50% ± 10%

Table 6-8. PSB Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
CHIRXGCLK (PSB mode)	51.44	19.44 MHz	20	—	10	10	Max	50% ± 10%
CHITXGCLK (PSB mode)	51.44	19.44 MHz	20	—	10	10	Max	50% ± 10%

Table 6-9. DS3/E3 Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
DS3RXCLKOUT [3:1](DS3)	22.353	44.736 MHz	20	GR-253	1.5	1.5	Nom	50% ± 5%
DS3RXCLKOUT [3:1](E3)	29.09	34.368 MHz	20	G.783	1.5	1.5	Nom	50% ± 5%

Table 6-10. Framer PLL Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
CG_PLLCLKOUT	647.66	1.544 MHz	32	GR-499	—	—	—	50% ± 5%
CG_PLLCLKOUT	488.28	2.048 MHz	50	G.823	—	—	—	50% ± 5%

Table 6-11. Shared Low-Speed Receive Line Input/Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
LINERXCLK (framer; DS1)	647.66	1.544 MHz	32	—	10	10	Max	50% ± 5%
LINERXCLK (framer; E1)	488.28	2.048 MHz	50	—	10	10	Max	50% ± 5%
LINERXCLK (M12)	647.66	1.544 MHz	32	—	10	10	Max	50% ± 5%
LINERXCLK (E12)	488.28	2.048 MHz	50	—	10	10	Max	50% ± 5%
LINERXCLK (M23)	158.42	6.312 MHz	30	—	10	10	Max	50% ± 5%
LINERXCLK (E23)	118.37	8.448 MHz	30	—	10	10	Max	50% ± 5%
LINERXCLK (DJA; DS1)	647.66	1.544 MHz	32	—	10	10	Max	50% ± 5%
LINERXCLK (DJA; E1)	488.28	2.048 MHz	50	—	10	10	Max	50% ± 5%
LINERXCLK (TPG; DS1)	647.66	1.544 MHz	32	—	10	10	Max	50% ± 5%
LINERXCLK (TPG; E1)	488.28	2.048 MHz	50	—	10	10	Max	50% ± 5%

Table 6-12. Shared Low-Speed Transmit Line Input/Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/Max	Duty Cycle
LINETXCLK (framer; DS1)	647.66	1.544 MHz	32	—	1.5	1.5	Nominal	50% ± 5%
LINETXCLK (framer; E1)	488.28	2.048 MHz	50	—	1.5	1.5	Nominal	50% ± 5%
LINETXCLK (M12)	647.66	1.544 MHz	32	—	10	10	Max	50% ± 5%
LINETXCLK (E12)	488.28	2.048 MHz	50	—	10	10	Max	50% ± 5%
LINETXCLK (M23)	158.42	6.312 MHz	30	—	10	10	Max	50% ± 5%
LINETXCLK (E23)	118.37	8.448 MHz	30	—	10	10	Max	50% ± 5%
LINETXCLK (DJA; DS1)	647.66	1.544 MHz	32	—	1.5	1.5	Nominal	50% ± 5%
LINETXCLK (DJA; E1)	488.28	2.048 MHz	50	—	1.5	1.5	Nominal	50% ± 5%
LINETXCLK (TPG; DS1)	647.66	1.544 MHz	32	—	1.5	1.5	Nominal	50% ± 5%
LINETXCLK (TPG; E1)	488.28	2.048 MHz	50	—	1.5	1.5	Nominal	50% ± 5%

Table 6-13. NSMI Input Clock Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/Max	Duty Cycle
NSMIRXCLK (framer)	19.29	51.84 MHz	20	—	3.5	3.5	Max	50% ± 5%
NSMIRXCLK (M13)	22.35	44.736 MHz	20	—	1.5	1.5	Nominal	50% ± 5%
NSMIRXCLK (E13)	29.09	34.368 MHz	20	—	1.5	1.5	Nominal	50% ± 5%

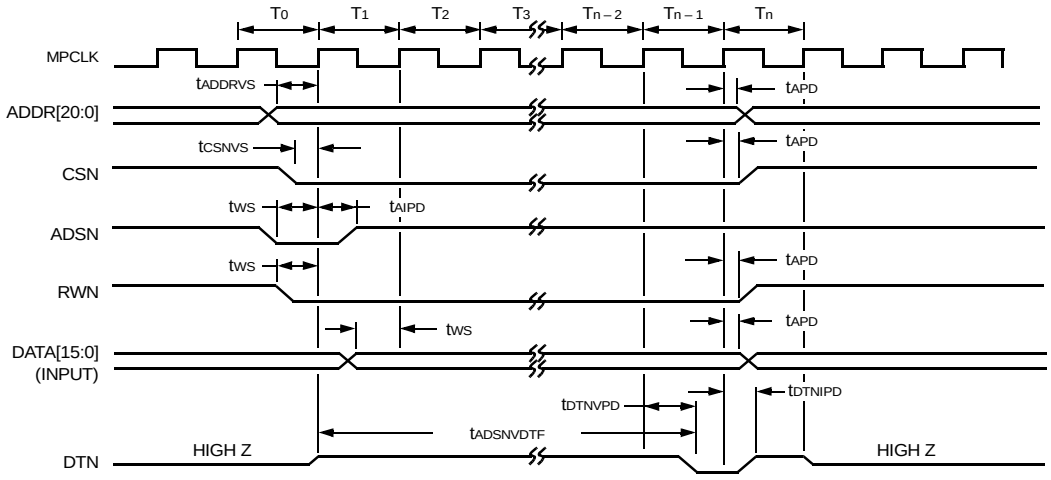
Table 6-14. NSMI Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/Max	Duty Cycle
RXDATAEN	19.29	51.84 MHz	20	—	1.5	1.5	Nominal	50% ± 5%
NSMITXCLK	19.29	51.84 MHz	20	—	1.5	1.5	Nominal	50% ± 5%

7 Microprocessor Interface Timing

7.1 Synchronous Write Mode

The synchronous microprocessor interface mode is selected when MPMODE (pin D2) = 1. In this mode, MPCLK used for the Ultraframer is the same as the microprocessor clock. Interface timing for the synchronous mode write cycle is given in Figure 7-1 and in Table 7-1, and for the read cycle in Figure 7-2 and in Table 7-2.



Notes:

MPCLK	Input clock to Ultraframer MPU block.
ADDR [20:0]	The address will be available throughout the entire cycle.
CSN (Input)	Chip select is an active-low signal.
ADSN (Input)	Address strobe is active-low. ADSN must be one MPCLK clock period wide.
RWN (Input)	The read (H) write (L) signal is always high except during a write cycle.
DATA[15:0]	Data will be available during cycle T1.
DTN (Output)	Data transfer acknowledge is active-low for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) DTN will become 3-stated when CSN is high. Typically, DTN is active four or five MPCLK cycles after ADSN is low.

Figure 7-1. Microprocessor Interface Synchronous Write Cycle—MPMODE Pin = 1

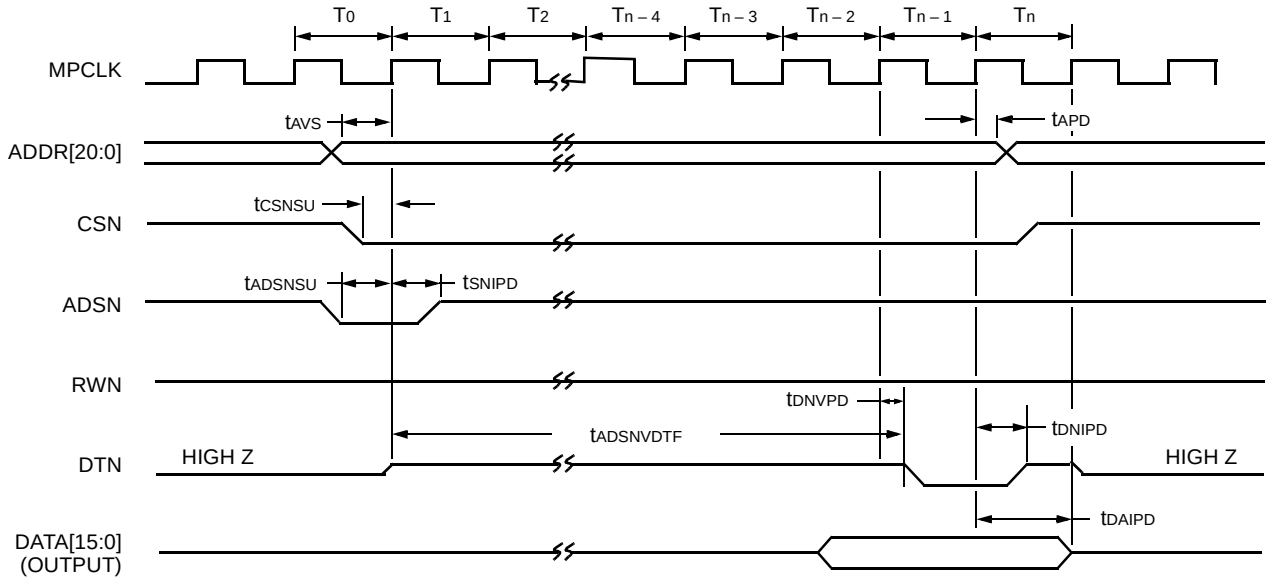
Table 7-1. Microprocessor Interface Synchronous Write Cycle Specifications

Symbol	Parameter	Setup (min)	Hold (min)	Delay (min)	Delay (max)	Unit
MPCLK	MPCLK 16 MHz Min—66* MHz Max Frequency	—	—	—	—	ns
tWS	ADSN, RWN, DATA (write) Valid to MPCLK	6.7	—	—	—	ns
tAPD	MPCLK to ADDR, RWN, DATA, CSN (write) Invalid	—	0	—	—	ns
tCSNVS	CSN Valid to MPCLK	6	—	—	—	ns
tADDRVS	ADDR Valid to MPCLK	3.5	—	—	—	ns
tAIPD	MPCLK to ADSN Invalid	—	0	—	—	ns
tDTNVPD	MPCLK to DTN Valid	—	—	2.5	12	ns
tDTNIPD	MPCLK to DTN Invalid	—	—	2.5	12	ns
TADSNVDTF	ADSN Valid to DTN Falling	—	—	—	—†	ns

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. MPU maximum bus operating frequency = 1/(MPU DTN setup time + tDTNVPD). For example, an 8 ns setup time would limit MPCLK to 50 MHz for reliable DTN detection.

† DTN fall is variable, depending on the block selected for access and in some cases the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. It should never exceed 50 MPCLK cycles. .

7.2 Synchronous Read Mode



Notes:

MPCLK	Input clock to Ultraframer MPU block.
ADDR [20:0]	The address will be available throughout the entire cycle, and must be stable before ADSN turns high.
CSN (Input)	Chip select is an active-low signal.
ADSN (Input)	Address strobe is active-low. ADSN must be one MPCLK clock period wide.
RWN (Input)	The read (H) write (L) signal is always high during the read cycle.
DTN (Output)	Data transfer acknowledge on the host bus interface is initiated on T6. This signal is active for one clock, and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) DTN will become 3-stated when CSN is high. Typically, DTN is active four or five MPCLK cycles after ADSN is low.
DATA [15:0]	Read data is stable in Tn – 1.

Figure 7-2. Microprocessor Interface Synchronous Read Cycle—MPMODE Pin = 1

Table 7-2. Microprocessor Interface Synchronous Read Cycle Specifications

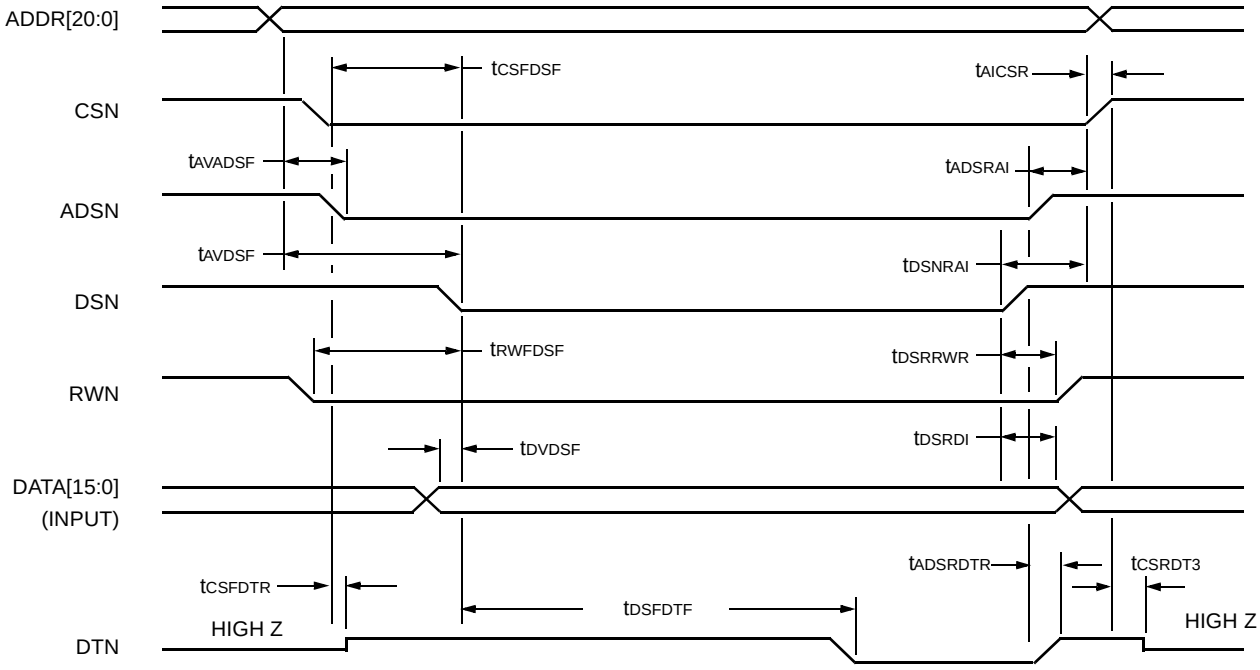
Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
MPCLK	MPCLK 16 MHz Min—66* MHz Max Frequency	—	—	—	—	ns
tAVS	ADDR Valid to MPCLK	3.5	—	—	—	ns
tAPD	MPCLK to ADDR Invalid	—	0	—	—	ns
tCSNSU	CSN Active to MPCLK	6	—	—	—	ns
tADSNSU	ADSN Valid to MPCLK	6	—	—	—	ns
tSNIPD	MPCLK to ADSN Inactive	—	0	—	—	ns
tDNVPD	MPCLK to DTN Valid	—	—	2.5	12	ns
tDNIPD	MPCLK to DTN Invalid	—	—	2.5	12	ns
tDAIPD	MPCLK to DATA 3-state	—	—	3.5	15	ns
tADSNVDTF	ADSN Valid to DTN Falling	—	—	—	—†	ns

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. MPU maximum bus operating frequency = 1/(MPU DTN setup time + tDNVPD). For example, an 8 ns setup time would limit MPCLK to 50 MHz for reliable DTN detection.

† DTN fall is variable, depending on the block selected for access and in some cases the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. It should never exceed 50 MPCLK cycles.

7.3 Asynchronous Write Mode

The asynchronous microprocessor interface mode is selected when MPMODE (pin D2) = 0. Interface timing for the asynchronous mode write cycle is given in Figure 7-3 and in Table 7-3, and for the read cycle in Figure 7-4 and in Table 7-4. Although this is an asynchronous interface, an MPCLK is still required. This clock can be different (asynchronous) from the MPU clock. Internal to the chip, RWN, ADSN, and DSN will be sampled by MPCLK.



Notes:

ADDR [20:0] Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle. ADDR must be held constant while ADSN and DSN are valid (low).

CSN (Input) Chip select is an active-low signal. CSN must be held low (active) until ADSN and DSN are deasserted.

ADSN (Input) Address strobe is active-low. ADSN must be stable for the entire period. ADSN and CSN may be connected and driven from the same source.

DSN (Input) Data strobe is active-low.

DATA [15:0] Write data is asynchronously passed from the host bus to the internal bus. Data will be available throughout the entire cycle. DATA must be held constant while DSN is valid (low).

RWN (Input) The read/write signal should be high for a read cycle and low for a write cycle. It should always be held high, except during a write cycle. RWN must be held low (write) until DSN is deasserted (high).

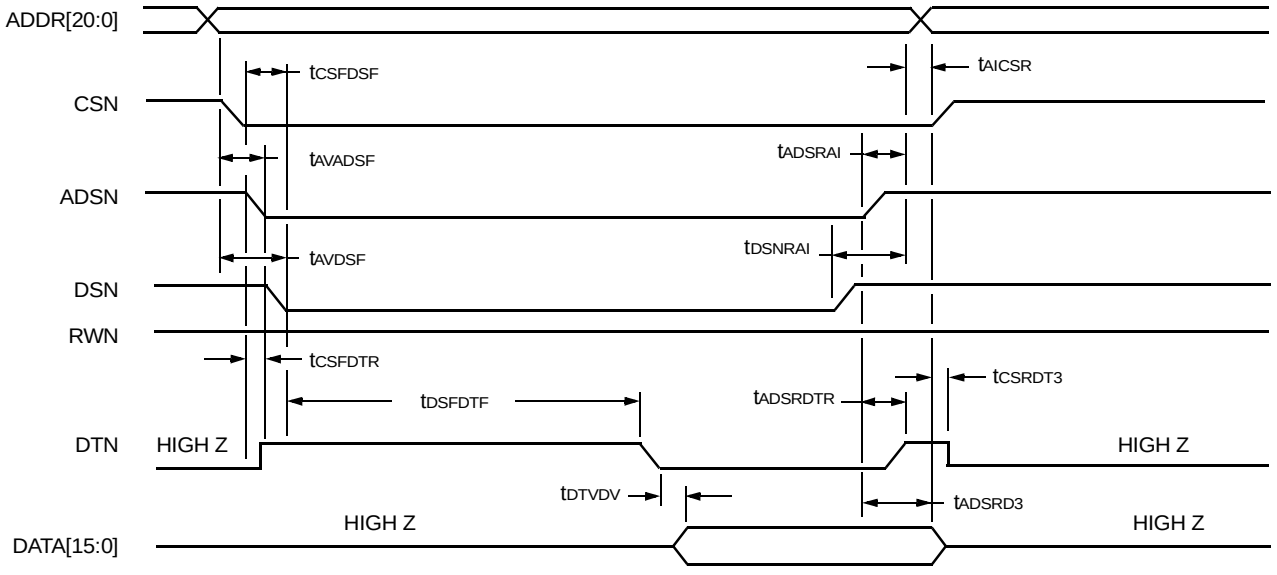
DTN (Output) Data transfer acknowledge (active-low). DTN is driven out of 3-state to inactive-high on the assertion of CSN. When the internal transaction is complete, DTN goes active-low. DTN is then driven high again when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high. DTN fall is variable, depending on the block selected for access and in some cases the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. In lab measurements, it has never exceeded 1000 ns.

Figure 7-3. Microprocessor Interface Asynchronous Write Cycle—MPMODE Pin = 0

Table 7-3. Microprocessor Interface Asynchronous Write Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
MPCLK	MPCLK 16 MHz Min—66 MHz Max Frequency	—	—	—	—	ns
t_{CSFDSF}	CSN Fall Setup and Hold to DSN Fall	0	—	—	—	ns
t_{AICSR}	CSN Rise to ADDR Invalid	—	0	—	—	ns
t_{AVADSF}	ADDR Valid Setup and Hold to ADSN Fall	1.0	—	—	—	ns
t_{ADSRAI}	ADSN Rise to ADDR Invalid	—	1.42	—	—	ns
t_{AVDSF}	ADDR Valid Setup and Hold to DSN Fall	0	—	—	—	ns
t_{DSNRAI}	DSN Rise to ADDR Invalid	—	0	—	—	ns
t_{RWFDSF}	RWN Fall Setup and Hold to DSN Fall	0	—	—	—	ns
t_{DSRRWR}	DSN Rise to RWN Rise	—	0	—	—	ns
t_{DVDSF}	DATA Valid Setup and Hold to DSN Fall	0	—	—	—	ns
t_{DSRDI}	DSN Rise to DATA Invalid	—	0	—	—	ns
t_{CSFDTR}	CSN Fall to DTN Rise	—	—	5.2	16.0	ns
t_{DSFDTF}	DSN Fall to DTN Fall	—	0	—	—	ns
$t_{ADSRDTR}$	ADSN or DSN Rise to DTN Rise	—	—	2.9	13.3	ns
t_{CSRDT3}	CSN Rise to DTN 3-state	—	—	2.9	13	ns

7.4 Asynchronous Read Mode



Notes:

ADDR [20:0] Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.
CSN (Input) Chip select is an active-low signal.
ADSN (Input) Address strobe is active-low.
DSN (Input) Data strobe is active-low.
RWN (Input) The read (H) write (L) signal is always high during a read cycle.
DTN (Output) Data transfer acknowledge (active-low). DTN is driven out of 3-state to inactive-high on the assertion of CSN. When the internal transaction is complete, DTN goes active-low. DTN is then driven high again when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high.
DATA [15:0] 16-bit data bus.

Figure 7-4. Microprocessor Interface Asynchronous Read Cycle—MPMODE Pin = 0

Table 7-4. Microprocessor Interface Asynchronous Read Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
MPCLK	MPCLK 16 MHz Min—66 MHz Max Frequency	—	—	—	—	ns
t_{CSFDSF}	CSN Fall Setup and Hold to DSN Fall	0	—*	—	—	ns
t_{AICSR}	CSN Rise to ADDR Invalid	—	0	—	—	ns
t_{AVADSF}	ADDR Valid Setup and Hold to ADSN Fall	1.0	—†	—	—	ns
t_{ADSRAI}	ADSN Rise to ADDR Invalid	—	1.42	—	—	ns
t_{AVDSF}	ADDR Valid Setup and Hold to DSN Fall	0	—†	—	—	ns
t_{DSNRAI}	DSN Rise to ADDR Invalid	—	0	—	—	ns
t_{CSFDTR}	CSN Fall to DTN Rise	—	—	5.2	16.0	ns
t_{DSFDTF}	DSN Fall to DTN Fall	—	0	—	—‡	ns
$t_{ADSRDTR}$	ADSN or DSN Rise to DTN Rise	—	—	2.9	13.3	ns
t_{CSRDT3}	CSN Rise to DTN 3-state	—	—	2.9	13.0	ns
t_{DTVDV}	DTN Valid to DATA Valid	—	—	—	0	ns
t_{ADSRD3}	ADSN Rise to DATA 3-state	—	—	2.9	14 + MPCLK§	ns

* CSN must be held low (active) until ADSN and DSN are deasserted.
† ADDR must be held constant while ADSN and DSN are valid (low).
‡ DTN fall is variable, depending on the block selected for access and in some cases, the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. It should never exceed 50 MPCLK cycles.
§ DATA[15:0] is enabled by a retimed version of the ADSN.

8 Other Timing

This interface may be used as either synchronous or asynchronous mode.

Table 8-1. General-Purpose Inputs Specifications

Name	Reference	Edge Rising/Falling	Rise Time (ns)	Fall Time (ns)	Setup (ns)	Hold (ns)
RSTN	Async	—	—	—	—	—
PMRST	Async	—	—	—	—	—
TDI and TMS	TCLK	R	5	5	19.5	6.4

Table 8-2. General-Purpose Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
TDO	TCLK	F	12.5	45

9 Hardware Design File References

(IBIS, Spice, BSDL, etc.) Available upon request.

10 909-Pin PBGA Diagram

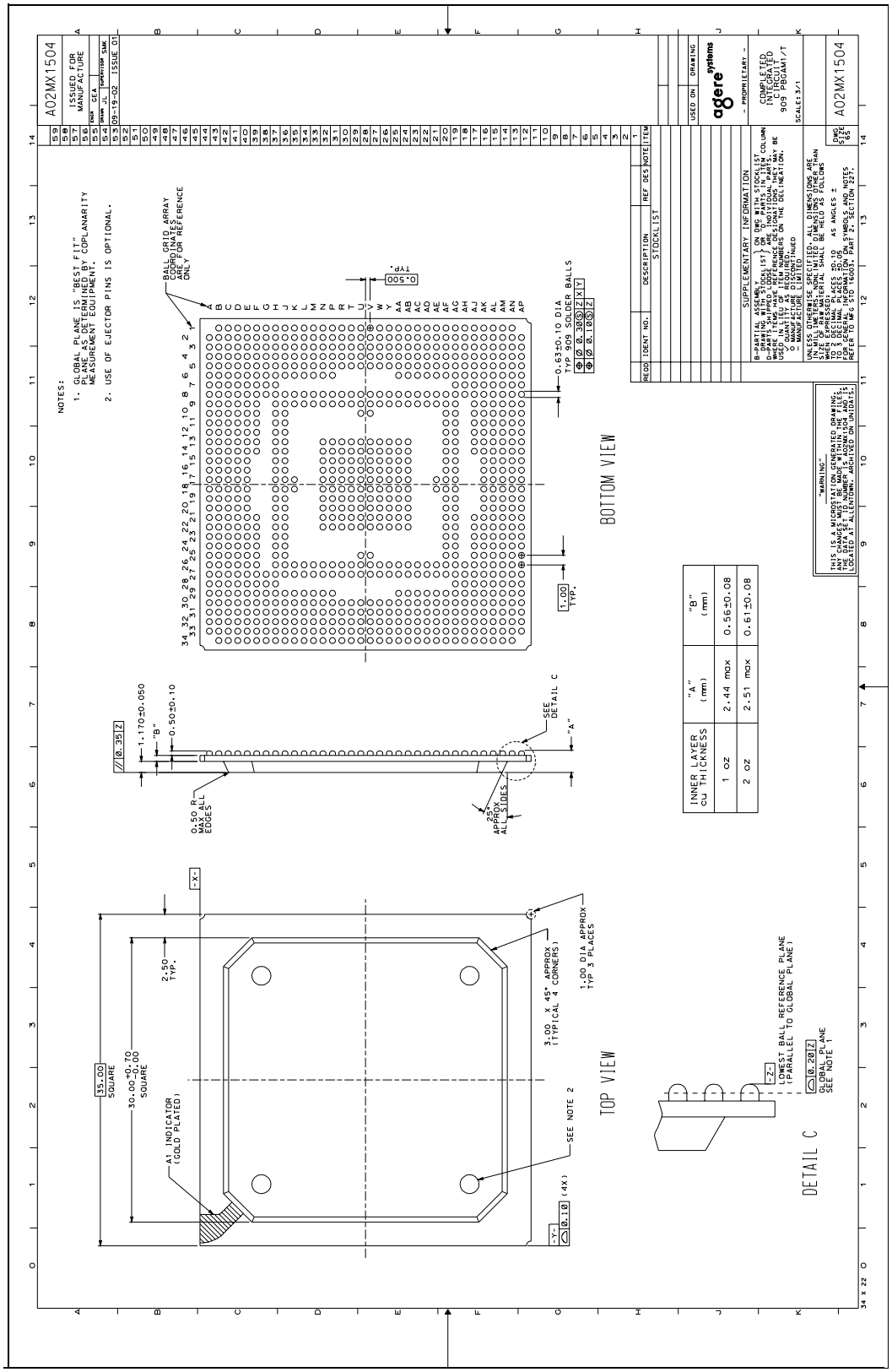


Figure 10-1. Ultraframer 909-Pin PBGA Balls and Dimensions

11 Ordering Information

Table 11-1. Ordering Information

Device	Package	Comcode
TFRA84J131BL-21	909-pin PBGA	700055303
TFRA84J131BL-3	909-pin PBGA	700052826

12 Glossary

AIS	Alarm indication signal
AMI	Alternate mark inversion
APS	Automatic protection switch
ASM	Associated signaling mode
BER	Bit error rate
BOM	Bit-oriented message
BPV	Bipolar violation
B8ZS	Binary 8 zero code suppression
CCI	Common channel signaling
CDR	Clock and data recovery
CHI	Concentrated highway interface
CMI	Coded mark inversion
CRC	Cyclic redundancy check
CRV	Coding rule violation
DACS	Digital access cross connects
DJA	Digital jitter attenuation
ESF	Extended superframe
EXZ	Excessive zeros
FCS	Frame check sequence
FDL	Facility data link
FEAC	Far-end alarm and control
FEBE	Far-end block error
HDB3	High-density bipolar of order three
HDLC	High-level data link control
LIU	Line interface unit
LOC	Loss of clock
LOF	Loss of frame
LOS	Loss of signal
LOPOH	Low-order path overhead
MCDR	Mate clock and data recovery
MRXC	Multirate cross connect
NSMI	Network serial multiplexed interface
OOF	Out of frame
PBGA	Pin ball grid array
POAC	Path overhead access channel
PRBS	Pseudorandom bit sequence
PRM	Performance report message
QRSS	Quasirandom signal source
RAI	Remote alarm indicator
RDI	Remote defect indication
RPOAC	Receive path overhead access channel
REI	Remote error indication
SDH	Synchronous digital hierarchy
SEF	Severely errored frame
SONET	Synchronous optical network
TCM	Tandem connection monitoring
TOAC	Transport overhead access channels
UPSR	Unidirectional path switch ring

13 Change History

On page 47, the second paragraph was deleted.

Other changes that were made to this document (since revision 4) are listed in Table 13-1.

Table 13-1. Changes

Change	Change	Change	Change	Change	Change	Change	Change	Change	Change
page 21	page 24	page 31	page 42	page 45	page 46	page 47	page 48	page 49	page 52

13.1 Navigating Through an *Adobe Acrobat* Document

If the reader displays this document in *Acrobat Reader*, clicking on any blue entry in the text will bring the reader to that reference point. Clicking on the back arrow in the toolbar of the *Acrobat Reader* (Go to previous View) will bring the reader back to the starting point.

For example, clicking on page 21 in Table 13-1 will bring the reader to page 21 of this document, which is the first change. Clicking on the back arrow in *Acrobat Reader*, will bring the reader back to this page.

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