

**LVDS Dual 2x2 Crosspoint/Repeater Switch**
**Features**

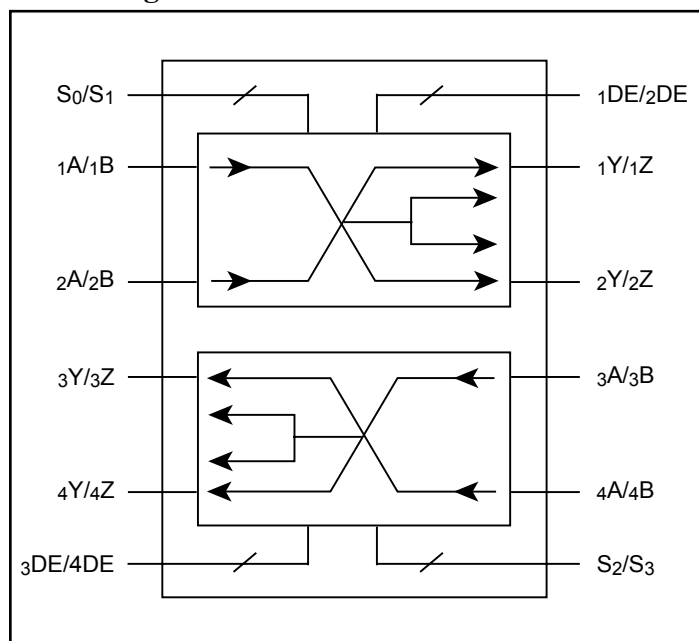
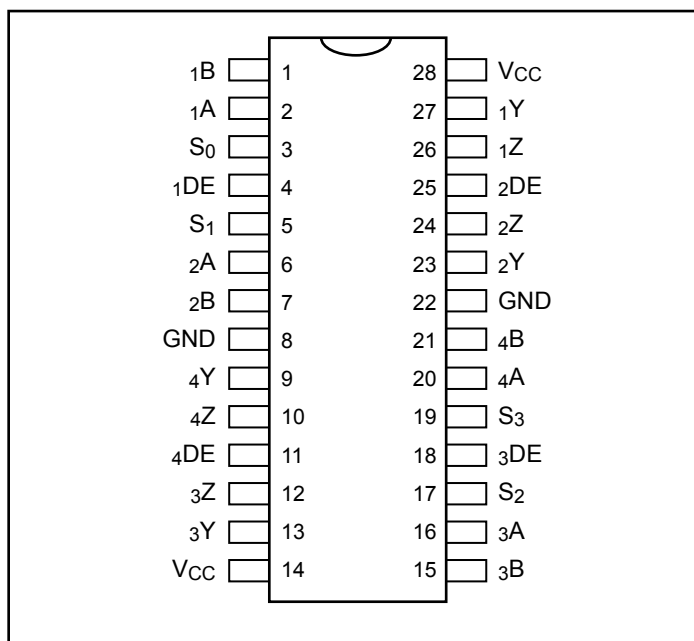
- Dual 2x2 Crosspoint/Repeater Switch
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995
- Designed for Signaling Rates up to 650 Mbit/s (325 MHz)
- Operates from a 3.3V Supply:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Low Voltage Differential Signaling with Output Voltages of  $\pm 350\text{mV}$  into:
  - $100\Omega$  load (PI90LV024)
  - $50\Omega$  load Bus LVDS Signaling (PI90LVB024)
- Accepts  $\pm 350\text{mV}$  differential inputs
- Wide common mode input range:  $0.2\text{V}$  to  $2.7\text{V}$
- Output drivers are high impedance when disabled or when  $V_{CC} \leq 1.5\text{V}$
- Inputs are open, short, and terminated fail safe
- Propagation Delay Time:  $3.5\text{ns}$
- ESD protection is  $10\text{kV}$  on bus pins
- Bus Pins are High Impedance when disabled or with  $V_{CC}$  less than  $1.5\text{V}$
- TTL Inputs are  $5\text{V}$  Tolerant
- Power Dissipation at  $400\text{Mbit/s}$  of  $250\text{mW}$
- Packaging (Pb-free & Green Available):
  - 28-pin QSOP (Q)
  - 28-pin TSSOP (L)

**Description**

The PI90LV024 and PI90LVB024 are monolithic dual 2x2 asynchronous crosspoint/repeater switches. The crosspoint function is based on a multiplexer tree architecture. Each 2x2 switch can be considered as a pair of 2:1 multiplexers that share the same inputs. The signal path through each switch is fully differential with minimal propagation delay. The signal path is unregistered, so no clock is required for the data inputs. The signal line drivers and receivers use Low Voltage Differential Signaling (LVDS) to achieve signaling rates as high as 650 Mbps.

The LVDS standard provides a minimum differential output voltage magnitude of  $247\text{mV}$  into a  $100\Omega$  load and receipt of  $100\text{mV}$  signals with up to  $1\text{V}$  of ground potential difference between a transmitter and receiver. The PI90LVB024 doubles the output drive current to achieve Bus LVDS signaling levels with a  $50\Omega$  load.

The intended application of these devices is for loop-through and redundant channel switching for both point-to-point base-band (PI90LV024) and multipoint (PI90LVB024) data transmissions over controlled impedance media. The package pin assignments enables easy routing for applications requiring signal feedback.

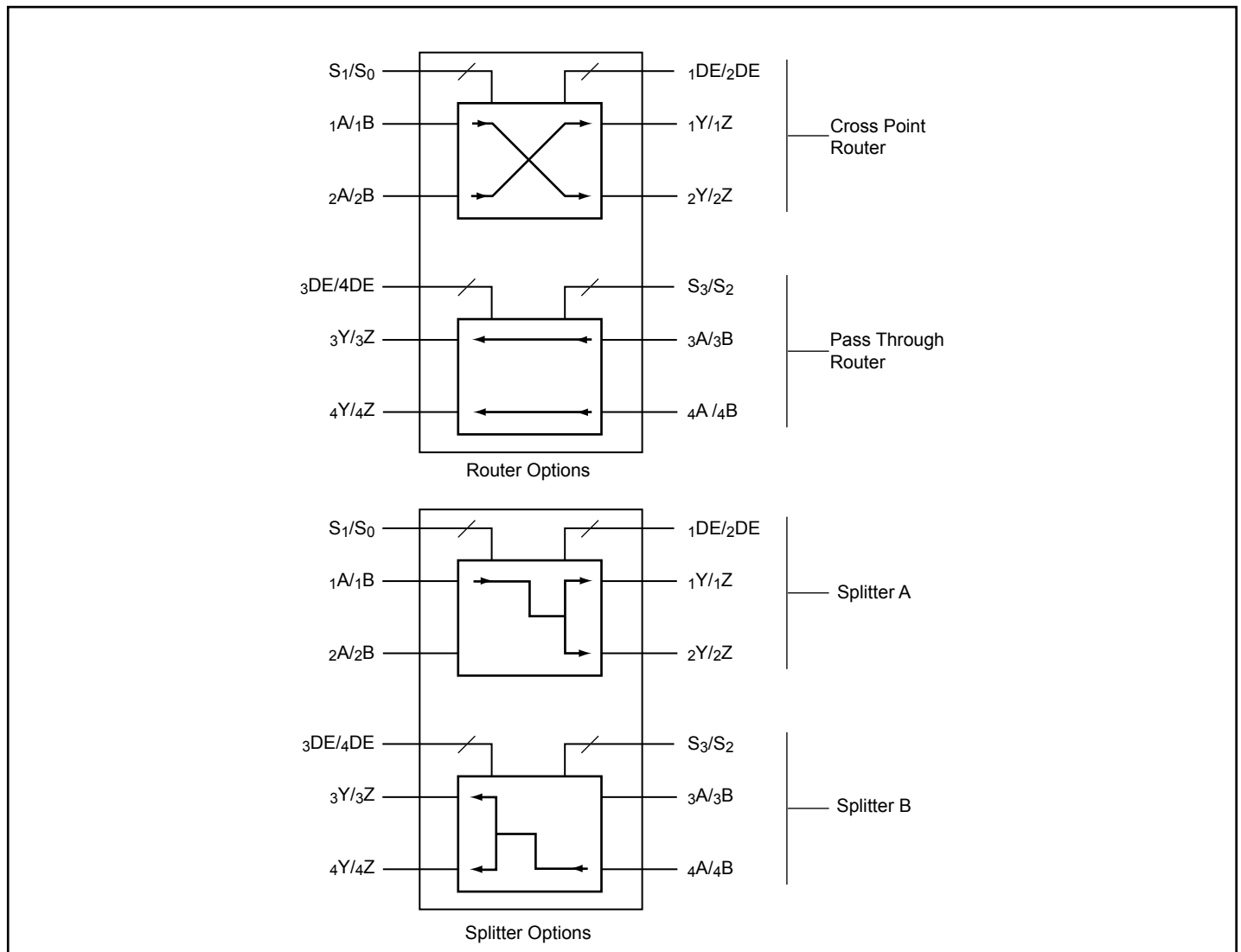
**Block Diagram**

**Pin Configuration**


**MUX Truth Table**

Input		Output		Function
S <sub>3</sub> , S <sub>1</sub>	S <sub>2</sub> , S <sub>0</sub>	<sub>1</sub> Y/ <sub>1</sub> Z - <sub>3</sub> Y/ <sub>3</sub> Z	<sub>2</sub> Y/ <sub>2</sub> Z - <sub>4</sub> Y/ <sub>4</sub> Z	
0	0	<sub>1</sub> A/ <sub>1</sub> B - <sub>3</sub> A/ <sub>3</sub> B	<sub>1</sub> A/ <sub>1</sub> B - <sub>3</sub> A/ <sub>3</sub> B	Splitter
0	1	<sub>2</sub> A/ <sub>2</sub> B - <sub>4</sub> A/ <sub>4</sub> B	<sub>2</sub> A/ <sub>2</sub> B - <sub>4</sub> A/ <sub>4</sub> B	Splitter
1	0	<sub>1</sub> A/ <sub>1</sub> B - <sub>3</sub> A/ <sub>3</sub> B	<sub>2</sub> A/ <sub>2</sub> B - <sub>4</sub> A/ <sub>4</sub> B	Router
1	1	<sub>2</sub> A/ <sub>2</sub> B - <sub>4</sub> A/ <sub>4</sub> B	<sub>1</sub> A/ <sub>1</sub> B - <sub>3</sub> A/ <sub>3</sub> B	Router

**Note:**

- Setting *n*DE to 0 will set Output *n*Y/*n*Z to High Impedance.



**Figure 1. Possible Signal Routing**

### Absolute Maximum Ratings Over Operating Free-Air Temperature<sup>(1)</sup>

Supply Voltage Range, $V_{CC}^{(2)}$ .....	-0.5V to 4V
Voltage Range (DE, S <sub>0</sub> , S <sub>1</sub> ).....	-0.5 to 6V
Input Voltage Range, .....	$V_I$ (A or B)-0.5V to $V_{CC} + 0.5V$
Electrostatic Discharge: A, B, Y, Z, and GND <sup>(3)</sup> .....	Class 3, A: 16kV, B:600V
All Pins .....	Class 3, A: 7kV, B:500V
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature 1, 6 mm (1/16 inch) from case for 10 seconds.....	260°C

**Notes:**

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.
2. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
3. Tested in accordance with MIL-STD-883C Method 3015.7

### Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
$V_{CC}$	Supply Voltage	3.0	3.3	3.6	V
$V_{IH}$	High-Level Input Voltage	2			
$V_{IL}$	Low-Level Input Voltage			0.8	
$ V_{ID} $	Magnitude of Differential Input	0.1		0.6	
$V_{IC}$	Common-Mode Input Voltage (see fig 2)	$\frac{ V_{ID} }{2}$		$2.4 - \frac{ V_{ID} }{2}$	
				$V_{CC} - 0.8$	
$T_A$	Operating Free-air temperature	-40		85	°C

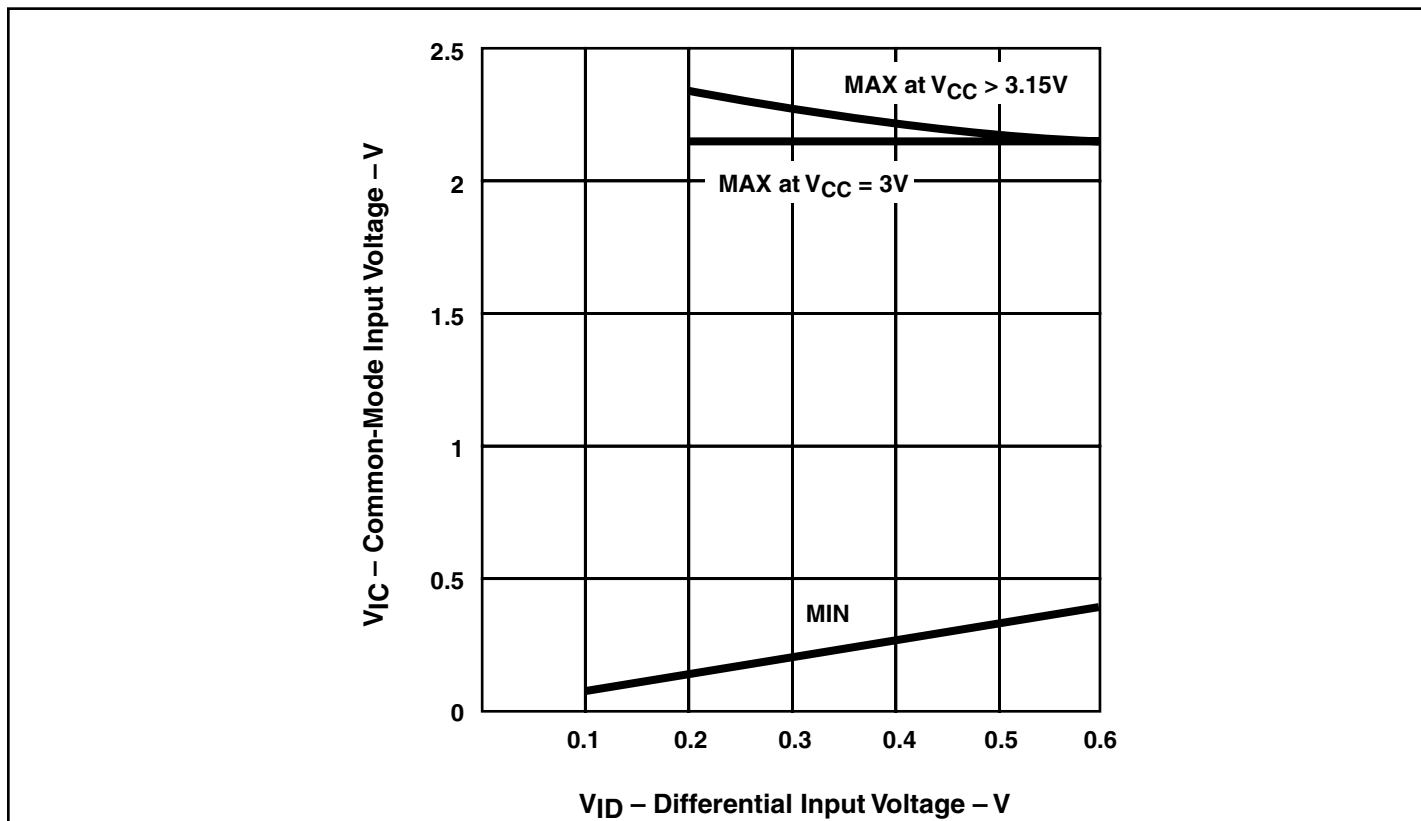


Figure 2. Common-Mode Input Voltage vs. Differential Voltage

**Receiver Electrical Characteristics Over Recommended Operating Conditions** (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Units
$V_{ITH+}$	Positive-going differential input voltage threshold	$V_{CM} = 1.2V$			100	mV
$V_{ITH-}$	Negative-going differential input voltage threshold		-100			
$I_I$	Input Current (A or B inputs)	$V_I = 0V$	-2		-20	$\mu A$
		$V_I = 2.4V$	-1.2			
$I_{I(OFF)}$	Power-off Input current (A or B inputs)	$V_{CC} = 0V$			20	

**Receiver / Driver Electrical Characteristics Over Recommended Operating Conditions**

(unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max	Units
$V_{OD}$	Differential Output Voltage Magnitude	$R_L = 100\Omega$ (LV024)	See Fig. 3	247	440	590	mV
$\Delta V_{OD}$	Change in Differential Output Voltage Magnitude between Logic States			-50		50	
$V_{OC(SS)}$	Steady-State Common-Mode Output Voltage	$R_L = 100\Omega$ (LVB024)	See Fig. 4	1.062		1.375	V
$\Delta V_{OC(SS)}$	Change in Steady-State Common-Mode Output Voltage between Logic States			-50	3	50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage					150	
$I_{CC}$	Supply Current	No Load			16	24	mA
		$R_L = 100\Omega$ (LV024)			26	40	
		$R_L = 50\Omega$ (LVB024)			42	54	
		Both Channels Disabled			6	12	
$I_H$	High-Level Input Current	DE	$V_{IH} = 5V$			40	nA
		$S_1, S_2, S_3, S_4$				-3	$\mu A$
$I_L$	Low-Level Input Current	DE	$V_{IL} = 0.8V$			-20	nA
		$S_1, S_2, S_3, S_4$				10	$\mu A$
$I_{OS}$	Short Circuit Output Current	$V_{OY}$ or $V_{OZ} = 0V$				-10	mA
		$V_{OD} = 0V$				-10	
$I_{OZ}$	High-Impedance Output Current	$V_{OD} = 600mV$			1.5	$\pm 25$	nA
		$V_O = 0V$ or $V_{CC}$			1.5	$\pm 25$	
$I_{O(OFF)}$	Power-Off Output Current	$V_{CC} = 0V, V_O = 3.6V$			1.5	$\pm 40$	
$C_{IN}$	Input Capacitance				3		pF
		$S_0 - S_3, 1DE - 4DE$			8		

**Note:**

- All typical values are at 25°C and with a 3.3V supply

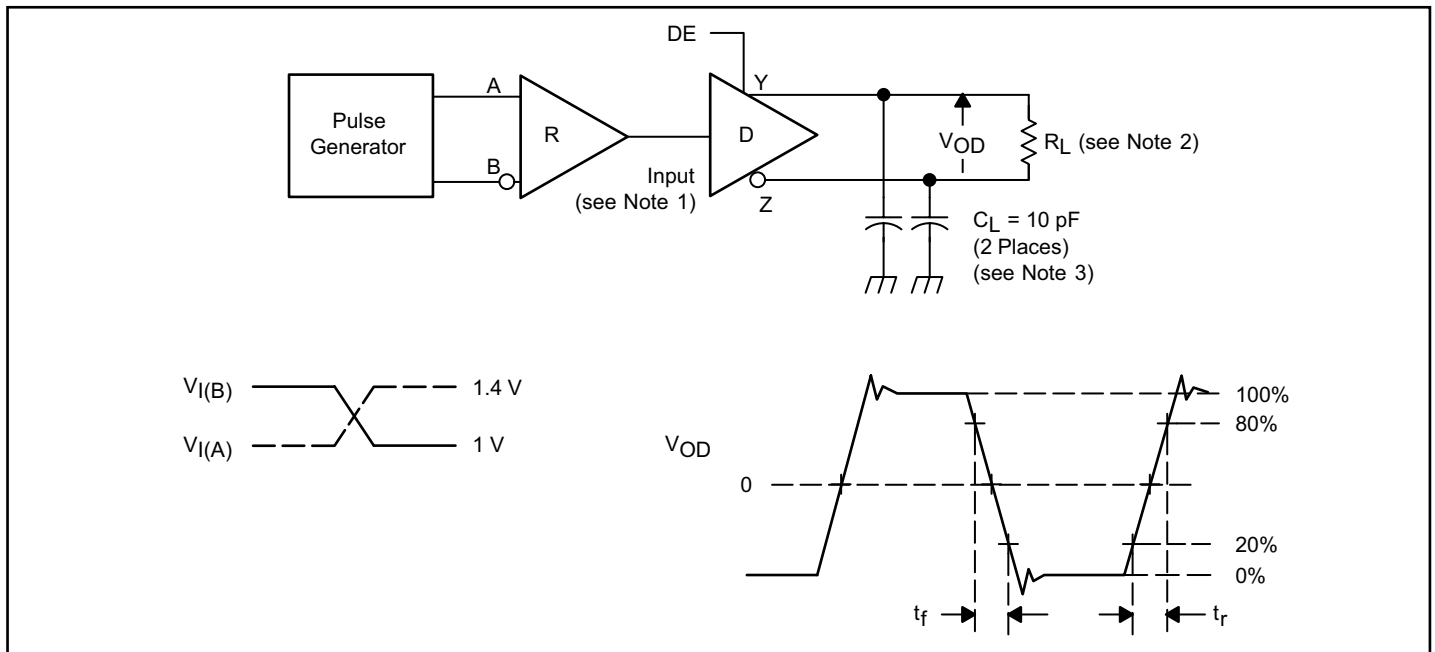
**Differential Receiver to Driver Switching Characteristics Over Recommended Operating Conditions**  
(unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units	
t <sub>PLH</sub>	Differential propagation delay, low-to-high	C <sub>L</sub> = 10pF (see fig. 5)		4.0	6.0	ns	
t <sub>PHL</sub>	Differential propagation delay, high-to-low			4.0	6.0		
t <sub>sk(p)</sub>	Pulse skew (   t <sub>PHL</sub> - t <sub>PLH</sub>   )			0.5	-		
t <sub>r</sub>	Transition, low-to-high		LV024		1.0		1.5
			LVB024		0.8		1.3
t <sub>f</sub>	Transition, high-to-low		LV024		1.0		1.5
		LVB024		0.8	1.3		
t <sub>PHZ</sub>	Propagation delay time, high-level to high impedance output	See fig. 6		4.0	10		
t <sub>PLZ</sub>	Propagation delay time, low-level to high impedance output			4.3	10		
t <sub>PZH</sub>	Propagation delay time, high-level to high impedance output			3.0	10		
t <sub>PZL</sub>	Propagation delay time, high-level to low impedance output			2.0	10		
t <sub>PHL_R1_DX</sub>	Channel-to-channel skew, receiver to driver <sup>(2)</sup>			95		ps	
t <sub>PLH_R1_DX</sub>				95			
t <sub>PHL_R2_DX</sub>				95			
t <sub>PLH_R2_DX</sub>				95			

**Notes:**

1. All typical values are at 25°C and with a 3.3V supply
2. These parametric values are measured over supply voltage and temperature ranges recommended for the device

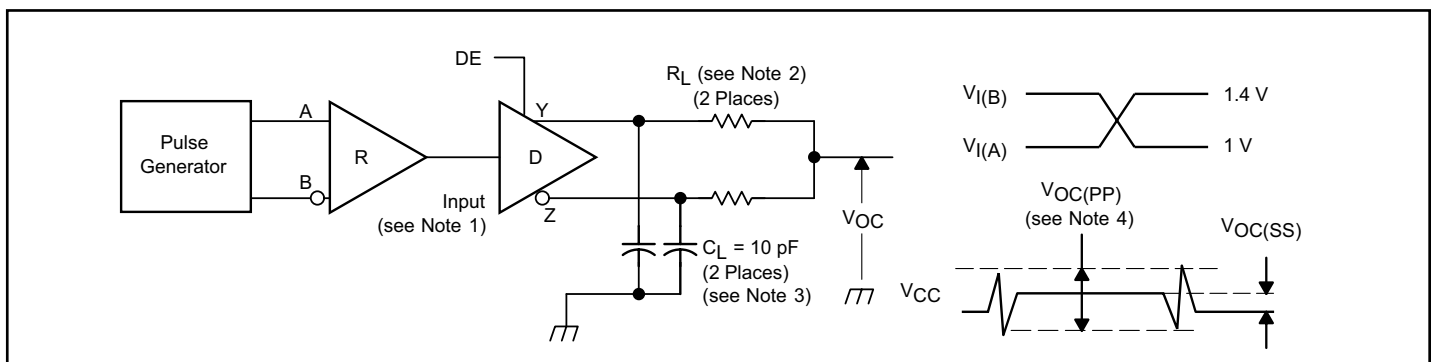
### Parameter Measurement Information



**Figure 3. Test Circuit and Voltage Definitions for the Differential Output Signal**

**Notes:**

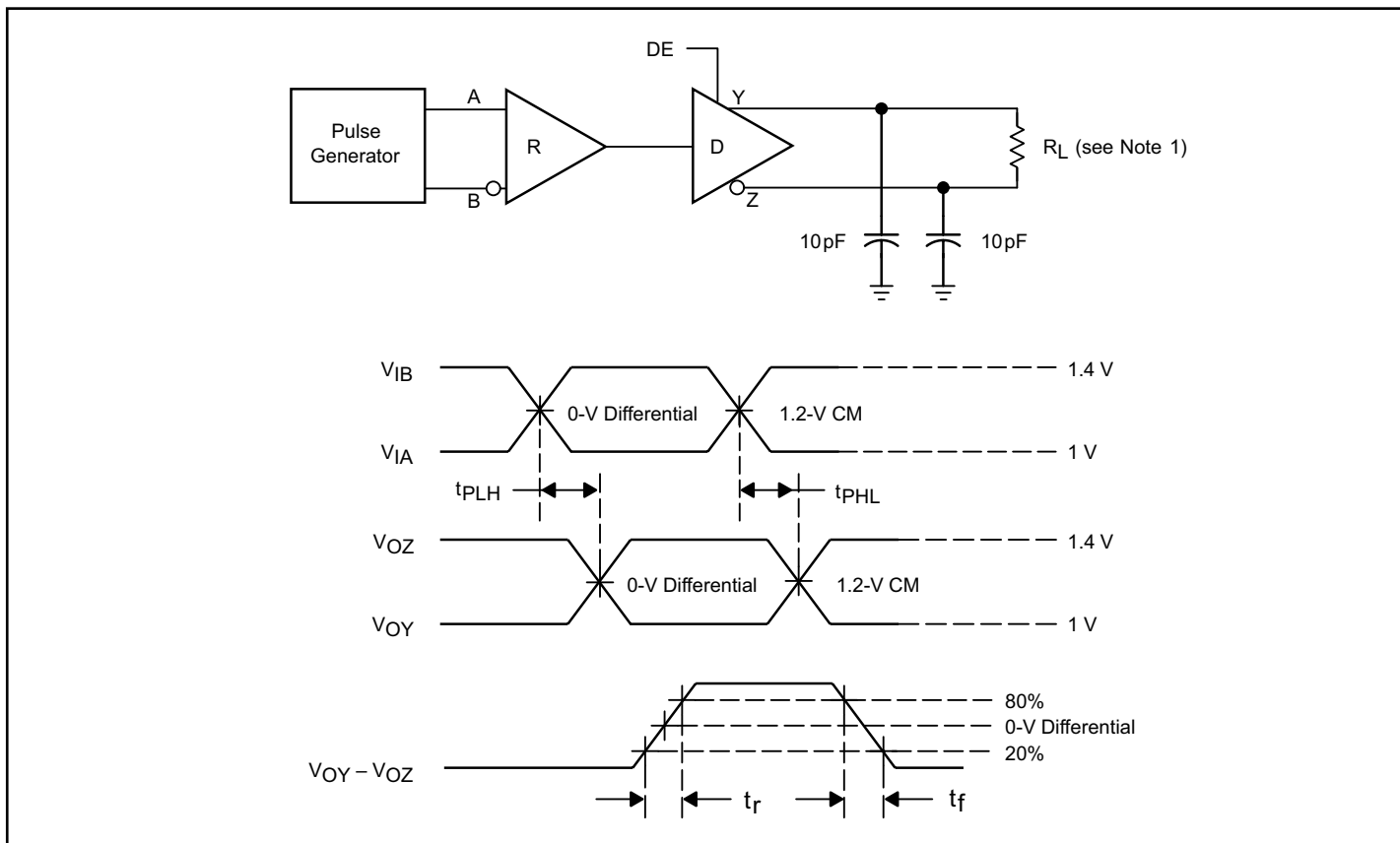
1. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1\text{ns}$ , pulse repetition rate (PRR) - 50 Mpps, pulse width =  $10 \pm 0.2\text{ns}$ .
2.  $R_L = 100\Omega$  or  $50\Omega \pm 1\%$ .
3.  $C_L$  includes instrumentation and fixture capacitance within 6mm of the D.U.T.
4. The measurement of  $V_{OC(PP)}$  is made on test equipment with a  $-3\text{dB}$  bandwidth of at least 300 MHz.



**Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**

**Notes:**

1. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1\text{ns}$ , pulse repetition rate (PRR) - 50 Mpps, pulse width =  $10 \pm 0.2\text{ns}$ .
2.  $R_L = 100\Omega$  or  $50\Omega \pm 1\%$ .
3.  $C_L$  includes instrumentation and fixture capacitance within 6mm of the D.U.T.
4. The measurement of  $V_{OC(PP)}$  is made on test equipment with a  $-3\text{dB}$  bandwidth of at least 300 MHz.

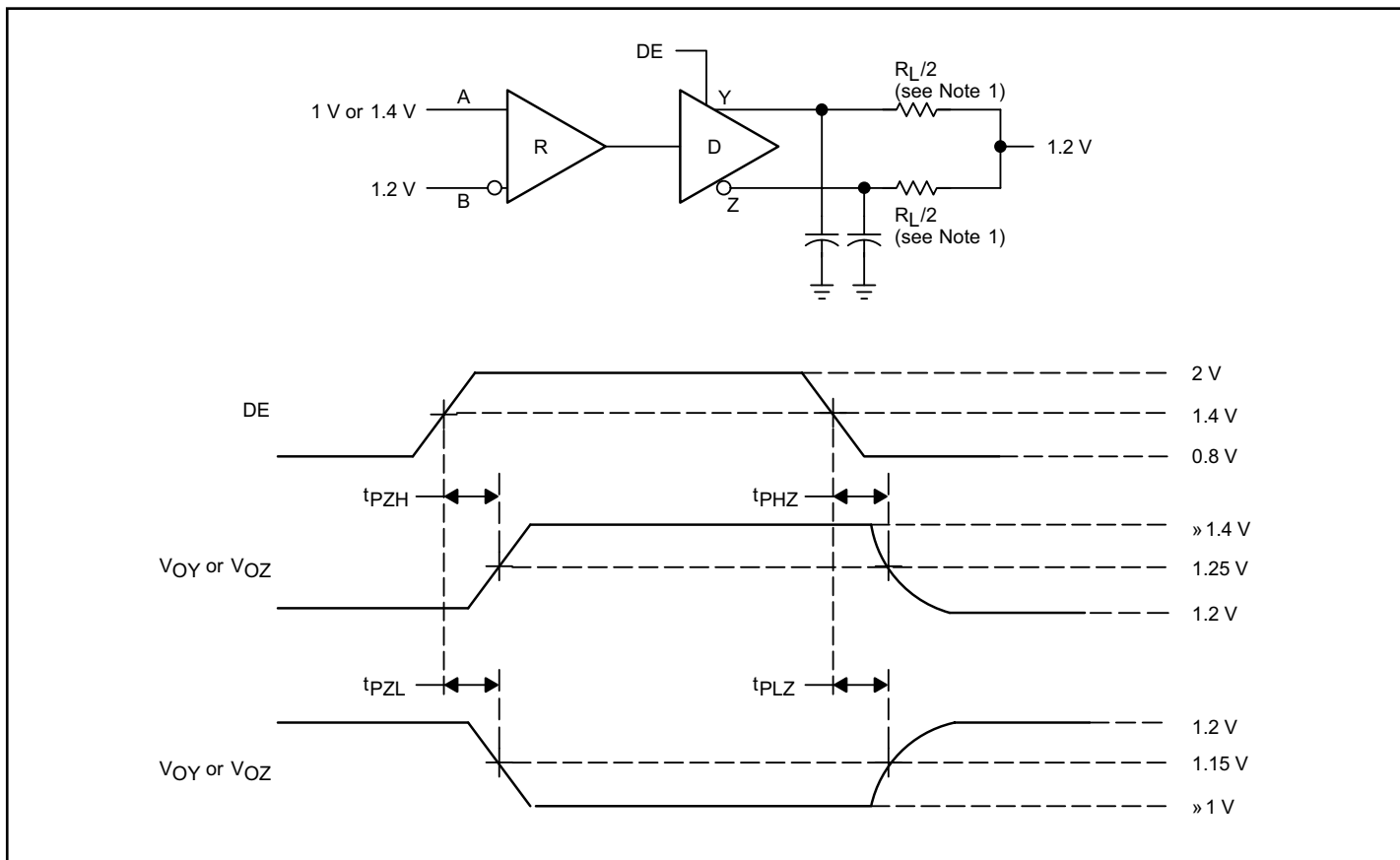


**Figure 5. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms**

**Notes:**

1.  $R_L = 100\Omega$  or  $50\Omega \pm 1\%$
2. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PPR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns.

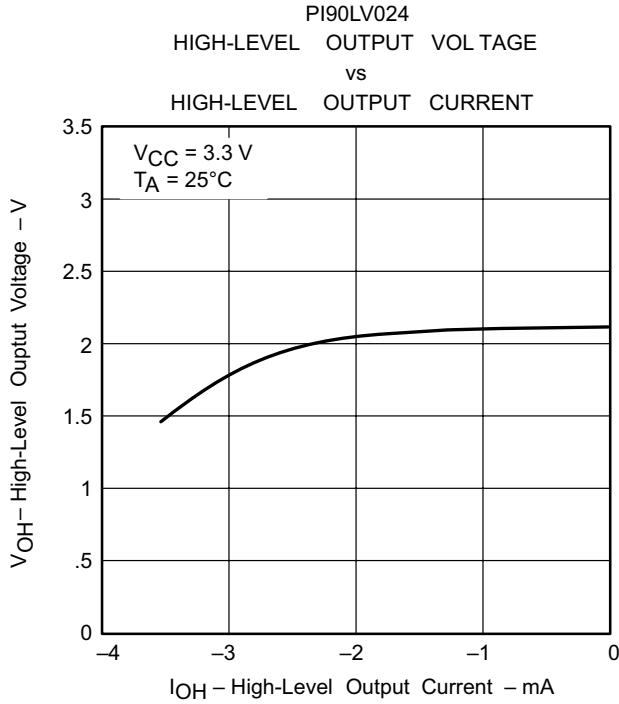
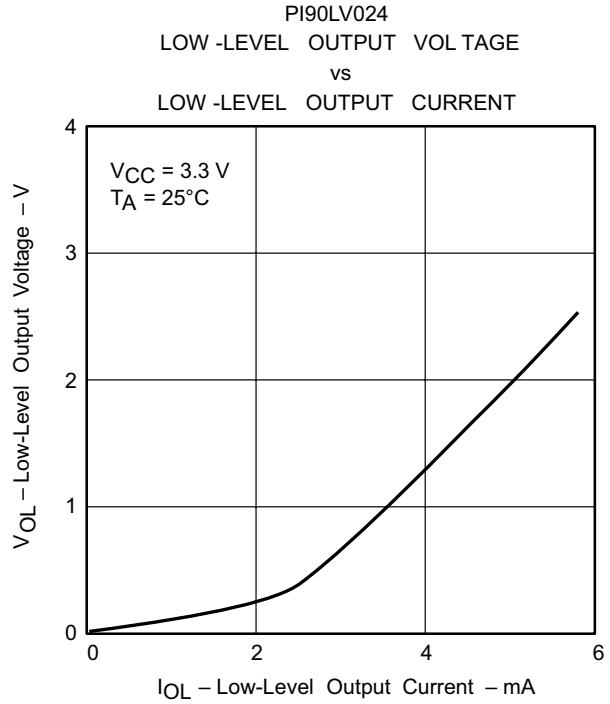
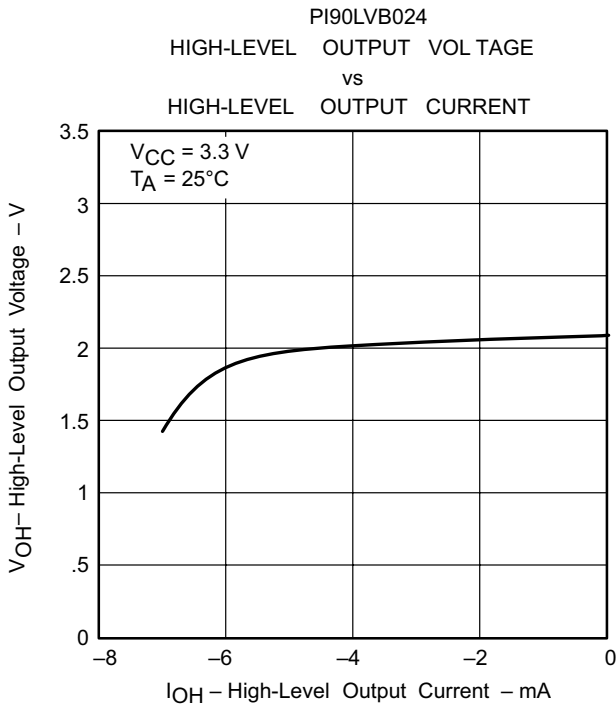
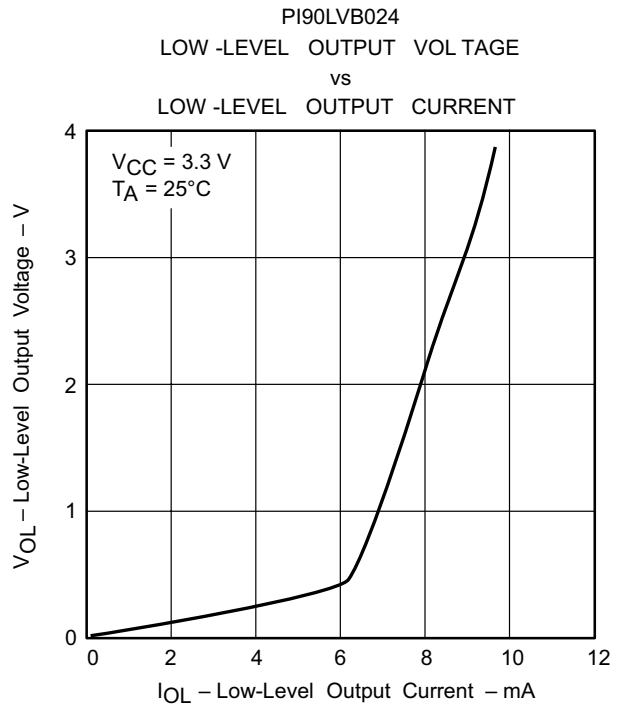




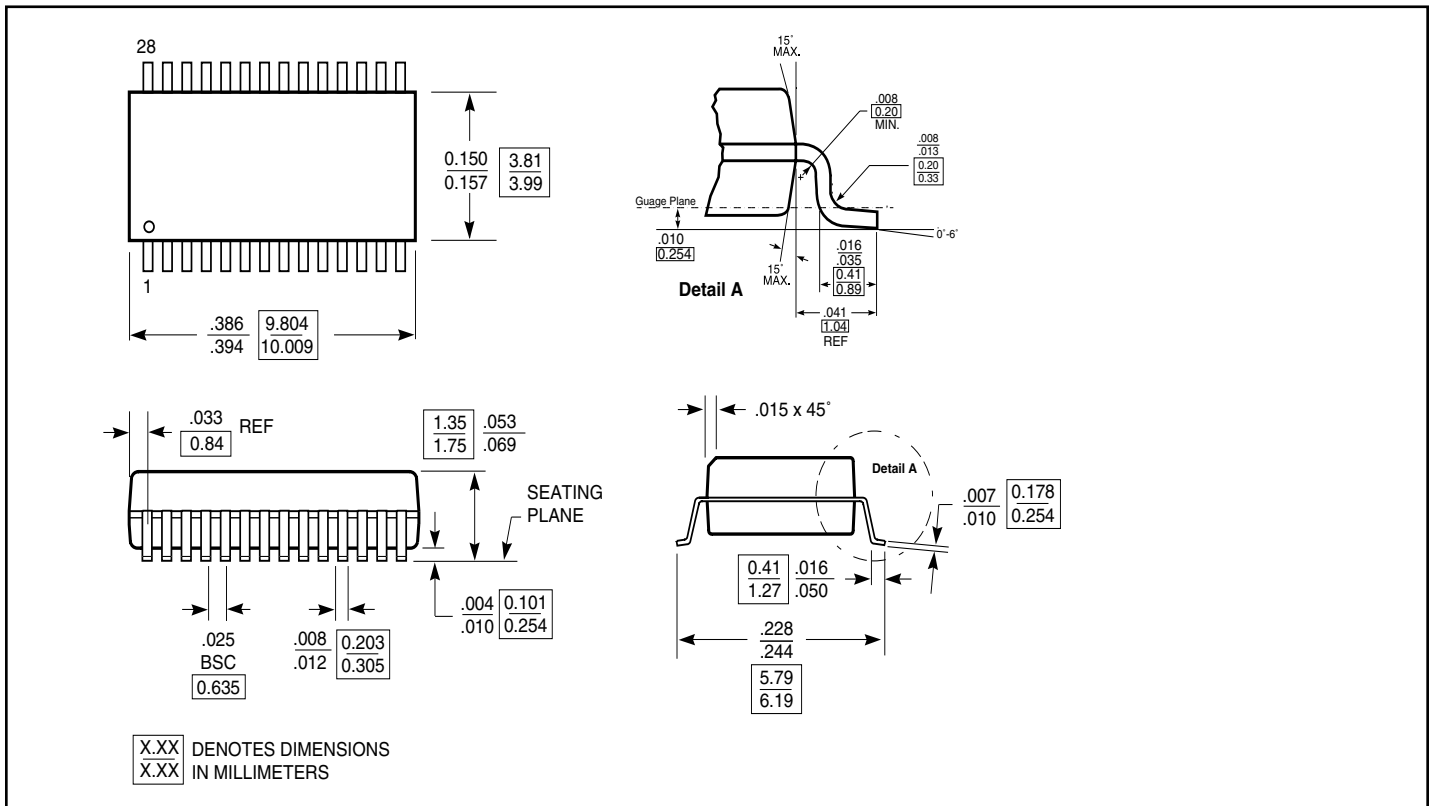
**Figure 6. Enable and Disable Timing Circuit**

**Notes:**

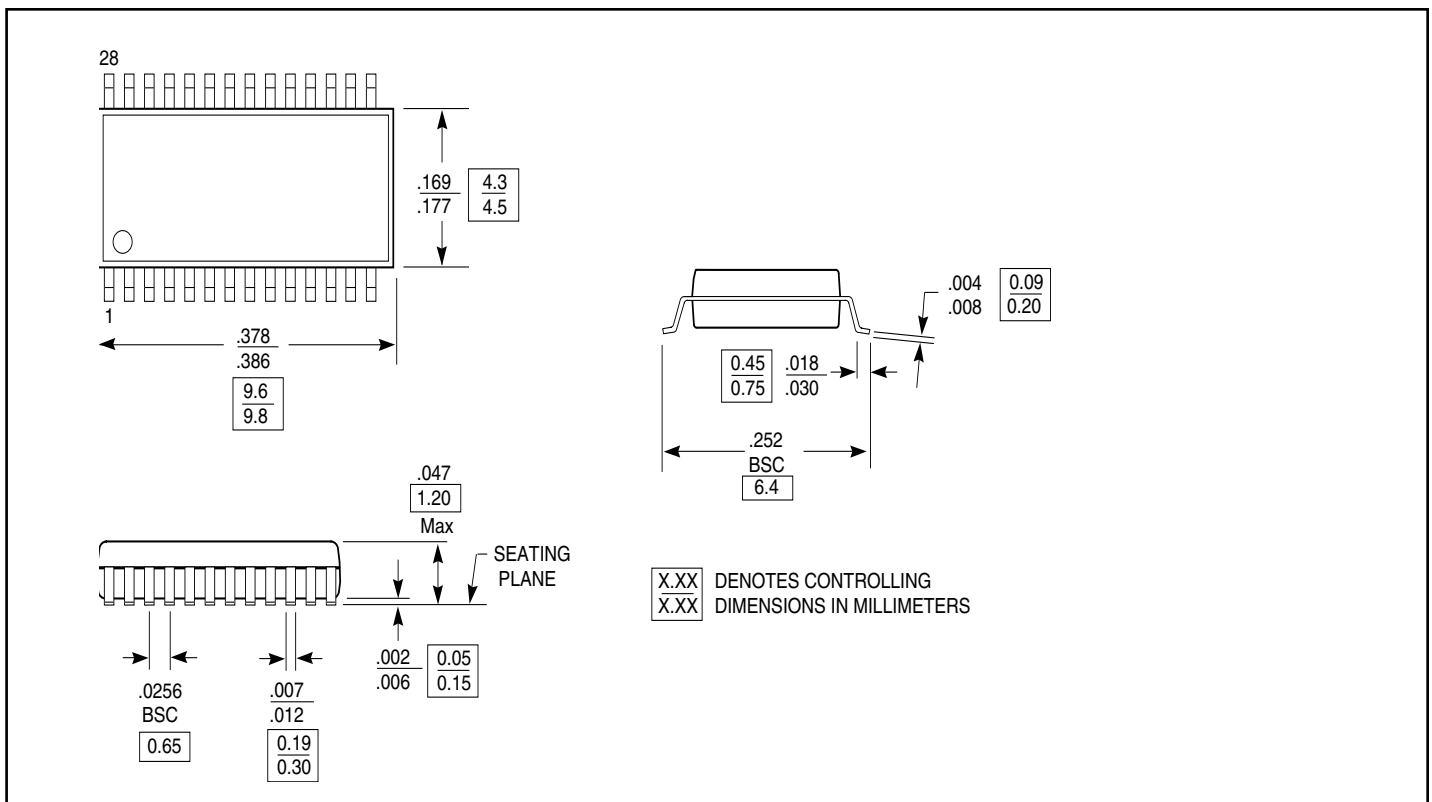
1.  $R_L = 100\Omega$  or  $50\Omega \pm 1\%$
2. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PPR) = 0.5 Mpps, pulse width =  $500 \pm 10\text{ns}$ .

**Typical Characteristics**

**Figure 7**

**Figure 8**

**Figure 9**

**Figure 10**

**Packaging Mechanical: 28-Pin QSOP (Q)**



**Packaging Mechanical: 28-Pin TSSOP (L)**



**Ordering Information**

<b>Ordering Code</b>	<b>Package Code</b>	<b>Packaging Description</b>
PI90LV024Q	Q	28-pin 150-mil SOIC
PI90LV024QE	Q	Pb-free & Green, 28-pin 150-mil SOIC
PI90LV024L	L	28-pin 170-mil TSSOP
PI90LV024LE	L	Pb-free & Green, 28-pin 170-mil TSSOP
PI90LVB024Q	Q	28-pin 150-mil SOIC
PI90LVB024QE	Q	Pb-free & Green, 28-pin 150-mil SOIC
PI90LVB024L	L	28-pin 170-mil TSSOP
PI90LVB024LE	L	Pb-free & Green, 28-pin 170-mil TSSOP

**Notes:**

1. Thermal Characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)