

# System Basis Chip TLE 6266 G

Integrated LS CAN, LDO and  
LS - HS Switches

Automotive and  
Industrial



Never stop thinking.

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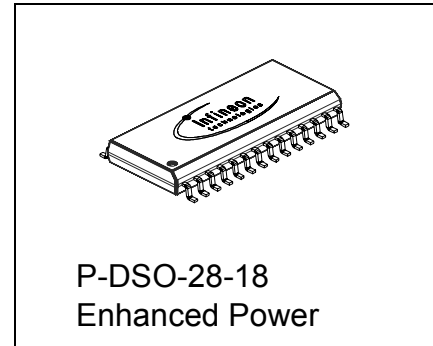
# System Basis Chip

# TLE 6266 G

## Datasheet

### 1 Features

- Standard Fault Tolerant differential CAN-Transceiver
- Bus Failure Management
- Low current consumption mode < 70µA
- CAN Data Transmission Rate up to 125 kBaud
- Low-Dropout Voltage Regulator 5V ± 2%
- Two Low Side Switches
- Three High Side Switches with internal Charge Pump
- Power On and Under-Voltage Reset Generator
- Vcc Supervisor
- Window Watchdog
- Flash Program Mode
- Programmable Cyclic Wake Timing via SPI
- Integrated Fail-Safe Mechanism
- Standard 16 bit SPI-Interface
- Wide Input Voltage and Temperature Range
- Thermal Protection
- Enhanced Power P-DSO-Package
- Wakeup Input Pin



Type	Ordering Code	Package
TLE 6266 G	on request	P-DSO-28-18

### 2 Description

The TLE 6266 G is a monolithic integrated circuit in an enhanced power P-DSO-28-18 package, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a 16 bit SPI interface to control and monitor the IC. Further there are integrated additional features like three high side switches, two low side switches, a window watchdog circuit and a reset circuit. The IC offers a low current consumption mode, that reduces the current to typ. 70µA.

The IC is designed to withstand the severe conditions of automotive applications and is optimized for low-speed data transmission (up to 125 kBaud).

### 3 Pin Configuration (top view)

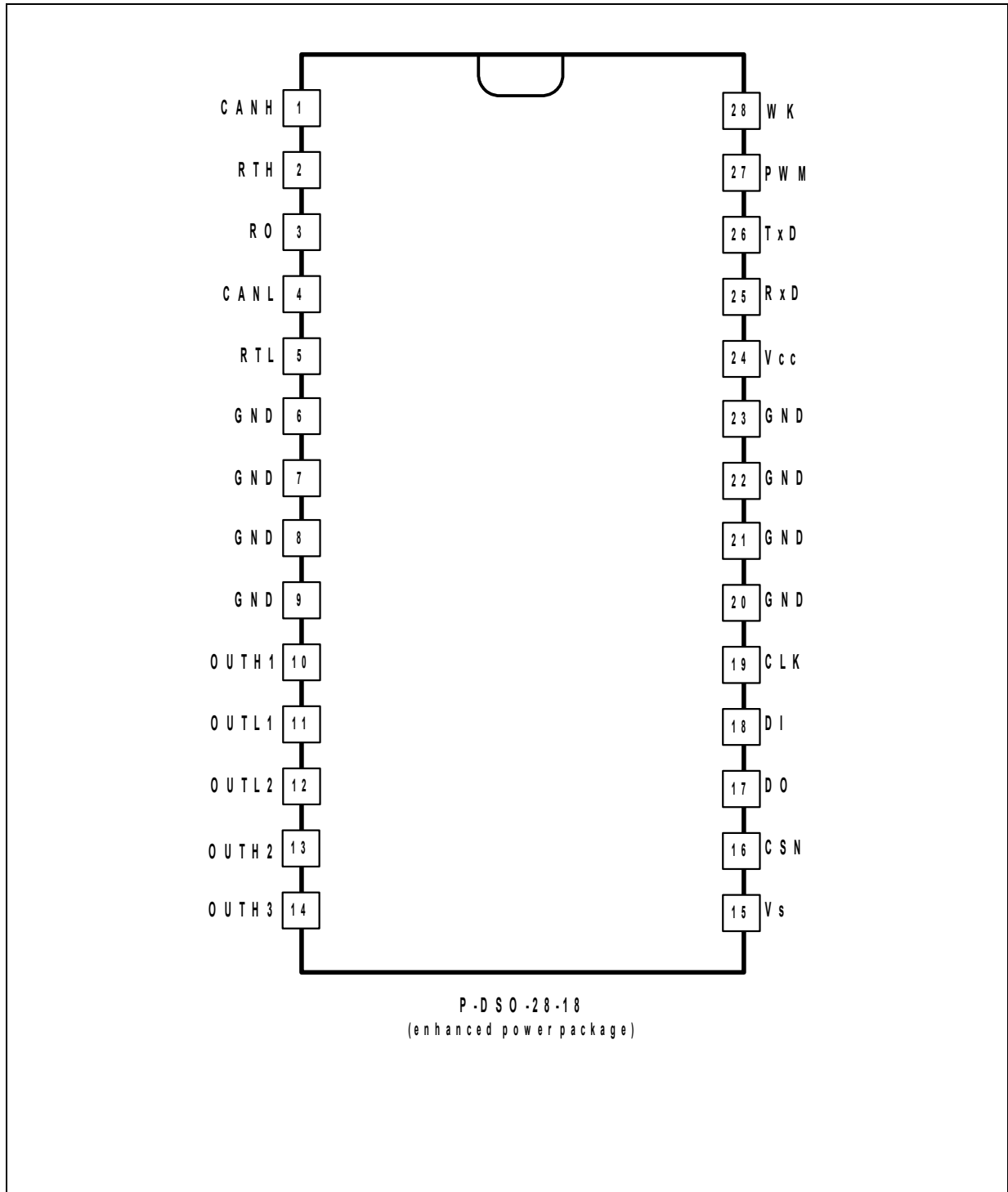


Figure 1 TLE 6266 Block Diagram

**4 Pin Definitions and Functions**

Pin No.	Symbol	Function
1	CANH	<b>CAN-H bus line</b> ; HIGH in dominant state
2	RTH	<b>CANH-Termination input</b> ; connected to CANH via external termination resistor
3	RO	<b>Reset output</b> ; open drain output; integrated pull up; active LOW
4	CANL	<b>CAN-L bus line</b> ; LOW in dominant state
5	RTL	<b>CANL-Termination input</b> ; connected to CANL via external termination resistor
6, 7, 8, 9, 20, 21, 22, 23	GND	<b>Ground</b> ; to reduce thermal resistance place cooling areas on PCB close to this pins.
10	OUTH1	<b>High side output 1</b> ; controlled via PWM input and/or SPI input, short circuit protected
11	OUTL1	<b>Low side output 1</b> ; SPI controlled, with active zener
12	OUTL2	<b>Low side output 2</b> ; SPI controlled, with active zener
13	OUTH2	<b>High side output 2</b> ; SPI controlled
14	OUTH3	<b>High side output 3</b> ; SPI controlled, in cyclic wake mode controlled by an internal autotiming function
15	Vs	<b>Power supply</b> ; block to GND directly at the IC with ceramic capacitor
16	CSN	<b>SPI interface Chip Select Not</b> ; CSN is an active low input; serial communication is enabled by pulling the CSN terminal LOW. CSN input should only be transitioned when CLK is LOW. CSN has an internal active pull up and requires CMOS logic level inputs. See <b>Figure 11</b> for more details.
17	DO	<b>SPI interface Data Out</b> ; DO is a tristate output that transfers diagnosis data to the control device. Serial data transferred from DO is a 16 bit diagnosis word with the Least Significant Bit (LSB) transmitted first. The output will remain 3-stated unless the device is selected by a LOW on Chip-Select-Not (CSN). DO will accept data on the rising edge of CLK-signal; see <b>Table 6</b> for output data protocol and <b>Figure 11</b> for more timing details.

**4 Pin Definitions and Functions (cont'd)**

Pin No.	Symbol	Function
18	DI	<b>SPI interface Data In</b> ; DI receives serial data from the control device. Serial data transmitted to DI is a 16 bit control word with the Least Significant Bit (LSB) transferred first. The input has an active pull down and requires CMOS logic level inputs. DI will accept data on the falling edge of CLK-signal; see <b>Table 6</b> for input data protocol and <b>Figure 11</b> for more details.
19	CLK	<b>SPI interface clock input</b> ; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs
24	V <sub>CC</sub>	<b>Output voltage regulator</b> ; 5V logic supply, block to GND with an 100nF external ceramic capacitor directly at the IC + external capacitor C <sub>Q</sub> ≥ 22 μF
25	RxD	<b>CAN Receive data output</b> ; push-pull output; LOW: bus becomes dominant, HIGH: bus becomes recessive
26	TxD	<b>CAN Transmit data input</b> ; integrated pull up; LOW: bus becomes dominant, HIGH: bus becomes recessive
27	PWM	<b>Pulse Width Modulation control</b> ; integrated pull down, active HIGH. To PWM-control highside-switch HS1
28	WK	<b>Wake-Up input</b> ; for detection of external wake-up events within cyclic wake mode, integrated pull down, active HIGH, switches on rising edge

## 5 Functional Block Diagram

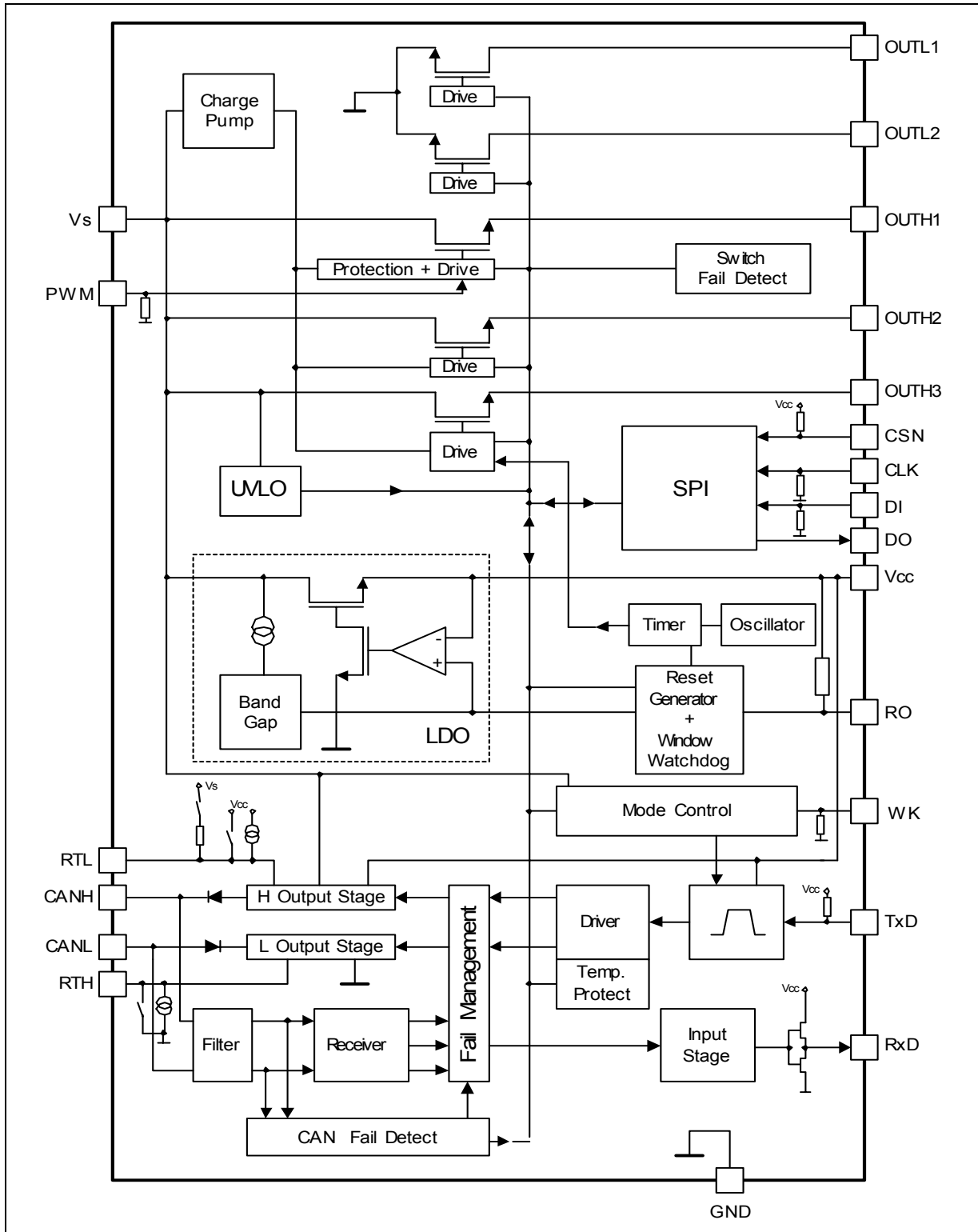


Figure 2 TLE 6266 G Functional Block Diagram

## 6 Circuit Description

The TLE 6266 G is a monolithic IC, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a SPI interface to control and monitor the IC. Further there are three high side switches, two low side switches, a window watchdog circuit and a reset circuit integrated. **Figure 2** shows the block diagram of the TLE 6266.

### 6.1 Operation Modes

The TLE 6266 offers four different operation modes (see **Figure 3**), that are controlled via the SPI input bits 9,10 (mode bits M0,M1) as shown in **Table 1**: the *normal* operation mode, the *receive-only* mode, the  $V_{bat}$  *stand-by* mode and the *cyclic wake* operation mode.

The cyclic wake mode itself is subdivided into two modes: the *cyclic HS OFF* and the *cyclic HS ON* mode. Cyclic wake and  $V_{bat}$  stand-by mode are both designed for periods that do not require communication on the CAN-Bus but offer a low power mode. The lowest current consumption is achieved in the cyclic wake HS OFF mode.

**Table 1 Operation modes bit settings**

	<b>Mode Bit M1 (SPI Bit 10)</b>	<b>Mode Bit M0 (SPI Bit 9)</b>
Normal operation	1	1
Cyclic Wake	1	0
RxD only	0	1
$V_{bat}$ stand-by	0	0

#### Normal Operation Mode

The normal operation mode is designed to receive and transmit data messages as well as to supply the ECU and control loads via HS- and LS- switches. RTL is switched to  $V_{CC}$ , RTH to GND. **Table 3** gives an overview about the available functions in this mode.

#### RxD-only Mode

In the receive-only mode the receiver stage is activated and the transmitter stage is deactivated. This means that data at the TxD input is not transmitted to the CAN bus but receiving of data is still possible. The CANL line is pulled-up to  $V_{CC}$  via the RTL output and CANH is pulled to GND via RTH. Furthermore, it is possible to bypass the signal at TxD to the RxD output during this mode. This mode is useful in combination to a dedicated network-management software that allows separate diagnosis for all nodes (see **Chapter 6.2**). **Table 3** gives an overview about the available functions in this mode.



### $V_{bat}$ stand-by Mode

In the  $V_{bat}$  stand-by mode the CAN transmitter and receiver stage are deactivated, to achieve a low power consumption. All other functions are active as in the normal mode (see **Table 3**). The CANL line is pulled-up to battery supply voltage via the RTL output and CANH pulled to GND via RTH. A wake-up request via a CAN message on the bus is immediately reported to the microcontroller by setting RxD=LOW. The wake pin WK is not active in this mode. A power-on condition ( $V_{bat}$  pin is supplied) or a watchdog reset, automatically switches the TLE 6266 to  $V_{bat}$  stand-by mode. Also if the supply voltage drops below the specified limits (undervoltage reset), the transceiver is automatically switched to  $V_{bat}$  stand-by mode or power down mode, respectively.

### Cyclic Wake Modes

In the cyclic wake operation mode the lowest power consumption is achieved. This mode consists of two states, the *Cyclic HS ON* and the *Cyclic HS OFF* mode. Everytime the cyclic HS ON mode is entered (from all other modes), a long open window is started.

In the **HS ON state** the transmitter, receiver and all switches, except the HS3 switch, are deactivated. The CANL line is pulled-up to battery supply voltage via the RTL output and CANH pulled to GND via RTH. A wake-up via CAN bus message sets the RxD output to LOW. Everytime the cyclic HS ON mode is entered , a long open window is started. If there is no valid watchdog trigger or a PWM transition into the HS OFF state during this time, a watchdog reset is activated. Only a correct trigger signal on the PWM pin causes a transition into the cyclic HS OFF state. This is called the “failsafe PWM” feature.

In the **HS OFF state**, almost all functions of the IC are deactivated(also HS3-switch). Only the wake-up input, the oscillator and the power-on reset circuit are activated. The oscillator is used to realize the HS3-cyclic wake function.This automatically switches to HS ON state after a programmed time, to enabled HS3 (see **Table 2**).The CANL line is pulled-up to battery supply voltage via the RTL output and CANH pulled to GND via RTH. Only the wake up via CAN message sets the RxD to low (visible in HS ON state).

There are three possibilities to enter the cyclic HS ON mode from the HS OFF mode:

- the cyclic wake function
- a CAN bus wake
- a rising edge at the wake-up pin

**Table 2 SPI Bit settings for the cyclic wake function**

Input Bit 13	Input Bit12	Period	# of Cycles (1 cycle = 512µs typ.)
0	0	48ms	94
0	1	96ms	188
1	0	192ms	376
1	1	no cyclic wake-up	-

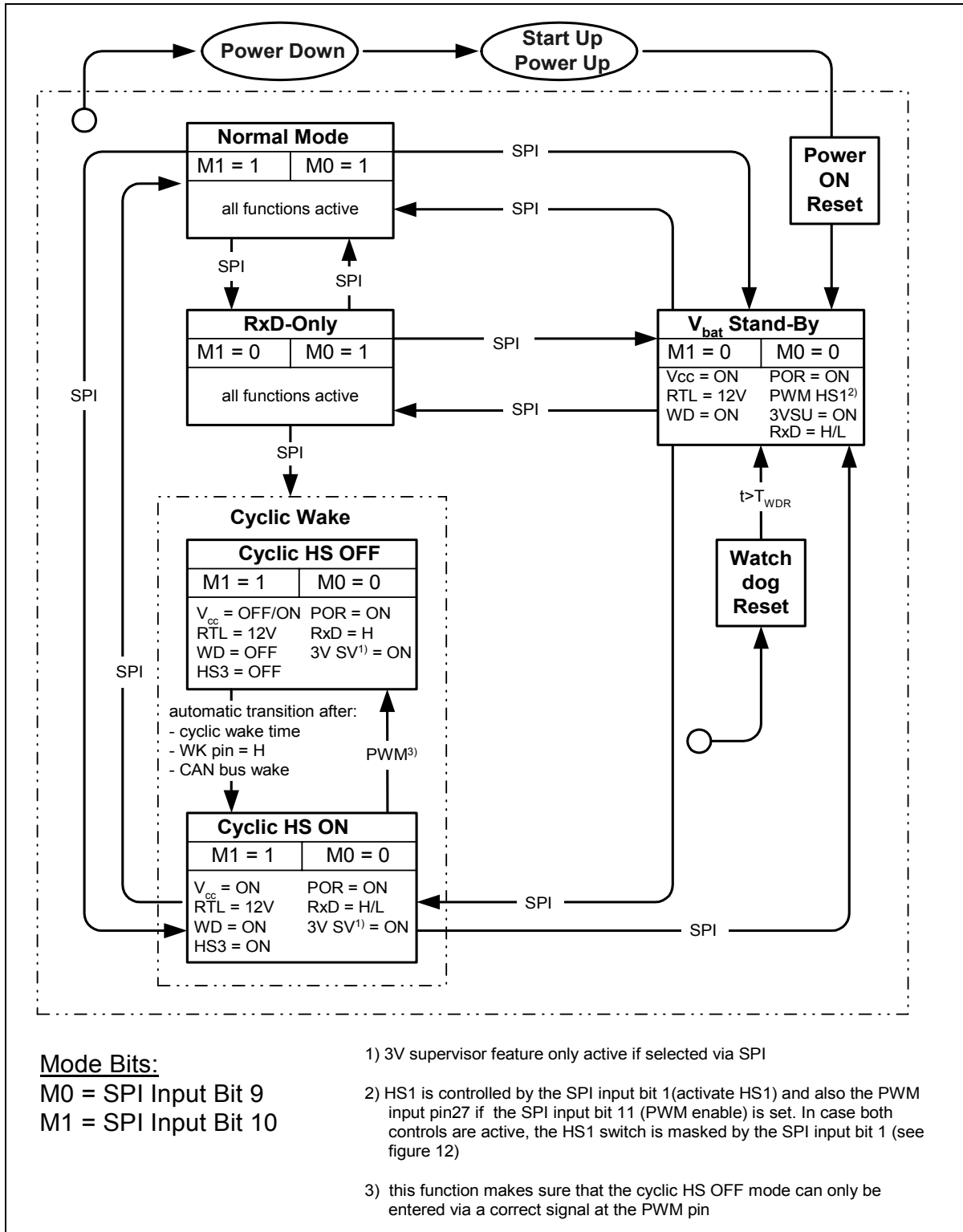


Figure 3 State Diagram

**Table 3 Operation mode table**

Feature	Normal mode	RxD only mode	V <sub>bat</sub> stand-by mode	Cyclic Wake HS ON	Cyclic Wake HS OFF
LDO	ON	ON	ON	ON	OFF/ON
Reset	ON	ON	ON	ON	ON
Watchdog	ON	ON	ON	ON	OFF
SPI	ON	ON	ON	ON	OFF
Oscillator	ON	ON	ON	ON	ON
CAN transmit	ON	OFF	OFF	OFF	OFF
CAN receive	ON	ON	OFF	OFF	OFF
OUTHS 1 <sup>1) 2) 3)</sup>	ON	ON	ON	OFF	OFF
PWM HS1 <sup>2)</sup>	ON	ON	ON	OFF	OFF
OUTHS 2 <sup>1) 3)</sup>	ON	ON	ON	OFF	OFF
OUTHS 3 <sup>1) 3)</sup>	ON	ON	ON	OFF	OFF
OUTHS 3 cycl. HS ON <sup>1) 3)</sup>	OFF	OFF	OFF	ON	OFF
OUTLS 1 <sup>1) 3)</sup>	ON	ON	ON	OFF	OFF
OUTLS 2 <sup>1) 3)</sup>	ON	ON	ON	OFF	OFF
OUT HS 3 Timebase-Test	ON	ON	ON	OFF	OFF
Wake Pin	OFF	OFF	OFF	OFF	ON
Failsafe PWM <sup>4)</sup>	OFF	OFF	OFF	ON	OFF
3V Supervisor <sup>1)</sup>	ON	ON	ON	ON	ON
RTL output	switched to Vcc	switched to Vcc	switched to Vs	switched to Vs	switched to Vs
RxD output	L = bus dominant; H = bus recessive	L = bus dominant; H = bus recessive	active low on CAN message wake-up	active low on CAN message wake-up	active low on CAN message wake-up

<sup>1)</sup> only active when selected via SPI

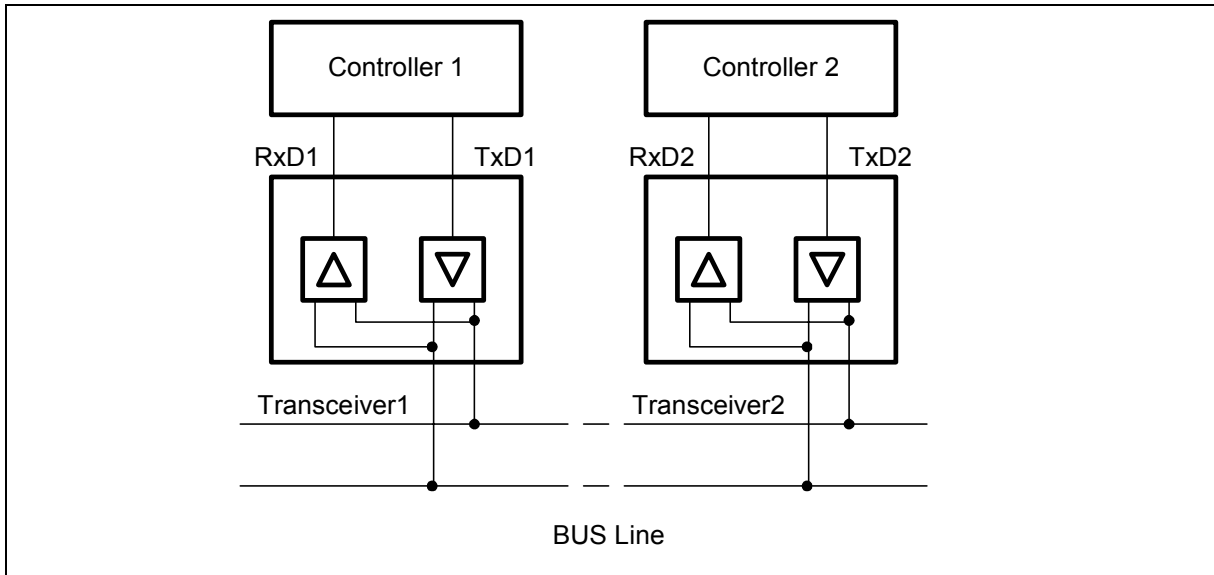
<sup>2)</sup> HS1 is controlled by the SPI input bit 1(activate HS1) and also the PWM input pin27 if the SPI input bit 11 (PWM enable) is set. In case both controls are active, the HS1 switch is masked by the SPI input bit 1 (see figure 12)

<sup>3)</sup> automatically disabled when a reset resp. watchdog reset occurs

<sup>4)</sup> this function makes sure that the cyclic HS OFF mode can only be entered via a correct signal at the PWM pin

## 6.2 LS CAN Transceiver

The CAN transceiver TLE 6266 works as the interface between the CAN protocol controller and the physical CAN bus-lines. **Figure 4** shows the principle configuration of a CAN network.



**Figure 4** CAN Network Example

In normal operation mode a differential signal is transmitted/received. When bus wiring failures are detected, the device automatically switches in a dedicated single-wire mode to maintain communication. While no data is transferred, the power consumption can be minimized by multiple low power operation modes. Further a receive-only mode is implemented that allows a separate CAN node diagnosis. During normal and Rx/D-only mode, RTL is switched to  $V_{CC}$  and RTH to GND. During  $V_{bat}$  stand-by and the cyclic wake mode, RTL is switched to  $V_S$  and RTH to GND.

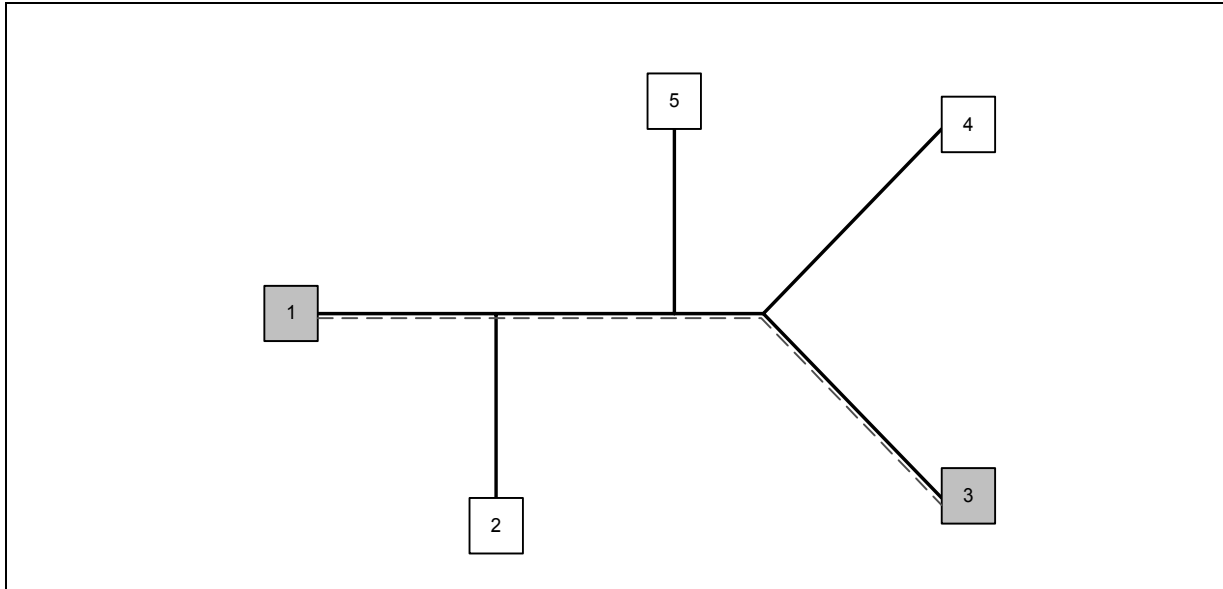
### Receive-only Mode

The receive only mode is designed for a special test procedure to check the bus connections. **Figure 5** shows a network consisting of 5 nodes. If the connection between node 1 and node 3 shall be tested, the nodes 2,4 and 5 are switched into receive only mode. Node 1 and node 3 are in normal mode. If node 1 sends a message, node 3 is the only node which can acknowledge the message, the other nodes can only listen but cannot send an acknowledge bit. If node 1 receives the acknowledge bit from node 3, the connection is OK.

### Electromagnetic Emission (EME)

To reduce radiated electromagnetic emission (EME), the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission (one of the

bus lines is affected by a bus line failure) the EME performance of the system is degraded from the differential mode.



**Figure 5 Testing the Bus Connection in Receive-only Mode**

### 6.3 Bus Failure Management

There are 9 different CAN bus wiring failures defined by the ISO 11519-2/ISO 11898-3 standard. These failures are divided into 7 failure groups (see **Table 4**). The difference between ISO11898-3 and ISO 11519-2 is also shown in **Table 4**. When a bus wiring failure is detected the device automatically switches to a dedicated CANH or CANL single-wire mode to maintain the communication if necessary. Therefore it is equipped with one differential receiver and four single ended comparators (two for each bus line).

To avoid false triggering by external RF influences, the single wire modes are activated after a certain delay time. As soon as the bus failure disappears the transceiver switches back to differential mode after another time delay.

The differential receiver threshold is set to typ. -2.5V. This ensures correct reception in the normal operation mode as well as in the failure cases 1, 2, 3a(6a) and 4(5) with a noise margin as high as possible. When one of the bus failures 3(6), 5(4), 6(3), 6a(3a), and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and output stage. The failure cases in brackets() are the failure cases according to ISO 11898-3. Simultaneously the multiplexing output of the receiver circuit is switched to the unaffected single ended comparator

The bus failures are monitored via the diagnosis protocol of the SPI. Therefore it is possible to distinguish 6 CAN bus failures or failure groups on the SPI output bits 8 to 13 (see Table 4 and 5). The failures are reported until transmission of the next CAN word begins.

The SPI output bit 0 for CAN bus wiring failure can be read out without SPI transmission directly via the CSN pin (CSN=LOW). A transition of the CSN pin signal from LOW to HIGH resets the SPI diagnosis bit 0..

**Table 4 CAN bus line failure cases** (according to ISO 11519-2 and ISO 11898-3)

<b>Failure #</b>	<b>failure description according to ISO 11898-3</b>	<b>failure description according to 11519-2</b>
1	CANH line interrupted	CANL line interrupted
2	CANL line interrupted	CANH line interrupted
3	CANH shorted to Vbat	CANL shorted to Vbat
3a	CANH shorted to Vcc	CANL shorted to Vcc (no ISO failure)
4	CANL shorted to GND	CANH shorted to GND
5	CANH shorted to GND	CANL shorted to GND
6	CANL shorted to Vbat	CANH shorted to Vbat
6a	CANL shorted to Vcc	CANH shorted to Vcc (no ISO failure)
7	CANL shorted to CANH	CANL shorted to CANH

In case the transmission data input TxD is permanently dominant, both, the CANH and CANL transmitting stage are disabled after a certain delay time  $t_{TXD}$ . This is necessary to prevent the bus from being blocked by a defective protocol unit or short to GND at the TxD input..

**Table 5 SPI output bits for bus failure diagnosis**

<b>OBIT</b>	<b>Bus Failure</b>
13	CAN Failure 2(1) and 4(5)
12	CAN Failure 1(2) and 3a(6a)
11	CAN Failure 6(3)
10	CAN Failure 6a(3a)
9	CAN Failure 5(4) and 7
8	CAN Failure 3(6)
0	CAN Bus Failure
H= ON L= OFF (...) values in brackets according to ISO11898-3 see table 4	

In order to protect the transceiver output stages from being damaged by shorts on the bus lines, current limiting circuits are integrated. The CANL and CANH output stage respectively are protected by an additional temperature sensor, that disables them as soon as the junction temperature exceeds the maximum value. In the temperature shut-down condition of the CAN output stages receiving messages from the bus lines is still possible. A thermal shutdown of the CAN-transceiver circuit is monitored via the SPI output bit 15. The CANH and CANL pins are also protected against electrical transients which may occur in the severe conditions of automotive environments

#### 6.4 Low Dropout Voltage Regulator

The TLE6266 is able to drive external 5V loads up to 45 mA. Its output voltage tolerance is less than  $\pm 2\%$ . In addition the regulator circuit drives the internal loads like the CAN-transceiver circuit. In the cyclic wake HS OFF operation mode the voltage regulator is switched on and off by a control mechanism (see **Chapter 6.5**).

The current limitation of the LDO is set to typ. 180mA, to grant that the external capacitor can be charged quickly. In normal operating mode the external current should be less than 45mA. This has to be guaranteed by the system architecture.

An external reverse current protection is recommended to prevent the output capacitor from being discharged by negative transients or low input voltage.

Stability of the output voltage is guaranteed for output capacitors  $C_{VCC} \geq 100$  nF. Nevertheless a lot of applications require a much larger output capacitance to buffer the output voltage in case of low input voltage or negative transients. Furthermore the due function of e.g. the reset and 3V-supervisor circuit are supported by a larger output capacitance because of their reaction times. Therefore a output capacitance  $C_{VCC} \geq 22$   $\mu$ F is recommended.

#### 6.5 LDO activation during Cyclic Wake HS OFF

During the cyclic wake HS OFF mode, the LDO is switched on and off, depending on the output voltage level, which is monitored internally. **Figure 6** shows a detailed flowchart of the  $V_{CC}$  control loop and also a graph of the  $V_{CC}$  voltage and the thresholds in this mode. The voltage regulator is switched on as soon as the voltage at  $V_{CC}$  falls below the load-threshold  $V_{CC TH}$  to charge an external capacitor. The voltage at  $V_{CC}$  starts to decrease and when the  $V_{CC TH}$  threshold is reached again, the capacitor is charged for additional 1ms. When the nominal voltage level  $V_{CC}$  is reached again, the voltage regulator is automatically deactivated to minimize the current consumption. The period of charging/decharging is dependant on the external stabilization capacitor at the  $V_{CC}$  pin. If the load is too high and  $V_{CC}$  falls below  $V_{CC TH}$  for  $t > 3\mu$ s, a reset is activated.

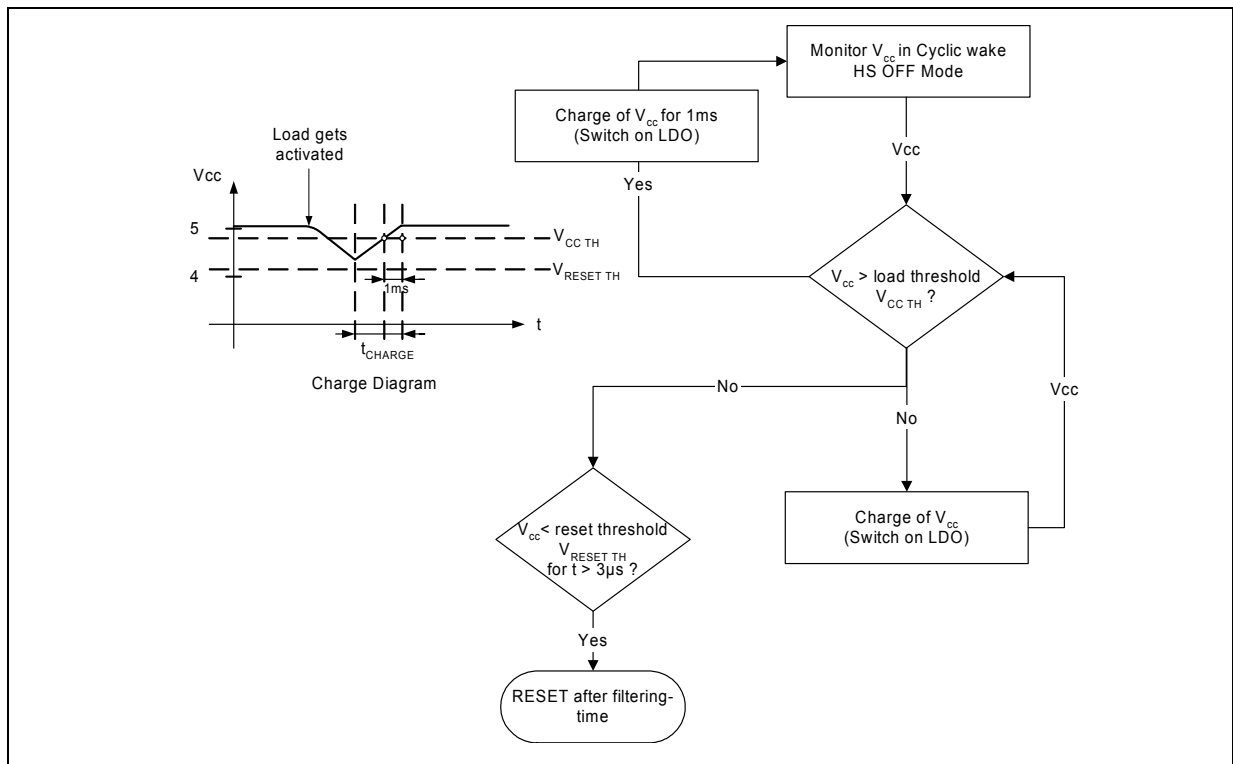


Figure 6 LDO activation flowchart for the cyclic wake HS OFF mode

### 6.6 3V-Supervisor

This feature is useful e.g. to monitor that the RAM data of the microcontroller might be damaged (prewarning) or the application is connected to V<sub>S</sub> the first time(OEM production line).

The 3V-supervisor is available in all operation modes and has to be activated via the SPI input bit 7 in normal operation mode. If the output voltage falls below the 3V-supervisor threshold V<sub>ST</sub>, an internal flip-flop is set LOW and the SPI monitors this by setting output bit 7 LOW. If the output voltage V<sub>cc</sub> > 3V-supervisor threshold V<sub>ST</sub>, the SPI output bit 7 is set HIGH.

The 3V supervisor uses a comparator to monitor the voltage. Additionally, there is a possibility to disable this comparator in order to reduce the current consumption. To do this, set SPI input bit 15 first and in the next step set SPI input bit 7.

### 6.7 SPI (serial peripheral interface)

The 16-bit wide programming word or input word (see **Table 6**) is read in via the data input DI, and this is synchronized with the clock input CLK supplied by the μC. The diagnosis word appears synchronously at the data output DO (see **Table 7**).



The transmission cycle begins when the chip is selected by the chip select not input CSN (H to L). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus for other usage.

The state of DI is shifted into the input register with every falling edge on CLK. The state of DO is shifted out of the output register after every rising edge on CLK. For more details of the SPI timing please refer to **Figure 11 to 15**.

**CAN Bus Wiring Failure direct Read-out**

The SPI output bit 0 for CAN bus wiring failure can be read out without SPI transmission directly via the CSN pin (CSN=LOW). A transition of the CSN pin signal from LOW to HIGH resets the SPI diagnosis bit 0.

**Table 6 SPI Input Data Protocol**

IBIT	Input Data
15	Disable 3V Reset Comparator
14	not used
13	Cyclic Wake Time Bit2
12	Cyclic Wake Time Bit1
11	PWM Enable HS1
10	Mode 1
9	Mode 0
8	not used
7	Supervisor Enable
6	LS-Switch 2
5	LS-Switch 1
4	Timebase Test
3	HS-Switch 3
2	HS-Switch 2
1	HS-Switch 1
0	Watchdog Trigger

H=ON  
L=OFF

**Table 7 SPI Output Data Protocol**

OBIT	Output Data
15	Thermal Shutdown Transceiver
14	Thermal Shutdown Switches
13	CAN Failure 2 and 4
12	CAN Failure 1 and 3a
11	CAN Failure 6
10	CAN Failure 6a
9	CAN Failure 5 and 7
8	CAN Failure 3
7	3V Supervisor (HIGH = Vcc > 3V)
6	Status LS2
5	Status LS1
4	Temperature Prewarning for all Switches
3	Vs Undervoltage Lockout
2	Window Watchdog Reset
1	Overcurrent HS1
0	CAN Bus Failure

H=ON  
L=OFF

## SPI CLK Monitoring during Cyclic Wake Mode

The TLE 6266 offers a feature to monitor the SPI clock signal (CLK pin) during the cyclic wake mode. If there are edges on the CLK signal, the IC performs a reset and the RO pin is set to LOW for  $t = t_{WDR}$  (after  $t_{WDR}$  a long open window is started and RO is HIGH again). This feature is activated if the CSN pin is set to HIGH.

## 6.8 Oscillator

The TLE 6266 has an internal oscillator with +/-15% accuracy. The typ. frequency of the oscillator is 125kHz. After an internal 64-times frequency divider, this gives a typ. cycle time  $t_{cyc} = 0.512\text{ms}$ . The frequency of the oscillator can be measured within the normal, the  $V_{bat}$  stand-by and the RxD-only mode. This is a timebase test (see **Chapter 6.15**), activated via SPI input bit 3 and 4. During this test, the HS3-switch will be activated cyclically.

## 6.9 Window Watchdog and Reset

When the output voltage  $V_{CC}$  exceeds the reset threshold voltage  $V_{RT}$  the reset output RO is switched HIGH after a delay time  $t_{RD}$ . This is necessary for a defined start of the microcontroller when the application is switched on. As soon as an under-voltage condition of the output voltage ( $V_{CC} < V_{RT}$ ) appears, the reset output RO is switched LOW again. The LOW signal is guaranteed down to an output voltage  $V_{CC} \geq 1\text{V}$ . Please refer to **Figure 17**, reset timing diagram.

In the cyclic wake HS OFF mode, the watchdog circuit is automatically disabled. Both, the undervoltage reset and the watchdog reset set all SPI input bits LOW.

### Long Open Window

After the delayed reset (LOW to HIGH transition of RO) the window watchdog circuit is started by opening a long open window. The long open window allows the microcontroller to run his set-up and to trigger the watchdog via the SPI afterwards. Within the long open window period a watchdog trigger is alternating detected as a "rising" or "falling edge" by sampling a HIGH on the SPI input bit 0. The trigger is accepted when the CSN input becomes HIGH after the transmission of the SPI word. After every reset condition (watchdog reset, undervoltage reset) as well as a transition from every mode into the cyclic wake HS ON mode, the watchdog starts the long open window and the default value of the SPI input bit 0 is LOW.

### Closed/Open Window

A correct watchdog trigger immediately results in starting the window watchdog by opening the closed window followed by the open window (see **Figure 18**). From now on the microcontroller has to service the watchdog trigger by inverting the SPI input bit 0 alternating. The "negative" or "positive" edge has to meet the open window time. A correct watchdog service immediately results in starting the next closed window. Please refer to **Figure 19**, watchdog timing diagram.

## Watchdog Trigger Failure

If the trigger signal does not meet the open window a watchdog reset is created by setting the reset output RO low for  $t_{WDR}$ . Then the watchdog starts again by opening the long open window. In addition, the SPI output bit 2 is set HIGH until the next successful watchdog trigger, to monitor a watchdog reset. SPI output bit 2 is also HIGH until the watchdog is correctly triggered after power-up/start-up. For fail safe reasons the TLE6266 is automatically switched in  $V_{bat}$  stand-by mode if a watchdog trigger failure occurs.

### 6.10 High Side Switch 1

The high side output OUTH1 is able to switch loads up to 250 mA. Its on-resistance is  $1.0 \Omega$  typ. @  $25^\circ\text{C}$ . This switch can be controlled either via the PWM input or the SPI input bit 1. When the input PWM is used, it has to be enabled by setting the SPI input bit 11 HIGH. In case of both control inputs being active the PWM signal is masked by the SPI signal (see **Figure 16**, High Side Switch 1 Timing Diagram).

The SPI output bit 14 monitors a thermal shutdown of the switches, whereas output bit 4 flags a thermal prewarning. So the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. Further OUTH1 is protected against short circuit and overload. The SPI output bit 1 indicates an overload of OUTH1. As soon as the under-voltage condition of the supply voltage is met ( $V_S < V_{UVOFF}$ ), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI output bit 3. Moreover the switch is disabled when a reset occurs. After the second correct triggered watchdog, the switch is released for usage.

### 6.11 High Side Switch 2

The high side output OUTH2 is able to switch loads up to 250 mA. Its on-resistance is  $1.0 \Omega$  typ. @  $25^\circ\text{C}$ . This switch is controlled via the SPI input bit 2.

The SPI output bit 14 monitors a thermal shutdown of the switches, whereas output bit 4 flags a thermal prewarning. So the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. As soon as the under-voltage condition of the supply voltage is met ( $V_S < V_{UVOFF}$ ), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI output bit 3. Moreover the switch is disabled when a reset occurs. After the second correct triggered watchdog, the switch is released for usage.

### 6.12 High Side Switch 3

The high side output OUTH3 is able to switch loads up to 250 mA. Its ON-resistance is  $1.0 \Omega$  typ. @  $25^\circ\text{C}$ . This switch is controlled via the SPI input bits 3 and 4. To supply external wake-up circuits in low power mode (cyclic wake mode), the output OUTH3 is

periodically activated by entering the cyclic wake HS ON mode. The autotiming period is programmable via SPI (see **Table 2**). This has to be done, to minimize the current consumption depending on the cyclic wake time (see **Figure 21**).

In the cyclic wake mode, the PWM signal is used to switch HS3 from the cyclic HS ON to the cyclic HS OFF state, if correctly triggered within the long open window (see **Figure 17**). This is called the “fail-safe PWM” feature

The SPI output bit 14 monitors a thermal shutdown of the switches, whereas output bit 4 flags a thermal prewarning. So the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. As soon as the under-voltage condition of the supply voltage is met ( $V_S < V_{UVOFF}$ ), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI output bit 3. Moreover the switch is disabled when a reset occurs. After the second correct triggered watchdog, the switch is released for usage.

### 6.13 Low Side Switches 1 & 2

The two low side outputs OUTL1 and OUTL2 are able to switch loads up to 100 mA. Their on-resistance is 1.5  $\Omega$  typ. @ 25°C. These switches are controlled via the SPI input bits 5 and 6. In case of high inrush currents a built-in zener circuit (typ. 37 V) activates the switches to protect them.

The SPI diagnosis bit 14 monitors a thermal shutdown of the switches, whereas bit 4 flags a thermal prewarning. So the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. The SPI output bits 5/6 are giving a feedback about current status (ON/OFF) of OUTL1/OUTL2. As soon as the under-voltage condition of the supply voltage is met ( $V_S < V_{UVOFF}$ ), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI diagnosis bit 3. In addition the outputs OUTL1 and OUTL2 are disabled when a reset occurs. After the second correct triggered watchdog, the switches are released for usage.

### 6.14 Wake Up Pin

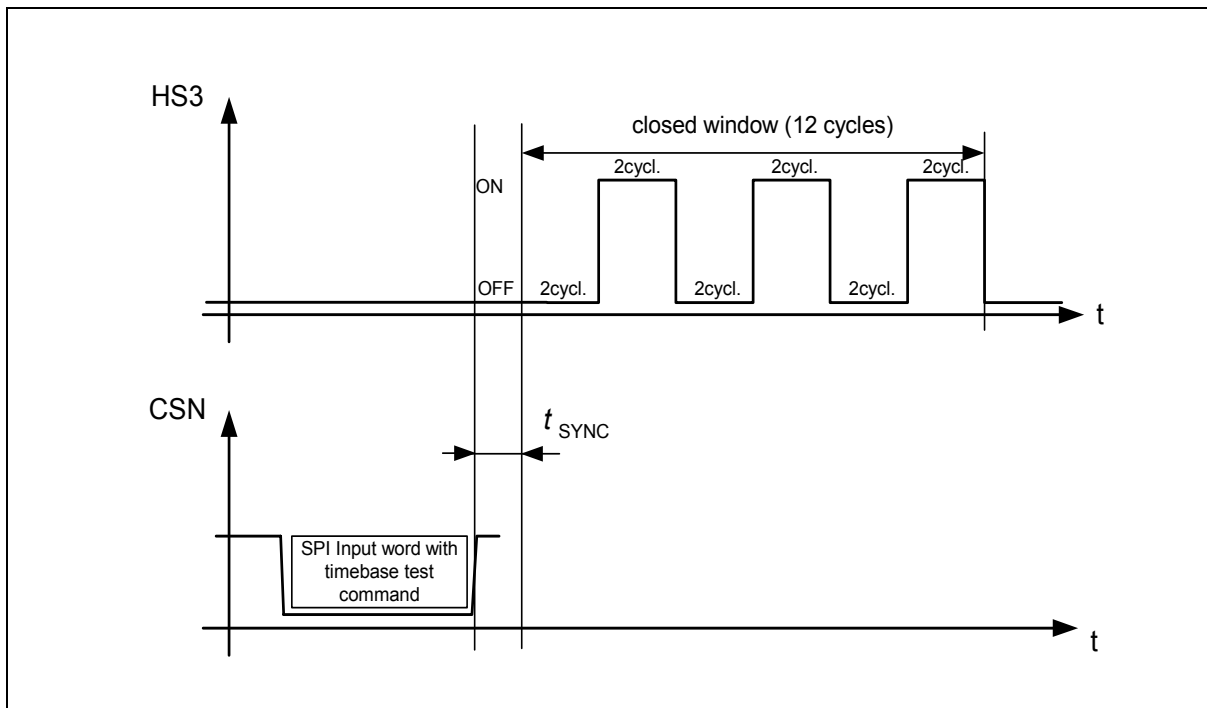
This pin is used to wake up the TLE 6266 with an external signal from the  $\mu$ C. The feature is active during cyclic HS OFF mode to switch the transceiver into the cyclic HS ON mode before starting up the  $\mu$ C. A correct wake up signal is a rising edge at the WK pin during cyclic HS OFF mode. The WK pin has an implemented pull-down resistance.

### 6.15 Timebase Test

This test is useful to measure the internal cycle time of the TLE 6266. The  $\mu$ C may use this information to activate special functions or routines in the cyclic wake mode, which

are depending on timing.(e.g. to switch on/off a LED after a certain number of cyclic HS ON conditions). During the long open window the timebase test is not available.

To measure the internal cyclic timing, the SPI input bit 3 and 4 have to be set HIGH. Then the HS3 switch is automatically enabled for 3 times during the closed window of the watchdog (see **Figure 7**). A correct SPI input word (with IBit 3 and 4 set HIGH) has to be read in first, to activate the timebase test. Due to the fact, that the input command gets activated after the CSN LOW to HIGH transition, it takes  $t_{\text{SYNC}}$  to activate the timebase test. If this SPI input command is given within the open window,  $t_{\text{SYNC}} = \text{max } 500\text{ns}$ . If the command is given during closed window (this is not a watchdog trigger command) the synchronisation  $t_{\text{SYNC}}$  can last up to  $500\mu\text{s}$ .



**Figure 7 Timebase Test Diagram**

### 6.16 Flash program mode

To disable the watchdog feature a flash program mode is available. This mode is selected by applying a voltage of  $6.8\text{V} < V_{\text{PWM}} < 7.2\text{V}$  at pin PWM. This is useful e.g. if the flash-memory of the micro has to be programmed and therefore a regular watchdog triggering is not possible. If the SPI is required in the flash program mode to change e.g. the mode of the TLE6266, the first input telegram has to be "00000000".

## 7 Explanation of the Mode Transitions

To better understand the description, the reader has to be familiar with the **Chapter 6**. All descriptions are starting from the normal mode, as the main operation mode. This means, the component was powered up before and after the power up procedure automatically in the  $V_{bat}$  stand-by mode.

Now, the watchdog circuit has to be operated correctly to switch the component in the other modes ( details see **Chapter 6**). So the starting point is the TLE 6266 in normal mode with a correct triggered watchdog like shown in **Figure 8,9,10**.

### Normal Mode and Cyclic HS ON

In normal mode, the watchdog has to be triggered within the open window with a dedicated SPI input command (Watchdog Trigger IBit 0, alternatively HIGH, LOW,...). The CAN bus communication is active and a message can be transferred/received. After the correct SPI input command to change into the Cyclic HS mode, the HS3 switch gets activated. In parallel a long open window is started, which has to be triggered. This mode can be operated as long as the watchdog is triggered correctly. In this mode, no communication is possible but an external circuit can be supplied by HS3. CANL is pulled up to  $V_s$  by the RTL termination, CANH is pulled to GND via RTH.

### Cyclic HS OFF mode

To switch from HS ON to HS OFF, the PWM input has to be triggered with a falling edge. This is called the PWM failsafe trigger to avoid unwanted transitions into the HS OFF mode. In the HS OFF mode the HS3 switch is deactivated and the lowest power consumption is achieved. The LDO monitors  $V_{cc}$  and switches on/off due to a special control mechanism explained in **Chapter 6.5**. Three possibilities can switch the TLE 6266 back to the cyclic wake HS ON mode:

#### 7.1 CAN Bus Wake-Up

CANL is pulled to  $V_s$ . A signal transition at CANL below a certain wake-up threshold causes a wake up and automatic transition into the cyclic HS ON mode (see **Figure 8**). HS3 is activated again and also the long open window of the watchdog mechanism. The watchdog has to be triggered correctly from that time on. If the signal at the PWM pin makes a HIGH to LOW transition, the device switches to HS OFF again.

This wake up via the CAN bus message is flagged to the  $\mu C$  by setting the RxD output pin from HIGH to LOW. The reason for this behavior is to indicate the  $\mu C$  a wake up request. Now, the  $\mu C$  is able to activate the whole module to serve the requested action by the bus system.

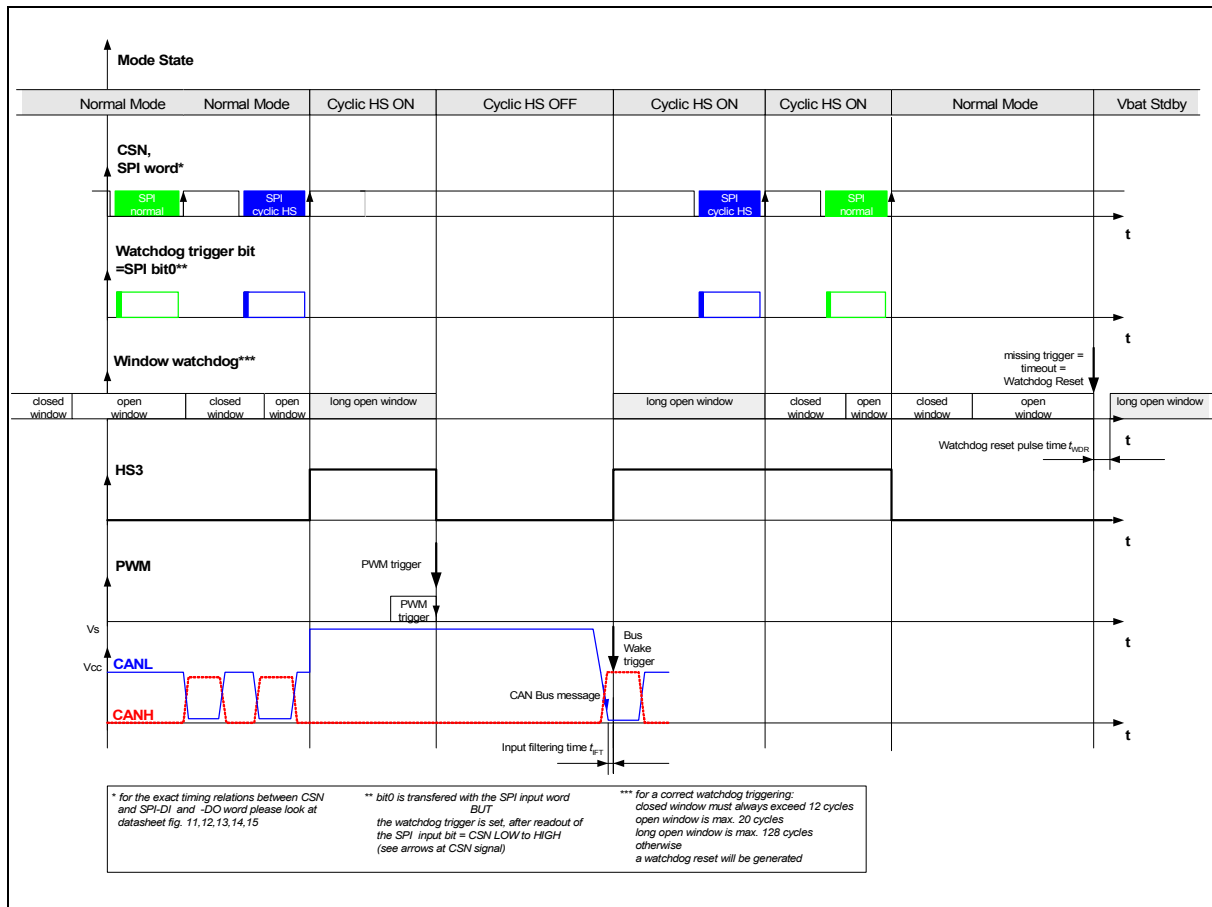


Figure 8 Cyclic Wake with CAN Message Wake-up

### 7.2 Wake-Up via Wake Pin

CANL is pulled to Vs. A signal transition at the wake pin WK from LOW to HIGH (rising edge) causes a wake up and automatic transition into the cyclic HS ON mode (see **Figure 9**). HS3 is activated again and also the long open window of the watchdog mechanism. The watchdog has to be triggered correctly from that time on. If the signal at the PWM pin makes a HIGH to LOW transition, the device switches to HS OFF again. This wake up via the wake pin is coming from an external circuitry (switch, etc.) and is not flagged by the RxD.

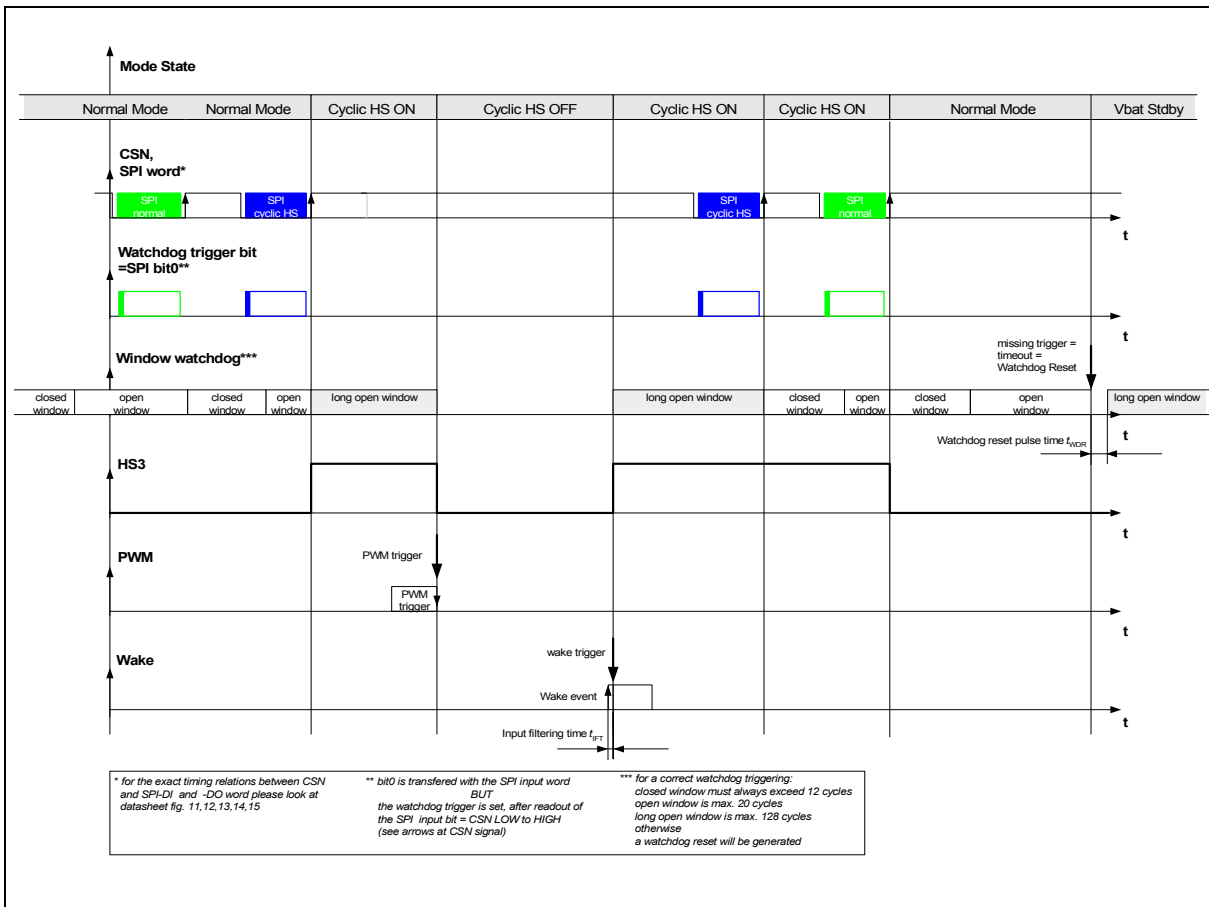


Figure 9 Cyclic Wake with Wake Pin

### 7.3 Wake-Up Cyclic Wake Autotiming Function

CANL is pulled to  $V_s$ . After the transition from HS ON to HS OFF, an autotiming function is started. This is a timer controlled by the internal oscillator, which can be programmed by SPI IBit 12,13. If the timer exceeds the programmed time this causes a wake up and automatic transition into the cyclic HS ON mode (see **Figure 10**). HS3 is activated again and also the long open window of the watchdog mechanism. The watchdog has to be triggered correctly from that time on. If the signal at the PWM pin makes a HIGH to LOW transition, the device switches to HS OFF again.

This wake up via the autotiming function is not flagged to the  $\mu C$  by setting the RxD pin.



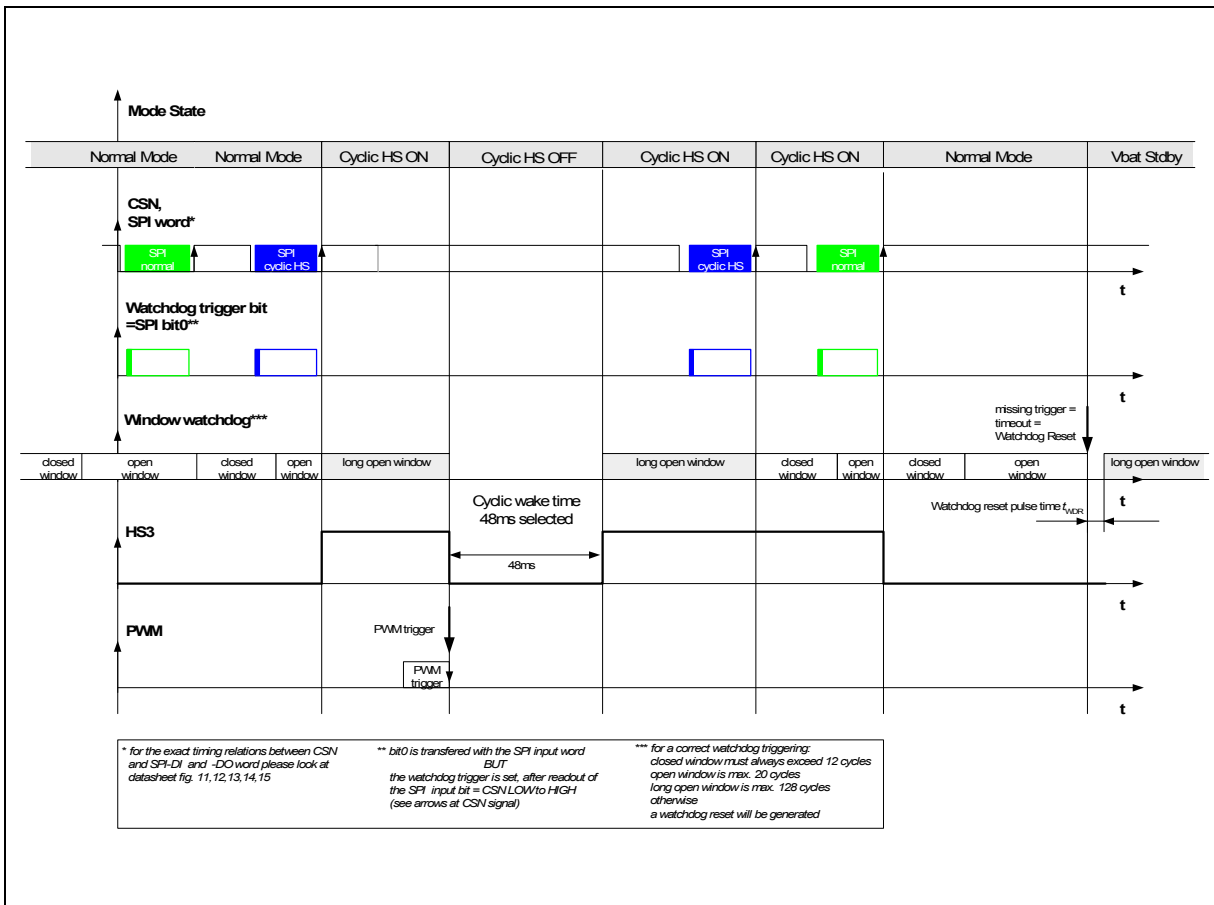


Figure 10 Cyclic Wake with Cyclic Wake Autotiming Function

## 8 Electrical Characteristics

### 8.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

#### Voltages

Supply voltage	$V_S$	-0.3	28	V	
Supply voltage	$V_S$	-0.3	40	V	$t_p < 0.5s; t_p/T < 0.1$
Regulator output voltage	$V_{CC}$	-0.3	5.5	V	
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	-10	28	V	
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	-40	40	V	$V_S > 0V$ $t_p < 0.5s; t_p/T < 0.1$
Transient voltage at CANH and CANL	$V_{BUS}$	-150	100	V	see ISO 7637
Logic input voltages (DI, CLK, CSN, WK, PWM, TxD)	$V_I$	-0.3	$V_{CC} + 0.3$	V	
Logic output voltage (DO, RO, RxD)	$V_{DO/RO/RD}$	-0.3	$V_{CC} + 0.3$	V	
Termination input voltage (RTH, RTL)	$V_{TL/TH}$	-0.3	$V_S + 0.3$	V	
Electrostatic discharge voltage at pin CANH, CANL to GND	$V_{ESD}$	-3000	3000	V	human body model; C = 100pF, R = 1.5k $\Omega$
Electrostatic discharge voltage to all pins	$V_{ESD}$	-1000	1000	V	human body model; C = 100pF, R = 1.5k $\Omega$

#### Currents

Output current; Vcc	$I_{CC}$	*	0,2	A	* internally limited
Output current; OUTH1	$I_{OUTH1}$	*	0.3	A	* internally limited
Output current; OUTH2	$I_{OUTH2}$	-0.7	0.3	A	$t_p < 0.5s; t_p/T < 0.1$ <sup>1)</sup>
Output current; OUTH3	$I_{OUTH3}$	-0.7	0.3	A	$t_p < 0.5s; t_p/T < 0.1$ <sup>1)</sup>
Output current; OUTL1	$I_{OUTL1}$	-0.2	0.4	A	$t_p < 0.5s; t_p/T < 0.1$ <sup>1)</sup>
Output current; OUTL2	$I_{OUTL2}$	-0.2	0.4	A	$t_p < 0.5s; t_p/T < 0.1$ <sup>1)</sup>

### 8.1 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
<b>Temperatures</b>					
Junction temperature	$T_j$	-40	150	°C	
Storage temperature	$T_{stg}$	-50	150	°C	

<sup>1)</sup> Not subject to production test - specified by design

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.*

**8.2 Operating Range (cont'd)**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	$V_{UV\ OFF}$	27	V	After $V_S$ rising above $V_{UV\ ON}$
Supply voltage slew rate	$dV_S/dt$	-0.5	5	V/ $\mu$ s	
Supply voltage increasing	$V_S$	-0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	$V_S$	-0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (DI, CLK, CSN, PWM, TxD )	$V_I$	-0.3	$V_{CC}$	V	
Output current	$I_{CC}$		45	mA	
Output capacitor	$C_{CC}$	22		$\mu$ F	
SPI clock frequency	$f_{CLK}$	–	1	MHz	
Junction temperature	$T_j$	-40	150	$^{\circ}$ C	

**Thermal Resistances**

Junction pin	$R_{thj-pin}$	–	25	K/W	measured to pin 7
Junction ambient	$R_{thj-a}$	–	65	K/W	

**Thermal Prewarning and Shutdown (junction temperatures)**

Thermal prewarning ON temperature	$T_{jPW}$	120	170	$^{\circ}$ C	bit 0 of SPI diagnosis word; hysteresis 30 $^{\circ}$ K (typ.)
Thermal shutdown temp.	$T_{jSD}$	150	200	$^{\circ}$ C	hysteresis 30 $^{\circ}$ K (typ.)
Ratio of SD to PW temp.	$T_{jSD} / T_{jPW}$	1.05	–	–	
Thermal shutdown temp. CAN	$T_{jSD}$	160	200	$^{\circ}$ C	hysteresis 10 $^{\circ}$ K (typ.)

*Note: Calculation of the junction temperature  $T_j = T_{amb} + P \times R_{thj-a}$*

### 8.3 Electrical Characteristics

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### Quiescent current Pin $V_S$

Current consumption	$I_S$	–	5	10	mA	normal mode
Quiescent current $I_{SSB1} = I_S - I_{CC}$	$I_{SSB1}$	–	75	100	$\mu\text{A}$	cycl. wake 48ms; $V_S=12\text{V}$ ; $T_j=25^\circ\text{C}$
Static quiescent current	$I_{STAT}$	–	–	85	$\mu\text{A}$	<u>no</u> cyclic wake; $V_S=12\text{V}$ ; $T_j=25^\circ\text{C}$

#### Voltage Regulator; Pin $V_{CC}$

Output voltage	$V_{CC}$	4.9	5.0	5.1	V	$0.1\text{mA} < I_{CC} < 30\text{mA}$
Output voltage	$V_{CC}$	4.8	5.0	5.5	V	$0\text{A} < I_{CC} < 100\mu\text{A}$
Line regulation	$\Delta V_{CC}$	-20		20	mV	$9\text{V} < V_S < 15\text{V}$ ; $I_{CC} = 10\text{mA}$
Load regulation	$\Delta V_{CC}$	-30	–	25	mV	$0.1\text{mA} < I_{CC} < 30\text{mA}$ ; $V_S = 9\text{V}$ ; $-40^\circ\text{C} < T < 25^\circ\text{C}$
		-25		25		$0.1\text{mA} < I_{CC} < 30\text{mA}$ ; $V_S = 9\text{V}$ ; $25^\circ\text{C} \leq T < 150^\circ\text{C}$
Power supply ripple rejection	PSRR	–	40	–	dB	$V_{SS} = 1\text{V}$ ; $f = 100\text{Hz}$ ; <b>not</b> subject to production test - specified by design
Output current limit	$I_{CCmax}$	155	-	-	mA	1)
Dropvoltage $V_{DR} = V_S - V_{CC}$	$V_{DR}$		0.15	0.45	V	$I_{CC} = 30\text{mA}$ ; see note 1)

#### Wake-up Input WK

Input current	$I_{IL}$	2	10	100	$\mu\text{A}$	
H-input voltage threshold	$V_{IH}$	–	–	$0.7 \times V_{CC}$	V	

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
L-input voltage threshold	$V_{IL}$	$0.2 \times V_{CC}$	–	–	V	
Hysteresis of input voltage	$V_{IHY}$	50	200	500	mV	
Input filtering time	$t_{IFT}$	–	–	3	$\mu\text{s}$	

1) measured when output voltage  $V_{CC}$  dropped 100 mV from the nom. value obtained at 13.5 V inp. voltage  $V_S$

### Oscillator

Oscillator frequency $f_{OSC}$	$f_{OSC}$		125		kHz	+/-15% accuracy
Cycle time (guaranteed by design)	$t_{CYC}$		512		$\mu\text{s}$	64 times frequency divider

### Reset Generator; Pin RO

Reset threshold voltage	$V_{RT}$	4.0	4.3	4.65	V	
Reset low output voltage	$V_{RO}$		0.2	0.4	V	$I_{RO} = 1\text{mA}$ ( $V_{CC} \geq V_{RT}$ ) or $V_{CC} \geq 1\text{V}$ ( $I_{RO} = 200 \mu\text{A}$ )
Reset high output voltage	$V_{RO}$	4.0		$V_{CC} + 0.1$	V	
Reset pull up current	$I_{RO}$	20	150	500	$\mu\text{A}$	$V_{RO} = 0\text{V}$
Reset reaction time	$t_{RR}$	1	3	10	$\mu\text{s}$	$V_{CC} < V_{RT}$ to RO = L; normal, RxD, stand-by mode; $-40^\circ\text{C} < T \leq 85^\circ\text{C}$
		1	3	15	$\mu\text{s}$	$V_{CC} < V_{RT}$ to RO = L; normal, RxD, stand-by mode; $T > 85^\circ\text{C}$
Reset reaction time	$t_{RR}$	–	–	50	$\mu\text{s}$	$V_{CC} < V_{RT}$ to RO = L; cyclic wake mode
Reset delay time (16 cyl.)	$t_{RD}$	6.1	8.1	10.2	ms	

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### 3 V Supervisor; (bit 7 of SPI output word)

Supervisor threshold voltage	$V_{ST}$	2.3	2.7	3.1	V	
Supervisor reaction time	$t_{SR}$	2	8	20	$\mu\text{s}$	not subject to production test - specified by design

#### Watchdog Generator

Watchdog trigger time	$t_{WD}$	7.6	10	12.3	ms	
Closed window time (12 cyl.)	$t_{CW}$	4.6	6.1	7.6	ms	
Open window time (20 cyl.)	$t_{OW}$	7.7	10.2	12.7	ms	
Watchdog reset-pulse time (4 cyl.)	$t_{WDR}$	1.5	2.0	2.6	ms	
Long open window (128 cyl.)	$t_{LOW}$		65		ms	

#### Under-Voltage Lockout (bit 3 of SPI output word)

UV-Switch-ON voltage	$V_{UV\ ON}$	–	5.35	6.00	V	$V_S$ increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	4.50	4.85	5.20	V	$V_S$ decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$

#### PWM Input to control OUTH1; Pin PWM (high active)

H-input voltage threshold	$V_{IH}$	–	–	$0.8 \times V_{CC}$	V	
L-input voltage threshold	$V_{IL}$	$0.2 \times V_{CC}$	–	–	V	
Hysteresis of input voltage	$V_{IHY}$	200	700	1000	mV	
Pull down current	$I_I$	2	10	100	$\mu\text{A}$	$V_I = 0.2 * V_{CC}$

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input capacitance	$C_i$	–	10	15	pF	Not subject to production test - specified by design

### Switches

#### High Side Output OUTH1; (controlled by PWM or bit 1 of SPI input word)

Static Drain-Source ON-Resistance; $I_{\text{OUTH1}} = -0.25 \text{ A}$	$R_{\text{DSON H1}}$	–	1.0	2.0	$\Omega$	
			1.5	4.0	$\Omega$	$5.2 \text{ V} \leq V_S \leq 9 \text{ V}$
Active zener voltage	$V_{\text{OUTH1}}$	-5.0	-3.0	-0.5	V	$I_{\text{OUTH1}} = -0.25 \text{ A}$
Clamp diode forward voltage	$V_{\text{OUTH1}}$		0.8	1	V	$I_{\text{OUTH1}} = 0.25 \text{ A}$
Leakage current	$I_{\text{OLH1}}$	-100	-5	–	$\mu\text{A}$	$V_{\text{OUTH1}} = 0 \text{ V}$
Switch ON delay time	$t_{\text{dONH1}}$		10	100	$\mu\text{s}$	PWM to OUTH1; $R_L = 100 \Omega$
Switch OFF delay time	$t_{\text{dOFFH1}}$		20	100	$\mu\text{s}$	PWM to OUTH1; $R_L = 100 \Omega$
Overcurrent shutdown threshold	$I_{\text{SDH1}}$	-1.0	-0.6	-0.3	A	
Shutdown delay time	$t_{\text{dSDH1}}$	10	25	50	$\mu\text{s}$	
Current limit	$I_{\text{OCLH1}}$	-2.0	-1.0	-0.5	A	

#### High Side Output OUTH2; (controlled by bit 2 of SPI input word)

Static Drain-Source ON-Resistance; $I_{\text{OUTH2}} = -0.25 \text{ A}$	$R_{\text{DSON H2}}$	–	1.0	2.0	$\Omega$	
			1.5	4.0	$\Omega$	$5.2 \text{ V} \leq V_S \leq 9 \text{ V}$
Active zener voltage	$V_{\text{OUTH2}}$	-5.0	-3.0	-0.5	V	$I_{\text{OUTH2}} = -0.25 \text{ A}$
Clamp diode forward voltage	$V_{\text{OUTH2}}$		0.8	1	V	$I_{\text{OUTH2}} = 0.25 \text{ A}$



### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Leakage current	$I_{OLH1}$	-100	-5	–	$\mu\text{A}$	$V_{OUTH2} = 0 \text{ V}$
Switch ON delay time	$t_{dONH1}$		10	100	$\mu\text{s}$	CSN high to OUTH2; $R_L = 100 \Omega$
Switch OFF delay time	$t_{dOFFH1}$		20	100	$\mu\text{s}$	CSN high to OUTH2; $R_L = 100 \Omega$

#### High Side Output OUTH3; (controlled by bit 3 and bit 4 of SPI input word)

Static Drain-Source ON-Resistance; $I_{OUTH3} = -0.25 \text{ A}$	$R_{DSON H3}$	–	1.0	2.0	$\Omega$	
			1.5	4.0	$\Omega$	$5.2 \text{ V} \leq V_S \leq 9 \text{ V}$
Active zener voltage	$V_{OUTH3}$	-5.0	-3.0	-0.5	V	$I_{OUTH3} = -0.25 \text{ A}$
Clamp diode forward voltage	$V_{OUTH3}$		0.8	1	V	$I_{OUTH3} = 0.25 \text{ A}$
Leakage current	$I_{OLH3}$	-100	-5	–	$\mu\text{A}$	$V_{OUTH3} = 0 \text{ V}$
Switch ON delay time	$t_{dONH3}$		10	100	$\mu\text{s}$	CSN high to OUTH3; $R_L = 100 \Omega$
Switch OFF delay time	$t_{dOFFH3}$		20	100	$\mu\text{s}$	CSN high to OUTH3; $R_L = 100 \Omega$

#### Low Side Output OUTL1 ( bit 5 of SPI input word)

Static Drain-Source ON-Resistance; $I_{OUTL1} = 0.1 \text{ A}$	$R_{DSON L1}$	–	1.5	3.0	$\Omega$	
			2.0	5.0	$\Omega$	$5.2 \text{ V} \leq V_S \leq 9 \text{ V}$
Active zener clamp voltage	$V_{OUTL1}$	32	37	42	V	$I_{OUTL1} = +0.1 \text{ A}$
Leakage current	$I_{OLL1}$			5	$\mu\text{A}$	$V_{OUTL1} = 15 \text{ V}$ ; $T_j < 85 \text{ }^\circ\text{C}$
Switch ON delay time	$t_{dONL1}$		5	50	$\mu\text{s}$	CSN high to OUTL1; $R_L = 100 \Omega$
Switch OFF delay time	$t_{dOFFL1}$		5	50	$\mu\text{s}$	CSN high to OUTL1; $R_L = 100 \Omega$

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### Low Side Output OUTL2 ( bit 6 of SPI input word)

Static Drain-Source ON-Resistance; $I_{OUTL2} = 0.1 \text{ A}$	$R_{DSON L2}$	–	1.5	3.0	$\Omega$	
			2.0	5.0	$\Omega$	$5.2 \text{ V} \leq V_S \leq 9 \text{ V}$
Active zener clamp voltage	$V_{OUTL2}$	32	37	42	V	$I_{OUTL2} = +0.1 \text{ A}$
Leakage current	$I_{OLL2}$			5	$\mu\text{A}$	$V_{OUTL2} = 15 \text{ V};$ $T_j < 85^\circ\text{C}$
Switch ON delay time	$t_{dONL2}$		5	50	$\mu\text{s}$	CSN high to OUTL2; $R_L = 100 \Omega$
Switch OFF delay time	$t_{dOFFL2}$		5	50	$\mu\text{s}$	CSN high to OUTL2; $R_L = 100 \Omega$

#### Timebase Test TBT(bit 4 of SPI input word)

HS3 ON timing	$t_{TBON}$		2		cycl.	
HS3 OFF timing	$t_{TBOFF}$		2		cycl.	
# of HS activations for TBT	$n_{TBT}$		3			

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### CAN-Transceiver

##### Receiver Output RxD

HIGH level output voltage	$V_{OH}$	$V_{CC} - 0.9$	–	$V_{CC}$	V	$I_0 = -250 \mu\text{A}$
LOW level output voltage	$V_{OL}$	0	–	0.9	V	$I_0 = 1.25 \text{mA}$

##### Transmission Input TxD

HIGH level input voltage	$V_{IH}$	$0.7 \times V_{CC}$	–	$V_{CC} + 0.3$	V	
LOW level input voltage	$V_{IL}$	-0.3	–	$0.3 \times V_{CC}$	V	
HIGH level input current	$I_{IH}$	-200	-50	-10	$\mu\text{A}$	$V_i = 4 \text{V}$
LOW level input current	$I_{IL}$	-800	-200	-40	$\mu\text{A}$	$V_i = 1 \text{V}$

#### Bus Lines CANL, CANH

Differential receiver recessive-to-dominant threshold voltage	$V_{dRxD(rd)}$	-3.0	-2.5	-2.2	V	$V_{CC} = 5.0 \text{V}$
Differential receiver dominant-to-recessive threshold voltage	$V_{dRxD(dr)}$	-3.2	-2.9	-2.6	V	$V_{CC} = 5.0 \text{V}$
CANH recessive output voltage	$V_{CANH,r}$	0.10	0.15	0.30	V	$TxD = V_{CC}$ ; $R_{RTH} < 4 \text{k}\Omega$
CANL recessive output voltage	$V_{CANL,r}$	$V_{CC} - 0.2$	–	–	V	$TxD = V_{CC}$ ; $R_{RTL} < 4 \text{k}\Omega$
CANH dominant output voltage	$V_{CANH,d}$	$V_{CC} - 1.4$	$V_{CC} - 1.0$	$V_{CC}$	V	$TxD = 0 \text{V}$ ; $I_{CANH} = -40 \text{mA}$

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CANL dominant output voltage	$V_{\text{CANL,d}}$	–	1.0	1.4	V	$T_{\text{xD}} = 0 \text{ V}$ ; $I_{\text{CANL}} = 40 \text{ mA}$
CANH output current	$I_{\text{CANH}}$	– 110	– 80	– 50	mA	$V_{\text{CANH}} = 0 \text{ V}$ ; $T_{\text{xD}} = 0 \text{ V}$
		– 5	0	5	$\mu\text{A}$	cycl. wake mode; $V_{\text{CANH}} = 12 \text{ V}$
CANL output current	$I_{\text{CANL}}$	50	80	110	mA	$V_{\text{CANL}} = 5 \text{ V}$ ; $T_{\text{xD}} = 0 \text{ V}$
		– 5	0	5	$\mu\text{A}$	cycl. wake mode; $V_{\text{CANL}} = 0 \text{ V}$ ; $V_S = 12 \text{ V}$
Voltage detection threshold for short-circuit to battery voltage on CANH and CANL	$V_{\text{det(th)}}$	6.5	7.3	8.0	V	
CANH wake-up voltage threshold	$V_{\text{CANH,wu}}$	1.2	1.9	2.7	V	
CANL wake-up voltage threshold	$V_{\text{CANL,wu}}$	2.2	3.1	3.9	V	
Wake-up voltage threshold hysteresis	$\Delta V_{\text{wu}}$	0.2	–	–	V	
CANH single-ended receiver threshold	$V_{\text{CANH}}$	1.5	2.1	2.6	V	failure cases 3, 5 and 7
CANL single-ended receiver threshold	$V_{\text{CANL}}$	2.4	2.9	3.4	V	failure case 6 and 6a
CANL leakage current	$I_{\text{CANL,IK}}$	– 5	0	5	$\mu\text{A}$	$V_{\text{CC}} = 0 \text{ V}$ ; $V_S = 0 \text{ V}$ ; $V_{\text{CANL}} = 12 \text{ V}$ ; $T_j < 85 \text{ }^\circ\text{C}$
CANH leakage current	$I_{\text{CANH,IK}}$	– 5	0	5	$\mu\text{A}$	$V_{\text{CC}} = 0 \text{ V}$ ; $V_S = 0 \text{ V}$ ; $V_{\text{CANH}} = 5 \text{ V}$ ; $T_j < 85 \text{ }^\circ\text{C}$

### Termination Outputs RTL, RTH

RTL to $V_{\text{CC}}$ switch-on resistance	$R_{\text{RTL}}$	–	40	95	$\Omega$	$I_o = -10 \text{ mA}$
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### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
RTL output voltage	$V_{\text{ORTL}}$	$V_{\text{CC}} - 1.0$	$V_{\text{CC}} - 0.7$	–	V	$ I_{\text{ol}}  < 1 \text{ mA}$ ;
RTL to BAT switch series resistance	$R_{\text{ORTL}}$	5	15	30	k $\Omega$	$V_{\text{BAT}}$ stand-by or cycl. wake mode
RTH to ground switch-on resistance	$R_{\text{RTH}}$	–	40	95	$\Omega$	$I_{\text{o}} = 10 \text{ mA}$
RTH output voltage	$V_{\text{ORTH}}$	–	0.7	1.0	V	$I_{\text{o}} = 1 \text{ mA}$ ; low power mode
RTH pull-down current	$I_{\text{RTH,pd}}$	40	75	120	$\mu\text{A}$	failure cases 6 and 6a
RTL pull-up current	$I_{\text{RTL,pu}}$	– 120	– 75	– 40	$\mu\text{A}$	failure cases 3, 3a, 5 and 7
RTH leakage current	$I_{\text{RTH,lk}}$	– 5	0	5	$\mu\text{A}$	$V_{\text{CC}} = 0 \text{ V}$ ; $V_{\text{S}} = 0 \text{ V}$ ; $V_{\text{RTH}} = 5 \text{ V}$ ; $T_j < 85 \text{ }^\circ\text{C}$
RTL leakage current	$I_{\text{RTL,lk}}$	– 5	0	5	mA	$V_{\text{CC}} = 0 \text{ V}$ ; $V_{\text{S}} = 0 \text{ V}$ ; $V_{\text{RTL}} = 12 \text{ V}$ ; $T_j < 85 \text{ }^\circ\text{C}$

### CAN-Transceiver

#### Dynamic Characteristics

CANH and CANL bus output transition time recessive-to-dominant	$t_{\text{rd}}$	0.6	1.2	2.1	$\mu\text{s}$	10% to 90%; $C_1 = 10 \text{ nF}$ ; $C_2 = 0$ ; $R_1 = 100 \Omega$
CANH and CANL bus output transition time dominant-to-recessive	$t_{\text{dr}}$	0.3	0.6	1.3	$\mu\text{s}$	10% to 90%; $C_1 = 1 \text{ nF}$ ; $C_2 = 0$ ; $R_1 = 100 \Omega$
Minimum dominant time for wake-up on CANL or CANH	$t_{\text{WU(min)}}$	8	22	38	$\mu\text{s}$	stand-by mode; $V_{\text{S}} = 12 \text{ V}$

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Failure cases 3 and 6 detection time	$t_{\text{fail}}$	10	45	80	$\mu\text{s}$	normal operating mode
Failure case 6a detection time		2	4	8	ms	normal operating mode
Failure cases 5, 6, 6a and 7 recovery time		10	45	80	$\mu\text{s}$	normal operating mode
Failure cases 3 recovery time		250	500	750	$\mu\text{s}$	normal operating mode
Failure cases 5 and 7 detection time		1.0	2.0	4.0	ms	normal operating mode
Failure cases 5 detection time		0.4	1.0	2.4	ms	stand-by mode; $V_S = 12 \text{ V}$
Failure cases 6, 6a and 7 detection time		0.8	4.0	8.0	ms	stand-by mode; $V_S = 12 \text{ V}$
Failure cases 5, 6, 6a and 7 recovery time		–	1	–	ms	stand-by mode; $V_S = 12 \text{ V}$
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{\text{PD(L)}}$	–	1.5	2.1	$\mu\text{s}$	$C_1 = 100 \text{ pF}$ ; $C_2 = 0$ ; $R_1 = 100 \Omega$ ; no failures and bus failure cases 1, 2, 3a and 4
		–	1.7	2.4	$\mu\text{s}$	$C_1 = C_2 = 3.3 \text{ nF}$ ; $R_1 = 100 \Omega$ ; no bus failure and failure cases 1, 2, 3a and 4
		–	1.8	2.5	$\mu\text{s}$	$C_1 = 100 \text{ pF}$ ; $C_2 = 0$ ; $R_1 = 100 \Omega$ ; bus failure cases 3, 5, 6, 6a and 7
		–	2.0	2.6	$\mu\text{s}$	$C_1 = C_2 = 3.3 \text{ nF}$ ; $R_1 = 100 \Omega$ ; bus failure cases 3, 5, 6, 6a and 7

**8.3 Electrical Characteristics (cont'd)**

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{PD(H)}$	–	1.2	2.0	$\mu\text{s}$	$C_1 = 100 \text{ pF}$ ; $C_2 = 0$ ; $R_1 = 100 \Omega$ ; no failures and bus failure cases 1, 2, 3a and 4
		–	2.5	3.5	$\mu\text{s}$	$C_1 = C_2 = 3.3 \text{ nF}$ ; $R_1 = 100 \Omega$ ; no bus failure and failure cases 1, 2, 3a and 4
		–	1.0	2.1	$\mu\text{s}$	$C_1 = 100 \text{ pF}$ ; $C_2 = 0$ ; $R_1 = 100 \Omega$ ; bus failure cases 3, 5, 6, 6a and 7
		–	1.5	2.6	$\mu\text{s}$	$C_1 = C_2 = 3.3 \text{ nF}$ ; $R_1 = 100 \Omega$ ; bus failure cases 3, 5, 6, 6a and 7
Edge-count difference (falling edge) between CANH and CANL for failure cases 1, 2, 3a and 4 detection	$n_e$	–	4	–	–	normal operating mode
Edge-count difference (rising edge) between CANH and CANL for failure cases 1, 2, 3a and 4 recovery		–	2	–	–	
TxD permanent dominant disable time	$t_{TxD}$	1.0	2.0	3.5	ms	normal mode

### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### SPI-Interface

##### Logic Inputs DI and CSN

H-input voltage threshold	$V_{IH}$	–	–	$0.7 \times V_{CC}$	V	
L-input voltage threshold	$V_{IL}$	$0.2 \times V_{CC}$	–	–	V	
Hysteresis of input voltage	$V_{IHY}$	50	200	500	mV	
Pull up current at pin CSN	$I_{ICSN}$	-100	-25	-5	$\mu\text{A}$	$V_{CSN} = 0.7 \times V_{CC}$
Pull down current at pin DI	$I_{ICLK/DI}$	5	25	100	$\mu\text{A}$	$V_{DI} = 0.2 \times V_{CC}$
Input capacitance at pin CSN, DI	$C_I$	–	10	15	pF	$0 \text{ V} < V_{CC} < 5.25 \text{ V}$

##### Logic Output DO

H-output voltage level	$V_{DOH}$	$V_{CC} - 1.0$	$V_{CC} - 0.7$	–	V	$I_{DOH} = 1 \text{ mA}$
L-output voltage level	$V_{DOL}$	–	0.2	0.4	V	$I_{DOL} = -1.6 \text{ mA}$
Tri-state leakage current	$I_{DOLK}$	-10	–	10	$\mu\text{A}$	$V_{CSN} = V_{CC}$ $0 \text{ V} < V_{DO} < V_{CC}$
Tri-state input capacitance	$C_{DO}$	–	10	15	pF	$V_{CSN} = V_{CC}$ $0 \text{ V} < V_{CC} < 5.25 \text{ V}$

#### Data Input Timing

*Not subject to production test - specified by design*

Clock period	$t_{pCLK}$	1000	–	–	ns	
Clock high time	$t_{CLKH}$	500	–	–	ns	
Clock low time	$t_{CLKL}$	500	–	–	ns	
Clock low before CSN low	$t_{bef}$	500	–	–	ns	



### 8.3 Electrical Characteristics (cont'd)

9 V <  $V_S$  < 16 V;  $I_{CC} = -100 \mu\text{A}$ ; normal mode; all outputs open;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ; CAN-transceiver circuitry:  $-40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CSN setup time	$t_{\text{lead}}$	500	–	–	ns	
CLK setup time	$t_{\text{lag}}$	500	–	–	ns	
Clock low after CSN high	$t_{\text{beh}}$	500	–	–	ns	
DI setup time	$t_{\text{DISU}}$	250	–	–	ns	
DI hold time	$t_{\text{DIHO}}$	250	–	–	ns	
Input signal rise time at pin DI, CLK and CSN	$t_{\text{rIN}}$	–	–	200	ns	
Input signal fall time at pin DI, CLK and CSN	$t_{\text{fIN}}$	–	–	200	ns	

#### Data Output Timing

DO rise time	$t_{\text{rDO}}$	–	50	100	ns	$C_L = 100 \text{ pF}$
DO fall time	$t_{\text{fDO}}$	–	50	100	ns	$C_L = 100 \text{ pF}$
DO enable time	$t_{\text{ENDO}}$	–	–	250	ns	low impedance
DO disable time	$t_{\text{DISDO}}$	–	–	250	ns	high impedance
DO valid time	$t_{\text{VADO}}$	–	100	250	ns	$V_{\text{DO}} < 0.2 V_{\text{CC}}$ ; $V_{\text{DO}} > 0.7 V_{\text{CC}}$ ; $C_L = 100 \text{ pF}$

## 9 Timing Diagrams

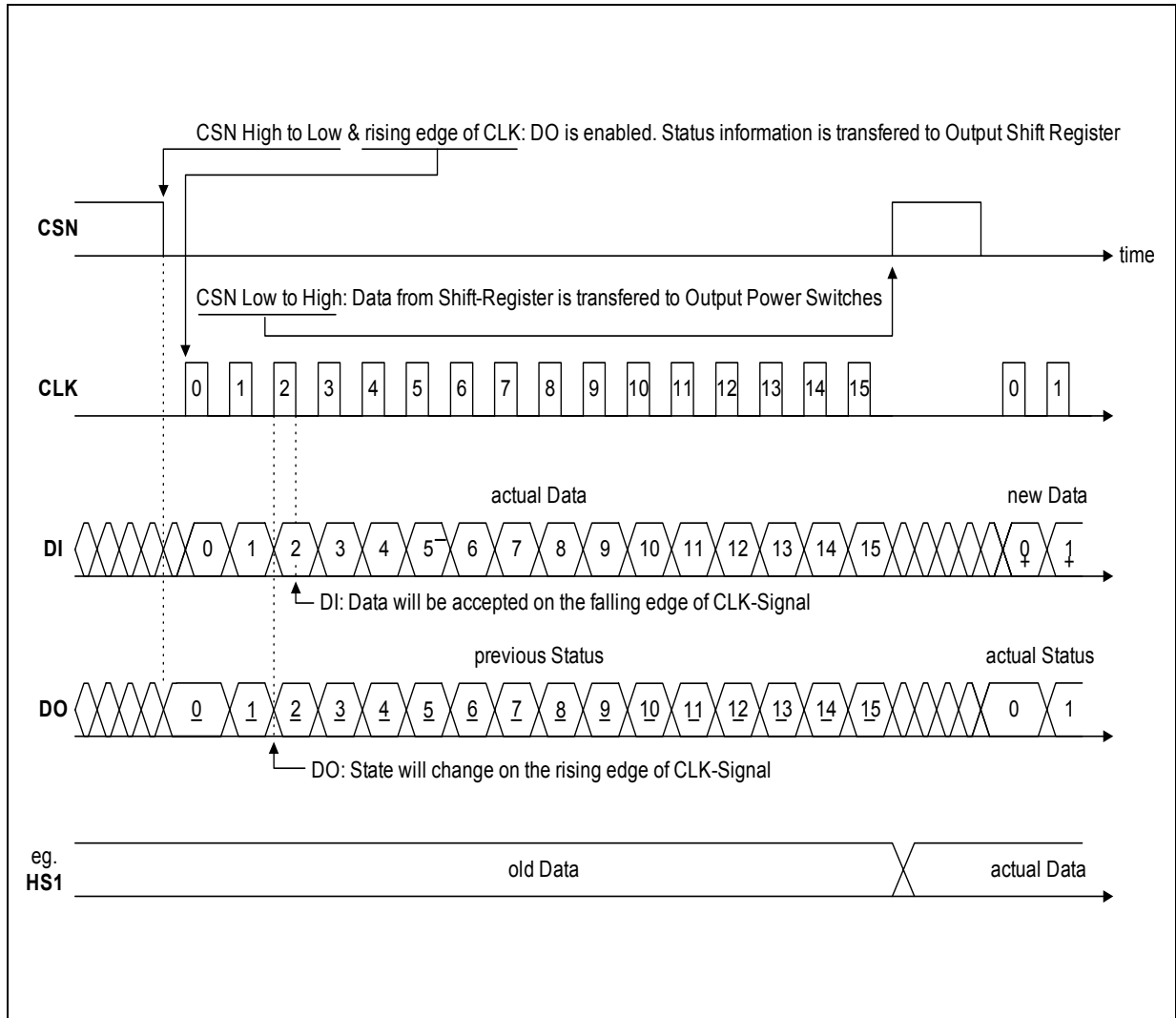


Figure 11 Data Transfer Timing

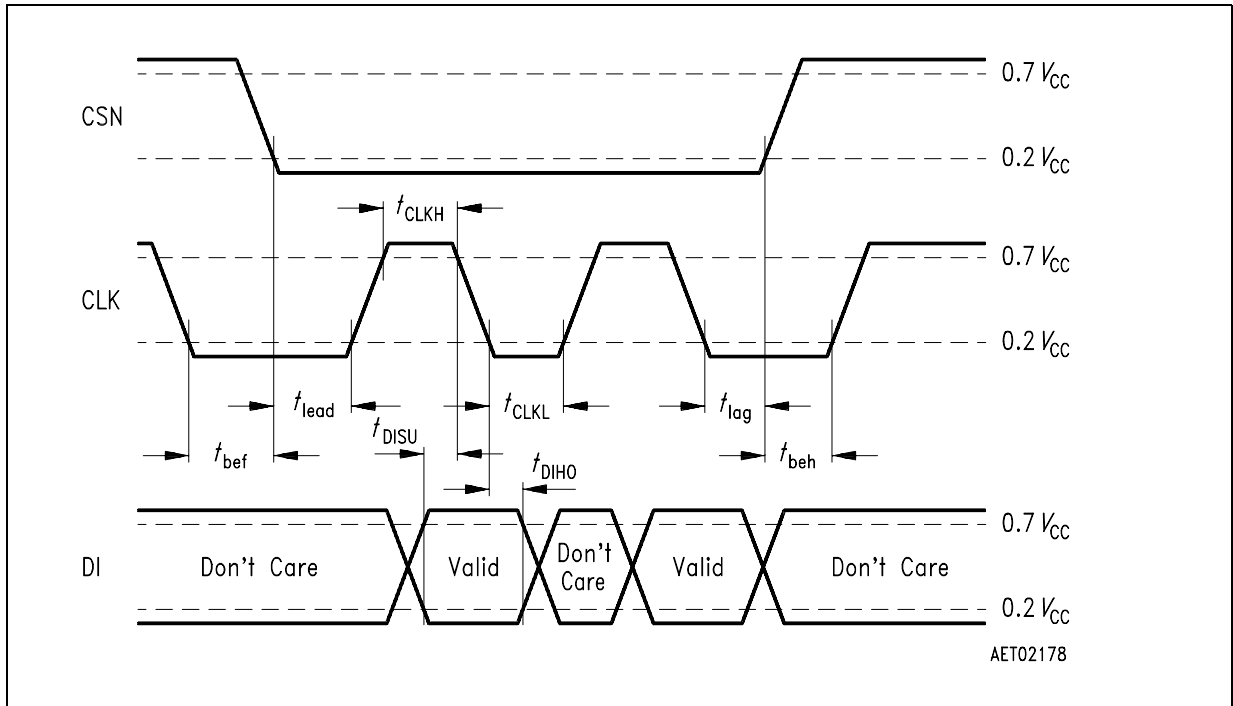


Figure 12 SPI-Input Timing

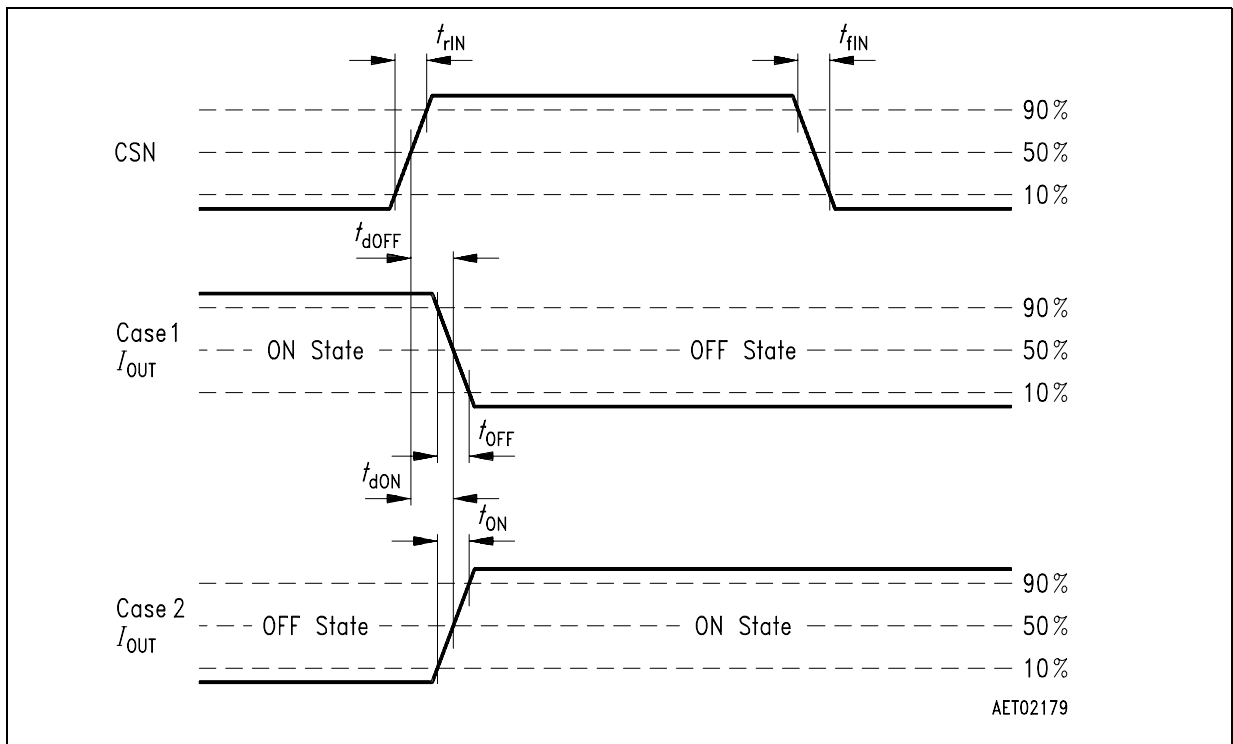


Figure 13 Turn OFF/ON Time

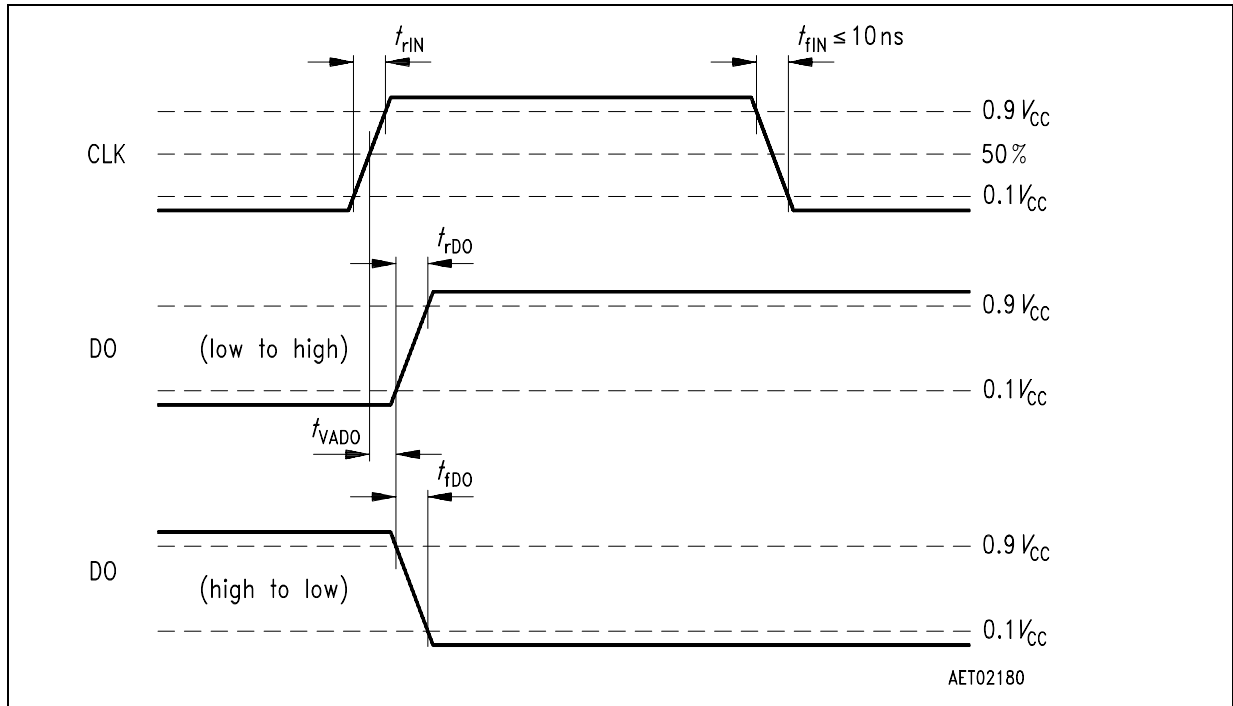


Figure 14 DO Valid Data Delay Time and Valid Time

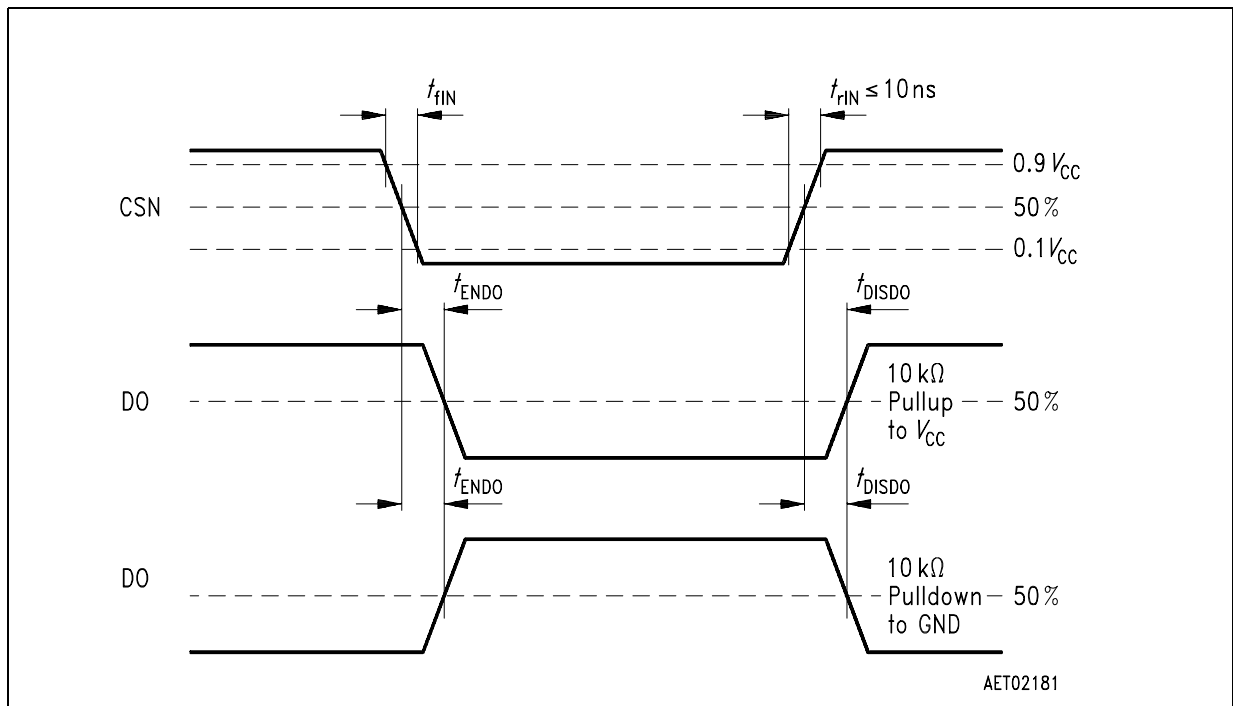


Figure 15 DO Enable and Disable Time

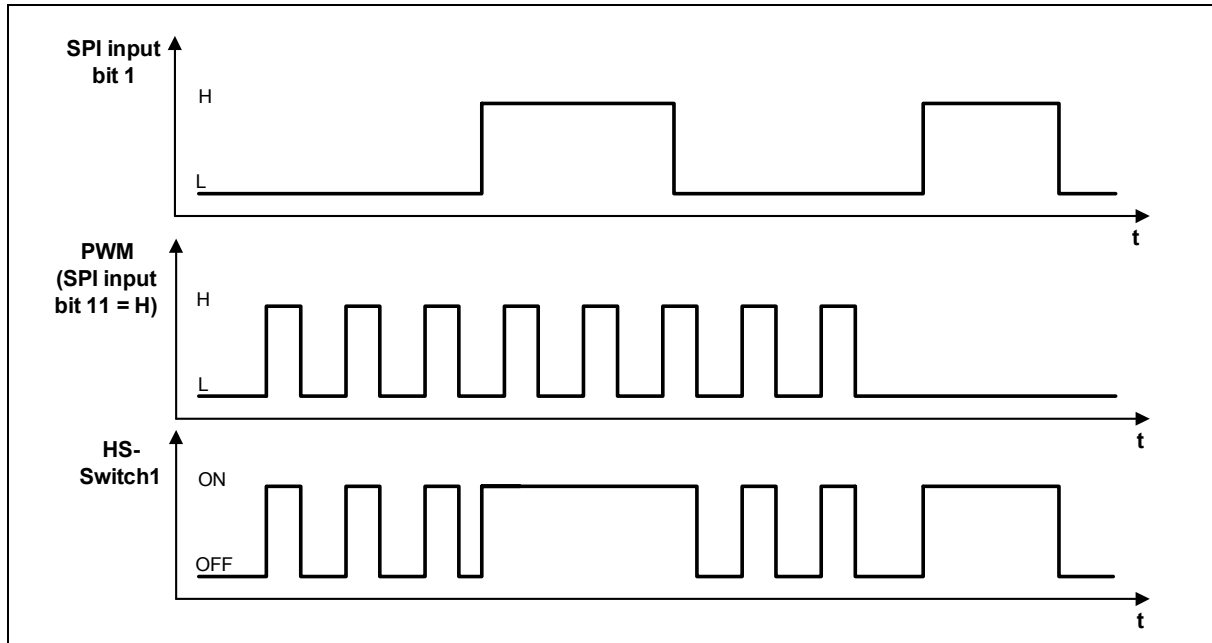


Figure 16 High Side Switch1 Timing Diagram

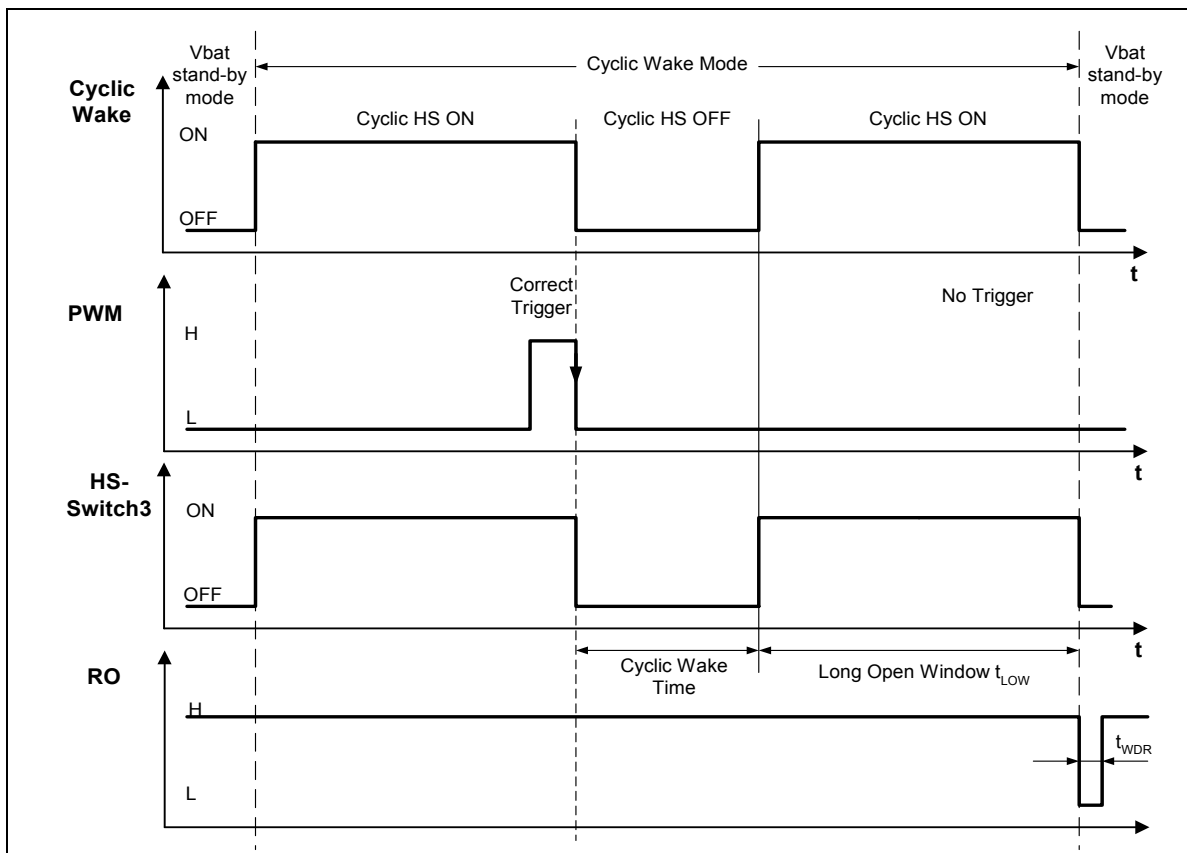


Figure 17 Cyclic Wake Timing Diagram

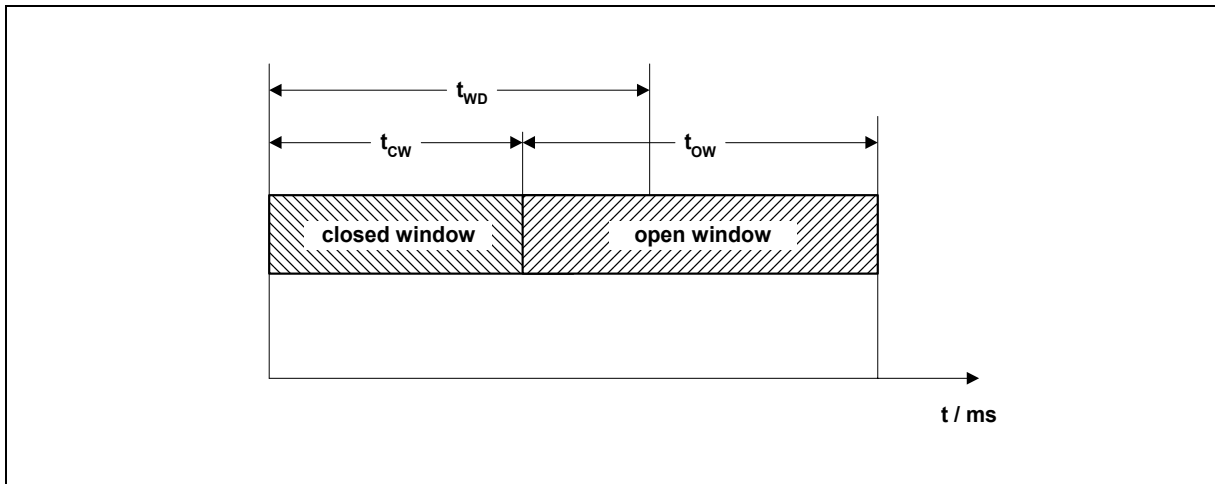


Figure 18 Watchdog Timeout Definitions

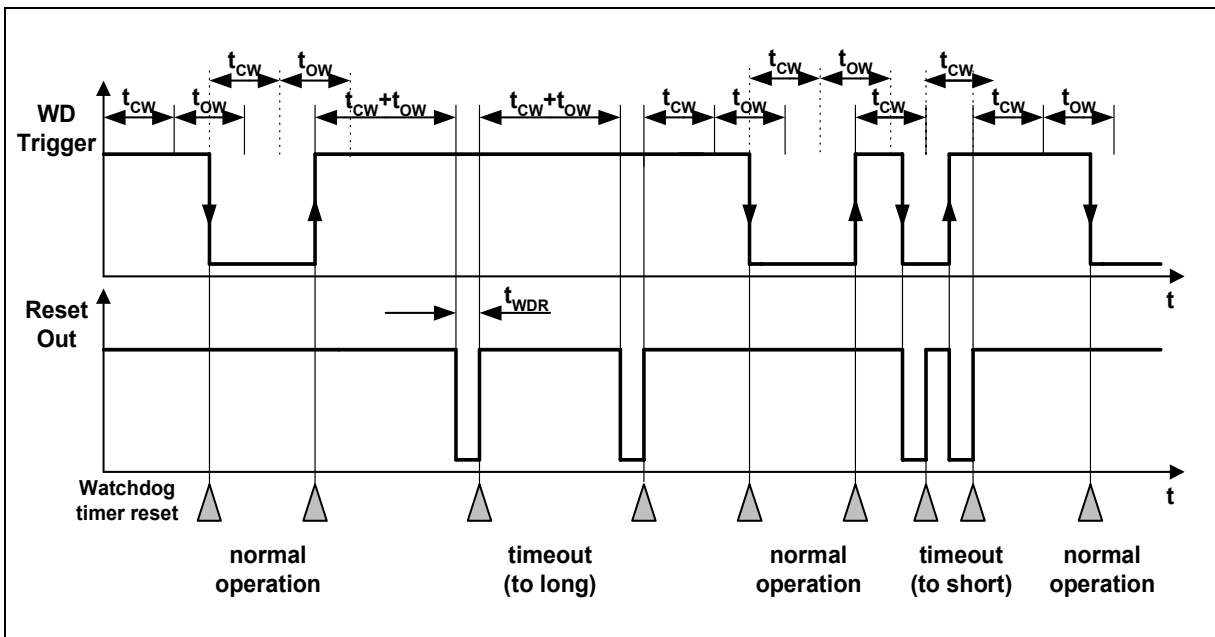


Figure 19 Watchdog Timing Diagram

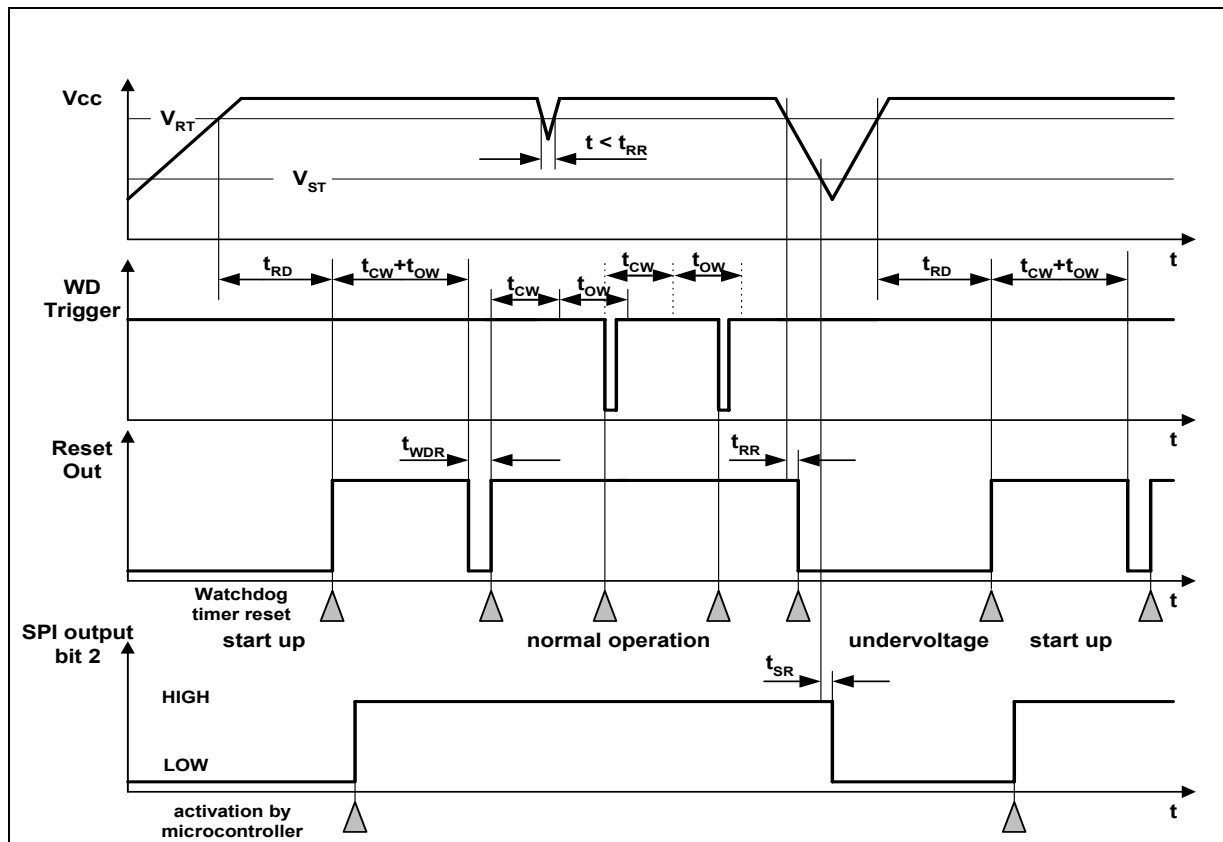


Figure 20 Reset Timing Diagram

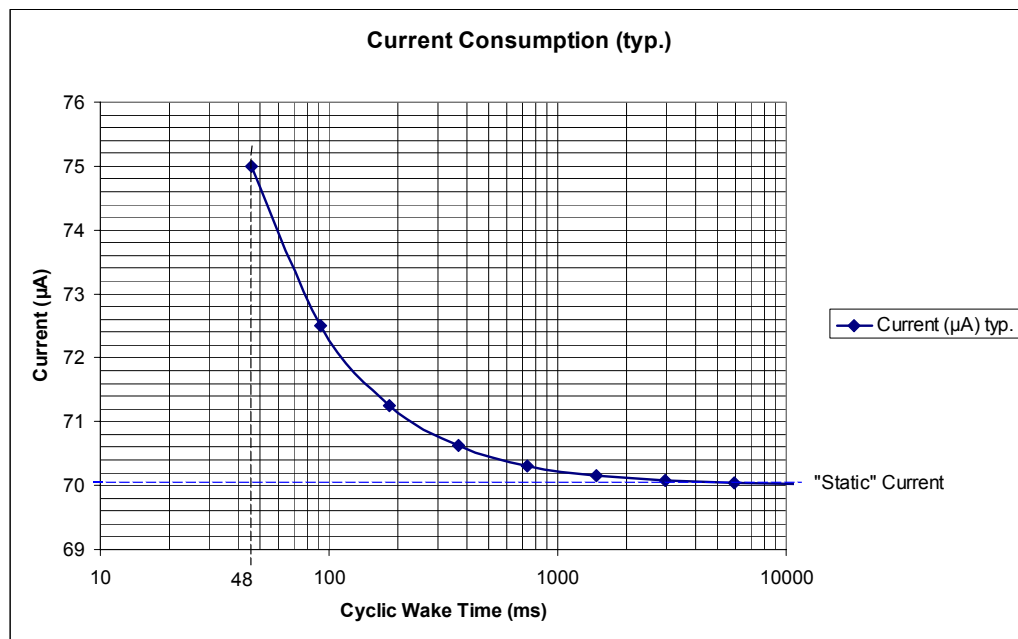


Figure 21 Current Consumption during Cyclic Wake Mode

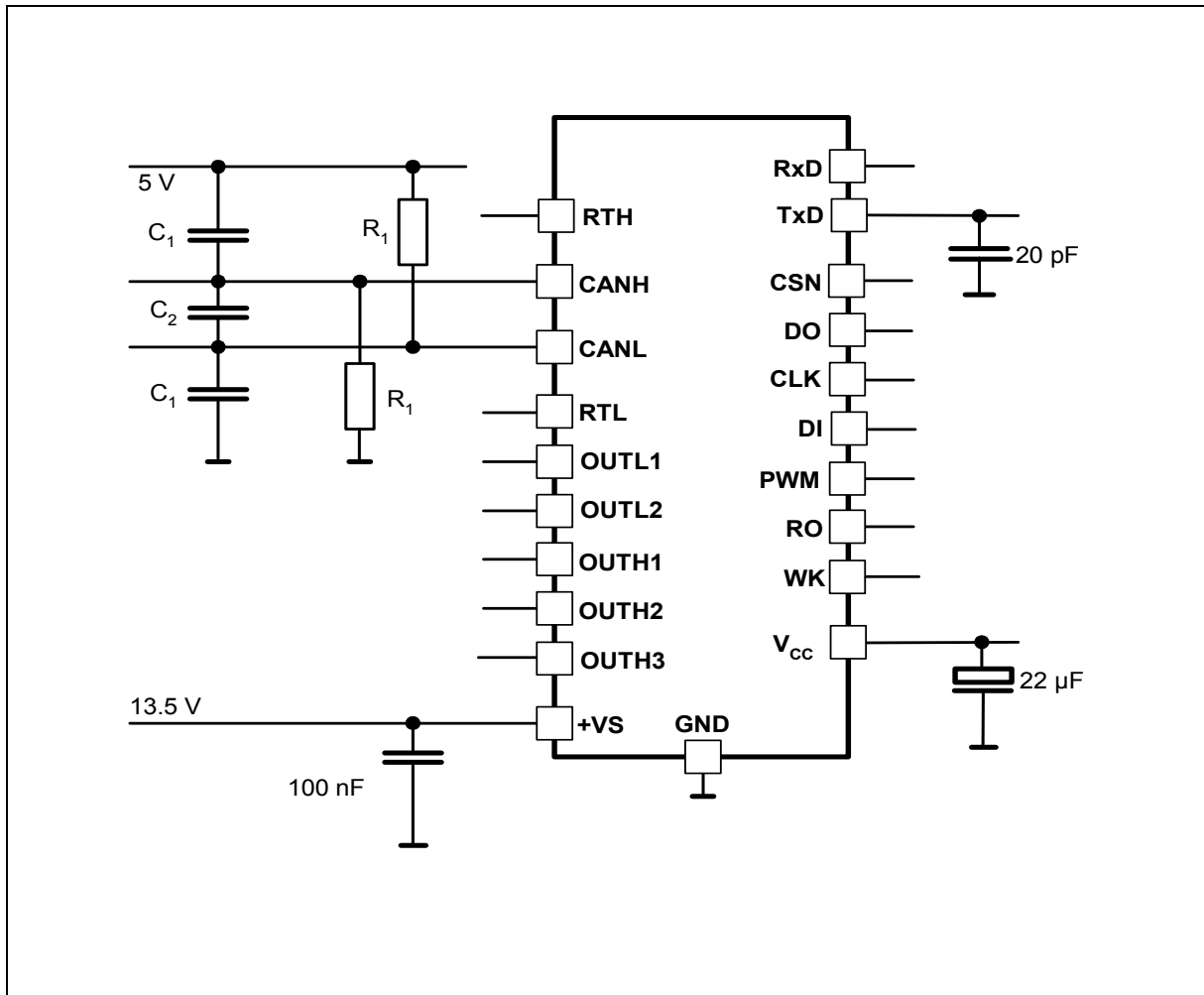


Figure 22 Timing Test Circuit



## 10 Application

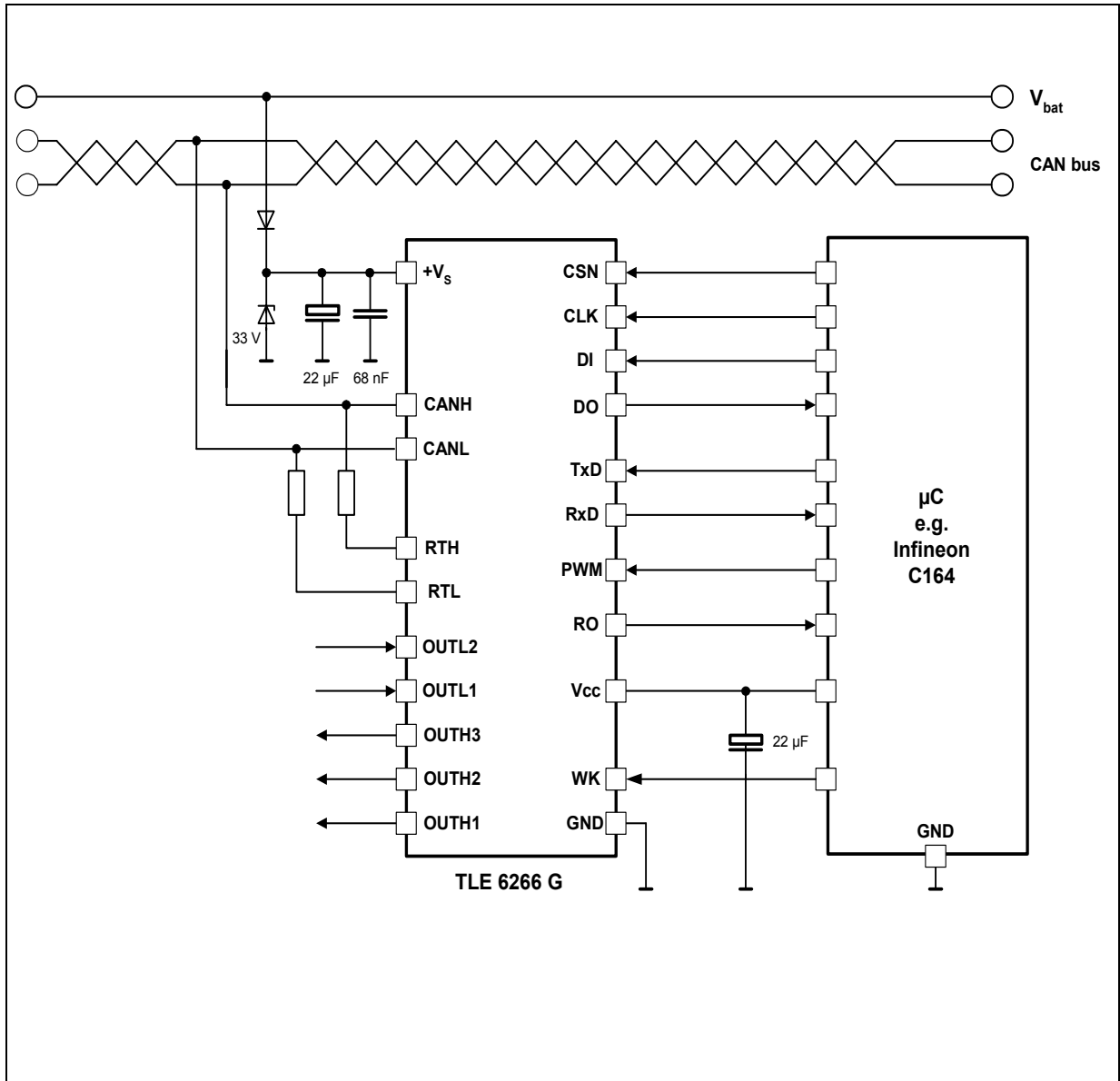
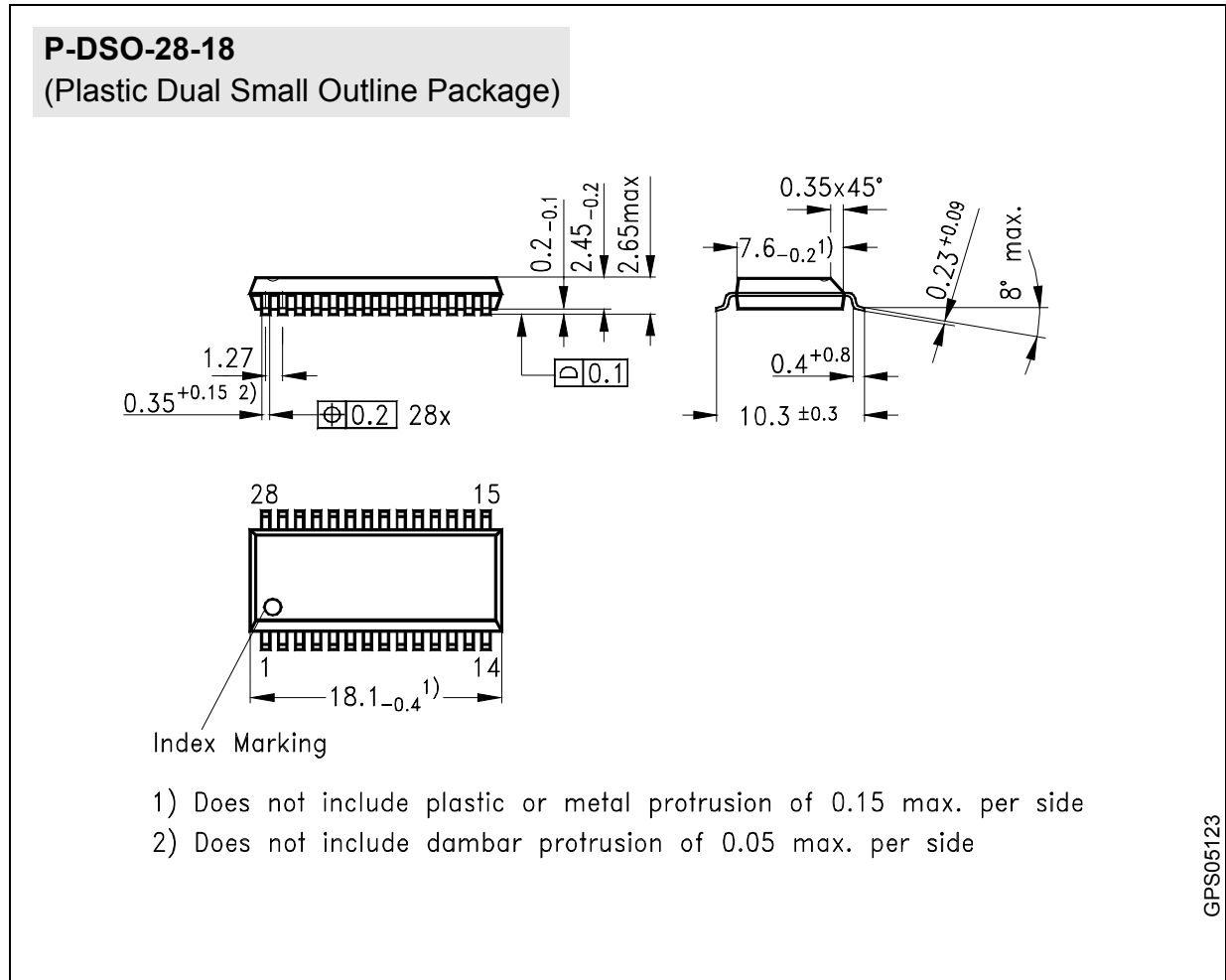


Figure 23 Application Circuit

## 11 Package Outlines



**Figure 24** The P-DSO-28-6 package

### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm