REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change screening and group A inspections. Update table I. Update vendor's part number.	87-06-22	M. A. Frye
B	Make changes to table I, 1.2.2, 1.3, 4.2a, and 4.3.2b. Editorial changes throughout. Make change to table II.	88-06-23	M. A. Frye
C	Add vendor CAGE number 01295 to the drawing as a supplier for device 02. Add burn-in test condition A to 4.2 and 4.3.2. Changes to table I and figure 4, pages 11 and 12. Editorial changes throughout.	89-12-13	M. A. Frye
D	Change to vendor similar Part or Identifying Number (PIN) for vendor CAGE 01295. Editorial changes throughout.	92-03-04	M. A. Frye
E	Update drawing to current requirements. Editorial changes throughout. - gap	02-01-04	Raymond Monnin

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	E																			
SHEET	15																			

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
James E. Jamison

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
86-08-08

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, BIPOLAR, MEMORY, 16 X 48 X 8 FIELD PROGRAMMABLE LOGIC SEQUENCER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-86709**

SHEET 1 OF 15

DSCC FORM 2233
APR 97

5962-E160-02

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86709	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	82S105	16 x 48 x 8, field programmable, logic sequencer, (FPLS)
02	82S105	16 x 48 x 8, field programmable, logic sequencer, (FPLS)

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	GDFP2-F28	28	Flat pack
3	CQCC1-N28	28	Leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage ..... 7.0 V dc maximum
Input voltage ..... 10.0 V dc maximum during programming and 5.5 V dc maximum during operation.
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation 1/ ..... 1.018 W
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}):
Cases X, Y, and 3 ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C
Output sink current 2/ ..... 100 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... 4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH}) ..... 2.0 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.
2/ Not applicable for device type 02.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3.1c), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3	All		0.8	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V	1, 2, 3	All	2		V
Input clamp voltage 2/	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA	1, 2, 3	All		-1.2	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_I = 0.45 V	1, 2, 3	01		-150	µA
		V_I = 0.4 V		02		-250	
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 5.5 V	1, 2, 3	All		50	µA
Clock input current	I_I	V_{CC} = 5.5 V, V_I = 0.45 V	1, 2, 3	01		-350	µA
Low level output voltage 3/	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V V_{IH} = 2 V, I_{OL} = 9.6 mA	1, 2, 3	All		0.5	V
High level output voltage 4/	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V V_{IH} = 2 V, I_{OH} = -2 mA	1, 2, 3	All	2.4		V
Output short-circuit current 2/ 5/	I_{OS}	V_{CC} = 5 V, V_O = 0 V	1, 2, 3	01	-15	-85	mA
		V_{CC} = 5.5 V, V_O = 2.25 V		02	-30	-112	
DC supply current 6/	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	All		185	mA
Three-state output current 7/	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V	1, 2, 3	01		60	µA
		V_{CC} = 5.5 V, V_{OUT} = 2.7 V		02		20	
		V_{CC} = 5.5 V, V_{OUT} = 0.45 V		01		-60	
		V_{CC} = 5.5 V, V_{OUT} = 0.4 V		02		-20	
Functional tests		See 4.3.1d	7, 8				
Propagation delay time, CLK to output	t_{CKO}	V_{CC} = 5.0 V R1 = 470Ω, R2 = 1 kΩ C_L = 30 pF See figure 4	9, 10, 11	01		35	ns
				02		20	
Propagation delay time, $\overline{OE}$ - to output- 8/	t_{OE}		9, 10, 11	01		40	
			9	02		25	
Propagation delay time, $\overline{OE}$ + to output+ 8/	t_{OD}		9	01		40	
				02		15	

See footnotes at end of table.

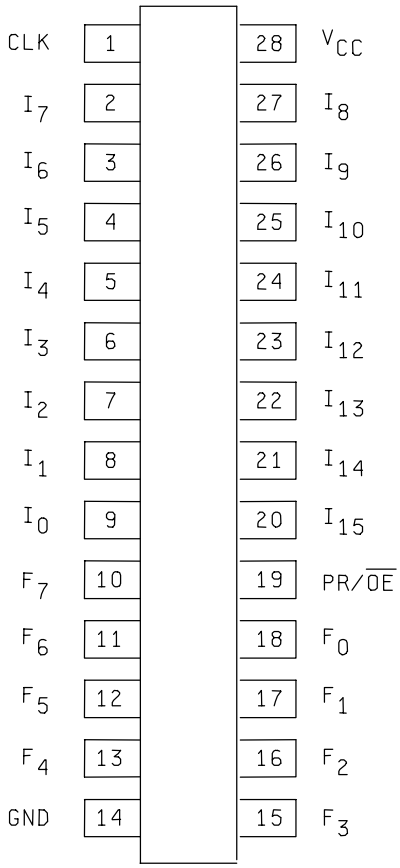
TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, power-on preset	t_{PPR}	$V_{CC} = 5.0\ V$ $R_1 = 470\Omega$, $R_2 = 1\ k\Omega$ $C_L = 30\ pF$, See figure 4	9, 10, 11	All		20	ns
Propagation delay time, preset	t_{PR}			01		45	
				02		25	
Pulse width, CLK high and CLK low 9/	t_{CKH} t_{CKL}			01	40		
				02	12		
Pulse width, CLK period	t_{CKP}			01	95		
				02	24		
Pulse width, CLK period (through complement array) 9/	t_{CKP}			All	135		
Pulse width, preset	t_{PRH}			All	40		
Setup time, input to CLK	t_{IS}			01	60		
				02	18		
Setup time, input to CLK (through complement array) 8/	t_{IS}			01	100		
				02	40		
Setup time, power-on preset	t_{VS}			All	5		
Setup time, preset 8/	t_{PRS}			All	5		
Hold time, CLK to input	t_{IH}			All	10		

1/ All voltage values are with respect to ground.
2/ Test one pin at a time.
3/ Measured with a programmed logic condition for which the output is at a low logic level and V_{IL} applied to PR/$\overline{OE}$. Output sink current is supplied through a resistor to V_{CC}.
4/ Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored or with V_{IH} applied to PR.
5/ Duration of short-circuit should not exceed 1 second.
6/ I_{CC} is measured with the PR/$\overline{OE}$ input grounded and the outputs open.
7/ Measured with V_{IH} applied to PR/$\overline{OE}$.
8/ Not testable on unprogrammed devices.
9/ To prevent spurious clocking, clock rise time (10% to 90%) ≤ 30 ns.

DEVICE TYPES 01 AND 02

CASES X AND Y



CASE 3

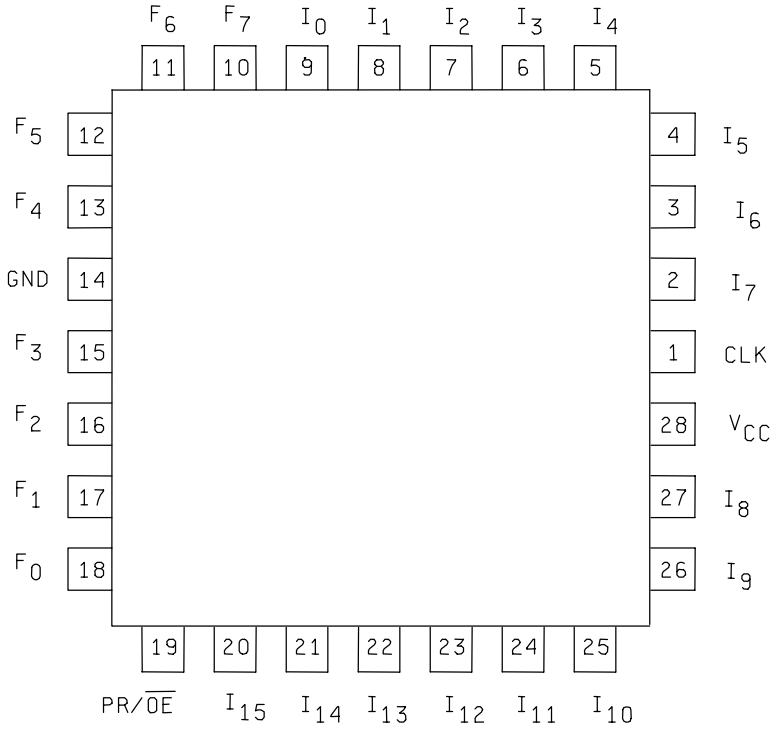


FIGURE 1. Terminal connections.

V_{CC}	Option		I_0	CLK	S	R	$Q_{P/F}$	F
	PR	$\overline{OE}$						
+5 V	H		*	X	X	X	H	H
	L		+10 V	X	X	X	Q_n	$(Q_{p)n}$
	L		X	X	X	X	Q_n	$(Q_{F)n}$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10 V	X	X	X	Q_n	$(Q_{P)n}$
		L	X	X	X	X	Q_n	$(Q_{F)n}$
		L	X	↑	L	L	Q_n	$(Q_{F)n}$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND	IND
↑		X	X	X	X	X	H	

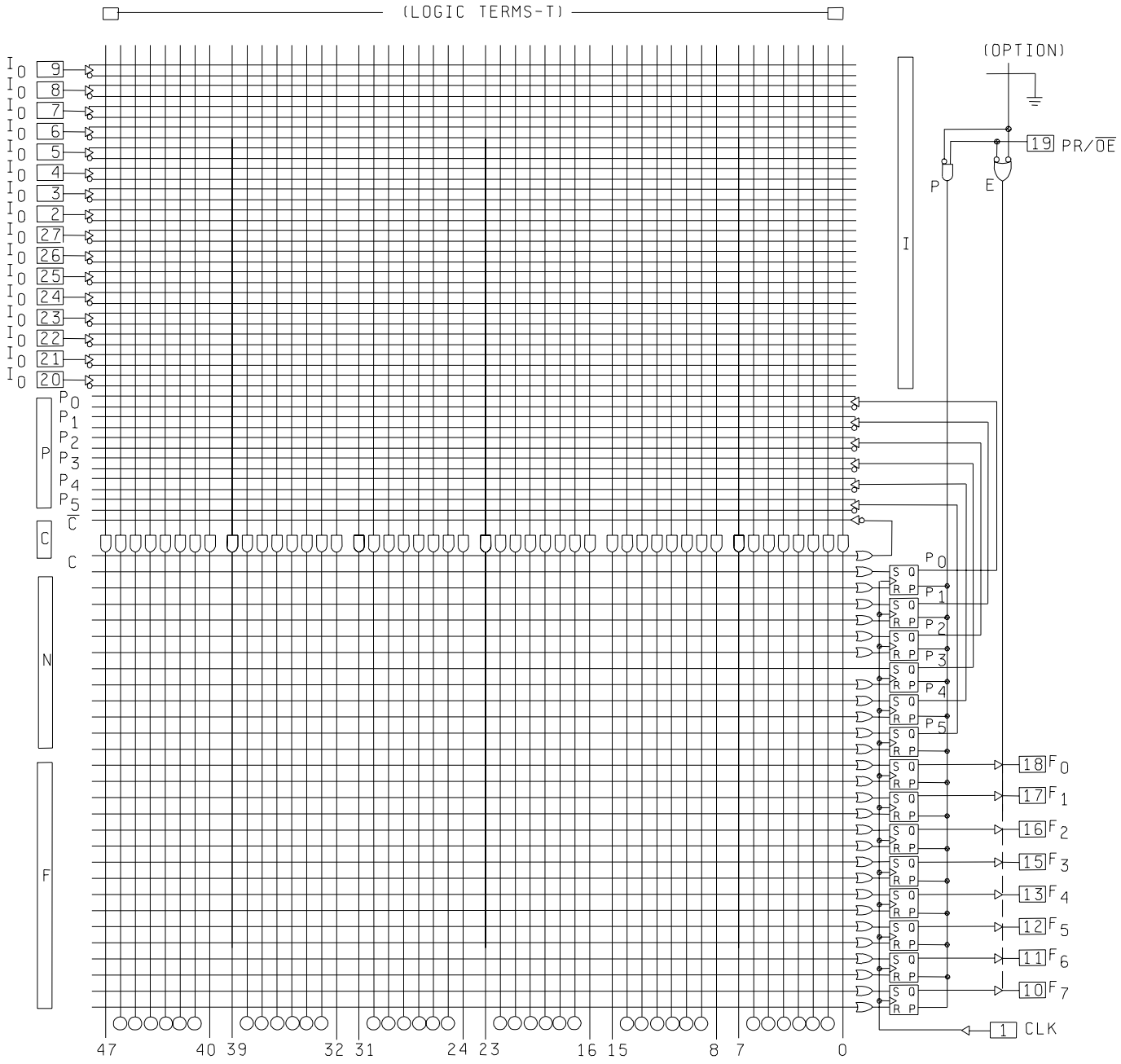
NOTES:

1. Positive logic

   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = (I_0, I_1, I_2)\ (P_0, P_1 \ldots P_5)$

2. Either preset (active-high) or $\overline{\text{output enable}}$ (active low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from low to high level.
4. R = S = High is an illegal input condition
5. * = H/L/+ 10 V
6. X = Don't care (s) ≤ 5.5 V.

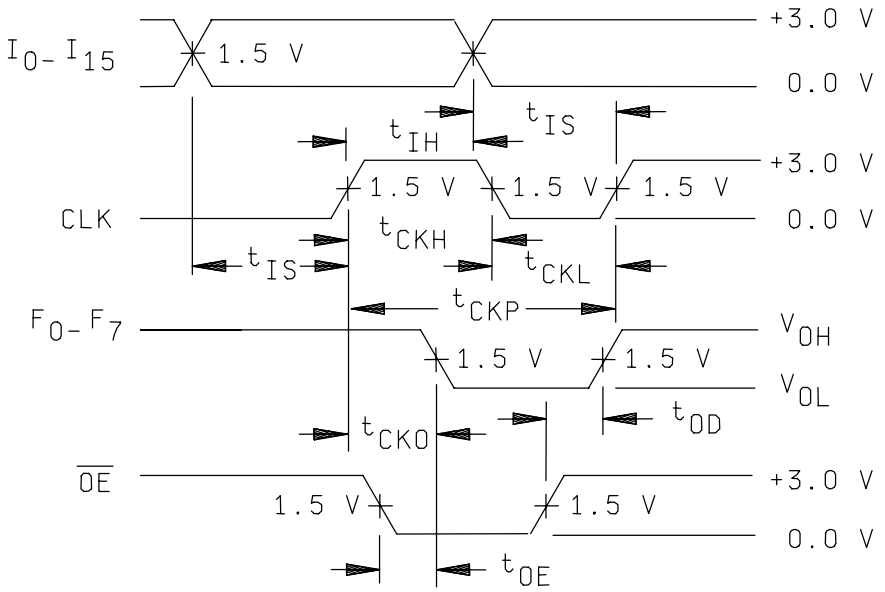
FIGURE 2. Truth table.



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown link float to a logic "0".

FIGURE 3. Logic diagram.

SEQUENTIAL MODE



ASYNCHRONOUS PRESETS

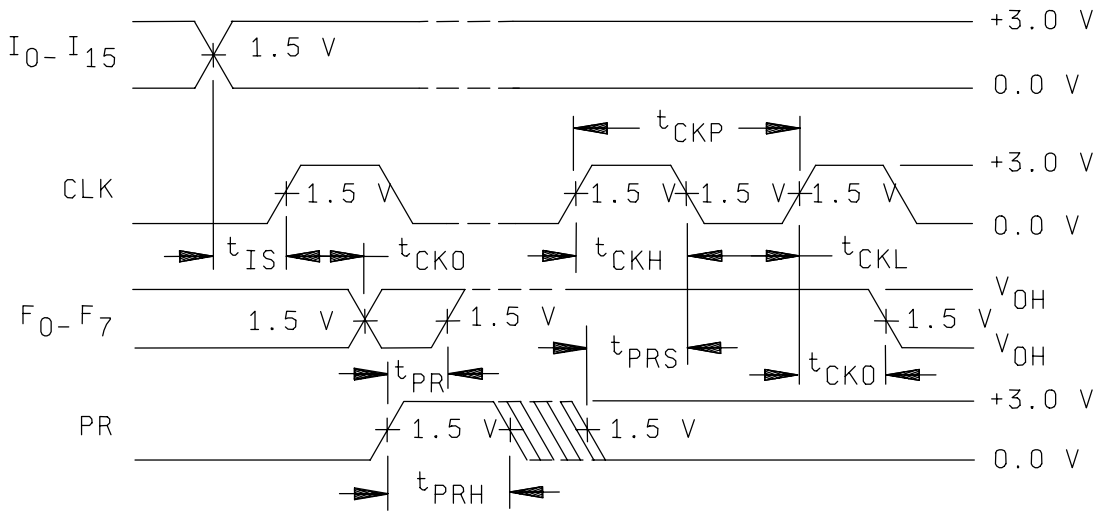
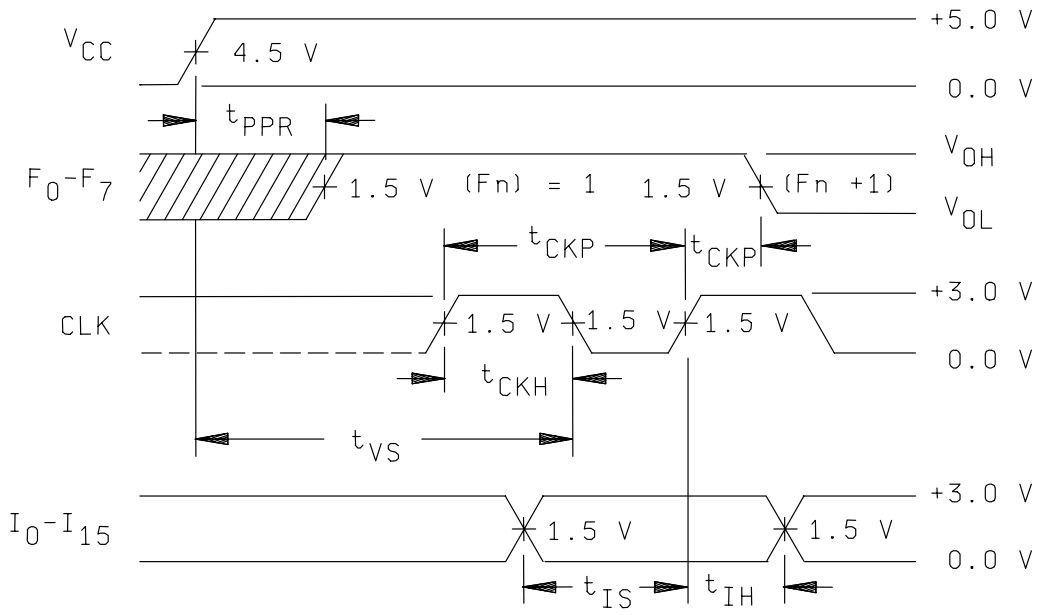
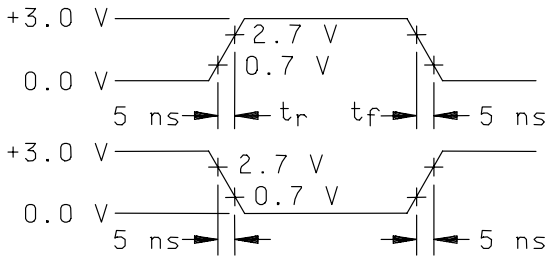


FIGURE 4. Waveforms and test circuit.

POWER-ON PRESET



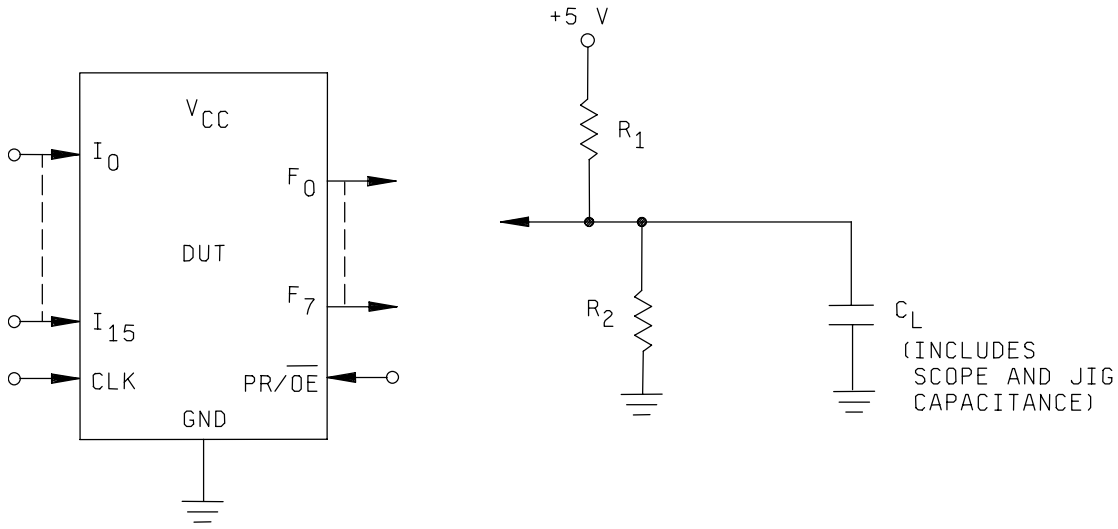
VOLTAGE WAVEFORM



MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5 V LEVEL OF INPUTS AND OUTPUTS, UNLESS OTHERWISE SPECIFIED

FIGURE 5. Waveforms and test circuit - Continued.

TEST LOAD CIRCUIT



NOTE: Voltage values shown in timing diagrams are for device 01 only.
For device 02 those values are:

a. V_{ref} = 1.3 V except for t_{PPR} (voltage waveform) which remains at 1.5 V.
b. Input voltage waveform (voltage waveform) is 0.3 V to 3.5 V.
c. t_r and t_f (voltage waveform) is 10% to 90% of the applied waveform.
d. Test load circuit (voltage waveform): +5 V changes to +7 V.

FIGURE 4. Waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices process to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

1/ * PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined with using high speed testers.
3/ Subgroups 7 and 8 functional tests shall also verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer. The test array function must be deleted prior to programming.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-01-04

Approved sources of supply for SMD 5962-86709 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8670901XA	0C7V7	82S105/BXA
	58625	SL82S105/BXA
5962-8670901YA	0C7V7	82S105/BYA
	58625	SL82S105/BYA
5962-86709013A	0C7V7	82S105/B3A
	58625	SL82S105/B3A
5962-8670902XA	3/	TIB82S105BMJ
5962-8670902YA	3/	TIB82S105BMW
5962-86709023A	3/	TIB82S105BMFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
58625	Lansdale Semiconductor, Inc. 2502 W. Huntington Drive Tempe, AZ 85282-3134
0C7V7	Qualified Parts Laboratory, Inc. 3605 Kifer Road Snata Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.