REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y, add vendor CAGE code 18324.	90-03-08	W. Heckman
B	Corrected supply voltage in 1.3 absolute max ratings. Technical changes to table I. Add new footnote 3/ to table I. Editorial changes throughout.	92-03-16	Monica Poelking
C	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	06-02-08	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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Michael A. Frye

DRAWING APPROVAL DATE
04 April 1989

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, CMOS, DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89532**

SHEET 1 OF 34

DSCC FORM 2233
APR 97

5962-E131-06

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89532	01	Q	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	88C681, 2692	Dual asynchronous receiver/transmitter (DUART)
02	88C681, 2692	Dual asynchronous receiver/transmitter (DUART) with 7-bit input and 8-bit output ports
03	68C681	Dual asynchronous receiver/transmitter (DUART)

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
U	CQCC1-N44	44	Square leadless chip carrier
Y	See figure 1.	52	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 1.0 W
Lead temperature (soldering, 5 seconds) ..... +300°C
Maximum junction temperature (T_J) ..... +175°C
Thermal resistance, junction-to-case (θ_{JC}):
  Cases X, Q, and U ..... See MIL-STD-1835
  Case Y ..... 20°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH}):
  Logic inputs ..... 2.0 V dc
  X1/CLK input ..... 4.0 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Maximum high level output current (I_{OH}) ..... -400 µA
Maximum low level output current (I_{OL}) ..... 2.4 mA
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Input high voltage (except X1/CLK)	V_{IH}				2.0		V
Input high voltage (X1/CLK)	V_{IH}				4.0		V
Output low voltage	V_{OL}	I_{OL} = 2.4 mA, V_{CC} = 4.5 V				0.4	V
Output high voltage (except open collector outputs)	V_{OH}	I_{OH} = -400 µA, V_{CC} = 4.5 V			2.4		V
Input leakage current	I_{IL}	V_I = 0 V to V_{CC}			-25	10	µA
Data bus three-state leakage current	I_{OZL}, I_{OZH}	V_O = 0.4 V to V_{CC}			-10	10	µA
X1/CLK low input current	I_{IL} (X1)	V_I = 0 V, X2 grounded			-6.0	0.0	mA
X1/CLK high input current	I_{IH} (X1)	$V_I = V_{CC}$, X2 grounded			-1.0	1.0	mA
X2 low input current 3/	I_{IL} (X2)	V_I = 0 V, X1/CLK floated			-100	0.0	µA
X2 high input current 3/	I_{IH} (X2)	$V_I = V_{CC}$, X1/CLK floated			0.0	100	µA
Open collector output leakage current	I_{OH}	V_O = 0.4 V to V_{CC}			-10	10	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V				15	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, F_C = 1 MHz See 4.3.1c	4			20	pF
Functional tests		See 4.3.1d	7, 8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reset pulse width	t_{RES}	See figure 4. 4/	9, 10, 11	01, 02	1.0		ns
A0–A3 setup time to RDN, WRN low	t_{AS}				10		ns
A0–A3 hold time from RDN, WRN low	t_{AH}				100		ns
CEN setup time to RDN, WND low	t_{CS}				0		ns
CEN hold time from RDN, WRN high	t_{CH}				0		ns
WRN, RDN pulse width	t_{RW}				225		ns
Data valid after RDN low	t_{DD}					175	ns
Data bus floating after RDN high	t_{DF}					110	ns
Data setup time before WRN high	t_{DS}				100		ns
Data hold time after WRN high	t_{DH}				20		ns
High time between READS and/or WRITES 5/ 6/	t_{RWD}				200		ns
Port input setup time before RDN low	t_{PS}				0		ns
Port input hold time after RDN high	t_{PH}				0		ns
Port output valid after WRN high	t_{PD}					400	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
INTRN (or OP3-OP7 when used as interrupts) negated from:		See figure 4. 4/					
Read RHR (RxRDY/FFULL interrupt)	t_{IR1}		9, 10, 11	01, 02		325	ns
Write THR (TxRDY interrupt	t_{IR2}					325	ns
Reset command (delta break interrupt)	t_{IR3}					325	ns
Stop C/T command (counter interrupt)	t_{IR4}					325	ns
Read IPCR (input port change interrupt)	t_{IR5}					325	ns
Write IMR (clear of interrupt mask bit)	t_{IR6}					325	ns
X1/CLK high or low time	t_{CLK}				100		ns
X1/CLK frequency	f_{CLK}				2.0	4.0	MHz
CTCLK (IP2) high or low time	t_{CTC}				100		ns
CTCLK (IP2) frequency 7/	f_{CTC}				0	4.0	MHz
RxC high or low time	t_{RX}				220		ns
RxC frequency (16X) 7/	f_{RX}				0	2.0	MHz
RxC frequency (1X) 7/	f_{RX}				0	1.0	MHz
TxC high or low time	t_{TX}				220		ns
TxC frequency (16X) 7/	f_{TX}				0	2.0	MHz
TxC frequency (1X) 7/	f_{TX}				0	1.0	MHz
TxD output delay from TxC low	t_{TXD}					350	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output delay from TxC low to TxD data output	t_{TCS}	See figure 4. 4/	9, 10, 11	01, 02	0	150	ns
RxD data setup time to RxC high	t_{RXS}				240		ns
RxD data hold time from RxC high	t_{RXH}				200		ns
RESETN pulse width	t_{RES}			03	1.0		µs
A1-A4 setup to CSN low	t_{AS}				10		ns
A1-A4 hold time from CSN high	t_{AH}				0		ns
R/WN setup time to CSN high	t_{RWS}				0		ns
R/WN holdup time to CSN high	t_{RWH}				0		ns
CSN high pulse width 8/	t_{CSW}				90		ns
CSN or IACKN high from DTACKN low 9/	t_{CSD}				20		ns
Data valid from CSN or IACKN low	t_{DD}					175	ns
Data bus floating from CSN or IACKN high	t_{DF}					100	ns
Data setup time to CLK high	t_{DS}				100		ns
Data hold time from CSN high	t_{DH}				0		ns
DTACKN low from read data	t_{DAL}				0		ns
DTACKN low (read cycle) from CLK high	t_{DCR}					125	ns
DTACKN low (write cycle) from CLK high	t_{DCW}					125	ns
DTACKN high from CSN or IACKN high	t_{DAH}					100	ns
DTACKN high impedance from CSN or IACKN high	t_{DAT}					125	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CSN or IACKN setup time to clock high 10/	t_{CSC}	See figure 4. 4/	9, 10, 11	03	90		ns
Port input setup to CSN low	t_{PS}				0		ns
Port input hold time CSN high	t_{PH}				0		ns
Port output valid from CSN high	t_{PD}					400	ns
INTRN, or OP3-OP7 when used as interrupts, negated from:							
Read RHR (RxRDY/FFULL interrupts)	t_{IR1}		9, 10, 11	03		325	ns
Write THR (TxRDY interrupt)	t_{IR2}					325	ns
Reset command (delta break interrupt)	t_{IR3}					325	ns
Stop C/T command (counter interrupts)	t_{IR4}					325	ns
Read IPCR (input port change interrupt)	t_{IR5}					325	ns
Write IMR (clear of interrupt mask bit)	t_{IR6}					325	ns
X1/CLK high or low time	t_{CLK}				100		ns
X1/CLK frequency	f_{CLK}				2.0	4.0	MHz
CTCLK high or low time	t_{CTC}				100		ns
CTCLK frequency	f_{CTC}				0	4.0	MHz
RxC high or low time	t_{RX}				220		ns
RxC frequency (16X)	f_{RX}				0	2.0	MHz
RxC frequency (1X)	f_{RX}				0	1.0	MHz

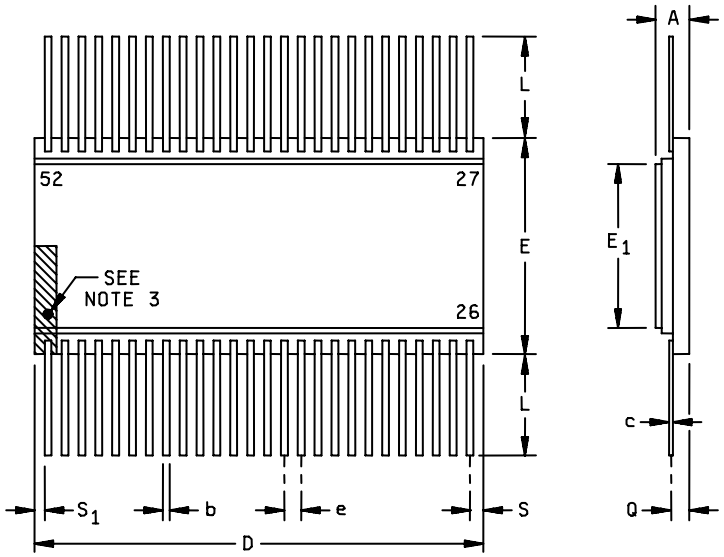
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TxC high or low time	t_{TX}	See figure 4. 4/	9, 10, 11	03	220		ns
TxC frequency (16X)	f_{TX}				0	2.0	MHz
TxC frequency (1X)	f_{TX}				0	1.0	MHz
TxD output delay from TxC low	t_{TXD}					350	ns
Output delay from TxC low to TxD data output	t_{TCS}				0	150	ns
RxD data setup time to RxC high	t_{RXS}				240		ns
RxD data hold time from RxC high	t_{RXH}				200		ns

1/ All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4 V and 2.4 V with a transition time of < 20 ns. For X1/CLK this swing is between 0.4 V and 4.4 V. All time measurements referenced at input voltages of 0.8 V and 2.0 V as appropriate.
2/ Test condition for outputs: C_L = 150 pF tied to ground, except interrupt outputs.
Test condition for interrupt outputs: C_L = 50 pF tied to ground, R_L = 2.7 kΩ to V_{CC}.
3/ For CMOS technology: $I_{IL(X2)}$ X1/CLK = V_{CC}, $I_{IH(X2)}$ X1/CLK = 0.0 V.
4/ Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the "strobing" input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN. CEN and RDN (also CEN and WRN) are AND'ed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
5/ If CEN is used as the "strobing" input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
6/ Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
7/ Minimum frequencies may not be tested, but are guaranteed by design.
8/ This specification will impose maximum 68000 CPU CLK to 6 MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
9/ This specification imposed a lower bound on CSN and IACKN low, guaranteeing that it will be low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
10/ This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.

Case Y



TOP VIEW

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.045	.100	1.14	2.54	
b	.015	.026	0.38	0.66	7
c	.008	.015	0.20	0.38	7
D	---	1.330	---	33.78	4
E	.620	.660	15.75	16.76	
E_1	.488	.498	12.40	12.65	
e	.050 BSC		1.27 BSC		5
L	.250	.370	6.35	9.40	
Q	.054	.066	1.37	1.68	6
S	---	.045	---	1.14	
S_1	.005	---	0.13	---	

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are for general information only.
3. A lead tap (enlargement) or index dot is located within the shaded area shown at pin 1. Other pin numbers proceed sequentially from pin 1 counterclockwise (as viewed from the top of the device).
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The reference pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline is located within ±.005 (0.13 mm) of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured at the point of exit of the lead body.
7. Lead dimensions include .003 inch allowance for hot solder dip lead finish.

FIGURE 1. Case outlines.

Device type:		01	
Case outline:		X	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	15	INTRN
2	A1	16	D6
3	A2	17	D4
4	A3	18	D2
5	WRN	19	D0
6	RDN	20	OP0
7	RxDB	21	TxDA
8	TxDB	22	RxDA
9	OP1	23	X1/CLK
10	D1	24	X2
11	D3	25	RESET
12	D5	26	CEN
13	D7	27	IP2
14	GND	28	V_{CC}

Device type:		02	
Case outline:		Q	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	21	INTRN
2	IP3	22	D6
3	A1	23	D4
4	IP1	24	D2
5	A2	25	D0
6	A3	26	OP6
7	IP0	27	OP4
8	WRN	28	OP2
9	RDN	29	OP0
10	RxDB	30	TxDA
11	TxDB	31	RxDA
12	OP1	32	X1/CLK
13	OP3	33	X2
14	OP5	34	RESET
15	OP7	35	CEN
16	D1	36	IP2
17	D3	37	IP6
18	D5	38	IP5
19	D7	39	IP4
20	GND	40	V_{CC}

FIGURE 2. Terminal connections.

Device type:		02					
Case outline:		U					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	12	NC	23	NC	34	NC
2	A0	13	TxDB	24	INTRN	35	RxDA
3	IP3	14	OP1	25	D6	36	X1/CLK
4	A1	15	OP3	26	D4	37	X2
5	IP1	16	OP5	27	D2	38	RESET
6	A2	17	OP7	28	D0	39	CEN
7	A3	18	D1	29	OP6	40	IP2
8	IP0	19	D3	30	OP4	41	IP6
9	WRN	20	D5	31	OP2	42	IP5
10	RDN	21	D7	32	OP0	43	IP4
11	RxDB	22	GND	33	TxDA	44	V_{CC}

NC = No connection.

Device type:		02					
Case outline:		Y					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	14	TxDB	27	INTRN	40	RxDA
2	IP3	15	OP1	28	D6	41	X1/CLK
3	A1	16	OP3	29	D4	42	X2
4	IP1	17	OP5	30	D2	43	RESET
5	A2	18	OP7	31	D0	44	CEN
6	A3	19	NC	32	NC	45	NC
7	NC	20	NC	33	NC	46	NC
8	NC	21	NC	34	NC	47	NC
9	NC	22	D1	35	OP6	48	IP2
10	IP0	23	D3	36	OP4	49	IP6
11	WRN	24	D5	37	OP2	50	IP5
12	RDN	25	D7	38	OP0	51	IP4
13	RxDB	26	GND	39	TxDA	52	V_{CC}

NC = No connection.

FIGURE 2. Terminal connections - Continued.

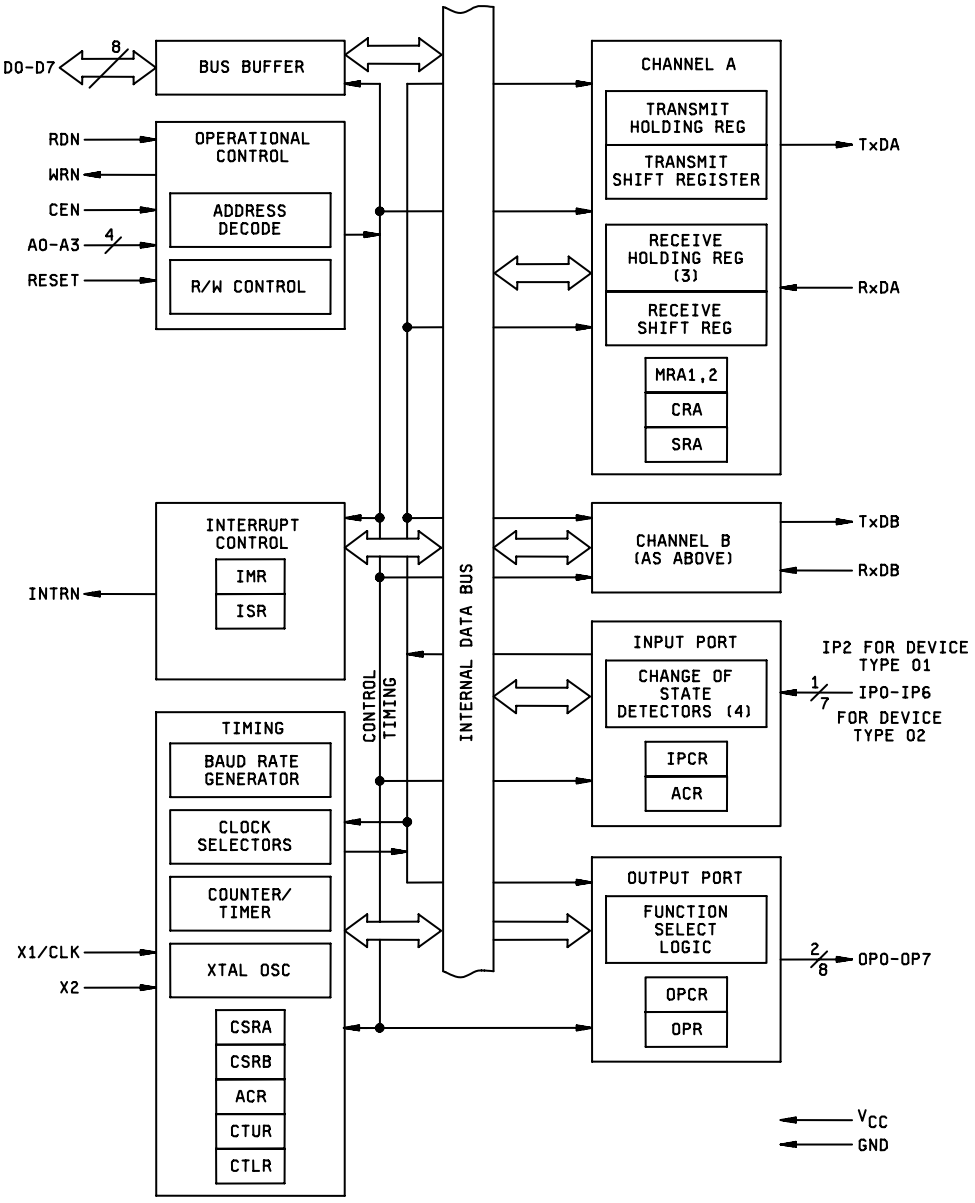
Device type:		03	
Case outline:		Q	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A1	21	INTRN
2	IP3	22	D6
3	A2	23	D4
4	IP1	24	D2
5	A3	25	D0
6	A4	26	OP6
7	IP0	27	OP4
8	R/WN	28	OP2
9	DTACKN	29	OP0
10	RxDB	30	TxDA
11	TxDB	31	RxDA
12	OP1	32	X1/CLK
13	OP3	33	X2
14	OP5	34	RESETN
15	OP7	35	CSN
16	D1	36	IP2
17	D3	37	IACKN
18	D5	38	IP5
19	D7	39	IP4
20	GND	40	V_{CC}

Device type:		03					
Case outline:		U					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	12	NC	23	NC	34	NC
2	A1	13	TxDB	24	INTRN	35	RxDA
3	IP3	14	OP1	25	D6	36	X1/CLK
4	A2	15	OP3	26	D4	37	X2
5	IP1	16	OP5	27	D2	38	RESETN
6	A3	17	OP7	28	D0	39	CSN
7	A4	18	D1	29	OP6	40	IP2
8	IP0	19	D3	30	OP4	41	IACKN
9	R/WN	20	D5	31	OP2	42	IP5
10	DTACKN	21	D7	32	OP0	43	IP4
11	RxDB	22	GND	33	TxDA	44	V_{CC}

NC = No connection.

FIGURE 2. Terminal connections - Continued.

Device types 01 and 02



NOTE: Device type 01 does not have 7-bit input port and 8-bit output port (see 6.7 pin descriptions).

FIGURE 3. Functional block diagram.

Device type 03

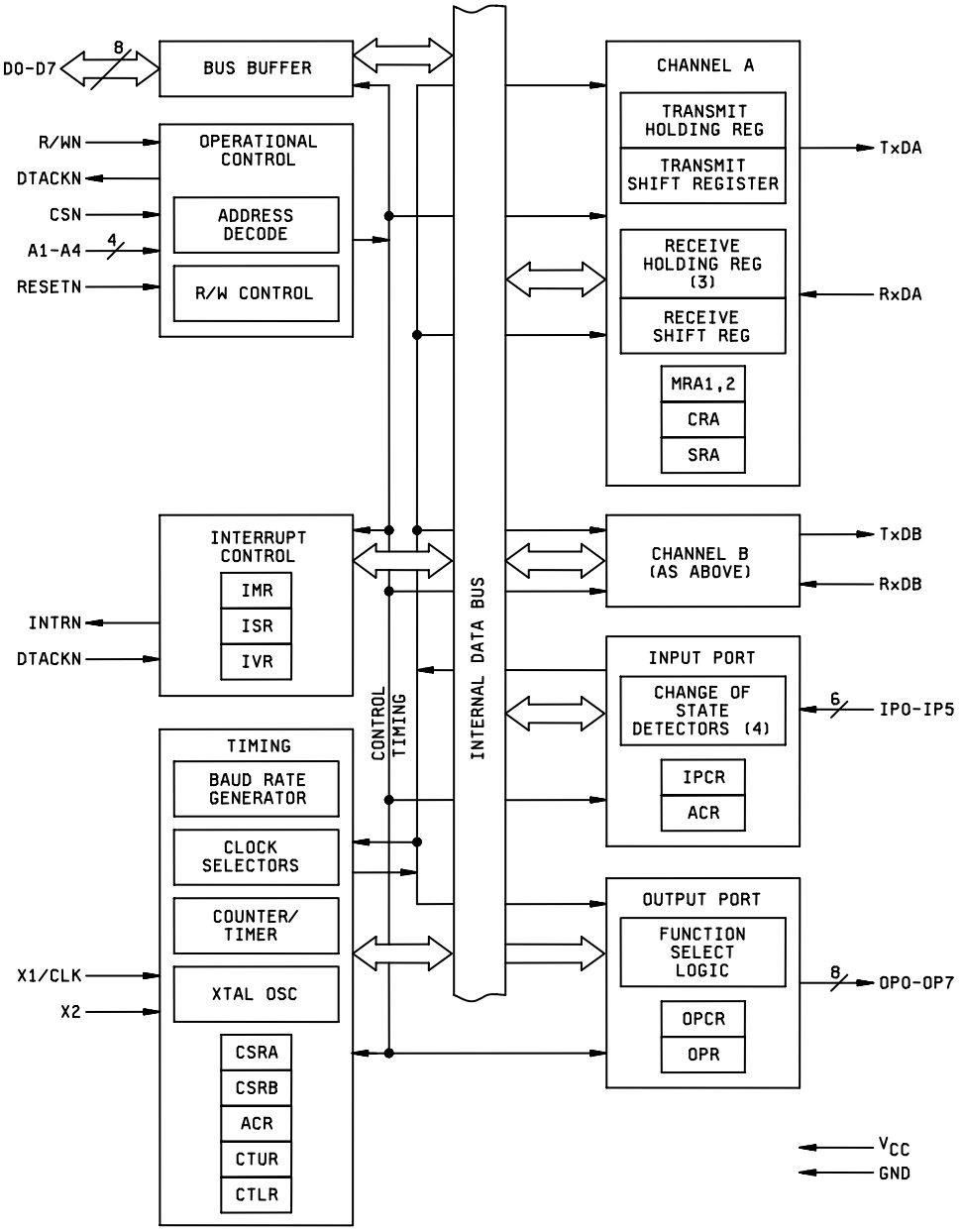


FIGURE 3. Functional block diagram - Continued.

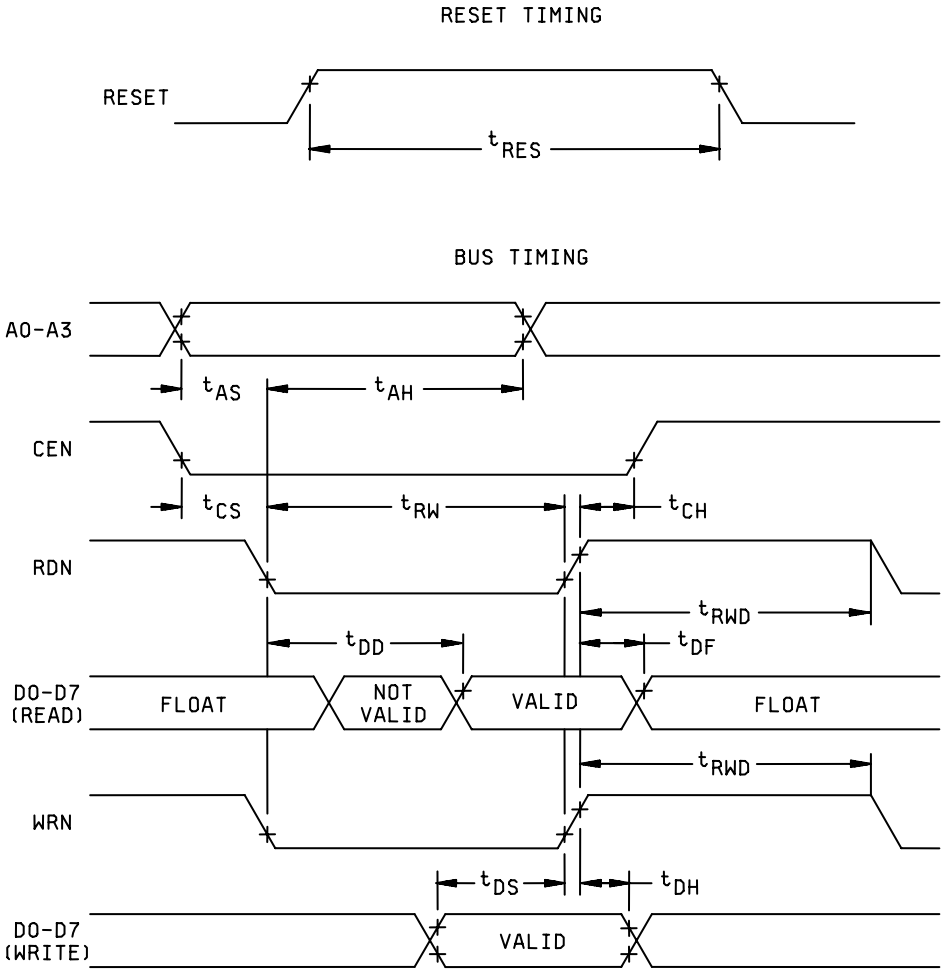
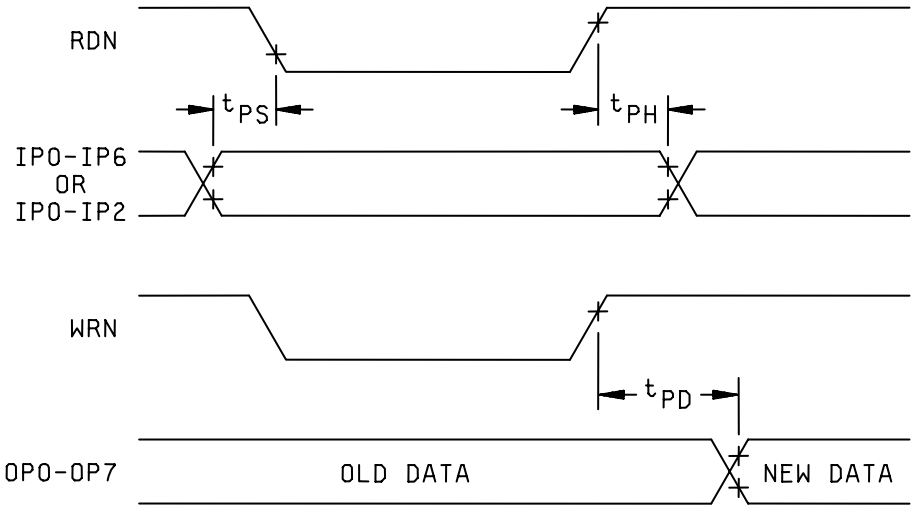
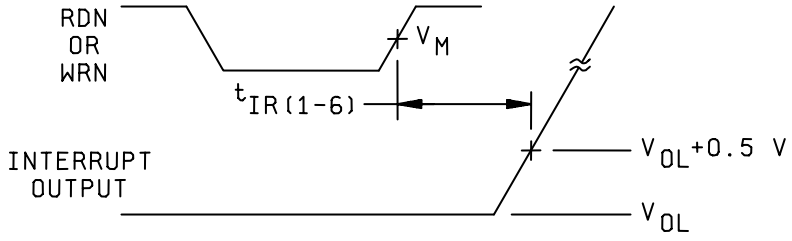


FIGURE 4. Timing waveforms and test circuits.

PORT TIMING



INTERRUPT TIMING



NOTES:
1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of the response is referenced from the midpoint of the switching signal, V_M, to a point 0.5 V above V_{OL}. This point represents the noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

FIGURE 4. Timing waveforms and test circuits - Continued.

Device types 01 and 02

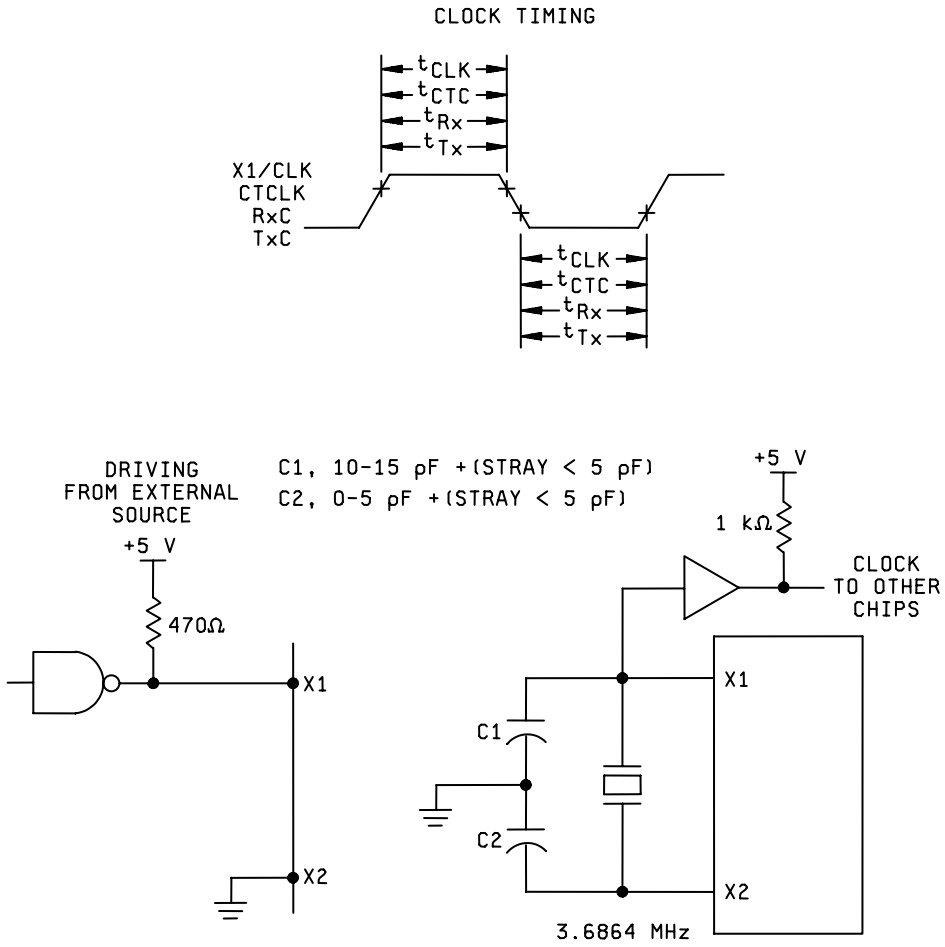


FIGURE 4. Timing waveforms and test circuits - Continued.

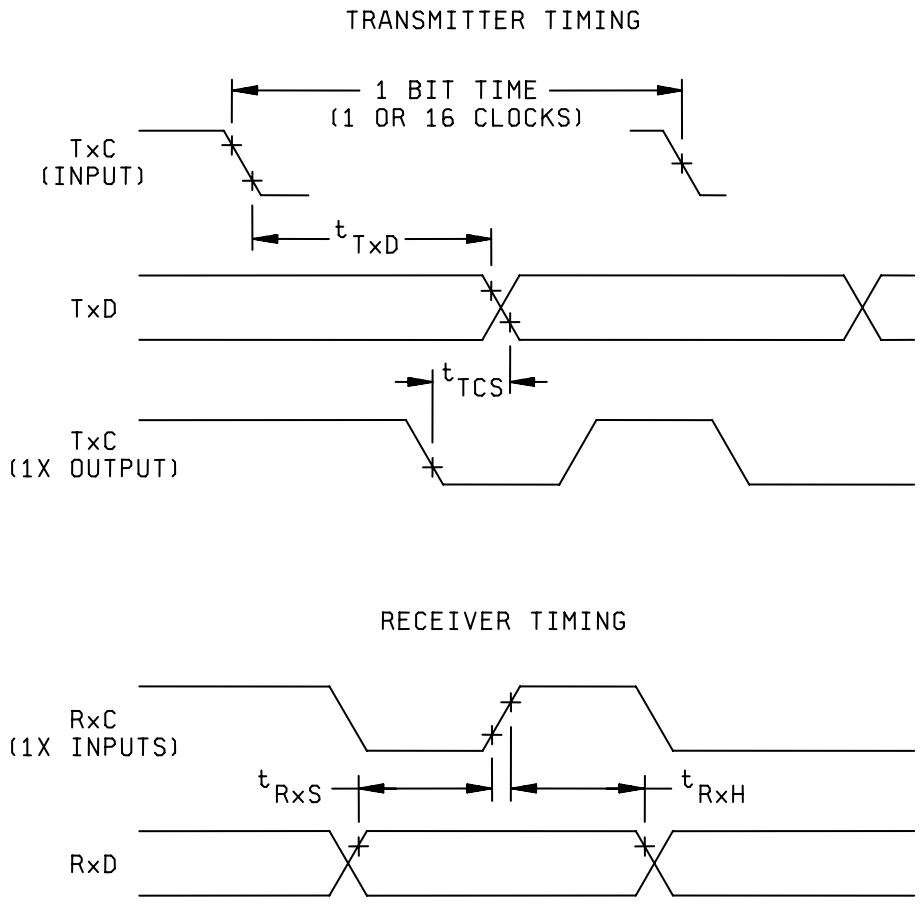
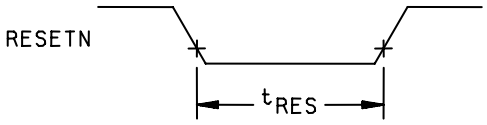


FIGURE 4. Timing waveforms and test circuits - Continued.

Device type 03

RESET TIMING



BUS TIMING (READ CYCLE)

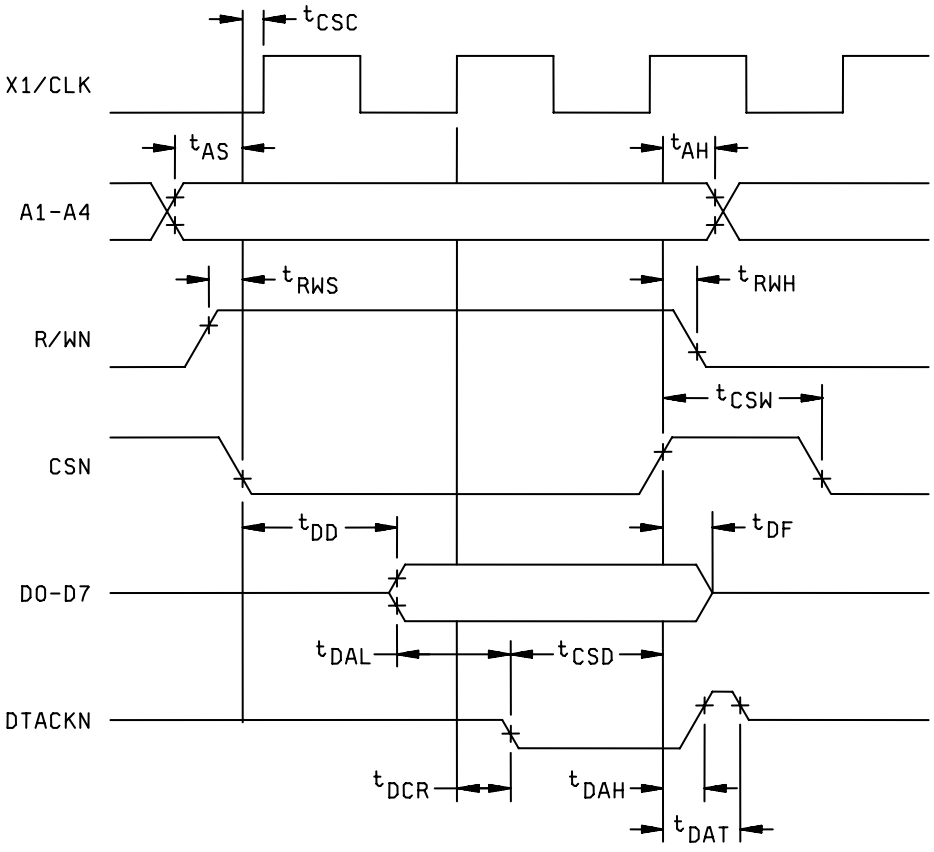


FIGURE 4. Timing waveforms and test circuits - Continued.

Device type 03

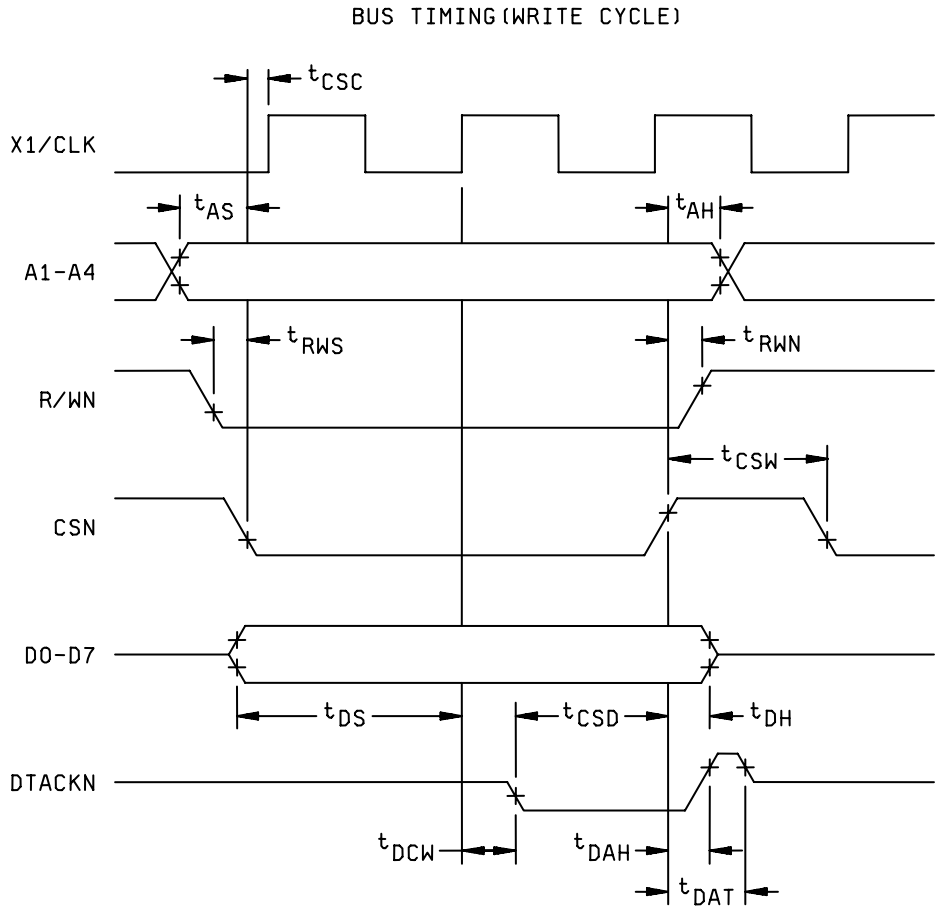


FIGURE 4. Timing waveforms and test circuits - Continued.

Device type 03

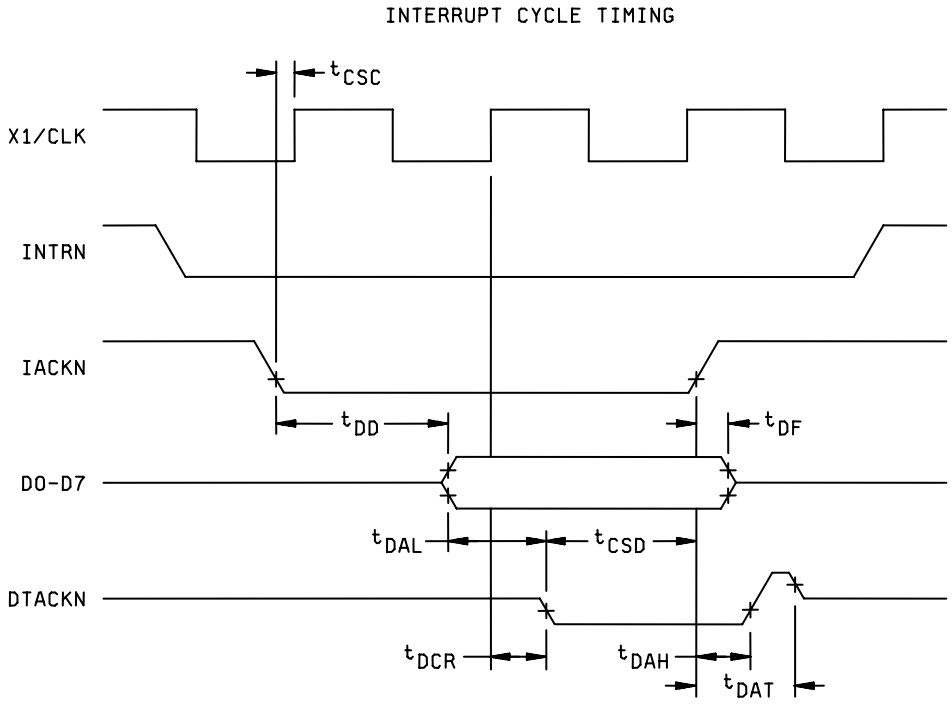
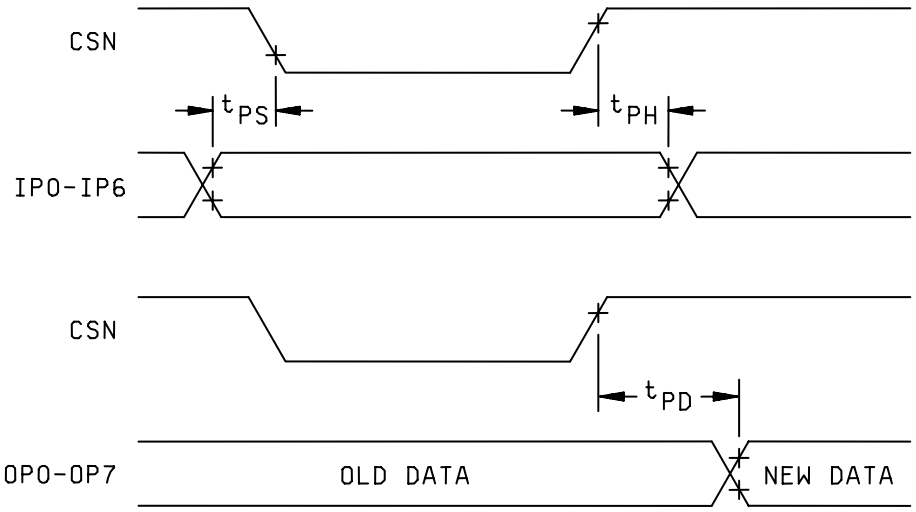
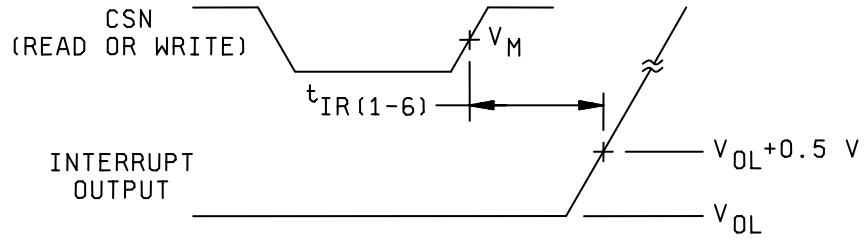


FIGURE 4. Timing waveforms and test circuits - Continued.

PORT TIMING



INTERRUPT TIMING



NOTES:
1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of the response is referenced from the midpoint of the switching signal, V_M, to a point 0.5 V above V_{OL}. This point represents the noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

FIGURE 4. Timing waveforms and test circuits - Continued.

Device type 03

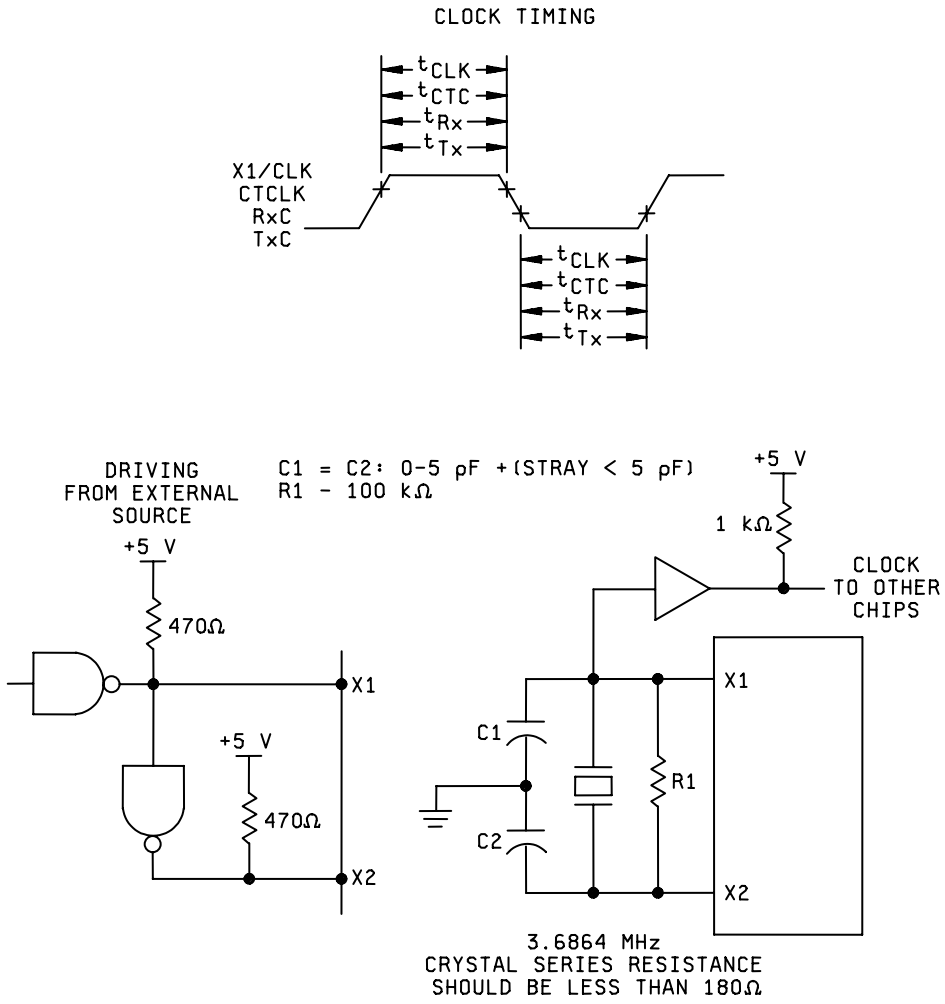


FIGURE 4. Timing waveforms and test circuits - Continued.

Device type 03

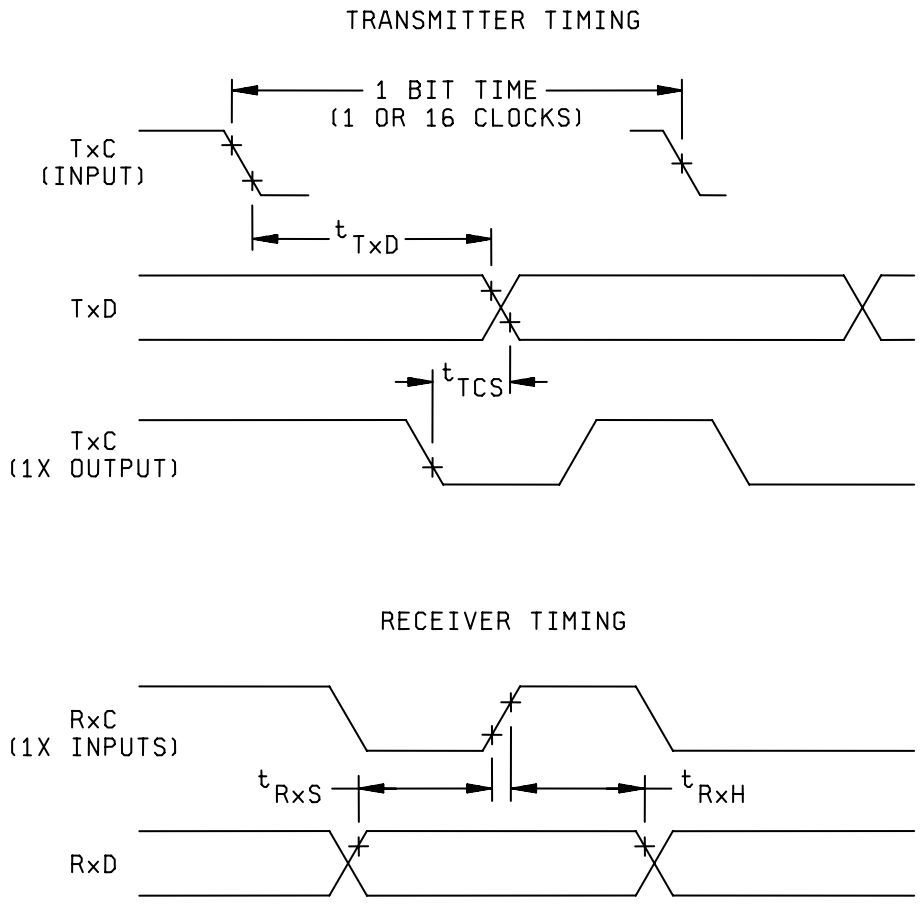


FIGURE 4. Timing waveforms and test circuits - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall include verification of the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Pin descriptions. The pin descriptions for the device types herein are as defined in table III as follows:

TABLE III. Pin descriptions.

For device types 01 and 02.

Mnemonic	Package Number of pins: 28	40	44	52	Device: 01	02	02	02	Type	Name and function
D0 - D7	X	X	X	X					I/O	Data Bus: Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	X					I	Chip Enable: Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0 – D7 as controlled by the WRN, RDN, and A0 – A3 inputs. When high, places the D0 – D7 lines in three-state condition.
WRN	X	X	X	X					I	Write Strobe: When low and CEN is also low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	X					I	Read Strobe: When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0 – A3	X	X	X	X					I	Address Inputs: Selects the DUART internal registers and ports for read/write operations.
RESET	X	X	X	X					I	Reset: A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0 – OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	X	X	X	X					O	Interrupt Request: Active low, open drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	X					I	Crystal 1: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 4 herein).
X2	X	X	X	X						Crystal 2: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 4 herein).
RxDA	X	X	X	X					I	Channel A Receiver Serial Data Input: The least significant bit is received first. "Mark" is high, "space" is low.
RxDB	X	X	X	X					I	Channel B Receiver Serial Data Input: The least significant bit is received first. "Mark" is high, "space" is low.

TABLE III. Pin descriptions - Continued.

For device types 01 and 02.

Mnemonic	Package Number of pins: 28	40	44	52	Device: 01	02	02	02	Type	Name and function
TxDA	X	X	X	X					O	Channel A Transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
TxDB	X	X	X	X					O	Channel B Transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
OPO	X	X	X	X					O	Output 0: General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated automatically on receive or transmit.
OP1	X	X	X	X					O	Output 1: General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated automatically on receive or transmit.
OP2		X	X	X					O	Output 2: General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3		X	X	X					O	Output 3: General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4		X	X	X					O	Output 4: General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5		X	X	X					O	Output 5: General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6		X	X	X					O	Output 6: General purpose output, or channel A open drain, active low, TxRDYA output.
OP7		X	X	X					O	Output 7: General purpose output, or channel B open drain, active low, TxRDYB output.
IP0		X	X	X					I	Input 0: General purpose input, or channel A clear to send active low input (CTSAN).
IP1		X	X	X					I	Input 1: General purpose input, or channel B clear to send active low input (CTSBN).
IP2	X	X	X	X					I	Input 2: General purpose input, or counter/timer external clock input.

TABLE III. Pin descriptions - Continued.

For device types 01 and 02.

Mnemonic	Package Number of pins: 28	40	44	52	Device: 01	02	02	02	Type	Name and function
IP3		X	X	X	I	Input 3: General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4		X	X	X	I	Input 4: General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5		X	X	X	I	Input 5: General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6		X	X	X	I	Input 6: General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	X	X	I	Power Supply: +5 V supply input.
GND	X	X	X	X	I	Ground: Ground.

TABLE III. Pin descriptions - Continued.

For device type 03.

Mnemonic	Pin number 1/	Type	Name and function
D0 – D7	25, 16, 24, 17, 23, 18, 22, 19	I/O	Data Bus: Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	Chip Select: Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0 – D7 as controlled by the R/WN and A1 – A4 inputs. When high, places the D0 – D7 lines in the three-state condition.
R/WN	8	I	Read/Write: A high input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1 – A4	1, 3, 5, 6	I	Address Inputs: Selects the DUART internal registers and ports for read/write operations.
RESETN	34	I	Reset: A low clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0 – OP7 in the high state, stops the counter/timer, and puts channel A and B in the inactive state, with the TxDA and TxDB outputs in the “mark” (high) state.
DTACKN	9	O	Data Transfer Acknowledge: Three-state active low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	Interrupt Request: Active low, open drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	Interrupt Acknowledge: Active low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	Crystal 1: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. If a crystal is used, a capacitor must be connected from this pin to ground (see figure 4 herein).
X2	33	I	Crystal 2: Connection for other side of the crystal. If a crystal is used, a capacitor must be connected from this pin to ground (see figure 4 herein). If an external clock is used, this pin should be grounded.
RxDA	31	I	Channel A Receiver Serial Data Input: The least significant bit is received first. “Mark” is high, “space” is low.
RxDB	10	I	Channel B Receiver Serial Data Input: The least significant bit is received first. “Mark” is high, “space” is low.

TABLE III. Pin descriptions - Continued.

For device type 03.

Mnemonic	Pin number 1/	Type	Name and function
TxDA	30	O	Channel A Transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
TxDB	11	O	Channel B Transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
OPO	29	O	Output 0: General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated automatically on receive or transmit.
OP1	12	O	Output 1: General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated automatically on receive or transmit.
OP2	28	O	Output 2: General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	13	O	Output 3: General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	27	O	Output 4: General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5	14	O	Output 5: General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6	26	O	Output 6: General purpose output, or channel A open drain, active low, TxRDYA output.
OP7	15	O	Output 7: General purpose output, or channel B open drain, active low, TxRDYB output.
IP0	7	I	Input 0: General purpose input, or channel A clear to send active low input (CTSAN).
IP1	4	I	Input 1: General purpose input, or channel B clear to send active low input (CTSBN).
IP2	36	I	Input 2: General purpose input, or channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.

TABLE III. Pin descriptions - Continued.

For device type 03.

Mnemonic	Pin number 1/	Type	Name and function
IP3	2	I	Input 3: General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	39	I	Input 4: General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	38	I	Input 5: General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	40	I	Power Supply: +5 V supply input.
GND	20	I	Ground: Ground.

1/ All pin numbers are for dual-in-line package except 52 pin flat package.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-02-08

Approved sources of supply for SMD 5962-89532 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8953201XA	0C7V7	2692/BXA
	3/	XR88C681YA883C
5962-8953202QA	0C7V7	2692/BQA
	3/	XR88C681QA883C
5962-8953202UA	0C7V7	2692/BUA
	3/	XR88C681XC883C
5962-8953202YA	0C7V7	2692/BYA
5962-8953203QA	3/	XR68C681QA883C
5962-8953203UA	3/	XR68C681X883C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.