Medium Power Differential Line Driver

The EL1507 is a very low power dual operational amplifier designed for central office and customer premise line driving for DMT ADSL solutions. This device features a high drive capability of 400mA while consuming only 7.5mA of supply current per amplifier from ±12V supplies. This driver achieves a typical distortion of less than -75dBc, at 1MHz into a 50Ω load. The EL1507 is available in the thermally-enhanced 16 Ld SO package, as well as a 16 Ld QFN package. Both are specified for operation over the full -40°C to +85°C temperature range.

The EL1507 has two control pins, C_0 and C_1. With the selection of C_0 and C_1, the device can be set into full-I_S power, ¾-I_S power, ½-I_S power, and power down disable modes. The EL1507 maintains excellent distortion and load driving capabilities even in the lowest power settings.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL1507CS	EL1507CS	-	16 Ld SOIC	MDP0027
EL1507CS-T7	EL1507CS	7”	16 Ld SOIC	MDP0027
EL1507CS-T13	EL1507CS	13”	16 Ld SOIC	MDP0027
EL1507CSZ (See Note)	EL1507CSZ	-	16 Ld SOIC (Pb-Free)	MDP0027
EL1507CSZ-T7 (See Note)	EL1507CSZ	7”	16 Ld SOIC (Pb-Free)	MDP0027
EL1507CSZ-T13 (See Note)	EL1507CSZ	13”	16 Ld SOIC (Pb-Free)	MDP0027
EL1507CL	1507CL	-	16 Ld QFN	MDP0046
EL1507CL-T7	1507CL	7”	16 Ld QFN	MDP0046
EL1507CL-T13	1507CL	13”	16 Ld QFN	MDP0046
EL1507CLZ (See Note)	1507CLZ	-	16 Ld QFN (Pb-Free)	MDP0046
EL1507CLZ-T7 (See Note)	1507CLZ	7”	16 Ld QFN (Pb-Free)	MDP0046
EL1507CL-T13 (See Note)	1507CLZ	13”	16 Ld QFN (Pb-Free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

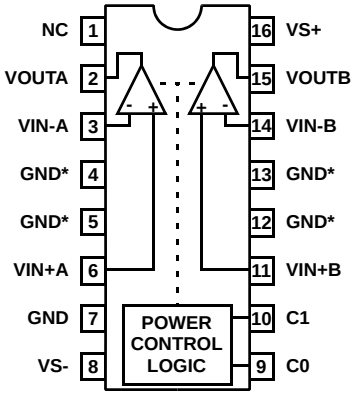
- Drives 360mA at 16V_{P-P} on ±12V supplies
- 40V_{P-P} differential output drive into 100Ω
- -75dBc typical driver output distortion driving 50Ω at 1MHz and 1/2-I_S bias current
- Low quiescent current of 3.5mA per amplifier in 1/2-I_S mode
- Power down disable mode
- Pb-free plus anneal available (RoHS compliant)

Applications

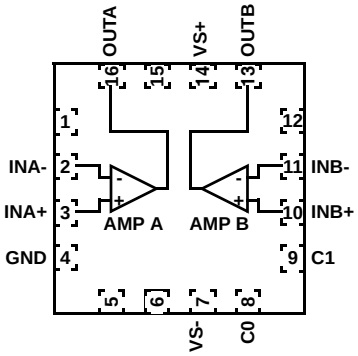
- ADSL G.DMT and G.lite CO line driving
- G.SHDSL, HDSL2 line driver
- ADSL CPE line driving
- Video distribution amplifier
- Video twisted-pair line driver

Pinouts

EL1507
(16 LD SO)
TOP VIEW



EL1507
(16 LD QFN)
TOP VIEW



NOTE: *These GND Pins are heat spreaders

Absolute Maximum Ratings (T_A = +25°C)

V_S+ to V_S- Supply Voltage. 26.4V
V_S+ Voltage to Ground . . . . . -0.3V to +26.4V
V_S- Voltage to Ground . . . . . -26.4V to 0.3V
Input C_0/C_1 to Ground 7V
V_{IN}+ Voltage . . . . . V_S- to V_S+
Current Into Any Input 8mA
Continuous Output Current 75mA
Operating Temperature Range . . . . . .-40°C to +85°C
Storage Temperature Range . . . . . .-60°C to +150°C
Operating Junction Temperature . . . . . .-40°C to +150°C
Power Dissipation . . . . . .See Power Supplies & Dissipation section

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = ±12V, R_F= 1.5kΩ, R_L= 75Ω to GND, T_A = +25°C. unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +4		70		MHz
HD	Total Harmonic Distortion	f = 1MHz, V_O = 16V_{P-P}, R_L = 50Ω		-75		dBc
dG	Differential Gain	A_V = +2, R_L = 37.5Ω		0.17		%
dθ	Differential Phase	A_V = +2, R_L = 37.5Ω		0.1		°
SR	Slew Rate	V_{OUT} from -4.5V to +4.5V	350	500		V/µs
DC PERFORMANCE						
V_{OS}	Offset Voltage		-17		17	mV
ΔV_{OS}	V_{OS} Mismatch		-10		10	mV
R_{OL}	Transimpedance	V_{OUT} from -4.5V to +4.5V	1	2	3.5	MΩ
INPUT CHARACTERISTICS						
I_B+	Non-Inverting Input Bias Current		-5		5	µA
I_B-	Inverting Input Bias Current		-30		30	µA
ΔI_B-	I_B- Mismatch		-20		20	µA
e_N	Input Noise Voltage			2.8		nV/√Hz
i_N+	+Input Noise Current			1.8		pA/√Hz
i_N-	-Input Noise Current			19		pA/√Hz
V_{IH}	Input High Voltage	C_0 & C_1 inputs	2.3			V
V_{IL}	Input Low Voltage	C_0 & C_1 inputs			1.5	V
I_{IH1}	Input High Current for C_1	C_1 = 5V	0.2		8	µA
I_{IH0}	Input High Current for C_0	C_0 = 5V	0.1		4	µA
I_{IL}	Input Low Current for C_1 or C_0	C_1 = 0V, C_0 = 0V	-1		1	µA
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing Single Ended	R_L = 100Ω to GND	±10.3	±10.9		V
V_{OUT} P	Loaded Output Swing Single Ended	R_L = 25Ω to GND	9.5	10.2		V
V_{OUT} N	Loaded Output Swing Single Ended	R_L = 25Ω to GND	-8.2	-9.8		V
I_{OUT}	Output Current	R_L = 0Ω		500		mA
SUPPLY						
V_S	Supply Voltage	Single supply	5		24	V
I_S+ (Full Power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V		7.5	9	mA

Electrical Specifications V_S = ±12V, R_F= 1.5kΩ, R_L= 75Ω to GND, T_A = +25°C. unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{S^-} (Full Power)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V		-7	-8.5	mA
I_{S^+} (3/4 Power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 5V, C_1 = 0V		6	7.5	mA
I_{S^-} (3/4 Power)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = 5V, C_1 = 0V		-5.5	-7	mA
I_{S^+} (1/2 Power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 0V, C_1 = 5V		3.9	5.1	mA
I_{S^-} (1/2 Power)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = 0V, C_1 = 5V		-3.3	-4.6	mA
I_{S^+} (Power Down)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 5V		0.6	1	mA
I_{S^-} (Power Down)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 5V		0	0.75	mA
I_{GND}	GND Supply Current per Amplifier	All outputs at 0V		0.6	1	mA

Typical Performance Curves

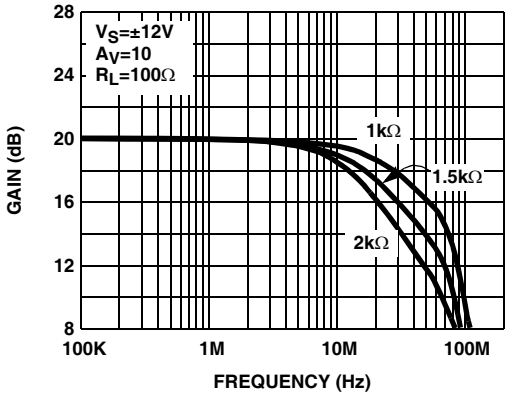


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CS - FULL POWER MODE)

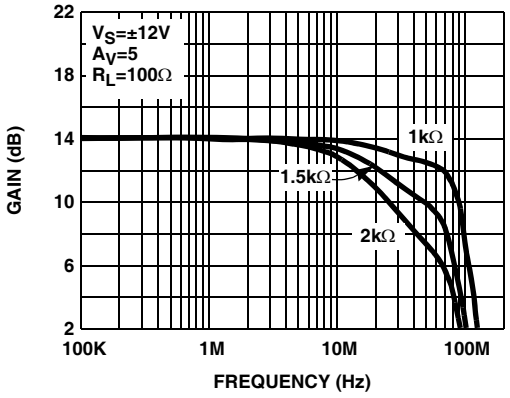


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CS - FULL POWER MODE)

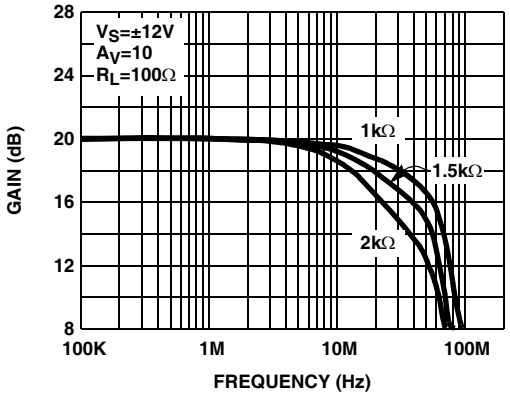


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CS - 3/4 POWER MODE)

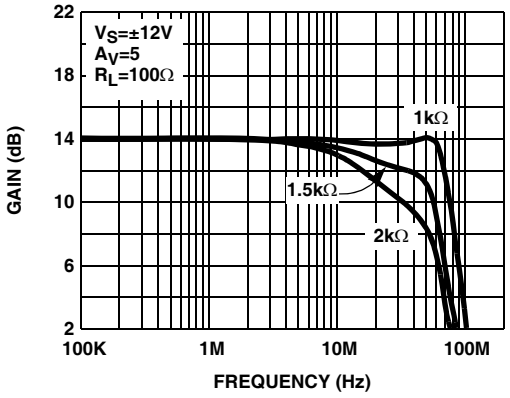


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CS - 3/4 POWER MODE)

Typical Performance Curves

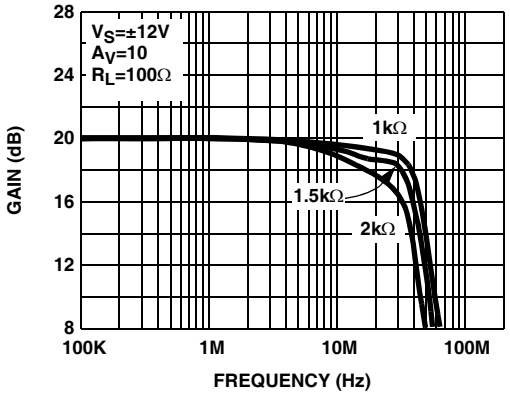


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CS - 1/2 POWER MODE)

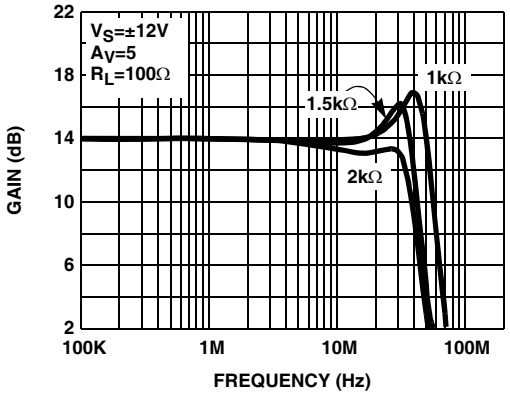


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CS - 1/2 POWER MODE)

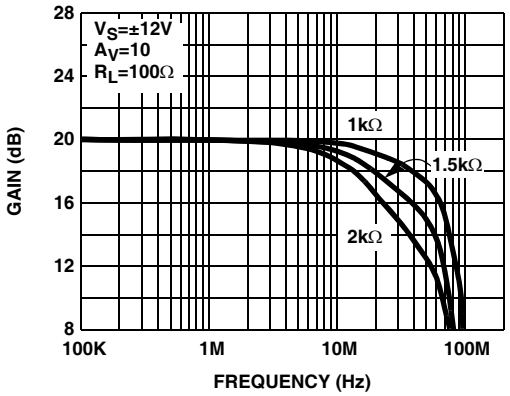


FIGURE 7. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CL - FULL POWER MODE)

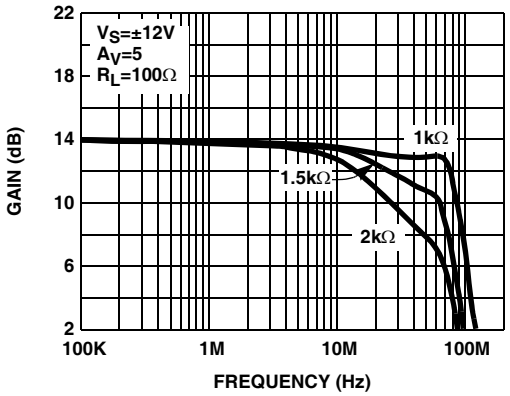


FIGURE 8. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CL - FULL POWER MODE)

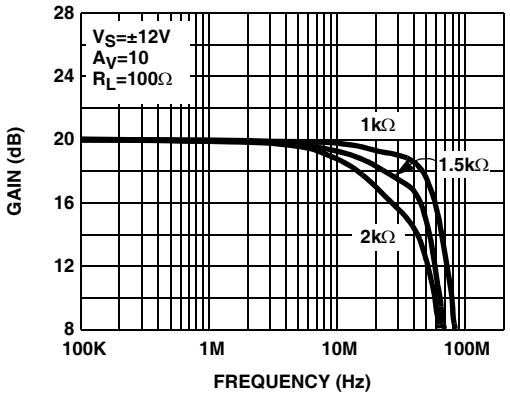


FIGURE 9. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CL - 3/4 POWER MODE)

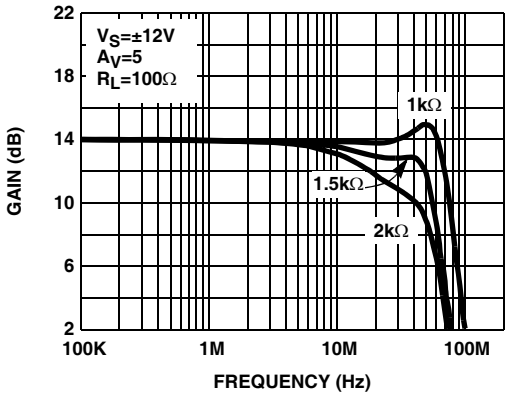


FIGURE 10. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CL - 3/4 POWER MODE)

Typical Performance Curves

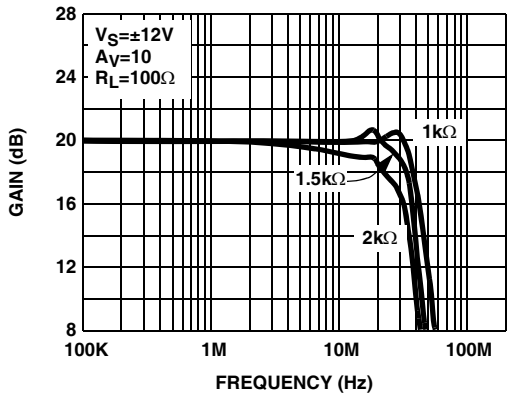


FIGURE 11. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CL - 1/2 POWER MODE)

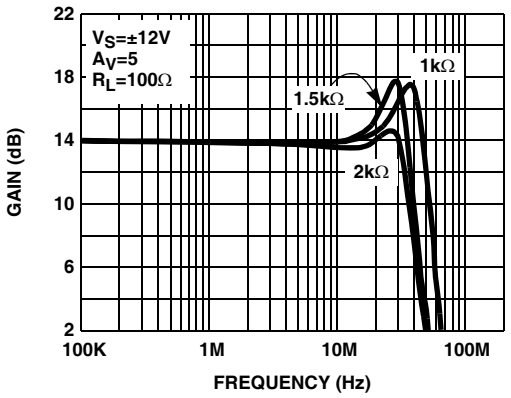


FIGURE 12. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (EL1507CL - 1/2 POWER MODE)

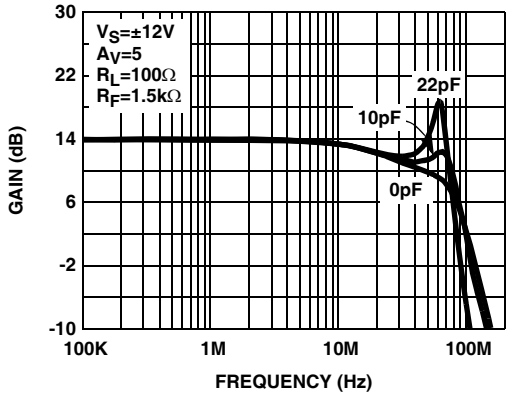


FIGURE 13. FREQUENCY RESPONSE vs C_{LOAD} (EL1507CS - FULL POWER MODE)

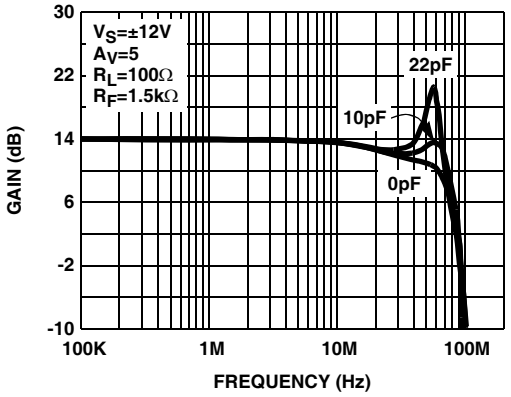


FIGURE 14. FREQUENCY RESPONSE vs C_{LOAD} (EL1507CL - FULL POWER MODE)

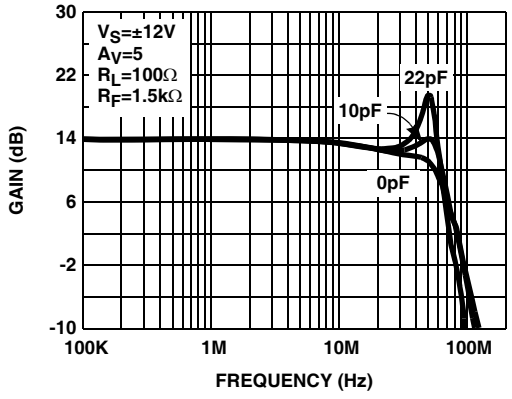


FIGURE 15. FREQUENCY RESPONSE vs C_{LOAD} (EL1507CS - 3/4 POWER MODE)

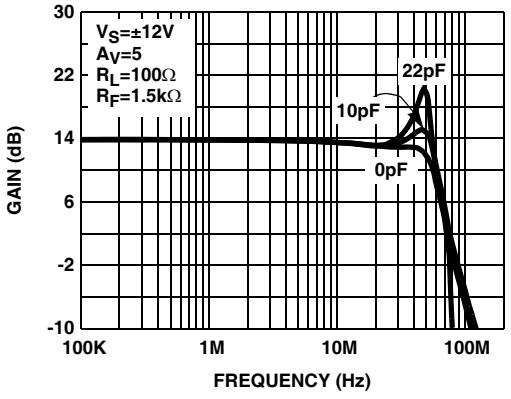


FIGURE 16. FREQUENCY RESPONSE vs C_{LOAD} (EL1507CL - 3/4 POWER MODE)

Typical Performance Curves

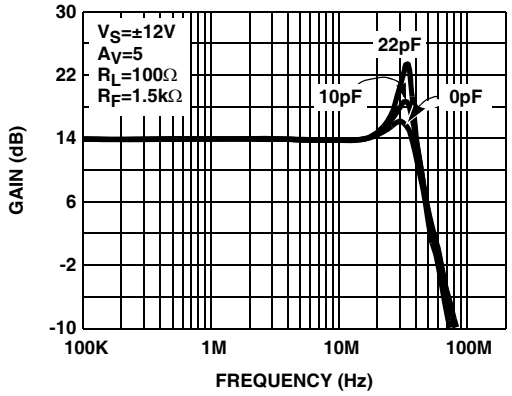


FIGURE 17. FREQUENCY RESPONSE vs C_{LOAD} (EL1507CS - 1/2 POWER MODE)

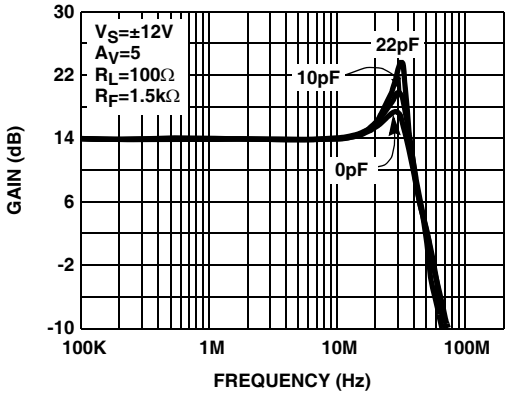


FIGURE 18. FREQUENCY RESPONSE vs C_{LOAD} (EL1507CL - 1/2 POWER MODE)

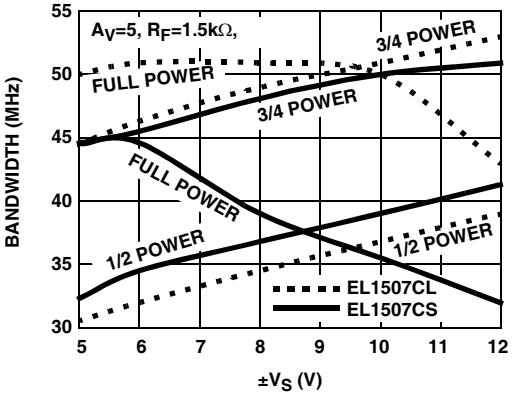


FIGURE 19. DIFFERENTIAL BANDWIDTH vs SUPPLY VOLTAGE

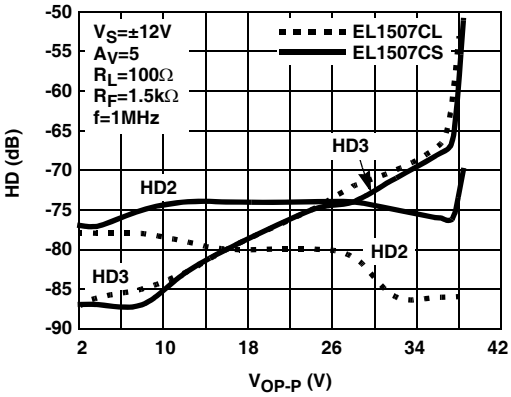


FIGURE 20. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (FULL POWER MODE)

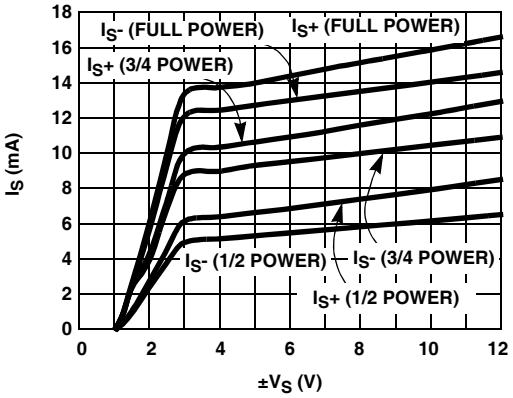


FIGURE 21. SUPPLY CURRENT vs SUPPLY VOLTAGE

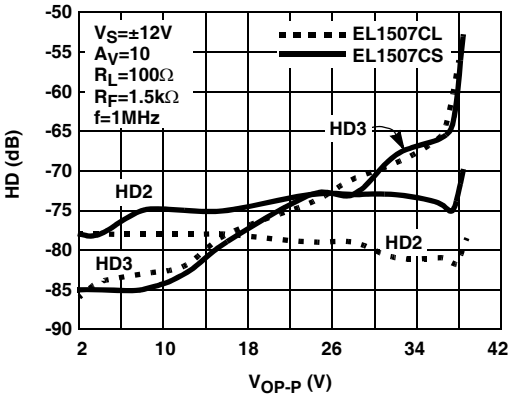


FIGURE 22. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (3/4 POWER MODE)

Typical Performance Curves

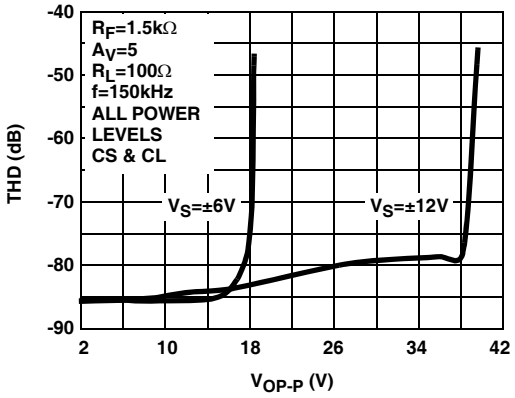


FIGURE 23. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE

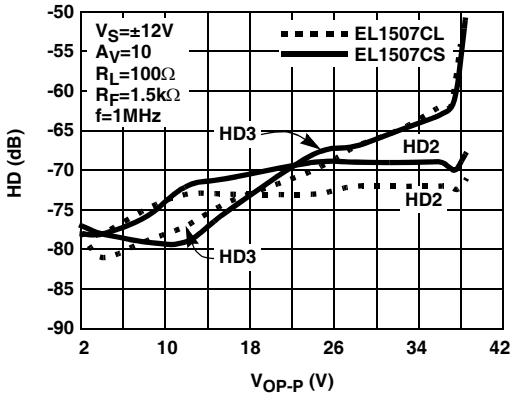


FIGURE 24. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (1/2 POWER MODE)

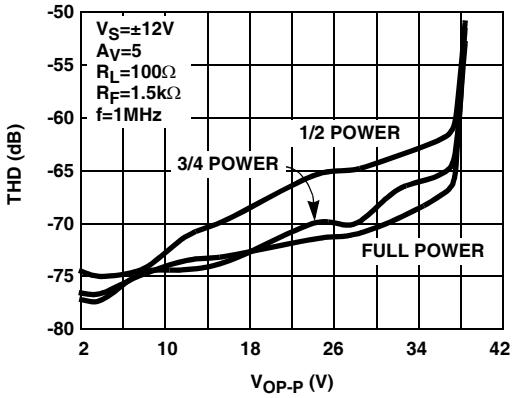


FIGURE 25. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (EL1507CS)

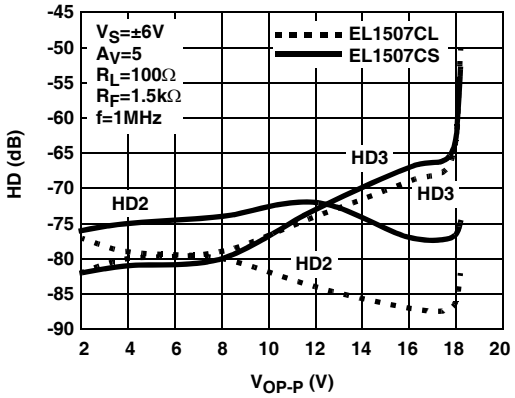


FIGURE 26. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (3/4 POWER MODE)

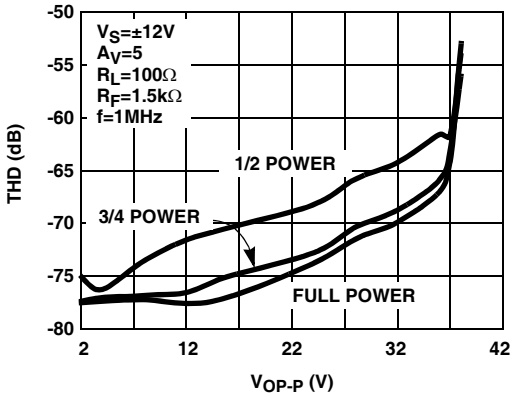


FIGURE 27. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (EL1507CL)

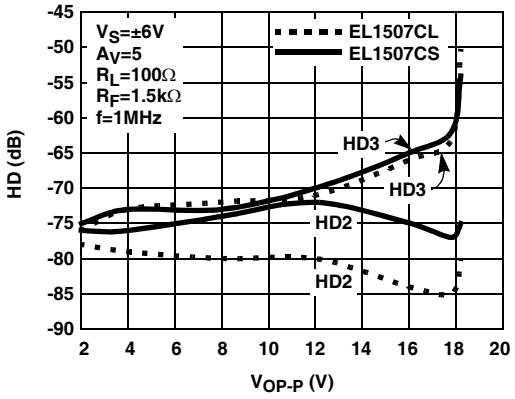


FIGURE 28. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (1/2 POWER MODE)

Typical Performance Curves

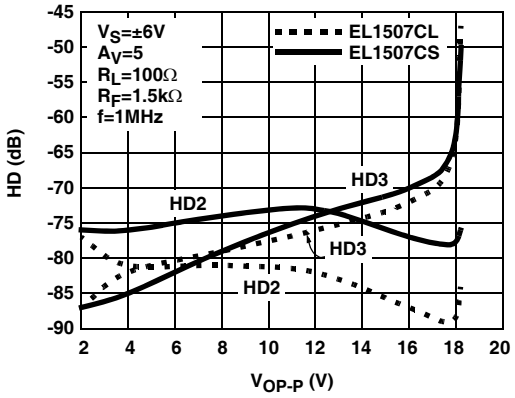


FIGURE 29. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (FULL POWER MODE)

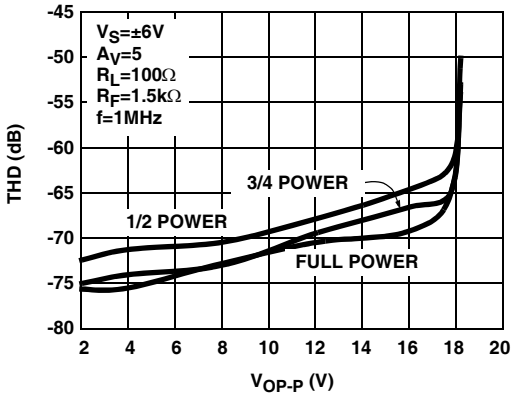


FIGURE 30. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (EL1507CS)

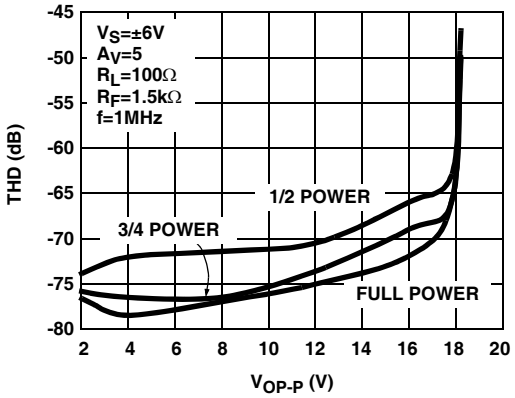


FIGURE 31. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (EL1507CL)

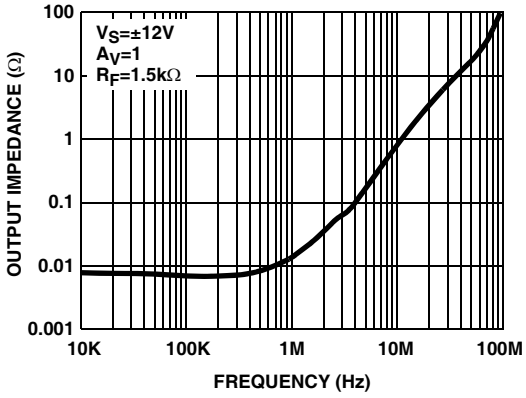


FIGURE 32. OUTPUT IMPEDANCE vs FREQUENCY (ALL POWER LEVELS)

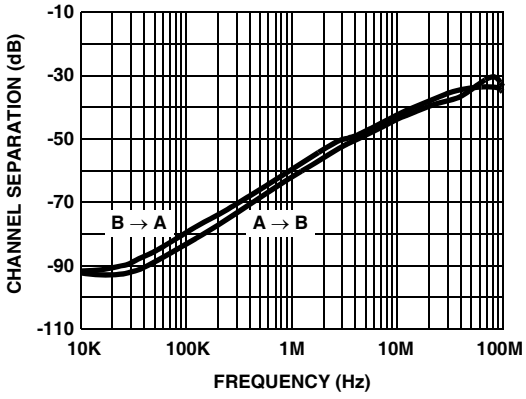


FIGURE 33. CHANNEL SEPARATION vs FREQUENCY (ALL POWER LEVELS)

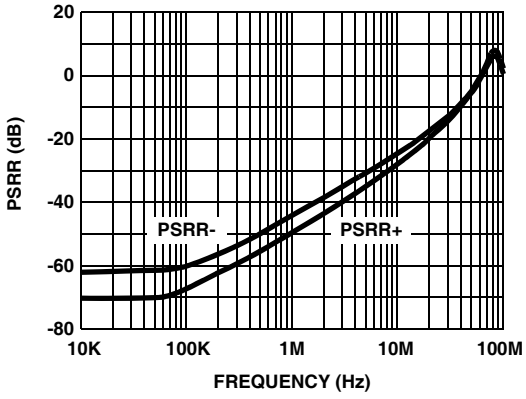


FIGURE 34. PSRR vs FREQUENCY

Typical Performance Curves

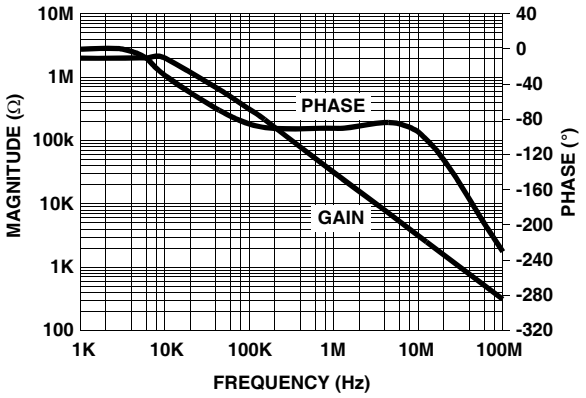


FIGURE 35. TRANSIMPEDANCE (R_{OL}) vs FREQUENCY

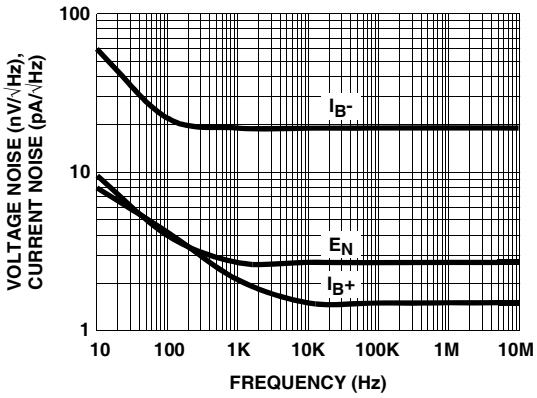


FIGURE 36. VOLTAGE AND CURRENT NOISE vs FREQUENCY

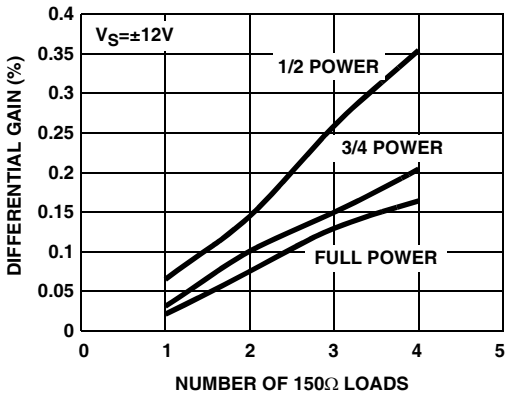


FIGURE 37. DIFFERENTIAL GAIN

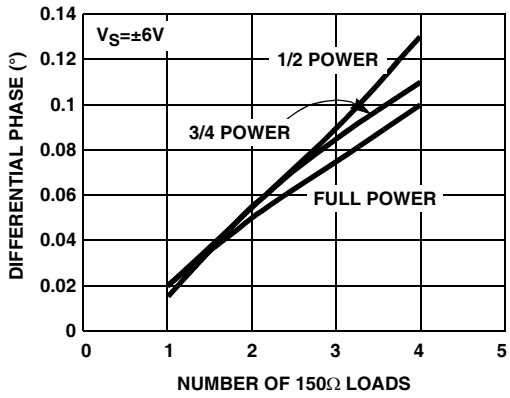


FIGURE 38. DIFFERENTIAL PHASE

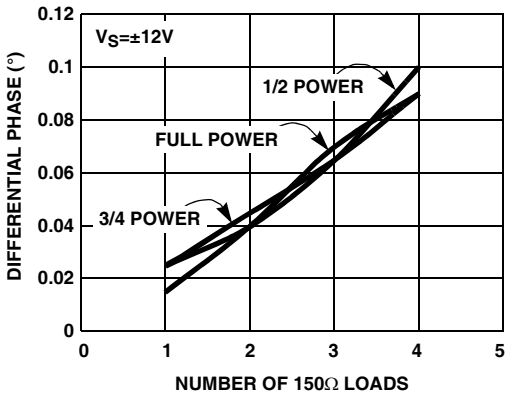


FIGURE 39. DIFFERENTIAL PHASE

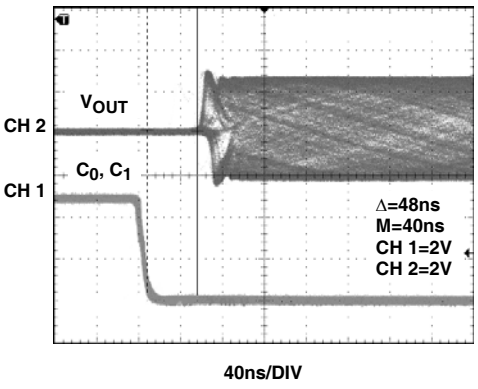


FIGURE 40. ENABLE RESPONSE

Typical Performance Curves

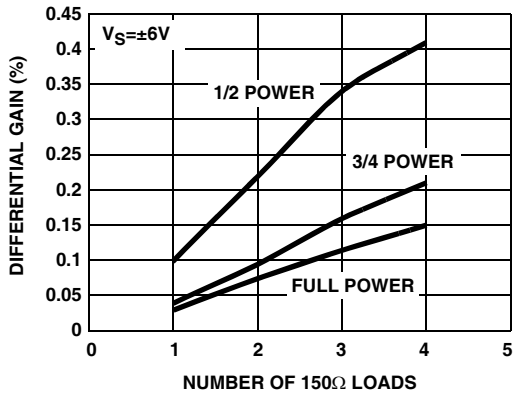


FIGURE 41. DIFFERENTIAL GAIN

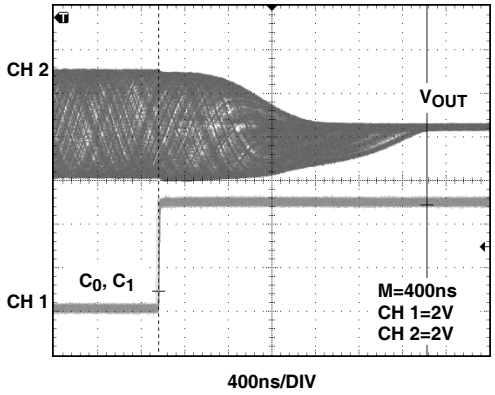


FIGURE 42. DISABLE RESPONSE

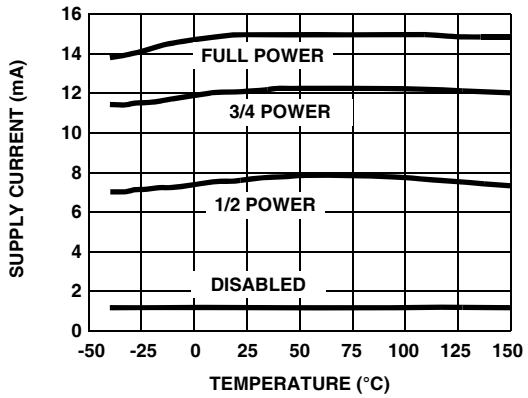


FIGURE 43. POSITIVE SUPPLY CURRENT vs TEMPERATURE

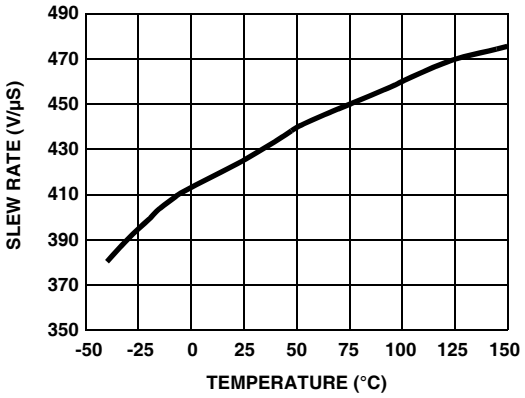


FIGURE 44. SLEW RATE vs TEMPERATURE

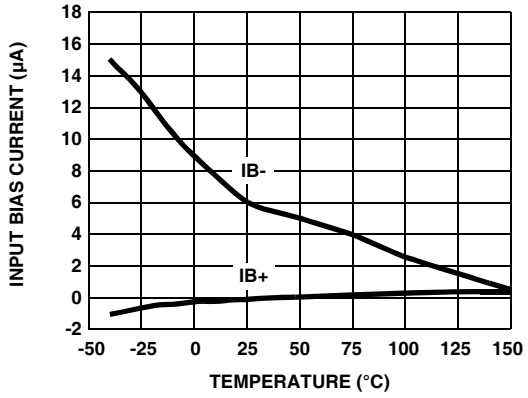


FIGURE 45. INPUT BIAS CURRENT vs TEMPERATURE

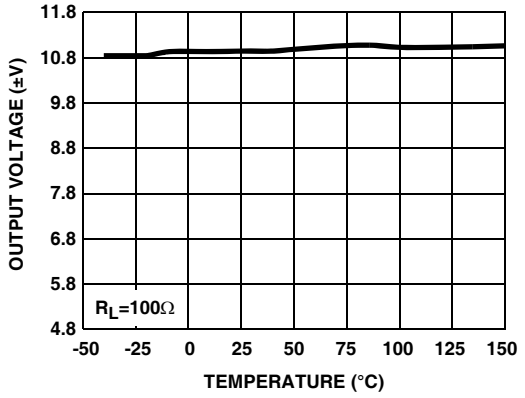


FIGURE 46. OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves

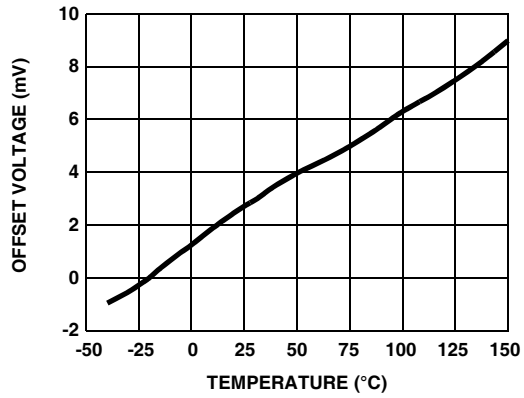


FIGURE 47. OFFSET VOLTAGE vs TEMPERATURE

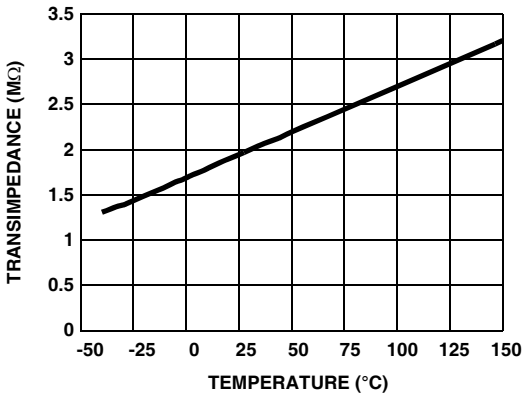


FIGURE 48. TRANSIMPEDANCE vs TEMPERATURE

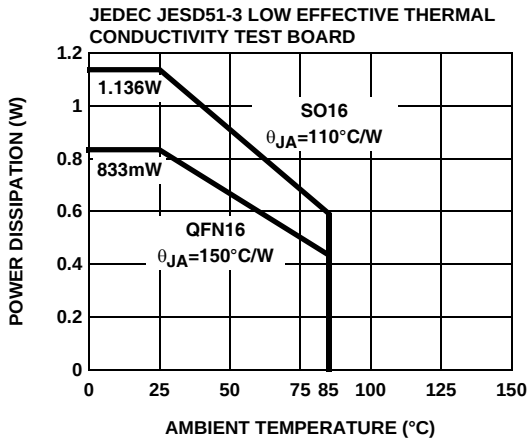


FIGURE 49. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

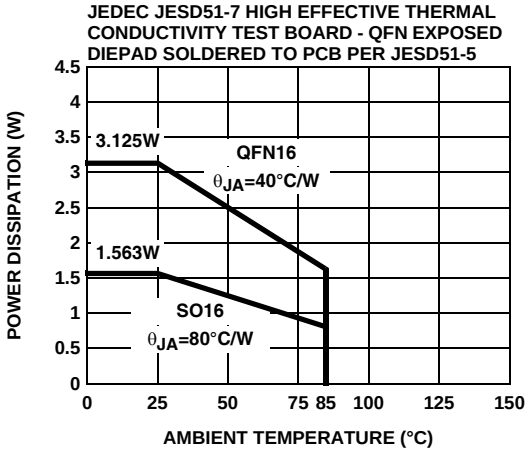


FIGURE 50. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

The EL1507 consists of two high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 4MHz and produce low distortion levels. A typical interface circuit is shown in Figure 51 below.

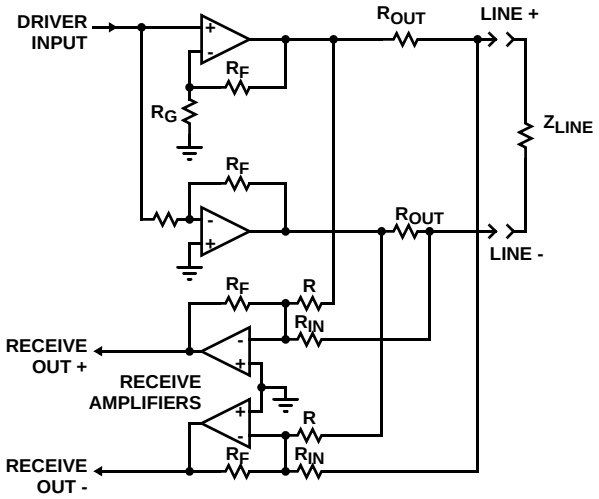


FIGURE 51. TYPICAL LINE INTERFACE CONNECTION

The amplifiers are wired with one in positive gain and the other in a negative gain configuration to generate a differential output for a single-ended input. They will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver.

If a differential signal is available to the drive amplifiers, they may be wired so:

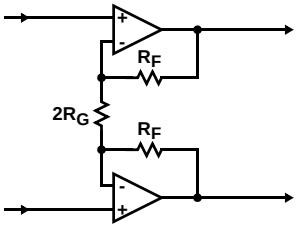


FIGURE 52. DRIVERS WIRED FOR DIFFERENTIAL INPUT

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The EL1507 amplifiers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4” of unshielded wiring, or 6” of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Power Supplies & Dissipation

Due to the high power drive capability of the EL1507, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the EL1507 has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the EL1507 is not constant with varying outputs. In reality, 7mA of the 15mA needed to power the drivers is converted in to output current. Therefore, in the equation below we should subtract the average output current, I_O, or 7mA, whichever is the lowest. We’ll call this term I_X.

Therefore, we can determine a quiescent current with the equation:

$$P_{Dquiescent} = V_S \times (I_S - 2I_X)$$

where:

V_S is the supply voltage (V_S+ to V_S-)

I_S is the maximum quiescent supply current (I_S+ + I_S-)

I_X is the lesser of I_O or 7mA (generally I_X = 7mA)

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage required from the EL1507 is close to the maximum available output swing. There is a trade off, however, with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with the following equation:

$$P_{Dtransistors} = 2 \times \overline{I_O} \times \left(\frac{V_S}{2} - \overline{V_O}\right)$$

where:

V_S is the supply voltage (V_S+ to V_S-)

V_O is the average output voltage per channel

I_O is the average output current per channel

The overall power dissipation (P_{DISS}) is obtained by adding $P_{Dquiescent}$ and $P_{Dtransistor}$.

Then, the θ_{JA} requirement needs to be calculated. This is done using the equation:

$$\theta_{JA} = \frac{(T_{JUNCT} - T_{AMB})}{P_{DISS}}$$

where:

T_{JUNCT} is the maximum die temperature (150°C)

T_{AMB} is the maximum ambient temperature

P_{DISS} is the dissipation calculated above

θ_{JA} is the junction to ambient thermal resistance for the package when mounted on the PCB

This θ_{JA} value is then used to calculate the area of copper needed on the board to dissipate the power.

The SO power packages are designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the center leads are internally connected to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique. A separate application note details the 16 Ld QFN PCB design considerations.

Single Supply Operation

The EL1507 can also be powered from a single supply voltage. When operating in this mode, the GND pins can still be connected directly to GND. To calculate power dissipation, the equations in the previous section should be used, with V_S equal to half the supply rail.

Output Loading

While the drive amplifiers can output in excess of 400mA transiently, the internal metallization is not designed to carry more than 75mA of steady DC current and there is no current-limit mechanism. This allows safely driving rms sinusoidal currents of 2 x 75mA, or 150mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Power Supplies

The power supplies should be well bypassed close to the EL1507. A 3.3µF tantalum capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1507 demonstration board, and documentation can be obtained from the factory.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (<1dB peaking) for different supply voltages and gains:

TABLE 1. OPTIMUM DRIVER FEEDBACK RESISTOR FOR VARIOUS GAINS AND SUPPLY VOLTAGES

Supply Voltage	Driver Voltage Gain		
	2.5	5	10
±5V	2k	1.8k	1.5k
±12V	2k	1.8k	1.5k

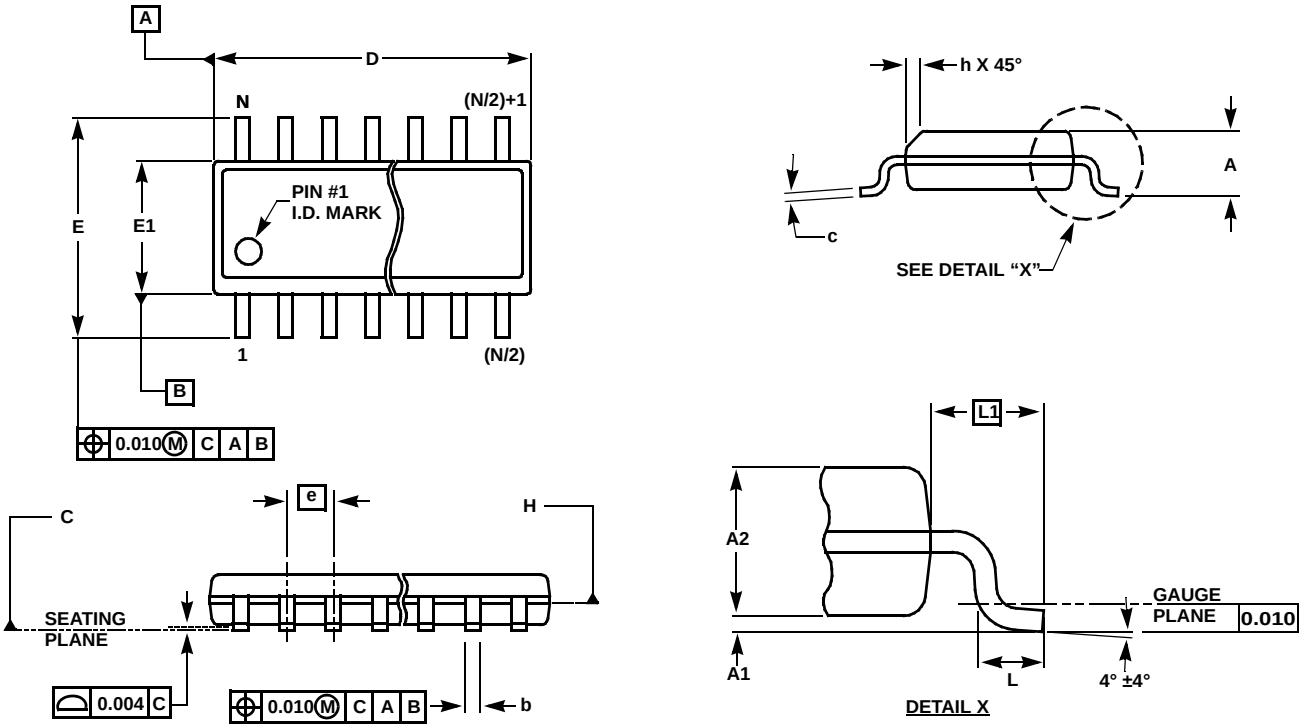
Power Control Function

The EL1507 contains two forms of power control operation. Two digital inputs, C_0 and C_1, can be used to control the supply current of the EL1507 drive amplifiers. As the supply current is reduced, the EL1507 will start to exhibit slightly higher levels of distortion and the frequency response will be limited. The 4 power modes of the EL1507 are set up as shown in the table below:

TABLE 2. POWER MODES OF THE EL1507

C_1	C_0	Operation
0	0	I_S Full Power Mode
0	1	¾-I_S Power Mode
1	0	½-I_S Power Mode
1	1	Power Down

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

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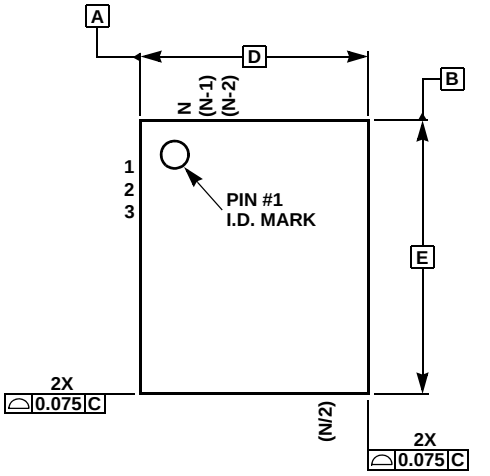
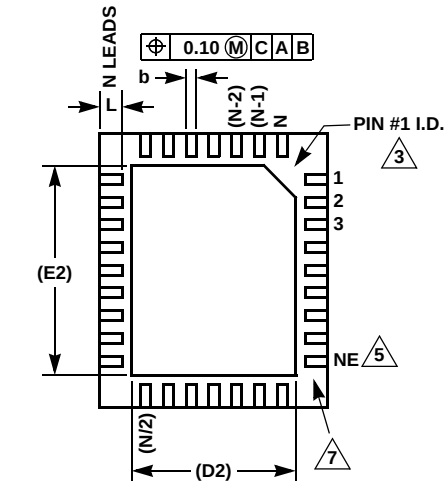
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

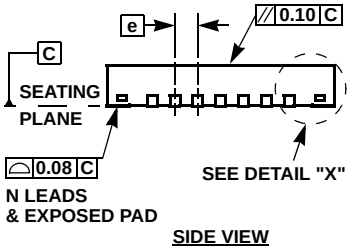
QFN (Quad Flat No-Lead) Package Family



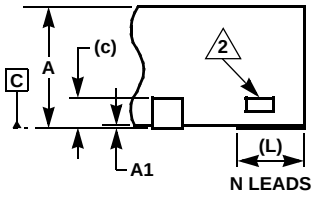
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN3	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	MILLIMETERS					TOLER-ANCE	NOTES
	QFN28	QFN2	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

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NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.