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RENESAS

User's Manual

μPD4991A

4-bit Parallel I/O Calendar Clock

Document No. S12923EJ2V0UM00 (2nd edition)
Date Published November 1997 N

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Caution

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

CHAPTER 1 OUTLINE OF μPD4991A

The μPD4991A is an IC for inputting/outputting 4-bit parallel time data and calendar data in a microcontroller system and has 1 channel for an alarm function.

This IC has seven types of internal counters: year, month, date, day of week, hour, minute, and second. The hour counter can be used in two modes: 12-hour and 24-hour modes. Month, date, day of week, minute, and second can be specified for the alarm function.

Because the operating voltage range of this IC is very wide, from 2.0 to 5.5 V (4.5 to 5.5 V when the IC is accessed), commercially available dry cells, mercury cells, lithium batteries, Ni-Cd batteries, and super capacitors (electric double-layer capacitors) can be used as back-up batteries.

The μPD4991A is suitable for systems requiring a watch function, such as personal computers, word processors, FAXes, ECRs, and POSs.

1.1 Features

- Time (hour, minute, and second) and calendar (leap year, year, month, date, and day of week) counters
- Alarm function (month, date, day of week, hour, minute, and second)
- Seven alarm coincidence signals and five interval timers
- Automatic identification and user-setting of leap year (up to 2099)
- 12- and 24-hour modes selectable
- High speed response (cycle time: 150 ns)
- Low current consumption (2 μA Typ. at back up)
- Address bus: 4 bits, data bus: 4 bits
- Upward-compatible with μPD4991 in function and characteristics (For details, refer to **Appendix 3**.)

Basic Specifications

- Reference frequency (crystal oscillation) ..... 32.768 kHz
- Data format ..... BCD
- Data function
  Year, month, date, day of week, hour, minute, and second counters
  Leap year is automatically identified or can be set by the user.
  Years are set in 2-digit units.
  Hours can be indicated in 12- or 24-hour mode.
- Data input/output (D_3, D_2, D_1, D_0)
  4-bit parallel input/output
  Data is input/output by enabling writing with the WE signal and enabling reading with the OE signal.
- Mode selection
  The mode is selected by setting the address to $0F_H$ and writing data.
- Timing pulse output (TP1, TP2)
  TP1 ... Alarm coincidence signal output
  2048, 1024, 64, 16, 1 Hz, or 1-pulse output (H → L) selectable
  TP2 ... Interval timer signal output
  60, 30, 10, 1, or 0.1 s selectable
- Chip select ($\overline{CS_1}$, CS_2)
  All input signals except X_{IN} are disabled when $\overline{CS_1}$ = "H" and CS_2 = "L".
  All input signals are selected when $\overline{CS_1}$ = "L" and CS_2 = "H".

1.2 Pin Configuration

The μPD4991A is available in two packages: 18-pin DIP and 20-pin SOP. Figure 1-1 shows the pin configuration. Ordering information is given below. Table 1-1 lists the function of each pin.

Ordering information

Part Number	Package
μPD4991ACX	18-pin plastic DIP (300 mil)
μPD4991AGS	20-pin plastic SOP (300 mil)

Figure 1-1. Pin Configuration (Top View)

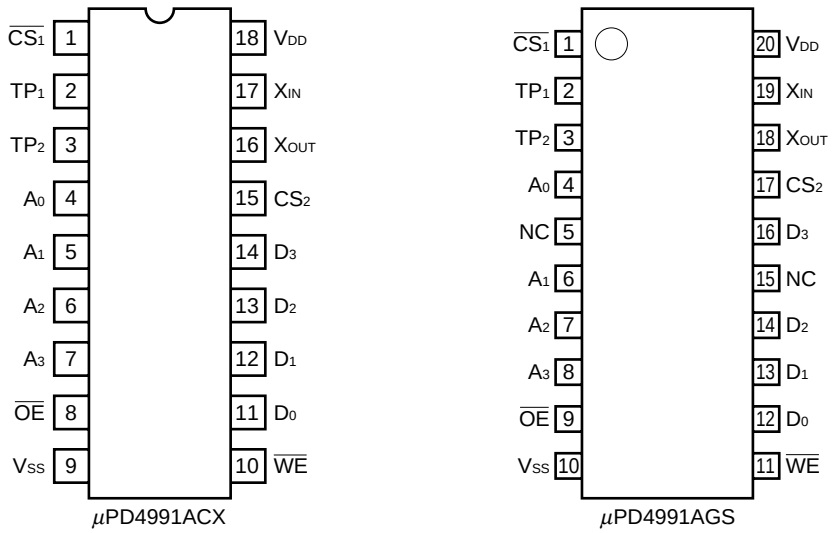


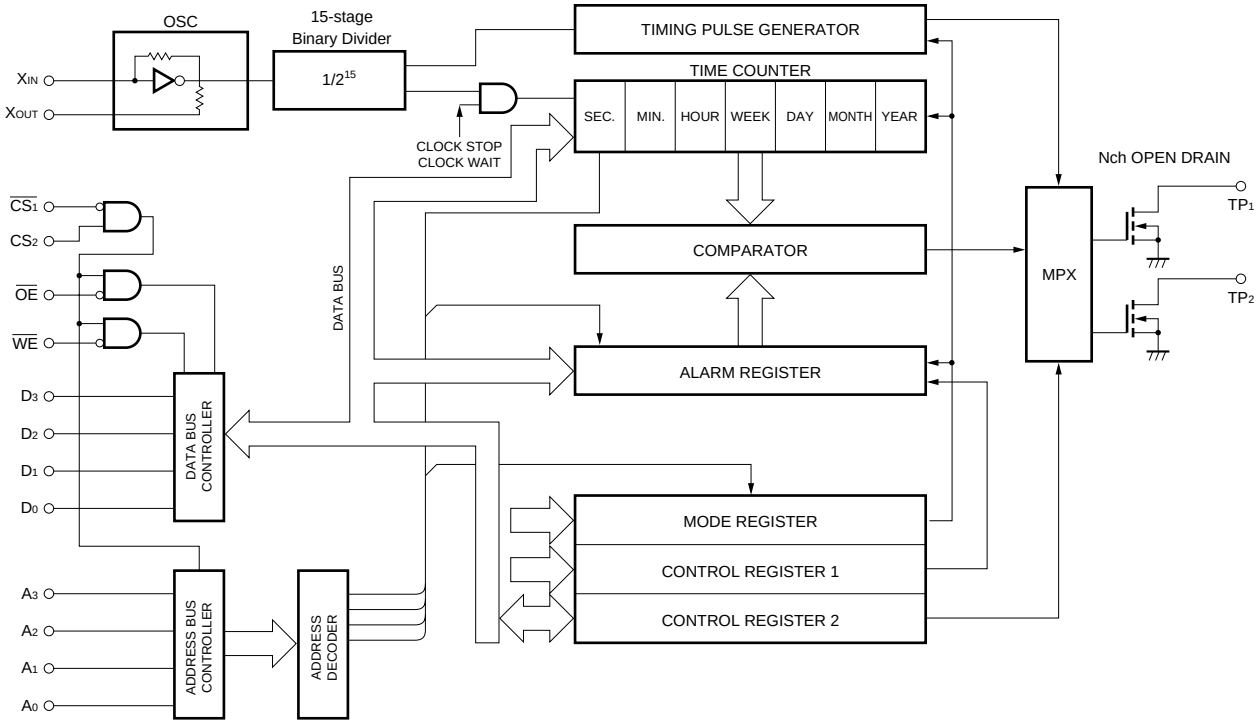
Table 1-1. Pin Functions

Pin Name	Symbol	Pin No.		Function
		DIP	SOP	
Chip select	$\overline{CS_1}$	1	1	When $\overline{CS_1}$ = "L" and CS_2 = "H", the μPD4991A can transfer data with a CPU.
	CS_2	15	17	
Timing pulse 1	TP1	2	2	Outputs an alarm coincidence signal.
Timing pulse 2	TP2	3	3	Outputs an interval timer signal
Address input	A_0	4	4	Specifies the internal address of the μPD4991A.
	A_1	5	6	
	A_2	6	7	
	A_3	7	8	
Read control input	$\overline{OE}$	8	9	While $\overline{OE}$ = "L", the contents specified by the address bus are read to the data bus.
Ground pin	V_{SS}	9	10	
Write control input	$\overline{WE}$	10	11	The contents of the data bus are written to an address specified by the address bus when $\overline{WE}$ rises.
Data bus pin	D_0	11	12	Bidirectional 4-bit bus which inputs/outputs watch data.
	D_1	12	13	
	D_2	13	14	
	D_3	14	16	
Crystal signal pin	X_{OUT}	16	18	Oscillation inverter output
Crystal signal pin	X_{IN}	17	19	Oscillation inverter input
Positive power supply	V_{DD}	18	20	

1.3 Block Diagram

Figure 1-2 shows the block diagram of the μPD4991A.

Figure 1-2. Block Diagram



1.4 Oscillation Stage and 15-stage Divider

A clock of 32.768 kHz is generated by using a 32.768-kHz crystal resonator and a CMOS inverter crystal oscillation circuit. This clock is divided by 15 to create a 1 Hz (1 second) time counter.

1.5 Mode and Register Configuration

The μPD4991A uses 13 data registers as time counters and 11 data registers to store alarm times. In addition, it also has six control/status registers for controlling the watch, alarm, and interval timer, and one mode register to specify the operation mode.

The μPD4991A has the following three modes.

1. **BASIC TIME MODE**
   Data write or read between the timer counter and CPU
   Command specification for control registers 1 and 2
2. **ALARM SET & TP1 CONTROL MODE**
   Data setting to alarm register
   TP1 function setting
   Leap year identification
   Command specification for control registers 1 and 2
3. **ALARM SET and TP2 CONTROL MODE**
   Data setting to alarm register
   TP2 function setting
   12-/24-hour mode selection
   Command specification for control registers 1 and 2

These modes can be selected by writing mode data (refer to **Table 2-1**) to address = 0F$_H$. Once a mode has been set, it remains valid until changed.

Table 1-2 shows the correspondence between registers and addresses.

Table 1-2. Registers and Their Addresses

ADDRESS		BASIC TIME MODE	TP 1 CONT.MODE	TP 2 CONT.MODE
HEX	MSB LSB	(TIME COUNTER)	(ALARM REGISTER)	(ALARM REGISTER)
0 H	0 , 0 , 0 , 0	Second, units digit	Second, units digit	
1 H	0 , 0 , 0 , 1	Second, tens digit	Second, tens digit	
2 H	0 , 0 , 1 , 0	Minute, units digit	Minute, units digit	
3 H	0 , 0 , 1 , 1	Minute, tens digit	Minute, tens digit	
4 H	0 , 1 , 0 , 0	Hour, units digit	Hour, units digit	
5 H	0 , 1 , 0 , 1	Hour, tens digit	Hour, tens digit	
6 H	0 , 1 , 1 , 0	Day of week digit	Day of week digit	
7 H	0 , 1 , 1 , 1	Date, units digit	Date, units digit	
08 H	1 , 0 , 0 , 0	Date, tens digit	Date, tens digit	
09 H	1 , 0 , 0 , 1	Month, units digit	Month, units digit	
0A H	1 , 0 , 1 , 0	Month, tens digit	Month, tens digit	
0B H	1 , 0 , 1 , 1	Year, units digit	TP1 FUNCTION CONT.	TP2 FUNCTION CONT.
0C H	1 , 1 , 0 , 0	Year, tens digit	Leap year counter	12-/24-hour mode, leap year valid/invalid
0D H	1 , 1 , 0 , 1	CONTROL REGISTER 1		
0E H	1 , 1 , 1 , 0	CONTROL REGISTER 2		
0F H	1 , 1 , 1 , 1	MODE REGISTER		

1.6 Cautions (Be sure to observe the following.)

1. Before writing the time, be sure to stop the watch.
   For details, refer to **3.1.1 Setting time**.

2. If the 12-hour mode has been changed to the 24-hour mode or vice versa, be sure to rewrite the hour counter.
   For details, refer to **(3) 12-/24-hour mode and leap year identification** in **2.3.3 ALARM SET & TP2 CONTROL MODE**.

3. Before changing the setting of the leap year counter, be sure to rewrite the year counter.
   For details, refer to **(3) Leap year counter** in **2.3.2 ALARM SET & TP1 CONTROL MODE**.

4. When accessing CONTROL REGISTER 2 to write during alarm coincidence, first set the alarm flag, and then access the register.
   For details, refer to **(3)** and **(4) CONTROL REGISTER 2** in **2.3.1 BASIC TIME MODE**.

5. Use TP1 or TP2 output, not X_{IN} or X_{OUT}, for adjustment of the oscillation frequency.
   For details, refer to **4.3 Adjusting Oscillation Frequency**.

6. Be sure to keep CS_2 low while the CPU is in the back-up status.
   For details, refer to **4.5 Power-Fail Circuit**.

7. Because only two digits are supported for the year code, use only the low-order 2 digits of the year when using the Western calendar.
   The μPD4991A correctly counts time even when the year changes from 1999 to 2000.
   This IC can automatically identify a leap year up till 2099. Although 2100 is not a leap year, the IC identifies this year as a leap year. However, if the user specifies a leap year, the other functions of this IC can continue to be used without any problem.

8. The application circuit and circuit constants in this document are shown for your reference only and are not intended to be used for mass production of an application system.
   The characteristic examples and application examples shown in this document are also for your reference only.
   When you design an actual application set, confirm that there are no operational problems.

[MEMO]

CHAPTER 2 OPERATIONS

2.1 Write Timing

Address A_0 through A_3 and data D_0 through D_3 are written to the IC when $\overline{WE}$ (write enable) is made high while $\overline{CS_1}$ = “L” and CS_2 = “H” (chip select status).

$\overline{WE}$ takes precedence over $\overline{OE}$ (read enable). Therefore, data can be written by asserting $\overline{WE}$ only when data is to be written, even when $\overline{OE}$ is always “L”.

Figures 2-1 and 2-2 show the write timing. To change the setting of the time counter, it is necessary to RESET/STOP the CLK. A correct value may not be written to the time counter if data is written to the time counter while it is operating. The other registers, however, are not affected.

Figure 2-1. Write Cycle Timing 1

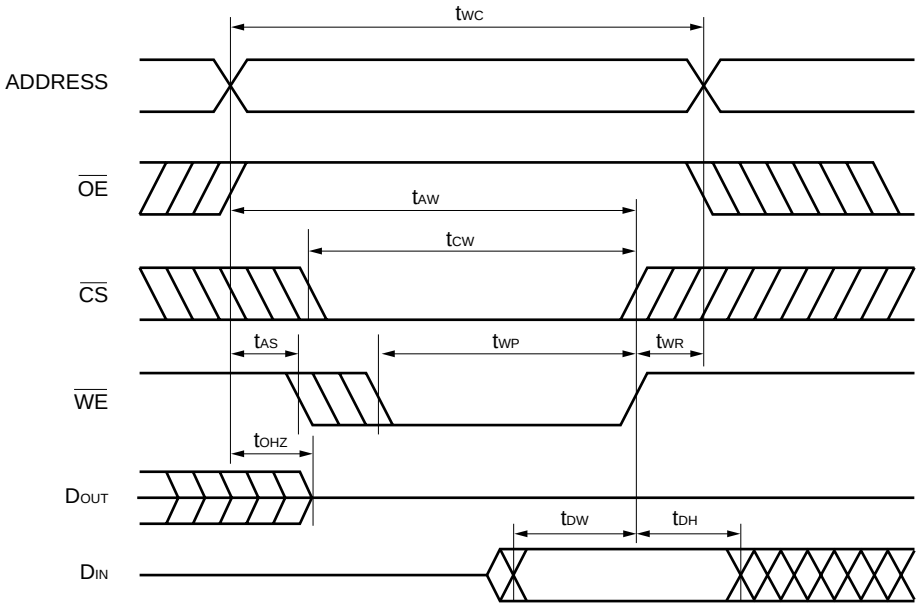
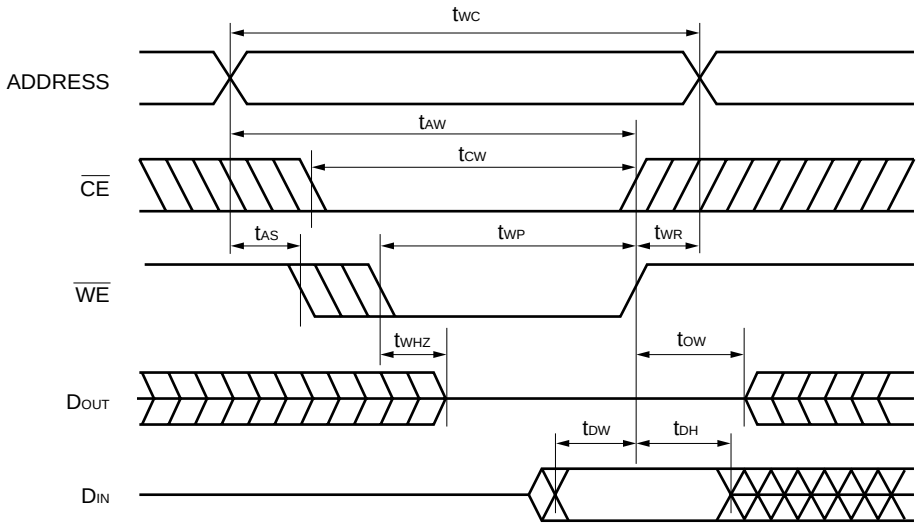


Figure 2-2. Write Cycle Timing 2 ($\overline{OE}$ = V_{IL})



2.2 Read Timing

The contents of address A_0 through A_3 are output to data D_0 through D_3 when $\overline{OE}$ (read enable) is made low while $\overline{CS_1}$ = "L" and $\overline{CS_2}$ = "H" (chip select status).

Figures 2-3 and 2-4 show the read timing. When a write-only (W/O) register is read, $0F_H$ is read to the data bus.

Because the value of the time counter is updated when a carry occurs from the 1-second digit, read the value of the time counter in accordance with the guidance in CHAPTER 3.

Figure 2-3. Read Cycle Timing 1

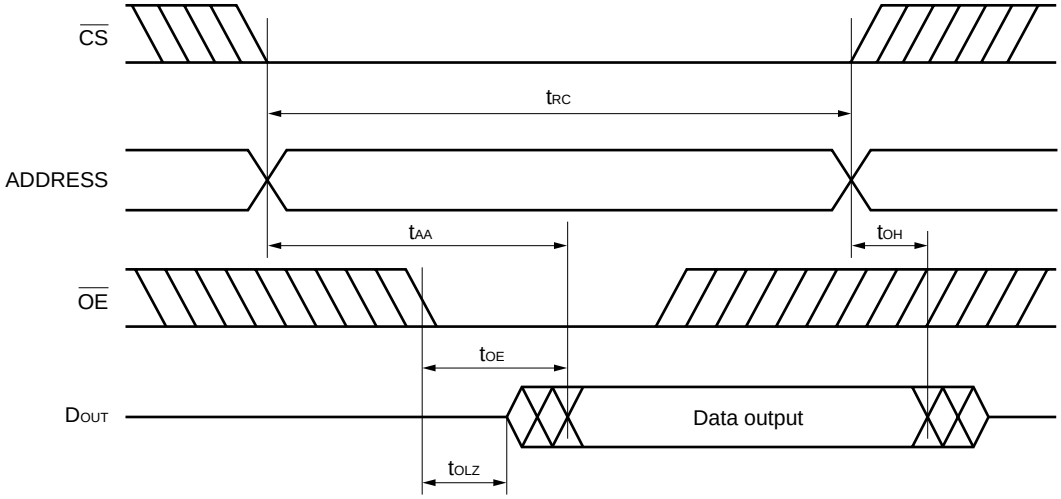
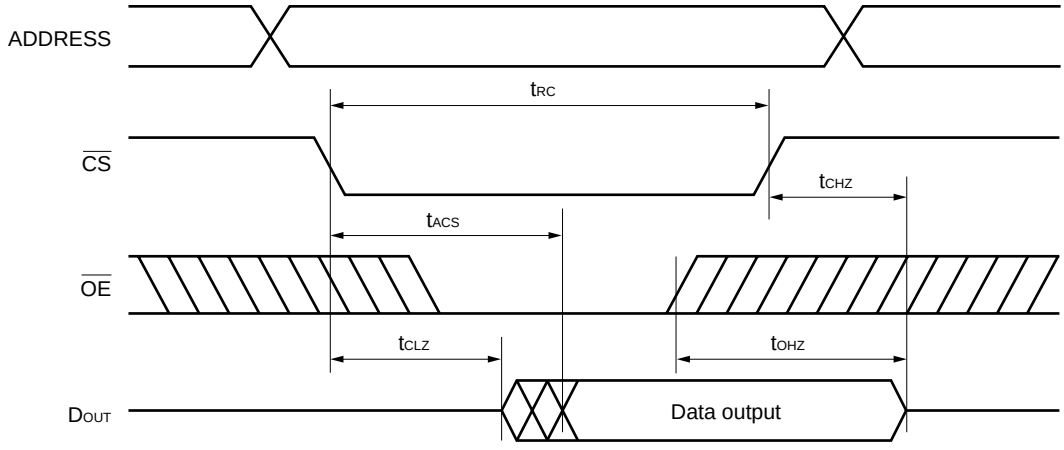


Figure 2-4. Read Cycle Timing 2



2.3 Mode Details

The registers assigned to addresses 0_H through $0C_H$ and the operation performed differ depending on the data written to address $0F_H$.

The μPD4991A has the following four major modes.

(1) BASIC TIME MODE (MODE REG. ← 0_H or 3_H)

In this mode, the timer counter can be accessed. Usually, this mode is used.

(2) TP1 CONTROL MODE (MODE REG. ← 1_H)

This mode is used to set alarm times and select an alarm output.

(3) TP2 CONTROL MODE (MODE REG. ← 2_H)

This mode is used to set alarm times and select an interval timer.

(4) TEST MODE (MODE REG. ← 08_H through $0F_H$)

This mode is used to test the functions of the time counter and alarm interval timer. When this mode is set, the time is fast-forwarded. Therefore, this mode is not used in normal operation.

Table 2-1 lists the modes.

Table 2-1. μPD4991A Mode List (address = $0F_H$)

X: Don't Care

Value Assigned to Mode Register			Operation Mode	Operation
HEX		D_3 D_2 D_1 D_0		
4_H	0_H	0, X, 0, 0	BASIC TIME	Sets and reads time data. Setting accuracy: 15.625 ms
5_H	1_H	0, X, 0, 1	ALARM SET & TP1 CONTROL	Sets alarm timer, selects TP1 output mode, and sets and reads leap year counter.
6_H	2_H	0, X, 1, 0	ALARM SET & TP2 CONTROL	Sets alarm timer, selects TP2 output mode, selects 12- or 24-hour mode, and validates or invalidates leap year.
7_H	3_H	0, X, 1, 1,	BASIC TIME	Same as MODE REG. ← 0_H. Setting accuracy: 30.52 μs
08_H		1, 0, 0, 0,	TEST (BASIC TIME)	Tests time counter. However, alarm and interval timer functions (TP1 and TP2) are undefined.
09_H		1, 0, 0, 1	TEST (BASIC TIME)	
$0A_H$		1, 0, 1, 0	TEST (BASIC TIME)	
$0B_H$		1, 0, 1, 1,	TEST (ALARM SET)	Tests alarm register and leap year counter.
$0C_H$		1, 1, 0, 0	TEST (ALARM SET)	Tests alarm register and selects 12- or 24-hour mode.
$0D_H$		1, 1, 0, 1	TEST (ALARM & TP1)	Tests alarm timer and TP1 output.
$0E_H$		1, 1, 1, 0	TEST (ALARM & TP2)	Tests alarm timer.
$0F_H$		1, 1, 1, 1	TEST (ALARM & TP2)	Tests interval timer and TP2 output.

2.3.1 BASIC TIME MODE (MODE REG. ← 0_H or 3_H)

In this mode, addresses 0_H through $0C_H$ are used as time counters to/from which time can be written or read (refer to **Table 2-2**).

Because a leap year cannot be identified or set and the 12- or 24-hour mode cannot be selected in this mode, setting related to a leap year and selection of the hour mode must be made in advance in TP1 CONTROL MODE or TP2 CONTROL MODE.

TIME RESET and ±30 sec ADJ. differ in operation depending on whether the MODE REGISTER is set to "0" or "3".

When TIME RESET or ±30 sec ADJ. is executed, the 15-stage divider that creates the 1 second pulse which is supplied to the timer counter is reset. **If the MODE REGISTER is set to "0", only stages 10 through 15 of the 15-stage divider are reset. Consequently, an error of up to 15.625 ms occurs**.

If the MODE REGISTER is set to "3", all the stages of the 15-stage divider are reset, and an error of up to 30.52 μs occurs. Because stages 1 through 9 of the 15-stage divider are used as the first stages of the interval timer, **an error of up to 1.95 ms occurs in the interval timer if all the stages of the divider are reset**.

Figure 2-5. Block Diagram of 15-Stage Divider

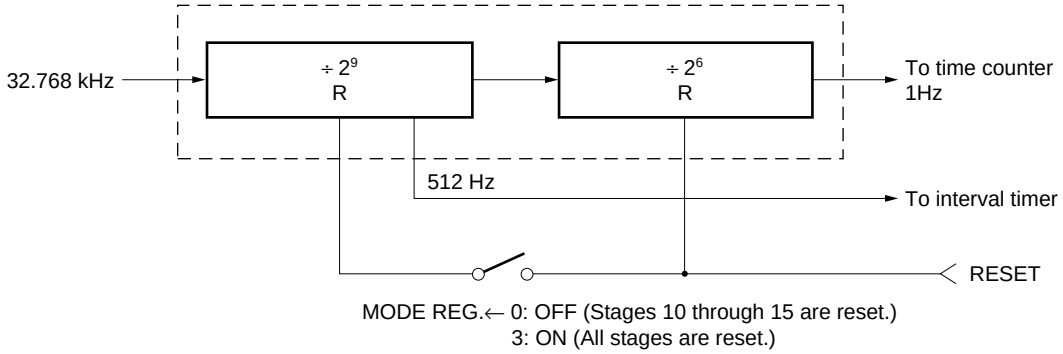


Table 2-2. Register Assignment in BASIC TIME MODE

<table>
<tr><th>Address</th><th>Register</th><th>Description</th></tr>
<tr><td>0 H</td><td>Second, units digit</td><td rowspan="12">Directly connected to time counter and updated in real-time.
Data format is BCD.
If time that does not exist is set (e.g., minute 70, hour 30, 13 p.m., February 30, etc.), then the wrong time is set.

(Note) The second highest bit D_2 of the 10-hour digit functions as $\overline{AM}$/PM flag in 12-hour mode (e.g., 5 p.m. is indicated as hour 45).

<table>
<tr><th></th><th>D_3</th><th>D_2</th><th>D_1</th><th>D_0</th></tr>
<tr><td>12-hour mode
R/W</td><td>X</td><td>$\overline{AM}$/PM flag</td><td>Data</td><td>Data</td></tr>
</table>
</td></tr>
<tr><td>1 H</td><td>Second, tens digit</td></tr>
<tr><td>2 H</td><td>Minute, units digit</td></tr>
<tr><td>3 H</td><td>Minute, tens digit</td></tr>
<tr><td>4 H</td><td>Hour, units digit</td></tr>
<tr><td>5 H</td><td>Hour, tens digit</td></tr>
<tr><td>6 H</td><td>Day of week digit</td></tr>
<tr><td>7 H</td><td>Date, units digit</td></tr>
<tr><td>08 H</td><td>Date, tens digit</td></tr>
<tr><td>09 H</td><td>Month, units digit</td></tr>
<tr><td>0A H</td><td>Month, tens digit</td></tr>
<tr><td>0B H</td><td>Year, units digit</td></tr>
<tr><td>0C H</td><td>Year, tens digit</td></tr>
<tr><td>0D H</td><td>CONTROL
REGISTER 1</td><td>
<table>
<tr><th></th><th>D_3</th><th>D_2</th><th>D_1</th><th>D_0</th></tr>
<tr><td>W/O</td><td>CLK
WAIT</td><td>CLK
STOP</td><td>±30 s
ADJ.</td><td>TIME
RESET</td></tr>
</table>
</td></tr>
<tr><td>0E H</td><td>CONTROL
REGISTER 2</td><td>
<table>
<tr><th></th><th>D_3</th><th>D_2</th><th>D_1</th><th>D_0</th></tr>
<tr><td>Write</td><td>0</td><td>Alarm
Disable</td><td>Alarm
Flag</td><td>TP1
Disable</td></tr>
<tr><td>Write</td><td>1</td><td>INT
STOP</td><td>INT
RESET</td><td>TP2
Disable</td></tr>
<tr><td>Read</td><td>X</td><td>Busy</td><td>Alarm
Flag</td><td>TP2
Flag</td></tr>
</table>
</td></tr>
<tr><td>0F H</td><td>MODE
REGISTER</td><td>W/O. Refer to Mode List.</td></tr>
</table>

X: Don’t Care
W/O: Write only

(1) Time counter (addresses 0_H through $0C_H$)

This counter stores time data in BCD format. **If time that does not exist is set, the wrong time is indicated. Be sure to set correct data.** The day counter takes a value from 0 to 6. The user can specify which value takes which day (Monday through Sunday). Tables 2-3 and 2-4 show correspondence between time and data.

Table 2-3. Time Counter Data

TIME COUNTER	DATA	TIME COUNTER	DATA
Second, units digit	0–9	Date, units digit	0–9
Second, tens digit	0–5	Date, tens digit	0–3
Minute, units digit	0–9	Month, units digit	0–9
Minute, tens digit	0–5	Month, tens digit	0–1
Hour, units digit	0–9	Year, units digit	0–9
Hour, tens digit	0–5	Year, tens digit	0–9
Day of week digit	0–6		

Table 2-4. Hour Counter Data

Time	24-Hour Mode	12-Hour Mode	Time	24-Hour Mode	12-Hour Mode
1 a.m.	01 H	01 H	1 p.m.	13 H	41 H
2 a.m.	02 H	02 H	2 p.m.	14 H	42 H
3 a.m.	03 H	03 H	3 p.m.	15 H	43 H
4 a.m.	04 H	04 H	4 p.m.	16 H	44 H
5 a.m.	05 H	05 H	5 p.m.	17 H	45 H
6 a.m.	06 H	06 H	6 p.m.	18 H	46 H
7 a.m.	07 H	07 H	7 p.m.	19 H	47 H
8 a.m.	08 H	08 H	8 p.m.	20 H	48 H
9 a.m.	09 H	09 H	9 p.m.	21 H	49 H
10 a.m.	10 H	10 H	10 p.m.	22 H	50 H
11 a.m.	11 H	11 H	11 p.m.	23 H	51 H
12 a.m.	12 H	52 H	12 p.m.	00 H	12 H

(2) CONTROL REGISTER 1 (address: $0D_H$)

This register controls clock supply to the timer counter, makes adjustments of ±30 seconds, and resets the 15-stage divider. Figure 2-6 shows the configuration of the control register 1, and Table 2-5 shows the commands of the register.

Figure 2-6. Configuration of Control Register 1

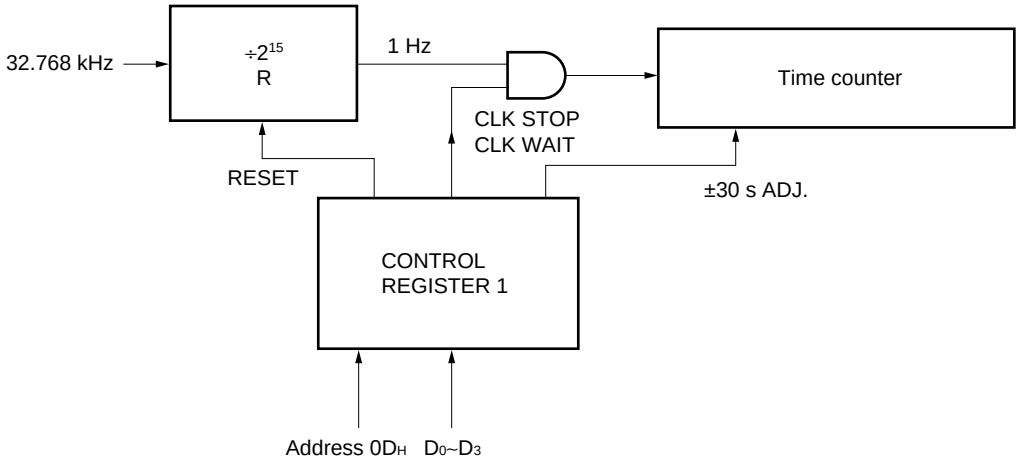


Table 2-5. CONTROL REGISTER 1 Command List (W/O)

HEX	D_3 D_2 D_1 D_0	Command	Operation
0_H	0, 0, 0, 0	CLOCK START	Starts time counter.
1_H	0, 0, 0, 1	CLOCK RESET START	Resets and then starts time counter.
2_H	0, 0, 1, 0	±30 sec ADJUST	Makes adjustment of ±30 seconds.
4_H	0, 1, 0, 0	CLOCK STOP	Stops time counter (when written).
8_H	1, 0, 0, 0	CLOCK WAIT	Stops time counter (when read).

(a) CLOCK RESET START (15-stage divider reset)

This command resets the 15-stage divider. When the MODE REGISTER is set to 0, stages 10 through 15 of the divider are reset; when the MODE REGISTER is set to 3, all the stages are reset. A carry occurs in the time counter about 1 second after this command has been executed.

This command is used when time data is written.

(b) ±30 sec ADJUST (±30-second adjustment)

This command resets the second counter (to 00 seconds).

If this command is executed when the value of the second counter between 00 and 29, it is reset to 00 without the units digit for minutes being affected. If it is executed when the second counter between 30 and 59, the counter is reset to 00 and the units digit for minutes is incremented by one.

This adjustment is carried across all the digits.

Example: 9 hours 59 minutes 45 seconds → 10 hours 00 minutes 00 seconds

(c) CLOCK STOP and CLOCK WAIT (stops time counter)

Both these commands disable input of the clock (1 Hz) to the watch counter and stop the watch. CLOCK STOP is used when time data is **written** (be sure to stop the watch when writing time data). CLOCK WAIT is used when time data is **read**. This is to prevent a new count from occurring and the CPU from reading wrong data when time data is read. Time data can be also read by using the BUSY signal or by reading the time data two times, without using CLOCK WAIT.

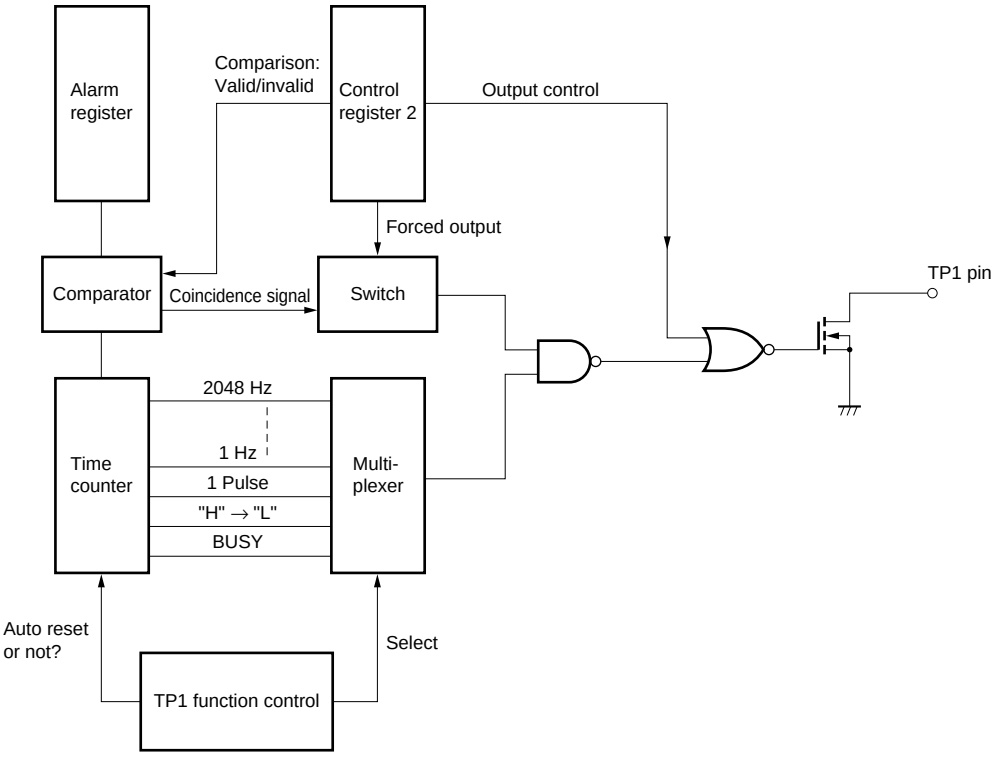
If the clock input is resumed within 0.5 seconds after the watch has been stopped by CLOCK STOP or CLOCK WAIT, the real time is not delayed (if a carry occurs from 1-second digit while the watch is stopped, adjustment of +1 second is made after the clock input is resumed).

(3) CONTROL REGISTER 2 (address 0E$_H$) [during write]

This register controls the alarm signal output to TP1 and the interval signal output to TP2. Figure 2-7 shows the diagram of the TP pin control block, and Table 2-6 lists the commands of CONTROL REGISTER 2.

Figure 2-7. TP Pin Control Block Diagram

Alarm signal control block



Interval timer control block

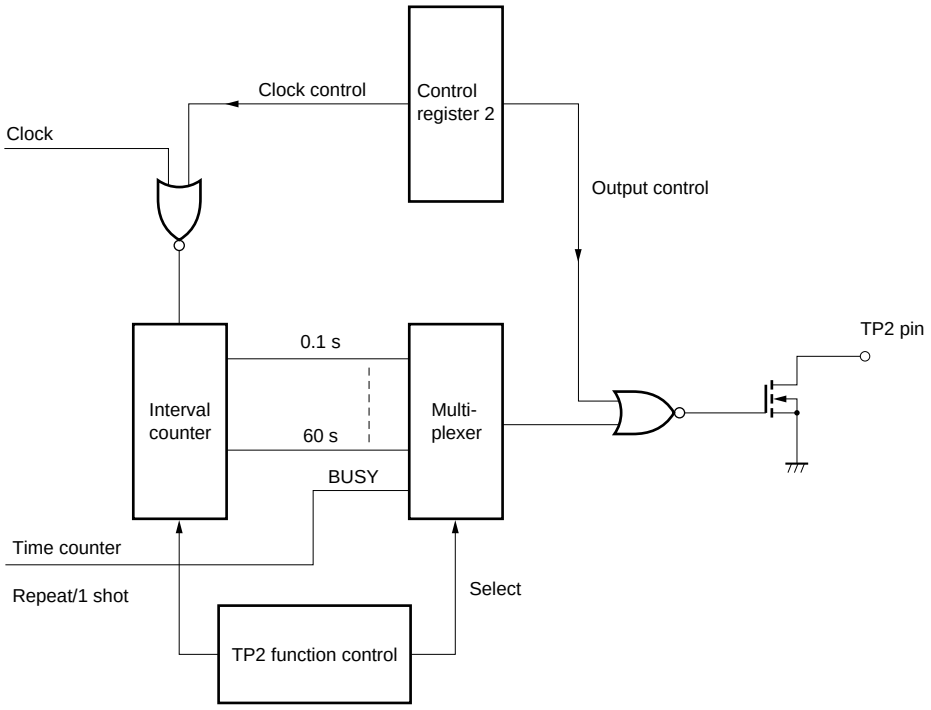


Table 2-6. CONTROL REGISTER 2 Command List (W/O)

D_3	D_2	D_1	D_0
0	ALARM DISABLE	ALARM FLAG	TP1 DISABLE
1	INTERVAL STOP	INTERVAL RESET	TP2 DISABLE

(a) TP1 control (when D_3 = 0)

i) TP1 DISABLE (D_0)

This bit controls output of TP1. When this bit is set, TP1 is forcibly turned OFF (high impedance) regardless of the other operations.

ii) ALARM FLAG (D_1)

This flag forcibly sets the alarm coincidence/non-coincidence status.

When this bit is set, the alarm coincidence status is set; when it is reset, the alarm non-coincidence status is set.

iii) ALARM DISABLE (D_2)

This bit makes valid/invalid the alarm register and the result of comparison by the time counter. When this bit is set, the result of comparison of alarm is ignored and the ALARM FLAG is not affected. If ALARM DISABLE and ALARM FLAG are set, therefore, the alarm signal can be always output to TP1.

(b) TP2 control (when D_3 = 1)

i) TP2 DISABLE (D_0)

This bit controls output of TP2. When this bit is set, TP2 is forcibly turned off (high impedance) regardless of the other operations.

ii) INTERVAL RESET (D_1)

When this bit is set, the interval timer is reset.

iii) INTERVAL STOP (D_2)

When this bit is set, the interval timer is stopped. If TP2 is low, however, the interval timer is stopped 30.5 μs after the low period.

(4) CONTROL REGISTER 2 (address $0E_H$) [during read]

Control register 2 is used to monitor the BUSY signal, interval signal, and alarm status.

Table 2-7. CONTROL REGISTER 2 Status (R/O)

D_3	D_2	D_1	D_0
X	BUSY FLAG	ALARM FLAG	INTERVAL FLAG

(a) BUSY FLAG

This is the count flag of the time counter. When this bit is 1, the time counter is in a count period. For details, refer to **(d) BUSY signal** in **2.3.2 (2)**.

(b) ALARM FLAG

When this bit is 1, it indicates an alarm coincidence status; when it is 0, it indicates an alarm non-coincidence status.

(c) INTERVAL FLAG

When this bit is 1, the interval output of TP2 is L; when it is 0, the interval output of TP2 is H.

Caution

If data is written to CONTROL REGISTER 2 in the alarm coincidence status, the ALARM FLAG may be reset. To access CONTROL REGISTER 2 to write, therefore, be sure to check whether the alarm coincidence or non-coincidence status is set (by reading the ALARM FLAG). In the alarm coincidence status, set the ALARM FLAG, and then access CONTROL REGISTER 2 to write.

2.3.2 ALARM SET & TP1 CONTROL MODE (MODE REG. ← 1)

In this mode, addresses 0_H through $0A_H$ are used as alarm registers that are used to set and check alarm times. Address $0B_H$ is used as a control register that selects an alarm coincidence signal to be output to TP1, and address $0C_H$ is used as a leap year counter. Addresses $0D_H$ through $0F_H$ are used in the same way as in the BASIC TIME MODE (refer to **Table 2-8**).

Table 2-8. Register Assignment in ALARM SET & TP1 CONTROL MODE

<table>
<tr><th>Address</th><th>Register</th><th>Description</th></tr>
<tr><td>0 H</td><td>Second, units digit</td><td rowspan="10">Alarm register
Sets and checks alarm time.
When these registers are set to $0F_H$, the digit corresponding to each register is assumed to coincide with the value of the time counter. When the alarm function is not used, these registers can be used as a back-up memory of 4 bits x 11 words (in which case alarm must be disabled).</td></tr>
<tr><td>1 H</td><td>Second, tens digit</td></tr>
<tr><td>2 H</td><td>Minute, units digit</td></tr>
<tr><td>3 H</td><td>Minute, tens digit</td></tr>
<tr><td>4 H</td><td>Hour, units digit</td></tr>
<tr><td>5 H</td><td>Hour, tens digit</td></tr>
<tr><td>6 H</td><td>Day of week digit</td></tr>
<tr><td>7 H</td><td>Date, units digit</td></tr>
<tr><td>08 H</td><td>Date, tens digit</td></tr>
<tr><td>09 H</td><td>Month, units digit</td></tr>
<tr><td>0A H</td><td>Month, tens digit</td></tr>
<tr><td>0B H</td><td>TP1 FUNCTION CONTROL</td><td>W/O. Selects TP1 output waveform.</td></tr>
<tr><td>0C H</td><td>Leap year counter</td><td>
<table>
<tr><th></th><th>D_3</th><th>D_2</th><th>D_1</th><th>D_0</th></tr>
<tr><td>R/W</td><td>X</td><td>X</td><td colspan="2">Leap year counter</td></tr>
</table>
0_H of this register indicates a leap year. This register takes a value of 0_H to 3_H.
</td></tr>
<tr><td>0D H</td><td>CONTROL REGISTER 1</td><td rowspan="3">Same in BASIC TIME MODE</td></tr>
<tr><td>0E H</td><td>CONTROL REGISTER 2</td></tr>
<tr><td>0F H</td><td>MODE REGISTER</td></tr>
</table>

X: Don't Care
W/O: Write only

(1) Alarm registers (addresses 0_H through $0A_H$)

Alarm time can be set in units from months to seconds. The contents written to the alarm registers are compared with the time counter each time a carry occurs from the second digits. If an alarm register is set to $0F_H$, the corresponding digit is assumed to coincide with the value of the time counter. When all the digits coincide, the ALARM FLAG is set, and the output waveform selected by TP1 FUNCTION CONTROL register is output under control of CONTROL REGISTER 1.

If $0F_H$ is written to some of the alarm registers, the following operations can be performed.

Example 1. Alarm coincides with the value of the time counter for 10 seconds every hour

Month, tens digit	Month, units digit	Date, tens digit	Date, units digit	Day of week digit	Hour, tens digit	Hour, units digit	Minute, tens digit	Minute, units digit	Second, tens digit	Second, units digit
0FH	0FH	0FH	0FH	0FH	0FH	0FH	0 H	0 H	0 H	0FH

From 00 minutes 0 seconds to 00 minutes 09 seconds the alarm value coincides with the value of the time counter.

Example 2. Alarm coincides with the value of the time counter for 24 hours on the first day of every month.

Month, tens digit	Month, units digit	Date, tens digit	Date, units digit	Day of week digit	Hour, tens digit	Hour, units digit	Minute, tens digit	Minute, units digit	Second, tens digit	Second, units digit
0FH	0FH	0 H	1 H	0FH	0FH	0FH	0FH	0FH	0FH	0FH

(2) TP1 FUNCTION CONTROL REGISTER (address 0BH)

These registers select the waveform that is to be output to TP1 (refer to **Table 2-9**).

Table 2-9. TP1 FUNCTION CONTROL REGISTERS

DATA			Operation	Description
HEX		D_3 D_2 D_1 D_0		
08 H	0 H	X, 0, 0, 0	2048 Hz	Output at duty factor of 50%
09 H	1 H	X, 0, 0, 1	1024 Hz	
0AH	2 H	X, 0, 1, 0	64 Hz	
0BH	3 H	X, 0, 1, 1	16 Hz	
0CH	4 H	X, 1, 0, 0	1 Hz	
0DH	5 H	X, 1, 0, 1	1 pulse	1-shot output with a pulse width of 30.5 μs during L period
0EH	6 H	X, 1, 1, 0	"H" $\rightarrow$ " L"	"L" during coincidence
	7 H	0, 1, 1, 1	BUSY	1-second count flag
		0, X, X, X	Alarm coincidence with auto reset	Resets ALARM FLAG and stops alarm output in case of alarm non-coincidence
		1, X, X, X	Alarm coincidence without auto reset	Once alarm coincidence has occurred, continues output even if alarm non-coincidence occurs.

X: Don't Care

(a) 1- to 2048-Hz output

These registers output a waveform with a duty factor of 50%. This waveform is always output to TP1 if the alarm is disabled and forced coincidence is selected by CONTROL REGISTER 2 (address 0EH $\leftarrow$ 6H).

(b) 1-pulse output

This register outputs a low-active pulse only once (pulse width: 30.5 μs).

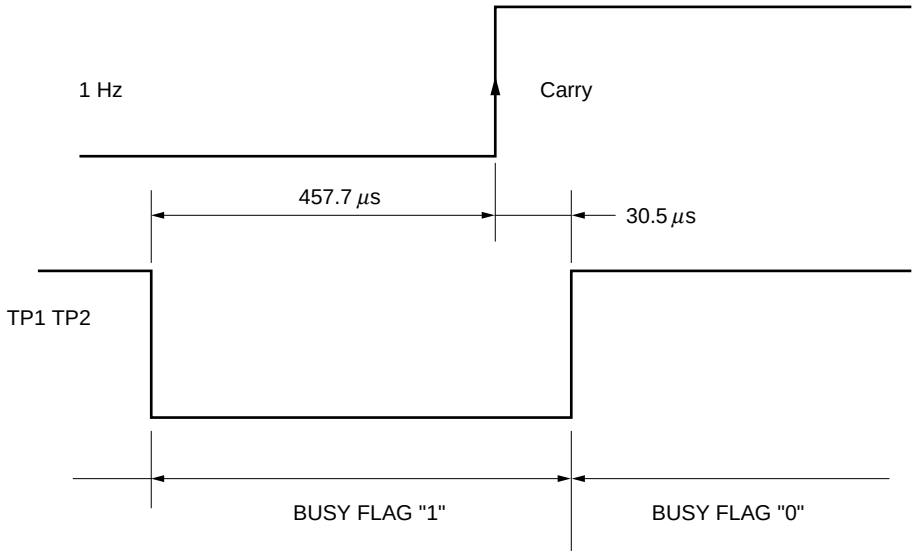
(c) "H" $\rightarrow$ "L"

This register goes from H to L on alarm coincidence. It keeps L in the case of alarm non-coincidence.

(d) BUSY signal

This is the count flag of the time counter. A carry occurs in the time counter 457.7 μs after the BUSY signal has risen. **If the value of the time counter is read while a carry occurs, the correct value may not be read.** For details, refer to **CHAPTER 3 ACCESS PROCEDURE**.

Figure 2-8. BUSY Signal

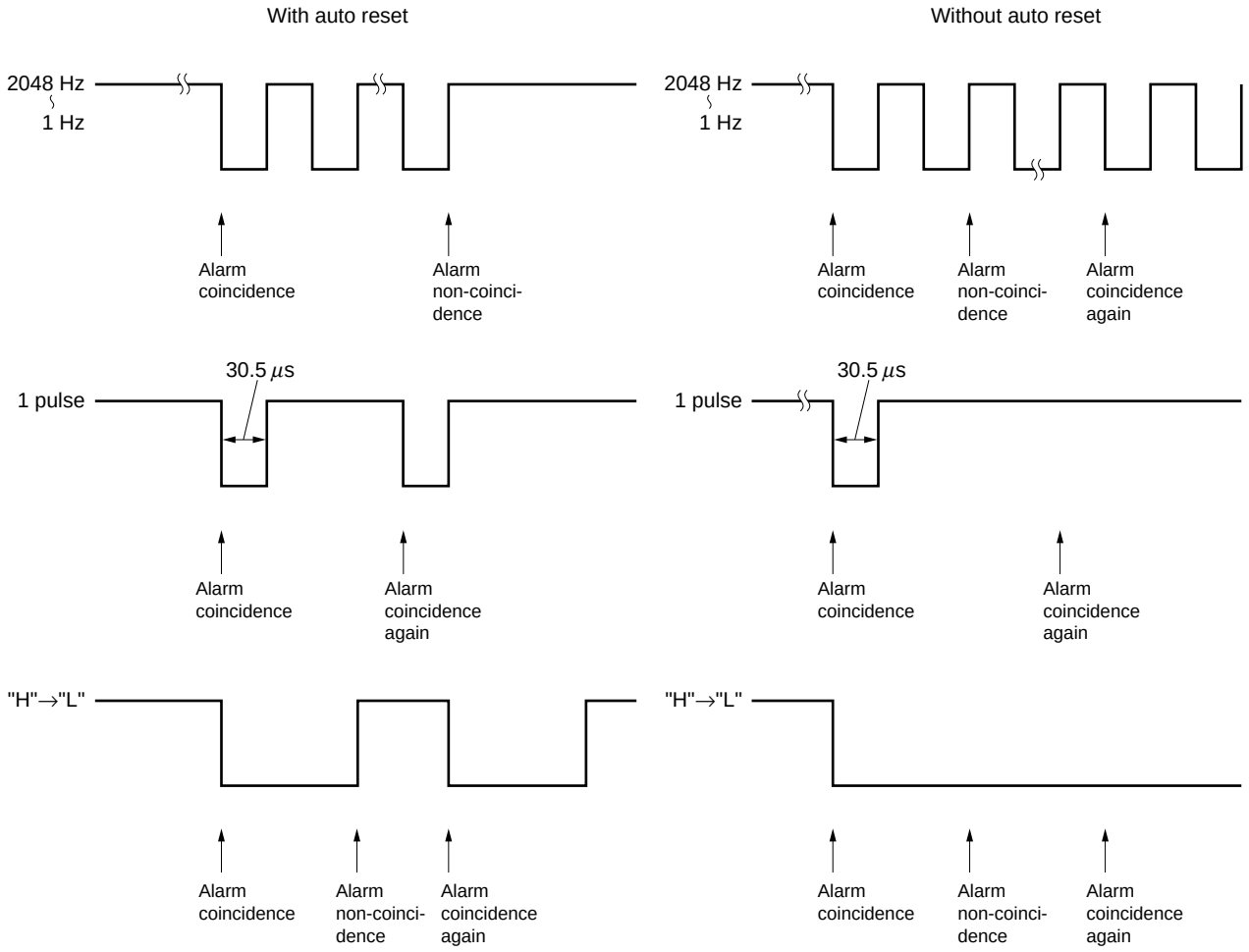


(e) Alarm flag with auto reset

When alarm coincidence occurs, the μPD4991A sets the ALARM FLAG and outputs an alarm signal to TP1. When alarm no longer coincides with the value of the time counter, and if the alarm coincidence with auto reset function is selected, the μPD4991A resets the ALARM FLAG and stops output from TP1 (restores to the H level).

If the alarm coincidence with auto reset function is not selected, TP1 output is not stopped. To stop it, write 0 to the ALARM FLAG of CONTROL REGISTER 2. This operation is illustrated in Figure 2-9.

Figure 2-9. TP1 Output Waveform



(3) Leap year counter (low-order 2 bits of address 0C$_H$)

This counter takes a value of 0$_H$ to 3$_H$ and is synchronized with the year counter. When the value of the leap counter is 0$_H$, a leap year is identified. If the leap year identification function is enabled, the last day of February in the leap year is 29.

Usually, the leap year counter is automatically set when the lower 2 digits of a year is written in the BASIC TIME MODE. Therefore, the user does not have to write a leap year. The μPD4991A operates from 1901 to 2099 without adjustment.

If a year other than a Western calender year is written to the year counter, the leap year counter may be rewritten after the year counter has been written (if the year is Showa in the Japanese calender, for example, divide the Showa year by 4 and add 1 to the result. Write this year to the leap year counter. Unless the year counter is rewritten, leap years will be automatically identified after that.)

If the year is Heisei, write the year to the year counter. The leap year counter does not have to be rewritten.

(4) CONTROL REGISTER 1

This register controls the clock of the time counter in the same manner as in the BASIC TIME MODE.

(5) CONTROL REGISTER 2

This register controls output of TP1 and TP2, alarm coincidence, and the clock to the interval timer, in the same manner as in the BASIC TIME MODE.

(6) MODE REGISTER

This register determines the operation mode of the μPD4991A in the same manner as in the BASIC TIME MODE.

2.3.3 ALARM SET & TP2 CONTROL MODE (MODE REG. ← 2)

In this mode, addresses 0_H through $0A_H$ are used as alarm registers (in the same manner as in the TP1 CONTROL MODE). Address $0B_H$ is used as a control register that selects an interval signal to be output to TP2, and address $0C_H$ is used to select 12- or 24-hour mode and enables or disables the leap year identification function. Addresses $0D_H$ through $0F_H$ are used in the same way as in the BASIC TIME MODE (refer to **Table 2-10**).

Table 2-10. Register Assignment in ALARM SET & TP2 CONTROL MODE

<table>
<tr><th>Address</th><th>Register</th><th>Description</th></tr>
<tr><td>0 H</td><td>Second, units digit</td><td rowspan="10">Alarm register
Sets and checks alarm time.
When these registers are set to $0F_H$, the digit corresponding to each register is assumed to coincide with the value of the time counter. When the alarm function is not used, these registers can be used as a back-up memory of 4 bits × 11 words (same as in TP1 CONTROL MODE).</td></tr>
<tr><td>1 H</td><td>Second, tens digit</td></tr>
<tr><td>2 H</td><td>Minute, units digit</td></tr>
<tr><td>3 H</td><td>Minute, tens digit</td></tr>
<tr><td>4 H</td><td>Hour, units digit</td></tr>
<tr><td>5 H</td><td>Hour, tens digit</td></tr>
<tr><td>6 H</td><td>Day of week digit</td></tr>
<tr><td>7 H</td><td>Date, units digit</td></tr>
<tr><td>08 H</td><td>Date, tens digit</td></tr>
<tr><td>09 H</td><td>Month, units digit</td></tr>
<tr><td>0A H</td><td>Month, tens digit</td></tr>
<tr><td>0B H</td><td>TP1 FUNCTION CONTROL</td><td>W/O. Selects TP2 output waveform.</td></tr>
<tr><td>0C H</td><td>Selects 12- or 24-hour mode and enables/ disables leap year identification</td><td>
<table>
<tr><th></th><th>D_3</th><th>D_2</th><th>D_1</th><th>D_0</th></tr>
<tr><td>R/W</td><td>$\overline{12}$/24H mode</td><td>Leap year identification disable</td><td>X</td><td>X</td></tr>
</table>
</td></tr>
<tr><td>0D H</td><td>CONTROL REGISTER 1</td><td rowspan="3">Same as in BASIC TIME MODE</td></tr>
<tr><td>0E H</td><td>CONTROL REGISTER 2</td></tr>
<tr><td>0F H</td><td>MODE REGISTER</td></tr>
</table>

X: Don't Care
W/O: Write only

(1) Alarm registers (addresses 0_H through $0A_H$)

These registers operate in the same manner as in the TP1 CONTROL MODE. Refer to **2.3.2 (1)**.

(2) TP2 FUNCTION CONTROL REGISTER (address $0B_H$)

These registers select the waveform that is to be output to TP2.

Table 2-11. TP2 FUNCTION CONTROL REGISTER

DATA			Operation	Description
HEX		D_3 D_2 D_1 D_0		
08 H	0 H	X, 0, 0, 0	0.1 sec INTERVAL	Interval timer output with pulse width of 30.5 μs during L period
09 H	1 H	X, 0, 0, 1	1 sec INTERVAL	
0A H	2 H	X, 0, 1, 0	10 sec INTERVAL	
0B H	3 H	X, 0, 1, 1	30 sec INTERVAL	
0C H	4 H	X, 1, 0, 0	60 sec INTERVAL	
	7 H	0, 1, 1, 1	BUSY signal	Count flag of time counter
		0, X, X, X	INTERVAL REPEAT	Successively performs interval output
		1, X, X, X	INTERVAL 1 SHOT	Performs interval output in only one cycle

X: Don't Care

(a) 0.1- to 60-sec INTERVAL output

These registers output an interval signal with a cycle of 0.1 to 60 seconds and a pulse width of 30.5 μs during the L period.

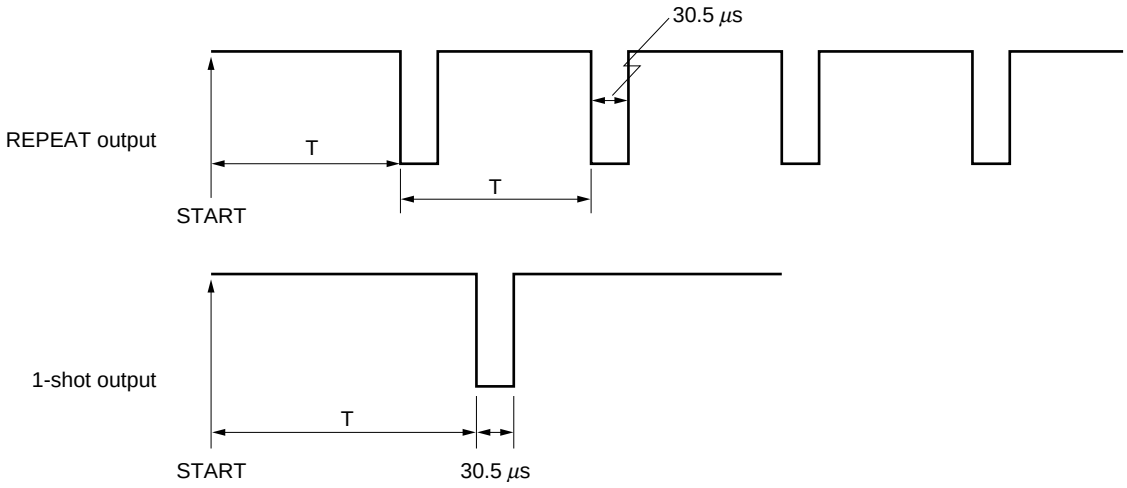
(b) BUSY

This is the count flag of the time counter and is the same as the BUSY signal in the TP1 CONTROL MODE.

(c) INTERVAL REPEAT/INTERVAL 1 SHOT

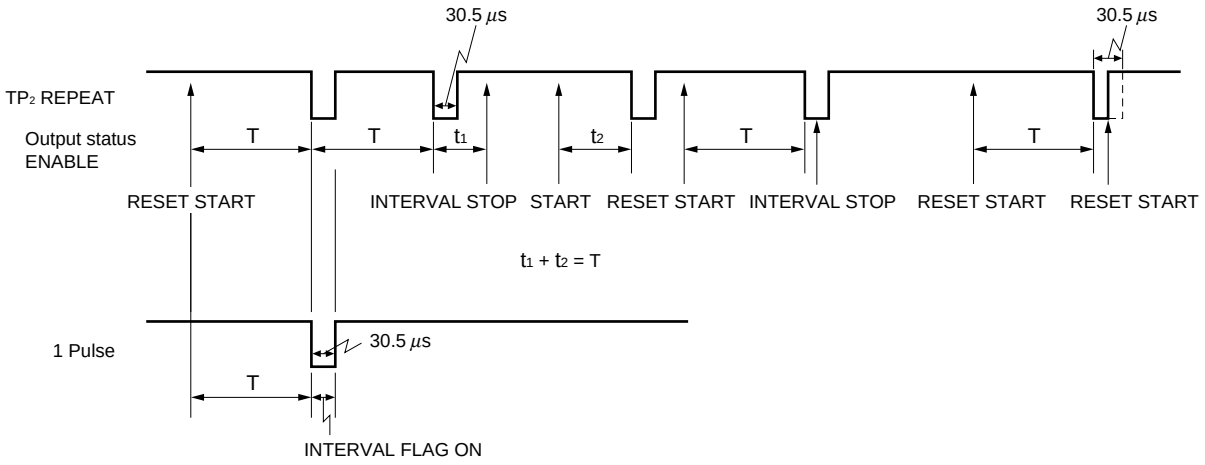
These registers control the repetition of the interval signal. Figure 2-10 shows the differences between the two.

Figure 2-10. TP2 Output Waveform



If CONTROL REGISTER 2 described earlier is used, the control operation shown in Figure 2-11 can be performed.

Figure 2-11. Interval Signal Output Example

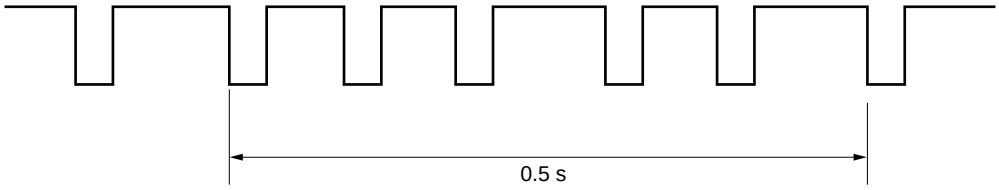


Note If the output status is disabled, the output is turned off (high impedance) regardless of the status of TP2.

Caution

The interval output is produced not once in a cycle of 0.1 s but in five times, as shown below.

Figure 2-12. 0.1-Second Interval Output



(3) 12-/24-hour mode and leap year identification (address 0CH)

Table 2-12. 12-/24-Hour Mode and Leap Year Identification Command (R/W)

D3	D2	D1	D0
$\overline{12}$-/24-hour mode	Leap year identification	X	X

X: Don't Care

(a) 12-/24-hour mode selection

This bit selects the 12-hour mode when it is 0; when it is 1, the 24-hour mode is selected.

In the 12-hour mode, the second highest bit (D_2) of the tens digit of hour serves as the $\overline{AM}$/PM flag.

Example

	Hour, tens digit				Hour, units digit				
	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	HEX
5 a.m.	0	0	0	0	0	1	0	1	05 H
		↕	$\overline{AM}$/PM flag						
5 p.m.	0	1	0	0	0	1	0	1	45 H
11 a.m.	0	0	0	1	0	0	0	1	11 H
11 p.m.	0	1	0	1	0	0	0	1	51 H

Caution

If the mode is changed between the 12- and 24-hour modes, the hour counter must be rewritten (if this flag is changed after data has been written to the hour counter, the value of the hour counter may be lost).

(b) Leap year identification

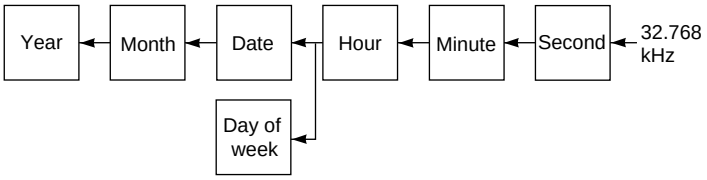
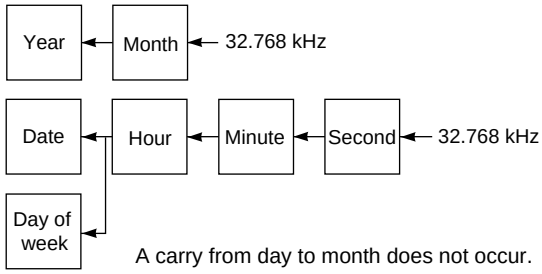
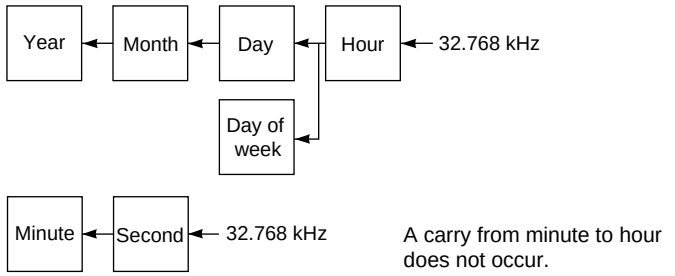
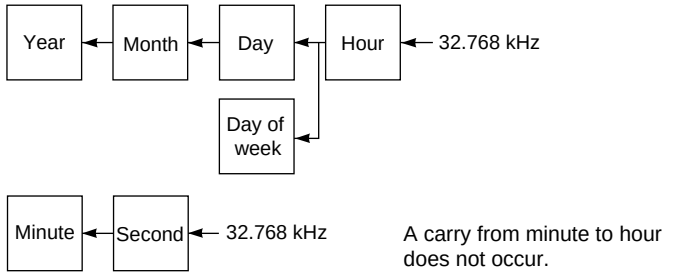
When this bit is set to 1, the leap year identification function is disabled. As a result, the end of February is 28 even if the value of the leap year counter is xx00.

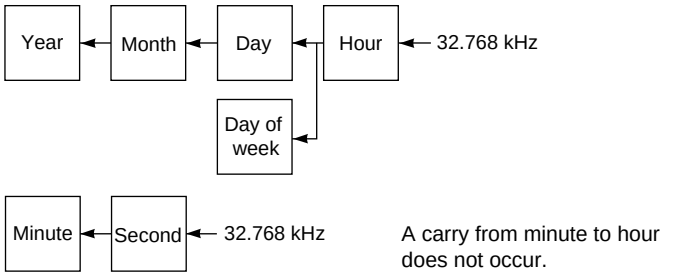
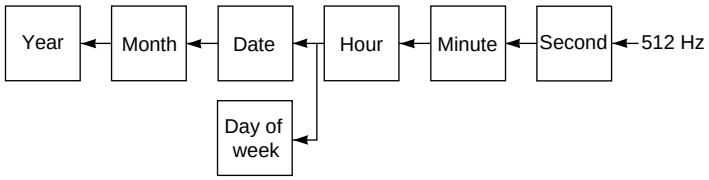
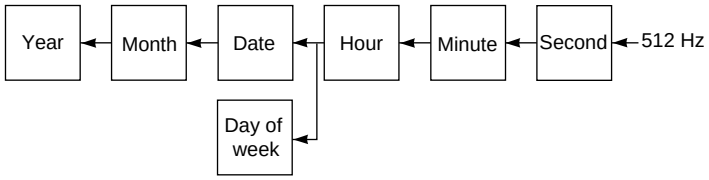
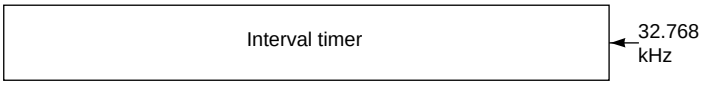
2.3.4 TEST MODE

This mode is to test the functions of the μPD4991A. In the TEST mode, a total of eight modes can be selected: three TEST (BASIC TIME) MODEs in which the time counter is read/written, two TEST (ALARM SET & TP1 CONT.) MODEs of the alarm timer, and three TEST (ALARM SET & TP2 CONT.) MODEs of the interval timer.

In each mode, the clock is input to the counter differently. For details, refer to **Table 2-13. Test Modes of μPD4991A**. Note that **some functions are disabled in the test mode**. Because the test mode is to test the functions, continous operation is not guaranteed if the device is normally used in the test mode.

Table 2-13. Test Modes of μPD4991A

Value Set to Mode Register					Operation Mode	Operation
HEX	D_3	D_2	D_1	D_0		
8 H	1,	0,	0,	0	TEST (BASIC TIME)	Second ← 32.768 kHz (fast-forward of 32768 times) Time data can be set and read, but the status of TP1 and TP2 is undefined. 
9 H	1,	0,	0,	1	TEST (BASIC TIME)	Second ← 32.768 kHz, Month ← 32.768 kHz Time data can be set and read, but the status of TP1 and TP2 is undefined. 
0AH	1,	0,	1,	0	TEST (BASIC TIME)	Second ← 32.768 kHz, Hour ← 32.768 kHz Time data can be set and read, but the status of TP1 and TP2 is undefined. 
0BH	1,	1,	0,	0	TEST (ALARM SET & TP1 CONTROL)	Second ← 32.768 kHz, Hour ← 32.768 kHz Sets alarm timer, selects TP1 output mode, and enables or disables leap year identification. However, the status of TP1 and TP2 is undefined. In this mode, time data cannot be written or read. 

Value Set to Mode Register					Operation Mode	Operation
HEX	D_3	D_2	D_1	D_0		
$0C_H$	1,	1,	0,	1	TEST (ALARM SET & TP2 CONTROL)	Second ← 32.768 kHz, Hour ← 32.768 kHz Sets alarm timer, selects TP2 output mode, and writes/reads data to/from leap year counter. However, the status of TP1 and TP2 is undefined. In this mode, time data cannot be written or read.  A carry from minute to hour does not occur.
$0D_H$	1,	1,	1,	0	TEST (ALARM SET & TP1 CONTROL)	Second ← 512 Hz (fast-forward of 512 times) Sets alarm timer, selects TP1 output mode, and selects leap year identification function. In this mode, time data cannot be written or read. 
$0E_H$	1,	1,	1,	0	TEST (ALARM SET & TP2 CONTROL)	Second ← 512 Hz Sets alarm timer, selects TP2 output mode, and writes/reads data to/from leap year counter. However, time data cannot be set/read in this mode. 
$0F_H$	1,	1,	1,	1	TEST (ALARM SET & TP2 CONTROL)	Interval timer ← 32.768 kHz Sets alarm timer, selects TP2 output mode, writes/reads data to/from leap year counter. In this mode, time data cannot be written or read. To time counter, 1 Hz is input.  The interval time of the interval timer output is 1/64. However, the "L" time of the pulse is unchanged from 30.5 μs.

[MEMO]

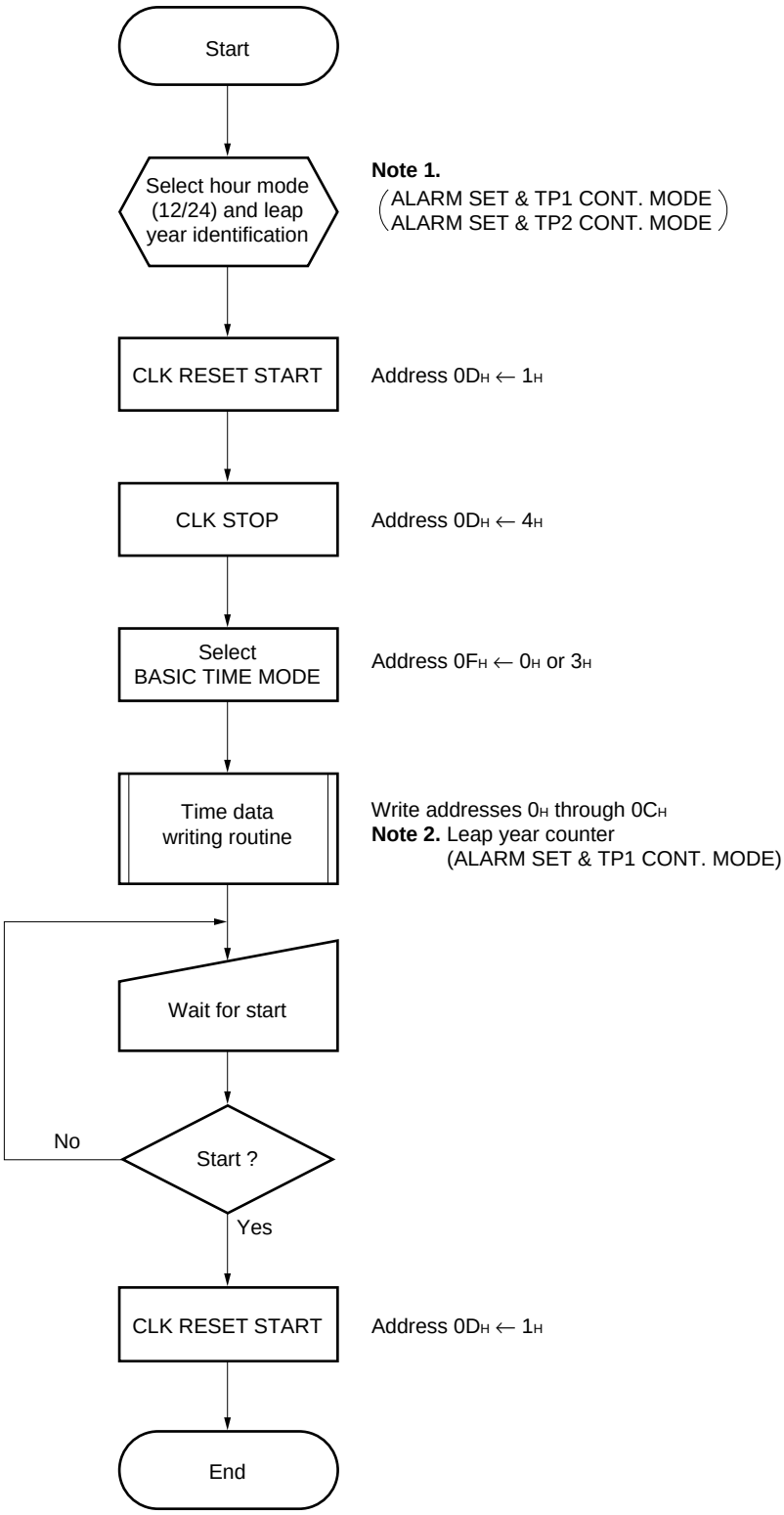
CHAPTER 3 ACCESS PROCEDURE

3.1 Writing and Reading Time

3.1.1 Setting time

Because the time counter is updated in real-time, the wrong value may be written to it if a carry occurs while data is being written to the time counter. To set the time, therefore, stop the clock supplied to the time counter. Figure 3-1 shows a flowchart illustrating the procedure for setting the time.

Figure 3-1. Setting Time



Notes 1. Once the 12- or 24-hour mode and leap year identification function have been selected, they do not have to be set again.

2. The user does not have to set the leap year counter if the lower 2 digits of the year are written to the counter.

3.1.2 Reading time

Because the time counter is updated every second, the wrong time data may be read if the time counter is read when a carry occurs. In principle, the time counter can be read in the following three ways.

<1> Use the BUSY flag, which is the count flag.

<2> Keep a carry from occurring while the time counter is read by using the CLK WAIT/CLK START command.

<3> Read the time counter two times and, only when the two values coincide, take that value as true.

(1) Using BUSY signal to interrupt CPU

The falling edge or rising edge of the BUSY signal is used to interrupt the CPU so that the time counter is read by the CPU every second.

If the CPU reads the time data of the μPD4991A in 457.7 μs after the interrupt has occurred, use the falling edge of the BUSY signal. If the CPU takes 457.7 μs or longer to read the data, use the rising edge. The BUSY signal is output to TP1 or TP2.

Figure 3-2. Using BUSY Signal for Interrupt

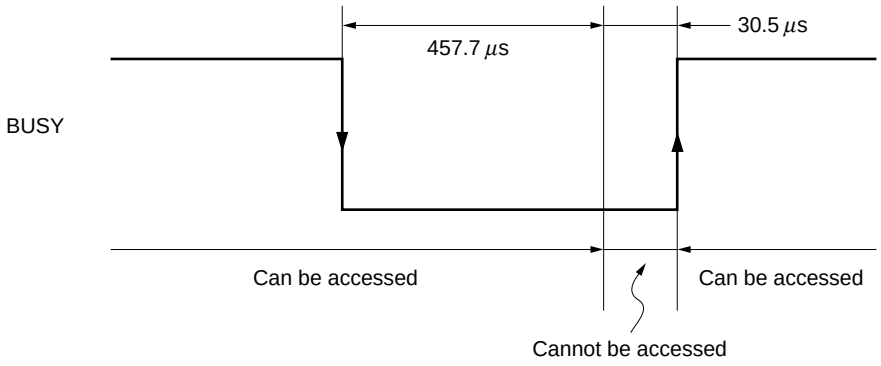
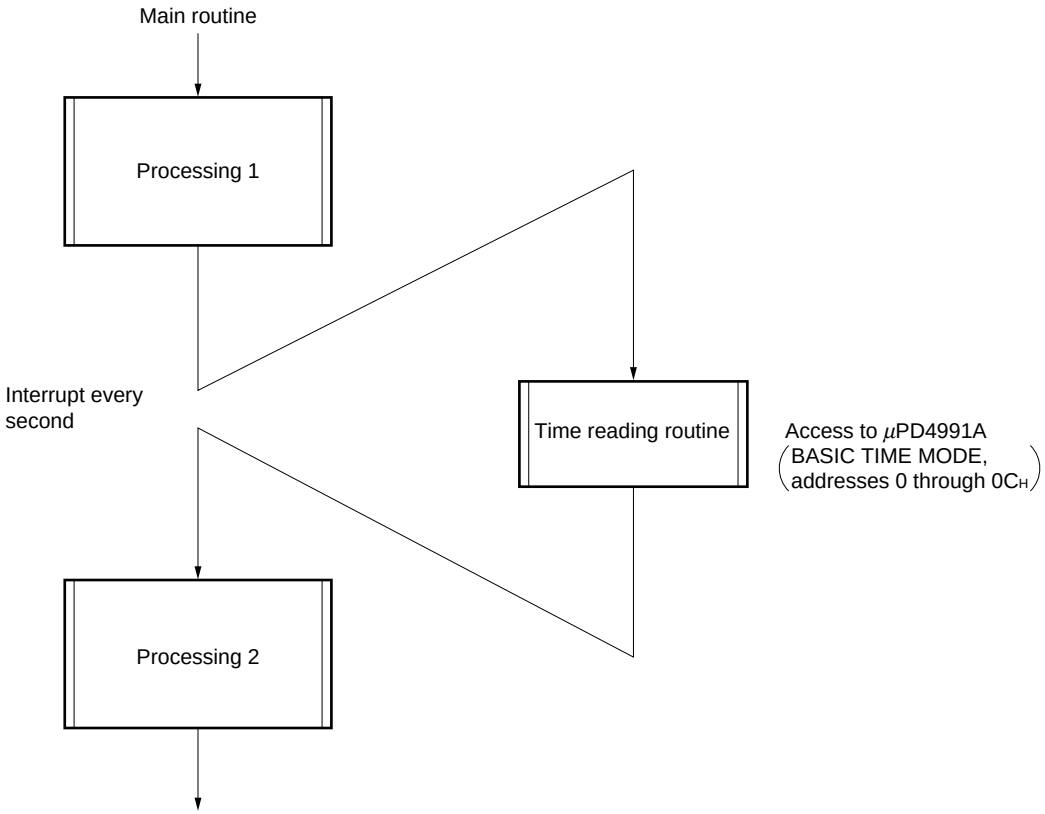


Figure 3-3. Reading Time by Using BUSY Signal for Interrupt

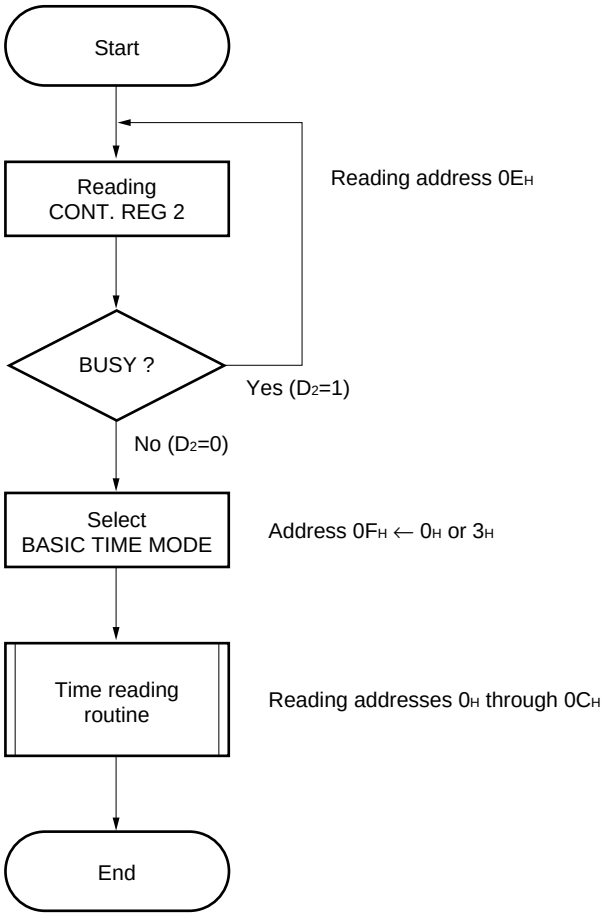


(2) Polling BUSY FLAG

In addition to outputting the BUSY signal to TP1 or TP2 as an interrupt signal, the time data can also be read by polling a high-order bit (D_2) of the CONTROL REGISTER 2 (address $0E_H$), which serves as a BUSY FLAG, before reading the time data. In this case, the data can be read only when the CONTROL REGISTER 2 is (D_3, D_2, D_1, D_0) = (x, 0, x, x). When the BUSY FLAG is "1", there is a possibility that a carry will occur from the time counter. Delay reading the time until the BUSY FLAG is cleared to "0".

Figure 3-4 shows this procedure.

Figure 3-4. Reading Time with BUSY FLAG



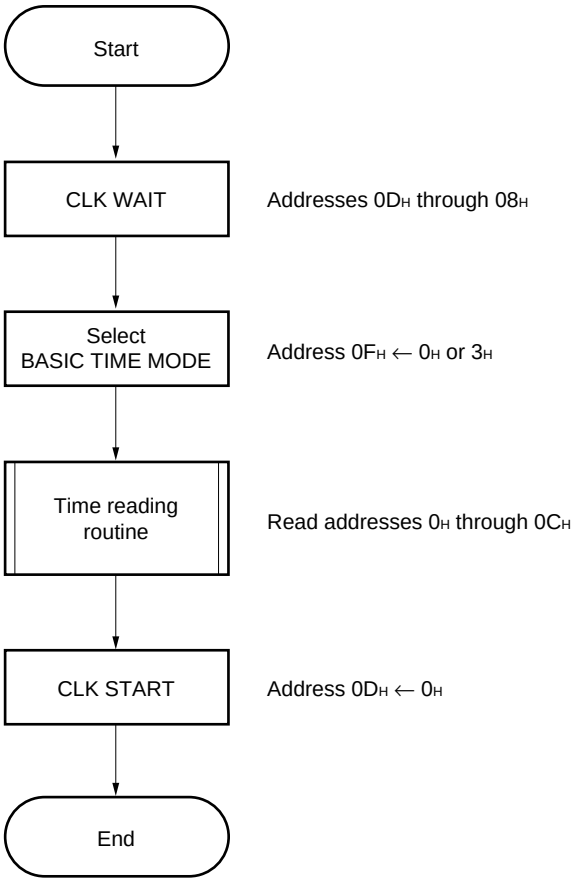
(3) Using CLK WAIT/CLK START command

By using the CLK control command of the CONTROL REGISTER 1, disable the carry from occurring while the time data is read.

Time is not delayed if the CLK START command is issued **within 0.5 seconds** after the CLK WAIT command is issued. Figure 3-5 shows this procedure.

This method is supported only by the μPD4991A in NEC's real-time clock IC series.

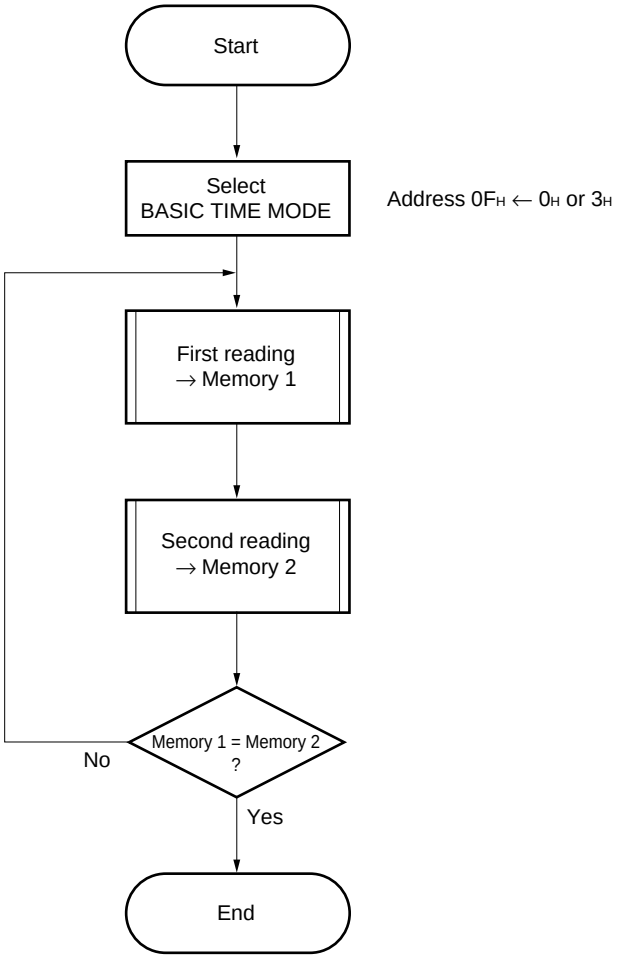
Figure 3-5. Reading Time with CLK WAIT/CLK START



(4) Reading two times

Read the time data two times. If the two values coincide, take that value as the correct value. This procedure is shown in Figure 3-6.

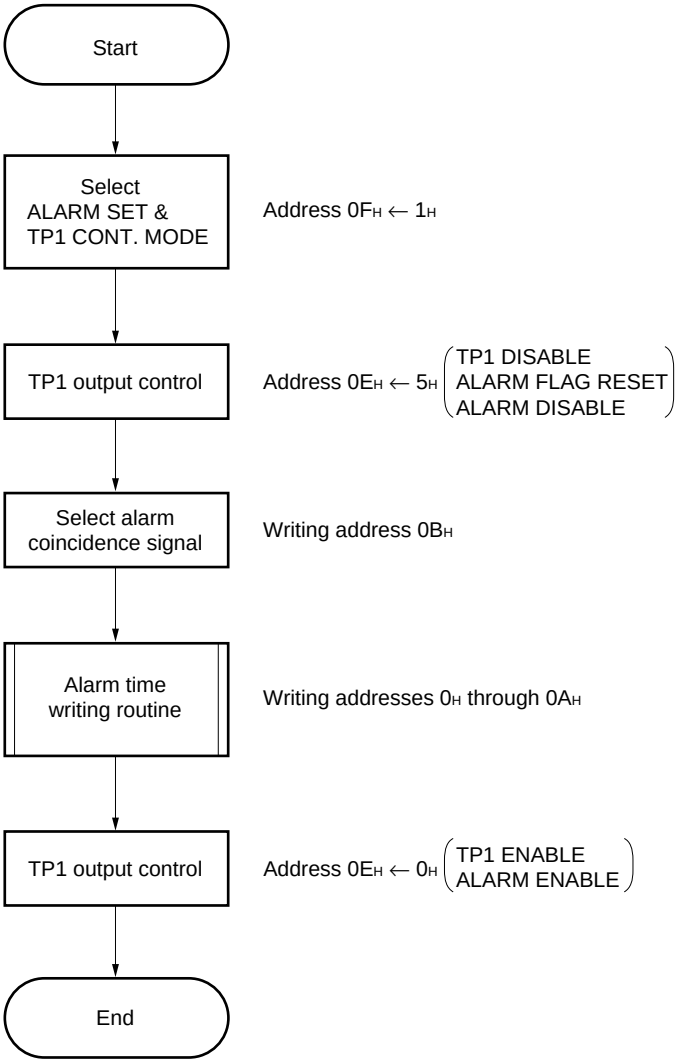
Figure 3-6. Reading Time Two Times



3.2 Setting Alarm Time

The alarm register can be rewritten at any time because it is independent of the time counter.
Figure 3-7 shows the procedure for rewriting the alarm register.

Figure 3-7. Setting Alarm Time



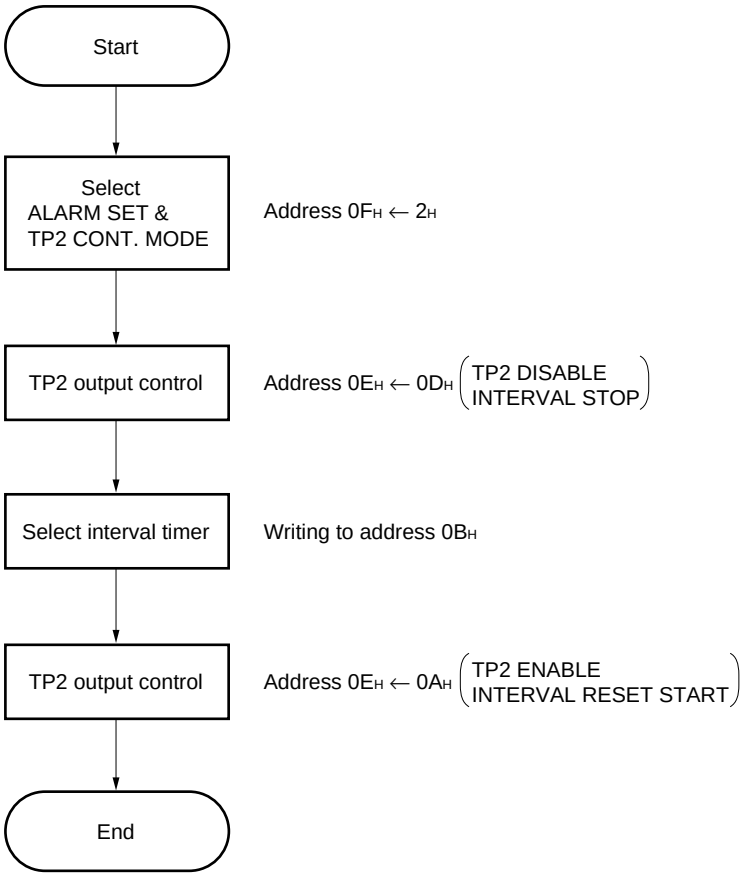
The alarm coincidence signal does not have to be selected every time unless the alarm coincidence signal is changed.

3.3 Setting Interval Timer

Because the interval timer is independent of the time counter, it can be stopped, resumed, or reset irrespective of the time counter operation. In the BASIC TIME MODE (MODE REG. ← 3_H), however, an error occurs in the interval timer if the CLOCK RESET command is executed. To execute this command, therefore, use the BASIC TIME MODE (MODE REG. ← 0_H) (for details, refer to **2.3.1 BASIC TIME MODE**).

Figure 3-8 shows the procedure of setting the interval timer.

Figure 3-8. Setting Interval Timer



The interval timer does not have to be selected every time unless the interval signal is changed.

[MEMO]

CHAPTER 4 ELECTRICAL SPECIFICATIONS AND INTERFACE

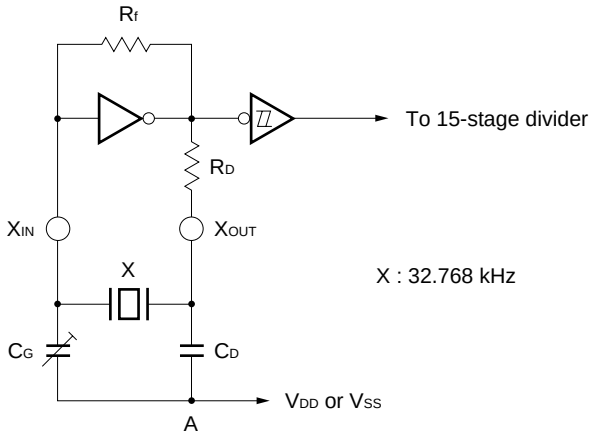
4.1 Crystal Oscillation Circuit

The μPD4991A has an oscillation circuit consisting of one CMOS inverter stage, feedback resistor R_f, and oscillation stabilization resistor R_D.

Figure 4-1 shows the equivalent circuit. The oscillation frequency is determined by external load capacitances C_G and C_D, and crystal resonator.

Because X_{IN} and X_{OUT} has stray capacitance in addition to C_G and C_D, either C_G or C_D must be adjusted (whichever it may be).

Figure 4-1. Crystal Oscillation Circuit of μPD4991A



Connect point A in Figure 4-1 to V_{DD} or V_{SS} of the μPD4991A. Whether it is connected to V_{DD} or V_{SS} does not make much difference in terms of characteristics.

Keep the wiring of the crystal resonator as short as possible. If the wiring length is too long, oscillation may be unstable, and the accuracy of the watch may be affected by external noise.

4.2 Oscillation Characteristics and Accuracy

The accuracy of the watch is always determined by the accuracy of the oscillation frequency. If the oscillation frequency changes by 100 ppm from 32.768 kHz, the watch accuracy is accordingly changed by 100 ppm. The oscillation frequency changes with the load capacitance, temperature, and supply voltage.

The dependencies of the oscillation frequency on these parameters are explained below.

4.2.1 Dependency on capacitance

Figure 4-3 shows the dependency of oscillation frequency f of on load capacitance C_G (which is measured with 2048 Hz output to TP1) where C_D = 20 pF, T_A = 25 °C, and V_{DD} = 5 V in the test circuit shown in Figure 4-2.

If C_G and C_D are too high (50 pF or more), the oscillation characteristics are degraded at a low voltage. Note that Figure 4-3 is only for reference, and that the characteristics vary depending on the crystal resonator used and the stray capacitance of the board.

Figure 4-2. Test Circuit for Dependency on Capacitance

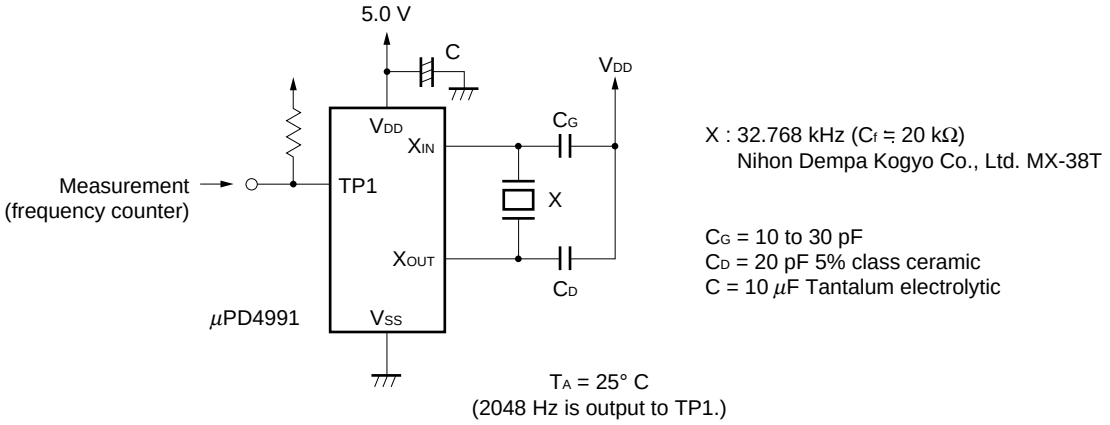
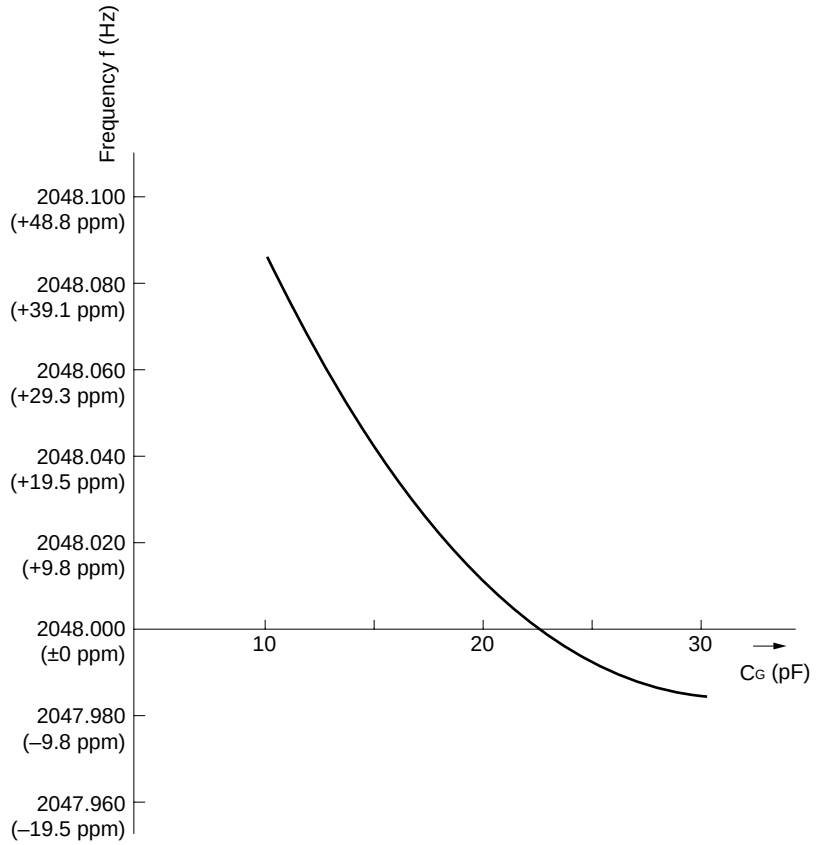


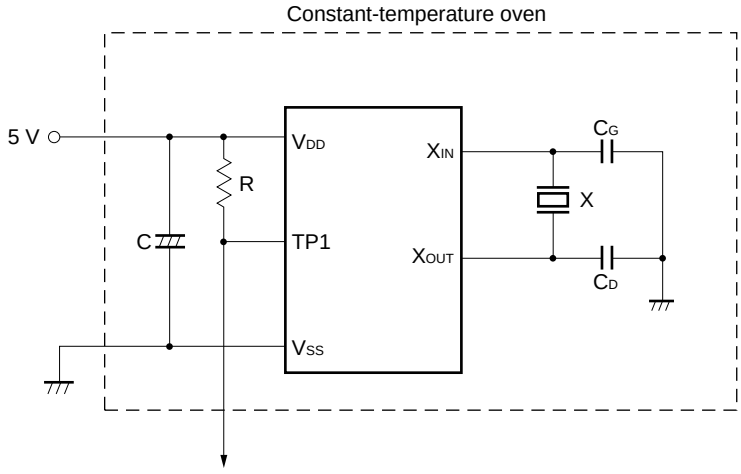
Figure 4-3. Oscillation Frequency f vs. Load Capacitance C_G



4.2.2 Dependency on temperature

The oscillation frequency heavily fluctuates with temperature as shown in Figure 4-5. The temperature characteristics show a negative quadratic curve peaking at around 25 °C. These characteristics are of a tuning fork crystal resonator.

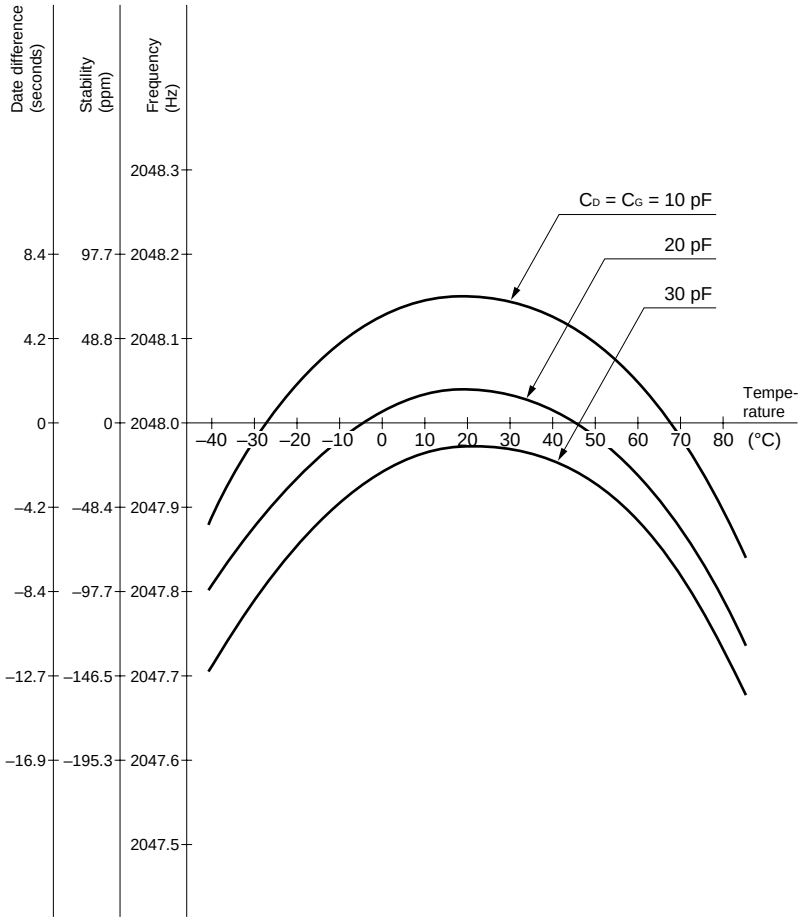
Figure 4-4. Test Circuit for Dependency on Temperature



X : 32.768 kHz ($C_f \fallingdotseq$ 20 kΩ)
Nihon Dempa Kogyo Co., Ltd. MX-38T

C = 10 μF Tantalum electrolytic

Figure 4-5. Oscillation Frequency f vs. Ambient Temperature T_A

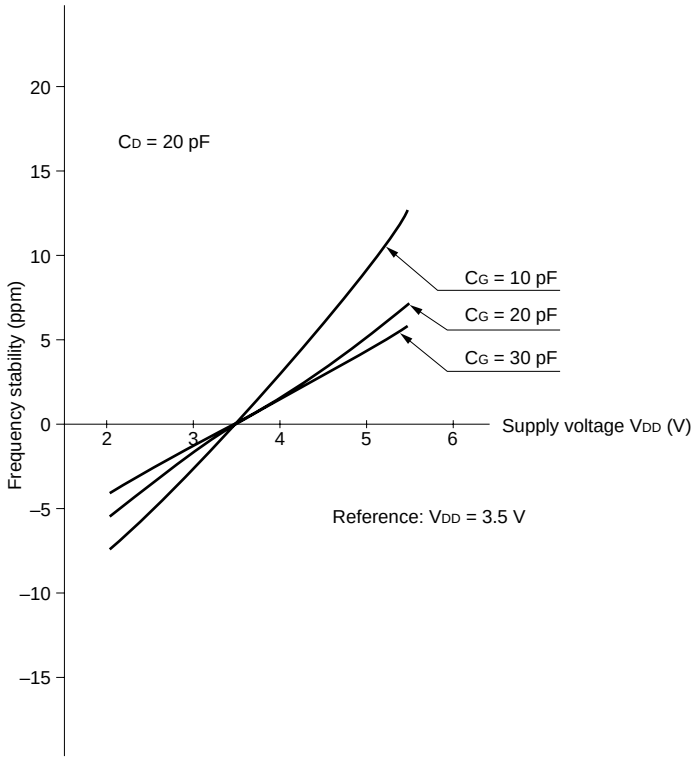


4.2.3 Dependency on supply voltage

The oscillation characteristics also vary with supply voltage V_{DD}. The closer the supply voltage for back up is to the voltage for access, the higher the watch accuracy.

The higher C_G and C_D, the better the dependency on the supply voltage, but the worse the oscillation characteristics at a low voltage (oscillation start voltage and oscillation maintain voltage).

Figure 4-6. Oscillation Frequency f vs. Supply Voltage V_{DD}



4.3 Adjusting Oscillation Frequency

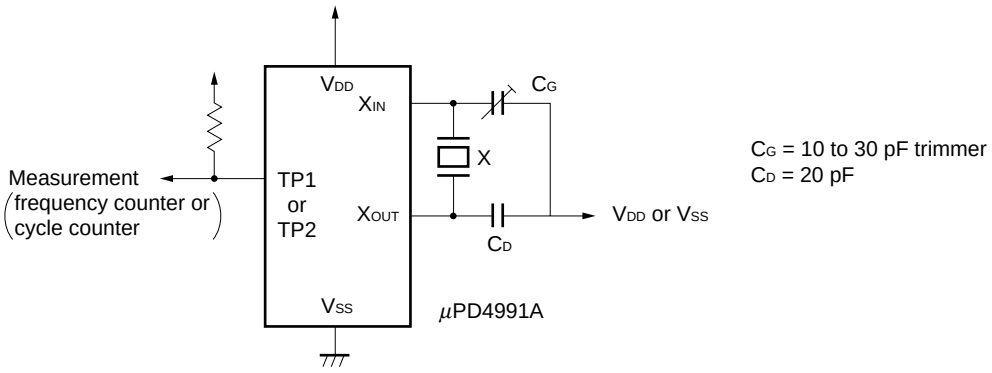
The accuracy of the watch depends on the stability of the oscillation frequency. In the actual operating conditions, however, it is mostly determined by the accuracy of adjustment of the oscillation frequency. To improve the accuracy, therefore, adjustment is essential.

C_G or C_D is used as a trimmer capacitor. To make an adjustment, the alarm coincidence signal is output to TP1 or the interval signal is output to TP2. While this signal is measured with a frequency counter or cycle counter, adjust the trimmer capacitor so that the frequency reaches the specified value or that the specified cycle is reached.

Be sure to use TP1 or TP2 for measurement.

If a test probe touches X_{IN} or X_{OUT}, oscillation may be stopped or the oscillation frequency may change because of the capacitance of the probe, making correct measurement impossible.

Figure 4-7. Adjusting Oscillation Frequency



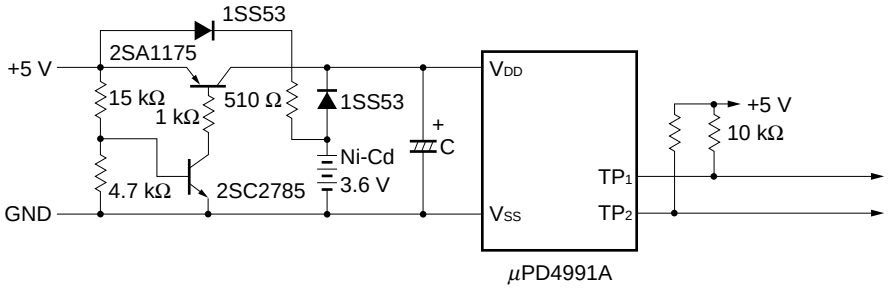
Caution Because the interval timer does not output an accurate 0.1-second interval signal, this signal should not be used for adjusting the oscillation frequency.

To output 2048 Hz to TP1, for example, the counter must be able to read 2048.00±0.02 Hz to ensure an adjustment accuracy of ±10 ppm. Similarly, when the 1-second interval signal is output to TP2, 1.000 00±0.000 01 sec. must be directly read.

4.4 Back-up Circuit

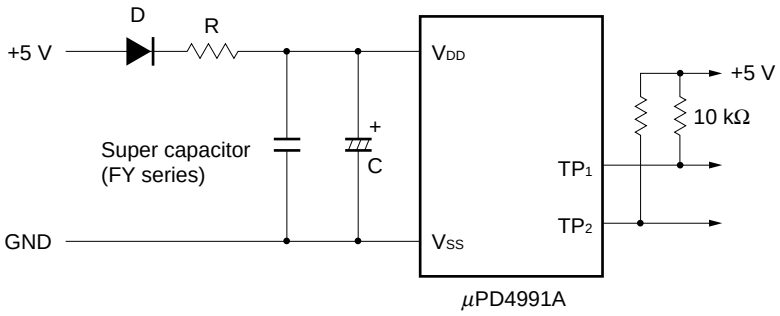
Because the μPD4991A is a CMOS IC, it can provide a back-up operation with a low-voltage battery. Figure 4-8 shows an example of using a Ni-Cd battery for back-up, and Figure 4-9 shows an example of using a super capacitor (high-capacitance, electric double-layer capacitor).

Figure 4-8. Example of Back-up Circuit Using Ni-Cd Battery



C: Supply voltage stabilization capacitor
(1 to 10 μF)
Tantalum electrolytic, etc.

Figure 4-9. Example of Back-up Circuit Using Super Capacitor



C: Supply voltage stabilization capacitor
(1 to 10 μF)
Tantalum electrolytic, etc.
R: For inrush current prevention
(depends on current capacity of +5 V)
D: Shottky barrier diode
($V_F \leq 0.3$ V)

If a 1.0-F super capacitor (such as FY0Z105) is used, the μPD4991A can be backed up for several days.

4.5 Power-fail Circuit

While the μPD4991A is backed up, the CS_2 pin must be fixed to low to inhibit access from an external device.

The power-fail circuit fixes CS_2 to low when the voltage of the +5-V power supply drops below the operating voltage of the CPU (for example, 4.5 V or lower), and must keep CS_2 low until the CPU starts operating again (refer to **Figure 4-10**).

Figure 4-11 shows a simple power-fail circuit that consists of a Zener diode and transistors. Figure 4-12 shows an example where the μPC2260V power IC with reset function is used.

Figure 4-10. Back-up Status and CS_2 Pin Voltage

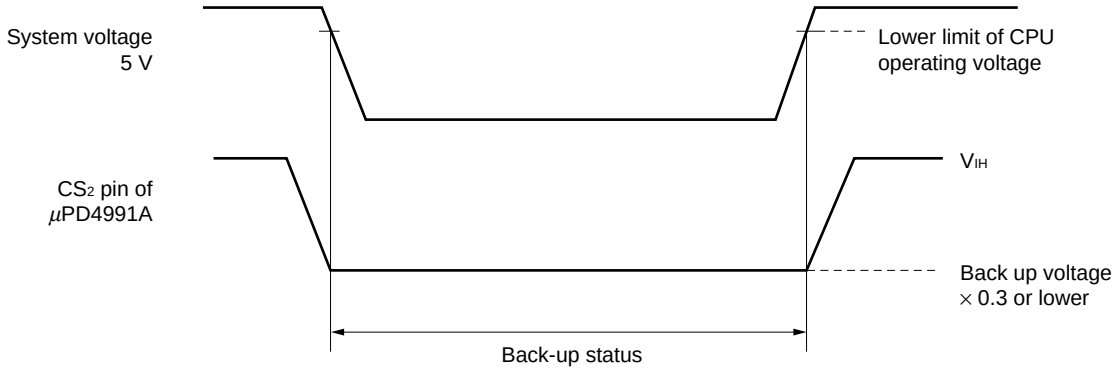


Figure 4-11. Power-Fail Circuit (Simple type)

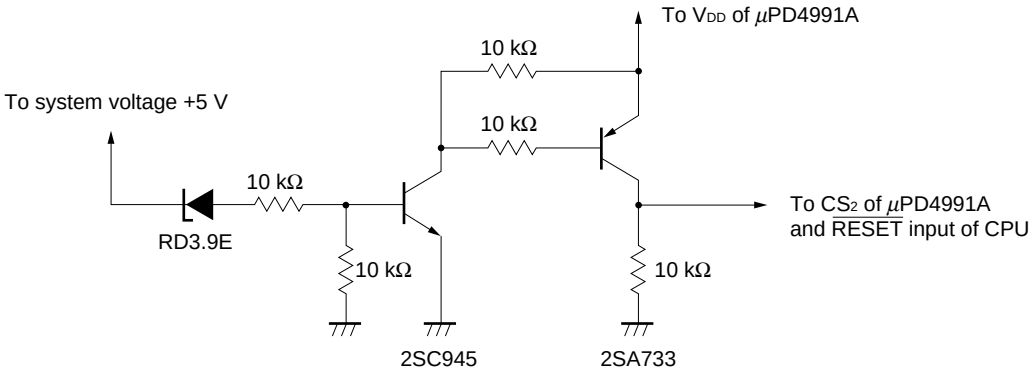
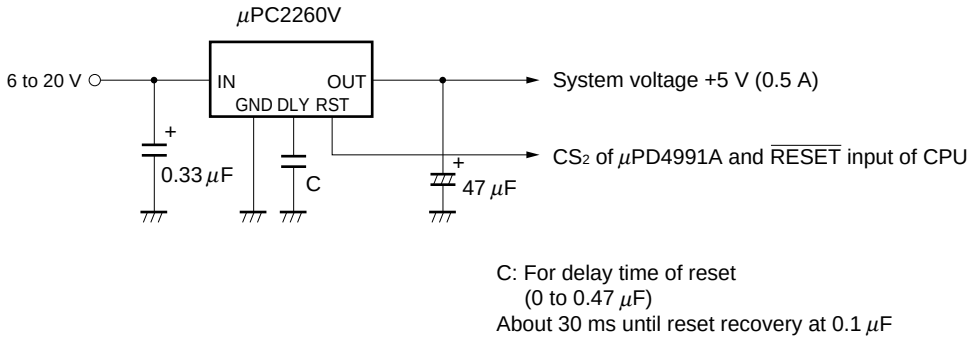


Figure 4-12. Power-Fail Circuit (with μPC2260V)



C: For delay time of reset
(0 to 0.47 μF)
About 30 ms until reset recovery at 0.1 μF

When the μPC2260V is used, the power supply circuit and power-fail circuit of the system can be simplified, contributing to miniaturization and cost reduction.

[MEMO]

APPENDIX

Appendix 1. Specifications of μPD4991A

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output pin voltage	V_{OUT}	7.0	V
Low-level output current (N-ch open drain)	I_{OUT}	30	mA
Operating temperature range	T_A	–40 to +85	°C
Storage temperature range	T_{stg}	–65 to +125	°C

Electrical Specifications (V_{SS} = 0 V, f = 32.768 kHz, C_G = C_D = 20 pF, Ci = 20 kΩ, T_A = –40 to +85 °C)

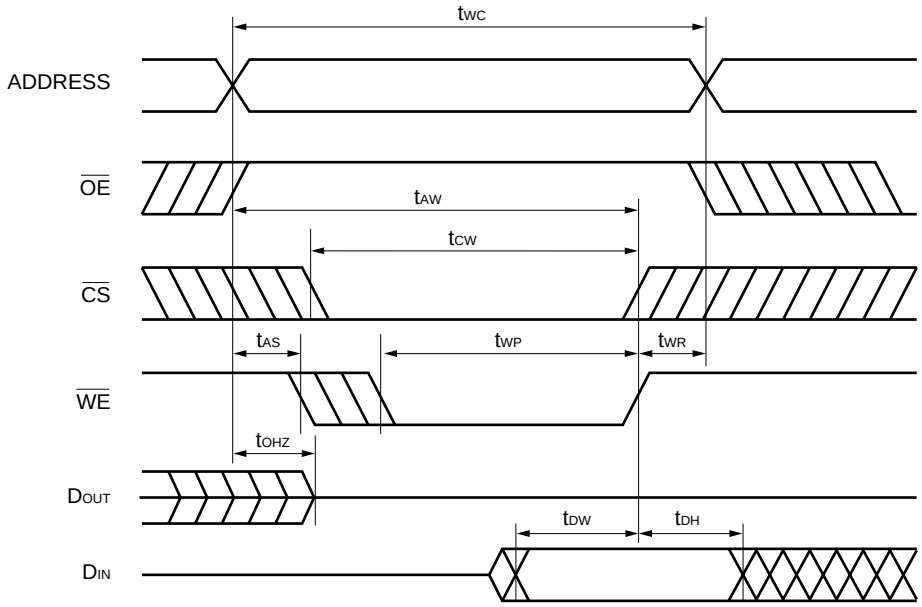
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage range	V_{DD}		2.0		5.5	V
High-level input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}		V_{SS}		0.3 V_{DD}	V
Current consumption	I_{DD}	V_{DD} = 3.6 V, V_{IN} = V_{SS}, T_A = –40 to 70 °C		5	14	μA
Current consumption	I_{DD}	V_{DD} = 2.4 V, V_{IN} = V_{SS}, T_A = –40 to 70 °C		2	6	μA
High-level input leakage current	I_{LIH}	V_{DD} = 5.5 V, V_{IN} = V_{DD}			+1.0	μA
Low-level input leakage current	I_{LIL}	V_{DD} = 5.5 V, V_{IN} = V_{SS}			–1.0	μA
High-level output voltage	V_{OH}	I_{OH} = –1.0 mA	2.4			V
Low-level output voltage	V_{OL1}	I_{OL} = 2.0 mA			0.4	V
Low-level output voltage	V_{OL2}	I_{OL} = 1.0 mA (Nch Open Drain)			0.4	V
High-level leakage current	I_{LOH}	TP_{out} = V_{DD} (Nch Open Drain)			1.0	μA

AC Characteristics

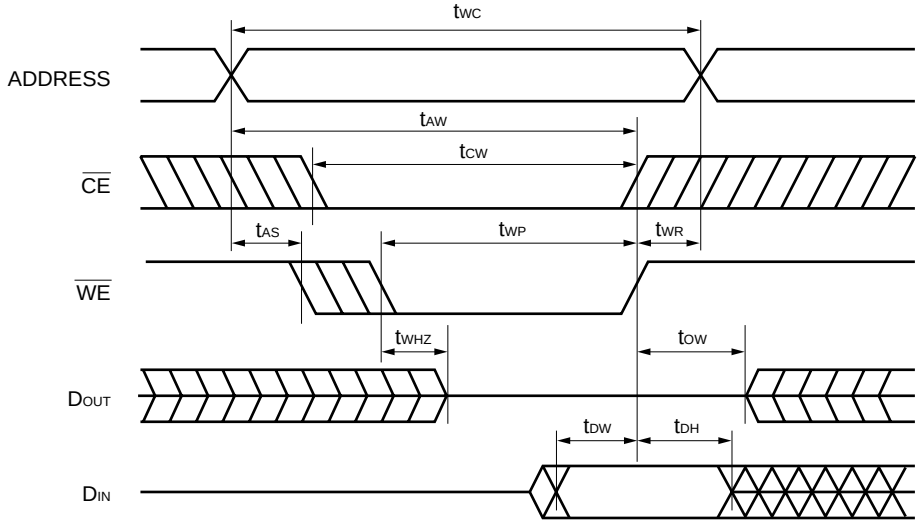
Write cycle (Unless otherwise specified, V_{DD} = 5 V±10%, T_A = –40 to +85 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cycle time	t_{WC}		150			ns
$\overline{CS}$ - $\overline{WE}$ reset time	t_{CW}		120			
Address - $\overline{WE}$ reset time	t_{AW}		120			
Address - $\overline{WE}$ setup time	t_{AS}		0			
Write pulse width	t_{WP}		90			
Address hold time	t_{WR}		20			
Input data setup time	t_{DW}		50			
Input data hold time	t_{DH}		0			
$\overline{WE}$ - output floating time	t_{WHZ}				50	

Write cycle timing 1



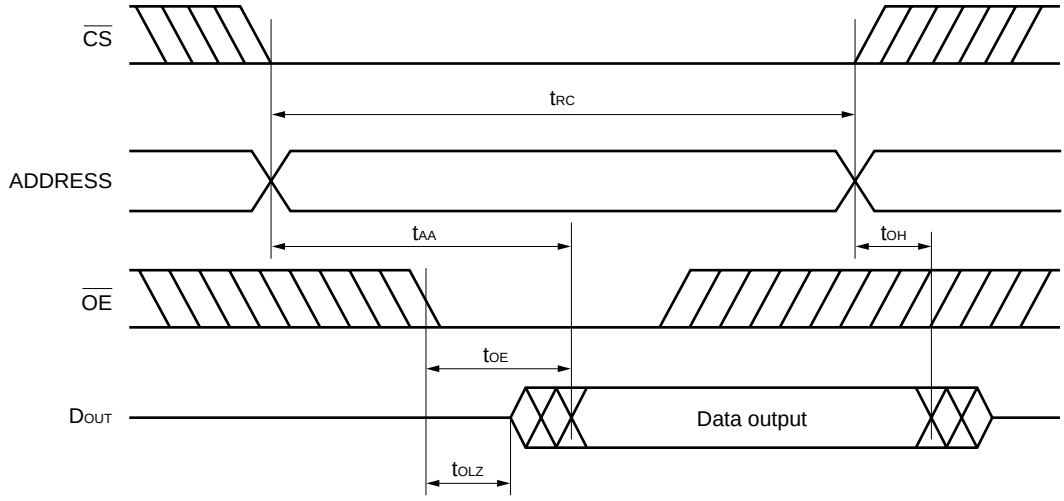
Write cycle timing 2 ($\overline{OE}$ = V_{IL})



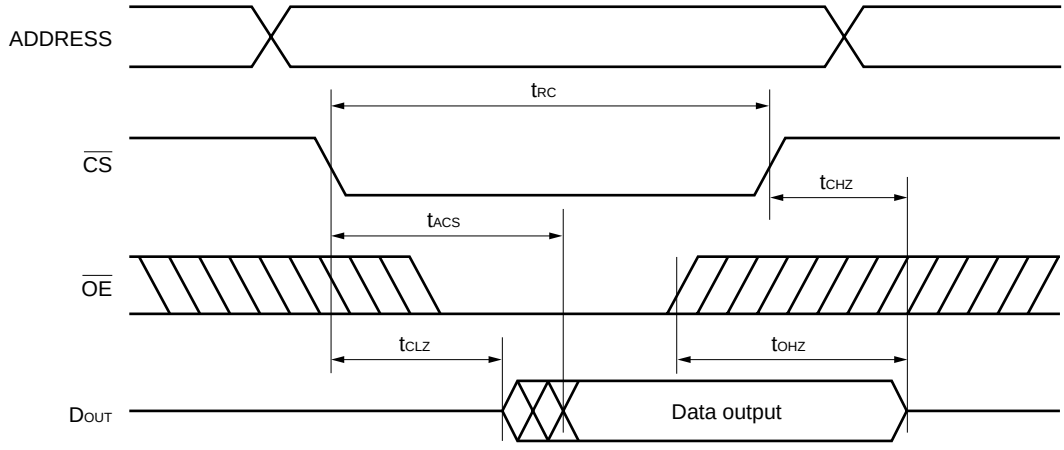
Read cycle (Unless otherwise specified, V_{DD} = 5 V±10%, T_A = –40 to +85 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}		150			ns
Address access time	t_{AA}				150	
$\overline{CS}$ - access time	t_{ACS}				150	
$\overline{OE}$ - output delay time	t_{OE}				75	
$\overline{OE}$ - output delay time	t_{OLZ}		5			
$\overline{OE}$ - output delay time	t_{OHZ}				50	
Output hold time	t_{OH}		15			
$\overline{CS}$ - output setup time	t_{CLZ}		10			
$\overline{CS}$ - output floating time	t_{CHZ}		5			

Read cycle timing 1

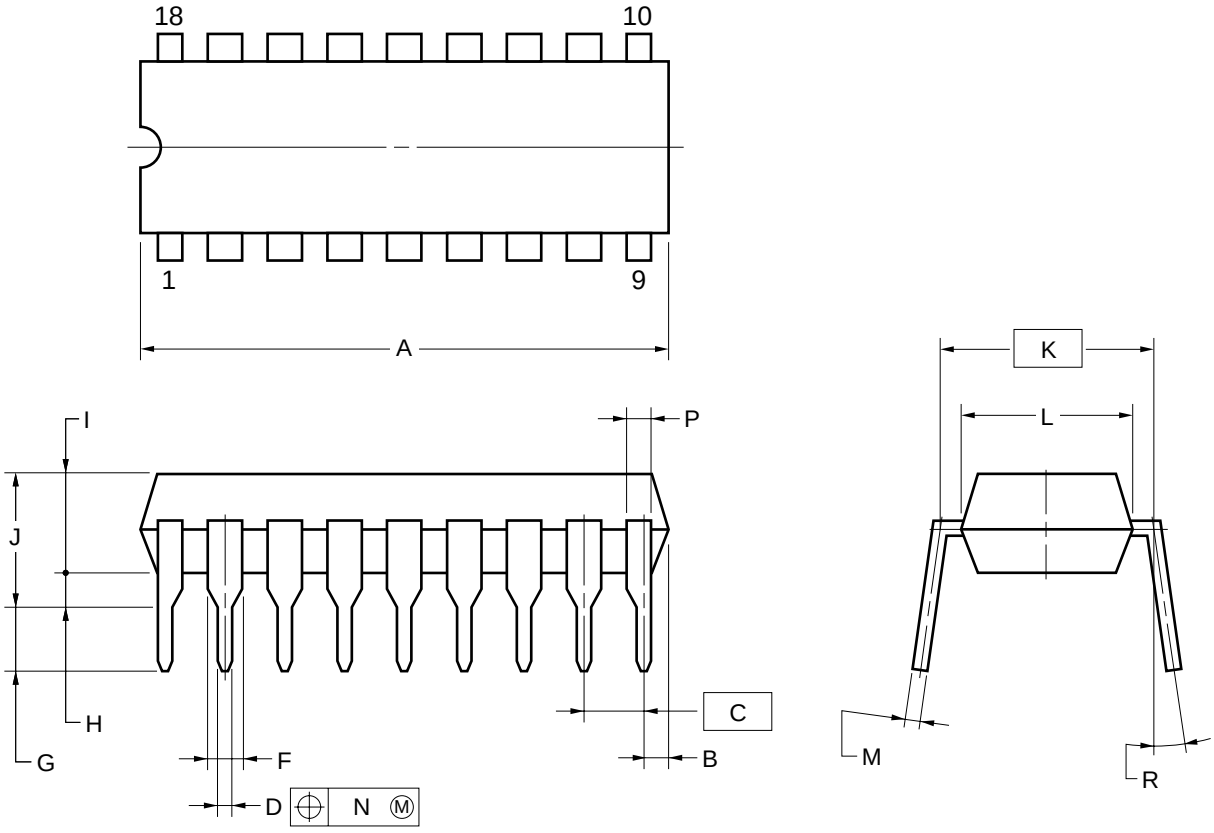


Read cycle timing 2



Appendix 2. Package Drawing

18PIN PLASTIC DIP (300 mil)



NOTES

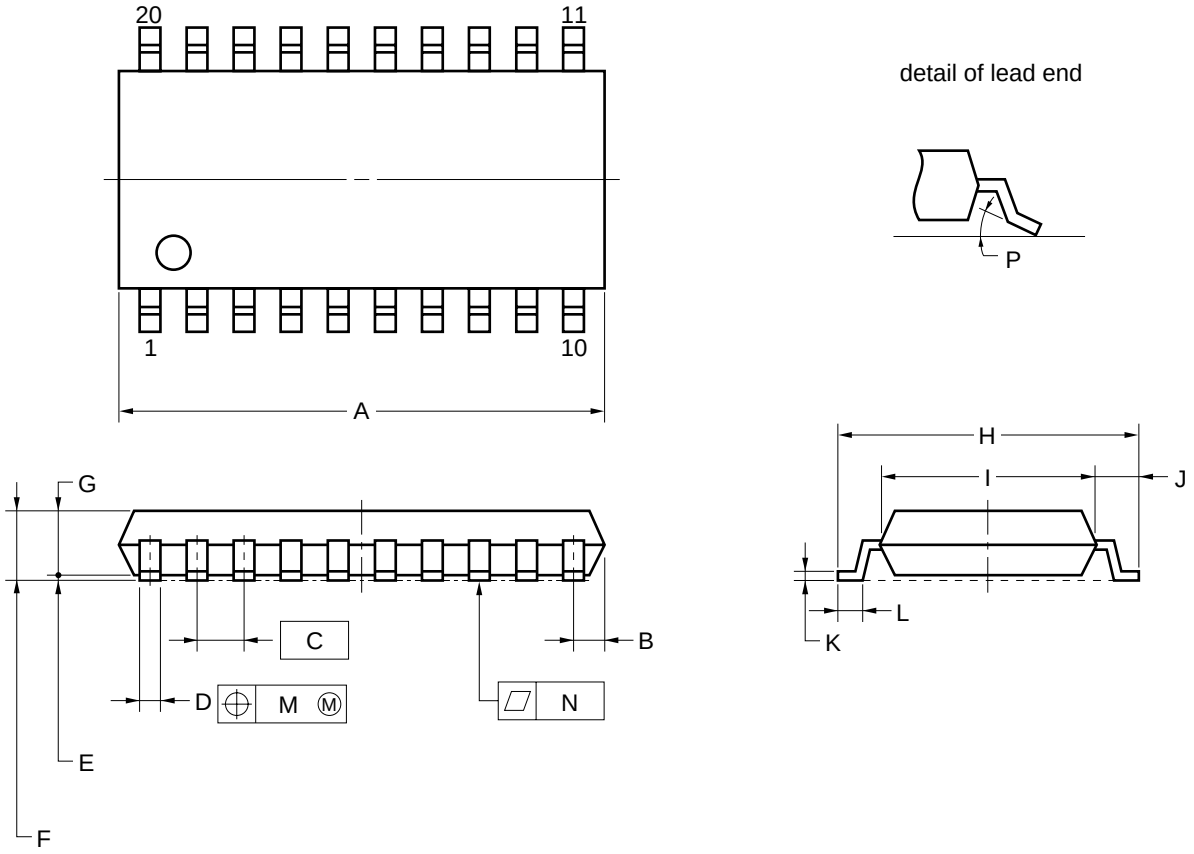
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.900 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.5 ± 0.3	0.138 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.
R	0~15°	0~15°

P18C-100-300A,C-1

20 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	12.7±0.3	0.500±0.012
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55±0.05	0.061±0.002
H	7.7±0.3	0.303±0.012
I	5.6±0.2	$0.220^{+0.009}_{-0.008}$
J	1.1	0.043
K	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P20GM-50-300B, C-5

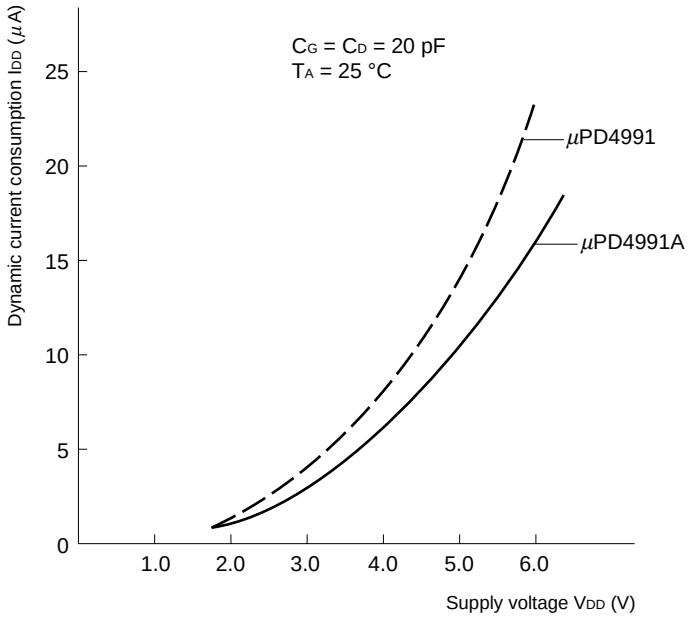
Appendix 3. Differences between μPD4991 and μPD4991A

The μPD4991A improves the characteristics of the μPD4991. The differences between the two are as follows:

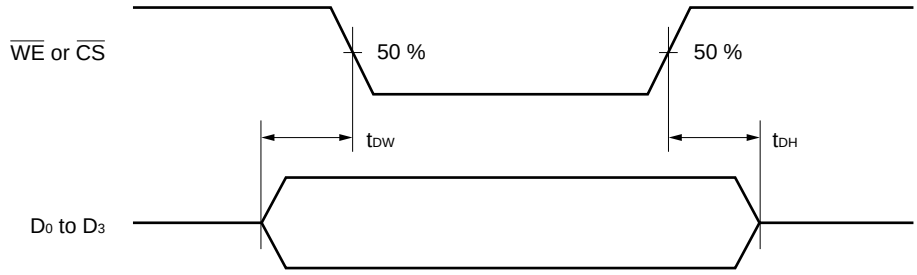
1. Specifications

Parameter	Symbol	μPD4991	μPD4991A	Remark
Current consumption	I_{DD}	20 μA MAX.	14 μA MAX.	V_{DD} = 3.6 V
Current consumption	I_{DD}	15 μA MAX.	—	V_{DD} = 3.0 V
Current consumption	I_{DD}	—	6 μA MAX.	V_{DD} = 2.4 V
Input data setup time	t_{DW}	0 ns MIN.	50 ns MIN.	Specification differs
Input data hold time	t_{DH}	0 ns MIN.	0 ns MIN.	Specification differs

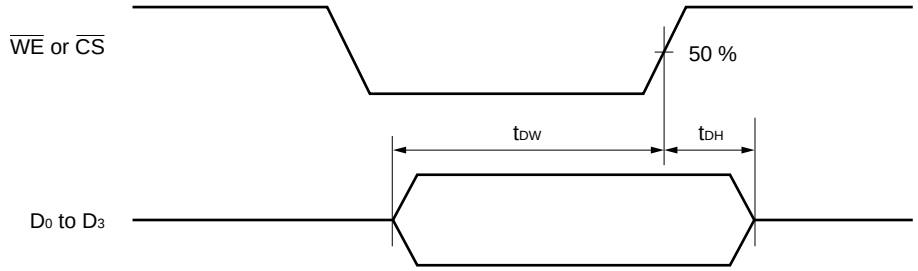
Dynamic Current Consumption



AC Timing Specification of μPD4991



AC Timing Specification of μPD4991A



2. Function

Parameter	μPD4991	μPD4991A
Valid range of ±30 s ADJUST	Units digit of second to units digit of minute (no carry to tens digit of minute)	All digits
BUSY flag on execution of ±30 s ADJUST flag	Not BUSY	BUSY until carry occurs from all digits
D_3 bit of CONTROL REGISTER 1	NOP	CLOCK WAIT

CLOCK WAIT and CLOCK STOP bits

Both these bits inhibit input of the clock (1 Hz) to the watch counter and stop the watch. The CLOCK STOP bit is used to set time of the watch (be sure to stop the watch when setting the time).

The CLOCK WAIT bit is used to prevent the CPU from reading the wrong data when a count is generated while the time is being read (the time is read by using the BUSY signal or by reading it two times, without using the CLOCK WAIT).

Even after the watch has been stopped by CLOCK STOP or CLOCK WAIT, the real time is not delayed if CLOCK RUN is executed within 0.5 second.

[MEMO]

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