



LOW SKEW, $\div 1/\div 2$ DIFFERENTIAL-TO-3.3V LVPECL FANOUT BUFFER

IDT8737-11

FEATURES:

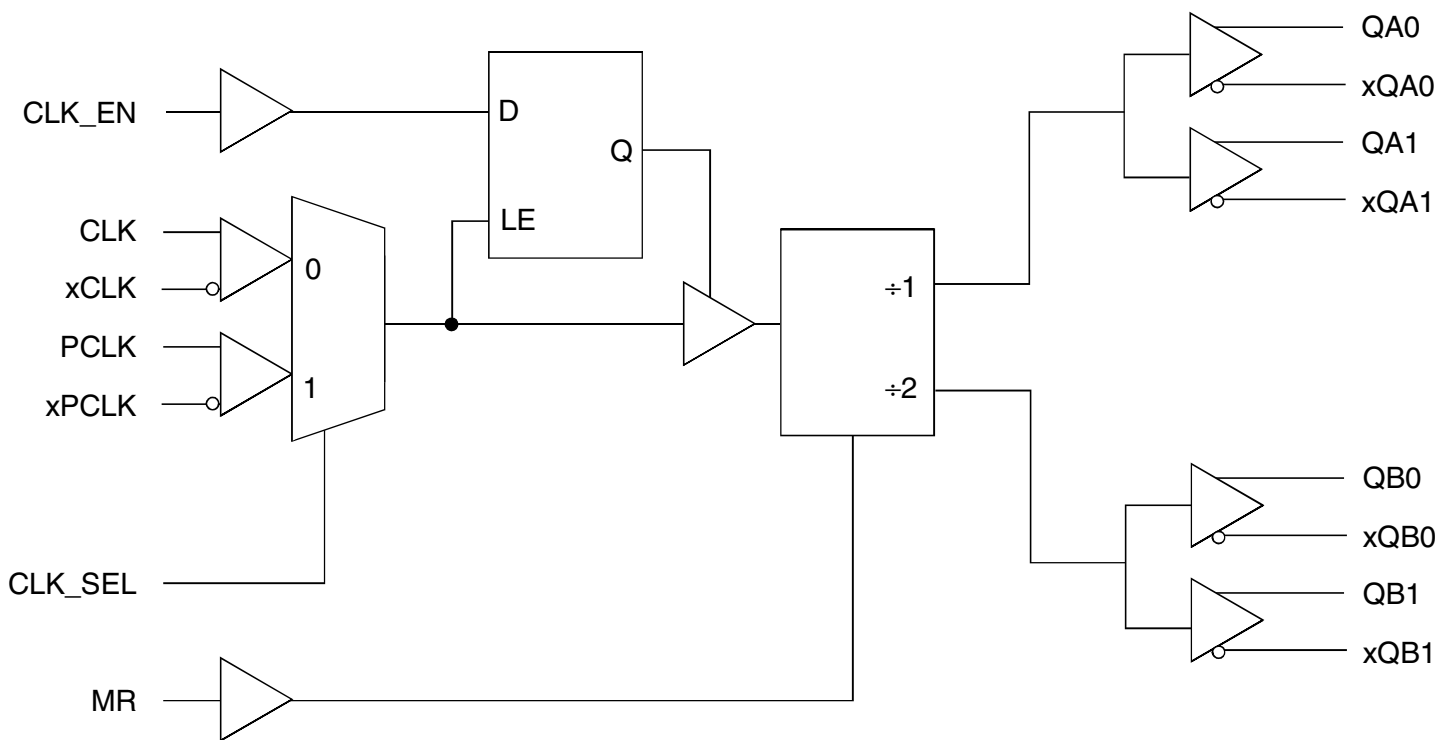
- Two divide-by-1 and two divide-by-2 differential 3.3V LVPECL outputs
- Selectable differential CLK, xCLK, or LVPECL clock inputs
- CLK, xCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, and HCSL
- PCLK, xPCLK supports the following input types: LVPECL, CML, and SSTL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal (LVCMOS, LVTTTL, GTL) to LVPECL levels with resistor bias on xCLK input
- Output skew: 60ps (max.)
- Part-to-part skew: as low as 200ps
- Bank skew:
 - Bank A, as low as 20ps
 - Bank B, as low as 35ps
- Propagation delay: 1.7ns (max.)
- 3.3V operating supply
- Available in TSSOP package

DESCRIPTION:

The IDT8737-11 is a low skew, high performance differential-to-3.3V LVPECL fanout buffer-divider. It has two selectable clock inputs. The CLK/xCLK pair can accept most standard differential input levels. The PCLK/xPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the IDT8737-11 ideal for clock distribution applications that demand well-defined performance and repeatability.

FUNCTIONAL BLOCK DIAGRAM

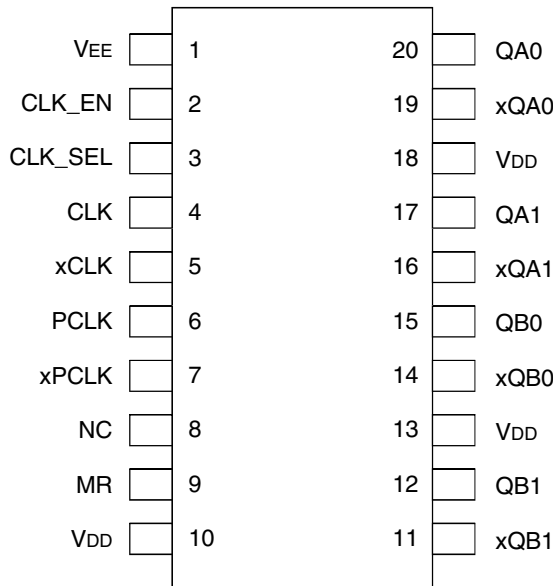


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COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

FEBRUARY 2009

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{DD}	Power Supply Voltage	4.6	V
V _I	Input Voltage	-0.5 to V _{DD} +0.5	V
V _O	Output Voltage	-0.5 to V _{DD} +0.5	V
θ _{JA}	Package Thermal Impedance (0lfpm)	92.6	°C/W
T _{STG}	Storage Temperature	-65 to +150	°C

NOTE:

1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Typ.	Max.	Unit
C _{IN}	Input Capacitance	—	4	pF
R _{PULLUP}	Input Pullup Resistor	51	—	KΩ
R _{PULLDOWN}	Input Pulldown Resistor	51	—	KΩ

PIN DESCRIPTION⁽¹⁾

Symbol	Number	Type	Description
VEE	1	Power	Negative Supply Pin
CLK_EN	2	Input Pullup	Synchronizing Clock Enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced LOW, xQ outputs are forced HIGH. LVTTTL / LVCMOS interface levels.
CLK_SEL	3	Input Pulldown	Clock Select Input. When HIGH, selects PCLK / xPCLK inputs. When LOW, selects CLK / xCLK inputs. LVTTTL / LVCMOS interface levels.
CLK	4	Input Pulldown	Non-Inverting Differential Clock Input
xCLK	5	Input Pullup	Inverting Differential Clock Input
PCLK	6	Input Pulldown	Non-Inverting Differential LVPECL Clock Input
xPCLK	7	Input Pullup	Inverting Differential LVPECL Clock Input
NC	8	Unused	No Connection
MR	9	Input Pulldown	Master Reset. Resets the output divider. LVTTTL / LVCMOS interface levels.
V _{DD}	10, 13, 18	Power	Positive Supply Pins
xQB1, QB1	11, 12	Output	Differential Output Pair. LVTTTL / LVCMOS interface levels.
xQB0, QB0	14, 15	Output	Differential Output Pair. LVTTTL / LVCMOS interface levels.
xQA1, QA1	16, 17	Output	Differential Output Pair. LVTTTL / LVCMOS interface levels.
xQA0, QA0	19, 20	Output	Differential Output Pair. LVTTTL / LVCMOS interface levels.

NOTE:

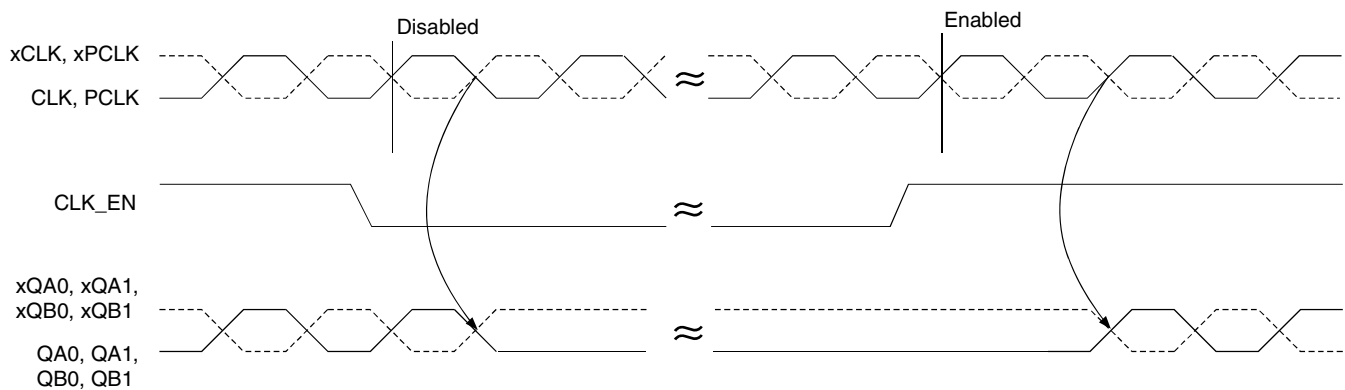
1. Pullup and Pulldown refer to internal input resistors. See Capacitance table for typical values.

CONTROL INPUT FUNCTION TABLE^(1,2)

Inputs				Outputs			
MR	CLK_EN	CLK_SEL	Selected Source	QA0, QA1	xQA0, xQA1	QB0, QB1	xQB0, xQB1
1	X	X	X	LOW	HIGH	LOW	HIGH
0	0	0	CLK, xCLK	Disabled; LOW	Disabled; HIGH	Disabled; LOW	Disabled; HIGH
0	0	1	PCLK, xPCLK	Disabled; LOW	Disabled; HIGH	Disabled; LOW	Disabled; HIGH
0	1	0	CLK, xCLK	Enabled	Enabled	Enabled	Enabled
0	1	1	PCLK, xPCLK	Enabled	Enabled	Enabled	Enabled

NOTES:

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in the CLK_EN Timing Diagram below.
2. In active mode, the state of the outputs is a function of the CLK / xCLK and PCLK / xPCLK inputs as described in the Clock Input Function table.



CLK_EN Timing Diagram

CLOCK INPUT FUNCTION TABLE⁽¹⁾

Inputs		Outputs				Input to Output Mode	Polarity
CLK or PCLK	xCLK or xPCLK	QAx	xQAx	QBx	xQBx		
0	1	L	H	L	H	Differential to Differential	Non-Inverting
1	0	H	L	H	L	Differential to Differential	Non-Inverting
0	Biased ⁽²⁾	L	H	L	H	Single-Ended to Differential	Non-Inverting
1	Biased ⁽²⁾	H	L	H	L	Single-Ended to Differential	Non-Inverting
Biased ⁽²⁾	1	L	H	L	H	Single-Ended to Differential	Inverting
Biased ⁽²⁾	0	H	L	H	L	Single-Ended to Differential	Inverting

NOTES:

1. H = HIGH
L = LOW
2. See Single-Ended Signal diagram under Application Information at the end of this datasheet.

POWER SUPPLY CHARACTERISTICS - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I _{EE}	Power Supply Current		—	—	50	mA

DC ELECTRICAL CHARACTERISTICS, LVCMOS / LVTTTL - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{IH}	CLK_EN, CLK_SEL, MR		2		V _{DD} + 0.3	V
V _{IL}	CLK_EN, CLK_SEL, MR		-0.3		0.8	V
I _{IH}	Input Current HIGH	CLK_EN	V _{IN} = V _{DD} = 3.465V		5	μA
		CLK_SEL, MR	V _{IN} = V _{DD} = 3.465V		150	
I _{IL}	Input Current LOW	CLK_EN	V _{IN} = 0V, V _{DD} = 3.465V	-150		μA
		CLK_SEL, MR	V _{IN} = 0V, V _{DD} = 3.465V	-5		

DC ELECTRICAL CHARACTERISTICS, DIFFERENTIAL - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{PP}	Peak-to-Peak Input Voltage		0.15		0.3	V
V _{CMR}	Common Mode Input Voltage ^(1,2)		V _{EE} + 0.5		V _{DD} - 0.85	V
I _{IH}	Input Current HIGH	xCLK	V _{IN} = V _{DD} = 3.465V		5	μA
		CLK	V _{IN} = V _{DD} = 3.465V		150	
I _{IL}	Input Current LOW	xCLK	V _{IN} = 0V, V _{DD} = 3.465V	-150		μA
		CLK	V _{IN} = 0V, V _{DD} = 3.465V	-5		

NOTES:

1. For single-ended applications, the max. input voltage for CLK / xCLK is V_{DD} + 0.3V.
2. Common mode voltage is defined as V_{IH}.

DC ELECTRICAL CHARACTERISTICS, LVPECL - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{IH}	Input Current HIGH	PCLK	V _{IN} = V _{DD} = 3.465V		5	μA
		xPCLK	V _{IN} = V _{DD} = 3.465V		150	
I _{IL}	Input Current LOW	PCLK	V _{IN} = 0V, V _{DD} = 3.465V	-150		μA
		xPCLK	V _{IN} = 0V, V _{DD} = 3.465V	-5		
V _{PP}	Peak-to-Peak Input Voltage		0.3		1	V
V _{CMR}	Common Mode Input Voltage ^(1,2)		V _{EE} + 1.5		V _{DD}	V
V _{OH}	Output Voltage HIGH ⁽³⁾		V _{DD} - 1.4		V _{DD} - 1	V
V _{OL}	Output Voltage LOW ⁽³⁾		V _{DD} - 2		V _{DD} - 1.7	V
V _{SWING}	Peak-to-Peak Output Voltage Swing		0.65		0.9	V

NOTES:

1. For single-ended applications, the max. input voltage for PCLK / xPCLK is V_{DD} + 0.3V.
2. Common mode voltage is defined as V_{IH}.
3. Outputs terminated with 50Ω to V_{DD} - 0.2V.

AC ELECTRICAL CHARACTERISTICS - COMMERCIAL

All parameters measured at 500MHz unless noted otherwise;
Cycle-to-cycle jitter = jitter on output; the part does not add jitter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F _{MAX}	Output Frequency				650	MHz
t _{PD}	Propagation Delay ⁽¹⁾	CLK, xCLK PCLK, xPCLK	f ≤ 650MHz	1	1.7	ns
t _{sk(o)}	Output Skew ^(2,4)				60	ps
t _{sk(b)}	Bank Skew ⁽⁴⁾	Bank A Bank B			20 35	ps
t _{sk(pp)}	Part-to-Part Skew ^(3,4)				200	ps
t _r	Output Rise Time	20 - 80% @ 50MHz	300		700	ps
t _f	Output Fall Time	20 - 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

NOTES:

1. Measured from the differential input crossingpoint to the differential output crossingpoint.
2. Defined as skew between outputs as the same supply voltage and with equal load conditions. Measured at the output differential crosspoints
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
4. This parameter is defined in accordance with JEDEC Standard 65.

POWER SUPPLY CHARACTERISTICS - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I _{EE}	Power Supply Current		—	—	55	mA

DC ELECTRICAL CHARACTERISTICS, LVCMOS / LVTTTL - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{IH}	CLK_EN, CLK_SEL, MR		2		V _{DD} + 0.3	V
V _{IL}	CLK_EN, CLK_SEL, MR		-0.3		0.8	V
I _{IH}	Input Current HIGH	CLK_EN CLK_SEL, MR	V _{IN} = V _{DD} = 3.465V		5 150	μA
I _{IL}	Input Current LOW	CLK_EN CLK_SEL, MR	V _{IN} = 0V, V _{DD} = 3.465V	-150		μA
			V _{IN} = 0V, V _{DD} = 3.465V	-5		

DC ELECTRICAL CHARACTERISTICS, DIFFERENTIAL - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V _{CMR}	Common Mode Input Voltage ^(1,2)		V _{EE} + 0.5		V _{DD} - 0.85	V
I _{IH}	Input Current HIGH	xCLK CLK	V _{IN} = V _{DD} = 3.465V		5 150	μA
I _{IL}	Input Current LOW	xCLK CLK	V _{IN} = 0V, V _{DD} = 3.465V	-150		μA
			V _{IN} = 0V, V _{DD} = 3.465V	-5		

NOTES:

1. For single-ended applications, the max. input voltage for CLK / xCLK is V_{DD} + 0.3V.
2. Common mode voltage is defined as V_{IH}.

DC ELECTRICAL CHARACTERISTICS, LVPECL- INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{IH}	Input Current HIGH	PCLK	V _{IN} = V _{DD} = 3.465V		5	μA
		xPCLK	V _{IN} = V _{DD} = 3.465V		150	
I _{IL}	Input Current LOW	PCLK	V _{IN} = 0V, V _{DD} = 3.465V	-150		μA
		xPCLK	V _{IN} = 0V, V _{DD} = 3.465V	-5		
V _{PP}	Peak-to-Peak Input Voltage		0.3		1	V
V _{CMR}	Common Mode Input Voltage ^(1,2)		V _{EE} + 1.5		V _{DD}	V
V _{OH}	Output Voltage HIGH ⁽³⁾		V _{DD} - 1.4		V _{DD} - 1	V
V _{OL}	Output Voltage LOW ⁽³⁾		V _{DD} - 2		V _{DD} - 1.7	V
V _{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.9	V

NOTES:

1. For single-ended applications, the max. input voltage for PCLK / xPCLK is V_{DD} + 0.3V.
2. Common mode voltage is defined as V_{IH}.
3. Outputs terminated with 50Ω to V_{DD} - 0.2V.

AC ELECTRICAL CHARACTERISTICS - INDUSTRIAL

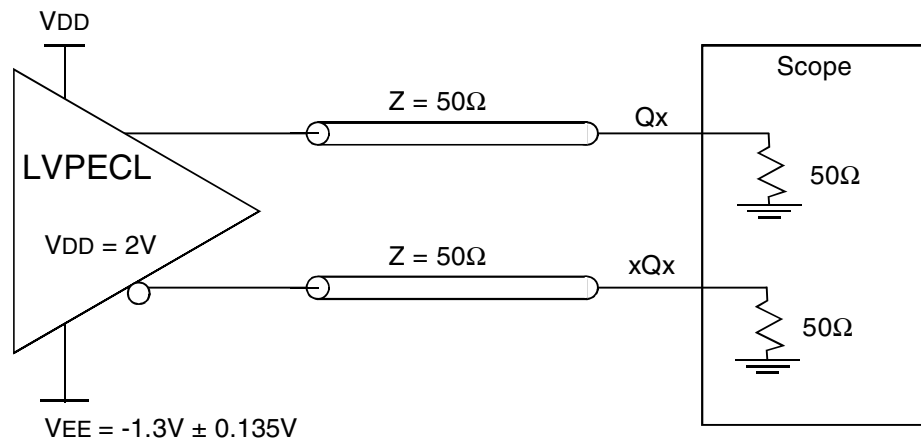
All parameters measured at 500MHz unless noted otherwise;
 cycle-to-cycle jitter = jitter on output; the part does not add jitter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
F _{MAX}	Output Frequency				650	MHz	
t _{PD}	Propagation Delay ⁽¹⁾	CLK, xCLK	f ≤ 650MHz	1		1.8	ns
		PCLK, xPCLK		1		1.7	
t _{SK(O)}	Output Skew ^(2,4)				75	ps	
t _{SK(B)}	Bank Skew ⁽⁴⁾	Bank A			30	ps	
		Bank B			45		
t _{SK(PP)}	Part-to-Part Skew ^(3,4)				300	ps	
t _r	Output Rise Time	20 - 80% @ 50MHz	300		700	ps	
t _f	Output Fall Time	20 - 80% @ 50MHz	300		700	ps	
odc	Output Duty Cycle		47	50	53	%	

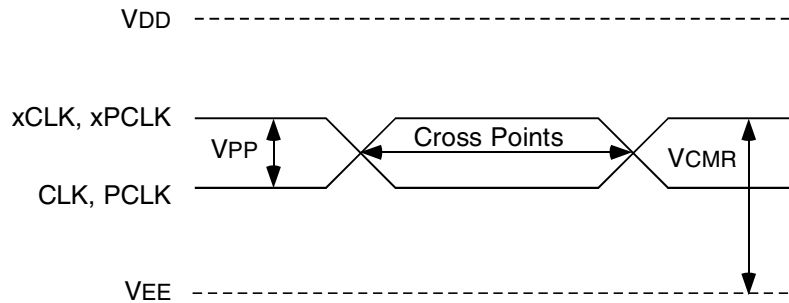
NOTES:

1. Measured from the differential input crossingpoint to the differential output crossingpoint.
2. Defined as skew between outputs as the same supply voltage and with equal load conditions. Measured at the output differential crosspoints
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
4. This parameter is defined in accordance with JEDEC Standard 65.

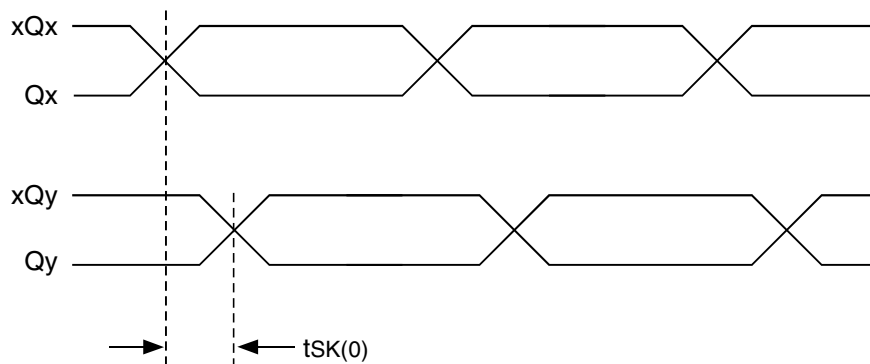
PARAMETER MEASUREMENT INFORMATION



Output Load Test Circuit

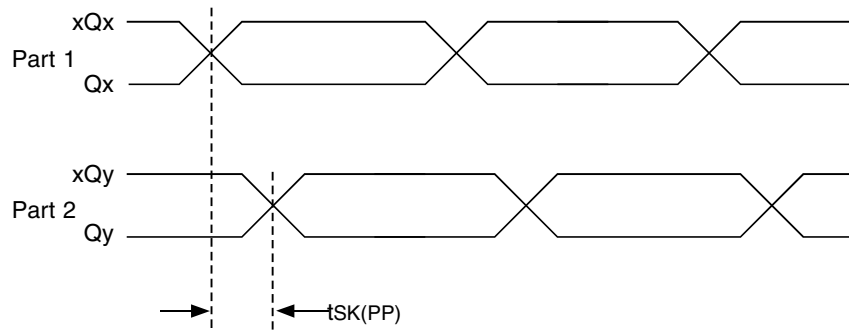


Differential Input Level

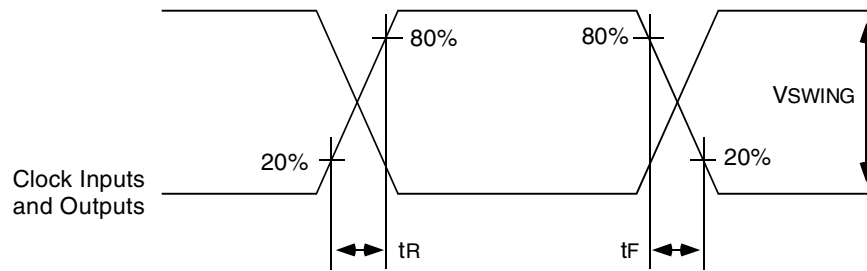


Output Skew

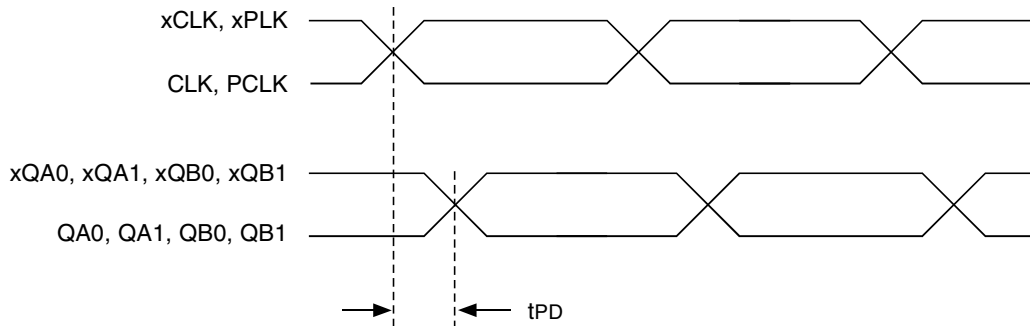
PARAMETER MEASUREMENT INFORMATION - CONTINUED



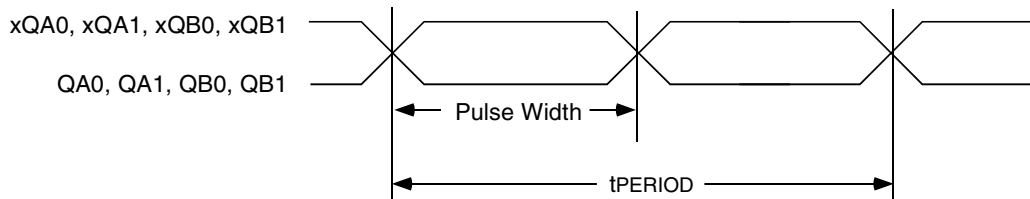
Part-to-Part Skew



Input and Output Rise and Fall Time



Propagation Delay



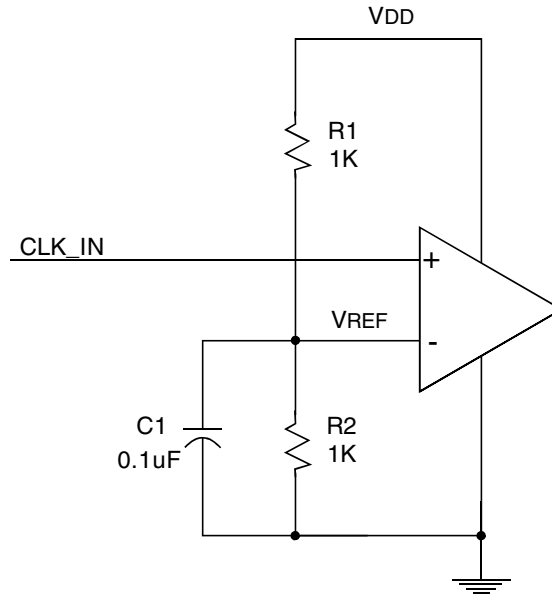
$$odc = \frac{t_w}{t_{PERIOD}}$$

odc and tPERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE-ENDED LEVELS

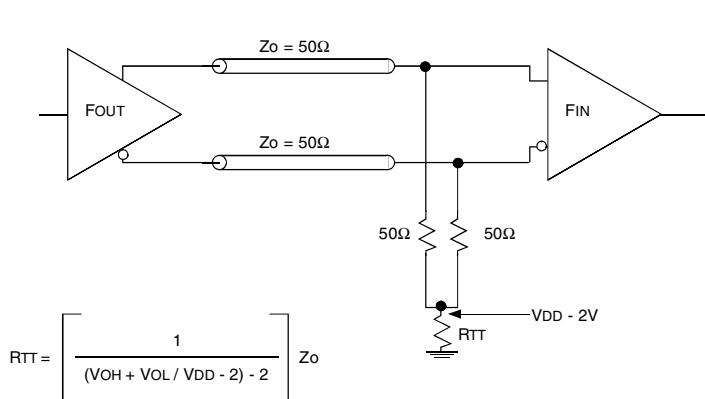
The diagram below shows how the differential input can be wired to accept single-ended levels. The reference voltage $V_{REF} \approx V_{DD}/2$ is generated by the bias resistors R1, R2, and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.



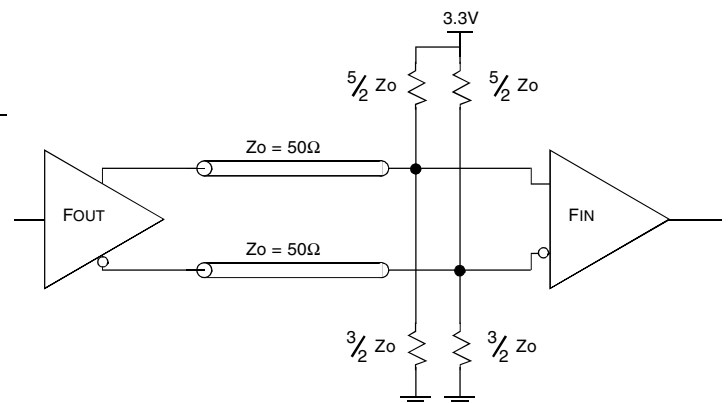
Single-Ended Signal Driving Differential Input

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. F_{OUT} and xF_{OUT} are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. The diagrams below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist. It is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



LVPECL Output Termination, layout A



LVPECL Output Termination, layout B

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the IDT8737-11. Equations and example calculations are also provided.

POWER DISSIPATION:

The total power dissipation for the IDT8737-11 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for the $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results. Please refer to the following section, **Calculations and Equations**, for details on calculating power dissipated in the load.

$$\text{Power (core)}_{MAX} = V_{DD_MAX} * I_{CC_MAX} = 3.465 * 55mA = 190.57mW$$

$$\text{Power (outputs)}_{MAX} = 30.2mW/\text{Loaded Output Pair}$$

$$\text{If all outputs are loaded, the total power is } 4 * 30.2mW = 120.8mW$$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 190.57mW + 120.8mW = 311.37mW$$

JUNCTION TEMPERATURE:

Junction temperature (t_J) is the temperature at the junction of the bond wire and bond pad. It directly affects the reliability of the device. The maximum recommended junction temperature for this device is 125°C.

$$\text{The equation for } t_J \text{ is as follows: } t_J = \theta_{JA} * Pd_{total} + T_A$$

t_J = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in **Power Dissipation**, above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance (θ_{JA}) must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 77.6°C/W per the following **Thermal Resistance** table. Therefore, t_J for an ambient temperature of 85°C with all its outputs switching is:

$$85^\circ C + 0.311W * 77.6^\circ C/W = 109.16^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

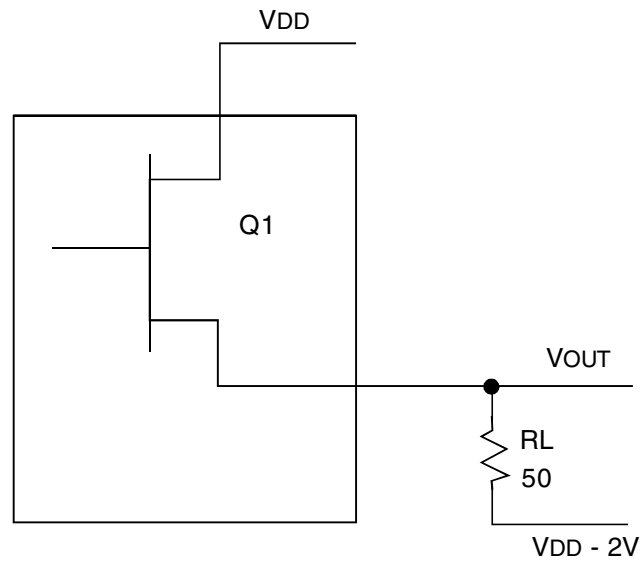
This calculation is only an example. t_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single-layer or multi-layer).

THERMAL RESISTANCE

θ_{JA} for 20-pin TSSOP, forced convection

θ_{JA} by Velocity (Linear Feet per minute)				
	0	200	400	Unit
Multi-Layer PCB, JEDEC Standard Test boards	92.6	77.6	70.9	°C/W

CALCULATIONS AND EQUATIONS



LVPECL Output Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations, which assume a 50Ω load and a termination voltage of $V_{DD} - 2V$.

For Logic HIGH: $V_{OUT} = V_{OH_MAX} = V_{DD_MAX} - 1V$.
 $(V_{DD_MAX} - V_{OH_MAX}) = 1V$

For Logic LOW: $V_{OUT} = V_{OL_MAX} = V_{DD_MAX} - 1.7V$.
 $(V_{DD_MAX} - V_{OL_MAX}) = 1.7V$

Pd_H is power dissipation when the output drives HIGH.

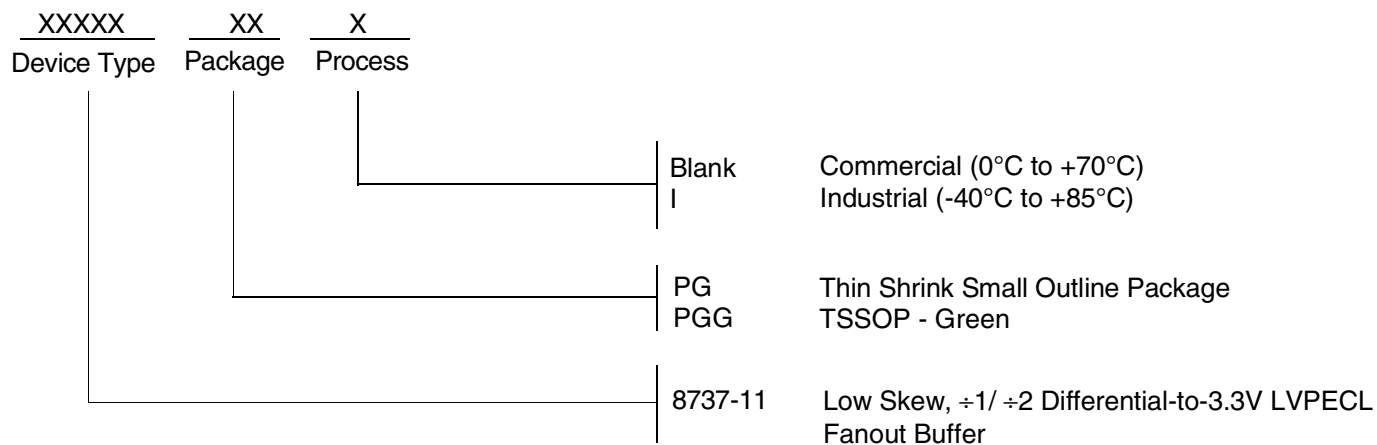
Pd_L is power dissipation when the output drives LOW.

$$Pd_H = \left\{ \frac{V_{OH_MAX} - (V_{DD_MAX} - 2V)}{R_L} \right\} * (V_{DD_MAX} - V_{OH_MAX}) = \left\{ \frac{2V - (V_{DD_MAX} - V_{OH_MAX})}{R_L} \right\} * (V_{DD_MAX} - V_{OH_MAX}) = \left[\frac{(2V - 1V)}{50\Omega} \right] * 1V = 20mW.$$

$$Pd_L = \left\{ \frac{V_{OL_MAX} - (V_{DD_MAX} - 2V)}{R_L} \right\} * (V_{DD_MAX} - V_{OL_MAX}) = \left\{ \frac{2V - (V_{DD_MAX} - V_{OL_MAX})}{R_L} \right\} * (V_{DD_MAX} - V_{OL_MAX}) = \left[\frac{(2V - 1.7V)}{50\Omega} \right] * 1.7V = 10.2mW.$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30.2mW$$

ORDERING INFORMATION



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