



### GENERAL DESCRIPTION



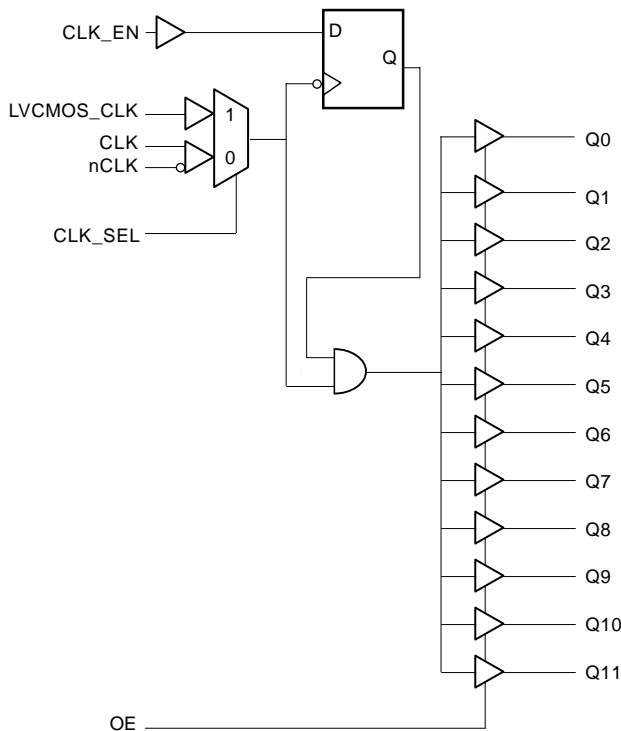
The ICS83948I-01 is a low skew, 1-to-12 Differential-to-LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83948I-01 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The LVCMOS\_CLK can accept LVCMOS or LVTTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83948I-01 is characterized at 3.3V core/3.3V output. Guaranteed output and part-to-part skew characteristics make the ICS83948I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

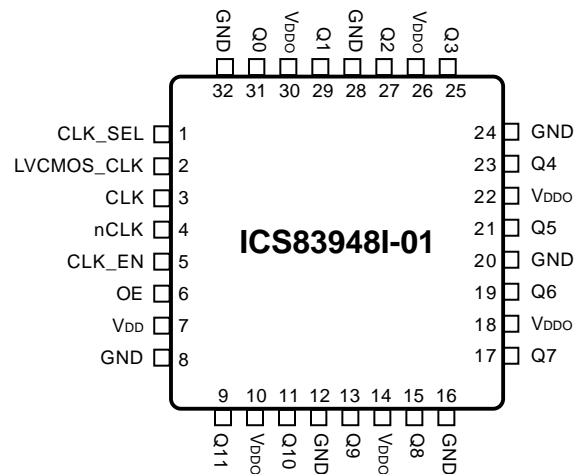
### FEATURES

- 12 LVCMOS outputs
- Selectable LVCMOS clock or differential CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- LVCMOS\_CLK accepts the following input levels: LVCMOS or LVTTTL
- Maximum output frequency: 150MHz
- Output skew: 350ps (maximum)
- Part to part skew: 1.5ns (maximum)
- 3.3V core, 3.3V output
- -40°C to 85°C ambient operating temperature
- Pin compatible with the MPC948/948L

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**32-Lead LQFP**  
7mm x 7mm x 1.4mm package body  
**Y Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

| Number   | Name   | Type   |          | Description  |
|--|--|--------|----------|--|
| 1  | CLK_SEL  | Input  | Pullup   | Clock select input. Selects LVCMOS clock input when HIGH. Selects CLK, nCLK inputs when LOW. LVCMOS / LVTTTL interface levels. |
| 2  | LVCMOS_CLK   | Input  | Pullup   | Clock input. LVCMOS / LVTTTL interface levels.   |
| 3  | CLK  | Input  | Pullup   | Non-inverting differential clock input.  |
| 4  | nCLK   | Input  | Pulldown | Inverting differential clock input.  |
| 5  | CLK_EN   | Input  | Pullup   | Clock enable. LVCMOS / LVTTTL interface levels.  |
| 6  | OE   | Input  | Pullup   | Output enable. LVCMOS / LVTTTL interface levels.   |
| 7  | V <sub>DD</sub>  | Power  |          | Core supply pin.   |
| 8, 12, 16,<br>20, 24, 28, 32                       | GND  | Power  |          | Power supply ground.   |
| 9, 11, 13, 15,<br>17, 19, 21, 23<br>25, 27, 29, 31 | Q11, Q10, Q9, Q8,<br>Q7, Q6, Q5, Q4,<br>Q3, Q2, Q1, Q0 | Output |          | Clock outputs. LVCMOS / LVTTTL interface levels.   |
| 10, 14, 18, 22, 26, 30                             | V <sub>DDO</sub>                                       | Power  |          | Output supply pins.  |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter                                  | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                          |                 |         |         | 4       | pF    |
| C <sub>PD</sub>       | Power Dissipation Capacitance (per output) |                 |         | 25      |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                      |                 |         | 51      |         | KΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                    |                 |         | 51      |         | KΩ    |
| R <sub>OUT</sub>      | Output Impedance                           |                 |         | 7       |         | Ω     |

**TABLE 3A. CLOCK SELECT FUNCTION TABLE**

| Control Input | Clock       |             |
|---------------|-------------|-------------|
| CLK_SEL       | CLK, nCLK   | LVCMOS_CLK  |
| 0             | Selected    | De-selected |
| 1             | De-selected | Selected    |

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

| Inputs  |            |                |                | Outputs | Input to Output Mode         | Polarity      |
|---------|------------|----------------|----------------|---------|------------------------------|---------------|
| CLK_SEL | LVCMOS_CLK | CLK            | nCLK           | Q0:Q12  |                              |               |
| 0       | —          | 0              | 1              | LOW     | Differential to Single Ended | Non Inverting |
| 0       | —          | 1              | 0              | HIGH    | Differential to Single Ended | Non Inverting |
| 0       | —          | 0              | Biased; NOTE 1 | LOW     | Single Ended to Single Ended | Non Inverting |
| 0       | —          | 1              | Biased; NOTE 1 | HIGH    | Single Ended to Single Ended | Non Inverting |
| 0       | —          | Biased; NOTE 1 | 0              | HIGH    | Single Ended to Single Ended | Inverting     |
| 0       | —          | Biased; NOTE 1 | 1              | LOW     | Single Ended to Single Ended | Inverting     |
| 1       | 0          | —              | —              | LOW     | Single Ended to Single Ended | Non Inverting |
| 1       | 1          | —              | —              | HIGH    | Single Ended to Single Ended | Non Inverting |

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".



**ABSOLUTE MAXIMUM RATINGS**

|  |                           |
|--|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm)         |
| Storage Temperature, $T_{stg}$           | -65°C to 150°C            |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

| Symbol    | Parameter                | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Input Supply Voltage     |                 | 3.0     | 3.3     | 3.6     | V     |
| $V_{DDO}$ | Output Supply Voltage    |                 | 3.0     | 3.3     | 3.6     | V     |
| $I_{DD}$  | Quiescent Supply Current |                 |         |         | 55      | mA    |

**TABLE 4B. DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

| Symbol    | Parameter                               | Test Conditions  | Minimum   | Typical | Maximum         | Units   |
|-----------|---|------------------|-----------|---------|-----------------|---------|
| $V_{IH}$  | Input High Voltage                      | LVCMOS/LVTTL     | 2         |         | 3.6             | V       |
| $V_{IL}$  | Input Low Voltage                       | LVCMOS/LVTTL     |           |         | 0.8             | V       |
| $V_{PP}$  | Peak-to-Peak Input Voltage              | CLK, nCLK        | 0.15      |         | 1.3             | V       |
| $V_{CMR}$ | Input Common Mode Voltage;<br>NOTE 1, 2 | CLK, nCLK        | GND + 0.5 |         | $V_{DD} - 0.85$ | V       |
| $I_{IN}$  | Input Current                           |                  |           |         | $\pm 100$       | $\mu A$ |
| $V_{OH}$  | Output High Voltage                     | $I_{OH} = -20mA$ | 2.5       |         |                 | V       |
| $V_{OL}$  | Output Low Voltage                      | $I_{OL} = 20mA$  |           |         | 0.4             | V       |

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

| Symbol             | Parameter                             | Test Conditions                          | Minimum                                  | Typical | Maximum              | Units |
|--------------------|---------------------------------------|--|--|---------|----------------------|-------|
| $f_{MAX}$          | Maximum Output Frequency              |  | 150                                      |         |                      | MHz   |
| $t_{PD}$           | Propagation Delay                     | CLK, nCLK;<br>NOTE 1A                    | 2.5                                      |         | 6.5                  | ns    |
|                    |                                       | LVCMOS_CLK;<br>NOTE 1B                   | 3  |         | 5.5                  | ns    |
| $t_{sk(o)}$        | Output Skew; NOTE 2, 6                | Measured on<br>rising edge @ $V_{DDO}/2$ |  |         | 350                  | ps    |
| $t_{sk(pp)}$       | Part-to-Part Skew;<br>NOTE 3, 6       | CLK, nCLK                                | Measured on<br>rising edge @ $V_{DDO}/2$ |         | 1.5                  | ns    |
|                    |                                       | LVCMOS_CLK                               |  |         | 2                    | ns    |
| $t_R$              | Output Rise Time                      | 0.8V to 2V                               | 0.2                                      |         | 1.0                  | ns    |
| $t_F$              | Output Fall Time                      | 0.8V to 2V                               | 0.2                                      |         | 1.0                  | ns    |
| $t_{PW}$           | Output Pulse Width                    |  | $t_{Period}/2 - 800$                     |         | $t_{Period}/2 + 800$ | ps    |
| $t_{PZL}, t_{PZH}$ | Output Disable Time; NOTE 4           |  |  |         | 11                   | ns    |
| $t_{PLZ}, t_{PHZ}$ | Output Enable Time; NOTE 4            |  |  |         | 11                   | ns    |
| $t_S$              | Clock Enable<br>Setup Time;<br>NOTE 5 | CLK_EN to<br>CLK                         | 1  |         |                      | ns    |
|                    |                                       | CLK_EN to<br>LVCMOS_CLK                  | 0  |         |                      | ns    |
| $t_H$              | Clock Enable<br>Hold Time;<br>NOTE 5  | CLK to<br>CLK_EN                         | 0  |         |                      | ns    |
|                    |                                       | LVCMOS_CLK<br>to CLK_EN                  | 1  |         |                      | ns    |

NOTE 1A: Measured from the differential input crossing point to  $V_{DDO}/2$  of the output.

NOTE 1B: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.  
Measured at  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

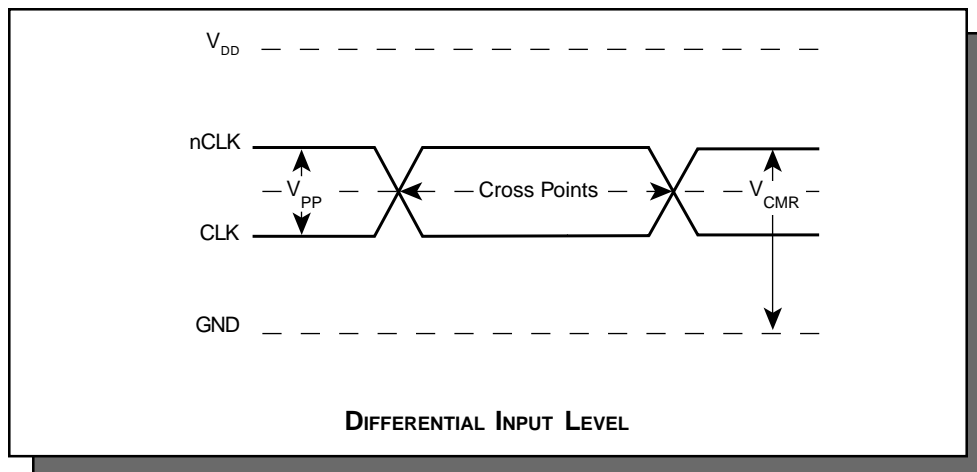
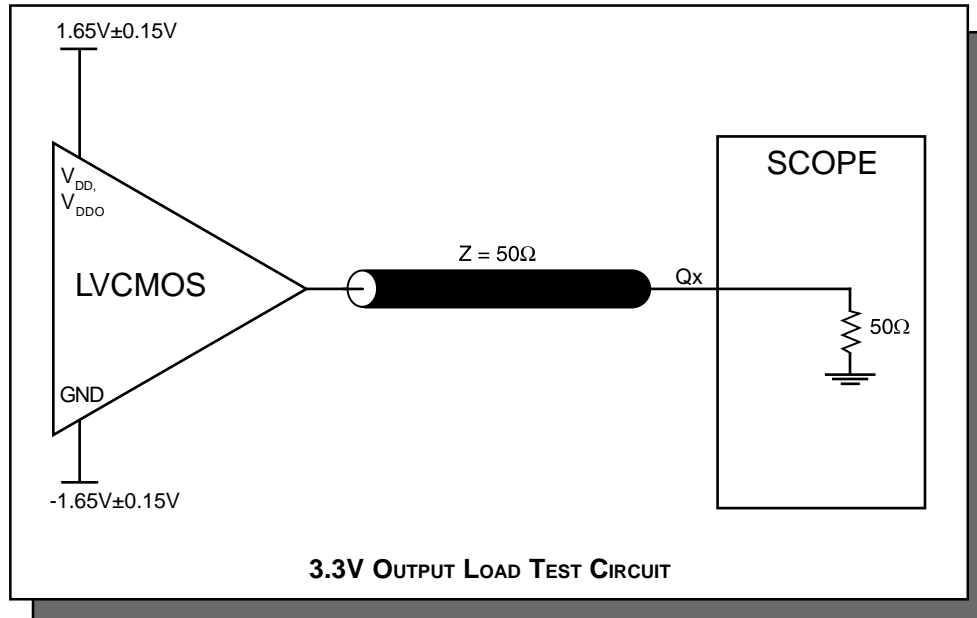
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

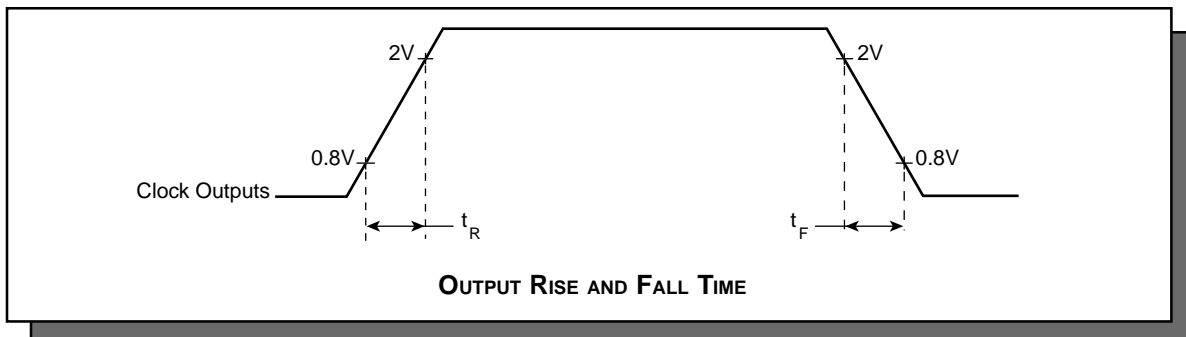
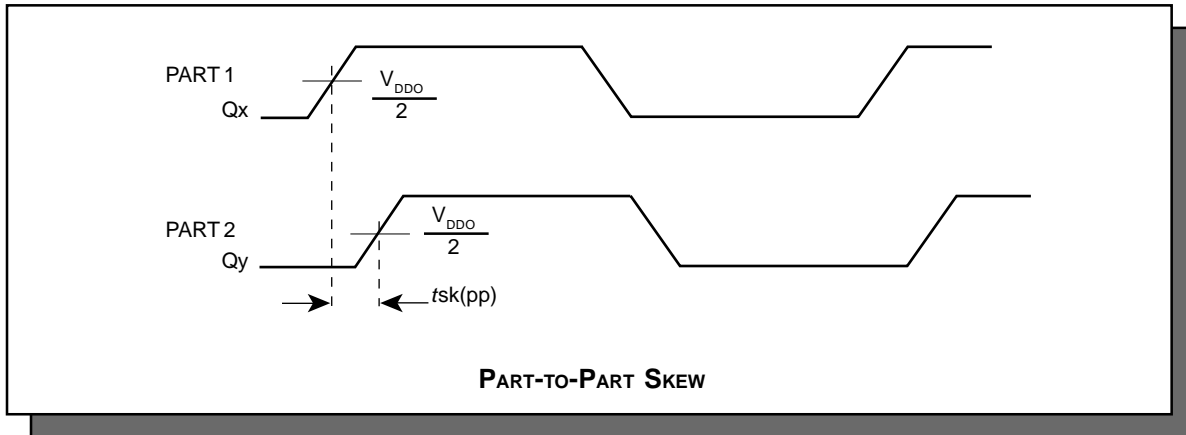
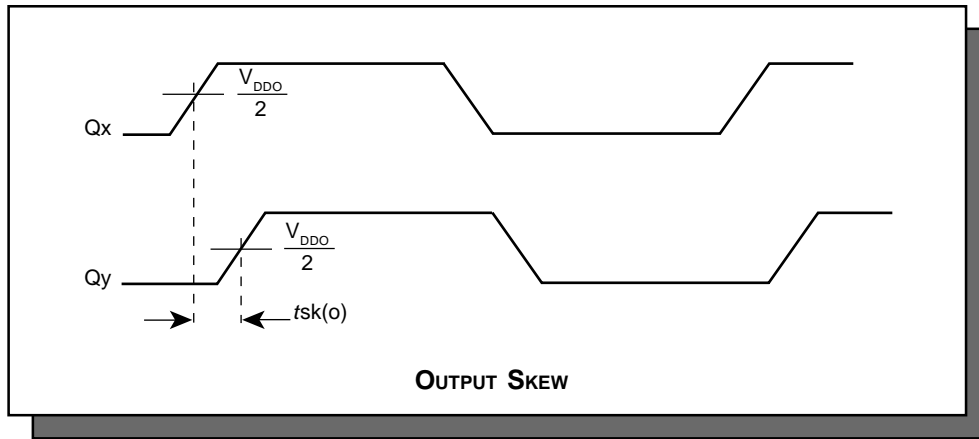
NOTE 5: Setup and Hold times are relative to the falling edge of the input clock.

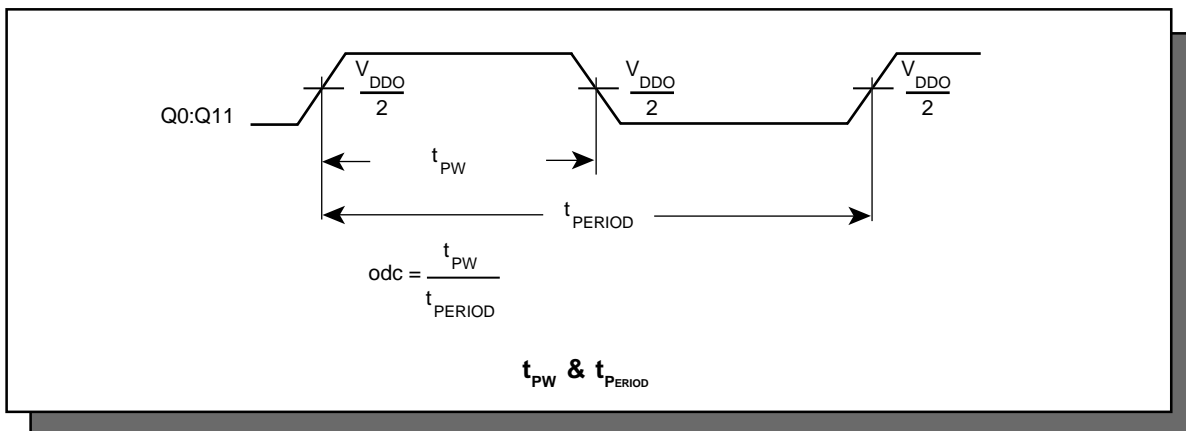
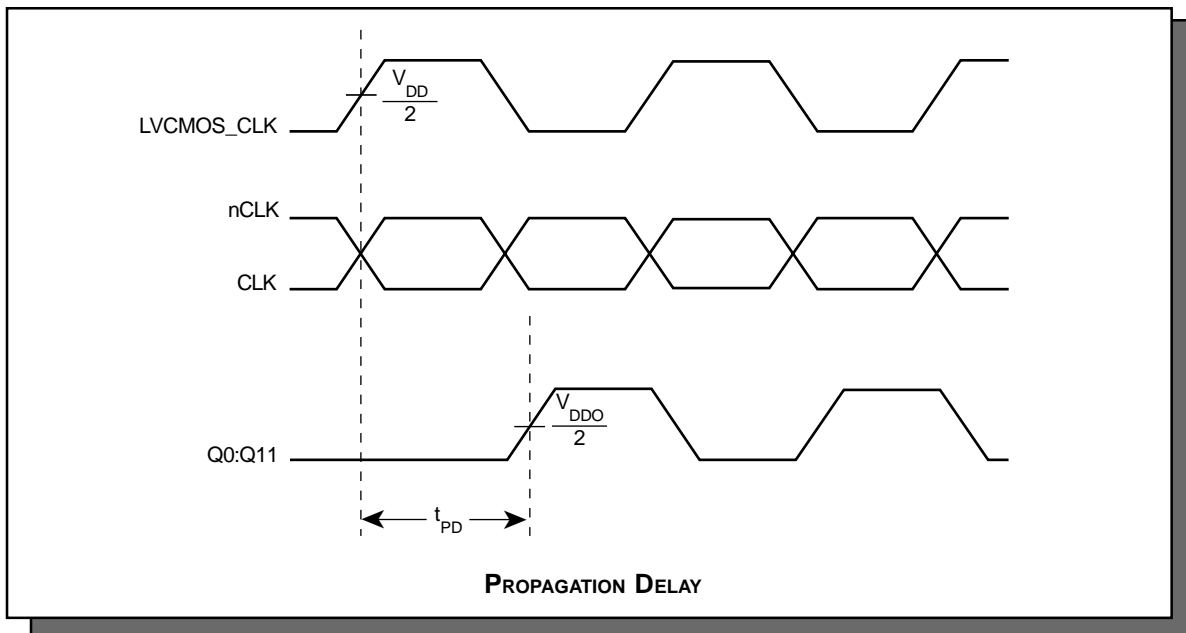
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.



## PARAMETER MEASUREMENT INFORMATION





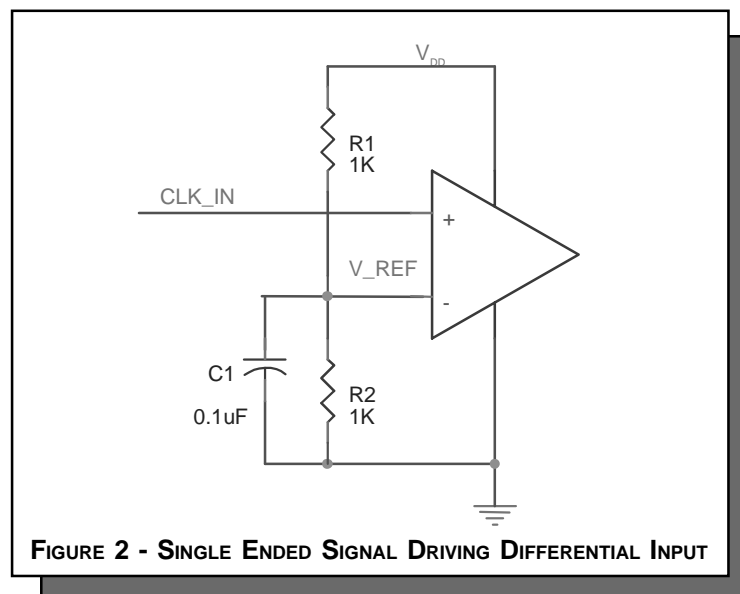




## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .







## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|--|----------|----------|----------|
|  | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS83948I-01 is: 1040



PACKAGE OUTLINE - Y SUFFIX

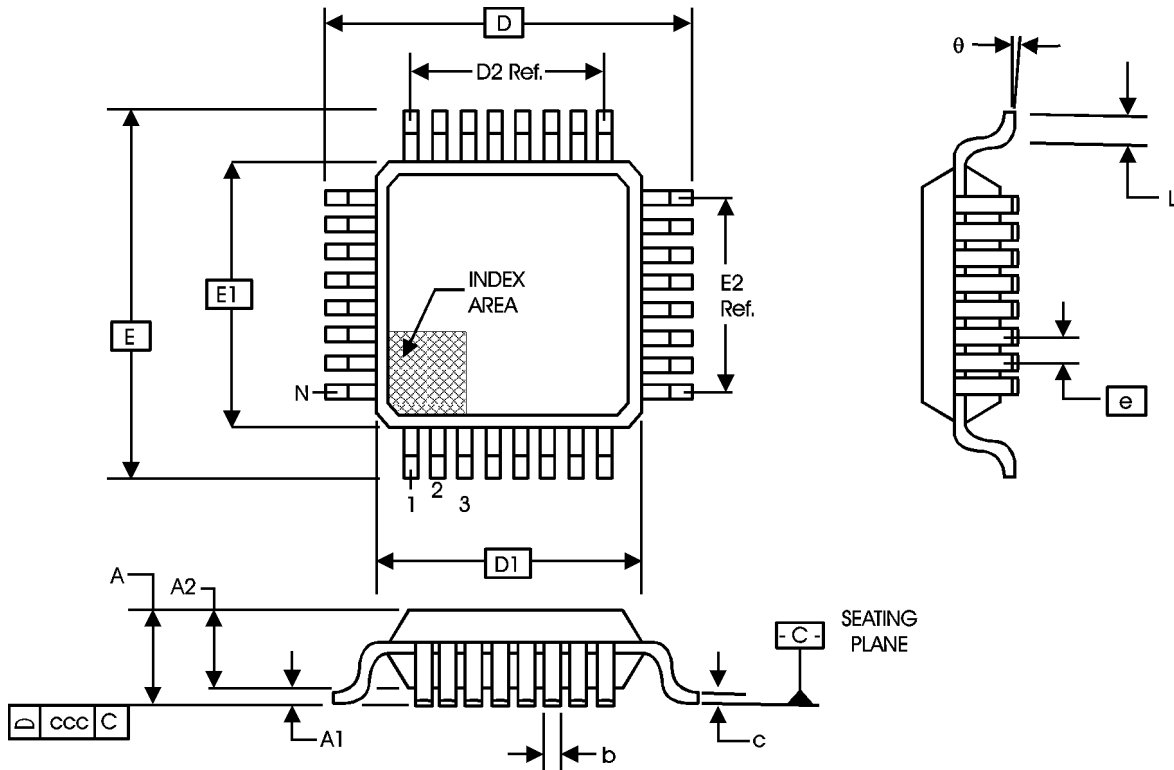


TABLE 7. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--|------------|---------|---------|
| SYMBOL   | BBA        |         |         |
|  | MINIMUM    | NOMINAL | MAXIMUM |
| N  | 32         |         |         |
| A  | --         | --      | 1.60    |
| A1   | 0.05       | --      | 0.15    |
| A2   | 1.35       | 1.40    | 1.45    |
| b  | 0.30       | 0.37    | 0.45    |
| c  | 0.09       | --      | 0.20    |
| D  | 9.00 BASIC |         |         |
| D1   | 7.00 BASIC |         |         |
| D2   | 5.60 Ref.  |         |         |
| E  | 9.00 BASIC |         |         |
| E1   | 7.00 BASIC |         |         |
| E2   | 5.60 Ref.  |         |         |
| e  | 0.80 BASIC |         |         |
| L  | 0.45       | 0.60    | 0.75    |
| theta  | 0°         | --      | 7°      |
| ccc  | --         | --      | 0.10    |

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MS-026



Integrated  
Circuit  
Systems, Inc.

**ICS83948I-01**  
LOW SKEW, 1-TO-12  
DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking       | Package                       | Count        | Temperature   |
|-------------------|---------------|-------------------------------|--------------|---------------|
| 83948AYI-01       | ICS83948AYI01 | 32 Lead LQFP                  | 250 per tray | -40°C to 85°C |
| 83948AYI-01T      | ICS83948AYI01 | 32 Lead LQFP on Tape and Reel | 1000         | -40°C to 85°C |

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